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1988/1989 CMOS
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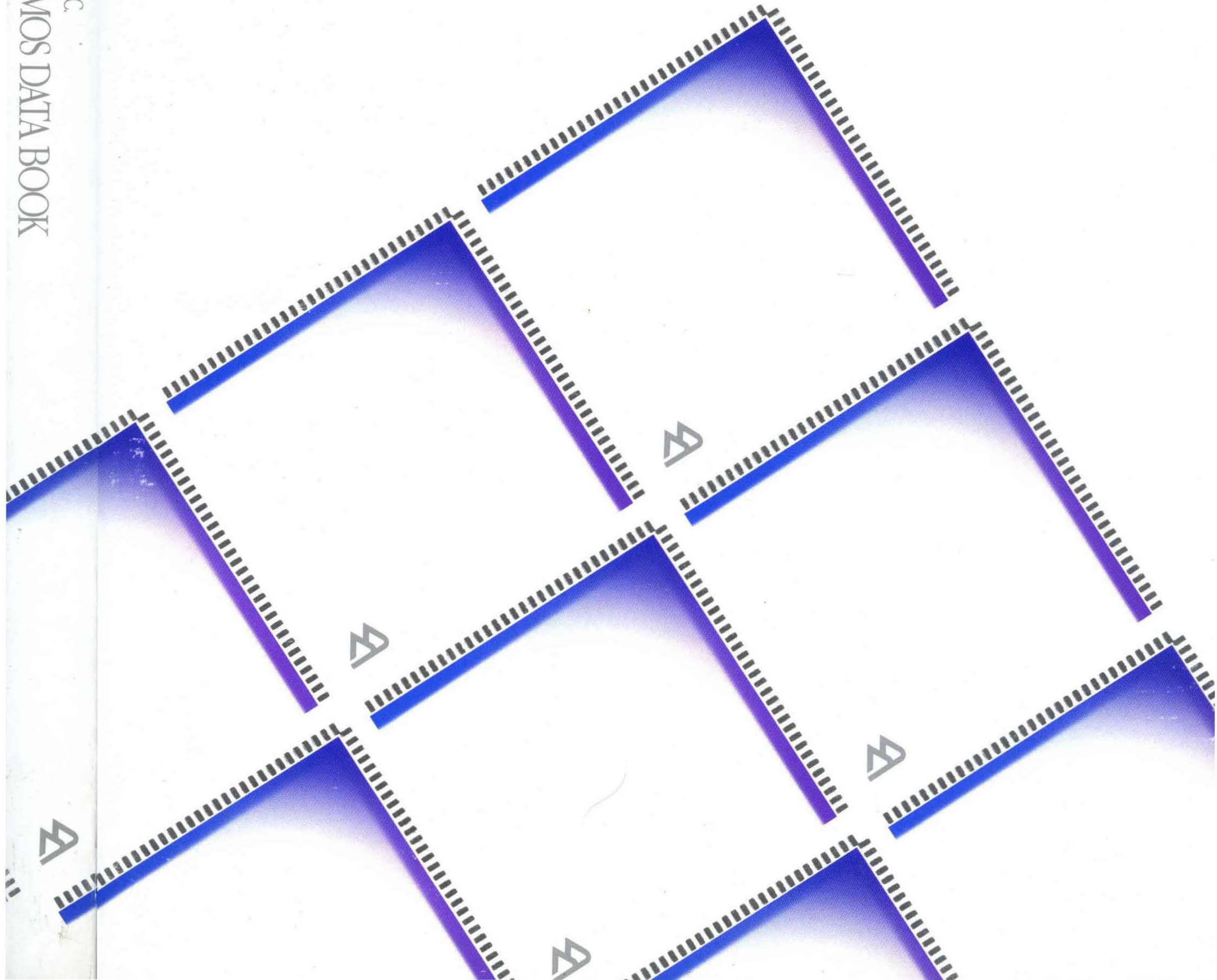

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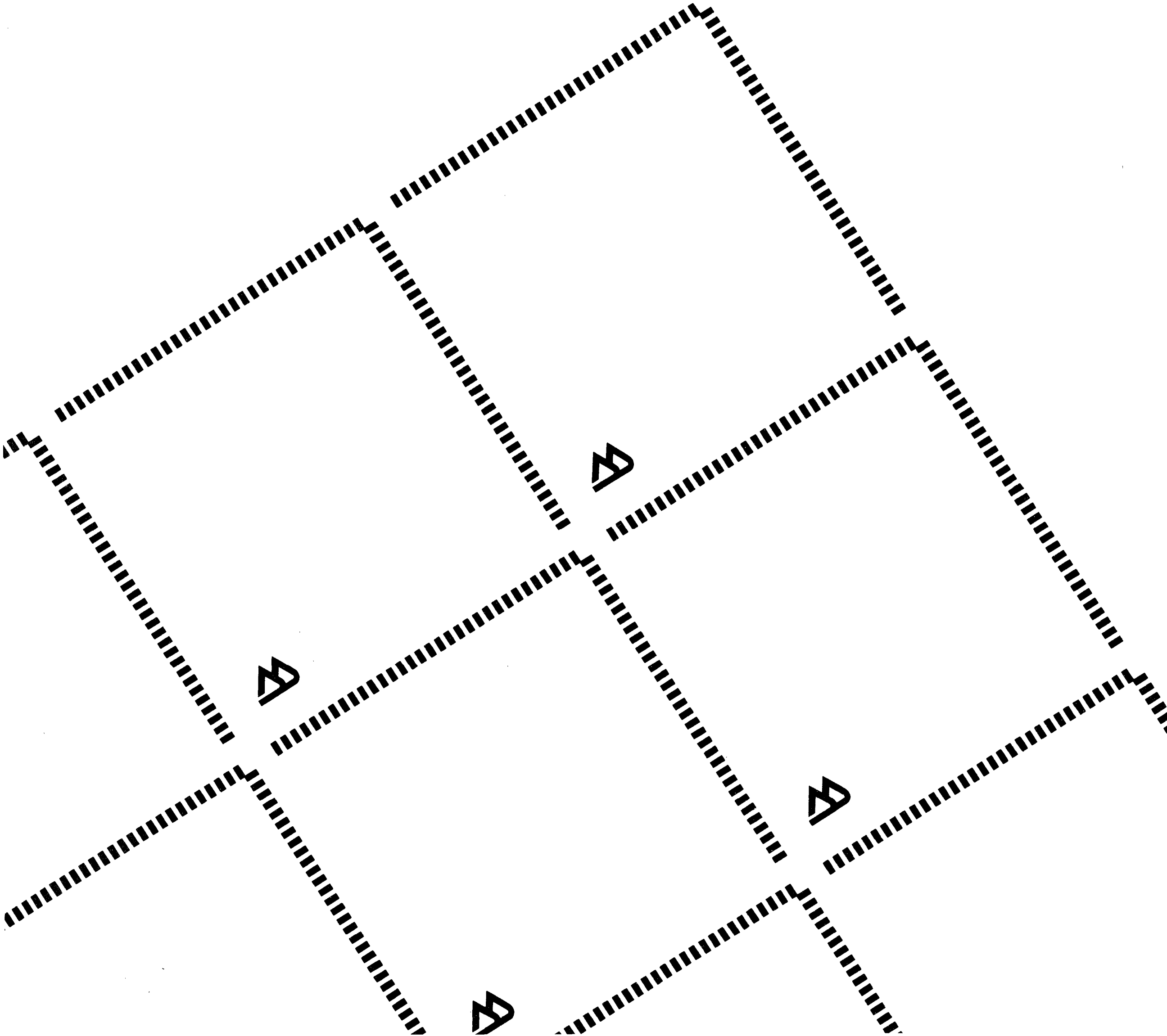


High-Performance CMOS Products for the Low-Power CMOS System

S-MOS Systems offers the best of both worlds: American product direction and engineering, backed by one of the largest and most automated all-CMOS factories in the world.

S-MOS was formed in 1983 to provide American and Canadian companies with the dedicated, localized service that would match such exceptional manufacturing capability.

As a result, S-MOS provides advanced CMOS products at competitive prices, and customers are supported by a cooperative long-term relationship that ensures satisfaction.

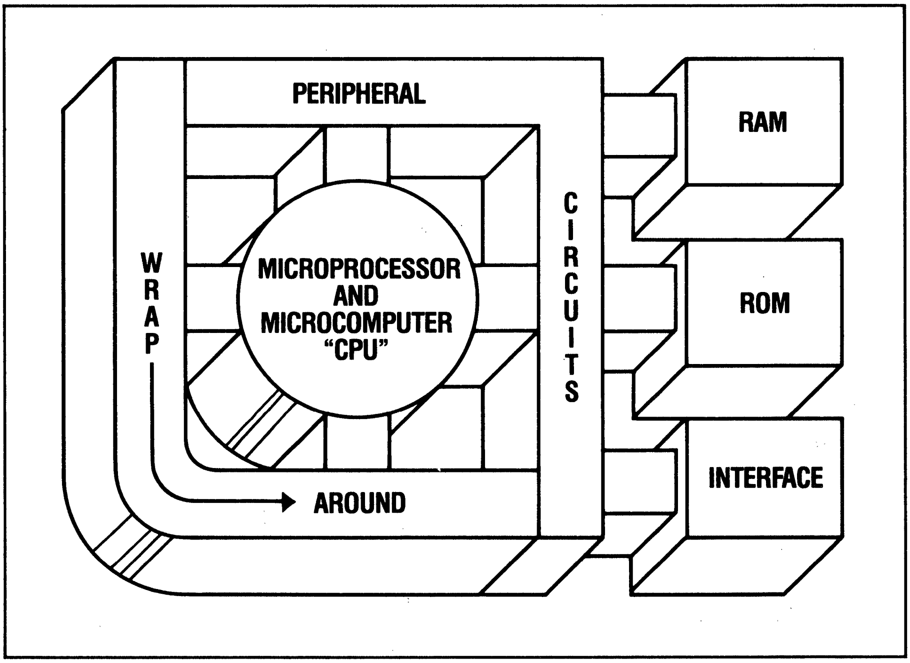
With S-MOS, you can take advantage of the high performance and low power requirements that make CMOS LSI and VLSI products so desirable. As CMOS specialists, we deliver high-quality single-chip microcomputers, peripherals, RAMs, ROMs, interface circuits, gate arrays, standard cell and compiled cell products.

Our manufacturing affiliate, Seiko Epson Corp., is one of the world's most advanced CMOS IC manufacturers. With 17 years of CMOS experience, Seiko Epson Corp. is part of the Seiko Group, famous for Seiko and Epson products.

Use of automated wafer fabrication and robotic manufacturing techniques and equipment contribute to our consistantly high throughput, and low reject rates. Our factory is currently capable of producing 40,000 four-inch (3 um), 20,000 five-inch (1.5 um) and 20,000 six-inch (1.2 um) wafers per month with a product reject rate of less than .0001%.

Our rapidly evolving process technology has made S-MOS/Seiko Epson one of the most advanced semiconductor suppliers in the world.

S-MOS also provides foundry services for OEMs and design houses. (Consult S-MOS Foundry Services Department for details.)



S-MOS takes a system approach to CMOS technology, providing the building blocks for a 100% CMOS system.

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S-MOS Systems, Inc. reserves the right to make changes in circuit design specifications and other information at any time without prior written notice.

1988/1989 CMOS DATA BOOK

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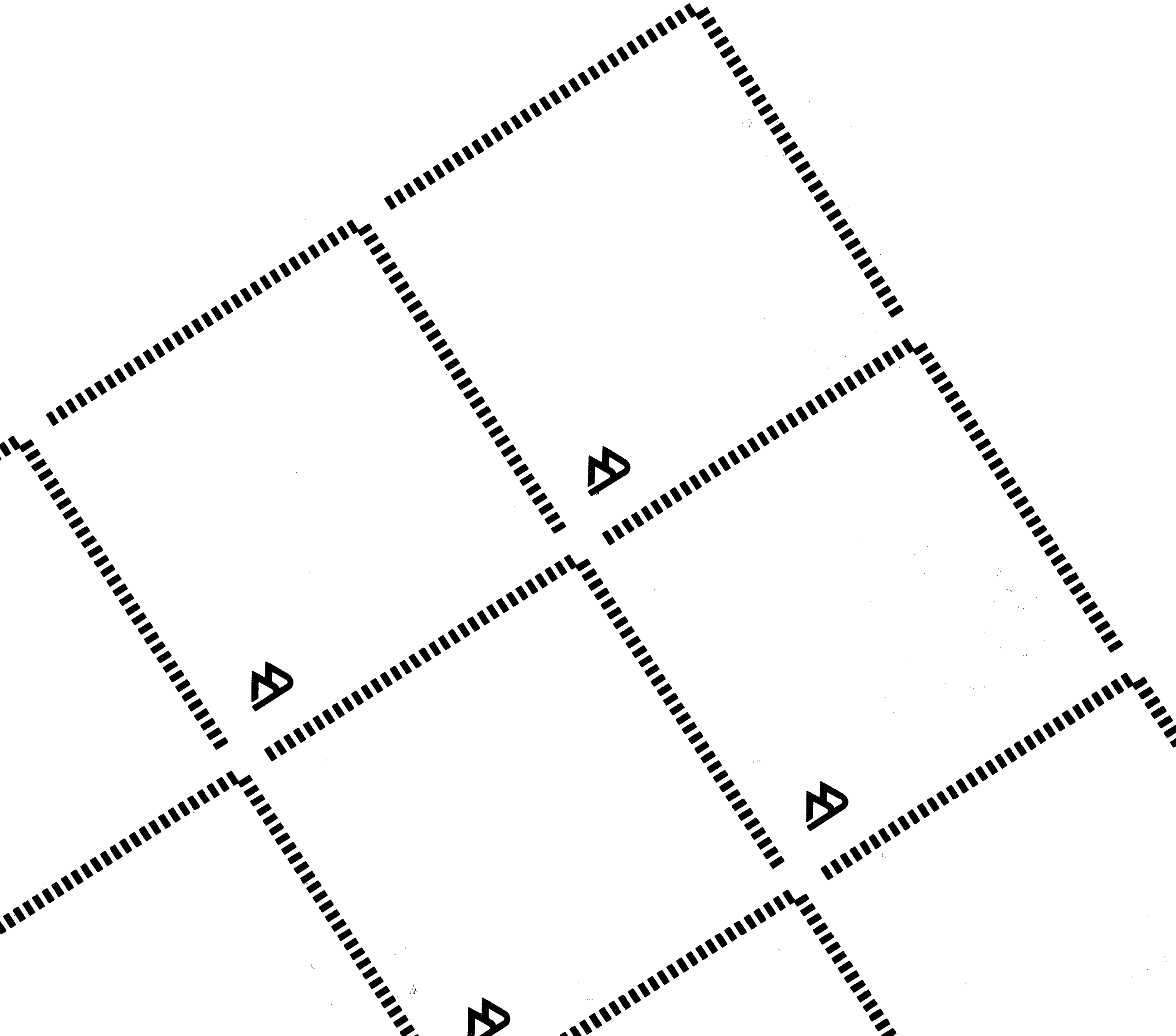


1. OUTLINE OF PRODUCTS

1.1 Product Code

The name assigned to each product is coded to indicate its function and package type.

Example : SRM2016C○○

S RM 2016 C ○○

- S-MOS SYSTEMS, INC.
- Abbreviation of Function
  (RM means RAM)
  (Please refer to Item 1.2)
- Product Number
- Package Code :
  C : Plastic DIP
  D : Die Form (Chip)
  F : Plastic QFP
  L : Ceramic QFP
  H : CERDIP, Ceramic DIP
  M : Plastic SOP
  J : PLCC, SOJ
  G : Plastic PGA
  P : Ceramic PGA
  S : Plastic Shrink DIP
  N : Plastic Skinny DIP
  Y : SOT
- Sub-Code :
  The Sub-Code can be used in any of three different ways :
  (a) As the User Code for Semi-Custom LSIs
  (b) As a Number to Distinguish Between Different Versions of the Same Product [i. e. 12, 15, or 20 to represent 120, 150 and 200 ns respectively] .
  (c) Revision of Product Features

1.2 S-MOS Product Prefix Guide

1.2.1 Standard & Semi Custom CMOS LSIs for Industry

Gate Array	Logic Array	SLA	Series
Standard Cell	Standard Cell	SSC	Series
Static RAM	Random Access Memory	SRM	Series
Mask ROM	Mask Programmed Memory	SMM	Series
Single-chip Microcomputer Microprocessor Peripheral	Microcomputer, CPU & Peripheral	SMC	Series
LCD Driver Thermal Head Driver VFD/PDP Driver Control LSI of Equipment	Electric Driver	SED	Series
Converter IC	Converter IC	SCI	Series
Telecommunication LSIs	Telecommunications	STC	Series
Image Sensor	Sensor	SEA	Series
Hybrid IC	Hybrid IC	SHB	Series
Module IC	Module	SEK	Series

1.2.2 Standard CMOS LSI for Consumers

IC for Watch and Clock	Time Piece	STP	Series
Single-chip Microcomputer	Microcomputer	SMC	Series
Melody IC	Melody	SVM	Series

1.2.3 Custom CMOS LSI

Low Voltage Operation IC	Device for Battery Operation
CMOS Linear IC	A/D • D/A Converter, PLL, VFO, SCF, etc.
High Voltage Operation IC	VFD/PDP Driver etc.
High Density Mounted IC	Hybrid LSI etc.

2. SPECIFICATIONS AND CHARACTERISTICS

2.1 Electrical Characteristics

To fully utilize the CMOS IC it is important to understand the circuit, its characteristics and its specifications. This chapter discusses the Absolute Maximum Ratings, the Recommended Operating Conditions and the Electrical Characteristics of CMOS integrated circuits.

Please note that the voltage value is based on a high level power supply (V_{DD}) or on a low level power supply (V_{SS}).

2.1.1 Absolute Maximum Ratings

The Absolute Maximum Ratings of a specification are the highest levels at which the circuit will safely operate. Exceeding this level may result in damage to, or destruction of, the circuit. It is, therefore, necessary to monitor such things as supply voltage, input voltage and the ambient temperature.

(1) Operating Voltage

This is the maximum voltage allowed at the power supply terminals. It is important not to let the voltage exceed the specification, not only in the stationary state, but also in the transient state, during power supply turn on, and includes noise on the power supply line. When the voltage exceeds the specification, it may cause some damage to the IC and may adversely effect its reliability.

(2) Input Voltage

This is the maximum voltage allowed into the input terminal. When voltage exceeding the specification is applied, the IC may lose functions because of damage to the input protection resistors or diodes.

(3) Output Current

This is the maximum value of current flow to or from the output. Generally, this is not specified for devices which have small output capacity. This value is provided for ICs, such as drivers which requires a large amount of current.

(4) Power Dissipation

This value shows the allowable dissipation for the device. It depends on the thermal characteristics of its package. For devices which must supply large amounts of output, this specifies the limitation of the output current.

(5) Operating Temperature

The ambient temperature range at which the IC will function reliably.

(6) Storage Temperature

The range of storage temperatures when no voltage is being applied on the IC. This is a very important factor, especially during air transportation.

(7) Soldering Temperature and Time

Maximum temperature and time allowed for soldering.

2.1.2 Recommended Operating Conditions

The Recommended Operating Conditions, such as supply voltage, input conditions, and external components, are the conditions necessary for the IC to function properly to meet the electrical characteristics. The operating conditions may be in the same column as the electrical characteristics.

2.1.3 Electrical Characteristics

AC and DC electrical characteristics are provided for each input pin and power supply pin. These characteristics are measured at either the ambient temperature specified or in the range of the operating temperatures specified under the worst conditions.

2.2 Symbol Definitions

SYMBOLS	PARAMETERS	EXPLANATION
C_D	Drain Capacitance	Static capacitance between output terminal and power supply terminal on the oscillation circuit.
C_G	Gate Capacitance	Static capacitance between input terminal and power supply terminal on the oscillation circuit.
C_I	Input Capacitance	Static capacitance between the input terminal and the power supply terminal.
$C_{I/O}$	Input/Output Capacitance	Static capacitance between the I/O terminal and the power supply terminal.
C_L	Loading Capacitance	Loading static capacitance for the external components
C_O	Output Capacitance	Static capacitance between the output terminal and the power supply terminal
f_{XXX}	XXX Frequency	XXX indicates either the function or the terminal name
f_{max}	Maximum Clock Frequency	Maximum Frequency input to the IC from an external pin
f_{CLK}	Clock Frequency	Clock Frequency input to the IC from an external pin
f_{OSC}	Oscillation Frequency	Oscillation Frequency
H	High level	Logical "H" level
I_{DD}	(V_{DD}) Supply Current	Supply current flows into the IC from the V_{DD} external terminal
I_{DDA}	Average Operating Current	Average supply current flows into the IC from the V_{DD} external terminal
I_{DDO}	Operating Supply Current	V_{DD} supply current while operating
I_{DDS}	Standby Supply Current	V_{DD} supply current while standby
I_I	Input Current	Current which flows to the input terminal
I_{LI}	Input Leakage Current	Leakage current which flows to the input terminal
I_{IH}	High Level Input Current	The input current at the "H" level input
I_{IL}	Low Level Input Current	The input current at the "L" level input
I_O	Output Current	Current which flows through the output terminal
I_{OH}	High Level Output Current	Output current when the output terminal voltage is V_{OH}
I_{OL}	Low Level Output Current	Output current when the output terminal voltage is V_{OL}
I_{LO}	Output Leakage Current	Leak current flowed when the power voltage is applied to the output terminal when in the 'off (high impedance)' condition
I_{SS}	(V_{SS}) Supply Current	Current flowed out of the V_{SS} terminal
L	Low Level	Logical "L" level
P_D	Power Dissipation	Allowable consumption of the electric power
R_I	Input Resistance	Built-in resistance for pulling up and pulling down the input
R_L	Loading Resistance	Loading resistance for the external components
T_a	Ambient Temperature	Ambient temperature of the IC
T_j	Junction Temperature	Junction temperature of the IC
T_{opr}	Operating Temperature	Surrounding temperature of the IC in operation
T_{stg}	Storage Temperature	Temperature of storage area the IC
T_{sol}	Soldering Temperature and Time	Soldering temperature and time

2.2 Symbol Definitions (cont.)

SYMBOLS	PARAMETERS	EXPLANATION
V_{DD}	(V_{DD}) Supply Voltage	Supply voltage or the operating voltage applied to the V_{DD} terminal
V_I	Input Voltage	Voltage applied to the input terminal
$V_{I/O}$	Input/Output Voltage	Voltage applied to the I/O terminal
V_{IH}	High Level Input Voltage	Input voltage which can be judged as "H" level
V_{IL}	Low Level Input Voltage	Input voltage which can be judged as "L" Level
V_O	Output Voltage	Voltage generated from or applied to the output terminal
V_{OH}	High Level Output Voltage	Voltage at the "H" level output
V_{OL}	Low Level Output Voltage	Voltage at the "L" level output
V_{rip}	Ripple Voltage	Ripple voltage Amplitude
V_{SS}	(V_{SS}) Supply Voltage	Supply voltage applied to the V_{SS} terminal
V_{SSn}	V_{SSn} Supply Voltage	N times pressurized power supply terminal or its voltage level
V_{STA}	Oscillation Start Voltage	Voltage for automatic starting
V_{STP}	Oscillation Stop Voltage	Voltage when oscillation stops
—	"H", "L" or High Impedance	Unfixed or unprovided level or high impedance
X	"H" or "L"	Unfixed or unprovided level
Z	High Impedance	High impedance condition in three states
t_a	Access Time	Time between the input of prescription and the output of the valid data
t_{ACC}	Address Access Time	Time required for obtaining the output of valid data after the address is given
t_{ACE}	Chip Enable Access Time	Time required for obtaining the output of the valid data after the chip enable signal is given
t_{ACS}	Chip Select Access Time	Time required for obtaining the output of the valid data after chip select signal is given
t_C	Cycle Time	Time from the start point of a complete operation to the start point of the next operation
t_{RC}	Read Cycle Time	Time required for one read cycle
t_{WC}	Write Cycle Time	Time required for one write cycle
t_f	Fall Time	Time required for the signal changed from "H" to "L"
t_h	Hold Time	Time required for the synchronous input to be held stable after the active clock edge
t_{DH}	Data Hold Time	Time required for the data input to be held stable after the active clock edge
t_{AH}	Address Hold Time	Time required for the address input to be held stable after the active clock edge
t_{OE}	Output Enable Delay Time	Time required for obtaining a valid output data after the output enable signal is given
t_{OH}	Output Hold Time	Time required for the output data to be held stable after the active clock edge
t_{pd}	Propagation Delay Time	Delay time between the active clock edge and the output change
t_{pHL}	Low Level Propagation Time	Delay time between the active clock edge and the output change from High to Low
t_{pLH}	High Level Propagation Time	Delay time between the active clock edge and the output change from Low to High
t_r	Rise Time	Time for changing the signal from Low to High
t_{su}	Set-up Time	Time required for the synchronous input remained stable before the next clock edge
t_{AS}	Address Set-up Time	Time required for the address input remained stable before the next clock edge
t_{DS}	Data Set-up Time	Time required for the data input remained stable before the next clock edge
t_{PW}	Pulse Width	Pulse width
t_{RP}	Read Pulse Width	Pulse width of the read signal
t_{WP}	Write Pulse Width	Pulse width of the write signal
t_{WR}	Write Recovery Time	Same as the address hold time t_{AH}

3. QUALITY ASSURANCE

S-MOS Systems, Inc. supported by the foundation of results acquired through experience in the adoption of low-power CMOS LSI for SEIKO quartz watches, has been providing highly reliable products that have set new standards in the industry.

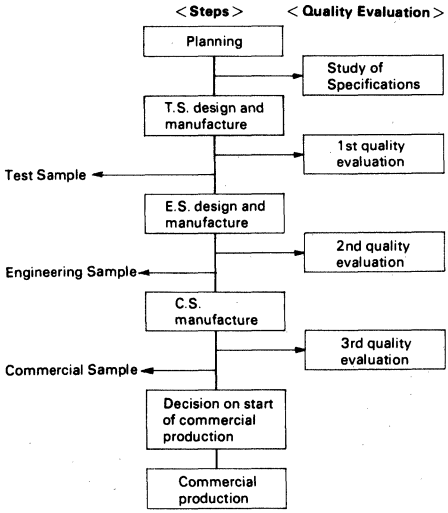
Today extremely high reliability is demanded of our customers' products. In step with this trend, extremely high reliability is demanded of semiconductor components.

To meet this demand in the market, we utilize a product quality assurance program which guarantees the highest quality in our products.

Our quality assurance program is as follows:

3.1 Quality Assurance System for Development of New Products

Our quality assurance efforts begin with a market survey to determine the user's specific needs. After the survey is completed, an analysis is made. Based on this analysis, an initial design is made. Next the initial design goes through prototype production and quality evaluation stages. Once these steps are completed, a new product, made according to the user's specifications is created. Fig. 3-1 shows the typical stages of new product development from initial planning to commercial production.



- Test Data, Field Data and Process Capabilities are used to compare the preliminary specs with the user's requirements. Market potential is also checked at this time.
- The test sample is evaluated for basic design capabilities and for conformance to the product specifications.
- The engineering sample is evaluated for quality assurance within the scope of the manufacturing conditions.
- The Production Sample is evaluated to determine if the quality level is achievable with the equipment available and under the existing manufacturing conditions.

Fig. 3-1 New Product Development Flow

3.1.1 Design

Market surveys are done so the designers know the exact specifications required by the user. Based on the information received, designs for the projected product are made. A "reliability" design is made using the data from reliability tests, field quality studies, past problems and available quality or reliability related information. Design staffs are given the purpose, environment and other factors relating to the application of a product to aid in its design.

3.1.2 Quality Evaluation

The quality evaluation is in two parts, the design evaluation and the reliability evaluation. The design evaluation determines if the target functions and performance level have been reached. The reliability evaluation verifies that long term quality is assured.

The reliability evaluation is done based on the particular objectives of the product. The evaluation is carried out under pre-established guidelines. It is performed according to EIAJ-IC-121 (Electronics Industries Association) standards and with MIL-STD-750B/883C and JIS-C7021 (Japanese Industrial Standards) where applicable. The application, environment and uniqueness of the manufacturing process are also taken into consideration.

3.1.3 Decision to Start Commercial Production

The decision is made whether or not to start commercial production after the sample or prototype production and quality evaluation are completed. This decision is based upon production capabilities, data verification on yield, reliability test results and the user's evaluation of the engineering sample.

3.2 Quality Assurance Systems for Commercial Production

Quality and reliability are assured by design checks in the Engineering and Manufacturing Departments and with verification of the finished product. Once in commercial production, quality control checks are made at various stages. Quality control begins at the assembly line. Inspections follow during the intermediate and final processes, ending with the shipping inspection. A quality asusrance flow chart is shown in Fig. 3-2.

3.2.1 Manufacturing Environment Control

Due to the sensitive nature of semiconductor devices, extreme care must be used during the manufacturing process. The manufacturing is done in a "clean room" where the temperature, humidity and dust are carefully monitored and controlled.

3.2.2 Control of Manufacturing and Measuring Equipment

Important elements of building reliability into a product are maintaining and controlling the manufacturing and measuring equipment. This equipment is used to monitor and control line conditions and/or to do intermediate inspections. With the evolution of devices to higher integrations and improved reliability, the production process must be controlled at a higher level. Routine checks and periodic inspections insure that we achieve these high standards.

3.2.3 Process Inspection

Quality Assurance is based on the theory that quality is built into the product. The inspection at each processing stage assures high quality. The inspection results are fed back into each process in order to stabilize the entire operation. These inspections also prevent defective parts from moving to the next process stage.

Fig. 3-3 and 3-4 show typical wafer process and assembly flow.

3.2.4 Shipping Inspection

The final inspection is performed when the product is ready to ship to reverify that the product meets our high standards. The electrical characteristics are 100% tested, and the environmental characteristics are tested on a lot sample basis. External visual inspection is also performed.

The shipping inspection is performed according to the category of the product. An example of the inspection process is shown in Table 3-1.

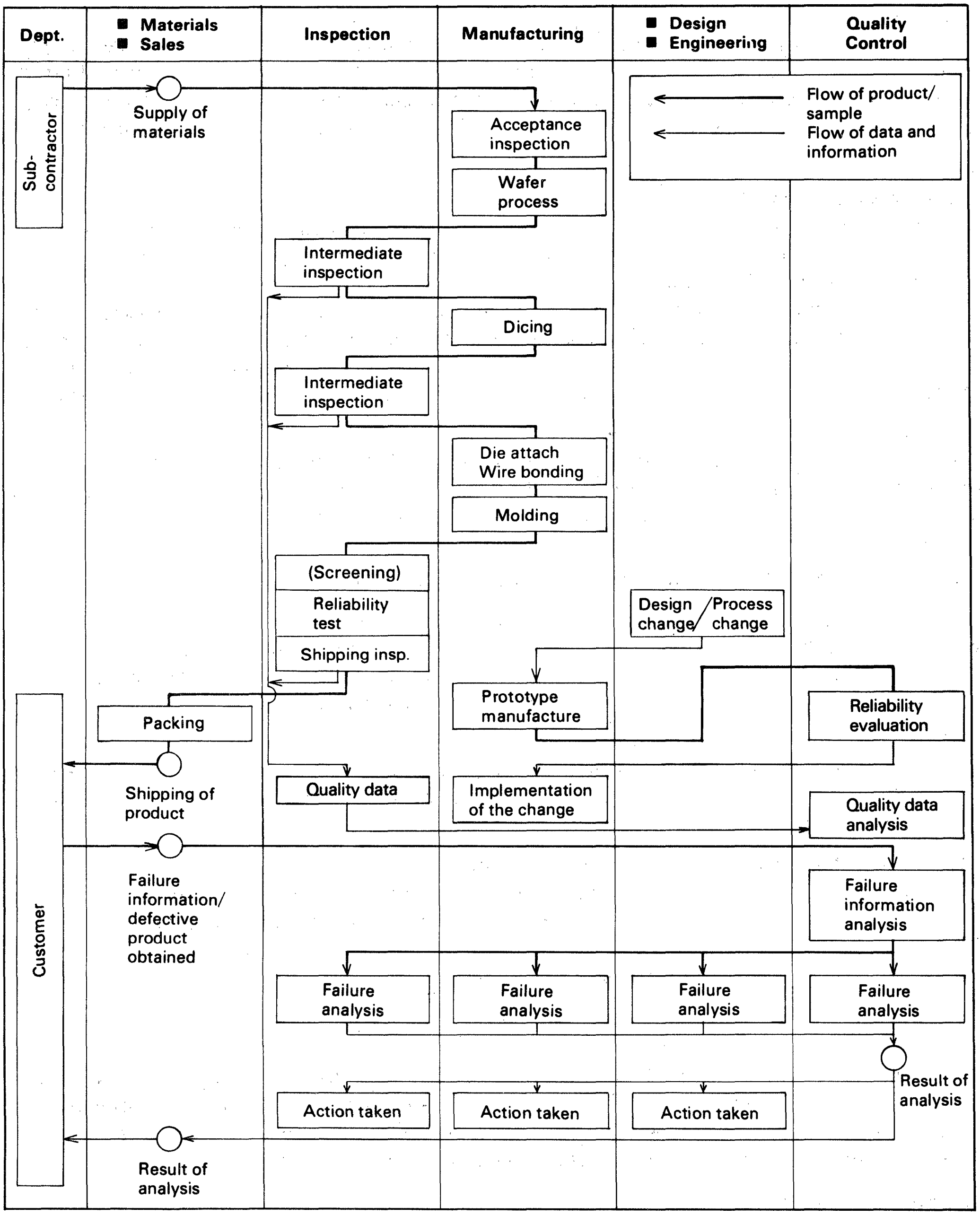


Fig. 3-2 Flow of Quality Assurance Activities in Commercial Production

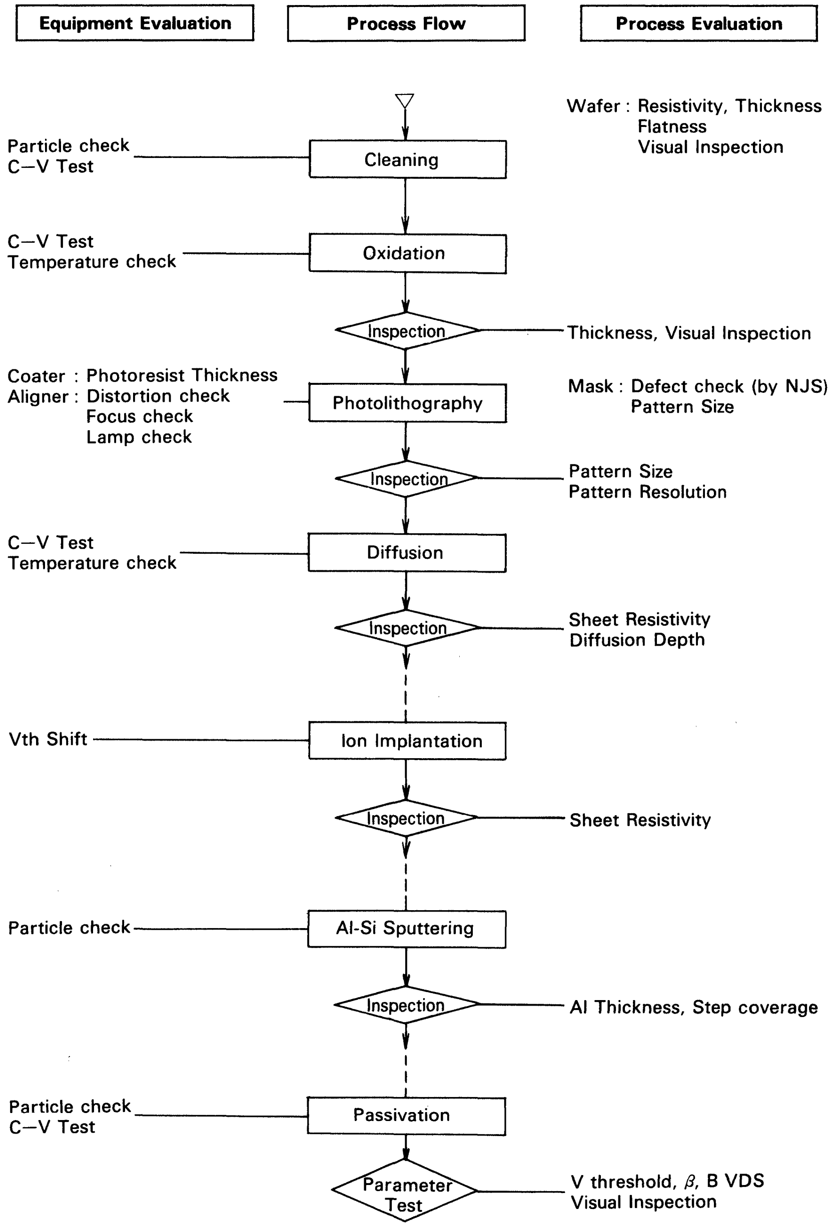


Fig. 3-3 Quality Assurance System for Wafer Production

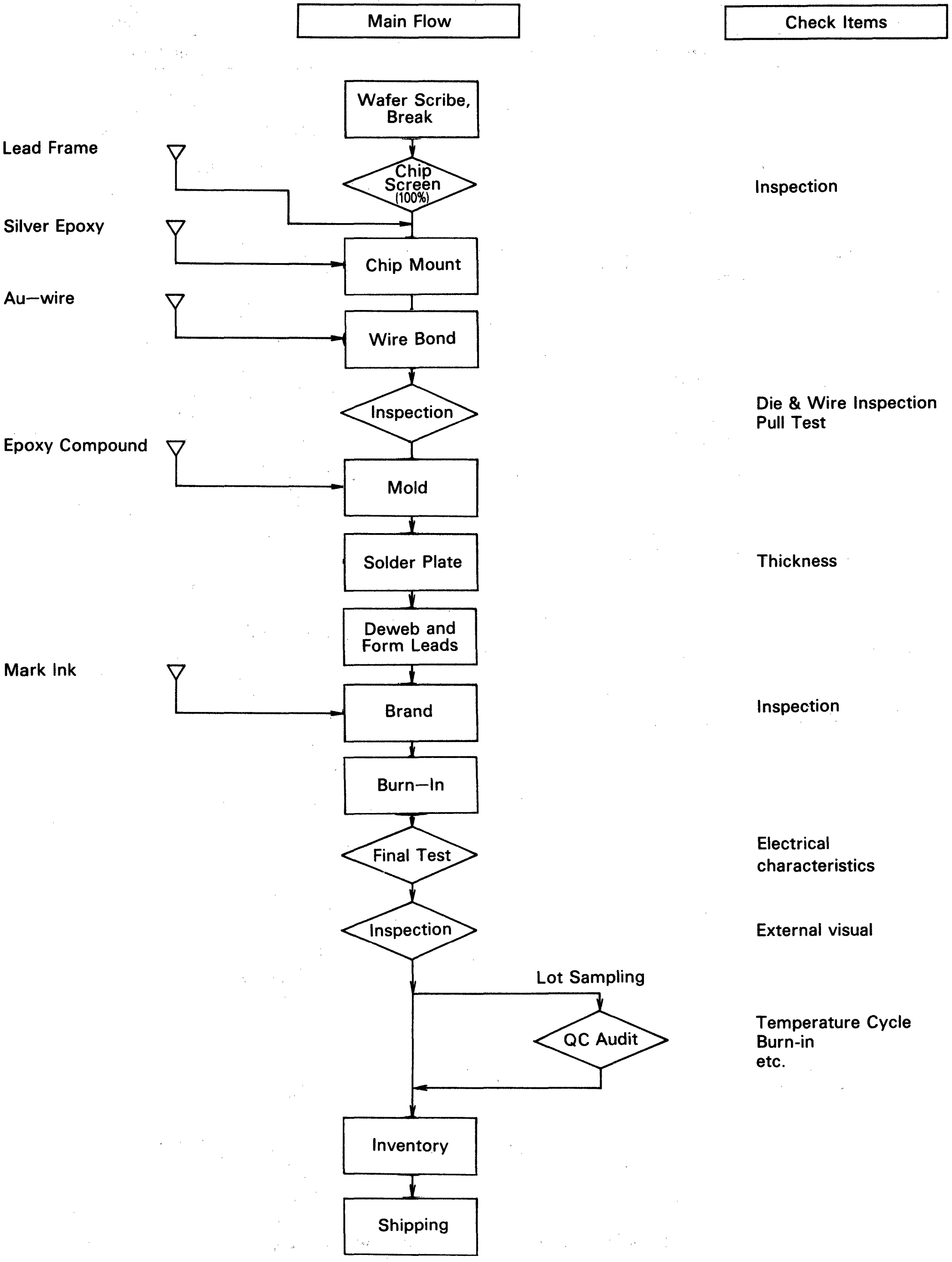
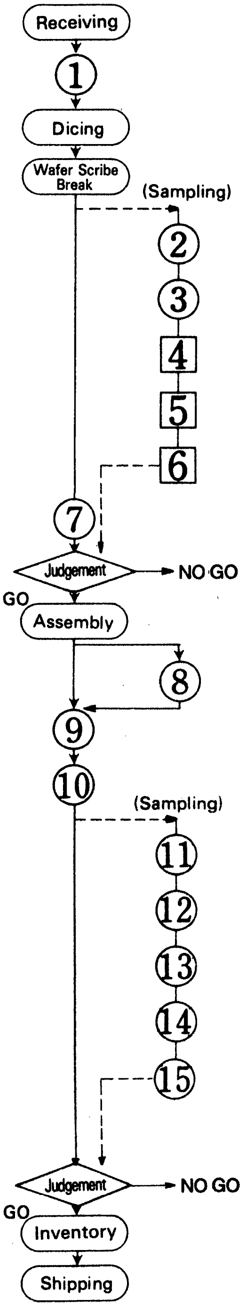


Fig. 3-4 Plastic Package Assembly Flowchart

Table 3-1 Example of Shipping Inspection

○: Each lot is inspected for quality assurance.
□: Specific lot is inspected to understand process levels.



Shipping Inspection for Pellet

No.	Process	Control point	Standard condition (method)
1	Electrical characteristics (100%)	Wafer process	Determined by product type
2	Resistance to heat	↑	Exposed to high temperature for short time
3	Bondability	↑	Wire pull Die shear strengh
4	Electrical characteristics/	↑	Determined by product types
5	Temperature cycle	↑	−55°C to 125°C (for 30 Min. at each temperature)
6	High temperature with bias	↑	125°C with Max. rated voltage applied
7	Visual inspection	Wafer process/ inspection process	Microscope

Shipping Inspection for Plastic package

8	Screening	Wafer process/ Assembling process	Burn-in Determined by product type
9	Electrical characteristics (100%)	↑	Determined by product type
10	Visual inspection (100%)	Assembling process	Visually checked
11	Temperature cycle	↑	−55°C to 125°C (for 30 minutes at each temperature
12	Electrical characteristics/ Visual inspection	Wafer process/ Assembling process	Determined by product types/visually checked
13	High temperature with bias	↑	125°C with Max. rated voltage applied
14	Pressure cooking	Assembling process	2 atmospheric (vapor) pressure (at 121°C)
15	Moisture resistance (with bias)	Wafer process/ Assembling process	85°C, 85% RH with Max. rated voltage applied

3.3 Reliability Testing

The reliability test includes environmental testing, life testing and mechanical testing. These tests are made in accordance with EIAJ-IC-121 as the prime standard, and with MIL-STD-750B/883C and JIS where applicable. The way the product is used, the application and the environment in which the product is operated are some of the factors taken into consideration when the conditions are set for the reliability test. It is important to conduct tests of new products under conditions that simulate how the product is to be used. In addition, standard tests are performed.

Table 3-2 summarizes the reliability test items and the factors associated with defects. Table 3-3 gives an example of typical conditions for reliability testing.

Table 3-2 Reliability Test Items and Factors Associated with Defects

Factors associated with defects Reliability test items	Junction isolation	Oxides	Metallization	Passivation	Die bonding	Wire bonding	Seal	Lead integrity	Solderability	Marking
High temperature bias	○	○	○	○	○	○	○			
High temperature storage	○	○	○	○		○	○			
Low temperature storage						○	○			
Boil	○	○	○	○	○	○	○			
Temperature cycle	○	○	○	○	○	○	○			
Mechanical shock						○	○	○		
Salt atmosphere							○	○	○	○
Thermal shock		○	○	○	○	○	○			
Vibration variable frequency			○		○	○				
Vibration constant frequency			○		○	○				
Lead integrity								○		
Bond strength			○		○	○				
Resistance to solvents							○			○

Table 3-3 Typical Conditions for Reliability Test

Test items		Test method		Purpose of test
		Reference standard	Test conditions	
Environmental test	Temperature cycle	EIAJ-IC-121 04 MIL-STD-883C 1010•5	−65°C to 150°C 100 cycles	Checks resistance to high and low temperatures, and varying temperatures
	Thermal shock	EIAJ-IC-121 03 MIL-STD-883C 1011•4	0°C to 100°C 10 cycles	Checks resistance to rapid temperature changes
	High temperature storage	EIAJ-IC-121 15 MIL-STD-883C 1008•2	Ta=150°C 1,000 hours	Checks resistance to heat when exposed to high temperature
	Low temperature storage	EIAJ-IC-121 16	Ta=−65°C 1,000 hours	Checks resistance to cold when exposed to low temperature
	Moisture resistance	EIAJ-IC-121 17	Ta=85°C, 85% RH 1,000 hours	Checks resistance to long-time operation and storage in the environment with high relative humidity
	Salt atmosphere	JIS-C7021 A-12 MIL-STD-202E 101D	35°C, 5% brine spray, 48 hours	Checks resistance to corrosion through acceleration test with coastal environment simulated atmosphere
	Pressure cooker	EIAJ-IC-121 18	2 atmospheric pressures (121°C) 96 hours	Checks resistance to accelerated humidity changes
	Resistance to soldering heat	EIAJ-IC-121 01	260°C, 10 seconds (solder bath)	Checks resistance to heat during soldering
	Resistance to solvents	EIAJ-IC-121 14 MIL-STD-883C 2015•4	Freon Trichloroethylene 10 minutes	Checks resistance of printed marking to solvent
Life test	High temperature steady state	EIAJ-IC-121 51 MIL-STD-883C 1005•4	Ta=125°C (steady operation) 1,000 hours	Checks resistance to electrical stress and thermal stress applied for extended time periods
	Moisture resistance (with bias)	EIAJ-IC-121 17	Ta=85°C, 85% RH (rated voltage applied) 1,000 hours	Checks resistance to long-time use with high relative humidity

(Continue)

Typical Conditions for Reliability Test (cont.)

Test items		Test method		Purpose of test
		Reference standard	Test conditions	
Mechanical test	Vibration variable frequency	EIAJ-IC-121 10 MIL-STD-883C 2007·1	100 Hz to 2,000 Hz 4 minutes/back and forth 4 times each for X, Y and Z (at 20G)	Checks resistance to vibration during transportation or operation
	Vibration fatigue	EIAJ-IC-121 10 MIL-STD-883C 2005·1	60 Hz 20G 32 hours each for X, Y and Z	Checks resistance to vibration during transportation or operation
	Mechanical shock	EIAJ-IC-121 08	1,500G 3 falls each for X, Y and Z	Checks resistance to shocks applied when the product is being handled, transported or operated
	Lead integrity	EIAJ-IC-121 11 MIL-STD-883C 2004·4	Tension 1.0 kg 10 seconds (DIP) Tension 0.3 kg 10 seconds (FP)	Checks resistance to forces to which the lead is subject during installation or operation
		EIAJ-IC-121 11 MIL-STD-883C 2004·4	Bend 90° 2 cycles : 42 Alloy	
	Solderability	EIAJ-IC-121 02 MIL-STD-202E 208C	230°C, 5 seconds flux used	Checks solderability to leads

3.4 Defective Product Policy

S-MOS Systems requests the user to return defective products. It is important to S-MOS that when a problem arises it be brought to our attention. Any product information, positive or negative, is valuable data which enables us to improve the quality of our product.

We will make a thorough investigation of the problem with the user's assistance. Where the problem occurred, how it developed and any other related information will be reviewed. The product's manufacturing process and reliability test data will also be reviewed.

The Quality Control Department will check all available information for solutions to prevent the problem from happening in the future. Quality Control will report the results of the investigation to the user through the Sales Department. The Manufacturing Department will be given the report so corrective action can be taken as necessary.

Fig. 3-5 shows that RMA (Returned Material Authorization) process.

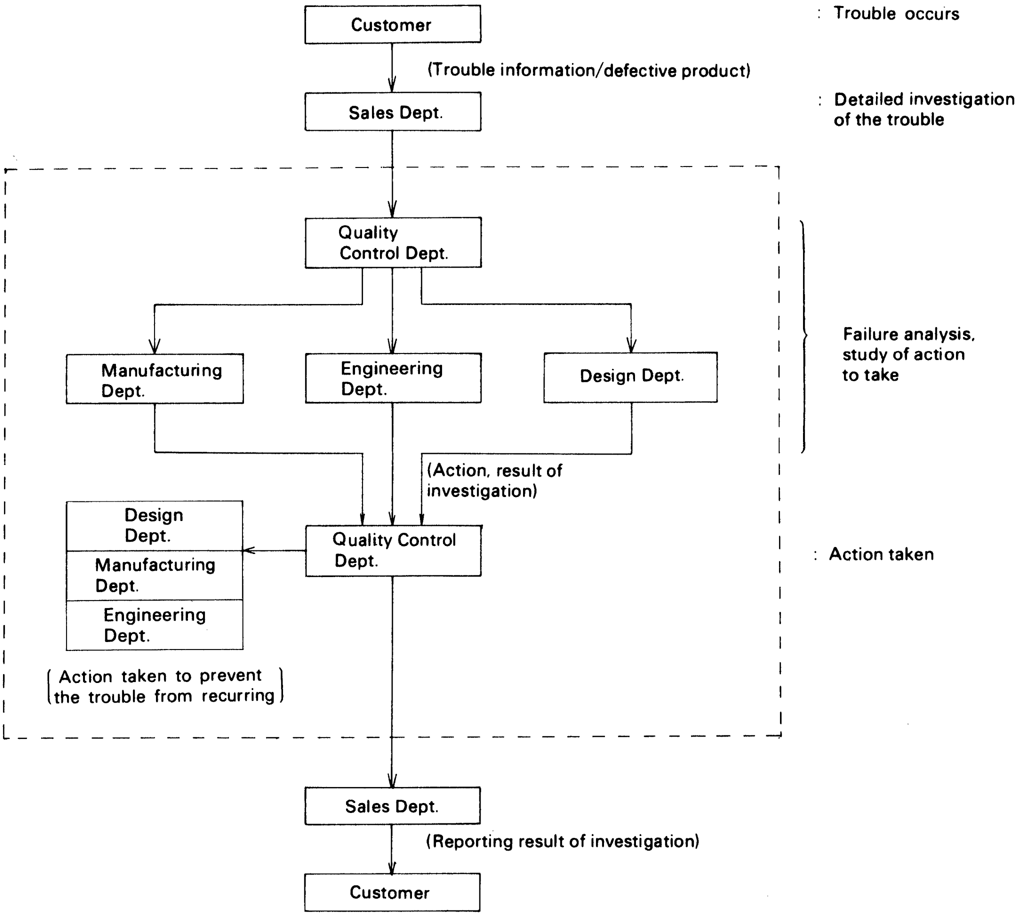


Fig. 3-5 Route of Actions against Trouble Occuring outside the Company

3.5 Operating Precautions

S-MOS System's plastic molded CMOS LSI devices are designed and manufactured for trouble free operation when used under normal operating conditions. Our products are subjected to stringent electrostatic, mechanical strength, and environmental tests for assured reliability. When working with our product the user should observe the following precautions:

(1) Use the product in the range of rated operating voltage, operating temperature, operating input/output voltage and input/output current. If the product is used outside these operating parameters, the user may experience high failure rates.

(2) Excessive electrical noise applied to the power or input pin of the device could cause it to latch up, resulting in malfunction or damage. If this occurs, turn the power off immediately, isolate the problem and turn the power on again.

(3) Do not expose the product to excessive mechanical vibration, repetitive shock stress, rapid or cyclic temperature changes. These factors can cause the wires in the plastic package to break.

(4) Although all terminals have electrostatic protection, damage may still occur if very high electrostatic potentials are applied. Use of a conductive container or aluminum foil for packaging and transportation is recommended. (Untreated plastic containers are NOT recommended.) Use grounded soldering tools and test equipment.

3.6 Solder-reflow Process of Plastic Flat Packages

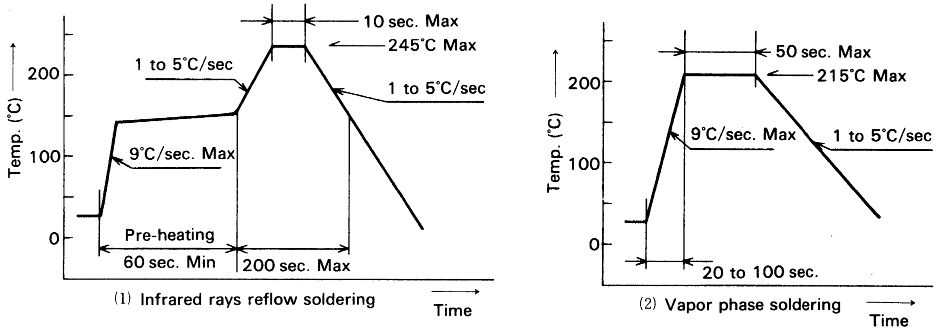
During the solder-reflow process, the plastic flat package is exposed to high temperatures (such as far-infrared) inside the reflow furnace. Therefore, the following precautions should be observed when packages are in the solder-reflow process :

(1) Maintain the maximum temperature of the resin of the package at 245°C for not more than 10 seconds.

(2) Maintain the outer surface of the reflow furnace temperature (resin surface temperature) at the curve shown in Fig. 3-6.

(3) The resin on plastic flat packages is prone to absorb moisture. Even at room temperature, the amount of moisture absorbed increases with time. If a wet package is put in the solder-reflow furnace, the resin may crack or the adhesiveness of the resin to the frame may be decreased.

(4) Items (1) through (3) are intended as a guideline based on our laboratory experience and are for reference only since packages will be stored in different environments and different types of reflow furnaces will be used. Thus, it is important that packages be checked for quality at the solder-reflow process before entering mass production.



(1) Infrared rays reflow soldering

(2) Vapor phase soldering

Fig. 3-6 Reflow Furnace Temperature Curve

3.7 Package Storage Guidelines

(1) Packages should be stored in the recommended environment. Maximum storage conditions for temperature and humidity are shown in Table 3.6.

(2) Packages which exceed the storage limits specified in Table 3.6, or which have absorbed too much moisture due to high temperature or high humidity, should be baked before the reflow process. The recommended procedures for drying the packages are shown in Table 3.7. This drying process will prevent the resin from cracking during the reflow process.

Table 3-6 Maximum Storage Conditions for Surface Mount Component (SMC)

PLASTIC FLAT PACKAGE & SOP

Storage Conditions		Allowable period
Before open dry-pack (≤35°C)		6 month
After open dry-pack	25°C. 60%	1.5 month
	30°C. 80%	12 day
	35°C. 90%	3 day (72 hour)

PLASTIC PLCC

Storage Conditions		Allowable period
Before open dry-pack (≤35°C)		6 month
After open dry-pack	25°C. 60%	2 month
	30°C. 80%	12 day
	35°C. 90%	3 day (72 hour)

Table 3-7 Dryout conditions for SMC

Package type \ Temperature	125°C	150°C
PLASTIC QFP, SOP	5 hour	2 hour
PLASTIC PLCC	20 hour	8 hour

4. PACKAGE INFORMATION

Package	Pin	Name
Plastic DIP	8 pin	C 8
	14pin	C14
	16pin	C16
	18pin	C18
	20pin	C20
	22pin	C22
	24pin	C24
	28pin	C28
	40pin	C40
	42pin	C42
CERDIP	16pin	H16
	18pin	H18
	20pin	H20
	24pin	H24
	28pin	H28
	40pin	H40
Plastic Shrink DIP	28pin	S28
	64pin	S64
Plastic Skinny DIP	24pin	N24
Plastic QFP	18pin	F18-4
	44pin	F44-2
	46pin	F46
	46pin	F46-5
	60pin	F60
	60pin	F60-2
	60pin	F60-5
	80pin	F80
	80pin	F80-5
	100pin	F100-5
	128pin	F128-8
	144pin	F144-8
	160pin	F160-8
Ceramic QFP	148pin	L148
Plastic SOP	14pin	M14
	16pin	M16
	24pin	M24
	24pin	M24-2
	28pin	M28-2
Ceramic PGA	64pin	P64
	72pin	P72
	132pin	P132
Plastic PGA	89pin	G89
PLCC	28pin	J28
	44pin	J44
	68pin	J68
	84pin	J84
SOT89	3pin	Y3

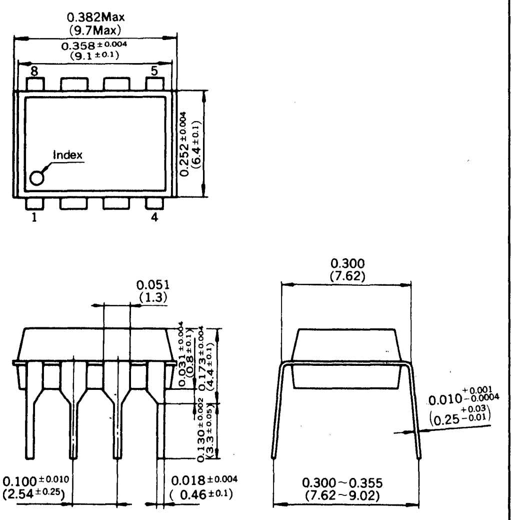
NOTE: Exact dimensions may vary slightly with use of different assembly lines.

Package Dimension Drawings

Page	Code	Package Type
21	C8	8-pin DIP
	C14	14-pin DIP
	C16	16-pin DIP
	C18	18-pin DIP
22	C20	20-pin DIP
	C22	22-pin DIP
	C24	24-pin DIP
	C28	28-pin DIP
23	C40	40-pin DIP
	C42	42-pin DIP
24	H16	16-pin CERDIP
	H18	18-pin CERDIP
	H20	20-pin CERDIP
	H24	24-pin CERDIP
C25	H28	28-pin CERDIP
	H40	40-pin CERDIP
26	S28	28-pin Shrink DIP
	S64	64-pin Shrink DIP
27	N24	24-pin Skinny DIP
28	F18-4	18-pin QFP
	F44-2	44-pin QFP
	F46	46-pin QFP
	F46-5	46-pin QFP
29	F60	60-pin QFP
	F60-2	60-pin QFP
	F60-5	60-pin QFP
	F80	80-pin QFP
30	F80-5	80-pin QFP
	F100-5	100-pin QFP
	F128-8	128-pin QFP
	F144-8	144-pin QFP
31	F160-8	160-pin QFP
32	L148	148-pin QFP
33	M14	14-pin SOP
	M16	16-pin SOP
	M24	24-pin SOP
	M24-2	24-pin SOP
34	M28-2	28-pin SOP
35	P64	64-pin PGA
	P72	72-pin PGA
	P132	132-pin PGA
36	G89	89-pin PGA
37	J28	28-pin PLCC
	J44	44-pin PLCC
	J68	68-pin PLCC
	J84	84-pin PLCC
38	Y3	3-pin SOT89

C8

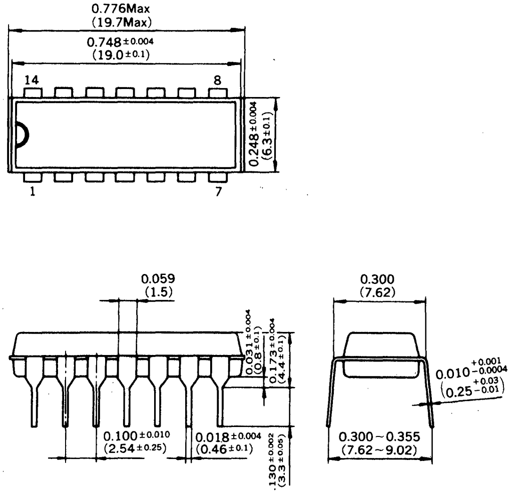
8-pin DIP



unit : inch
(mm)

C14

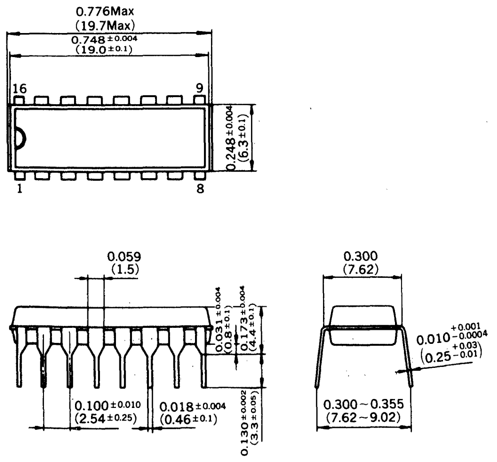
14-pin DIP



unit : inch
(mm)

C16

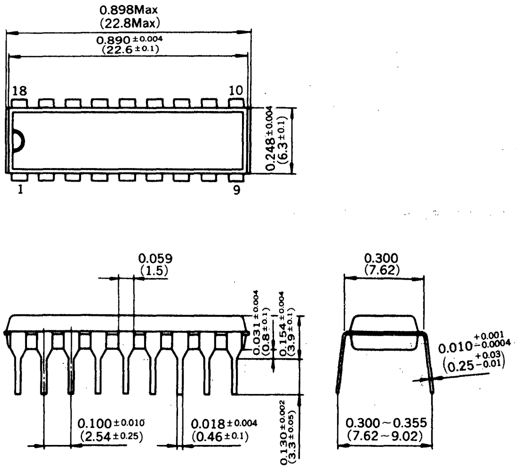
16-pin DIP



unit : inch
(mm)

C18

18-pin DIP

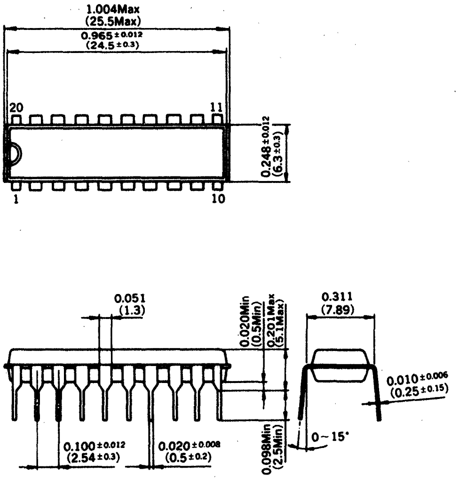


unit : inch
(mm)

NOTE : Dimensions shown in inches and are derived from their metric equivalents. Please use metric dimensions for board layouts.

C20

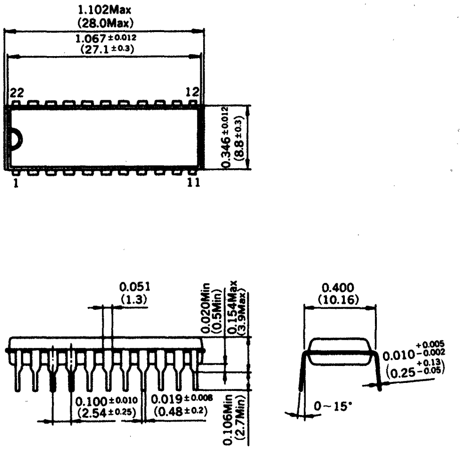
20-pin DIP



unit : inch
(mm)

C22

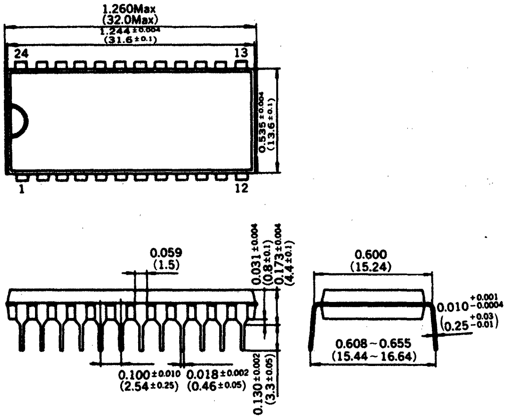
22-pin DIP



unit : inch
(mm)

C24

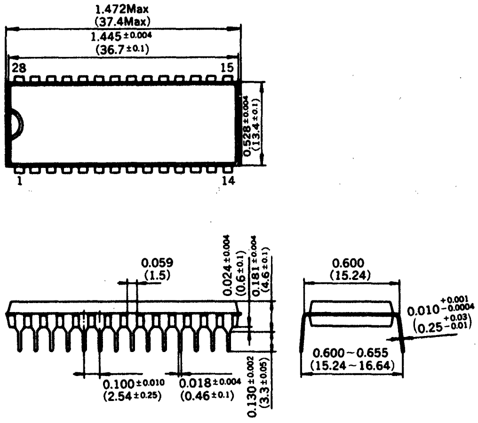
24-pin DIP



unit : inch
(mm)

C28

28-pin DIP

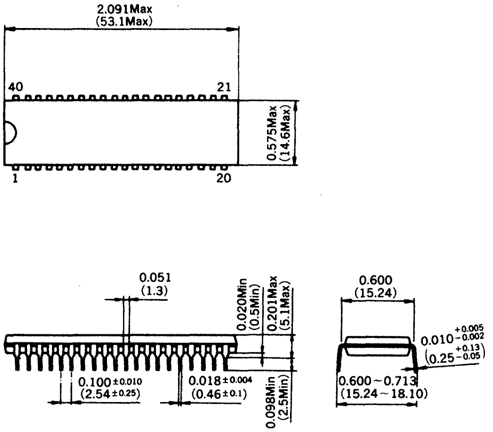


unit : inch
(mm)

NOTE : Dimensions shown in inches and are derived from their metric equivalents. Please use metric dimensions for board layouts.

C40

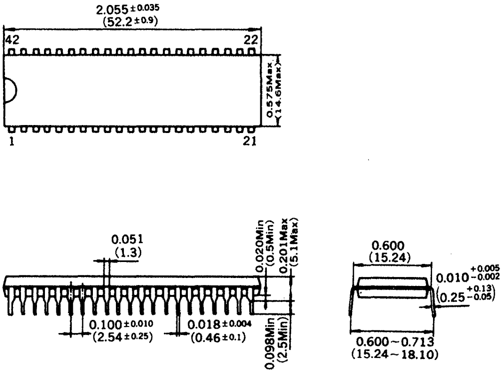
40-pin DIP



unit : inch
(mm)

C42

42-pin DIP

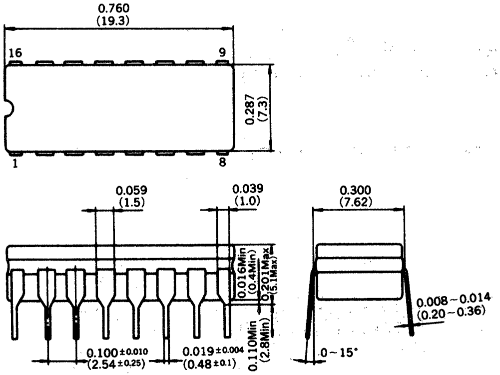


unit : inch
(mm)

NOTE : Dimensions shown in inches and are derived from their metric equivalents. Please use metric dimensions for board layouts.

H16

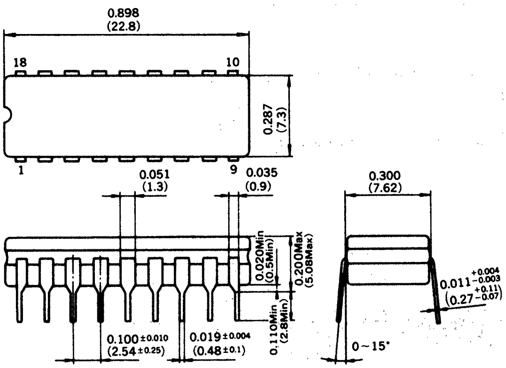
16-pin CERDIP



unit : inch
(mm)

H18

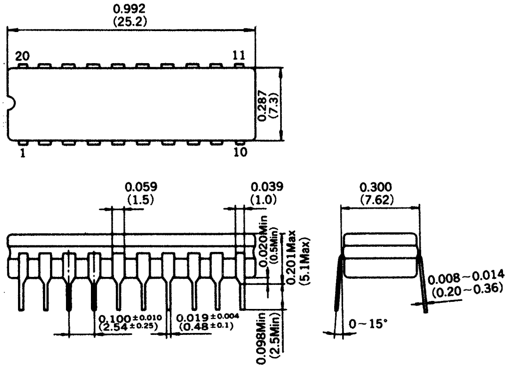
18-pin CERDIP



unit : inch
(mm)

H20

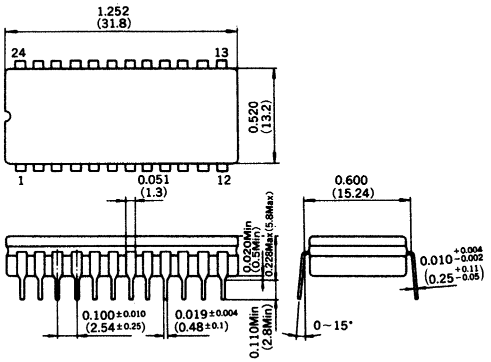
20-pin CERDIP



unit : inch
(mm)

H24

24-pin CERDIP

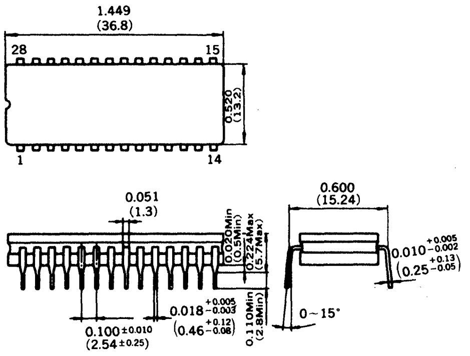


unit : inch
(mm)

NOTE : Dimensions shown in inches and are derived from their metric equivalents. Please use metric dimensions for board layouts.

H28

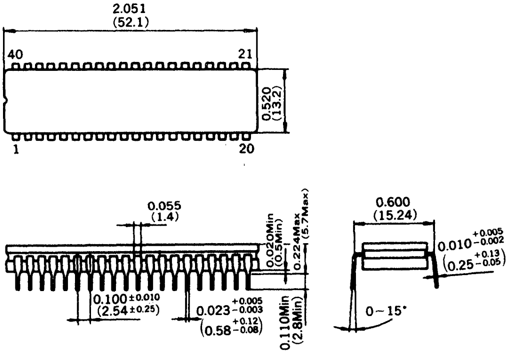
28-pin CERDIP



unit : inch
(mm)

H40

40-pin CERDIP

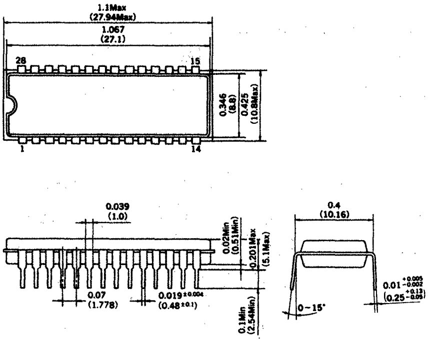


unit : inch
(mm)

NOTE : Dimensions shown in inches and are derived from their metric equivalents. Please use metric dimensions for board layouts.

S28

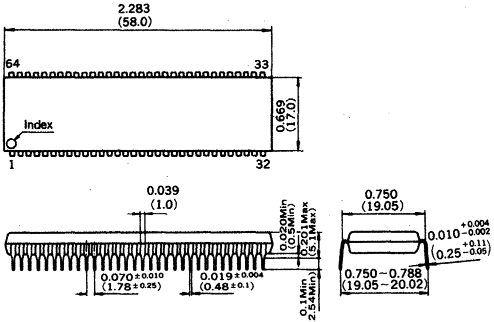
28-pin Shrink DIP



unit : inch
(mm)

S64

64-pin Shrink DIP

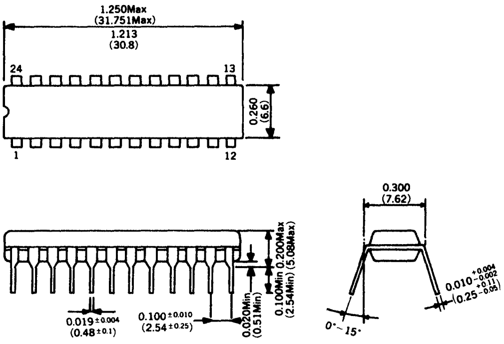


unit : inch
(mm)

NOTE : Dimensions shown in inches and are derived from their metric equivalents. Please use metric dimensions for board layouts.

N24

24-pin Skinny DIP

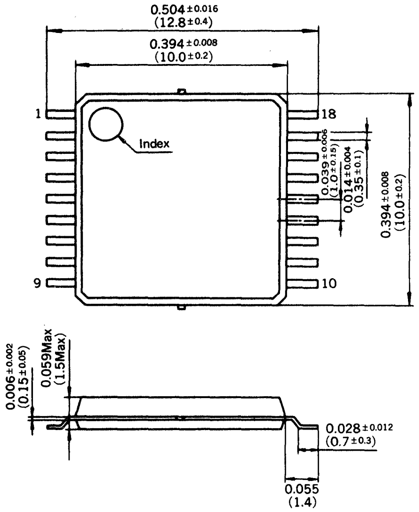


unit : inch
(mm)

NOTE : Dimensions shown in inches and are derived from their metric equivalents. Please use metric dimensions for board layouts.

F18-4

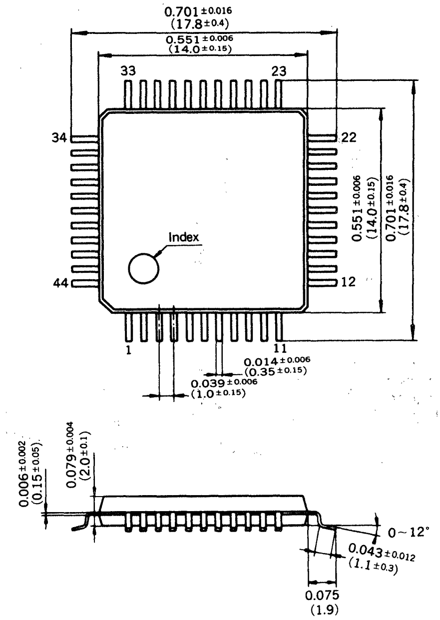
18-pin QFP



unit : inch
(mm)

F44-2

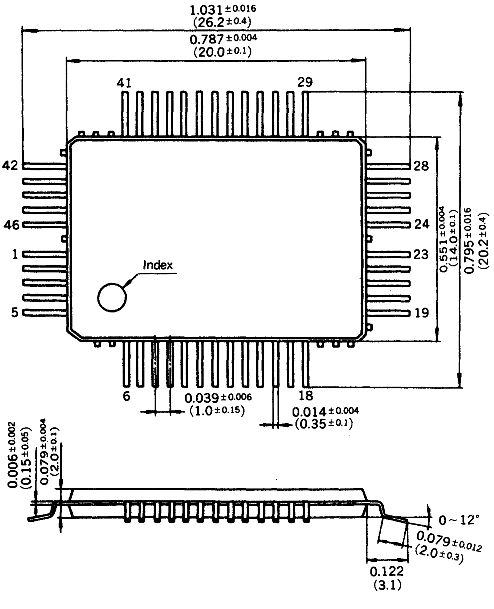
44-pin QFP



unit : inch
(mm)

F46

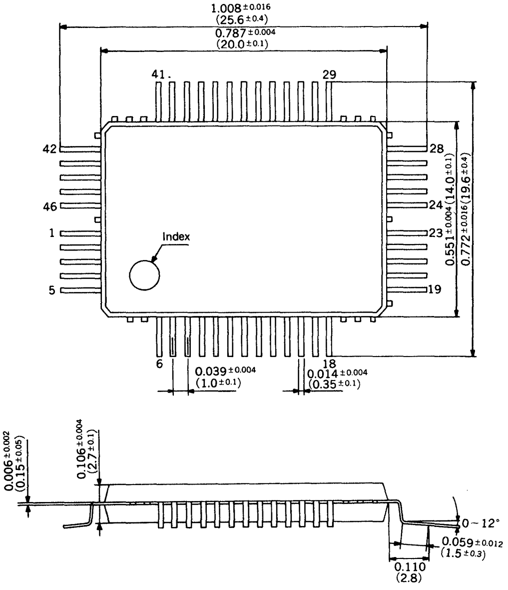
46-pin QFP



unit : inch
(mm)

F46-5

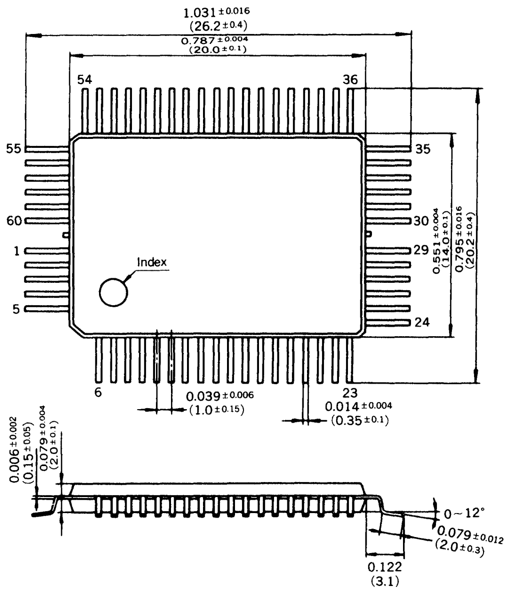
46-pin QFP



unit : inch
(mm)

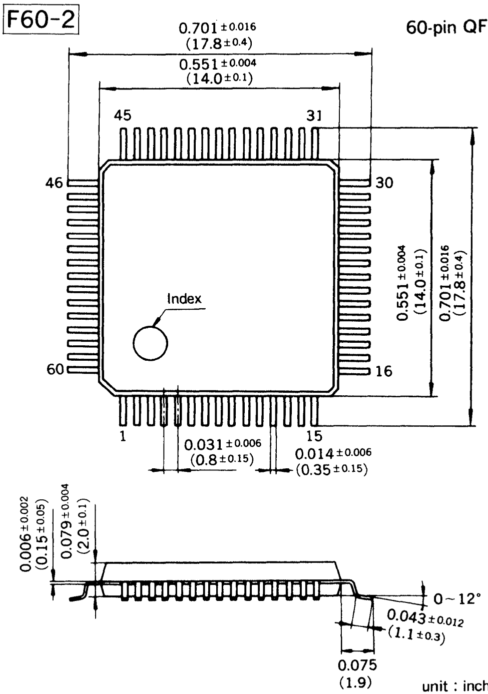
NOTE : Dimensions shown in inches and are derived from their metric equivalents. Please use metric dimensions for board layouts.

F60 60-pin QFP



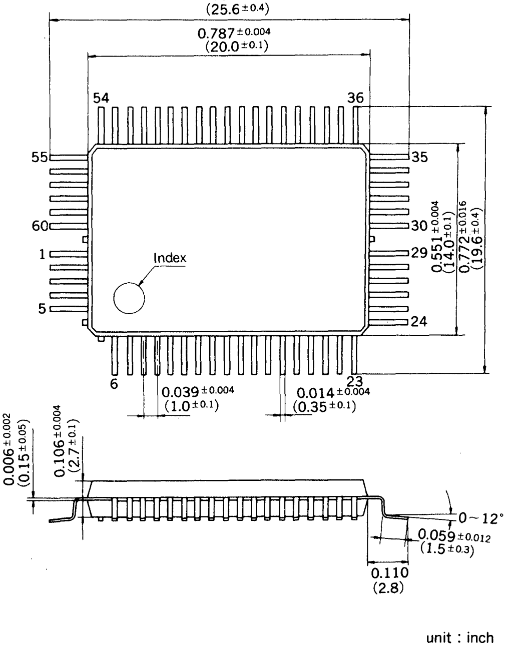
unit : inch
(mm)

F60-2 60-pin QFP



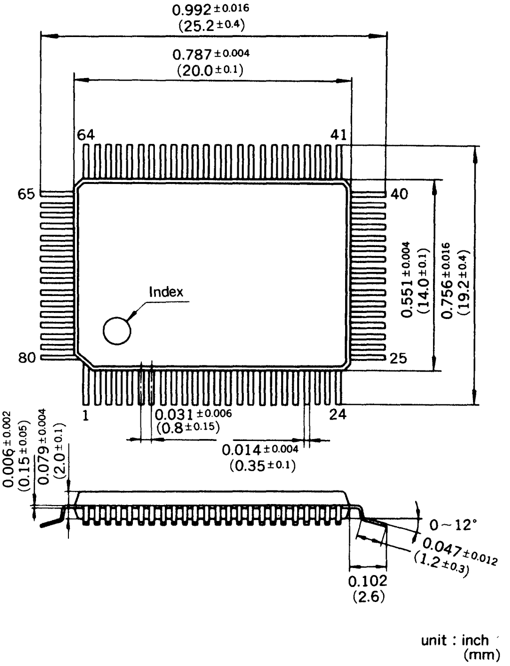
unit : inch
(mm)

F60-5 60-pin QFP



unit : inch
(mm)

F80 80-pin QFP

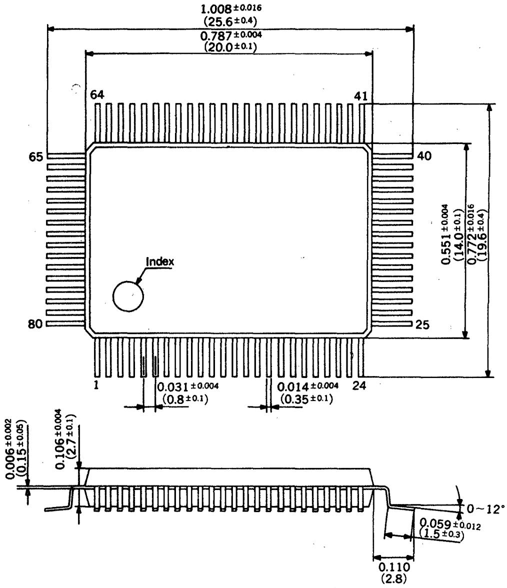


unit : inch
(mm)

NOTE : Dimensions shown in inches and are derived from their metric equivalents. Please use metric dimensions for board layouts.

F80-5

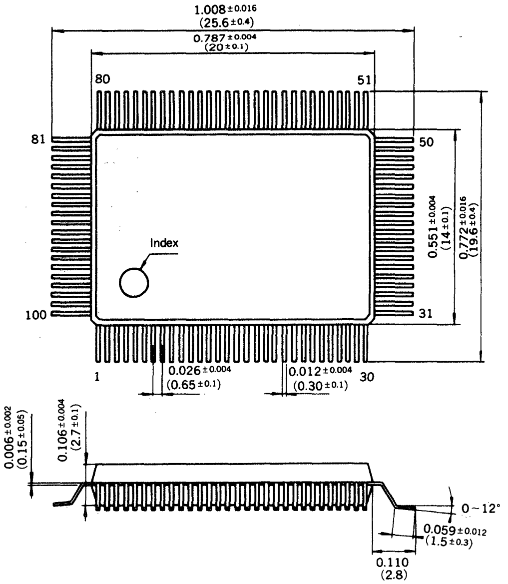
80-pin QFP



unit : inch
(mm)

F100-5

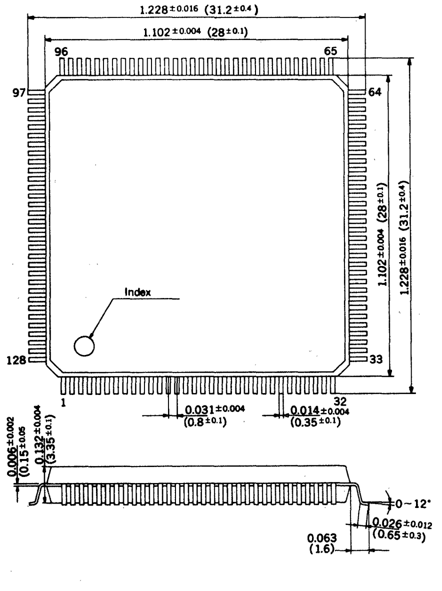
100-pin QFP



unit : inch
(mm)

F128-8

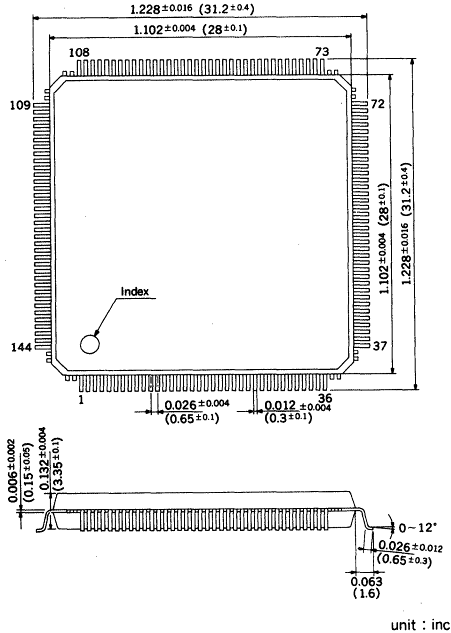
128-pin QFP



unit : inch
(mm)

F144-8

144-pin QFP

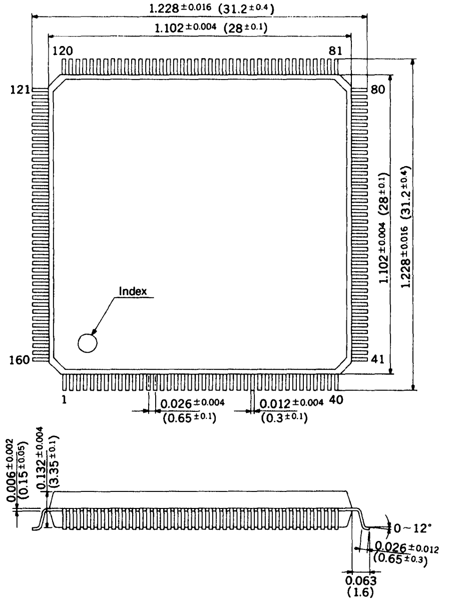


unit : inch
(mm)

NOTE : Dimensions shown in inches and are derived from their metric equivalents. Please use metric dimensions for board layouts.

F160-8

160-pin QFP

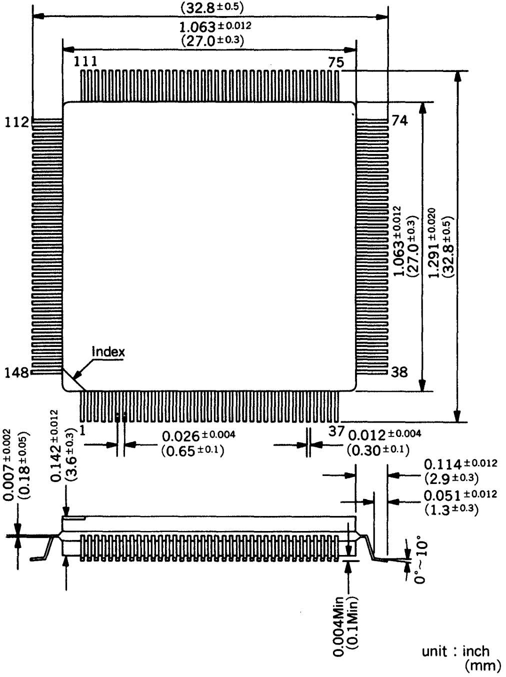


unit : inch
(mm)

NOTE : Dimensions shown in inches and are derived from their metric equivalents. Please use metric dimensions for board layouts.

L148

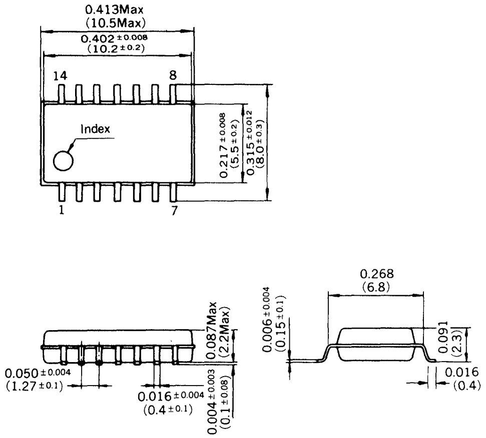
148-pin QFP



NOTE : Dimensions shown in inches and are derived from their metric equivalents. Please use metric dimensions for board layouts.

M14

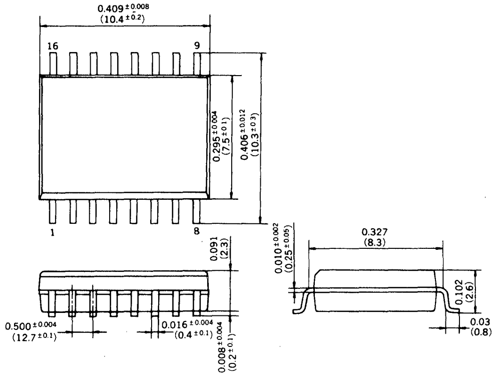
14-pin SOP



unit : inch
(mm)

M16

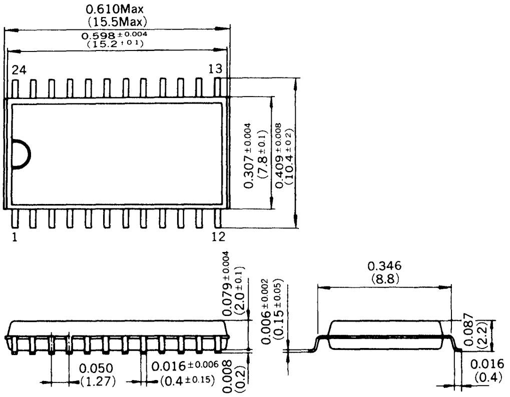
16-pin SOP



unit : inch
(mm)

M24

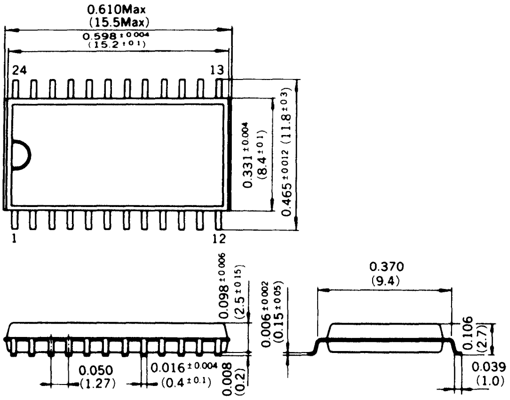
24-pin SOP



unit : inch
(mm)

M24-2

24-pin SOP

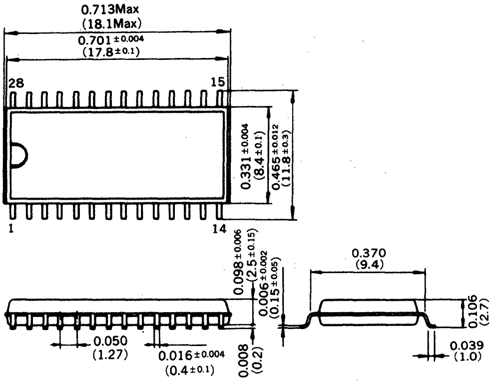


unit : inch
(mm)

NOTE : Dimensions shown in inches and are derived from their metric equivalents. Please use metric dimensions for board layouts.

M28-2

28-pin SOP

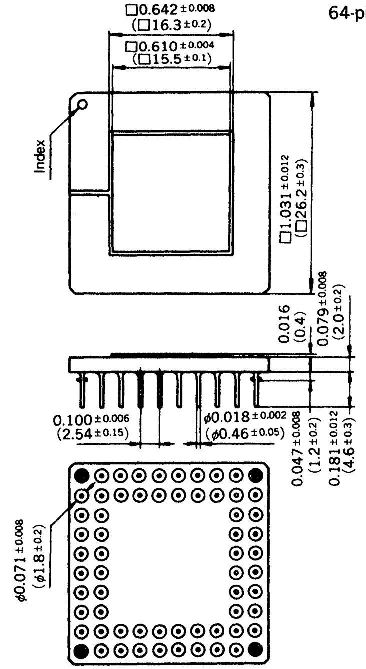


unit : inch
(mm)

NOTE : Dimensions shown in inches and are derived from their metric equivalents. Please use metric dimensions for board layouts.

P64

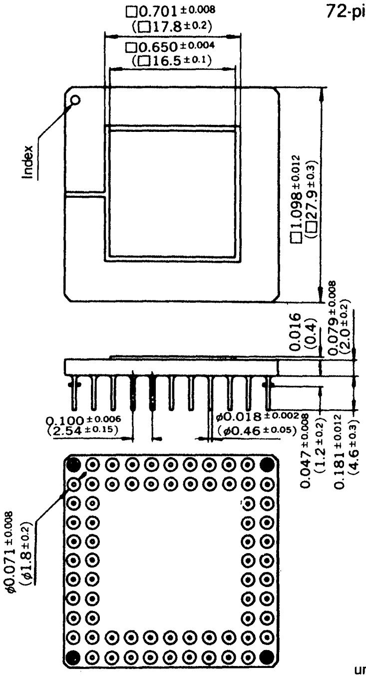
64-pin PGA



unit : inch
(mm)

P72

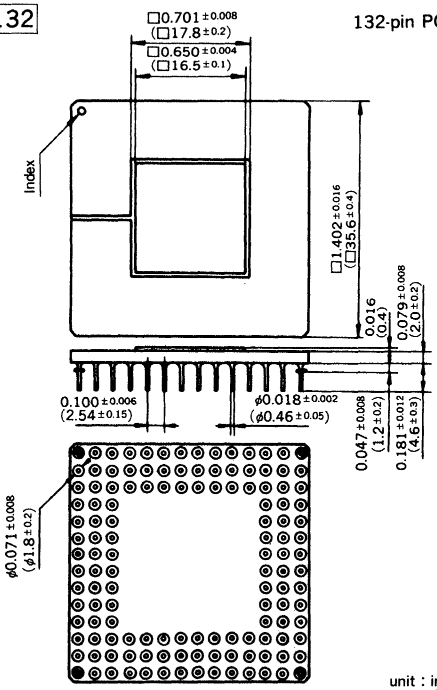
72-pin PGA



unit : inch
(mm)

P132

132-pin PGA

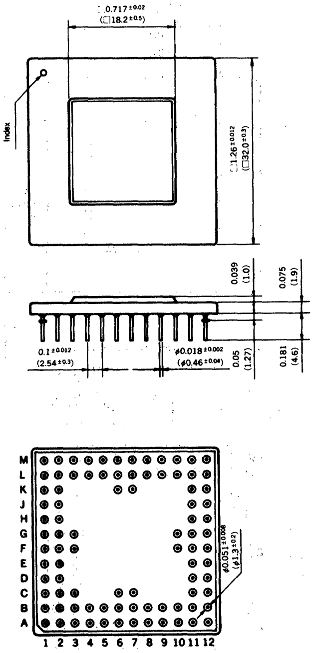


unit : inch
(mm)

NOTE : Dimensions shown in inches and are derived from their metric equivalents. Please use metric dimensions for board layouts.

G89

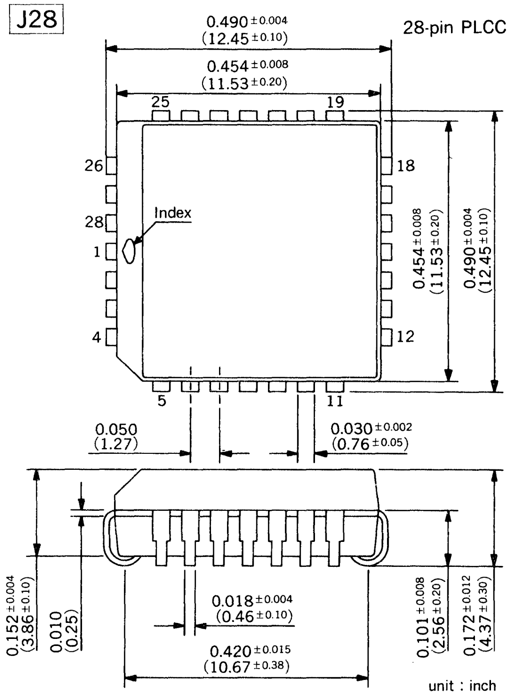
89-pin PGA



unit : inch
(mm)

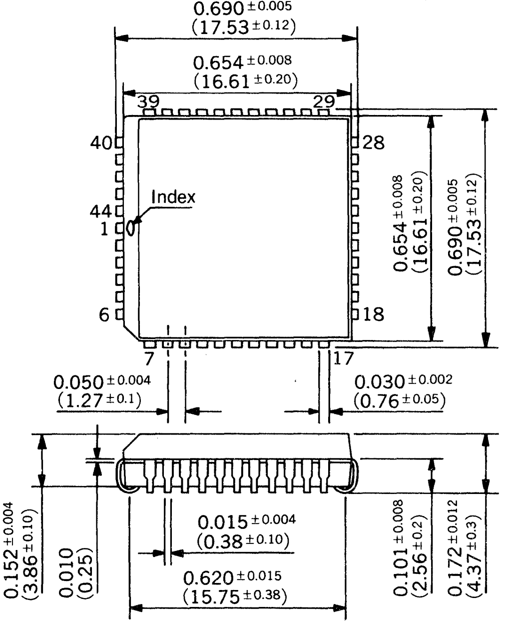
NOTE : Dimensions shown in inches and are derived from their metric equivalents. Please use metric dimensions for board layouts.

J28 28-pin PLCC



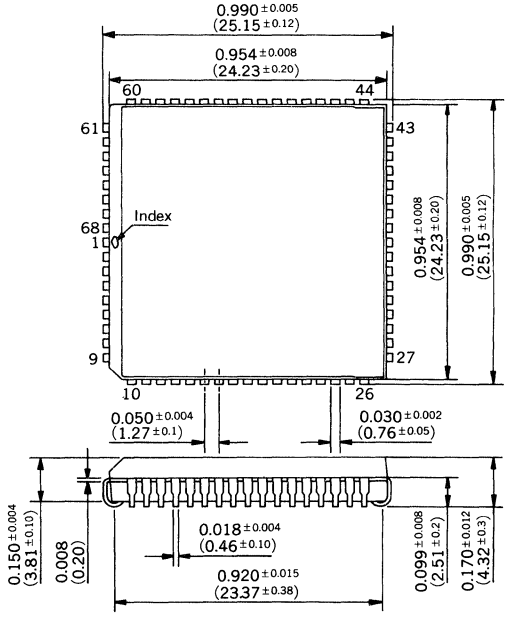
unit : inch
(mm)

J44 44-pin PLCC



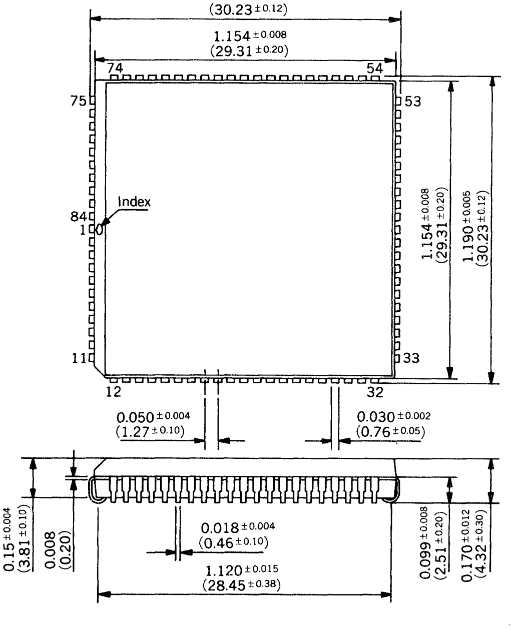
unit : inch
(mm)

J68 68-pin PLCC



unit : inch
(mm)

J84 84-pin PLCC

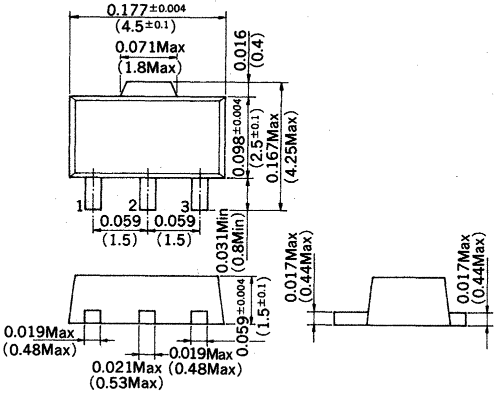


unit : inch
(mm)

NOTE : Dimensions shown in inches and are derived from their metric equivalents. Please use metric dimensions for board layouts.

Y3

3-pin SOT89



unit : inch
(mm)

NOTE : Dimensions shown in inches and are derived from their metric equivalents. Please use metric dimensions for board layouts.

5. DEVELOPMENT OF SEMI-CUSTOM CIRCUITS

5.1 Development of the Mask ROM and the Single Chip Microcomputer ROM

5.1.1 Mask ROM Customer Code Pattern

Customer code is entered into the Mask ROM using CAD. The ROM code data should be submitted by EPROM or magnetic tape in accordance with the following specifications. The chip enable and the chip select are assigned by completing the "Mask ROM Order Sheet" attached to the ROM code data. Consult S-MOS when using media other than the EPROM or magnetic tape.

(1) EPROM Requirements
  (a) Most EPROMs are acceptable.
  (b) The product name of the EPROM must be written on the "Mask ROM Order Sheet."
  (c) Submit two sets of EPROM data and data list when placing an order.

(2) Magnetic Tape Requirements
  (a) Magnetic tape must be compatible with IBM's magnetic tape device:
    - Number of Tracks: 9
    - Magnetic Recording Density: 800 BPI or 1600 BPI
      (The density should be specified on the "Mask ROM Order Sheet.")
  (b) Magnetic Tape Code: EBCDIC
  (c) Format of the Magnetic Tape:
    - Without tape mark at the head
    - Without label
    - Record Size: 80 byte/record
    - Block Size: 10 records/block
    - Two continuous tape marks at the end of the file
  (d) When writing the ROM code data of multiple chips on a single magnetic tape, there should be one tape mark at the end of each file and two tape marks at the end of the last file. Separate magnetic tapes should be used for each semicustom LSI.

(3) Data Form
  (a) Divide the eight bit code in half; the upper four bits and the lower four bits. Each four bits should be converted into a hexadecimal.
  (b) The data form is shown in Fig. 5-1. Data is written on the tape in ASCII hexadecimal code.
    - Record Mark — Colon ":" indicates the beginning of a record.
    - Number of Codes — Number of object codes stored in one record will be indicated in two hexidecimal digits.
    - Location Address — The head address for each record should be written in four hexadecimal digits. The number should start from 0000 in ascending order.
    - Record Type — Should be in two hexadecimal digits, 01 for the last record and 00 for all others.
    - Code — One eight bit word is written in two hexadecimal digits.
    - Check Sum — The number of codes, the location address, the record type and the codes are subtracted in order from the primary value 00. The results are written in two hexadecimal digits.
    - Last Record — Indicated by 00000001FF RETURN.

(4) Check Sum Calculation

The subtraction is made on the assumption that the binary subtracting device is used and borrowing is ignored.

Example:

The number of codes (10) is subtracted from the primary value.

$$\begin{array}{r} 0000\ 0000 \\ -)\underline{0001\ 0000} \\ 1111\ 0000 \end{array}$$

The upper 8 bits of the location address (00) is then subtracted.

$$\begin{array}{r} 1111\ 0000 \\ -)\underline{0000\ 0000} \\ 1111\ 0000 \end{array}$$

The lower 8 bits (00), the record type (00) and the code (7D) are subtracted in sequence.

$$\begin{array}{r} 1111\ 0000 \\ -)\underline{0111\ 1101} \\ 0111\ 0011 \end{array}$$

next the code (FE) is subtracted.

$$\begin{array}{r} 0111\ 0011 \\ -)\underline{1111\ 1110} \\ 0111\ 0101 \end{array}$$

This procedure is repeated until the last code is subtracted.

$$\begin{array}{r} 0111\ 0101 \\ -)\underline{0010\ 0000} \\ 0101\ 0101 \\ \vdots \end{array}$$

The check sum will be 66.

$$\begin{array}{r} 1110\ 0100 \\ -)\underline{0111\ 1110} \\ 0110\ 0110 \end{array}$$

(5) ROM Code Revisions

After the EPROM or magnetic tape has been submitted, ROM code revisions due to a design change will be accepted before Mask manufacturing begins only. A revised EPROM or magnetic tape must be submitted also.

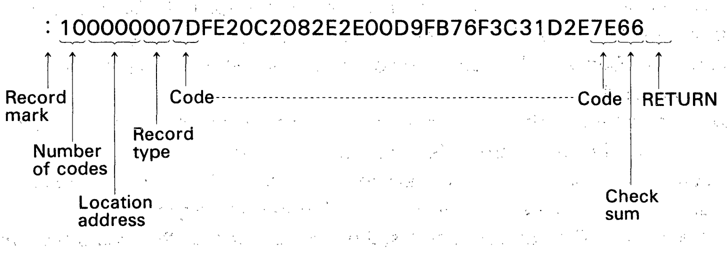
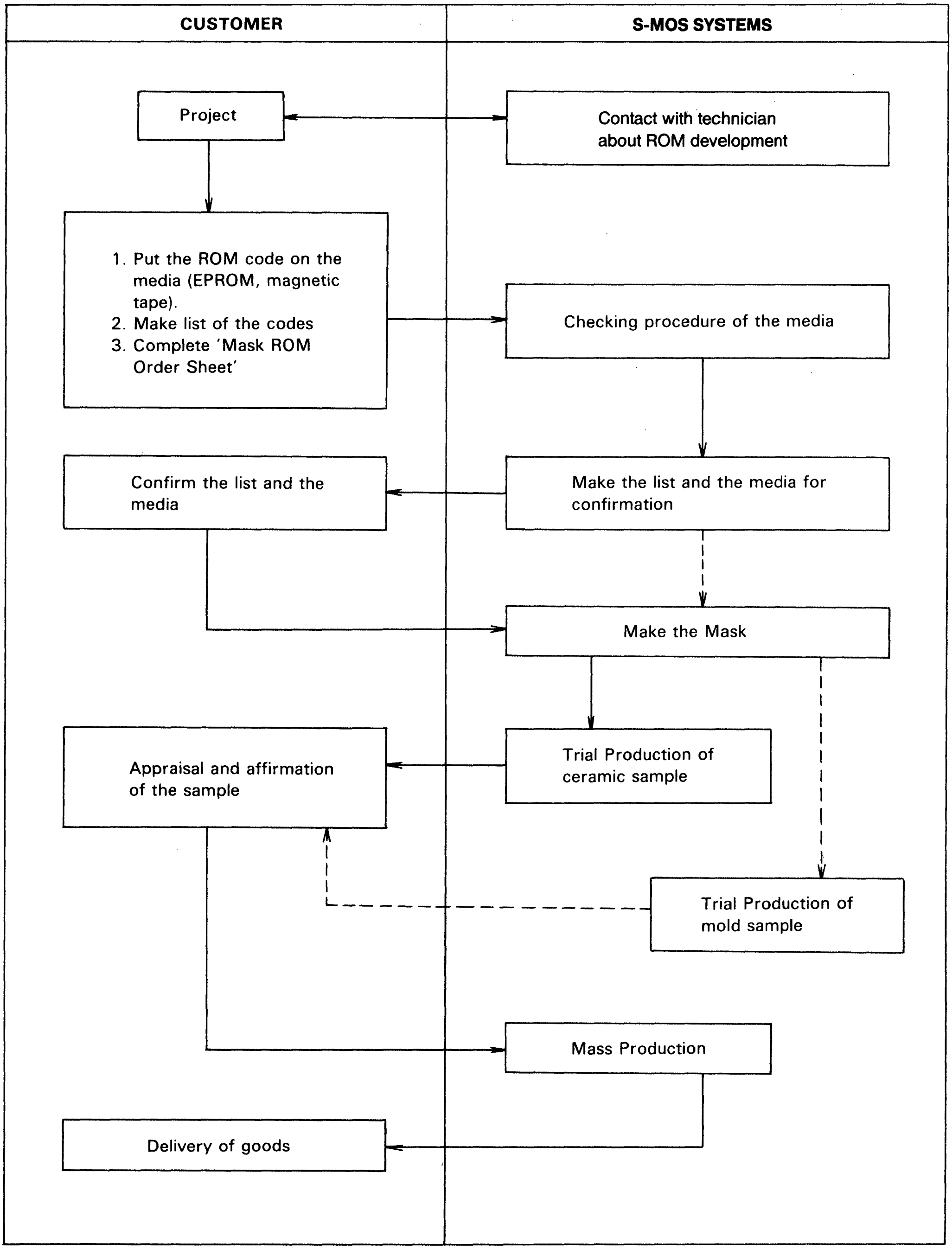


Fig. 5-1 Data Format

5.1.2 Flow Chart of Mask ROM Development



Development Routine

(1) The solid line indicates the standard development procedure.
(2) The dotted line indicates the procedure at customer's request.

Schedule

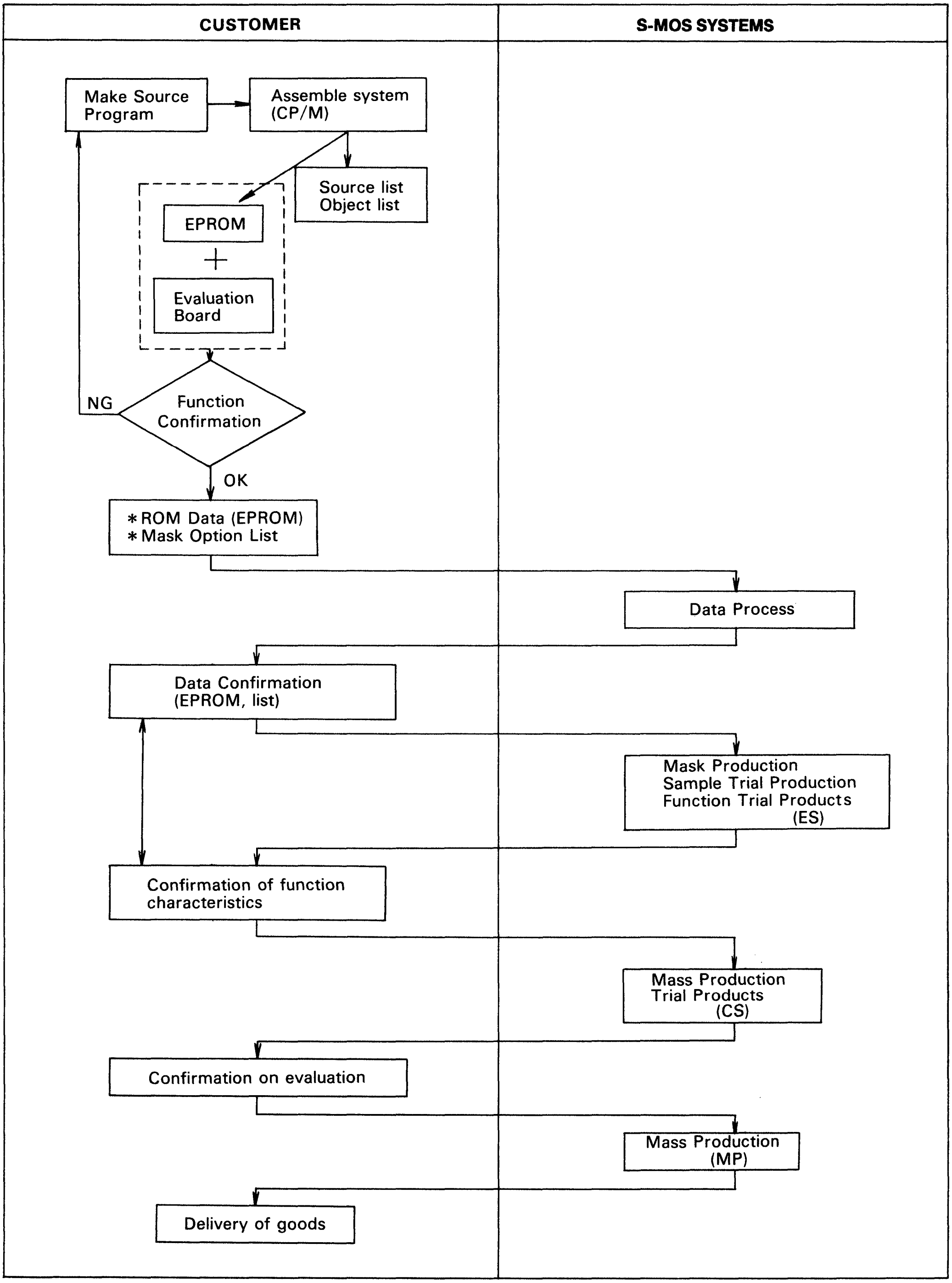
(1) Five weeks (standard) — from list confirmation to ceramic sample
(2) Six weeks (standard) — from list confirmation to mold sample
(3) Six weeks (standard) — from sample confirmation to the delivery of goods

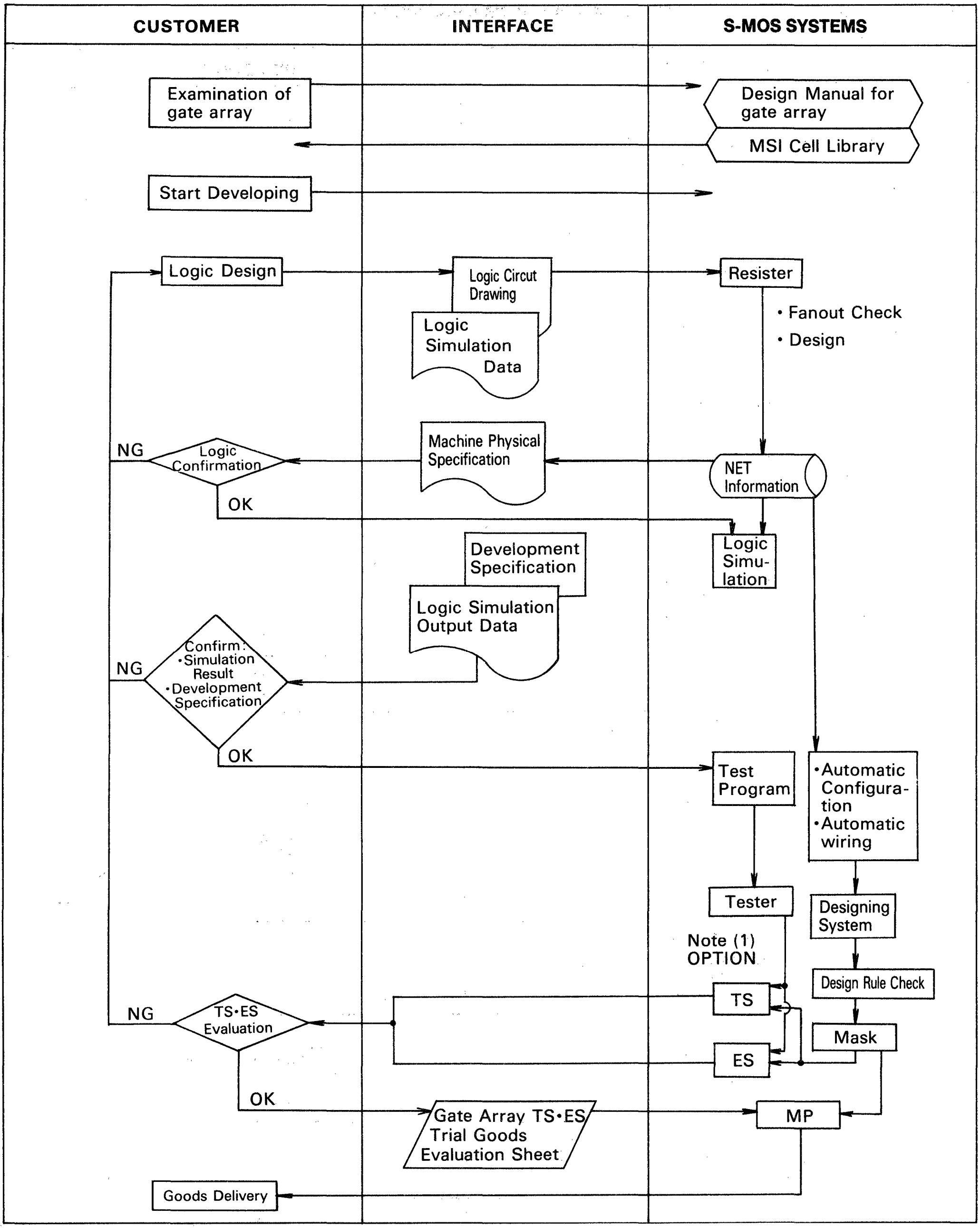
Quantity

(1) Normally, five ceramic samples are included in the mask charge.
(2) Normally, less than one hundred mold samples are available with the charge.

Flow Chart of Single-chip Microcomputer ROM Development (Table 5.1.3)
(1) Please refer to the "Order of Mask ROM custom code pattern" for making the ROM data (EPROM).
(2) CS may be omitted by mutual agreement of the customer and S-MOS Systems.
(3) If S-MOS Systems develops the software, the evaluation instruments for the LCD Panel and its Objective System must be prepared by the customer for S-MOS Systems.

5.1.3 Flow Chart of Single-chip Microcomputer ROM Development

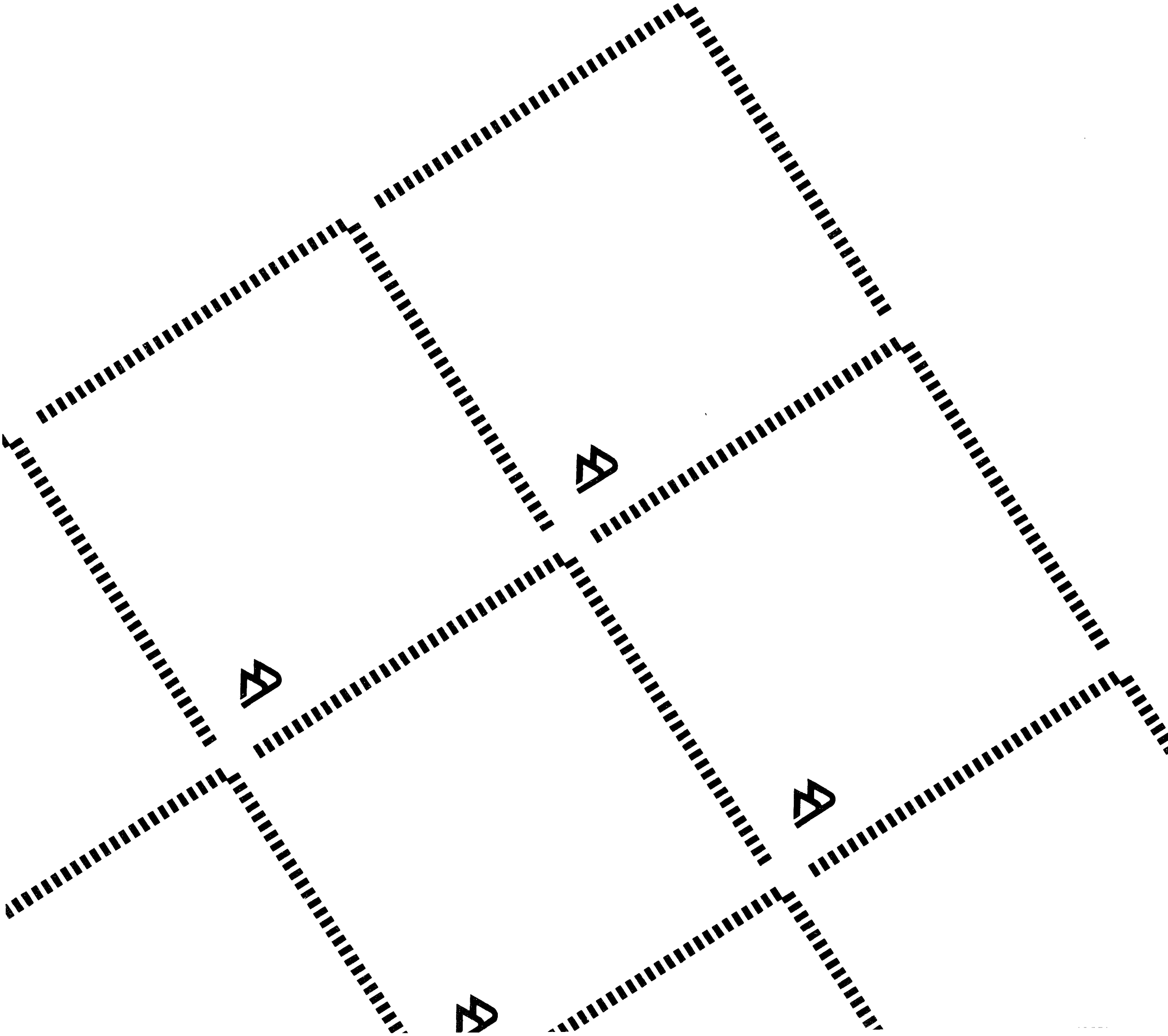




NOTE) 1. TS is available upon request. Its packaging form is different from that of mass production.
2. Since the time for delivery is based on the standard, there may be some small differences between the scheduled date and the actual delivery date.
3. Twenty ESs are included in the cost for development.

1988/1989 CMOS DATA BOOK

A. MEMORIES



PF217-03

SRM2114C$_{25/L7}$

CMOS 4K-BIT STATIC RAM

●Low Supply Current

●Access Time 250ns/700ns

●1,024 Words×4 Bits

■DESCRIPTION

The SRM2114C$_{25/L7}$ is a 1,024 words×4 bits asynchronous, static, random access memory on a monolithic CMOS chip. Its very low standby current consumption makes it ideal for applications requiring non-volatile storage with back-up batteries. The static nature of the memory requires no external clock or refreshing circuit.

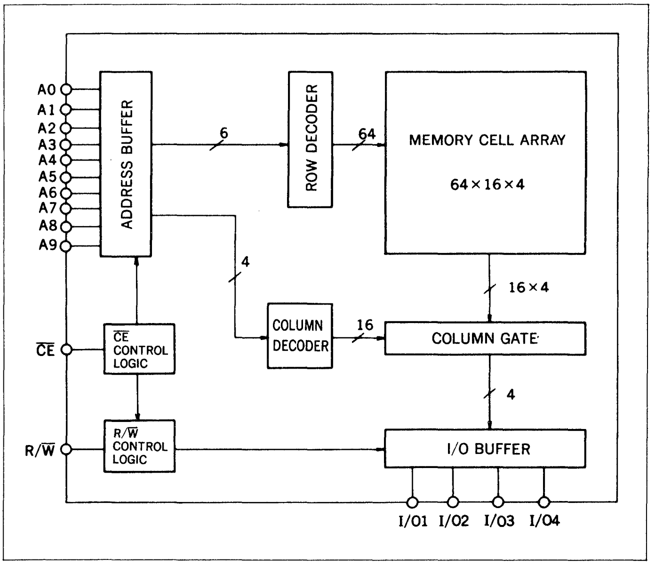
Both the input and output ports are TTL compatible; and the three-state output allows easy expansion of memory capacity. These features make the SRM2114C$_{25/L7}$ usable for widerange of applications from microprocessor systems to terminal devices.

The SRM2114C$_{L7}$ is a low power variation of SRM2114C$_{25}$.

■FEATURES

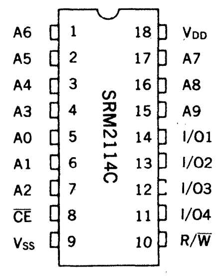
- ●Access time ····················250ns (Max)/700ns (Max)
- ●Single power supply ········5V±10%/3 to 5V
- ●Low supply current ············Standby : 0.1μA (Typ)/0.1μA (Typ)
  Operation : 14mA (Typ)/9mA (Typ)
- ●Completely static operation
- ●TTL compatible inputs and outputs
- ●3-state output with wired-OR capability
- ●Operation with back-up batteries
- ●Package·························18-pin DIP (plastic)
  24-pin SOP (plastic)

■BLOCK DIAGRAM

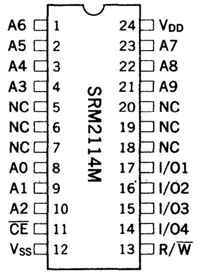


■PIN CONFIGURATION

● 18-pin DIP



● 24-pin SOP



NC : no connection

■PIN DESCRIPTION

A0 to A9	Address Input
R/W	Read/Write
CE	Chip Enable
I/O1 to 4	Data Input/Output
V_{DD}	Power Supply (+)
V_{SS}	Power Supply (−)

■ABSOLUTE MAXIMUM RATINGS

($V_{SS}=0V$)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.5 to 7.0	V
Input voltage	V_I	−0.5 to 7.0	V
I/O voltage	$V_{I/O}$	−0.5 to V_{DD}+0.3	V
Power dissipation	P_D	1.0	W
Operating temperature	T_{opr}	−40 to 85 [−10 to 70]	°C
Storage temperature	T_{stg}	−65 to 150	°C
Soldering temperature and time	T_{sol}	260°C, 10s (at lead)	—

[ ]: SRM2114C$_{L7}$

■RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	SRM2114C$_{25}$			SRM2114C$_{L7}$			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply voltage	V_{DD}	4.5	5.0	5.5	3.0	4.5	5.0	V
	V_{SS}	—	0	—	—	0	—	
Input voltage	V_{IH}	2.2	—	V_{DD}+0.3	V_{DD}−0.4	—	V_{DD}+0.3	V
	V_{IL}	−0.3	—	0.8	−0.3	—	0.4	V

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

(SRM2114C$_{25}$……$V_{DD}=5V\pm10\%$, $V_{SS}=0V$, Ta=−40 to 85°C)
(SRM2114C$_{L7}$……$V_{DD}=3$ to 5V, $V_{SS}=0V$, Ta=−10 to 70°C)

Parameter	Symbol	SRM2114C$_{25}$				SRM2114C$_{L7}$				Unit
		Conditions	Min	Typ	Max	Conditions	Min	Typ	Max	
Input leakage Current	I_{LI}	$V_I=0$ to V_{DD}	−1.0	—	1.0	$V_I=0$ to V_{DD}	−1.0	—	1.0	μA
Standby supply current	I_{DDS}	$\overline{CE}=V_{DD}-0.2V$	—	0.1	5	$\overline{CE}=V_{DD}-0.2V$	—	0.1	5	μA
Operating supply current	I_{DDO}	$\overline{CE}=V_{IL}$ *$C_L=100pF$	—	*14	*35	$\overline{CE}=V_{IL}$ $t_{RC}=1000ns$	—	6	10	mA
						$I_0=0mA$ $t_{RC}=700ns$	—	9	15	
Output leakage current	I_{LO}	$V_O=0$ to V_{DD}	−1.0	—	1.0	$V_O=0$ to V_{DD}	−1.0	—	1.0	μA
High level output voltage	V_{OH}	$I_{OH}=-1.0mA$	2.4	—	—	$I_{OH}=-100\mu A$	V_{DD}−0.2	—	—	V
Low level output voltage	V_{OL}	$I_{OL}=2.0mA$	—	—	0.4	$I_{OL}=100\mu A$	—	—	0.2	V

* $C_L=0pF$ Typ7 Max25

●Terminal Capacitance

(f=1MHz, SRM2114C$_{25}$……$V_{DD}=5V\pm10\%$, $V_{SS}=0V$, Ta=−40 to 85°C
SRM2114C$_{L7}$……$V_{DD}=3$ to 5V, $V_{SS}=0V$, Ta=−10 to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C_I	$V_I=0V$	—	—	7	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}=0V$	—	—	10	pF

●AC Electrical Characteristics

○Read Cycle

(SRM2114C$_{25}$……$V_{DD}=5V\pm10\%$, $V_{SS}=0V$, Ta=−40 to 85°C)
(SRM2114C$_{L7}$……$V_{DD}=3$ to 5V, $V_{SS}=0V$, Ta=−10 to 70°C)

Parameter	Symbol	Conditions	SRM2114C$_{25}$		SRM2114C$_{L7}$		Unit
			Min	Max	Min	Max	
Read cycle time	t_{RC}	*1	250	—	700	—	ns
Address access time	t_{ACC}		—	250	—	700	ns
$\overline{CE}$ access time	t_{ACE}		—	250	—	700	ns
$\overline{CE}$ output set time	t_{CLZ}	*2	0	—	0	—	ns
$\overline{CE}$ output floating	t_{CHZ}		—	120	—	140	ns
Output hold time	t_{OH}	*1	10	—	10	—	ns

○Write Cycle

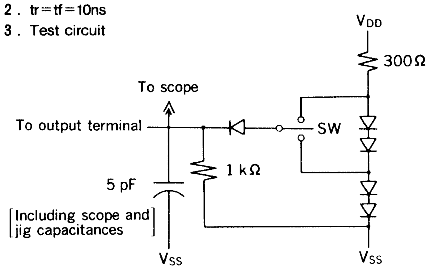
Parameter	Symbol	Conditions	SRM2114C25		SRM2114CL7		Unit
			Min	Max	Min	Max	
Write cycle time	t_{WC}	*1	250	—	700	—	ns
Address setup time	t_{AS}		0	—	0	—	ns
Write pulse width	t_{WP}		150	—	420	—	ns
Address hold time	t_{WR}		0	—	0	—	ns
Input data setup time	t_{DW}		100	—	280	—	ns
Input data hold time	t_{DH}		0	—	0	—	ns
R/$\overline{W}$ Output floating	t_{WHZ}	*3	—	120	—	140	ns

*1 Test conditions. [( ):SRM2114CL7]

1. Input pulse level: 0.8 to 2.2V ($V_{DD}-0.4V$ to 0.4V)
2. tr=tf=10ns
3. Output load: $I_{TTL}+C_L=100pF$ [Including scope and jig capacitances] ($C_L=100pF$)
4. Timing reference level: 1.5V ($V_{DD}/2$)

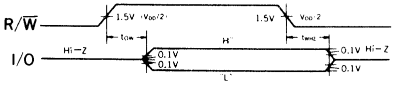
*3 Test conditions

1. Input pulse level: 0.8 to 2.2V ($V_{DD}-0.4V$ to 0.4V)
2. tr=tf=10ns
3. Test circuit



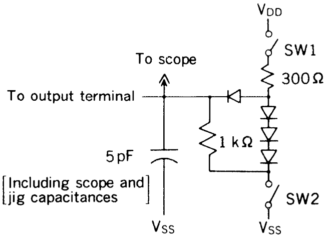
- ○SW is set to the V_{DD} side when measuring Hi-Z→"High" and "High"→Hi-Z of t_{OW} or t_{WHZ}.
- ○SW is set to the V_{SS} side when measuring Hi-Z→"Low" and "Low"→Hi-Z of t_{OW} or t_{WHZ}.

Output turn-on turn-off times



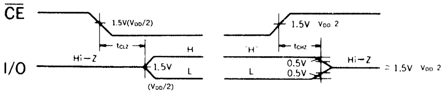
*2 Test conditions

1. Input pulse level: 0.8 to 2.2V ($V_{DD}-0.4V$ to 0.4V)
2. tr=tf=10ns
3. Test circuit



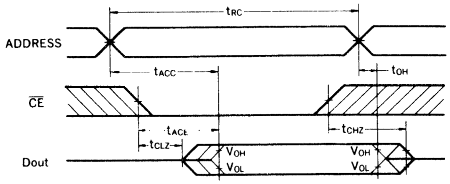
- ○SW1, SW2 are closed when measuring t_{CHZ}.
- ○SW1 is open, SW2 is closed when measuring Hi-Z→"High" of t_{CLZ}.
- ○SW1 is closed, SW2 is open when measuring Hi-Z→"Low" of t_{CLZ}.

Output turn-on turn-off times



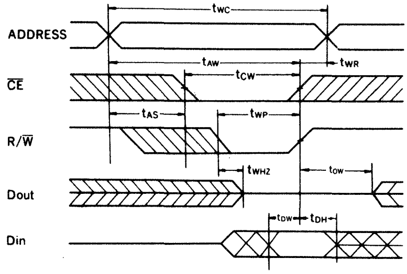
●Timing Chart

○Read Cycle



* R/$\overline{W}$ is "High" during read cycle.

○Write Cycle



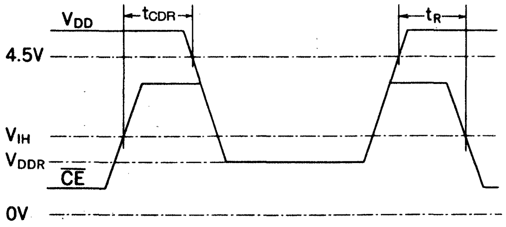
■DATA RETENTION CHARACTERISTICS WITH LOW SUPPLY VOLTAGE

(SRM2114C25······Ta = −40 to 85°C)
(SRM2114CL7······Ta = −10 to 70°C)

Parameter	Symbol	Conditions		SRM2114C25			SRM2114CL7			Unit
		SRM2114C25	SRM2114CL7	Min	Typ	Max	Min	Typ	Max	
Data retention supply voltage	V_{DDR}	$V_I = 0$ or V_{DD}, $\overline{CE} = V_{DD}$		2.0	—	5.5	2.0	—	5.0	V
Data retention supply current	I_{DDR}	$V_{DD}=2.0V$, 25°C	$V_{DD}=3.0V$, 25°C	—	—	2	—	—	2.5	μA
$\overline{CE}$ setup time	t_{CDR}	Refer to the figure below		0	—	—	0	—	—	ns
$\overline{CE}$ recovery time	t_R			t_{RC}*	—	—	t_{RC}*	—	—	ns

*t_{RC}: Read cycle time

Data retention timing



* When retaining data in standby mode, supply voltage can be lowered within a certain range. But read or write cycle cannot be performed while the supply voltage is low.

■FUNCTIONS

●Truth Table

$\overline{CE}$	R/$\overline{W}$	A0 to A9	DATA I/O	MODE
H	X	X	Hi-Z	Unselected
L	L	Stable	Input data	Write
L	H	Stable	Output data	Read

X: "H" or "L"

●Reading Data

Data can be read out if an address is set while $\overline{CE}$ is "Low", and R/$\overline{W}$ is "High".

●Writing Data

There are the following two ways of writing data into the memory.

(1) Hold $\overline{CE}$ "L", set the address, and apply low level pulse to R/$\overline{W}$.

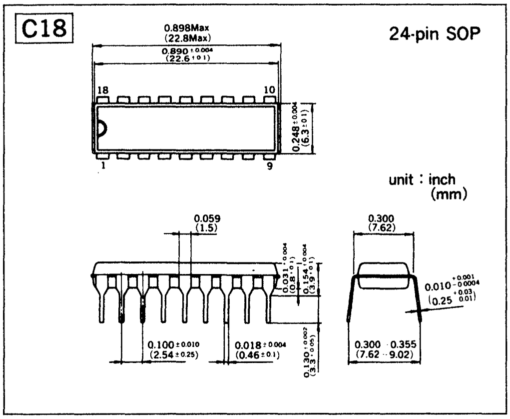
(2) Set the address and apply Low level pulse to $\overline{CE}$ and R/$\overline{W}$.

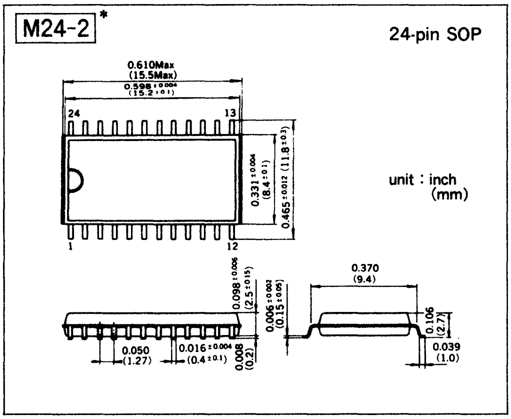
In each case, data from the DATA I/O terminal is latched at the positive transition of "L" pulse of $\overline{CE}$ or R/$\overline{W}$. The DATA I/O terminal is in high-impedance state when $\overline{CE}$ is "H" or R/$\overline{W}$ is "L", so competition of data driver and memory output can be avoided.

●Standby Mode

When $\overline{CE}$ is "H", SRM2114C$_{25/L7}$ is in standby mode and only retains the data. In this mode, DATA I/O terminals are in high-impedance state, and all inputs of addresses, R/$\overline{W}$, or data can be any "H" or "L". The current flowing in the SRM2114C$_{25/L7}$ is only leakage current.

■PACKAGE DIMENSIONS

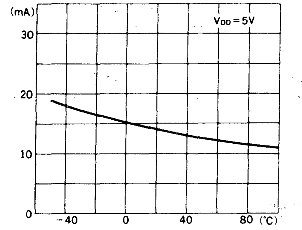




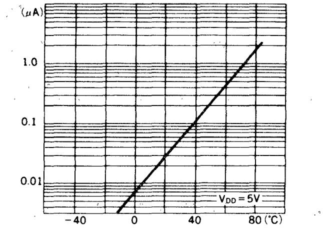
*Represents model SRM2114M$_{25/L7}$ that has the same electrical characteristics as model SRM2114C$_{25/L7}$.

■CHARACTERISTICS CURVES

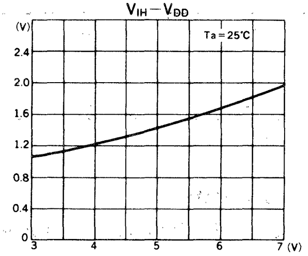
$I_{DDO}-Ta$



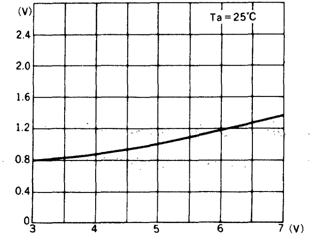
$I_{DDS}-Ta$



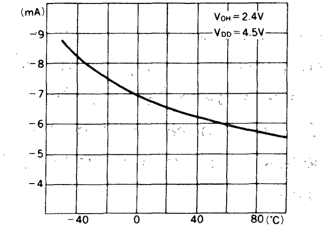
$V_{IH}-V_{DD}$



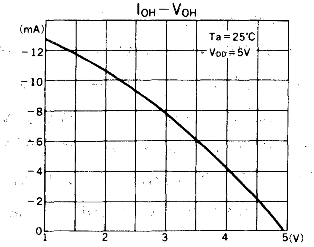
$V_{IL}-V_{DD}$



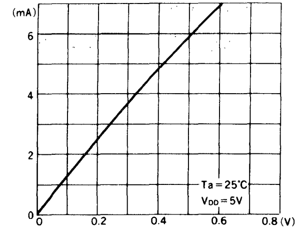
$I_{OH}-Ta$



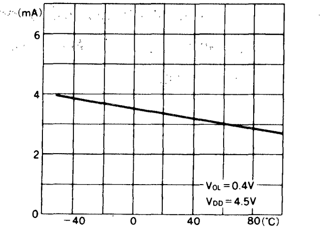
$I_{OH}-V_{OH}$



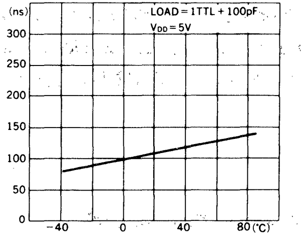
$I_{OL}-V_{OL}$



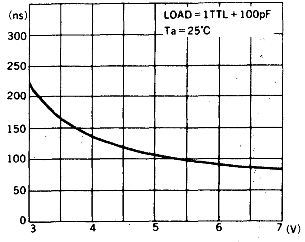
$I_{OL}-Ta$



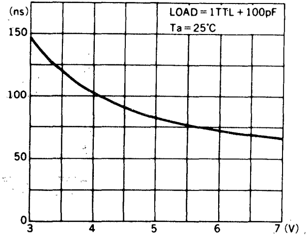
$t_{ACC}-Ta$



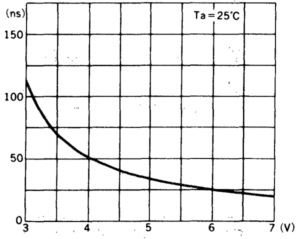
$t_{ACC}-V_{DD}$



$t_{ACE}-V_{DD}$



$t_{WP}-V_{DD}$



SRM2016C$_{10/12}$

CMOS 16K-BIT STATIC RAM

- ●Low Supply Current
- ●Access Time 100ns/120ns
- ●2,048 Words × 8 Bits Asynchronous

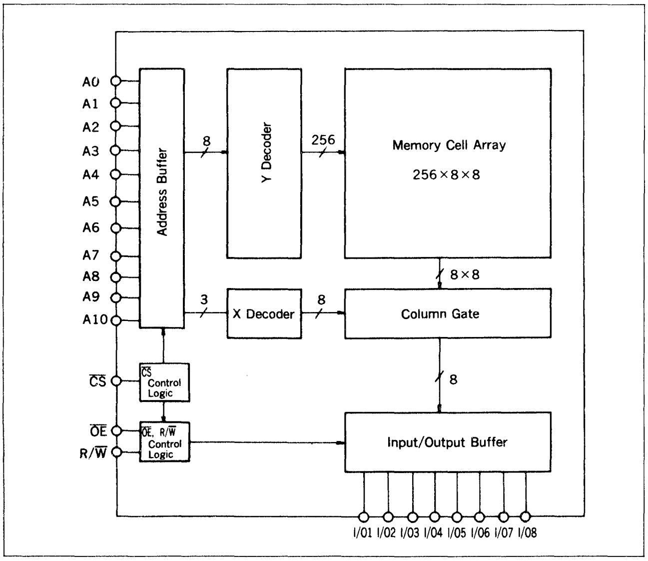
■DESCRIPTION

The SRM2016C$_{10/12}$ is a 2,048 words × 8 bits asynchronous, static, random access memory on a monolithic CMOS chip. Its very low standby power requirement makes it ideal for applications requiring non-volatile storage with back-up batteries. The asynchronous and static nature of the memory requires no external clock or refreshing circuit. Both the input and output ports are TTL compatible and the 3-state output allows easy expansion of memory capacity.

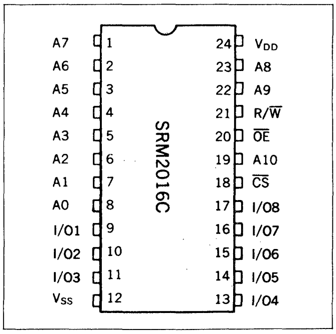
■FEATURES

●Access time ··········SRM2016C$_{10}$ 100ns (Max)
SRM2016C$_{12}$ 120ns (Max)
●Low supply current ··········standby : 1μA (Typ)
operation : SRM2016C$_{10}$ 30mA (Typ)
SRM2016C$_{12}$ 25mA (Typ)
●Complete static operation
●Single power supply ··········5V±10%
●TTL compatible inputs and outputs
●3-state output with wired-OR capability
●Non-volatile storage with back-up batteries
●Package··········SRM2016C$_{10/12}$ 24-pin DIP (plastic)
SRM2016M$_{10/12}$ 24-pin SOP (plastic)
SRM2016N$_{10/12}$ 24-pin Skinny DIP (plastic)

■BLOCK DIAGRAM



■PIN CONFIGURATION



■PIN DESCRIPTION

A0 to A10	Address Input
R/$\overline{W}$	Read/Write
$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Select
I/O1 to 8	Data Input/Output
V_{DD}	Power Supply (+5V)
V_{SS}	Power Supply (0V)

■ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.5 to 7.0	V
Input voltage*	V_I	−0.5 to 7.0	V
Input/output voltage*	$V_{I/O}$	−0.5 to V_{DD}+0.3	V
Power dissipation	P_D	1.0	W
Operating temperature	T_{opr}	0 to 70	℃
Storage temperature	T_{stg}	−65 to 150	℃
Soldering temp. & time	T_{sol}	260°C, 10s (at lead)	—

*V_I, $V_{I/O}$= −1.0V when pulse width is 50 ns

■RECOMMENDED OPERATING CONDITIONS

(Ta=0 to 70℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
	V_{SS}		0	0	0	V
Input voltage	V_{IH}		2.2	3.5	V_{DD}+0.3	V
	V_{IL}		−0.3*	—	0.8	V

*V_{IL}(Min)= −1.0V when pulse width is 50ns

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

(V_{DD}=5V±10%, V_{SS}=0V, Ta=0 to 70℃)

Parameter	Symbol	Conditions	SRM2016C10			SRM2016C12			Unit
			Min	Typ*	Max	Min	Typ*	Max	
Input leakage current	I_{LI}	V_{DD}=5.5V, V_I=0 to V_{DD}	−1	—	1	−1	—	1	μA
Output leakage current	I_{LO}	$\overline{CS}$=V_{IH}, or $\overline{OE}$=V_{IH}, $V_{I/O}$=0 to V_{DD}	−1	—	1	−1	—	1	μA
Operating supply current	I_{DDO}	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA	—	30	60	—	25	50	mA
	I_{DDO1}	V_{IH}=3.5V, V_{IL}=0.6V, $I_{I/O}$=0mA	—	16	—	—	16	—	mA
Average operating current	I_{DDA}	Min. cycle, duty=100%, $I_{I/O}$=0mA	—	30	60	—	25	50	mA
Standby supply current	I_{DDS}	$\overline{CS}$=V_{IH}	—	1.5	3.0	—	1.5	3.0	mA
	I_{DDS1}	$\overline{CS}$=V_{DD}−0.2V	—	1	50	—	1	50	μA
Output voltage	V_{OL}	I_{OL}=4.0mA	—	—	0.4	—	—	0.4	V
	V_{OH}	I_{OH}= −1.0mA	2.4	—	—	2.4	—	—	V

* Typical values are for reference, with V_{DD}=5V and Ta=25℃ assumed

●Terminal Capacitance

(f=1MHz, Ta=25℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C_I	V_I=0V	—	4	6	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	6	8	pF

●AC Electrical Characteristics

○**Read Cycle**

(V_{DD}=5V±10%, V_{SS}=0V, Ta=0 to 70℃)

Parameter	Symbol	Conditions	SRM2016C10		SRM2016C12		Unit
			Min	Max	Min	Max	
Read cycle time	t_{RC}	*1	100	—	120	—	ns
Address access time	t_{ACC}		—	100	—	120	ns
$\overline{CS}$ access time	t_{ACS}		—	100	—	120	ns
$\overline{CS}$ output setup time	t_{CLZ}	*2	10	—	10	—	ns
$\overline{OE}$ access time	t_{OE}	*1	—	55	—	60	ns
$\overline{OE}$ output setup time	t_{OLZ}	*2	5	—	10	—	ns
$\overline{CS}$ output floating	t_{CHZ}		0	40	0	40	ns
$\overline{OE}$ output floating	t_{OHZ}		0	40	0	40	ns
Output hold time	t_{OH}	*1	10	—	10	—	ns

○ **Write Cycle**

(V_{DD}=5V±10%, V_{SS}=0V, Ta=0 to 70°C)

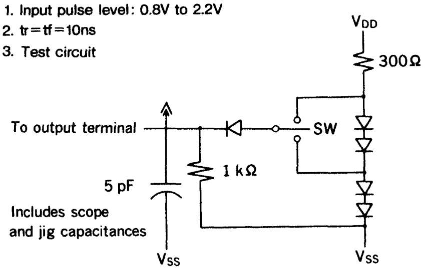
Parameter	Symbol	Conditions	SRM2016C10		SRM2016C12		Unit
			Min	Max	Min	Max	
Write cycle time	t_{WC}	*1	100	—	120	—	ns
Chip select time ($\overline{\text{CS}}$)	t_{CW}		80	—	85	—	ns
Address enable time	t_{AW}		80	—	85	—	ns
Address setup time	t_{AS}		0	—	0	—	ns
Write pulse width	t_{WP}		65	—	70	—	ns
$\overline{\text{OE}}$ output floating	t_{OHZ}	*2	0	40	0	40	ns
R/$\overline{\text{W}}$ output floating	t_{WHZ}	*3	0	45	0	50	ns
Input data setup time	t_{DW}	*1	45	—	50	—	ns
Address hold time	t_{WR}		5	—	5	—	ns
Input data hold time	t_{DH}		0	—	0	—	ns
R/$\overline{\text{W}}$ output setup time	t_{OW}	*3	5	—	10	—	ns

*1 Test conditions.

1. Input pulse level: 0.8V to 2.2V
2. tr=tf=10ns
3. Input/output timing reference level: 1.5V
4. Output load: I_{TTL}+C_L=100pF

*3 Test conditions.

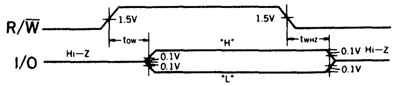
1. Input pulse level: 0.8V to 2.2V
2. tr=tf=10ns
3. Test circuit



○ SW is set to the VDD side when measuring Hi-z-high and high-Hi-z of tOW or tWHZ.

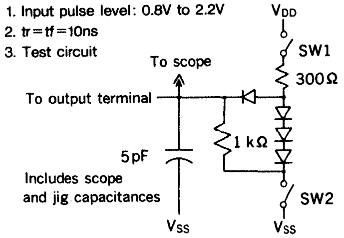
○ SW is set to the Vss side when measuring Hi-z-low and low-Hi-z of tOW or tWHZ.

Output turn-on turn-off times



*2 Test conditions.

1. Input pulse level: 0.8V to 2.2V
2. tr=tf=10ns
3. Test circuit

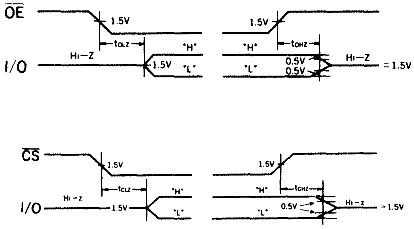


○ Both SW1 and SW2 are closed when measuring tCHZ or tOHZ.

○ SW1 is open and SW2 is closed when measuring Hi-z-high of tOLZ or tCLZ.

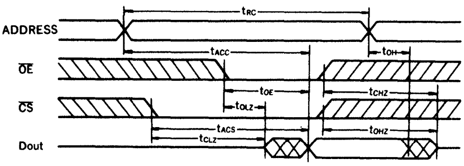
○ SW1 is closed and SW2 is open when measuring Hi-z-low of tOLZ or tCLZ.

Output turn-on turn-off times

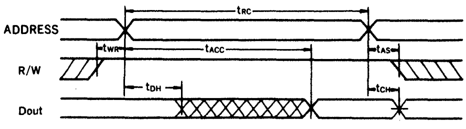


● Timing Chart

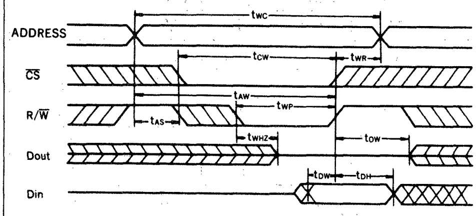
○ Read cycle 1 ($\overline{\text{OE}}$, $\overline{\text{CS}}$ control, R/$\overline{\text{W}}$=high)



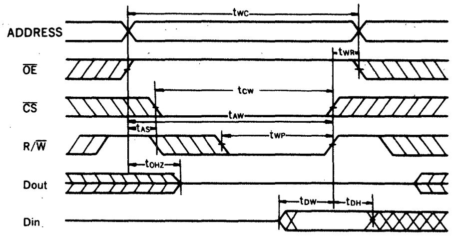
○ Read cycle 2 (R/$\overline{\text{W}}$ control, $\overline{\text{OE}}$=low, $\overline{\text{CS}}$=low)



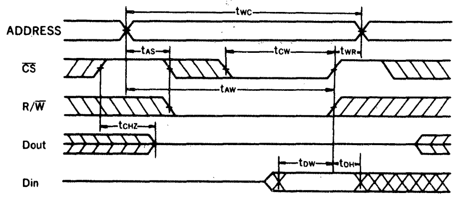
○Write cycle 1 (R/$\overline{W}$ control, OE=low)



○Write cycle 2 (R/$\overline{W}$ control)



○Write cycle 3 (CS control, OE=low)



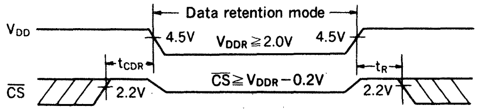
■DATA RETENTION CHARACTERISTICS WITH LOW VOLTAGE POWER SUPPLY

(Ta=0 to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDR}	$\overline{CS} \geqq V_{DDR}-0.2V$	2.0	—	5.5	V
Data retention current	I_{DDR}	$V_{DD}=3.0V$, $\overline{CS} \geqq 2.8V$	—	—	25	μA
Chip select data hold time	t_{CDR}	Refer to the figure below.	0	—	—	ns
Operation recovery time	t_R		t_{RC}*	—	—	ns

* t_{RC} : read cycle time

Data retention timing



Note: When retaining data in standby mode, supply voltage can be lowered within a certain range. Read or write cycle cannot be performed while the supply voltage is low.

■FUNCTIONS

●Truth Table

$\overline{CS}$	$\overline{OE}$	R/$\overline{W}$	A0 to A10	DATA I/O	Mode	I_{DD}
H	—	—	—	Hi-Z	Unselected	I_{DDS}, I_{DDS1}
L	L	H	Stable	Output data	Read	I_{DDO}
L	H	L	Stable	Input data	Write	I_{DDO}
L	L	L	Stable	Input data	Write	I_{DDO}

X: "H" or "L" —: "H", "L" or "Hi

●Reading Data

Data can be read out if an address is set while $\overline{CS}$ and $\overline{OE}$ are held low, and R/$\overline{W}$ is held high.

●Writing Data

There are the following three ways of writing data into the memory.

(1) Hold $\overline{CS}$ low, set the address, and apply a low pulse to R/$\overline{W}$.

(2) Hold R/$\overline{W}$ low, set the address, and apply a low pulse to $\overline{CS}$.

(3) Set the address, then apply low pulses to both $\overline{CS}$ and R/$\overline{W}$.

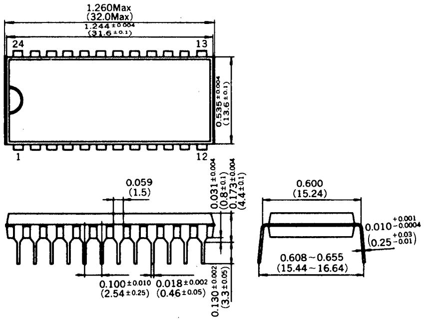
In each case, data from the DATA I/O terminal is fetched into the SRM2016C$_{10/12}$ at the last transition of a section in which both $\overline{CS}$ and R/$\overline{W}$ are low. Because the DATA I/O terminal is in high-impedance state when $\overline{CS}$ or $\overline{OE}$ is high, or R/$\overline{W}$ is low, contention of the data driver on the bus and memory output is avoided.

●Standby Mode

When $\overline{CS}$ is high, SRM2016C$_{10/12}$ is in the stand-by mode and only retains the data. At this time the DATA I/O terminal is in high-impedance state and input of an address, R/$\overline{W}$ signal, or data is prohibited. When $\overline{CS}$ is above V$_{DD}$−0.2V,current flowing within the SRM2016C$_{10/12}$ chip is only that in the high-resistance portion of the memory cells and leakage current.

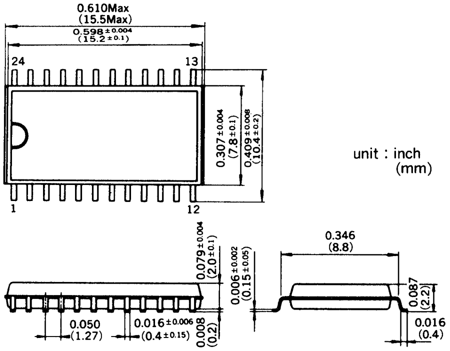
■PACKAGE DIMENSIONS

C24 24-pin DIP

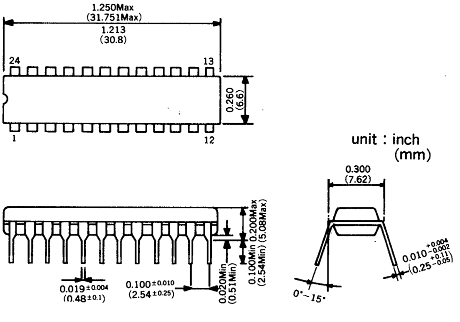


unit : inch (mm)

M24 *1 24-pin SOP



N24 *2 24-pin Skinny DIP



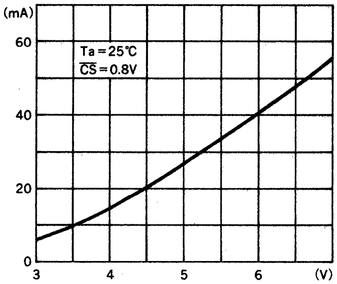
*1 Represents model SRM2016M$_{10/12}$ that has the same electrical characteristics as model SRM2016C$_{10/12}$.

*2 Represents model SRM2016N$_{10/12}$ that has the same electrical characteristics as model SRM2016C$_{10/12}$.

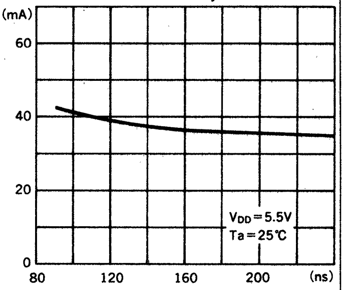
■CHARACTERISTICS CURVES

I_{DDO}—Ta

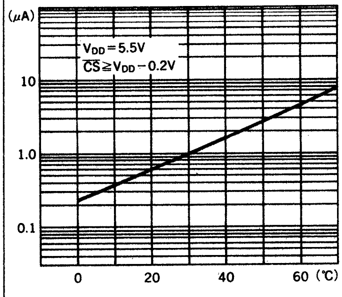
I_{DDO}—V_{DD}



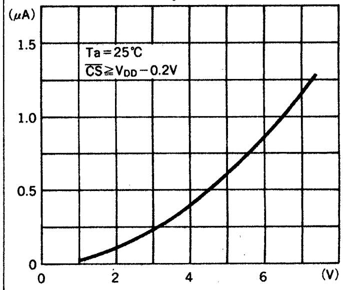
I_{DDA}—t_{cyc}



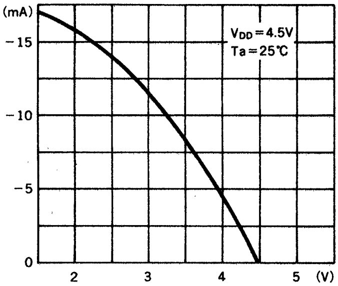
I_{DDS1}—Ta



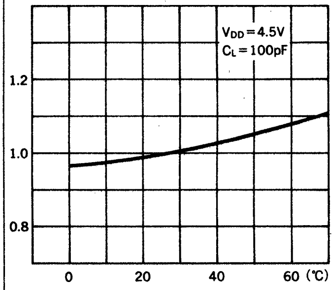
I_{DDS1}—V_{DD}



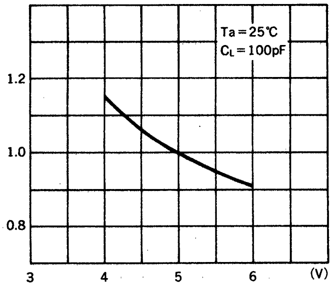
I_{OH}—V_{OH}



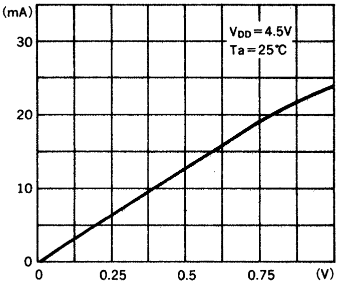
Normalized t_{ACC}·t_{ACS}·t_{OE}—Ta



Normalized t_{ACC}·t_{ACS}·t_{OE}—V_{DD}



I_{OL}—V_{OL}



SRM2017C$_{10/12}$

CMOS 16K-BIT STATIC RAM

- ●Low Supply Current
- ●Access Time 100ns/120ns
- ●2,048 Words×8 Bits Asynchronous

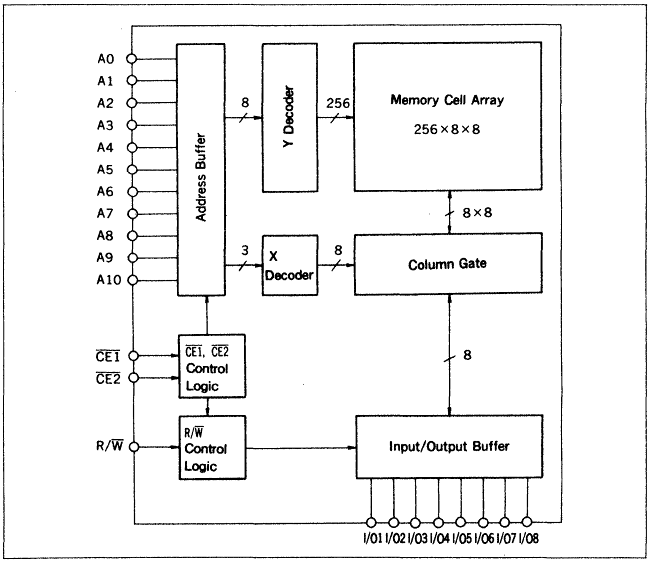
■DESCRIPTION

The SRM2017C$_{10/12}$ is a 2,048 words × 8 bits asynchronous, static, random access memory on a monolithic CMOS chip. Its very low standby power requirement makes it ideal for applications requiring non-volatile storage with back-up batteries. The asynchronous and static nature of the memory requires no external clock or refreshing circuit. Both the input and output ports are TTL compatible and the 3-state output allows easy expansion of memory capacity.

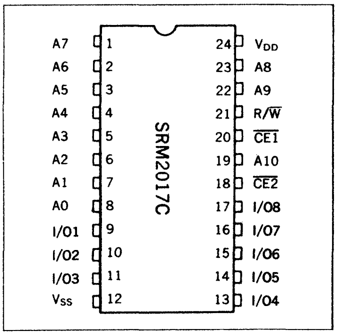
■FEATURES

- ●Access time ······························SRM2017C$_{10}$ 100ns (Max)
  SRM2017C$_{12}$ 120ns (Max)
- ●Low supply current ······························standby : 1μA (Typ)
  operation : SRM2017C$_{10}$ 30mA (Typ)
  SRM2017C$_{12}$ 25mA (Typ)
- ●Complete static operation
- ●Single power supply ······························5V±10%
- ●TTL compatible inputs and outputs
- ●3-state output with wired-OR capability
- ●Non-volatile storage with back-up batteries
- ●Package······························SRM2017C$_{10/12}$ 24-pin DIP (plastic)
  SRM2017M$_{10/12}$ 24-pin SOP (plastic)
  SRM2017N$_{10/12}$ 24-pin Skinny DIP (plastic)

■BLOCK DIAGRAM



■PIN CONFIGURATION



■PIN DESCRIPTION

A0 to A10	Address Input
R/$\overline{W}$	Read/Write
$\overline{CE1}$	Chip Enable 1
$\overline{CE2}$	Chip Enable 2
I/O1 to 8	Data Input/Output
V_{DD}	Power Supply (+5V)
V_{SS}	Power Supply (0V)

■ABSOLUTE MAXIMUM RATINGS

($V_{SS}=0V$)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.5 to 7.0	V
Input voltage*	V_I	−0.5 to 7.0	V
Input/output voltage*	$V_{I/O}$	−0.5 to $V_{DD}+0.3$	V
Power dissipation	P_D	1.0	W
Operating temperature	T_{opr}	0 to 70	℃
Storage temperature	T_{stg}	−65 to 150	℃
Soldering temp. & time	T_{sol}	260°C, 10s (at lead)	—

*V_I, $V_{I/O}=-1.0V$ when pulse width is 50 ns

■RECOMMENDED OPERATING CONDITIONS

($Ta=0$ to 70℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
	V_{SS}		0	0	0	V
Input voltage	V_{IH}		2.2	3.5	$V_{DD}+0.3$	V
	V_{IL}		−0.3*	—	0.8	V

*V_{IL}(Min)$=-1.0V$ when pulse width is 50ns

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

($V_{DD}=5V\pm10\%$, $V_{SS}=0V$, $Ta=0$ to 70℃)

Parameter	Symbol	Conditions	SRM2017C10			SRM2017C12			Unit
			Min	Typ*	Max	Min	Typ*	Max	
Input leakage current	I_{LI}	$V_{DD}=5.5V, V_I=0$ to V_{DD}	−1	—	1	−1	—	1	μA
Output leakage current	I_{LO}	$\overline{CE1}$ or $\overline{CE2}=V_{IH}, V_{I O}=0$ to V_{DD}	−1	—	1	−1	—	1	μA
Operating supply current	I_{DDO}	$\overline{CE2}=V_{IL}$, $I_{I/O}=0mA$	—	30	60	—	25	50	mA
	I_{DDO1}	$V_{IH}=3.5V, V_{IL}=0.6V, I_{I/O}=0mA$	—	16	—	—	16	—	mA
Average operating current	I_{DDA}	Min. cycle, duty=100%, $I_{I/O}=0mA$	—	30	60	—	25	50	mA
Standby supply current	I_{DDS}	$\overline{CE2}=V_{IH}$	—	1.5	3.0	—	1.5	3.0	mA
	I_{DDS1}	$\overline{CE2}=V_{DD}-0.2V$	—	1	50	—	1	50	μA
Output voltage	V_{OL}	$I_{OL}=4.0mA$	—	—	0.4	—	—	0.4	V
	V_{OH}	$I_{OH}=-1.0mA$	2.4	—	—	2.4	—	—	V

*Typical values are for reference, with $V_{DD}=5V$ and $Ta=25℃$ assumed.

●Terminal Capacitance

($f=1MHz$, $Ta=25℃$)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C_I	$V_I=0V$	—	4	6	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}=0V$	—	6	8	pF

●AC Electrical Characteristics

○**Read Cycle**

($V_{DD}=5V\pm10\%$, $V_{SS}=0V$, $Ta=0$ to 70℃)

Parameter	Symbol	Conditions	SRM2017C10		SRM2017C12		Unit
			Min	Max	Min	Max	
Read cycle time	t_{RC}	*1	100	—	120	—	ns
Address access time	t_{ACC}		—	100	—	120	ns
$\overline{CE1}$ access time	t_{ACE1}		—	55	—	55	ns
$\overline{CE2}$ access time	t_{ACE2}		—	100	—	120	ns
$\overline{CE1}$ output setup time	t_{CLZ1}	*2	10	—	10	—	ns
$\overline{CE1}$ output floating	t_{CHZ1}		0	40	0	40	ns
$\overline{CE2}$ output setup time	t_{CLZ2}		10	—	10	—	ns
$\overline{CE2}$ output floating	t_{CHZ2}		0	40	0	40	ns
Output hold time	t_{OH}	*1	10	—	10	—	ns

○ Write Cycle

($V_{DD}=5V\pm10\%$, $V_{SS}=0V$, Ta=0 to 70°C)

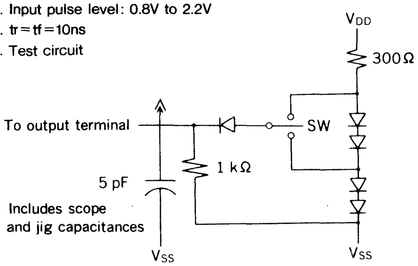
Parameter	Symbol	Conditions	SRM2017C10		SRM2017C12		Unit
			Min	Max	Min	Max	
Write cycle time	t_{WC}	*1	100	—	120	—	ns
Chip select time ($\overline{CE1}$)	t_{CW1}		80	—	85	—	ns
Chip select time ($\overline{CE2}$)	t_{CW2}		80	—	85	—	ns
Address enable time	t_{AW}		80	—	85	—	ns
Address setup time	t_{AS}		0	—	0	—	ns
Write pulse width	t_{WP}		65	—	70	—	ns
Input data setup time	t_{DW}		45	—	50	—	ns
Address hold time	t_{WR}		5	—	5	—	ns
Input data hold time	t_{DH}		0	—	0	—	ns
R/$\overline{W}$ output setup time	t_{OW}	*3	5	—	10	—	ns
R/$\overline{W}$ output floating	t_{WHZ}		0	45	0	50	ns

*1 Test conditions.

1. Input pulse level: 0.8V to 2.2V
2. tr=tf=10ns
3. Input/output timing reference level: 1.5V
4. Output load: $I_{TTL}+C_L=100pF$

*3 Test conditions.

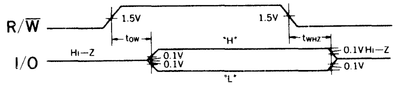
1. Input pulse level: 0.8V to 2.2V
2. tr=tf=10ns
3. Test circuit



○ SW is set to the V_{DD} side when measuring Hi-z-high and high-Hi-z of t_{OW} or t_{WHZ}.

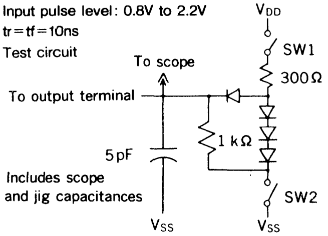
○ SW is set to the V_{SS} side when measuring Hi-z-low and low-Hi-z of t_{OW} or t_{WHZ}.

Output turn-on turn-off times



*2 Test conditions.

1. Input pulse level: 0.8V to 2.2V
2. tr=tf=10ns
3. Test circuit

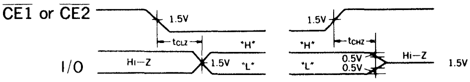


○ Both SW1 and SW2 are closed when measuring t_{CHZ} or t_{OHZ}.

○ SW1 is open and SW2 is closed when measuring Hi-z-high of t_{CLZ} or t_{OLZ}.

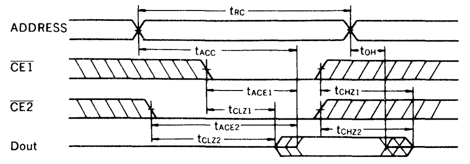
○ SW1 is closed and SW2 is open when measuring Hi-z-low of t_{CLZ} or t_{OLZ}.

Output turn-on turn-off times

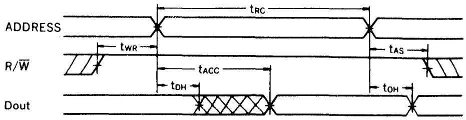


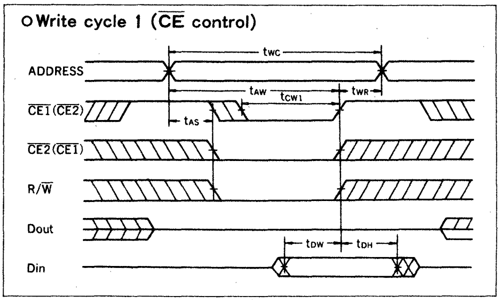
● Timing Chart

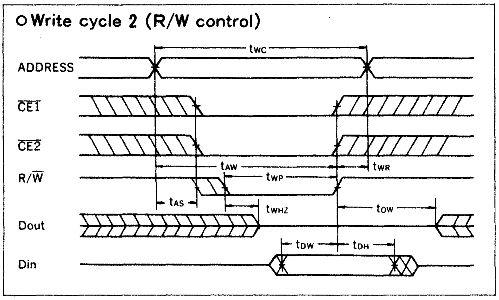
○ Read cycle 1 ($\overline{CE}$ control)



○ Read cycle 2 (R/$\overline{W}$ control, $\overline{CE1}=\overline{CE2}$=low)




○Write cycle 1 ($\overline{CE}$ control)


○Write cycle 2 (R/W control)

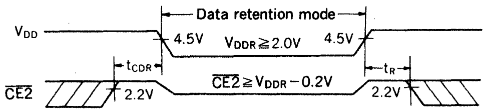
■DATA RETENTION CHARACTERISTICS WITH LOW SUPPLY VOLTAGE

(Ta=0 to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDR}	$\overline{CE2} \geqq V_{DDR} - 0.2V$	2.0	—	5.5	V
Data retention current	I_{DDR}	$V_{DD} = 3.0V$, $\overline{CE2} \geqq 2.8V$	—	—	25	μA
Chip select data hold time	t_{CDR}	Refer to the figure below.	0	—	—	ns
Operation recovery time	t_R		t_{RC}*	—	—	ns

* t_{RC} : read cycle time

Data retention timing



Note: When retaining data in the stand-by mode, supply voltage can be lowered within a certain range. Read or write cycle cannot be performed while the supply voltage is low.

■FUNCTIONS

●Truth Table

$\overline{CE1}$	$\overline{CE2}$	R/W	A0 to A10	DATA I/O	Mode	I_{DD}
—	H	—	—	Hi-Z	Unselected	I_{DDS}, I_{DDS1}
H	L	X	X	Hi-Z	Unselected	I_{DDO}
L	L	H	Stable	Output data	Read	I_{DDO}
L	L	L	Stable	Input data	Write	I_{DDO}

X: "H" or "L" —: "H", "L" or "Hi-Z"

●Reading Data

Data can be read out if an address is set while $\overline{CE1}$ is held low, and R/$\overline{W}$ is held high.

●Writing Data

There are the following three ways of writing data into the memory.

(1) Hold $\overline{CE1}$ and $\overline{CE2}$ low, set the address, and apply a low pulse to R/$\overline{W}$.

(2) Hold R/$\overline{W}$ low and hold $\overline{CE1}$ or $\overline{CE2}$ low, set the address, and apply a low pulse to $\overline{CE2}$ or $\overline{CE1}$.

(3) Set the address, then apply low pulses to $\overline{CE1}$, $\overline{CE2}$, and R/$\overline{W}$.

In each case, data from the DATA I/O terminal is fetched into the SRM2017C$_{10/12}$ at the last transition of a section in which $\overline{CE1}$, $\overline{CE2}$, and R/$\overline{W}$ are low. Because the DATA I/O terminal is in high-impedance state when both $\overline{CE1}$ and $\overline{CE2}$ are high or R/$\overline{W}$ is low, competition of data driver and memory output is avoided.

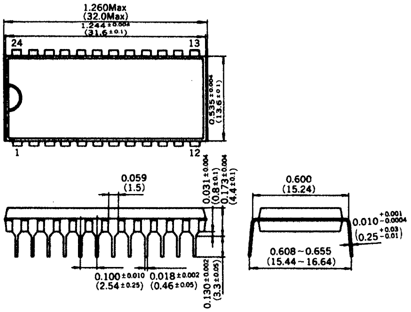
●Standby Mode

When $\overline{CE2}$ is high, SRM2017C$_{10/12}$ is in the stand-by mode and only retains the data. At this time the DATA I/O terminal is in high-impedance state and input of an address, R/$\overline{W}$ signal, or data is prohibited. When $\overline{CE2}$ is above V$_{DD}$−0.2V, current flowing within the SRM2017C$_{10/12}$ chip is only that in the high-resistance portion of the memory cells and leakage current.

■PACKAGE DIMENSIONS

C24

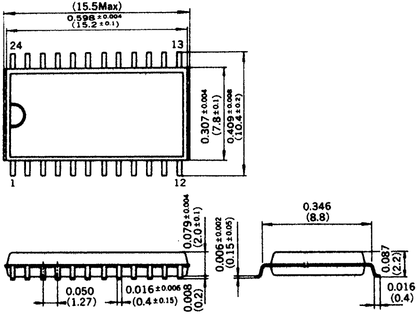
24-pin DIP



unit : inch
(mm)

M24 *1

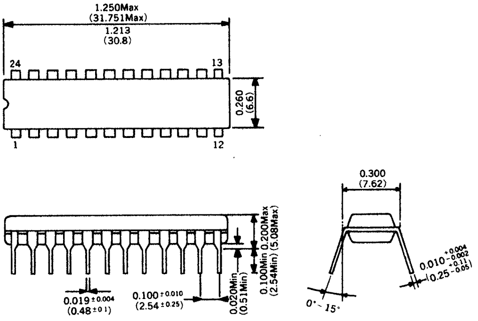
24-pin SOP



unit : inch
(mm)

N24 *2

24-pin Skinny DIP



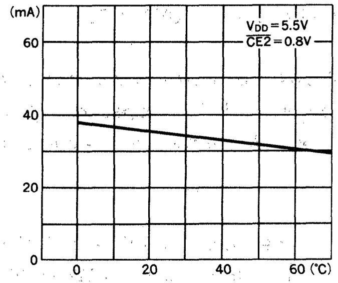
unit : inch
(mm)

*1 Represents model SRM2017M$_{10/12}$ that has the same electrical characteristics as model SRM2017C$_{10/12}$.

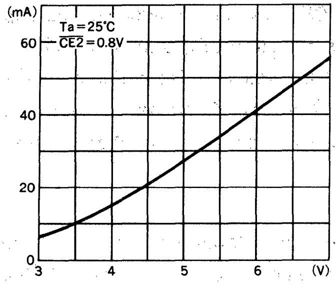
*2 Represents model SRM2017N$_{10/12}$ that has the same electrical characteristics as model SRM2017C$_{10/12}$.

■CHARACTERISTICS CURVES

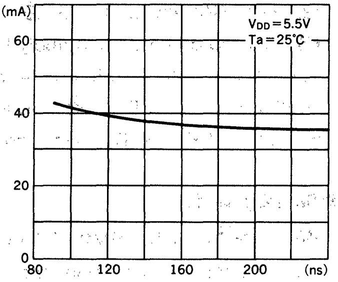
I_{DDO}—Ta



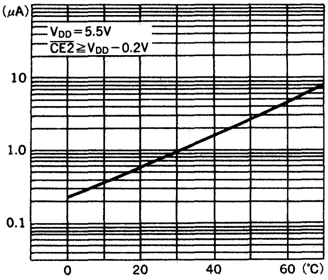
I_{DDO}—V_{DD}



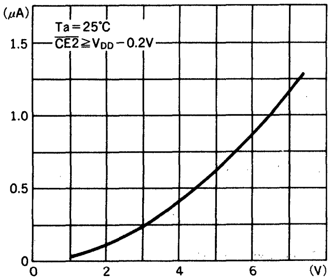
I_{DDA}—t_{cyc}



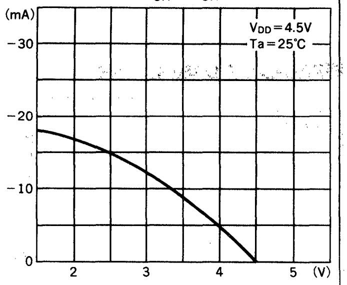
I_{DDS1}—Ta



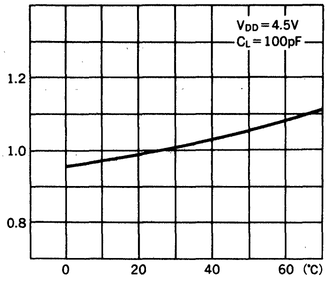
I_{DDS1}—V_{DD}



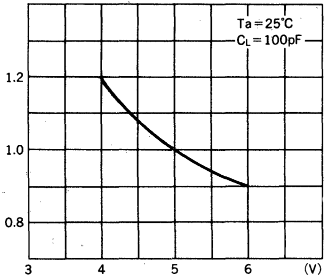
I_{OH}—V_{OH}



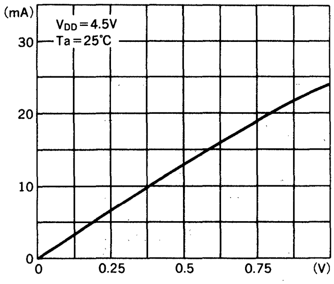
Normalized t_{ACC}·t_{ACE1}·t_{ACE2}—Ta



Normalized t_{ACC}·t_{ACE1}·t_{ACE2}—V_{DD}



I_{OL}—V_{OL}



SRM2018C$_{10/12}$

CMOS 16K-BIT STATIC RAM

- ●Low Supply Current
- ●Access Time 100ns/120ns
- ●2,048 Words × 8 Bits Asynchronous

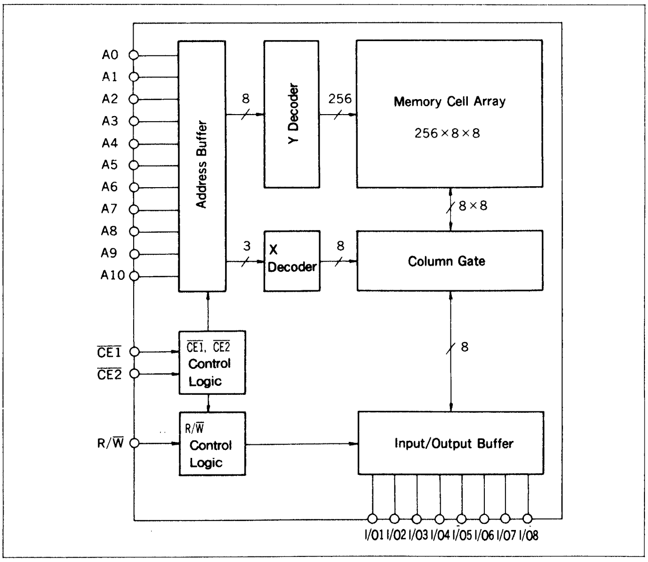
■DESCRIPTION

The SRM2018C$_{10/12}$ is a 2,048 words × 8 bits asynchronous, static, random access memory on a monolithic CMOS chip. Its very low standby power requirement makes it ideal for applications requiring non-volatile storage with back-up batteries. The asynchronous and static nature of the memory requires no external clock or refreshing circuit. Both the input and output ports are TTL compatible and the 3-state output allows easy expansion of memory capacity.

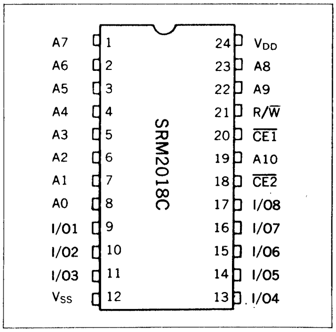
■FEATURES

●Access time ··········SRM2018C$_{10}$ 100ns (Max)
SRM2018C$_{12}$ 120ns (Max)
●Low supply current ··········standby : 1μA (Typ)
operation : SRM2018C$_{10}$ 30mA (Typ)
●Complete static operation SRM2018C$_{12}$ 25mA (Typ)
●Single power supply ··········5V±10%
●TTL compatible inputs and outputs
●3-state output with wired-OR capability
●Non-volatile storage with back-up batteries
●Package··········SRM2018C$_{10/12}$ 24-pin DIP (plastic)
SRM2018M$_{10/12}$ 24-pin SOP (plastic)
SRM2018N$_{10/12}$ 24-pin Skinny DIP (plastic)

■BLOCK DIAGRAM



■PIN CONFIGURATION



■PIN DESCRIPTION

A0 to A10	Address Input
R/$\overline{W}$	Read/Write
$\overline{CE1}$	Chip Enable 1
$\overline{CE2}$	Chip Enable 2
I/O1 to 8	Data Input/Output
V_{DD}	Power Supply (+5V)
V_{SS}	Power Supply (0V)

■ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.5 to 7.0	V
Input voltage*	V_I	−0.5 to 7.0	V
Input/output voltage*	$V_{I/O}$	−0.5 to V_{DD}+0.3	V
Power dissipation	P_D	1.0	W
Operating temperature	T_{opr}	0 to 70	℃
Storage temperature	T_{stg}	−65 to 150	℃
Soldering temp. & time	T_{sol}	260°C, 10s (at lead)	—

*V_I, $V_{I/O}$= −1.0V when pulse width is 50ns

■RECOMMENDED OPERATING CONDITIONS

(Ta=0 to 70℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
	V_{SS}		0	0	0	V
Input voltage	V_{IH}		2.2	3.5	V_{DD}+0.3	V
	V_{IL}		−0.3*	—	0.8	V

*V_{IL}(Min)= −1.0V when pulse width is 50ns

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

(V_{DD}=5V±10%, V_{SS}=0V, Ta=0 to 70℃)

Parameter	Symbol	Conditions	SRM2018C10			SRM2018C12			Unit
			Min	Typ*1	Max	Min	Typ*1	Max	
Input leakage current	I_{LI}	V_{DD}=5.5V, V_I=0 to V_{DD}	−1	—	1	−1	—	1	μA
Output leakage current	I_{LO}	$\overline{CE1}$ or $\overline{CE2}$=V_{IH}, $V_{I/O}$=0 to V_{DD}	−1	—	1	−1	—	1	μA
Operating supply current	I_{DDO}	$\overline{CE1}$ and $\overline{CE2}$=V_{IL}, $I_{I/O}$=0mA	—	30	60	—	25	50	mA
	I_{DDO1}	V_{IH}=3.5V, V_{IL}=0.6V, $I_{I/O}$=0mA	—	16	—	—	16	—	mA
Average operating current	I_{DDA}	Min. cycle, duty=100%, $I_{I/O}$=0mA	—	30	60	—	25	50	mA
Standby supply current	I_{DDS}	$\overline{CE1}$ or $\overline{CE2}$=V_{IH}	—	1.5	3.0	—	1.5	3.0	mA
	I_{DDS1}	$\overline{CE1}$ or $\overline{CE2}$=V_{DD}−0.2V *2	—	1	50	—	1	50	μA
Output voltage	V_{OL}	I_{OL}=4.0mA	—	—	0.4	—	—	0.4	V
	V_{OH}	I_{OH}= −1.0mA	2.4	—	—	2.4	—	—	V

*1 Typical values are for reference, with V_{DD}=5V and Ta=25℃ assumed.
*2 $\overline{CE1}$=V_{DD}−0.2V and $\overline{CE2}$=0.2V or V_{DD}−0.2V, $\overline{CE2}$=V_{DD}−0.2V and $\overline{CE1}$=0.2V or V_{DD}−0.2V

●Terminal Capacitance

(f=1MHz, Ta=25℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C_I	V_I=0V	—	4	6	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	6	8	pF

●AC Electrical Characteristics

○**Read Cycle**

(V_{DD}=5V±10%, V_{SS}=0V, Ta=0 to 70℃)

Parameter	Symbol	Conditions	SRM2018C10		SRM2018C12		Unit
			Min	Max	Min	Max	
Read cycle time	t_{RC}	*1	100	—	120	—	ns
Address access time	t_{ACC}		—	100	—	120	ns
$\overline{CE1}$ access time	t_{ACE1}		—	100	—	120	ns
$\overline{CE2}$ access time	t_{ACE2}		—	100	—	120	ns
$\overline{CE1}$ output setup time	t_{CLZ1}	*2	10	—	10	—	ns
$\overline{CE1}$ output floating	t_{CHZ1}		0	40	0	40	ns
$\overline{CE2}$ output setup time	t_{CLZ2}		10	—	10	—	ns
$\overline{CE2}$ output floating	t_{CHZ2}		0	40	0	40	ns
Output hold time	t_{OH}	*1	10	—	10	—	ns

○ **Write Cycle**

(V_{DD}=5V±10%, V_{SS}=0V, Ta=0 to 70°C)

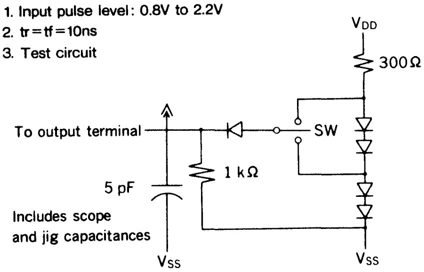
Parameter	Symbol	Conditions	SRM2018C10		SRM2018C12		Unit
			Min	Max	Min	Max	
Write cycle time	t_{WC}	*1	100	—	120	—	ns
Chip select time ($\overline{CE1}$)	t_{CW1}		80	—	85	—	ns
Chip select time ($\overline{CE2}$)	t_{CW2}		80	—	85	—	ns
Address enable time	t_{AW}		80	—	85	—	ns
Address setup time	t_{AS}		0	—	0	—	ns
Write pulse width	t_{WP}		65	—	70	—	ns
Input data setup time	t_{DW}		45	—	50	—	ns
Address hold time	t_{WR}		5	—	5	—	ns
Input data hold time	t_{DH}		0	—	0	—	ns
R/$\overline{W}$ output setup time	t_{OW}	*3	5	—	10	—	ns
R/$\overline{W}$ output floating	t_{WHZ}		0	45	0	50	ns

*1 Test conditions.

1. Input pulse level: 0.8V to 2.2V
2. tr=tf=10ns
3. Input/output timing reference level: 1.5V
4. Output load: $I_{TTL}+C_L$=100pF

*3 Test conditions.

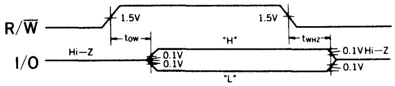
1. Input pulse level: 0.8V to 2.2V
2. tr=tf=10ns
3. Test circuit



○ SW is set to the V_{DD} side when measuring Hi-z-high and high-Hi-z of t_{OW} or t_{WHZ}.

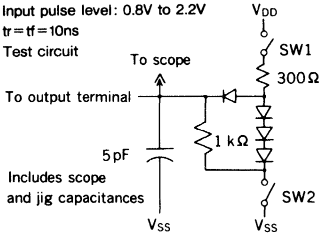
○ SW is set to the Vss side when measuring Hi-z-low and low-Hi-z of t_{OW} or t_{WHZ}.

Output turn-on turn-off times



*2 Test conditions.

1. Input pulse level: 0.8V to 2.2V
2. tr=tf=10ns
3. Test circuit

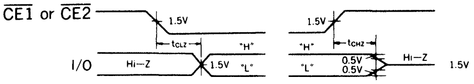


○ Both SW1 and SW2 are closed when measuring t_{CHZ} or t_{OHZ}.

○ SW1 is open and SW2 is closed when measuring Hi-z-high of t_{CLZ} or t_{OLZ}.

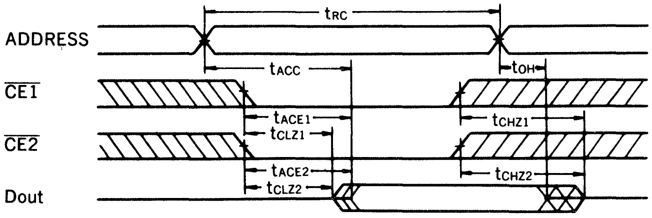
○ SW1 is closed and SW2 is open when measuring Hi-z-low of t_{CLZ} or t_{OLZ}.

Output turn-on turn-off times

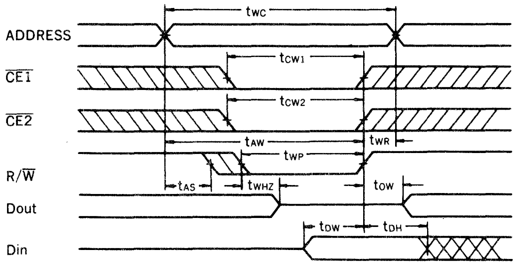


●Timing Chart

○ Read cycle



○Write cycle



■DATA RETENTION CHARACTERISTICS WITH LOW VOLTAGE POWER SUPPLY

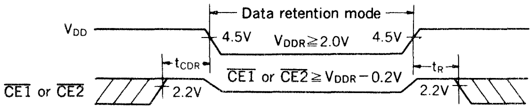
(Ta=0 to 70℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDR}	$\overline{\text{CE1}}$ or $\overline{\text{CE2}} \geqq V_{DDR}-0.2V$	2.0	—	5.5	V
Data retention current	I_{DDR}	V_{DD}=3.0V, $\overline{\text{CE1}}$ or $\overline{\text{CE2}} \geqq 2.8V$ *2	—	—	25	μA
Chip select data hold time	t_{CDR}	Refer to the figure below.	0	—	—	ns
Operation recovery time	t_R		t_{RC}*1	—	—	ns

*1 t_{RC} : read cycle time

*2 $\overline{\text{CE1}} \geqq 2.8V$ and $\overline{\text{CE2}} \geqq 2.8V$ or $\overline{\text{CE2}} \leqq 0.2V$, $\overline{\text{CE2}} \geqq 2.8V$ and $\overline{\text{CE1}} \geqq 2.8V$ or $\overline{\text{CE1}} \leqq 0.2V$

Data retention timing



Note: When retaining data in the stand-by mode, supply voltage can be lowered within a certain range. Read or write cycle cannot be performed while the supply voltage is low.

■FUNCTIONS

●Truth Table

$\overline{\text{CE1}}$	$\overline{\text{CE2}}$	R/W	A0 to A10	DATA I/O	Mode	I_{DD}
H	X	—	—	Hi-Z	Unselected	I_{DDS}, I_{DDS1}
X	H	—	—	Hi-Z	Unselected	I_{DDS}, I_{DDS1}
L	L	H	Stable	Output data	Read	I_{DDO}
L	L	L	Stable	Input data	Write	I_{DDO}

X: "H" or "L", —: "H", "L" or "Hi-Z"

●Reading Data

Data can be read out if an address is set while $\overline{\text{CE1}}$ and $\overline{\text{CE2}}$ are held low and R/$\overline{\text{W}}$ is held high.

●Writing Data

There are the following three ways of writing data into the memory.

(1) Hold $\overline{\text{CE1}}$ and $\overline{\text{CE2}}$ low, set the address, and apply a low pulse to R/$\overline{\text{W}}$.

(2) Hold R/$\overline{\text{W}}$ low and hold $\overline{\text{CE1}}$ or $\overline{\text{CE2}}$ low, set the address, and apply a low pulse to $\overline{\text{CE2}}$ or $\overline{\text{CE1}}$.

(3) Set the address, then apply low pulses to $\overline{\text{CE1}}$, $\overline{\text{CE2}}$, and R/$\overline{\text{W}}$.

In each case, data from the DATA I/O terminal is fetched into the SRM2018C$_{10/12}$ at the last transition of a section in which $\overline{\text{CE1}}$, $\overline{\text{CE2}}$, and R/$\overline{\text{W}}$ are low. Because the DATA I/O terminal is in high-impedance state when both $\overline{\text{CE1}}$ and $\overline{\text{CE2}}$ are high or R/$\overline{\text{W}}$ is low, competition of data driver and memory output is avoided.

●Standby Mode

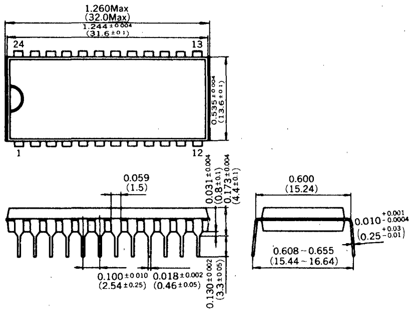
When $\overline{\text{CE1}}$ or $\overline{\text{CE2}}$ is high, SRM2018C$_{10/12}$ is in the stand-by mode and only retains the data. At this time the DATA I/O terminal is in a high-impedance state and input of an address, R/$\overline{\text{W}}$ signal, or data is prohibited. When $\overline{\text{CE1}}$ or $\overline{\text{CE2}}$ is above V$_{DD}$–0.2V,* current flowing within the SRM2018C$_{10/12}$ chip is only that in the high-resistance portion of the memory cells and leakage current.

* $\overline{\text{CE1}}$ = V$_{DD}$ − 0.2V and $\overline{\text{CE2}}$ = 0.2V or V$_{DD}$ − 0.2V
$\overline{\text{CE2}}$ = V$_{DD}$ − 0.2V and $\overline{\text{CE1}}$ = 0.2V or V$_{DD}$ − 0.2V

■PACKAGE DIMENSIONS

C24

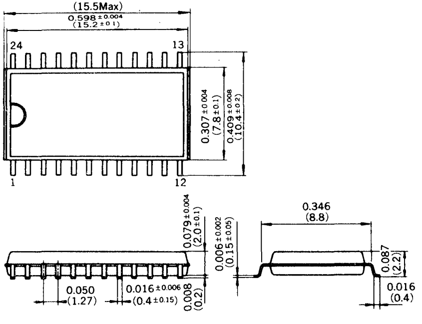
24-pin DIP



unit : inch
(mm)

M24 *1

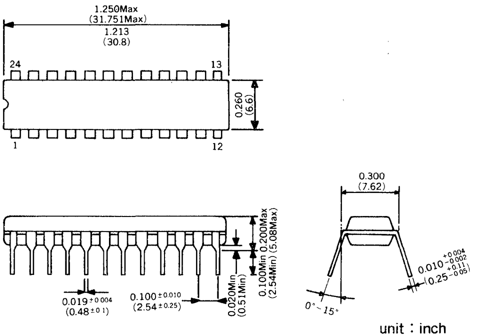
24-pin SOP



unit : inch
(mm)

N24 *2

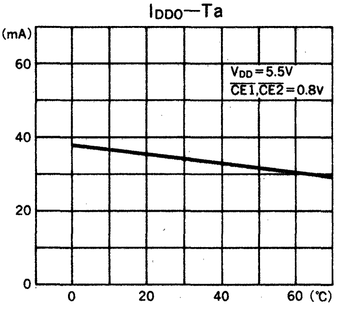
24-pin Skinny DIP



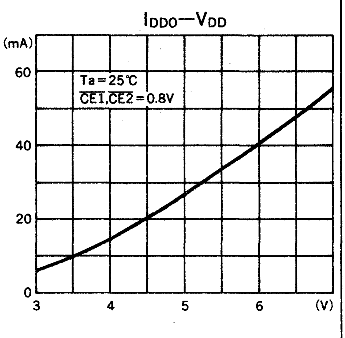
unit : inch
(mm)

*1 Represents model SRM2018M$_{10/12}$ that has the same electrical characteristics as model SRM2018C$_{10/12}$.
*2 Represents model SRM2018N$_{10/12}$ that has the same electrical characteristics as model SRM2018C$_{10/12}$.

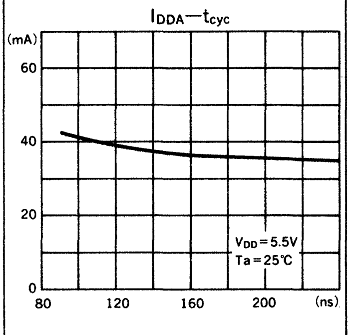
■CHARACTERISTICS CURVES



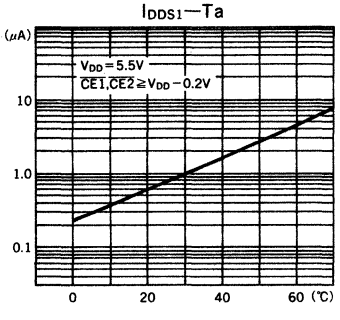
I_{DDO}—Ta



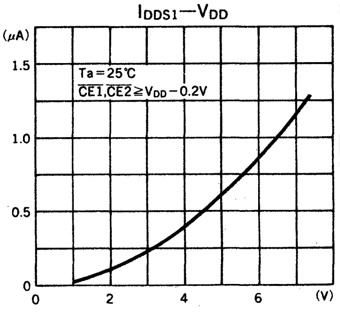
I_{DDO}—V_{DD}



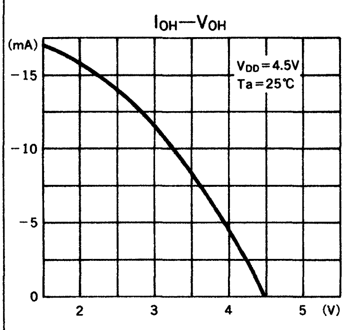
I_{DDA}—t_{cyc}



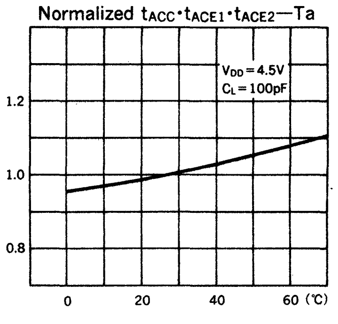
I_{DDS1}—Ta



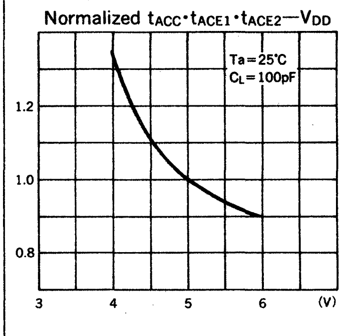
I_{DDS1}—V_{DD}



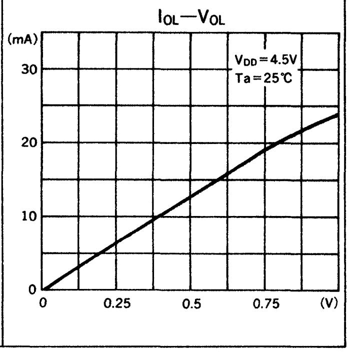
I_{OH}—V_{OH}



Normalized t_{ACC}·t_{ACE1}·t_{ACE2}—Ta



Normalized t_{ACC}·t_{ACE1}·t_{ACE2}—V_{DD}



I_{OL}—V_{OL}

SRM2264LC$_{90/10/12}$

HIGH SPEED CMOS 64K-BIT STATIC RAM

- ●Low Supply Current
- ●Access Time 90ns/100ns/120ns
- ●8,192 Words×8 Bits Asynchronous

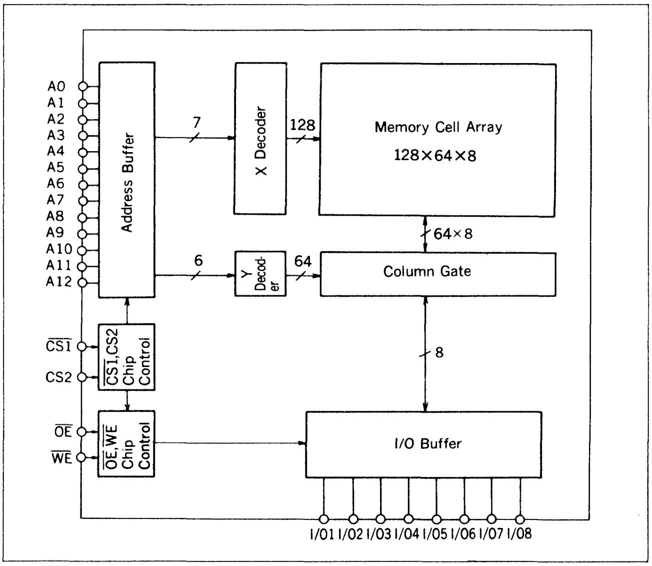
■DESCRIPTION

The SRM2264LC$_{90/10/12}$ is an 8,192 words × 8 bits asynchronous, static, random access memory on a monolithic CMOS chip. Its very low standby power requirement makes it ideal for applications requiring non-volatile storage with back-up batteries. The asynchronous and static nature of the memory requires no external clock or refreshing circuit. Both the input and output ports are TTL compatible and the 3-state output allows easy expansion of memory capacity.

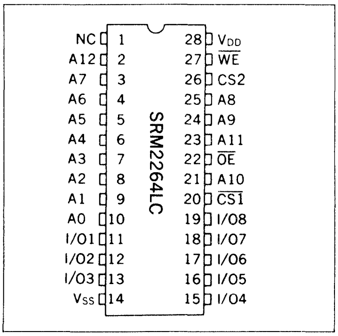
■FEATURES

●Fast Access time··········SRM2264LC$_{90}$ 90ns (Max)
SRM2264LC$_{10}$ 100ns (Max)
SRM2264LC$_{12}$ 120ns (Max)
●Low supply current··········standby : 0.5μA (Typ)
operation: 50mA (Typ)······ 90ns
47mA (Typ)······100ns
45mA (Typ)······120ns
●Completely static··········No clock required
●Single power supply··········5V±10%
●TTL compatible inputs and outputs
●3-state output with wired-OR capability
●Non-volatile storage with back-up batteries
●Package··········SRM2264LC$_{90/10/12}$ 28-pin DIP(plastic)
SRM2264LM$_{90/10/12}$ 28-pin SOP(plastic)

■BLOCK DIAGRAM



■PIN CONFIGURATION



■PIN DESCRIPTION

A0 to A12	Address Input
$\overline{\text{WE}}$	Write Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{CS1}}$, CS2	Chip Select
I/O1 to 8	Data I/O
V_{DD}	Power Supply(+5V)
V_{SS}	Power Supply(0V)
NC	No connection

■ABSOLUTE MAXIMUM RATINGS

($V_{SS}=0V$)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	-0.5 to 7.0	V
Input voltage*	V_I	-0.5 to 7.0	V
Input/Output voltage*	$V_{I/O}$	-0.5 to $V_{DD}+0.3$	V
Power dissipation	P_D	1.0	W
Operating temperature	T_{opr}	0 to 70	℃
Storage temperature	T_{stg}	-65 to 150	℃
Soldering temperature and time	T_{sol}	260℃, 10s (at lead)	—

* V_I, $V_{I/O}$ (Min) $= -1.0V$ (Pulse width is 50ns)

■DC RECOMMENDED OPERATING CONDITIONS

($V_{SS}=0V$, $Ta=0$ to $70℃$)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}	—	4.5	5.0	5.5	V
	V_{SS}	—	0	0	0	V
Input voltage	V_{IH}	—	2.2	3.5	$V_{DD}+0.3$	V
	V_{IL}	—	-0.3*	0	0.8	V

*If pulse width is less than 50ns, it is $-1.0V$

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

($V_{DD}=5V\pm10\%$, $V_{SS}=0V$, $Ta=0$ to $70℃$)

Parameter	Symbol	Conditions	SRM2264LC90			SRM2264LC10			SRM2264LC12			Unit
			Min	Typ*1	Max	Min	Typ*1	Max	Min	Typ*1	Max	
Input leakage	I_{LI}	$V_I=0$ to V_{DD}	-1	—	1	-1	—	1	-1	—	1	μA
Standby supply current	I_{DDS}	$\overline{CS1}=V_{IH}$ or $CS2=V_{IL}$	—	0.5	1.0	—	0.5	1.0	—	0.5	1.0	mA
	I_{DDS1}	$\overline{CS1}=CS2\geqq V_{DD}-0.2V$ or $CS2\leqq0.2V$	—	0.5	20	—	0.5	20	—	0.5	20	μA
Average operating current	I_{DDA}	$V_I=V_{IL}, V_{IH}$ $I_{I/O}=0mA$ $t_{cyc}=Min$	—	50	85	—	47	82	—	45	80	mA
Operating supply current	I_{DDO}	$V_I=V_{IL}, V_{IH}$ $I_{I/O}=0mA$	—	35	60	—	35	60	—	35	60	mA
Output leakage	I_{LO}	$\overline{CS1}=V_{IH}$ or $CS2=V_{IL}$ or $\overline{WE}=V_{IL}$ or $\overline{OE}=V_{IH}$ $V_{I\,O}=0$ to V_{DD}	-1	—	1	-1	—	1	-1	—	1	μA
High level output voltage	V_{OH}	$I_{OH}=-1.0mA$	2.4	$V_{DD}-0.1$	—	2.4	$V_{DD}-0.1$	—	2.4	$V_{DD}-0.1$	—	V
Low level output voltage	V_{OL}	$I_{OL}=4.0mA$	—	0.2	0.4	—	0.2	0.4	—	0.2	0.4	V

*1 Typcal values are measured at $Ta=25℃$ and $V_{DD}=5.0V$

●Terminal Capacitance

($f=1MHz$, $Ta=25℃$)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Address Capacitance	C_{ADD}	$V_{ADD}=0V$	—	3	5	pF
Input Capacitance	C_I	$V_I=0V$	—	5	6	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}=0V$	—	6	7	pF

●AC Electrical Characteristics

○Read Cycle

($V_{DD}=5V\pm10\%$, $V_{SS}=0V$, $Ta=0$ to $70℃$)

Parameter	Symbol	Conditions	SRM2264LC90		SRM2264LC10		SRM2264LC12		Unit
			Min	Max	Min	Max	Min	Max	
Read cycle time	t_{RC}	*1	90	—	100	—	120	—	ns
Address access time	t_{ACC}		—	90	—	100	—	120	ns
Chip select 1 access time	t_{ACS1}		—	90	—	100	—	120	ns
Chip select 2 access time	t_{ACS2}		—	90	—	100	—	120	ns
Output enable access time	t_{OE}		—	50	—	50	—	60	ns
Chip select 1 output set time	t_{CLZ1}	*2	10	—	10	—	10	—	ns
Chip select 1 output floating	t_{CHZ1}		—	35	—	35	—	40	ns
Chip select 2 output set time	t_{CLZ2}		10	—	10	—	10	—	ns
Chip select 2 output floating	t_{CHZ2}		—	35	—	35	—	40	ns
Output enable output set time	t_{OLZ}		5	—	5	—	5	—	ns
Output enable output floating	t_{OHZ}		—	35	—	35	—	40	ns
Output hold time	t_{OH}	*1	10	—	10	—	10	—	ns

○ **Write Cycle**

(V_{DD}=5V±10%, V_{SS}=0V, Ta=0 to 70°C)

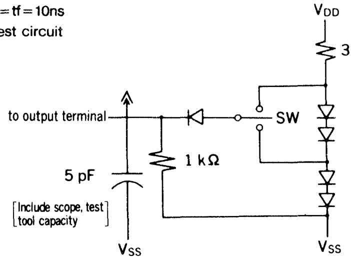
Parameter	Symbol	Conditions	SRM2264LC$_{90}$		SRM2264LC$_{10}$		SRM2264LC$_{12}$		Unit
			Min	Max	Min	Max	Min	Max	
Write cycle time	t_{WC}	*1	90	—	100	—	120	—	ns
Chip select time 1	t_{CW1}		75	—	80	—	85	—	ns
Chip select time 2	t_{CW2}		75	—	80	—	85	—	ns
Address enable time	t_{AW}		75	—	80	—	85	—	ns
Address setup time	t_{AS}		0	—	0	—	0	—	ns
Write pulse width	t_{WP}		60	—	60	—	70	—	ns
Address hold time	t_{WR}		0	—	0	—	0	—	ns
Input data setup time	t_{DW}		50	—	50	—	50	—	ns
Input data hold time	t_{DH}		0	—	0	—	0	—	ns
$\overline{WE}$ Output floating	t_{WHZ}	*3	—	35	—	35	—	40	ns
$\overline{WE}$ Output setup time	t_{OW}		5	—	5	—	5	—	ns

***1 Test Conditions**

1. Input pulse level : 0.8V to 2.4V
2. tr=tf=10ns
3. Input and output timing reference levels : 1.5V
4. Output load $I_{TTL}+C_L$=100pF

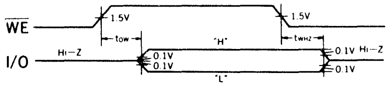
***3 Test Conditions**

1. Input pulse level : 0.8V to 2.4V
2. tr=tf=10ns
3. Test circuit



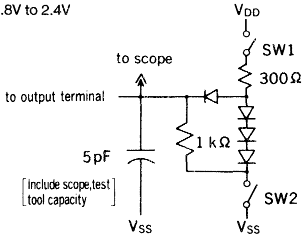
Test : tow,twHz Hi-Z→"H" and "H"→Hi-Z SW is VDD side
Test : tow,twHz Hi-Z→"L" and "L"→Hi-Z SW is Vss side

Output turnon turnoff time



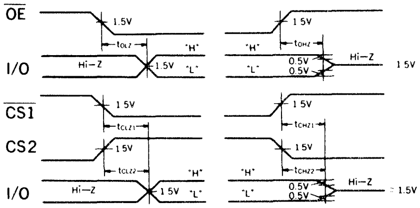
***2 Test Conditions**

1. Input pulse level : 0.8V to 2.4V
2. tr=tf=10ns
3. Test circuit



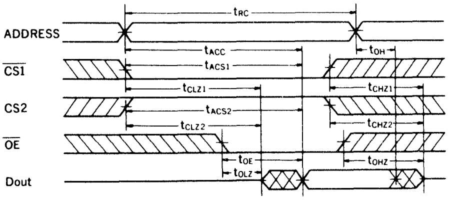
Test : tCHZ1, tCHZ2, tOHZ Both SW1 and SW2 are close
Test : tCLZ1, tCLZ2, tOLZ Hi-Z→"H" SW1 is open, SW2 is close.
Test : tCLZ1, tCLZ2, tOLZ Hi-Z→"L" SW1 is close, SW2 is open.

Output turnon turnoff time

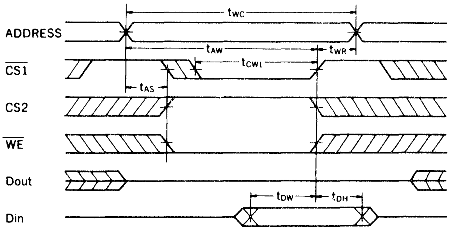


●Timing Chart

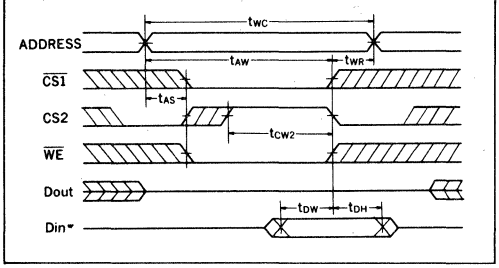
○ **Read Cycle**



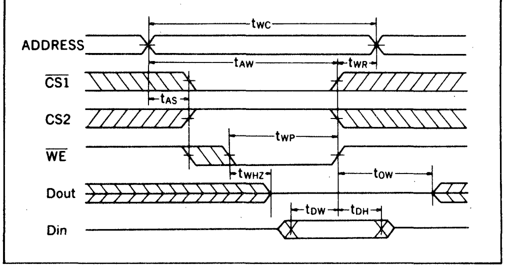
○ **Write Cycle (1) ($\overline{CS1}$ Control)**



○ **Write Cycle (2) (CS2 Control)**



○ **Write Cycle (3) (WE Control)**



Note : 1. During read cycle time, $\overline{WE}$ is to be "H" level.
2. During write cycle time that is controlled by $\overline{CS1}$ or CS2, Output Buffer is in high impedance state whether $\overline{OE}$ level is "H" or "L".
3. During write cycle time that is controlled by $\overline{WE}$, Output Buffer is high impedance state if $\overline{OE}$ is "H" level.

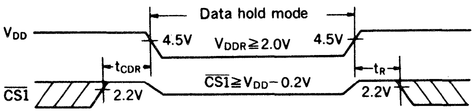
■ DATA RETENTION CHARACTERISTIC WITH LOW VOLTAGE POWER SUPPLY

(Ta = 0 to 70°C)

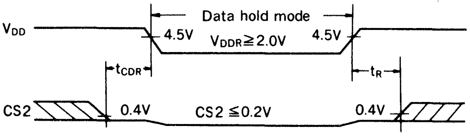
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDR}		2.0	—	5.5	V
Data retention current	I_{DDR}	$V_{DD}=3V$ $\overline{CS1}=CS2 \geq V_{DD}-0.2V$ or $CS2 \leq 0.2V$	—	—	10	μA
Chip select·data hold time	t_{CDR}		0	—	—	ns
Operation recovery time	t_R		t_{RC}*	—	—	ns

*t_{RC} = Read cycle time

Data retention timing ($\overline{CS1}$ Control)



Data retention timing (CS2 Control)



■ FUNCTIONS

●Truth Table

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	A0 to A12	DATA I/O	Mode	I_{DD}
H	X	—	—	—	Hi-Z	Unselected	I_{DDS}, I_{DDS1}
—	L	—	—	—	Hi-Z	Unselected	I_{DDS}, I_{DDS1}
L	H	X	L	Stable	Input data	Write	I_{DDO}
L	H	L	H	Stable	Output data	Read	I_{DDO}
L	H	H	H	Stable	Hi-Z	Output disable	I_{DDO}

X : "H" or "L", — : "H", "L" or "Hi-Z"

●Reading data

Data is able to be read when the address is setted while holding $\overline{CS1}$ = "L", CS2 = "H", $\overline{OE}$ = "L" and $\overline{WE}$ = "H". Since Data I/O terminals are in high impedance state when $\overline{OE}$ = "H", the data bus line can be used for any other objective, then access time apparently is able to be cut down.

●Writing data

There are the following four ways of writing data into the memory.

(1) Hold CS2="H", $\overline{WE}$="L" set addresses and give "L" pulse to $\overline{CS1}$.

(2) Hold $\overline{CS1}$="L", $\overline{WE}$="L", set addresses and give "H" pulse to CS2.

(3) Hold $\overline{CS1}$="L", CS2="H", set addresses and give "L" pulse to $\overline{WE}$.

(4) After setting addresses, give "L" pulse to $\overline{CS1}$, $\overline{WE}$ and give "H" pulse to CS2.

Anyway, data on the Data I/O terminals are latched up into the SRM2264LC$_{90/10/12}$ at the end of the period that $\overline{CS1}$, $\overline{WE}$ are "L" level, and CS2 is "H" level. As Data I/O terminals are in high impedance state when any of $\overline{CS1}$, $\overline{OE}$="H", or CS2="L", the contention on the data bus can be avoided.

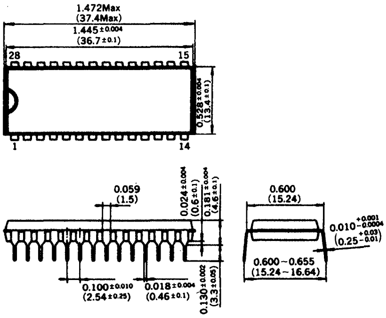
●Standby mode

When $\overline{CS1}$ is "H" or CS2 is "L" level, the SRM2264$_{90/10/12}$ is in the standby mode which has retaning date operation. In this case Data I/O terminals are Hi-Z, and all inputs of addresses, $\overline{WE}$ and data can be any "H" or "L". When $\overline{CS1}$ and CS2 level are in the range over V$_{DD}$-0.2V, or CS2 level is in the range under 0.2V, in the SRM2264LC$_{90/10/12}$ there is almost no current flow except through the high resistance parts of the memory.

■PACKAGE DIMENSIONS

C28

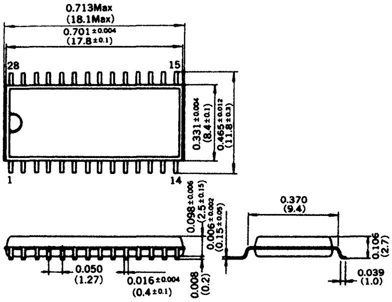
28-pin DIP



unit : inch
(mm)

M28-2 *1

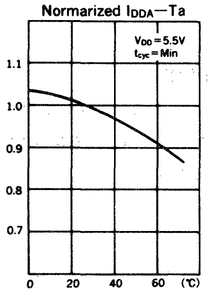
28-pin SOP

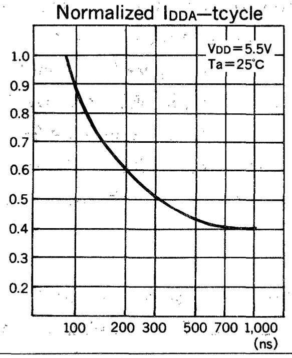


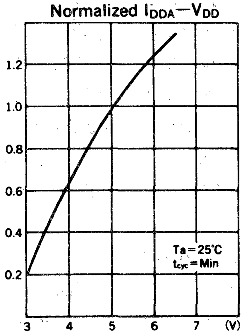
unit : inch
(mm)

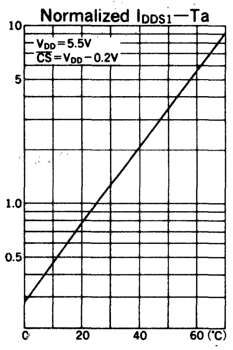
*1 SRM2264LM$_{90/10/12}$ has the same characteristics as SRM2264LC$_{90/10/12}$.

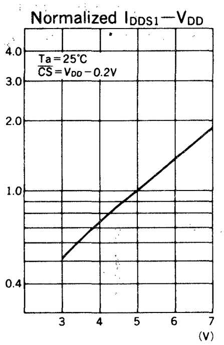
■CHARACTERISTICS CURVES

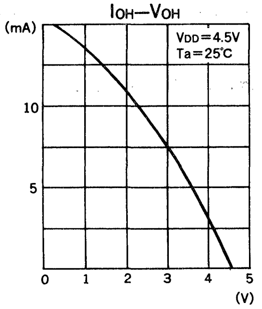

Normarized I_{DDA}—Ta

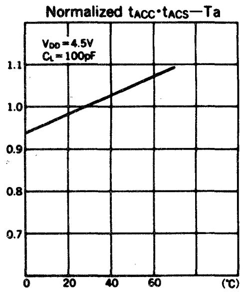

Normalized I_{DDA}—tcycle

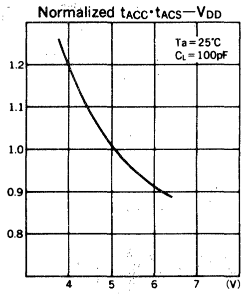

Normalized I_{DDA}—V_{DD}

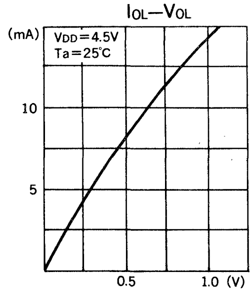

Normalized I_{DDS1}—Ta


Normalized I_{DDS1}—V_{DD}


I_{OH}—V_{OH}


Normalized t_{ACC}·t_{ACS}—Ta


Normalized t_{ACC}·t_{ACS}—V_{DD}


I_{OL}—V_{OL}

SRM20256LC$_{10/12}$

CMOS 256K-BIT STATIC RAM

- ●Low Supply Current
- ●Access Time 100ns/120ns
- ●32,768 Words×8 Bits Asynchronous

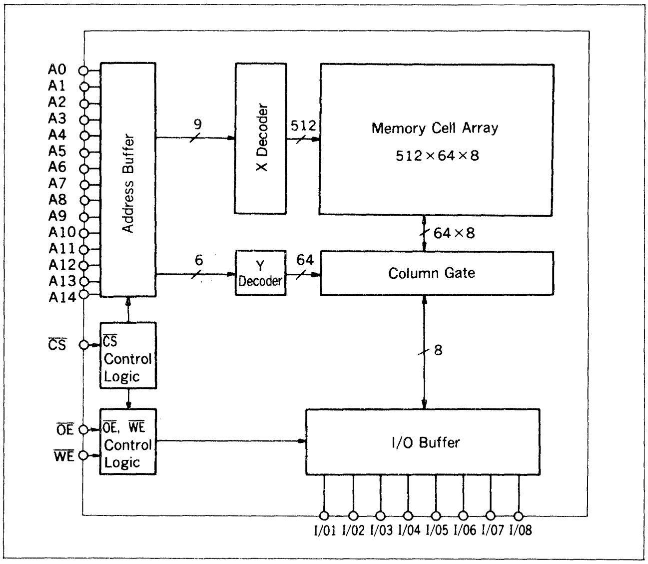
■DESCRIPTION

The SRM20256LC$_{10/12}$ is a 32,768 word×8 bits asynchronous, static, random access memory fabricated using an advanced CMOS technology. Its very low standby power requirement makes it ideal for applications requiring non-volatile storage with back-up batteries. The asynchronous and static nature of the memory requires no external clock or refresh circuit. Input and output ports are TTL compatible and the 3-state output allows easy expansion of memory capacity.

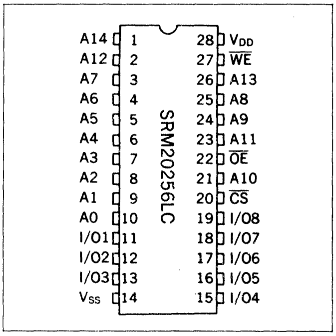
■FEATURES

●Fast access time	SRM20256LC$_{10}$	100ns (Max)
	SRM20256LC$_{12}$	120ns (Max)
●Low supply current	standby : 2μA (Typ)	
	operation : 13mA/1MHz (Typ)	
●Completely static	no clock required	
●Single power supply	5V±10%	
●TTL compatible inputs and outputs		
●3-state output		
●Battery back-up operation		
●Package	SRM20256LC$_{10/12}$	28-pin DIP (plastic)
	SRM20256LM$_{10/12}$	28-pin SOP (plastic)
	SRM20256LS$_{10/12}$	28-pin Shrink DIP (plastic)

■BLOCK DIAGRAM



■PIN CONFIGURATION



■PIN DESCRIPTION

A0 to A14	Address Input
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Select
I/01 to 8	Data Input/Output
V_{DD}	Power Supply (+5V)
V_{SS}	Power Supply (0V)

■ABSOLUTE MAXIMUM RATINGS

($V_{SS}=0V$)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.5 to 7.0	V
Input voltage	V_I	−0.5* to 7.0	V
Input/Output voltage	$V_{I/O}$	−0.5* to V_{DD}+0.3	V
Power dissipation	P_D	1.0	W
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−65 to 150	°C
Soldering temperature and time	T_{sol}	260°C, 10s (Lead only)	—

*V_I, $V_{I/O}$(Min) = −1.0V when pulse width is less or equal to 50ns

■DC RECOMMENDED OPERATING CONDITIONS

($V_{SS}=0V$, Ta=0 to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
	V_{SS}		0	0	0	V
Input voltage	V_{IH}		2.2	3.5	V_{DD}+0.3	V
	V_{IL}		−0.3*	0	0.8	V

*V_{IL}(Min) = −1.0V when pulse width is less or equal to 50ns

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

($V_{DD}=5V\pm10\%$, $V_{SS}=0V$, Ta=0 to 70°C)

Parameter	Symbol	Conditions	SRM20256LC$_{10}$			SRM20256LC$_{12}$			Unit
			Min	Typ*	Max	Min	Typ*	Max	
Input leakage	I_{LI}	$V_I=0$ to V_{DD}	−1	—	1	−1	—	1	μA
Standby supply current	I_{DDS}	$\overline{CS}=V_{IH}$	—	1.5	3.0	—	1.5	3.0	mA
	I_{DDS1}	$\overline{CS}\geqq V_{DD}-0.2V$	—	2	100	—	2	100	μA
Average operating current	I_{DDA}	$V_I=V_{IL}$, V_{IH} $I_{I/O}=0mA$ t_{cyc}=Min	—	40	70	—	37	70	mA
	I_{DDA1}	$V_I=V_{IL}$, V_{IH} $I_{I/O}=0mA$ $t_{cyc}=1\mu s$	—	13	—	—	13	—	mA
Operating supply current	I_{DDO}	$V_I=V_{IL}$, V_{IH} $I_{I/O}=0mA$	—	35	65	—	35	65	mA
Output leakage	I_{LO}	$\overline{CS}=V_{IH}$ or $\overline{WE}=V_{IL}$ or $\overline{OE}=V_{IH}$ $V_{I/O}=0$ to V_{DD}	−1	—	1	−1	—	1	μA
High level output voltage	V_{OH}	$I_{OH}=-1.0mA$	2.4	V_{DD}−0.1	—	2.4	V_{DD}−0.1	—	V
Low level output voltage	V_{OL}	$I_{OL}=2.1mA$	—	0.2	0.4	—	0.2	0.4	V

*Typical values are measured at Ta=25°C and V_{DD}=5.0V

●Terminal Capacitance

(f=1MHz, Ta=25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Address Capacitance	C_{ADD}	$V_{ADD}=0V$	—	—	10	pF
Input Capacitance	C_I	$V_I=0V$	—	—	10	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}=0V$	—	—	10	pF

●AC Electrical Characteristics

○Read Cycle

($V_{DD}=5V\pm10\%$, $V_{SS}=0V$, Ta=0 to 70°C)

Parameter	Symbol	Conditions	SRM20256LC$_{10}$		SRM20256LC$_{12}$		Unit
			Min	Max	Min	Max	
Read cycle time	t_{RC}	*1	100	—	120	—	ns
Address access time	t_{ACC}		—	100	—	120	ns
$\overline{CS}$ access time	t_{ACS}		—	100	—	120	ns
$\overline{OE}$ access time	t_{OE}		—	50	—	60	ns
$\overline{CS}$ output set time	t_{CLZ}	*2	10	—	10	—	ns
$\overline{CS}$ output floating	t_{CHZ}		—	35	—	40	ns
$\overline{OE}$ output set time	t_{OLZ}		5	—	5	—	ns
$\overline{OE}$ output floating	t_{OHZ}		—	35	—	40	ns
Output hold time	t_{OH}	*1	10	—	10	—	ns

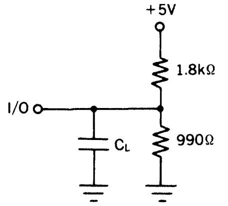
○ Write Cycle

($V_{DD}=5V\pm10\%$, $V_{SS}=0V$, Ta=0 to 70°C)

Parameter	Symbol	Conditions	SRM20256LC$_{10}$		SRM20256LC$_{12}$		Unit
			Min	Max	Min	Max	
Write cycle time	t_{WC}	*1	100	—	120	—	ns
Chip select time	t_{CW}		80	—	85	—	ns
Address valid to end of write	t_{AW}		80	—	85	—	ns
Address setup time	t_{AS}		0	—	0	—	ns
Write pulse width	t_{WP}		75	—	80	—	ns
Address hold time	t_{WR}		0	—	0	—	ns
Input data set time	t_{DW}		45	—	50	—	ns
Input data hold time	t_{DH}		0	—	0	—	ns
Write to Output floating	t_{WHZ}	*2	—	35	—	40	ns
Output Active from end of write	t_{OW}		10	—	10	—	ns

*1 Test Conditions

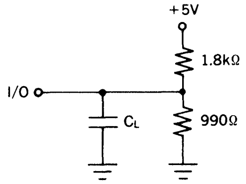
1. Input pulse level: 0.6V to 2.4V
2. tr=tf=5ns
3. Input and output timing reference levels: 1.5V
4. Output load C_L=100pF



C_L=100pF (Includes Jig Capacitance)

*2 Test Conditions

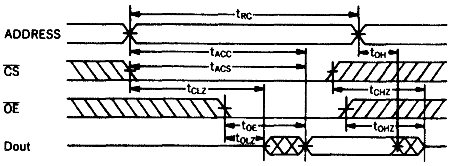
1. Input pulse level: 0.6V to 2.4V
2. tr=tf=5ns
3. Input timing reference levels: 1.5V
4. Output timing reference levels:
   ±200mV (the level displaced from stable output voltage level)
5. Output load C_L=5pF



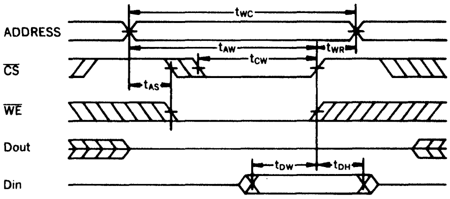
C_L=5pF (Includes Jig Capacitance)

●Timing Chart

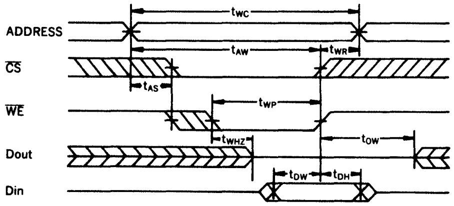
○ Read Cycle



○ Write Cycle (CS Control)



○ Write Cycle (2) (WE Control)



Note :

1. During read cycle time, WE is to be "H" level.
2. During write cycle time that is controlled by CS, Output Buffer is in high impedance state, whether OE level is "H" or "L".
3. During write cycle time that is controlled by WE, Output Buffer is in high impedance state if OE is "H" level.

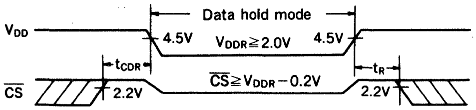
■DATA RETENTION CHARACTERISTIC WITH LOW VOLTAGE POWER SUPPLY

($V_{SS}=0V$, $Ta=0$ to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDR}		2.0	—	5.5	V
Data retention current	I_{DDR}	$V_{DD}=3V$, $\overline{CS}\geqq V_{DDR}-0.2V$	—	1	50	μA
Chip select data hold time	t_{CDR}		0	—	—	ns
Operation recovery time	t_R		t_{RC}*	—	—	ns

*t_{RC}=Read cycle time

Data retention timing



■FUNCTIONS

●Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	A0 to A14	DATA I/O	Mode	I_{DD}
H	—	—	—	Hi—Z	Standby	I_{DDS}, I_{DDS1}
L	X	L	Stable	D_{IN}	Write	I_{DDA}, I_{DDA1}
L	L	H	Stable	D_{OUT}	Read	I_{DDA}, I_{DDA1}
L	H	H	Stable	Hi—Z	Output disable	I_{DDA}, I_{DDA1}

●Read Mode

The Data appear when the address is setted while holding $\overline{CS}$="L", $\overline{OE}$="L" and $\overline{WE}$="H". When $\overline{OE}$="H", Data I/O terminals are in high impedance state, that makes circuit design and bus control easy.

●Write Mode

There are the following 3 ways of writing data into memory.

(1) Hold $\overline{CS}$="L" and $\overline{WE}$="L", set address.

(2) Hold $\overline{CS}$="L" then set address and give "L" pulse to $\overline{WE}$.

(3) After setting addresses, give "L" pulse to both $\overline{CS}$ and $\overline{WE}$.

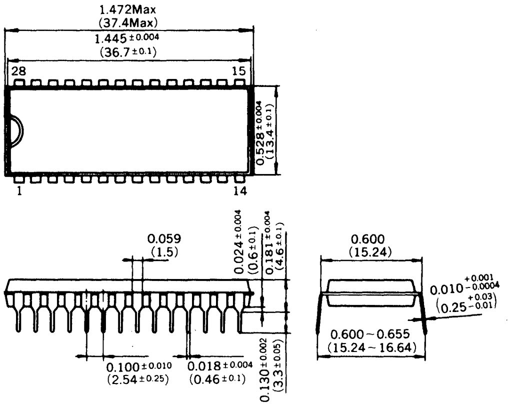
In above any case data on the DATA I/O terminals are latched up into the SRM20256LC10/12 when $\overline{CS}$ or $\overline{WE}$ is in positive-going. Since DATA I/O terminals are high impedance when $\overline{CS}$ or $\overline{OE}$="H", bus contention between data driver and memory outputs can be avoided.

●Standby Mode

When $\overline{CS}$ is "H" the SRM20256LC10/12 become in the stand-by mode. In this mode, data I/O terminals are Hi-Z, and all inputs of addresses, $\overline{WE}$ and data can be any "H" or "L". When $\overline{CS}$ is over than V_{DD}—0.2V, the SRM20256LC10/12 is in the data retention battery back-up mode, in this case, there is a small current in the SRM20256LC10/12 which flow through the high resistances of the memory cells.

■PACKAGE DIMENSIONS

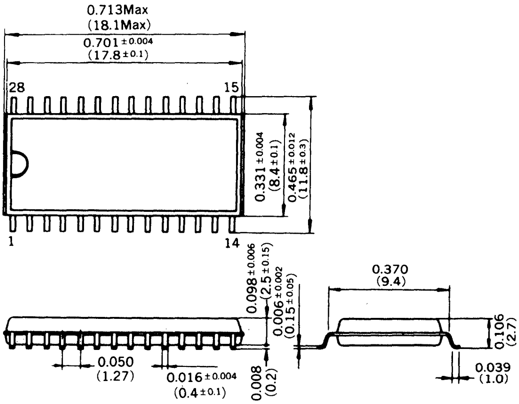
C28



28-pin DIP

unit : inch
(mm)

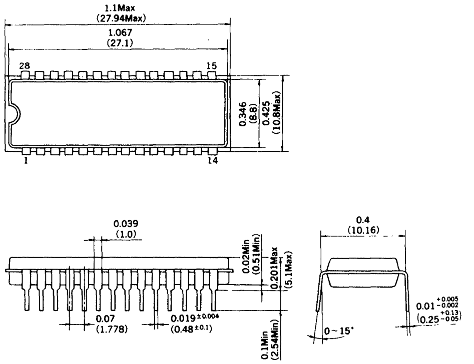
M28-2 *1



28-pin SOP

unit : inch
(mm)

S28 *2



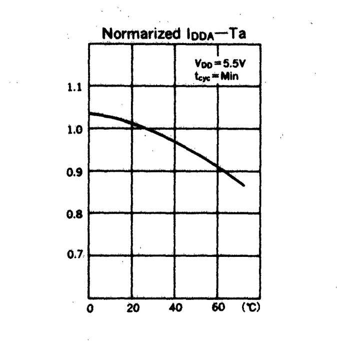
28-pin Shrink DIP

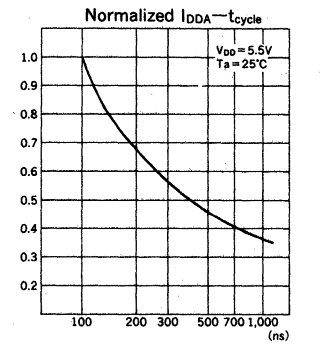
unit : inch
(mm)

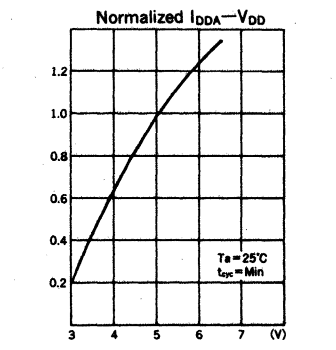
*1 Represents SRM20256LM$_{10/12}$ that has the same electrical characteristics as SRM20256LC$_{10/12}$.

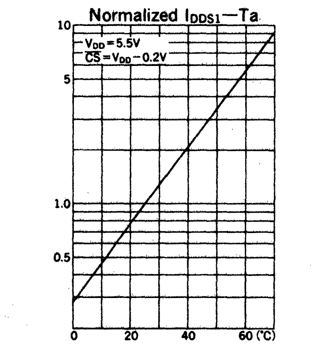
*2 Represents SRM20256LS$_{10/12}$ that has the same electrical characteristics as SRM20256LC$_{10/12}$.

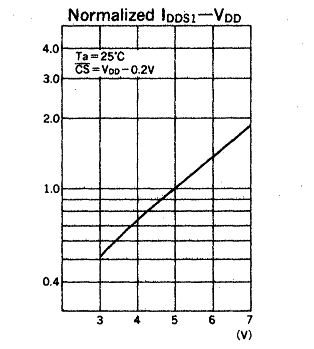
■CHARACTERISTICS CURVES

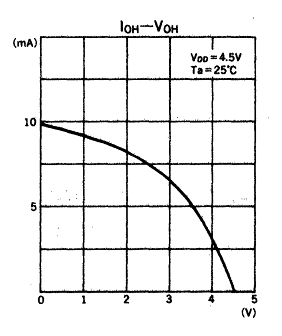


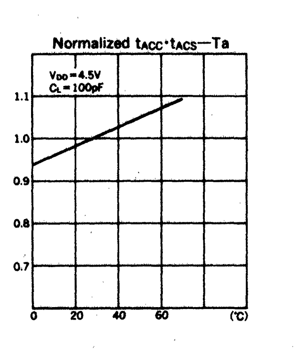


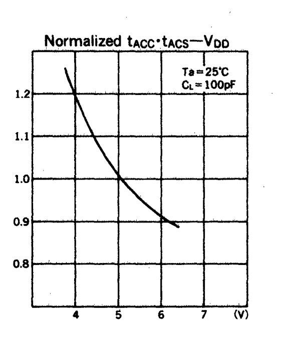


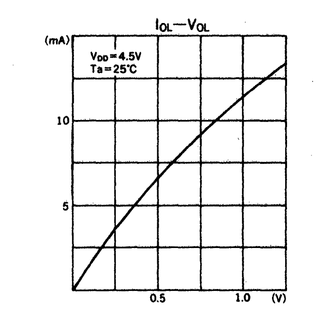












PF281-02

SRM20256LCT$_{10/12}$

CMOS 256K-BIT STATIC RAM

- ●Industrial Temperature Range
- ●Low Supply Current
- ●Access Time 100ns/120ns
- ●32,768 Words×8 Bits Asynchronous

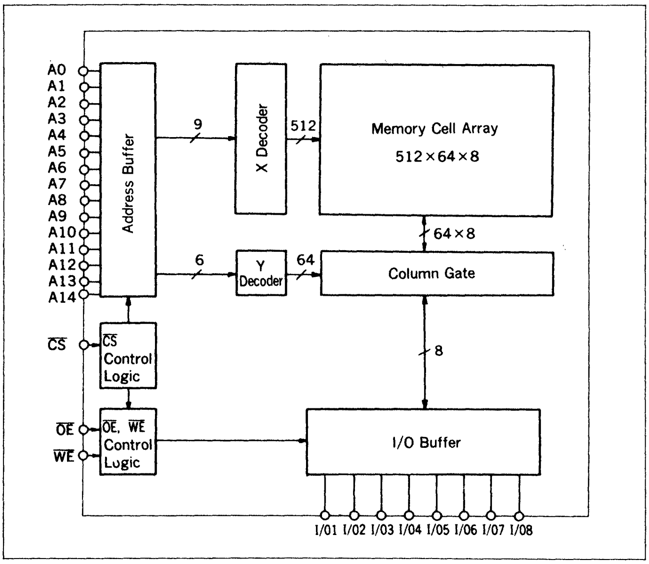
■DESCRIPTION

The SRM20256LCT$_{10/12}$ is a 32,768 word ×8 bits asynchronous, static, random access memory fabricated using advanced CMOS technology. Its very low stand-by power feature makes it ideal for applications requiring non-volatile storage with back-up batteries. And −40 to 85°C operating temperature range makes it ideal for industrial use. The asynchronous and static nature of the memory requires no external clock of refresh circuit. Input and output ports are TTL compatible and the 3-state output allows easy expansion of memory capacity.

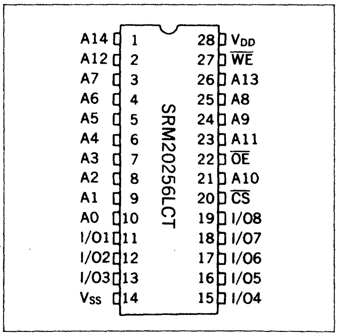
■FEATURES

●Industrial temperature range	−40 to 85°C	
●Fast access time	SRM20256LCT$_{10}$	100ns (Max)
	SRM20256LCT$_{12}$	120ns (Max)
●Low supply current	standby	: 2μA (Typ)
	operation	: 13mA/1MHz (Typ)
●Completely static	no clock required	
●Single power supply	5V±10%	
●TTL compatible inputs and outputs		
●3-state output		
●Battery back-up operation		
●Package	SRM20256LCT$_{10/12}$	28-pin DIP (plastic)
	SRM20256LMT$_{10/12}$	28-pin SOP (plastic)
	SRM20256LST$_{10/12}$	28-pin Shrink DIP (plastic)

■BLOCK DIAGRAM



■PIN CONFIGURATION



■PIN DESCRIPTION

A0 to A14	Address Input
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Select
I/O1 to 8	Data Input/Output
V$_{DD}$	Power Supply (+5V)
V$_{SS}$	Power Supply (0V)

■ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.5 to 7.0	V
Input voltage	V_I	−0.5* to 7.0	V
Input/Output voltage	$V_{I/O}$	−0.5* to V_{DD}+0.3	V
Power dissipation	P_D	1.0	W
Operating temperature	T_{opr}	−40 to 85	℃
Storage temperature	T_{stg}	−65 to 150	℃
Soldering temperature and time	T_{sol}	260℃, 10s (Lead only)	—

*V_I, $V_{I/O}$(Min) = −1.0V when pulse width is less or equal to 50ns

■DC RECOMMENDED OPERATING CONDITIONS

(V_{SS}=0V, Ta=−40 to 85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
	V_{SS}		0	0	0	V
Input voltage	V_{IH}		2.2	3.5	V_{DD}+0.3	V
	V_{IL}		−0.3*	0	0.8	V

*V_{IL}(Min) = −1.0V when pulse width is less or equal to 50ns

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

(V_{DD}=5V±10%, V_{SS}=0V, Ta=−40 to 85℃)

Parameter	Symbol	Conditions	SRM20256LCT$_{10}$			SRM20256LCT$_{12}$			Unit
			Min	Typ*	Max	Min	Typ*	Max	
Input leakage	I_{LI}	V_I=0 to V_{DD}	−1	—	1	−1	—	1	μA
Standby supply current	I_{DDS}	$\overline{CS}$=V_{IH}	—	1.5	3.0	—	1.5	3.0	mA
	I_{DDS1}	$\overline{CS}$≧V_{DD}−0.2V	—	2	200	—	2	200	μA
Average operating current	I_{DDA}	V_I=V_{IL}, V_{IH} $I_{I/O}$=0mA t_{cyc}=Min	—	40	70	—	37	70	mA
	I_{DDA1}	V_I=V_{IL}, V_{IH} $I_{I/O}$=0mA t_{cyc}=1μs	—	13	—	—	13	—	mA
Operating supply current	I_{DDO}	V_I=V_{IL}, V_{IH} $I_{I/O}$=0mA	—	35	65	—	35	65	mA
Output leakage	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{WE}$=V_{IL} or $\overline{OE}$=V_{IH} $V_{I/O}$=0 to V_{DD}	−1	—	1	−1	—	1	μA
High level output voltage	V_{OH}	I_{OH}=−1.0mA	2.4	V_{DD}−0.1	—	2.4	V_{DD}−0.1	—	V
Low level output voltage	V_{OL}	I_{OL}=2.1mA	—	0.2	0.4	—	0.2	0.4	V

*Typical values are measured at Ta=25℃ and V_{DD}=5.0V

●Terminal Capacitance

(f=1MHz, Ta=25℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Address Capacitance	C_{ADD}	V_{ADD}=0V	—	—	10	pF
Input Capacitance	C_I	V_I=0V	—	—	10	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	—	10	pF

●AC Electrical Characteristics

○Read Cycle

(V_{DD}=5V±10%, V_{SS}=0V, Ta=−40 to 85℃)

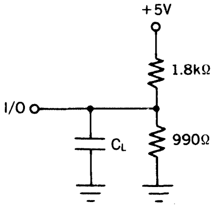
Parameter	Symbol	Conditions	SRM20256LCT$_{10}$		SRM20256LCT$_{12}$		Unit
			Min	Max	Min	Max	
Read cycle time	t_{RC}	*1	100	—	120	—	ns
Address access time	t_{ACC}		—	100	—	120	ns
$\overline{CS}$ access time	t_{ACS}		—	100	—	120	ns
$\overline{OE}$ access time	t_{OE}		—	50	—	60	ns
$\overline{CS}$ output set time	t_{CLZ}	*2	10	—	10	—	ns
$\overline{CS}$ output floating	t_{CHZ}		—	35	—	40	ns
$\overline{OE}$ output set time	t_{OLZ}		5	—	5	—	ns
$\overline{OE}$ output floating	t_{OHZ}		—	35	—	40	ns
Output hold time	t_{OH}	*1	10	—	10	—	ns

○ Write Cycle

(V_{DD}=5V±10%, V_{SS}=0V, Ta=−40 to 85°C)

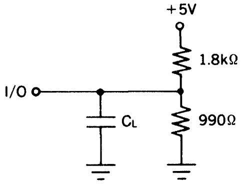
Parameter	Symbol	Conditions	SRM20256LCT$_{10}$		SRM20256LCT$_{12}$		Unit
			Min	Max	Min	Max	
Write cycle time	t_{WC}	*1	100	—	120	—	ns
Chip select time	t_{CW}		80	—	85	—	ns
Address valid to end of write	t_{AW}		80	—	85	—	ns
Address setup time	t_{AS}		0	—	0	—	ns
Write pulse width	t_{WP}		75	—	80	—	ns
Address hold time	t_{WR}		5	—	5	—	ns
Input data set time	t_{DW}		45	—	50	—	ns
Input data hold time	t_{DH}		0	—	0	—	ns
Write to Output floating	t_{WHZ}	*2	—	35	—	40	ns
Output Active from end of write	t_{OW}		5	—	5	—	ns

*1 Test Conditions
1 . Input pulse level : 0.6V to 2.4V
2 . tr=tf=5ns
3 . Input and output timing reference levels : 1.5V
4 . Output load C_L=100pF



C_L=100pF (Includes Jig Capacitance)

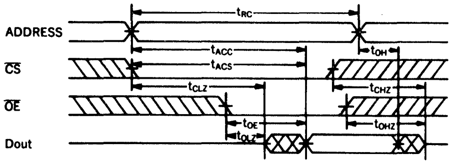
*2 Test Conditions
1 . Input pulse level : 0.6V to 2.4V
2 . tr=tf=5ns
3 . Input timing reference levels : 1.5V
4 . Output timing reference levels :
±200mV (the level displaced from stable output voltage level)
5 . Output load C_L=5pF



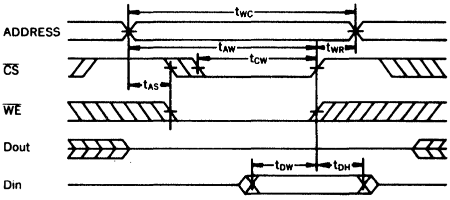
C_L=5pF (Includes Jig Capacitance)

●Timing Chart

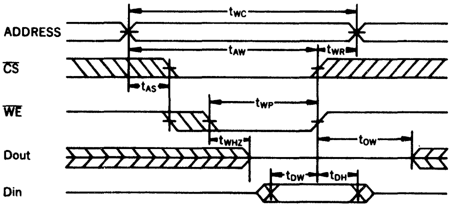
○ Read Cycle



○ Write Cycle ($\overline{CS}$ Control)



○ Write Cycle (2) ($\overline{WE}$ Control)



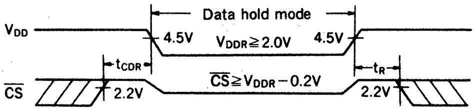
Note :
1. During read cycle time, $\overline{WE}$ is to be "H" level.
2. During write cycle time that is controlled by $\overline{CS}$, Output Buffer is in high impedance state, whether $\overline{OE}$ level is "H" or "L".
3. During write cycle time that is controlled by $\overline{WE}$, Output Buffer is in high impedance state if $\overline{OE}$ is "H" level.

■DATA RETENTION CHARACTERISTIC WITH LOW VOLTAGE POWER SUPPLY (V_{SS}=0V, Ta=−40 to 85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDR}		2.0	—	5.5	V
Data retention current	I_{DDR}	$V_{DD}=3V, \overline{CS} \geqq V_{DDR}-0.2V$	—	1	100	μA
Chip select data hold time	t_{CDR}		0	—	—	ns
Operation recovery time	t_R		t_{RC}*	—	—	ns

*t_{RC}=Read cycle time

Data retention timing



■FUNCTIONS

●Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	A0 to A14	DATA I/O	Mode	I_{DD}
H	—	—	—	Hi—Z	Standby	I_{DDS}, I_{DDS1}
L	X	L	Stable	D_{IN}	Write	I_{DDA}, I_{DDA1}
L	L	H	Stable	D_{OUT}	Read	I_{DDA}, I_{DDA1}
L	H	H	Stable	Hi—Z	Output disable	I_{DDA}, I_{DDA1}

●Read Mode

The Data appear when the addresses is setted while holding $\overline{CS}$ ="L", $\overline{OE}$="L" and $\overline{WE}$="H". When $\overline{OE}$ ="H", Data I/O terminals are in high impedance state, that makes it easy for circuit design and bus control.

●Write Mode

There are following 3ways of writing data into the memory.

(1) Hod $\overline{CS}$="L", $\overline{WE}$="L", set address.
(2) Hold $\overline{CS}$="L", set address and give "L" pulse to $\overline{WE}$.
(3) After setting addresses, "L" pulse to both $\overline{CS}$ and $\overline{WE}$.

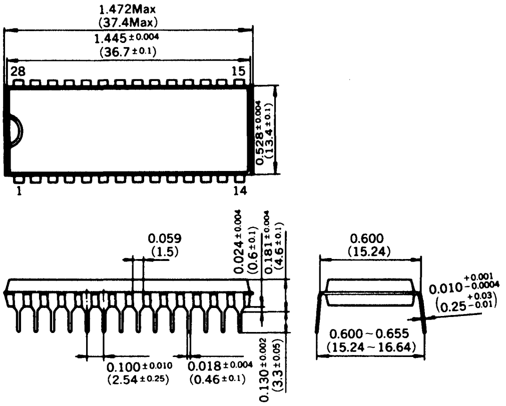
In above any case, Data on the DATA I/O terminals are latched up into the SRM20256LCT10/12 when $\overline{CS}$ or $\overline{WE}$ is in positive-going. Since DATA I/O terminals are in high impedance state when $\overline{CS}$ or $\overline{OE}$="H", the contention on the data bus can be aboided.

●Standby Mode

When $\overline{CS}$ is "H" the SRM20256LCT10/12 is in the standby mode. In this case Data I/O terminals are in Hi-Z, so that all inputs of addressses, $\overline{WE}$ and data can be any "H" or "L". When $\overline{CS}$ is over than $V_{DD}-0.2V$, the SRM20256LCT10/12 is in the data retention battery back-up mode, in this mode, there is a small current in the SRM20256LCT10/12 which flow through the high resistances of the memory cells.

■PACKAGE DIMENSIONS

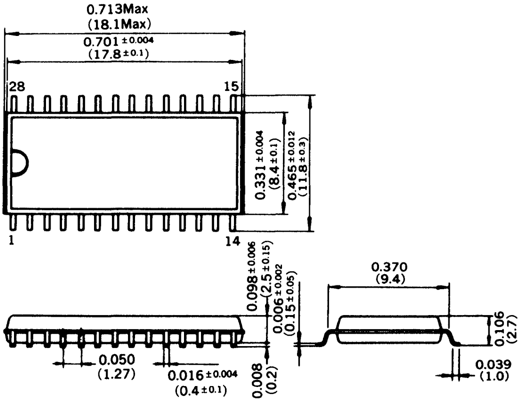
C28



28-pin DIP

unit : inch
(mm)

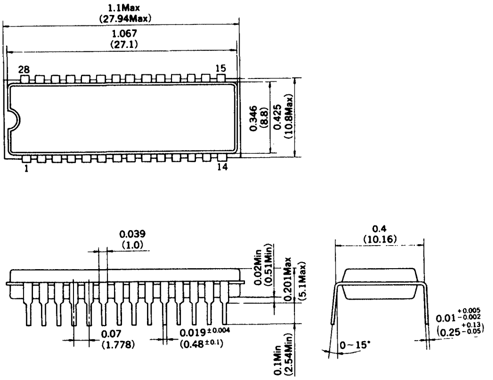
M28-2 *1



28-pin SOP

unit : inch
(mm)

S28 *2



28-pin Shrink DIP

unit : inch
(mm)

*1 Represents SRM20256LMT$_{10/12}$ that has the same electrical characteristics as SRM20256LCT$_{10/12}$.
*2 Represents SRM20256LST$_{10/12}$ that has the same electrical characteristics as SRM20256LCT$_{10/12}$.

■CHARACTERISTICS CURVES

Under measurment

SRM21256N$_{35/45/55}$

CMOS 256K-BIT STATIC RAM

preliminary

- ●**Low Supply Current**
- ●**Access Time 35ns/45ns/55ns**
- ●**65,536 Words × 4 Bits Asynchronous**

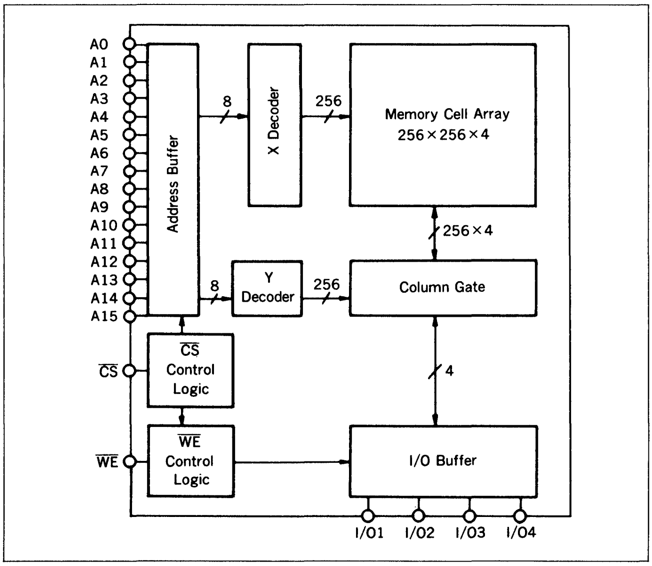
■DESCRIPTION

The SRM21256N$_{35/45/55}$ is a 65,536-word × 4 bits asynchronous, static random access memory fabricated using advanced CMOS technology. Since it is asyncronous and static, the memory does not require an external clock or refresh circuitry. Input and output ports are TTL compatible and the 3-state output allows easy expansion of memory capacity.

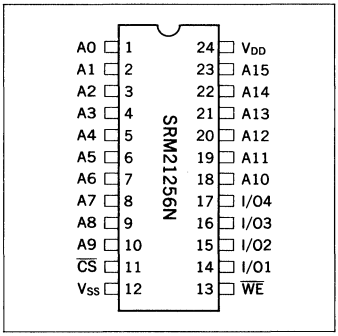
■FEATURES

●Fast access time	SRM21256N$_{35}$ 35ns(Max) SRM21256N$_{45}$ 45ns(Max) SRM21256N$_{55}$ 55ns(Max)
●Low supply current	stand-by : 3mA(Max) operation : 120mA(Max)
●Completely static	no clock required
●Single power supply	5V ± 10%
●TTL compatible inputs and outputs	
●3-state output	
●Package	SRM21256N$_{35/45/55}$ 24-pin Skinny DIP (300 mil plastic package)

■BLOCK DIAGRAM



■PIN CONFIGURATION



■PIN DESCRIPTION

A0 to A15	Address Input
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
I/O1 to 4	Data Input/Output
V$_{DD}$	Power Supply (+5V)
V$_{SS}$	Power Supply (0V)

■ABSOLUTE MAXIMUM RATINGS

($V_{SS}=0V$)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.5 to 7.0	V
Input voltage	V_I	−0.5* to 7.0	V
Input/Output voltage	$V_{I/O}$	−0.5* to $V_{DD}+0.3$	V
Power dissipation	P_D	1.0	W
Operating temperature	T_{opr}	0 to 70	℃
Storage temperature	T_{stg}	−65 to 150	℃
Soldering temperature and time	T_{sol}	260℃, 10s (Lead only)	—

*V_I, $V_{I/O}$(Min) = −3.0V when pulse width is ≦20ns

■DC RECOMMENDED OPERATING CONDITIONS

($V_{SS}=0V$, Ta=0 to 70℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
	V_{SS}		0	0	0	V
Input voltage	V_{IH}		2.2	—	$V_{DD}+0.3$	V
	V_{IL}		−0.3*	—	0.8	V

*V_{IL}(Min) = −3.0V when pulse width is ≦20ns

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

($V_{DD}=5V\pm10\%$, $V_{SS}=0V$, Ta=0 to 70℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input leakage	I_{LI}	$V_I=0$ to V_{DD}	−1	—	1	μA
Standby supply current	I_{DDS}	$\overline{CS}=V_{IH}$	—	—	10	mA
	I_{DDS1}	$\overline{CS}\geqq V_{DD}-0.2V$	—	—	2	mA
Average operating current	I_{DDA}	$V_I=V_{IL}$, V_{IH} $I_{I/O}=0mA$ $t_{cyc}=Min$	—	—	120	mA
Output leakage	I_{LO}	$\overline{CS}=V_{IH}$ or $\overline{WE}=V_{IL}$ $V_{I/O}=0$ to V_{DD}	−1	—	1	μA
High level output voltage	V_{OH}	$I_{OH}=-4.0mA$	2.4	—	—	V
Low level output voltage	V_{OL}	$I_{OL}=8.0mA$	—	—	0.4	V

●Terminal Capacitance

(f=1MHz, Ta=25℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Address Capacitance	C_{ADD}		—	—	10	pF
Input Capacitance	C_I		—	—	10	pF
I/O Capacitance	$C_{I/O}$		—	—	10	pF

●AC Electrical Characteristics

○Read Cycle

($V_{DD}=5V\pm10\%$, $V_{SS}=0V$, Ta=0 to 70℃)

Parameter	Symbol	Conditions	SRM21256N35		SRM21256N45		SRM21256N55		Unit
			Min	Max	Min	Max	Min	Max	
Read cycle time	t_{RC}	*1	35	—	45	—	55	—	ns
Address access time	t_{ACC}		—	35	—	45	—	55	ns
$\overline{CS}$ access time	t_{ACS}		—	35	—	45	—	55	ns
$\overline{CS}$ output set time	t_{CLZ}	*2	5	—	5	—	5	—	ns
$\overline{CS}$ output floating	t_{CHZ}		0	15	0	20	0	25	ns
Output hold time	t_{OH}	*1	5	—	5	—	5	—	ns

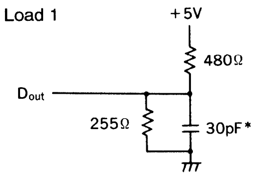
○ Write Cycle

($V_{DD}=5V\pm10\%$, $V_{SS}=0V$, Ta=0 to 70°C)

Parameter	Symbol	Conditions	SRM21256N$_{35}$		SRM21256N$_{45}$		SRM21256N$_{55}$		Unit
			Min	Max	Min	Max	Min	Max	
Write cycle time	t_{WC}	*1	35	—	45	—	55	—	ns
Chip select time	t_{CW}		30	—	40	—	50	—	ns
Address valid to end of write	t_{AW}		30	—	40	—	50	—	ns
Address setup time	t_{AS}		0	—	0	—	0	—	ns
Write pulse width	t_{WP}		25	—	35	—	45	—	ns
Address hold time	t_{WR}		0	—	0	—	0	—	ns
Input data set time	t_{DW}		15	—	20	—	25	—	ns
Input data hold time	t_{DH}		0	—	0	—	0	—	ns
Write to Output floating	t_{WHZ}	*2	0	15	0	20	0	25	ns
Output Active from end of write	t_{OW}		0	—	0	—	10	—	ns

*1 Test Conditions

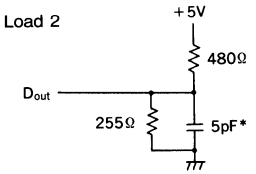
1. Input pulse level: V_{SS} to 3.0V
2. $t_r=t_f=5ns$
3. Input and output timing reference levels: 1.5V
4. Output load $C_L=30pF$



*Including scope and jig.

*2 Test Conditions

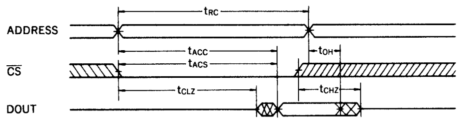
1. Input pulse level: V_{SS} to 3.0V
2. $t_r=t_f=5ns$
3. Input timing reference levels: 1.5V
4. Output timing reference levels: ±200mV (the level displaced from stable output voltage level)
5. Output load $C_L=5pF$



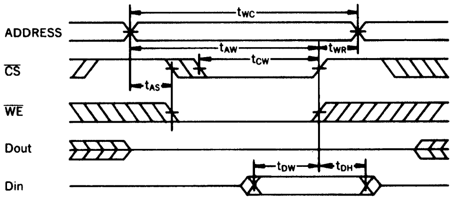
*Including scope and jig.

●Timing Chart

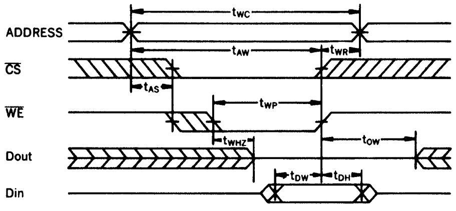
○ Read Cycle



○ Write Cycle (1) ($\overline{CS}$ Control)



○ Write Cycle (2) ($\overline{WE}$ Control)



Note : During read cycle time, $\overline{WE}$ should be "H" level.

FUNCTIONS

Truth Table

$\overline{CS}$	$\overline{WE}$	A0 to A15	DATA I/O	Mode	I_{DD}
H	*	*	Hi-Z	Standby	I_{DDS}, I_{DDS1}
L	L	Stable	D_{IN}	Write	I_{DDA}
L	H	Stable	D_{OUT}	Read	I_{DDA}

* : "H" or "L"

Read Mode

The Data appear when the address is setted while holding $\overline{CS}$="L", and $\overline{WE}$="H".

Write Mode

There are following 3 ways of writing data into memory.

(1) Hold $\overline{WE}$="L", set sddress and give "L" pulse to $\overline{CS}$.
(2) Hold $\overline{CS}$="L", set address and give "L" pulse to $\overline{WE}$.
(3) After setting addresses, give "L" pulse to both $\overline{CS}$ and $\overline{WE}$.

In above any case, data on the DATA I/O terminals are latched up into the SRM21256N when $\overline{CS}$ or $\overline{WE}$ is in positive-going. Since DATA I/O terminals are high impedance when $\overline{CS}$="H", the contention on the data bus can be avoided.

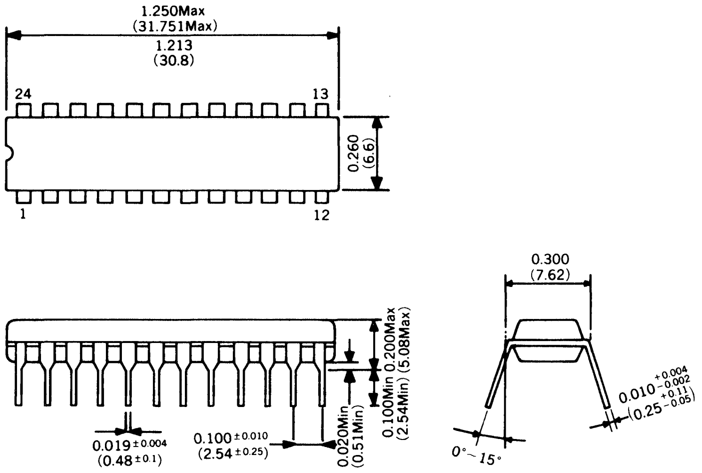
Standby Mode

When $\overline{CS}$ is "H" the SRM21256N is in the stand-by mode. In this case, Data I/O terminals are in Hi-Z, so that all inputs of addresses, $\overline{WE}$ and data can be any "H" or "L".

■PACKAGE DIMENSIONS

N24

24-pin DIP



unit : inch
(mm)

■CHARACTERISTICS CURVES

Under measurment

PF051-05

SMM2364C

CMOS 64K-BIT MASK ROM

- **Low Supply Current**
- **Access Time 350ns/450ns**
- **8,192 Words × 8 Bits Asynchronous**

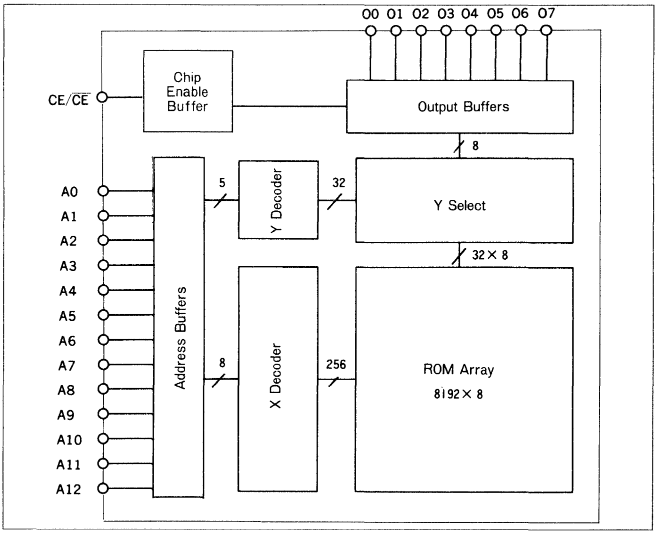
■ DESCRIPTION

The SMM2364C is an 8,192 words × 8 bits asynchronous, static, mask programmable ROM on a monolithic CMOS chip and is characterized by fast access time and very low power dissipation. The nature "static" of the memory eliminates the need of an external clock. Both the input and output are TTL compatible. The 3-state output and mask programmable chip enable provide easy system design and easy expansion of the memory capacity. These features make the SMM2364C usable for wide-ranged applications, especially as a memory for low power dissipation devices using microprocessors.

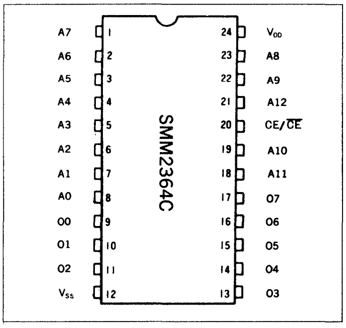
■ FEATURES

- Access time··································350/450ns
- Low supply current·························standby : 0.1μA (Typ)
  operation: 15mA/12mA (Typ)
- Completely static
- Single power supply························5V ±10%
- TTL compatible inputs and outputs
- 3-state output with wired-OR capability
- Package·······································24-pin DIP (plastic)

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



■ PIN DESCRIPTION

A0 to A12	Address Inputs
CE/$\overline{CE}$	Chip Enable
O0 to O7	Data Outputs
V_{DD}	Power Supply (+5V)
V_{SS}	Power Supply (0V)

■ABSOULTE MAXIMUM RATINGS

($V_{SS}=0V$)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.3 to 7.0	V
Input voltage	V_I	−0.3 to $V_{DD}+0.3$	V
Output voltage	V_O	−0.3 to $V_{DD}+0.3$	V
Power dissipation	P_D	1.0	W
DC output current	I_O	10	mA
Operating temperature	T_{opr}	−65 to 150	°C
Storage temperature	T_{stg}	−10 to 70	°C
Soldering temperature and time	T_{sol}	260°C, 10 s (at lead)	—

■ELECTRICAL CHARACTERISTICS

●DC Characteristics

($V_{DD}=+5V\pm10\%$, $V_{SS}=0V$, $Ta=-10$ to $+70°C$)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High level input voltage	V_{IH}		2.2	—	$V_{DD}+0.3$	V
Low level input voltage	V_{IL}		−0.3	—	0.8	V
Input leakage current	I_{LI}	$0\leqq V_I\leqq V_{DD}$	−1.0	—	1.0	μA
Standby supply current	I_{DDS}	$CE=V_{SS}+0.2$ or $\overline{CE}=V_{DD}-0.2$	—	—	40	μA
Operating supply current	I_{DDO}	with output open	—	15*/12	40*/30	mA
Output leakage current	I_{LO}	$0\leqq V_O\leqq V_{DD}$	−1.0	—	1.0	μA
High level output voltage	V_{OH}	$I_{OH}=-1.0mA$	2.4	—	—	V
Low level output voltage	V_{OL}	$I_{OL}=2.0mA$	—	—	0.4	V
Input capacitance	C_I	f=1 MHz	—	—	7	pF
Output capacitance	C_O	f=1 MHz	—	—	10	pF

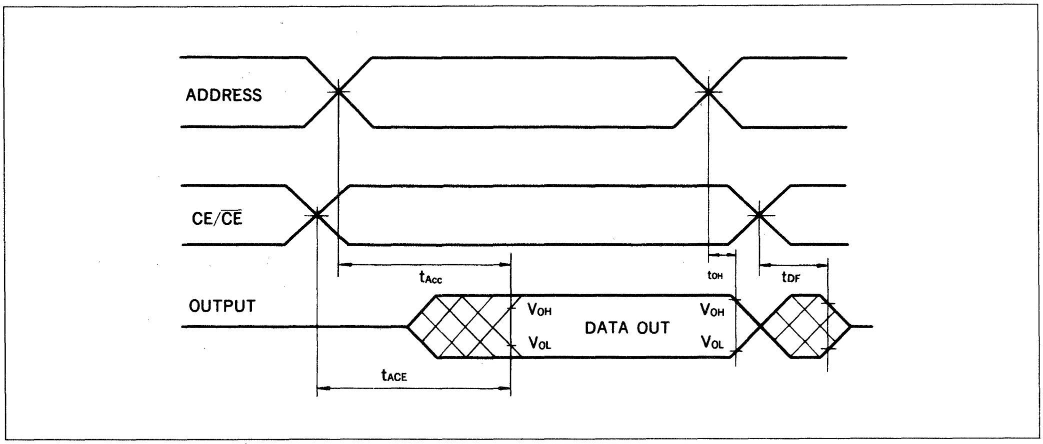
*at access time 350ns

●AC Characteristics

($V_{DD}=+5V\pm10\%$, $V_{SS}=0V$, $Ta=-10$ to $+70°C$)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Address access time	t_{ACC}	$C_L=1TTL+100pF$	—	—	350/450	ns
$\overline{CE}$ access time	t_{ACE}	$V_{IH}=2.2V$, $V_{IL}=0.8V$	—	—	350/450	ns
Output floating	t_{DF}	$V_{OH}=2.2V$, $V_{OL}=0.8V$	—	—	150	ns
Output hold time	t_{OH}	$tr=tf=10ns$	0	—	—	ns

●Timing Chart



■ FUNCTIONS

●Truth Table

CE	$\overline{CE}$	A0 to A12	O0 to O7	MODE
L	H	X	Hi-Z	Standby
H	L	Stable	Output data	Read

(X : H or L)

●Read mode

Data can be read by simply setting an address with CE held at "H" or $\overline{CE}$ at "L".

●Stanby mode

Setting CE at "L" or $\overline{CE}$ at "H" initiates the standby mode. In this mode, the output impedance goes high and all address inputs are disabled. Within the chip, no circuit allows current folw and only the leakage current exists.

●Specifying CE/$\overline{CE}$

CE/$\overline{CE}$ is mask programmable and may be selected for either active level. When ordering, specify the active level of CE/$\overline{CE}$.

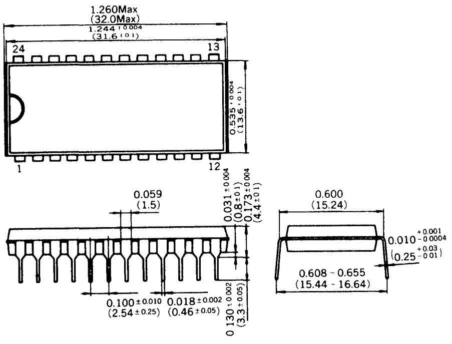
[NOTE] **RECOMMENDATIONS**

1. The SMM2364C is a mask programmable ROM on a CMOS chip. In the data read mode, transient current will frow in the chip at the time of transistor transition. For protection of such transients, it is recommended to connect a high-frequency capacitor and an electrolytic capacitor between the power supplies V_{DD} and V_{SS}.
2. The input and output of the SMM2364C are TTL compatible. It is recommended that, when the chip is connected to TTL, pull-up resistors be connected to the CE/CE and address input terminal.

■ PACKAGE DIMENSIONS

C24

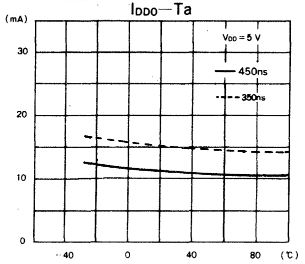
24-pin DIP



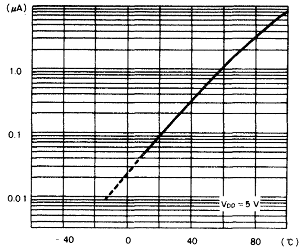
unit : inch
(mm)

CHARACTERISTICS CURVES

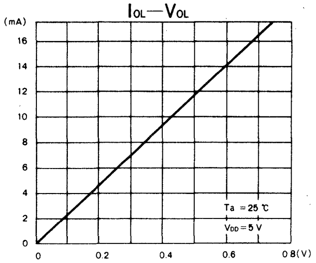
I_{DDO}—Ta



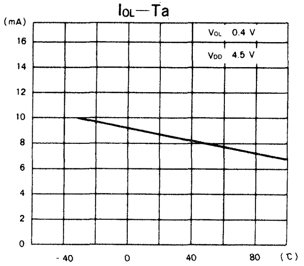
I_{DDS}—Ta



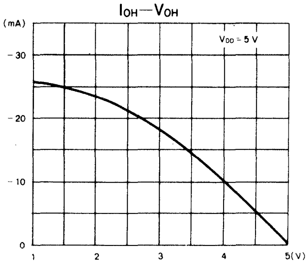
I_{OL}—V_{OL}



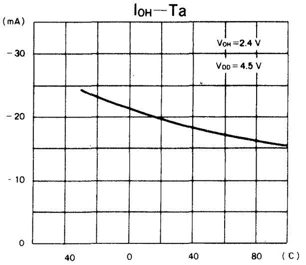
I_{OL}—Ta



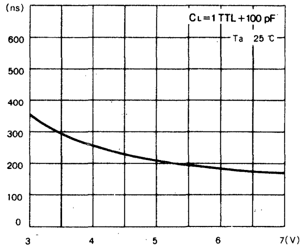
I_{OH}—V_{OH}



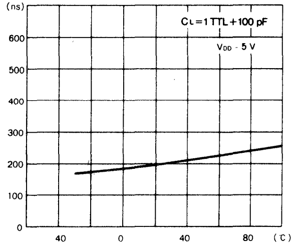
I_{OH}—Ta



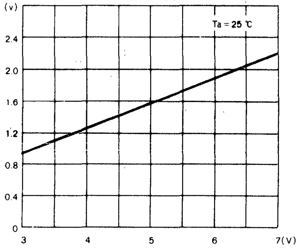
t_{ACC}—V_{DD}



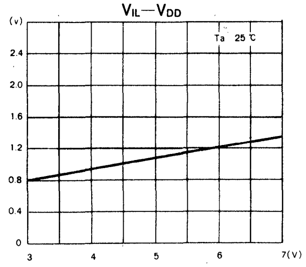
t_{ACC}—Ta



V_{IH}—V_{DD}



V_{IL}—V_{DD}



PF063-04

SMM2365C

CMOS 64K-BIT MASK ROM

●Low Supply Current
●Access Time 350ns/450ns
●8,192 Words × 8 Bits Asynchronous

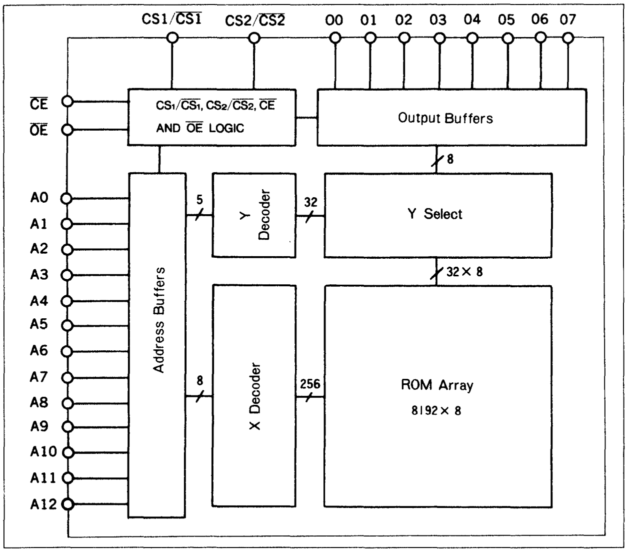
■ DESCRIPTION

The SMM2365C is an 8,192 words × 8 bits asynchronous, static, mask programmable ROM on a monolithic CMOS chip and is characterized by fast access time and very low power dissipation. The nature "static" of the memory eliminates the need of an external clock. Both the input and output are TTL compatible. The 3-state output and mask programmable chip select allow for easy system design and easy expansion of the memory capacity. These features make the SMM2365C usable for a widerange of applications, especially as a memory for low power dissipation devices using microprocessors.

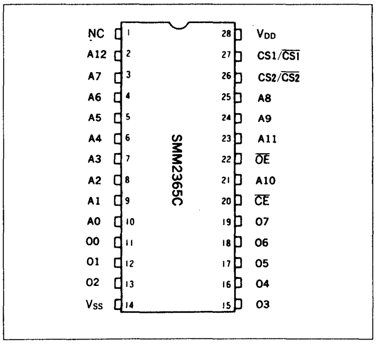
■ FEATURES

- Access time……………………………………350/450ns
- Low supply current……………………………standby: 0.1μA Typ
  operation: 15mA/12mA
- Completely static
- Single power supply …………………………5 V±10%
- TTL compatible inputs and outputs
- 3-state output with wired-OR capability
- Package…………………………………………28-pin DIP (plastic)

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



■ PIN DESCRIPTION

A0 to A12	Address Input
$\overline{\text{OE}}$	Output Enable
$\overline{\text{CE}}$	Chip Enable
CS1/$\overline{\text{CS1}}$,CS2/$\overline{\text{CS2}}$	Chip Select
O0 to O7	Data Output
V_{DD}	Power Supply(+5V)
V_{SS}	Power Supply(0V)
NC	No Connection

■ABSOLUTE MAXIMUM RATINGS

($V_{SS}=0V$)

Parameter	Symbol	Ratings	Unit
Suppy voltage	V_{DD}	−0.3 to 7.0	V
Input voltage	V_I	−0.3 to $V_{DD}+0.3$	V
Output voltage	V_O	−0.3 to $V_{DD}+0.3$	V
Power dissipation	P_D	1.0	W
DC output current	I_O	10	mA
Operating temperature	T_{opr}	−10 to 70	°C
Storage temperature	T_{stg}	−65 to 150	°C
Soldering temperature and time	T_{sol}	260°C, 10 s (at lead)	—

■ELECTRICAL CHARACTERISTICS

●DC Characteristics

($V_{DD}=+5V\pm10\%$, $V_{SS}=0V$, $Ta=-10$ to $+70°C$)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High level input voltage	V_{IH}		2.2	—	$V_{DD}+0.3$	V
Low level input voltage	V_{IL}		−0.3	—	0.8	V
Input leakage current	I_{LI}	$0\leqq V_I\leqq V_{DD}$	−1.0	—	1.0	μA
Standby supply current	I_{DDS}	$\overline{CE}=V_{DD}-0.2$	—	0.1	40	μA
Operating supply current	I_{DDO}	with output open	—	15*/12	40*/30	mA
Output leakage current	I_{LO}	$0\leqq V_O\leqq V_{DD}$	−1.0	—	1.0	μA
High level output voltage	V_{OH}	$I_{OH}=-1.0mA$	2.4	—	—	V
Low level output voltage	V_{OL}	$I_{OL}=2.0mA$	—	—	0.4	V
Input capacitance	C_I	f=1 MHz	—	—	7	pF
Output capacitance	C_O	f=1 MHz	—	—	10	pF

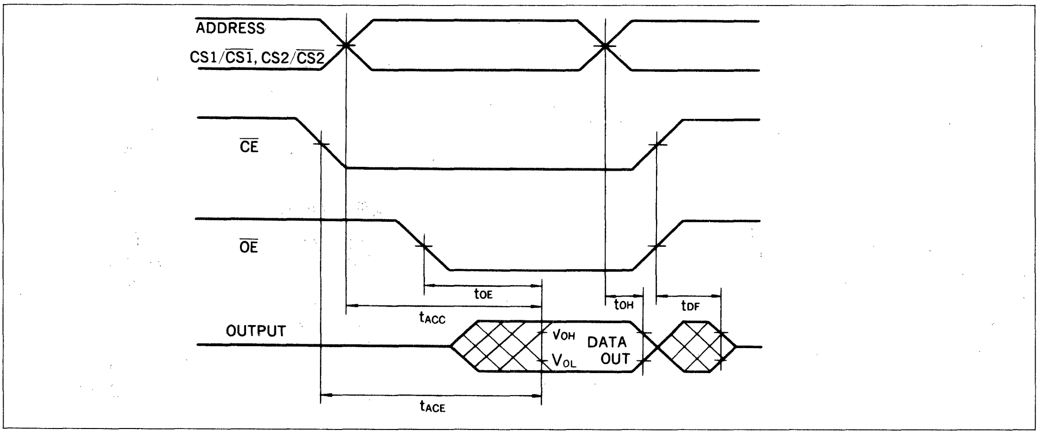
∗at access time 350 ns

●AC Characteristics

($V_{DD}=5V\pm10\%$, $V_{SS}=0V$, $Ta=-10$ to $+70°C$)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Address access time	t_{ACC}	$C_L=1$ TTL+100 pF $V_{IH}=2.2V$, $V_{IL}=0.8V$ $V_{OH}=2.2V$, $V_{OL}=0.8V$ tr=tf=10 ns	—	—	350/450	ns
$\overline{CE}$ access time	t_{ACE}		—	—	350/450	ns
$\overline{OE}$ access time	t_{OE}		—	—	150	ns
Output floating	t_{DF}		—	—	150	ns
Output hold time	t_{OH}		0	—	—	ns

●Timing Chart



■ FUNCTIONS

●Truth Table

$\overline{CE}$	CS1/$\overline{CS1}$, CS2/$\overline{CS2}$, A0 to A12	$\overline{OE}$	O0 to O7	MODE
H	X	X	Hi-Z	Standby
L	Stable	H	Hi-Z	Output disable
L	Stable	L	Output data	Read

X: "H" or "L"

●Read mode

Data can be read by simply setting an address with $\overline{CE}$ held at "L", $\overline{OE}$ at "L", CS1/$\overline{CS1}$, CS2/$\overline{CS2}$ at each active level.

●Standby mode

Setting $\overline{CE}$ at "H" initiates the standby mode. In this mode, the output impedance goes high and all chip select and address inputs are disabled. Within the chip, no circuit allows current flow and only the leakage current exists.

●Output disable

When $\overline{OE}$ is set at "H", the output impedance goes high.

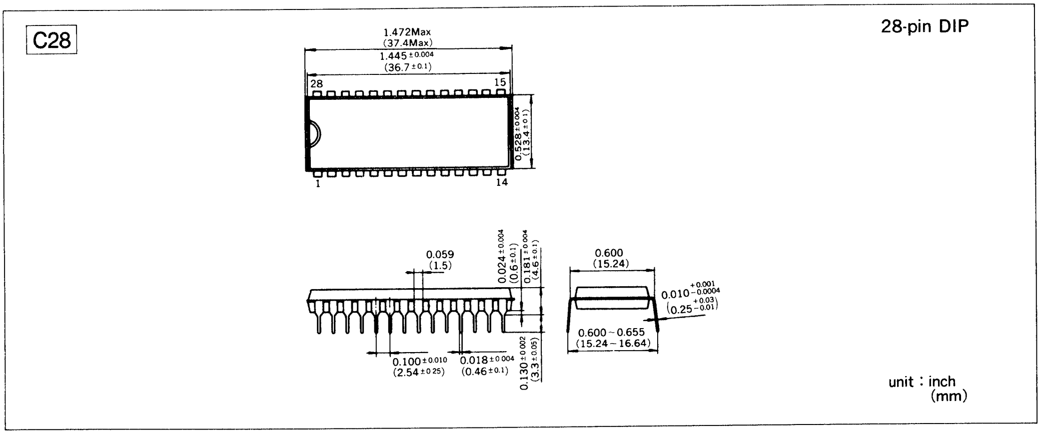
●Specifying CS1/$\overline{CS1}$, CS2/$\overline{CS2}$

CS1/$\overline{CS1}$, CS2/$\overline{CS2}$ is mask programmable and may be selected for either active level. When ordering, specify the active level of CS1/$\overline{CS1}$, CS2/$\overline{CS2}$.

[NOTE] **RECOMMENDATIONS**

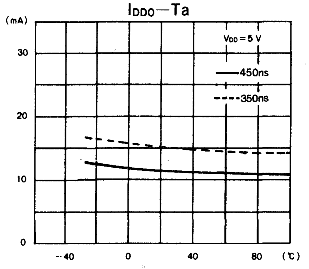
1. The SMM2365C is a mask programmable ROM on a CMOS chip.In the data read mode,transient current will flow in the chip at the time of transistor transition. For protection of such transients, it is recommended to connect a high-frequency capacitor and an electrolytic capacitor between the power supplies V_{DD} and V_{SS}.
2. The input and output of the SMM2365C are TTL compatible. It is recommended that, when the chip is connected to TTL, pull-up resistors be connected to the $\overline{CE}$, $\overline{OE}$, chip select and address input terminal.

■ PACKAGE DIMENSIONS

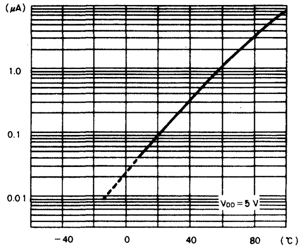


CHARACTERISTICS CURVES

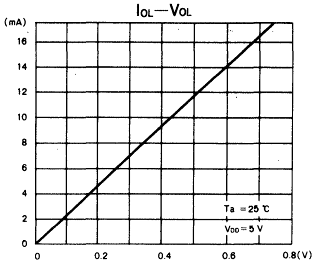
I_{DDO}—Ta



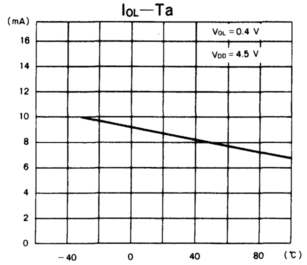
I_{DDS}—Ta



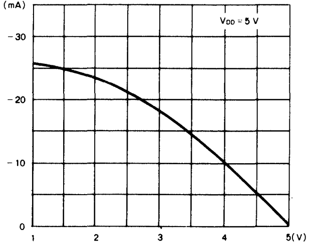
I_{OL}—V_{OL}



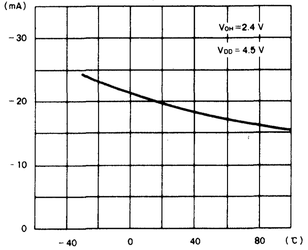
I_{OL}—Ta



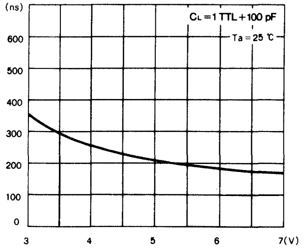
I_{OH}—V_{OH}



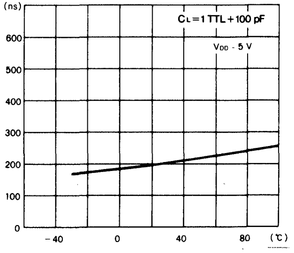
I_{OH}—Ta



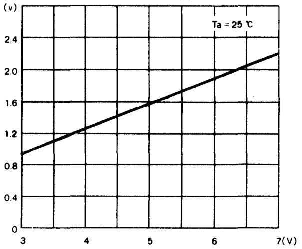
t_{ACC}—V_{DD}



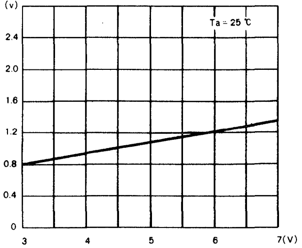
t_{ACC}—Ta



V_{IH}—V_{DD}



V_{IL}—V_{DD}



SMM6365C

CMOS 64K-BIT MASK ROM

- ●Low Power Dissipation
- ●Access Time 250ns
- ●8,192 Words×8 Bits Asynchronous

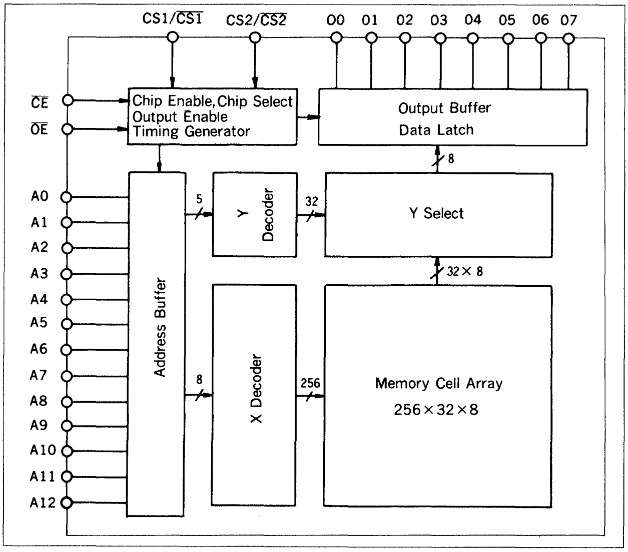
■ DESCRIPTION

The SMM6365C is an 8,192 words × 8 bits asynchronous CMOS mask programmable ROM. This device operates on a single power supply, its input and output levels are TTL compatible and the outputs are 3-state types. The device does not require clock circuit; it has a detection circuit which detects the difference of address, CS1/$\overline{\text{CS1}}$, CS2/$\overline{\text{CS2}}$ and $\overline{\text{CE}}$ input. With the detected signal, the timing signal is generated (internal synchronous type). With such a significant performance, power dissipation is low, processing speed is high and it can be used for various applications.

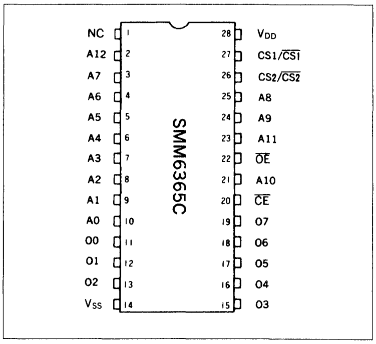
■ FEATURES

- Access time 250ns
- Low supply current .... Standby: 0.1 μA (Typ)
  Operation: 16 mA (Typ)
- Internal synchronous type
- Single power supply .... 5V ± 10%
- TTL compatible inputs and outputs
- 3-state output with wired – OR Capability
- Package.. 28-pin DIP (plastic)

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



■ PIN DESCRIPTION

A0 to A12	Address Input
$\overline{\text{CE}}$	Chip Enable
CS1/$\overline{\text{CS1}}$,CS2/$\overline{\text{CS2}}$	Chip Select
$\overline{\text{OE}}$	Output Enable
O0 to O7	Data Output
V_{DD}	Power Supply (+5V)
V_{SS}	Power Supply (0V)
NC	No connection

■ ABSOLUTE MAXIMUM RATINGS

($V_{SS}=0V$)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	–0.5 to 7.0	V
Input voltage	V_I	–0.5 to $V_{DD}+0.3$	V
Output voltage	V_O	–0.5 to $V_{DD}+0.3$	V
Power dissipation	P_D	1.0	W
DC output current	I_O	10	mA
Operating temperature	T_{opr}	–10 to 70	°C
Storage temperature	T_{stg}	–65 to 150	°C
Soldering temperature and time	T_{sol}	260°C, 10 s (at lead)	—

■ ELECTRICAL CHARACTERISTICS

● DC Characteristics

($V_{DD}=5V \pm 10\%$, $V_{SS}=0V$, $T_a=-10$ to $+70°C$)

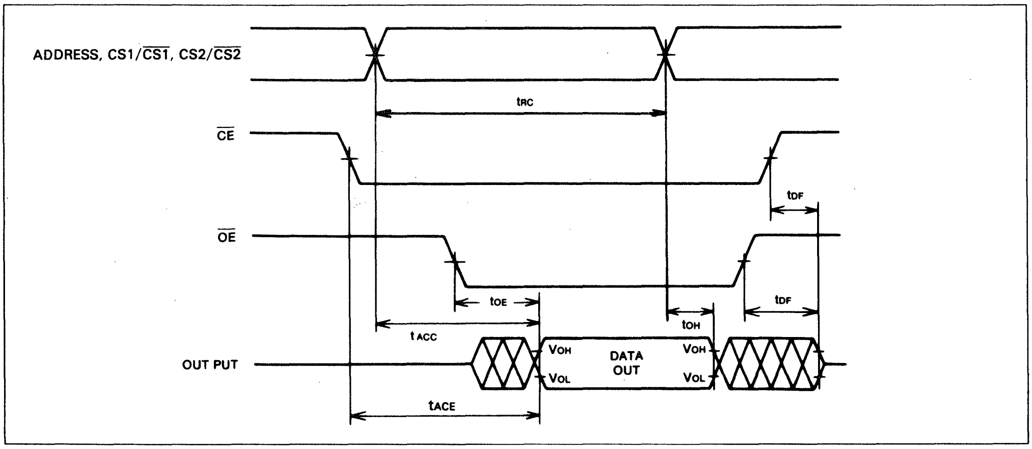
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High level input voltage	V_{IH}		2.2	—	$V_{DD}+0.3$	V
Low level input voltage	V_{IL}		–0.5	—	0.8	V
Input leakage current	I_{LI}	$0 \leqq V_I \leqq V_{DD}$	–2.0	—	2.0	μA
Standby supply current	I_{DDS}	$\overline{CE}=V_{DD}-0.2$	—	0.1	40	μA
Operating supply current	I_{DDO}	with output open	—	16	30	mA
Output leakage current	I_{LO}	$0 \leqq V_O \leqq V_{DD}$	–10.0	—	10.0	μA
High level output voltage	V_{OH}	$I_{OH}=-1.0mA$	2.4	—	—	V
Low level output voltage	V_{OL}	$I_{OL}=3.2mA$	—	—	0.4	V
Input capacitance	C_I	f = 1 MHz	—	—	10	pF
Output capacitance	C_O	f = 1 MHz	—	—	15	pF

● AC Characteristics

($V_{DD}=5V \pm 10\%$, $V_{SS}=0V$, $T_a=-10$ to $+70°C$)

Parameter	Symbol	Conditions	Min	Max	Unit
Read cycle time	t_{RC}	$C_L=1TTL+100pF$	250	—	ns
Address access time	t_{ACC}	$V_{IH}=2.2V$	—	250	ns
$\overline{CE}$ access time	t_{ACE}	$V_{IL}=0.8V$	—	250	ns
$\overline{OE}$ access time	t_{OE}	$V_{OH}=1.5V$	—	80	ns
Output floating	t_{DF}	$V_{OL}=1.5V$	—	80	ns
Output hold time	t_{OH}	$t_r=t_f=10ns$	0	—	ns

● Timing Chart



■ FUNCTIONS

● Truth Table

$\overline{CE}$	CS1/$\overline{CS1}$,CS2/$\overline{CS2}$,A0 to A12	$\overline{OE}$	O0 to O7	MODE
H	X	X	Hi—Z	Standby
L	Stable	H	Hi—Z	Output Disable
L	Stable	L	Data out	Read

X : "H" or "L"

● Read mode

Data can be read by simply setting an address with $\overline{CE}$ held at "L", $\overline{OE}$ held at "L" and CS1/$\overline{CS1}$, CS2/$\overline{CS2}$ held at active level. At the time of power-on, the initial state cannot be determined because of the operation of internal clock circuit. If the power is on in the mode of holding $\overline{CE}$ = "L" and a certain address is fixed, the data related to the address may not appear. Data should be read after the supply voltage becomes stable, and $\overline{CE}$ is set at "H" or the address input is changed in the mode of $\overline{CE}$ = "L".

● Standby mode

Setting $\overline{CE}$ at "H" initiates the standby mode. In this mode, the output impedance goes high and all address input is disabled. Within the chip, no circuit allows current flow and only the leakage current exists.

● Out put disable

When $\overline{OE}$ is set at "H", the output impedance goes high.

● Specifying CS1/$\overline{CS1}$, CS2/$\overline{CS2}$

CS1/$\overline{CS1}$, CS2/$\overline{CS2}$ is mask programmable and may be selected for either active level. When ordering, specify the active level of CS1/$\overline{CS1}$, CS2/$\overline{CS2}$.

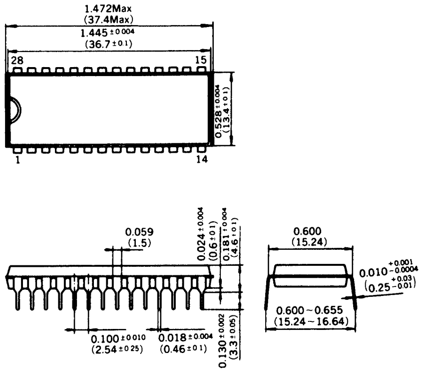
[NOTE] RECOMMENDATIONS

1. The SMM6365C is a mask programmable ROM on a CMOS chip. In the data read mode, transient current will flow in the chip at the time of transistor switching transition.
   For protection of such transients, it is recommended to connect a high-frequency capacitor and an electrolytic capacitor between the power supplies V_{DD} and V_{SS}.
2. The input and output of the SMM6365C are TTL compatible. It is recommended that, when the chip is connected to TTL, pull-up resistors be connected to the $\overline{CE}$, CS1/$\overline{CS1}$, CS2/$\overline{CS2}$, $\overline{OE}$ and address input terminal.

■ PACKAGE DIMENSIONS

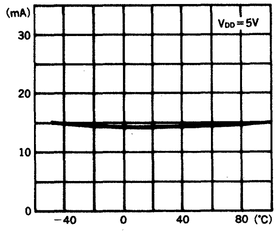
C28

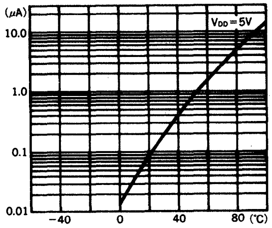
28-pin DIP

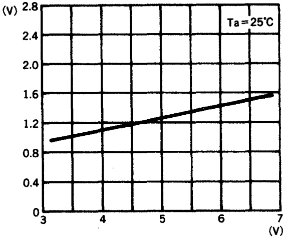


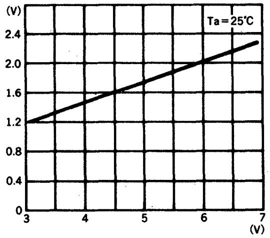
unit : inch
(mm)

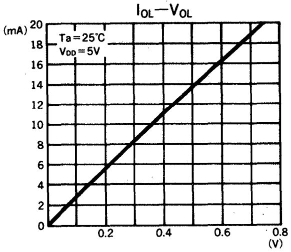
■ CHARACTERISTICS CURVES

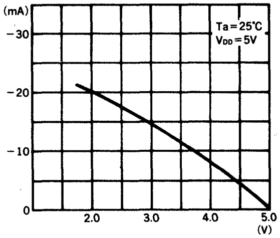

I_{DDO}—Ta

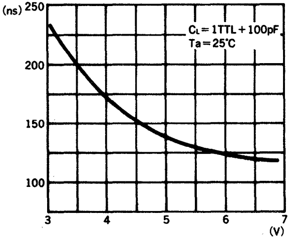

I_{DDS}—Ta

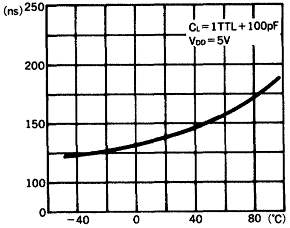

V_{IL}—V_{DD}

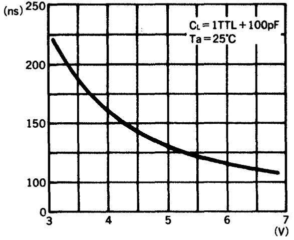

V_{IH}—V_{DD}

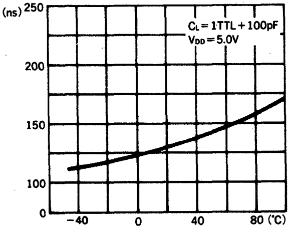

I_{OL}—V_{OL}

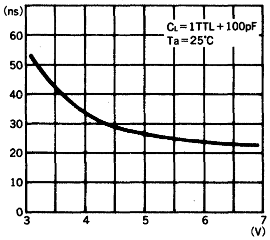

I_{OH}—V_{OH}

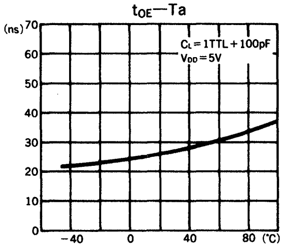

t_{ACE}—V_{DD}


t_{ACE}—Ta


t_{ACC}—V_{DD}


t_{ACC}—Ta


t_{OE}—V_{DD}


t_{OE}—Ta

SMM6312C

CMOS 128K-BIT MASK ROM

- ●Low Supply Current
- ●Access Time 250ns
- ●16,384 Words×8 Bits Asynchronous

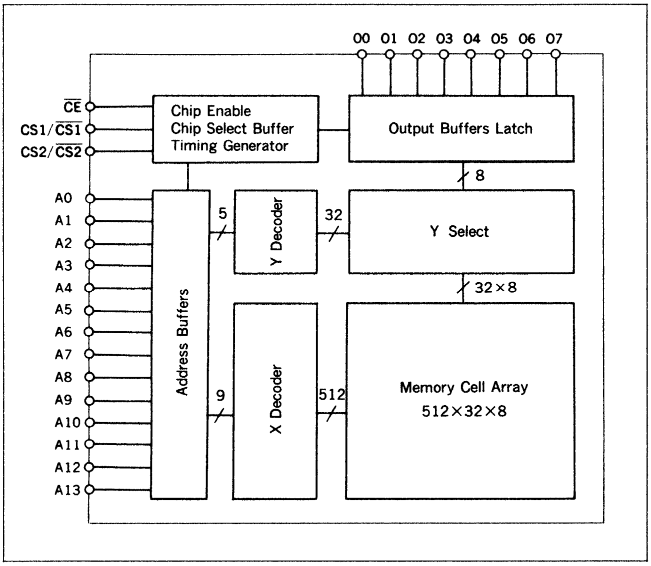
■ DESCRIPTION

The SMM6312C is a 16,384 words × 8 bits asynchronous CMOS mask programmable ROM. This device operates on a single power supply, its input and output levels are TTL compatible and the outputs are 3 state types. This device does not require clock circuit ; it has a detection circuit which detects the difference of address, CS1/$\overline{\text{CS1}}$, CS2/$\overline{\text{CS2}}$ and $\overline{\text{CE}}$ input. With the detected signal, the timing signal is generated (internal synchronous type). With such a significant performance, power dissipation is low, processing speed is high and it can be used for various applications.

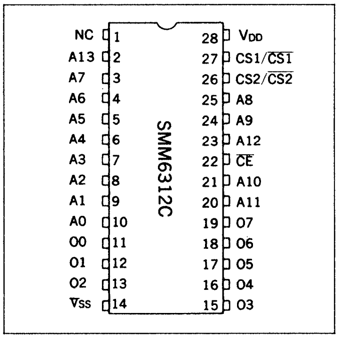
■ FEATURES

- ● Access time ··250ns
- ● Low supply current······································standby : 0.1μA (Typ)
  operation : 16mA (Typ)
- ● Single power supply ·····························5V±10%
- ● Internal synchronous type
- ● TTL compatible inputs and outputs
- ● 3-state output with wired-OR capability
- ● Package ···28-pin DIP (plastic)

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



■ PIN DESCRIPTION

A0 to A13	Address Input
$\overline{\text{CE}}$	Chip Enable
CS1/$\overline{\text{CS1}}$, CS2/$\overline{\text{CS2}}$	Chip Select
O0 to O7	Data Output
VDD	Power Supply (+5V)
Vss	Power Supply (0V)
NC	No connection

■ ABSOLUTE MAXIMUM RATINGS

($V_{SS}=0V$)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.5 to 7.0	V
Input voltage	V_I	−0.5 to $V_{DD}+0.3$	V
Output voltage	V_O	−0.5 to $V_{DD}+0.3$	V
Power dissipation	P_D	1.0	W
DC output current	I_O	10	mA
Operating temperature	T_{opr}	−10 to 70	℃
Storage temperature	T_{stg}	−65 to 150	℃
Soldering temperature and time	T_{sol}	260℃, 10s (at lead)	—

■ ELECTRICAL CHARACTERISTICS

● DC Characteristics

($V_{DD}=+5V\pm10\%$, $V_{SS}=0V$, $Ta=-10$ to $+70$℃)

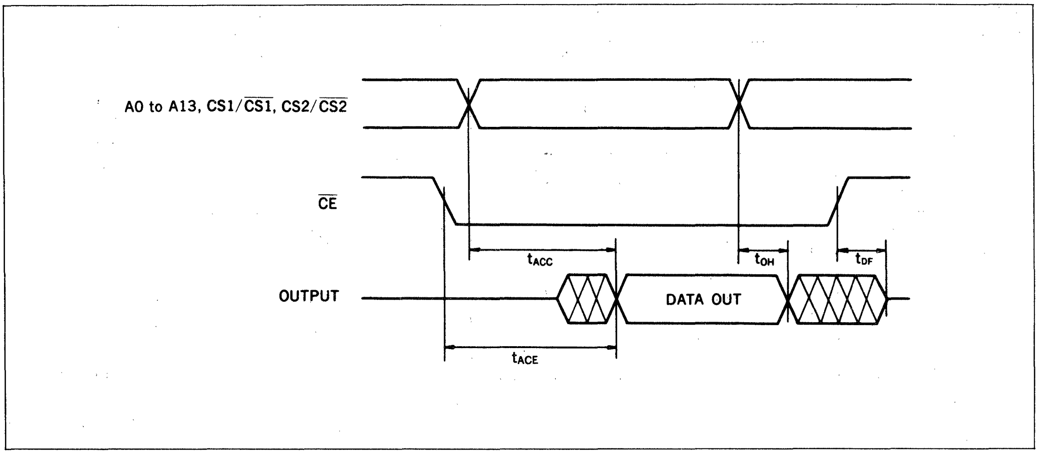
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High level input voltage	V_{IH}		2.2	—	$V_{DD}+0.3$	V
Low level input voltage	V_{IL}		−0.5	—	0.8	V
Input leakage current	I_{LI}	$0\leqq V_I\leqq V_{DD}$	−2.0	—	2.0	μA
Standby supply current	I_{DDS}	$\overline{CE}=V_{DD}-0.2V$	—	0.1	40	μA
Operating supply current	I_{DDO}	with output open	—	16	30	mA
Output leakage current	I_{LO}	$0\leqq V_O\leqq V_{DD}$	−10.0	—	10.0	μA
High level output voltage	V_{OH}	$I_{OH}=-1.0mA$	2.4	—	—	V
Low level output voltage	V_{OL}	$I_{OL}=3.2mA$	—	—	0.4	V
Input capacitance	C_I	f=1MHz	—	—	10	pF
Output capacitance	C_O	f=1MHz	—	—	15	pF

● AC Characteristics

($V_{DD}=+5V\pm10\%$, $V_{SS}=0V$, $Ta=-10$ to $+70$℃)

Parameter	Symbol	Conditions	Min	Max	Unit
Read cycle time	t_{RC}	$C_L=1TTL+100pF$ $V_{IH}=2.2V$ $V_{IL}=0.8V$ $V_{OH}=1.5V$ $V_{OL}=1.5V$ tr=tf=10ns	250	—	ns
Address access time	t_{ACC}		—	250	ns
$\overline{CE}$ access time	t_{ACE}		—	250	ns
Output floating	t_{DF}		—	80	ns
Output hold time	t_{OH}		0	—	ns

● Timing Chart



FUNCTIONS

Truth Table

$\overline{CE}$	CS1/$\overline{CS1}$, CS2/$\overline{CS2}$, A0 to A13	O0 to O7	MODE
H	X	Hi-Z	Standby
L	Stable	Output data	Read

X : "H" or "L"

Read mode

Data can be read by simply setting an address with $\overline{CE}$ held at "L", CS1/$\overline{CS1}$, CS2/$\overline{CS2}$ at each active level. At the time of power-on the initial state cannot be determined because of the operation of the internal clock circuit. If the power is on in the mode of holding $\overline{CE}$ "L" and a certain address is fixed, the data related to the address may not appear. Data should be read after the supply voltage becomes stable, and $\overline{CE}$ is set at "H" or the address input is changed in the mode of $\overline{CE}$ "L".

Standby mode

Setting $\overline{CE}$ at "H" initiates the standby mode. In this mode, the output impedance goes high and all address input is disabled.

Specifying CS1/$\overline{CS1}$, CS2/$\overline{CS2}$

CS1/$\overline{CS1}$, CS2/$\overline{CS2}$ is mask programmable and may be selected for either active level. When ordering, specify the active level.

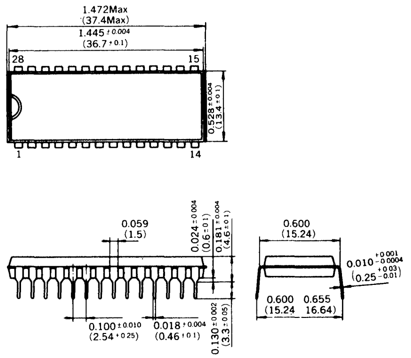
[NOTE] **RECOMMENDATIONS**

1. The SMM6312C is a mask programmable ROM on a CMOS chip. In the data read mode, transient current will flow in the chip at the time of transistor transition. For protection of such transients, it is recommended to connect a high-frequency capacitor and an electrolytic capacitor between the power supplies V_{DD} and V_{SS}.
2. The input and output of SMM6312C are TTL compatible. It is recommended that, when the chip is connected to TTL, pull up resistors be connected to the $\overline{CE}$, CS1/$\overline{CS1}$, CS2/$\overline{CS2}$ and address input terminal.

PACKAGE DIMENSIONS

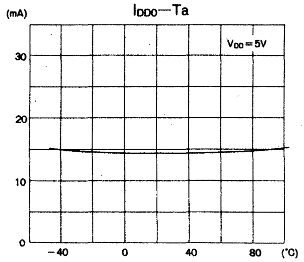
C28

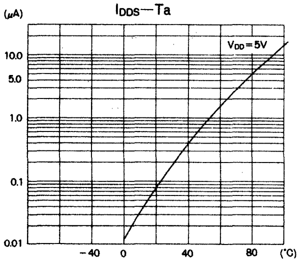
28-pin DIP

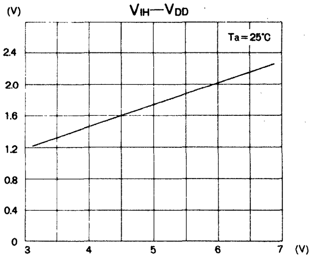


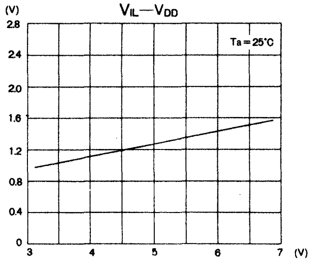
unit : inch
(mm)

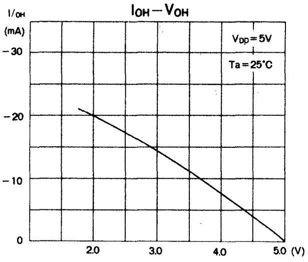
CHARACTERISTICS CURVES

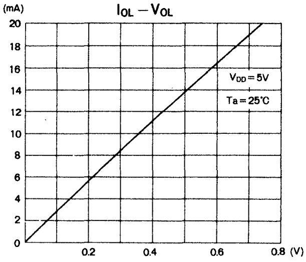

I_{DDO}—Ta

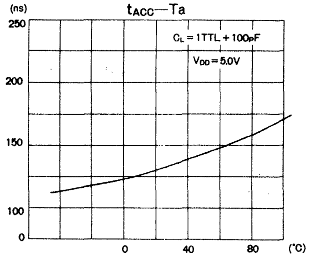

I_{DDS}—Ta

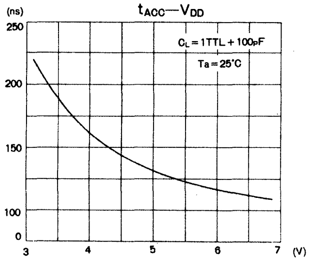

V_{IH}—V_{DD}

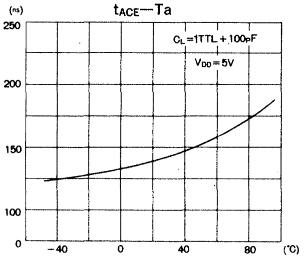

V_{IL}—V_{DD}

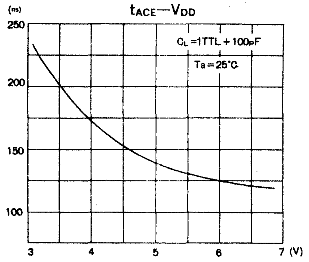

I_{OH}—V_{OH}


I_{OL} — V_{OL}


t_{ACC}—Ta


t_{ACC}—V_{DD}


t_{ACE}—Ta


t_{ACE}—V_{DD}

SMM6313C

CMOS 128K-BIT MASK ROM

- ●Low Supply Current
- ●Access Time 250ns
- ●16,384 Words×8 Bits Asynchronous

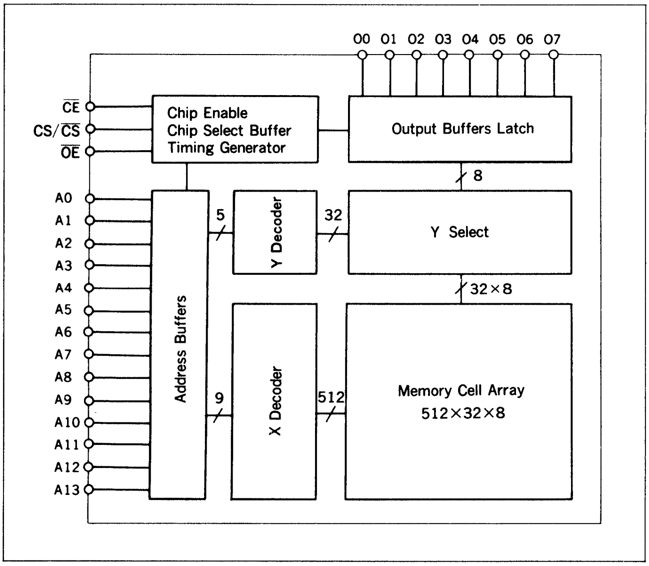
■DESCRIPTION

The SMM6313C is a 16,384 words × 8 bits asynchronous CMOS mask programmable ROM. This device operates on a single power supply, its input and output levels are TTL compatible and the outputs are 3 state types. This device does not require clock circuit ; it has a detection circuit which detects the difference of address, CS/$\overline{\text{CS}}$ and $\overline{\text{CE}}$ input. With the detected signal, the timing signal is generated (internal synchronous type). With such a significant performance, power dissipation is low, processing speed is high and it can be used for various applications.

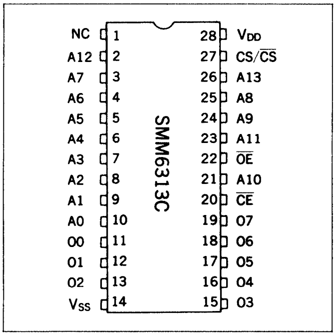
■FEATURES

- ● Access time ··250ns
- ● Low supply current ·····························standby : 0.1μA (Typ)
  operation : 16mA (Typ)
- ● Single power supply ····························5V±10%
- ● Internal synchronous type
- ● TTL compatible inputs and outputs
- ● 3-state output with wired-OR capability
- ● Package ··28-pin DIP (plastic)

■BLOCK DIAGRAM



■PIN CONFIGURATION



■PIN DESCRIPTION

A0 to A13	Address Input
$\overline{\text{CE}}$	Chip Enable
CS/$\overline{\text{CS}}$	Chip Select
$\overline{\text{OE}}$	Output Enable
00 to 07	Data Output
V_{DD}	Power Supply (+5V)
V_{SS}	Power Supply (0V)
NC	No connection

■ ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.5 to 7.0	V
Input voltage	V_I	−0.5 to V_{DD}+0.3	V
Output voltage	V_O	−0.5 to V_{DD}+0.3	V
Power dissipation	P_D	1.0	W
DC output current	I_O	10	mA
Operating temperature	T_{opr}	−10 to 70	℃
Storage temperature	T_{stg}	−65 to 150	℃
Soldering temperature and time	T_{sol}	260°C, 10s (at lead)	—

■ ELECTRICAL CHARACTERISTICS

● DC Characteristics

(V_{DD}=+5V±10%, V_{SS}=0V, Ta=−10 to +70°C)

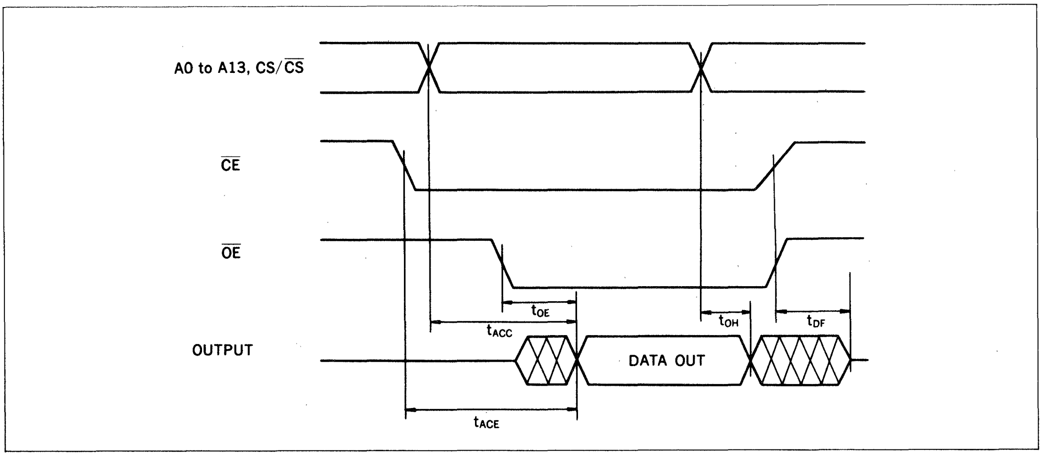
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High level input voltage	V_{IH}		2.2	—	V_{DD}+0.3	V
Low level input voltage	V_{IL}		−0.5	—	0.8	V
Input leakage current	I_{LI}	$0 \leqq V_I \leqq V_{DD}$	−2.0	—	2.0	μA
Standby supply current	I_{DDS}	$\overline{CE}=V_{DD}-0.2V$	—	0.1	40	μA
Operating supply current	I_{DDO}	with output open	—	16	30	mA
Output leakage current	I_{LO}	$0 \leqq V_O \leqq V_{DD}$	−10.0	—	10.0	μA
High level output voltage	V_{OH}	$I_{OH}=-1.0mA$	2.4	—	—	V
Low level output voltage	V_{OL}	$I_{OL}=3.2mA$	—	—	0.4	V
Input capacitance	C_I	f=1MHz	—	—	10	pF
Output capacitance	C_O	f=1MHz	—	—	15	pF

● AC Characteristics

(V_{DD}=+5V±10%, V_{SS}=0V, Ta=−10 to +70°C)

Parameter	Symbol	Conditions	Min	Max	Unit
Read cycle time	t_{RC}	C_L=1TTL+100pF V_{IH}=2.2V V_{IL}=0.8V V_{OH}=1.5V V_{OL}=1.5V tr=tf=10ns	250	—	ns
Address access time	t_{ACC}		—	250	ns
$\overline{CE}$ access time	t_{ACE}		—	250	ns
$\overline{OE}$ access time	t_{OE}		—	80	ns
Output floating	t_{DF}		—	80	ns
Output hold time	t_{OH}		0	—	ns

● Timing Chart



■ FUNCTIONS

● Truth Table

$\overline{\text{CE}}$	CS/$\overline{\text{CS}}$, A0 to A13	$\overline{\text{OE}}$	O0 to O7	MODE
H	X	X	Hi-Z	Standby
L	Stable	H	Hi-Z	Output disable
L	Stable	L	Output data	Read

X : "H" or "L"

● Read mode

Data can be read by simply setting an address with $\overline{\text{CE}}$ held at "L", $\overline{\text{OE}}$ at "L", CS/$\overline{\text{CS}}$ at each active level. At the time of power-on the initial state cannot be determined because of the operation of the internal clock circuit. If the power is on in the mode of holding $\overline{\text{CE}}$ "L" and a certain address is fixed, the data related to the address may not appear. Data should be read after the supply voltage becomes stable, and $\overline{\text{CE}}$ is set at "H" or the address input is changed in the mode of $\overline{\text{CE}}$ "L".

● Standby mode

Setting $\overline{\text{CE}}$ at "H" initiates the standby mode. In this mode, the output impedance goes high and all address input is disabled.

● Output disable

When $\overline{\text{OE}}$ is set at "H", the output impedance goes high.

● Specifying CS/$\overline{\text{CS}}$

CS/$\overline{\text{CS}}$ is mask programmable and may be selected for either active level. When ordering, specify the active level.

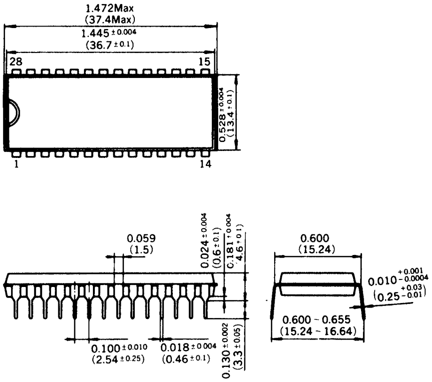
[NOTE] RECOMMENDATIONS

1. The SMM6313C is a mask programmable ROM on a CMOS chip. In the data read mode, transient current will flow in the chip at the time of transistor transition. For protection of such transients, it is reommended to connect a high-frequency capacitor and an electrolytic capacitor between the power supplies V_{DD} and V_{SS}.
2. The input and output of SMM6313C are TTL compatible. It is recommended that, when the chip is connected to TTL, pull up resistors be connected to the $\overline{\text{CE}}$, CS/$\overline{\text{CS}}$ and address input terminal.

■ PACKAGE DIMENSIONS

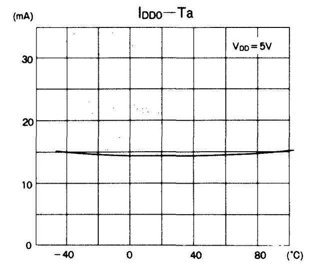
C28

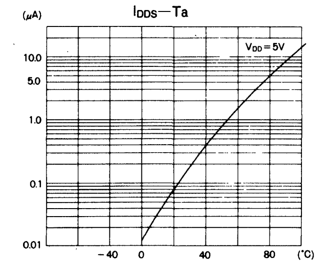
28-pin DIP

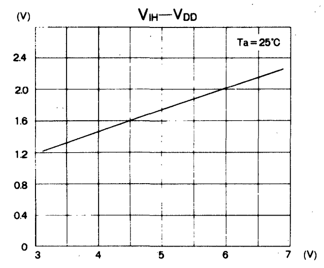


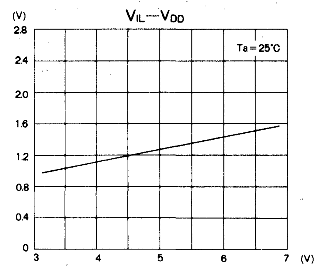
unit : inch
(mm)

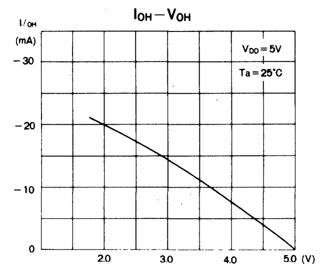
■CHARACTERISTICS CURVES

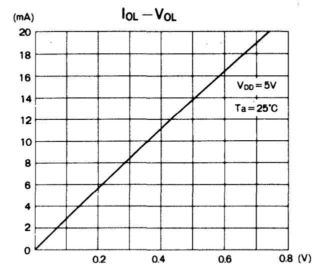

I_{DDO}—Ta

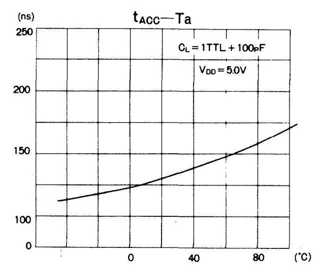

I_{DDS}—Ta

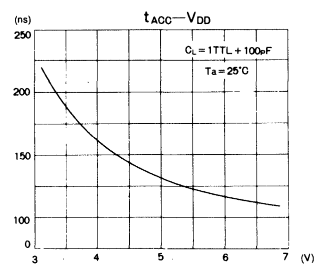

V_{IH}—V_{DD}

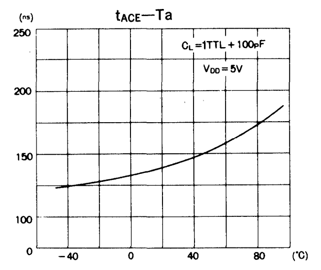

V_{IL}—V_{DD}

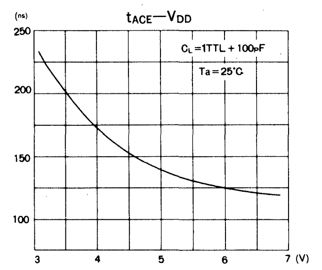

I_{OH}—V_{OH}

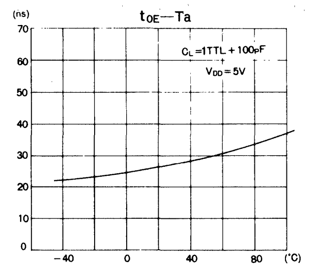

I_{OL}—V_{OL}

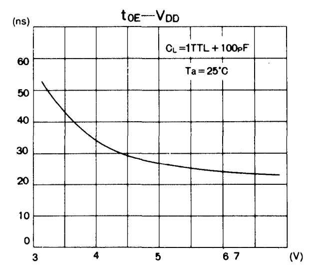

t_{ACC}—Ta


t_{ACC}—V_{DD}


t_{ACE}—Ta


t_{ACE}—V_{DD}


t_{OE}—Ta


t_{OE}—V_{DD}

SMM6325C

CMOS 256K-BIT MASK ROM

- **Low Supply Current**
- **Access Time 250 ns**
- **32,768 Words × 8 Bits Asynchronous**

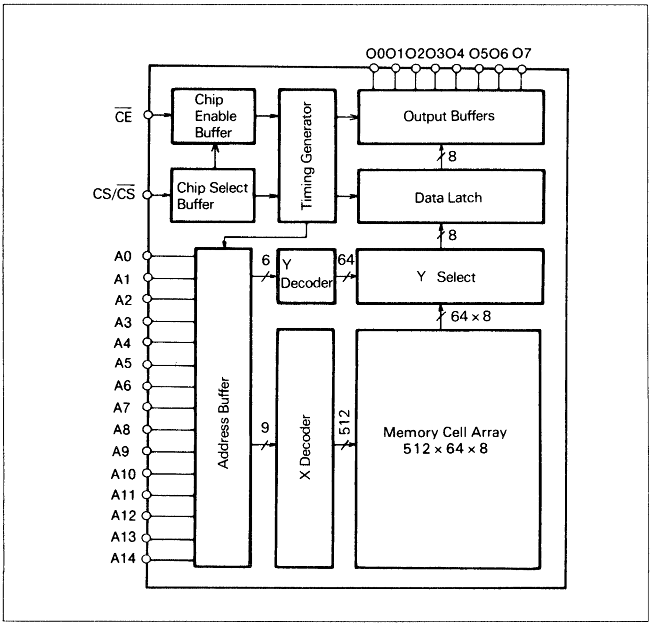
■ DESCRIPTION

The SMM6325C is a 32,768 words x 8 bits asynchronous CMOS mask programmable ROM. This device operates on a single power supply, its input and output levels are TTL compatible and the outputs are 3-state types. The device does not require clock circuit; it has a detection circuit which detects the difference of address, CS/$\overline{CS}$ and $\overline{CE}$ input. With the detected signal, the timing signal is generated (internal synchronous type). With such a significant performance, supply current is low, processing speed is high and it can be used for various applications.

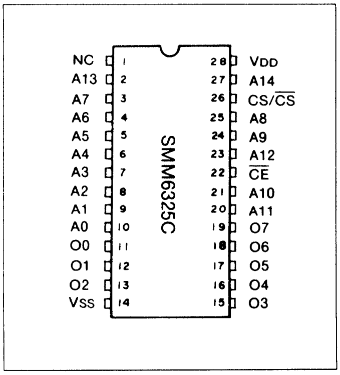
■ FEATURES

- Access time .... 250 ns
- Low supply current .... Standby : 0.1 μA (Typ)
  Operation: 16mA (Typ)
- Internal synchronous type
- Single power supply.. 5V ± 10%
- TTL compatible inputs and outputs
- 3-state output with wired – OR capability
- Package.. 28-pin DIP (plastic)

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



■ PIN DESCRIPTION

A0 to A14	Address Input
$\overline{CE}$	Chip Enable
CS/$\overline{CS}$	Chip Select
O0 to O7	Data Output
VDD	Power Supply (+5V)
Vss	Power Supply (0V)
NC	No connection

■ ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	–0.5 to 7.0	V
Input voltage	V_I	–0.5 to V_{DD} + 0.3	V
Output voltage	V_O	–0.5 to V_{DD} + 0.3	V
Power dissipation	P_D	1.0	W
DC output current	I_O	10	mA
Operating temperature	T_{opr}	–10 to 70	°C
Storage temperature	T_{stg}	–65 to 150	°C
Soldering temperature and time	T_{sol}	260°C, 10 s (at lead)	—

■ ELECTRICAL CHRACTERISTICS

● DC Characteristics

(V_{DD} = 5V ± 10%, V_{SS} = 0V, Ta = –10 to 70°C)

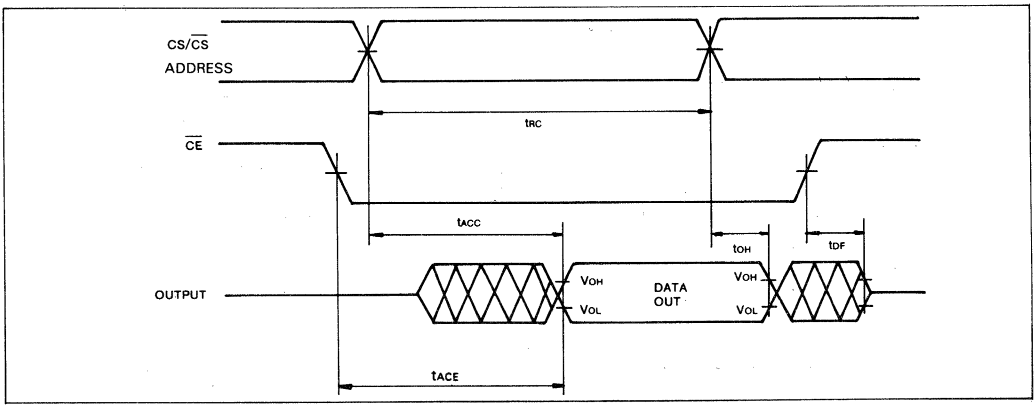
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High level input voltage	V_{IH}		2.2	—	V_{DD} + 0.3	V
Low level input voltage	V_{IL}		–0.5	—	0.8	V
Input leakage current	I_{LI}	$0 \leqq V_I \leqq V_{DD}$	2.0	—	2.0	μA
Standby supply current	I_{DDS}	$\overline{CE} = V_{DD} - 0.2$	—	0.1	40	μA
Operating supply current	I_{DDO}	with output open	—	16	30	mA
Output leakage current	I_{LO}	$0 \leqq V_O \leqq V_{DD}$	–10.0	—	10.0	μA
High level output voltage	V_{OH}	I_{OH} = –1.0 mA	2.4	—	—	V
Low level output voltage	V_{OL}	I_{OL} = 3.2 mA	—	—	0.4	V
Input capacitance	C_I	f = 1 MHz	—	—	10	pF
Output capacitance	C_O	f = 1 MHz	—	—	15	pF

● AC Characteristics

(V_{DD} = 5V ± 10%, V_{SS} = 0V, Ta = –10 to +70°C)

Parameter	Symbol	Conditions	Min	Max	Unit
Read cycle time	t_{RC}	CL = 1TTL + 100 pF V_{IH} = 2.2V V_{IL} = 0.8V V_{OH} = 1.5V V_{OL} = 1.5V tr = tf = 10ns	250	—	ns
Address access time	t_{ACC}		—	250	ns
$\overline{CE}$ access time	t_{ACE}		—	250	ns
Output floating	t_{DF}		—	80	ns
Output hold time	t_{OH}		0	—	ns

● Timing Chart



FUNCTIONS

Truth Table

$\overline{\text{CE}}$	CS/$\overline{\text{CS}}$, A0 to A14	O0 to O7	MODE
H	X	Hi—Z	Standby
L	Stable	Output data	Read

X: H or L

Read mode
Data can be read by simply setting an address and CS/$\overline{\text{CS}}$ with $\overline{\text{CE}}$ held at "L". At the time of power-on, the initial state cannot be determined because of the operation of the internal clock circuit. If the power is on in the mode of CE = "L" and a certain address is fixed, the data related to the address may not appear. Data should be read after the supply voltage becomes stable, and $\overline{\text{CE}}$ is set at "H" or the address input is changed in the mode of $\overline{\text{CE}}$ = "L".

Standby mode
Setting $\overline{\text{CE}}$ at "H" initiates the standby mode. In this mode, the output impedance goes high and all address input is disabled. Within the chip, no circuit allows current flow.

Specifying CS/$\overline{\text{CS}}$
CS/$\overline{\text{CS}}$ is mask programmable and may be selected for either active level.
When ordering, specify the active level CS/$\overline{\text{CS}}$.

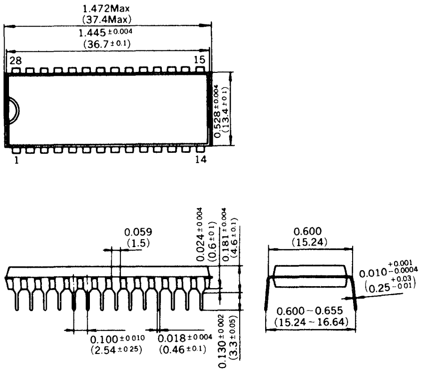
[NOTE] RECOMMENDATIONS

1. The SMM6325C is a mask programmable ROM on a CMOS chip. In the data read mode, transient current will flow in the chip at the time of transistor transition.
   For protection of such transients, it is recommended to connect a high-frequency capacitor and on electrolytic capacitor between the power supplies VDD and VSS.
2. The input and output of the SMM6325C are TTL compatible. It is recommended that, when the chip is connected to TTL, pull-up resistors be connected to the $\overline{\text{CE}}$, CS/$\overline{\text{CS}}$ and address input terminal.

PACKAGE DIMENSIONS

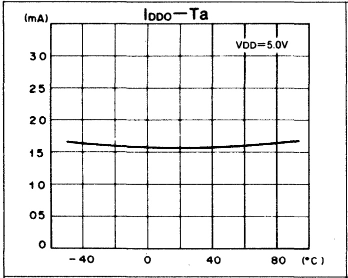
C28

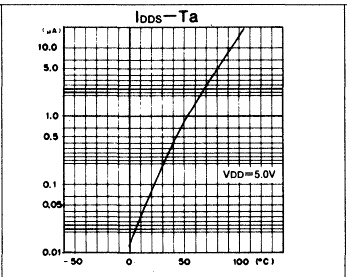
28-pin DIP

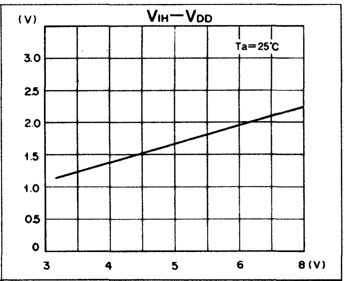


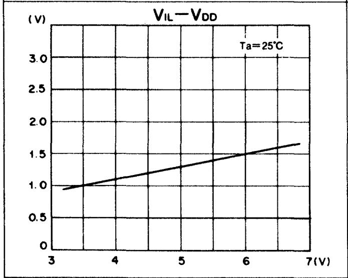
unit : inch
(mm)

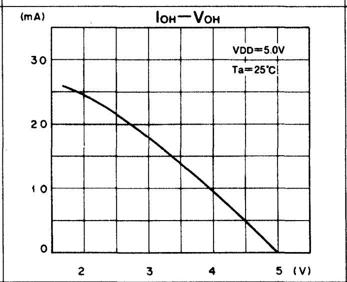
■ CHARACTERISTICS CURVES

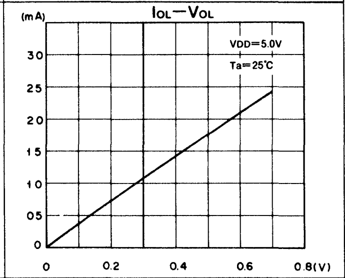

I_{DDO}—Ta

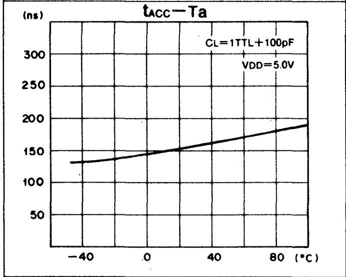

I_{DDS}—Ta

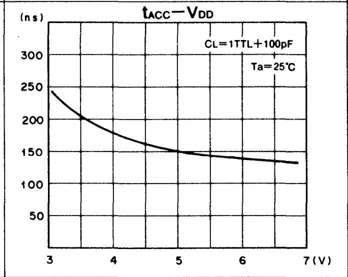

V_{IH}—V_{DD}

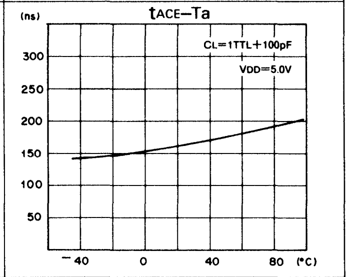

V_{IL}—V_{DD}

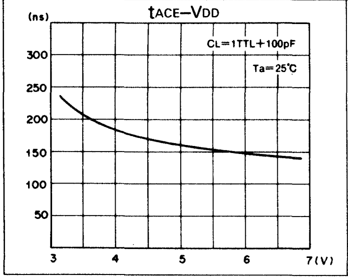

I_{OH}—V_{OH}


I_{OL}—V_{OL}


t_{ACC}—Ta


t_{ACC}—V_{DD}


t_{ACE}—Ta


t_{ACE}—V_{DD}

SMM6326C

CMOS 256K-BIT MASK ROM

- **Low Supply Current**
- **Access Time 250 ns**
- **32,768 Words×8 Bits Asynchronous**

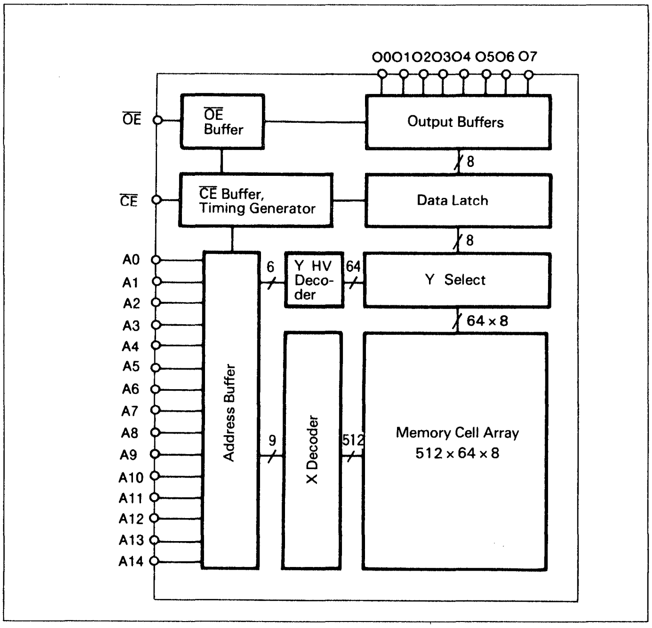
■ DESCRIPTION

The SMM6326C is a 32,768 words × 8 bits asynchronous CMOS mask programmable ROM. This device operates on a signal power supply, its input and output levels are TTL compatible and the outputs are 3-state types. The device does not require clock circuit; it has a detection circuit which detects the difference of address and $\overline{CE}$ input. With the detected signal, the timing signal is generated (internal synchronous type). With such a significant performance, supply current is low, processing speed is high and it can be used for various applications.

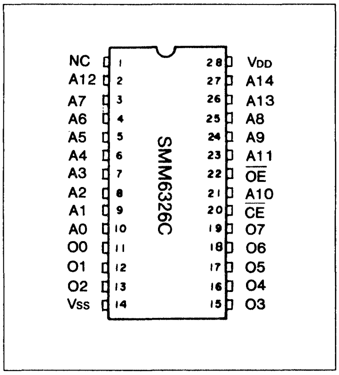
■ FEATURES

- Access time 250ns
- Low supply current .... Standby: 0.1 μA (Typ)
  Operation: 16 mA (Typ)
- Internal synchronous type
- Single power supply.. 5V ± 10%
- TTL compatible inputs and outputs
- 3-state output with wired – OR Capability
- Package... 28-pin DIP (plastic)

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



■ PIN DESCRIPTION

A0 to A14	Address Input
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0 to O7	Data Output
VDD	Power Supply (+5V)
Vss	Power Supply (0V)
NC	No connection

■ ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.5 to 7.0	V
Input voltage	V_I	−0.5 to V_{DD} + 0.3	V
Output voltage	V_O	−0.5 to V_{DD} + 0.3	V
Power dissipation	P_D	1.0	W
DC output current	I_O	10	mA
Operating temperature	T_{opr}	−10 to 70	°C
Storage temperature	T_{stg}	−55 to 125	°C
Soldering temperature and time	T_{sol}	260°C, 10 s (at lead)	—

■ ELECTRICAL CHARACTERISTICS

● DC Characteristics

(V_{DD} = 5V ± 10%, V_{SS}=0V, Ta = −10 to + 70°C)

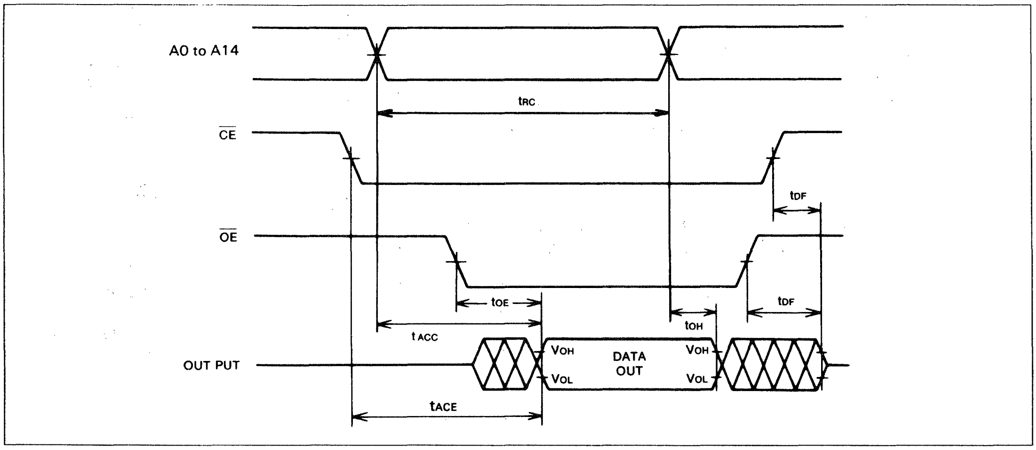
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High level input voltage	V_{IH}		2.2	—	V_{DD} + 0.3	V
Low level input voltage	V_{IL}		−0.5	—	0.8	V
Input leakage current	I_{LI}	$0 \leqq V_I \leqq V_{DD}$	−2.0	—	2.0	μA
Standby supply current	I_{DDS}	$\overline{CE} = V_{DD} - 0.2$	—	0.1	40	μA
Operating supply current	I_{DDO}	with output open	—	16	30	mA
Output leakage current	I_{LO}	$0 \leqq V_O \leqq V_{DD}$	−10.0	—	10.0	μA
High level output voltage	V_{OH}	I_{OH} = −1.0mA	2.4	—	—	V
Low level output voltage	V_{OL}	I_{OL} = 3.2mA	—	—	0.4	V
Input capacitance	C_I	f = 1 MHz	—	—	10	pF
Output capacitance	C_O	f = 1 MHz	—	—	15	pF

● AC Characteristics

(V_{DD} = 5V ± 10%, V_{SS}=0V, Ta = −10 to +70°C)

Parameter	Symbol	Conditions	Min	Max	Unit
Read cycle time	t_{RC}	C_L = ITTL + 100pF	250	—	ns
Address access time	t_{ACC}	V_{IH} = 2.2V	—	250	ns
$\overline{CE}$ access time	t_{ACE}	V_{IL} = 0.8V	—	250	ns
$\overline{OE}$ access time	t_{OE}	V_{OH} = 1.5V	—	80	ns
Output floating	t_{DF}	V_{OL} = 1.5V	—	80	ns
Output hold time	t_{OH}	tr = tf = 10ns	0	—	ns

● Timing Chart



■ FUNCTIONS

● Truth Table

$\overline{CE}$	A0 to A14	$\overline{OE}$	O0 to O7	MODE
H	X	X	Hi–Z	Standby
L	Stable	H	Hi–Z	Output disable
L	Stable	L	Output data	Read

X: "H" or "L"

● Read mode

Data can be read by simply setting an address with $\overline{CE}$ held at "L". At the time of power-on, the initial state cannot be determined because of the operation of the internal clock circuit. If the power is on in the mode of holding $\overline{CE}$ = "L" and a certain address is fixed, the data related to the address may not appear. Data should be read after the supply voltage becomes stable, and $\overline{CE}$ is set at "H" or the address input is changed in the mode of $\overline{CE}$ = "L".

● Standby mode

Setting $\overline{CE}$ at "H" initiates the standby mode. In this mode, the output impedance goes high and all address input is disabled. Within the chip, no circuit allows current flow and only the leakage current exists.

● Out put disable

When $\overline{OE}$ is set at "H", the output impedance goes high.

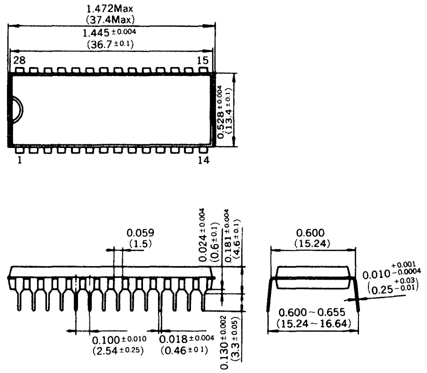
[NOTE] RECOMMENDATIONS

1. The SMM6326C is a mask programmable ROM on a CMOS chip. In the data read mode, transient current will flow in the chip at the time of transistor transition.
   For protection of such transients, it is recommended to connect a high-frequency capacitor and on electrolyticcapacitor between the power supplies VDD and VSS.
2. The input and output of the SMM6326C are TTL compatible. It is recommended that, when the chip is connected to TTL, pull-up resistors be connected to the $\overline{CE}$, $\overline{OE}$ and address input terminal.

■ PACKAGE DIMENSIONS

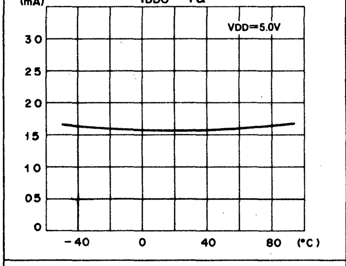
C28

28-pin DIP

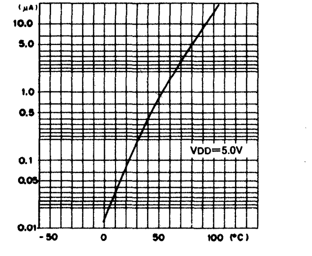


unit: inch
(mm)

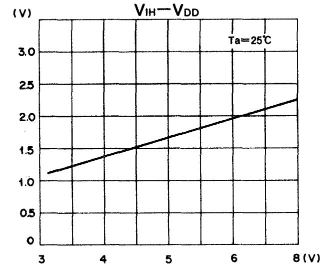
■ CHARACTERISTICS CURVES



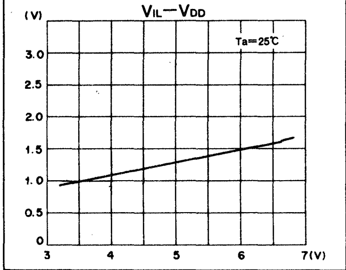
I_{DDO}—Ta



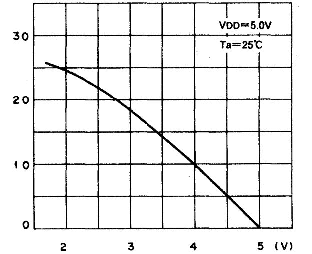
I_{DDS}—Ta



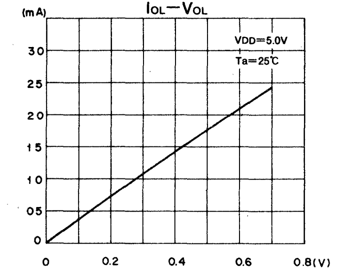
V_{IH}—V_{DD}



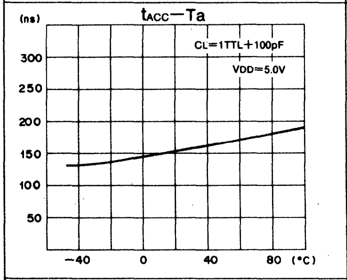
V_{IL}—V_{DD}



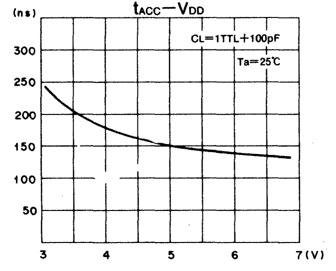
I_{OH}—V_{OH}



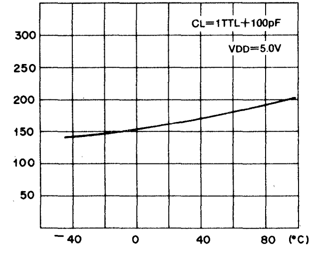
I_{OL}—V_{OL}



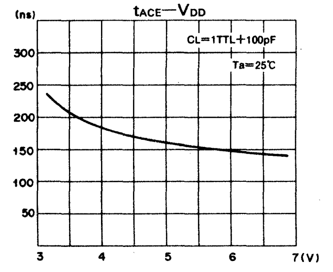
t_{ACC}—Ta



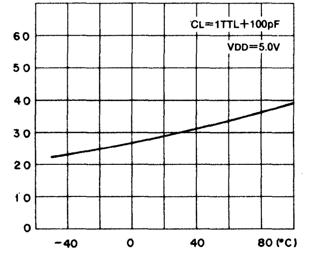
t_{ACC}—V_{DD}



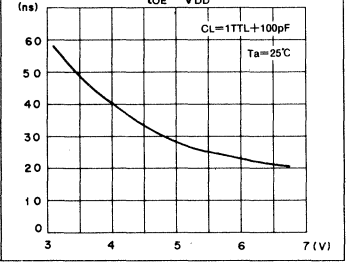
t_{ACE}—Ta



t_{ACE}—V_{DD}



t_{OE}—Ta



t_{OE}—V_{DD}

SMM43100C

CMOS 1M-BIT MASK ROM

- ●Low supply current
- ●Access time 100ns
- ●131,072words × 8bits asynchronous

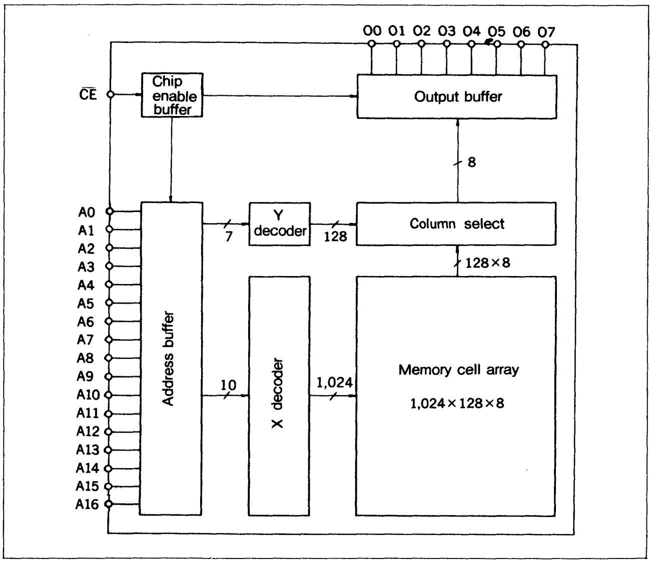
■DESCRIPTION

The SMM43100C is a 131,072 words × 8 bits mask programmable asynchronous CMOS read-only memory (ROM) and operates on a single power source. Both the input and output ports are TTL compatible with 3-state output. This memory requires no external clock, since it has perfect static operation.

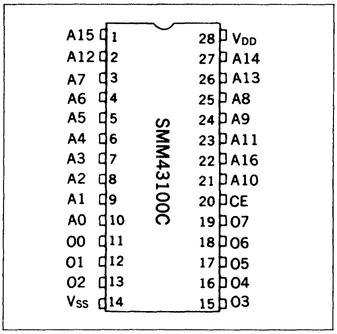
■FEATURES

- ●Access time ······································100ns
- ●Low supply current ································Standby : 0.1μA (Typ)
  Operation : 30mA (Typ)
- ●Asynchronous type
- ●Single power supply ······························5V ±10%
- ●TTL-compatible input and output
- ●3-state output with wired-OR capability
- ●Package··28-pin DIP (plastic)

■BLOCK DIAGRAM



■PIN CONFIGURATION



■PIN DESCRIPTION

A0 to A16	Address input
CE	Chip enable
O0 to O7	Data output
V_{DD}	Power supply(+5V)
V_{SS}	Power supply(0V)

■ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	-0.3 to 7.0	V
Input voltage	V_I	-0.3 to $V_{DD}+0.3$	V
Output voltage	V_O	-0.3 to $V_{DD}+0.3$	V
Power dissipation	P_D	1.0	W
Output current	I_O	10	mA
Operating temperature	T_{opr}	-10 to 70	°C
Storage temperature	T_{stg}	-65 to 150	°C
Soldering temperature and time	T_{sol}	260°C, 10s (at lead)	—

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

($V_{DD}=5V \pm 10\%$, Ta$=-10°$ to $70°C$)

Parameter	Symbol	Conditions	Min	Typ *	Max	Unit
High level input voltage	V_{IH}	—	2.2	—	$V_{DD}+0.3$	V
Low level input voltage	V_{IL}	—	-0.3	—	0.8	V
Input leakage current	I_{LI}	$0 \leqq V_I \leqq V_{DD}$	-2.0	—	2.0	μA
Standby supply current	I_{DDS}	$\overline{CE}=V_{DD}-0.2$	—	0.1	40	μA
Operating supply current	I_{DDO}	with output pin open	—	30	50	mA
Output leakage current	I_{LO}	$0 \leqq V_O \leqq V_{DD}$	-10.0	—	10.0	μA
High level output voltage	V_{OH}	$I_{OH}=-1.0mA$	2.4	—	—	V
Low level output voltage	V_{OL}	$I_{OL}=3.2mA$	—	—	0.4	V
Input terminal capacitance	C_I	f=1MHz	—	—	10	pF
Output terminal capacitance	C_O	f=1MHz	—	—	15	pF

*Typical values are measured at $V_{DD}=5V$ and Ta = 25°C

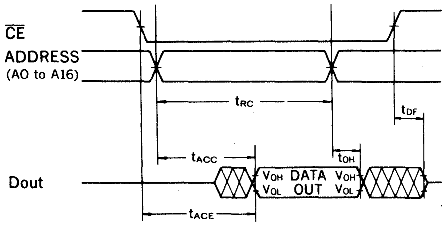
●AC Electrical Characteristics

($V_{DD}=5V \pm 10\%$, Ta $=-10°$ to $70°C$)

Parameter	Symbol	Conditions	Min	Max	Unit
Read cycle time	t_{RC}	• Input pulse level : $V_{IH}=2.4V$ $V_{IL}=0.6V$ • $C_L=1TTL+100pF$ • Input/Output Reference level : 1.5V tr=tf=10ns	100	—	ns
Address access time	t_{ACC}		—	100	ns
$\overline{CE}$ access time	t_{ACE}		—	100	ns
Output floating time	t_{DF}		—	40	ns
Output hold time	t_{OH}		0	—	ns

●Timing Chart

○ **Read Cycle**



FUNCTIONS

Truth table

$\overline{CE}$	A0 to A16	O0 to O7	Mode
H	X	High impedance	Standby
L	Stable	Output data	Read

X : "H" or "L"

Reading data

Data can be read by setting addresses while holding $\overline{CE}$ = "L".

Standby mode

When $\overline{CE}$ is "H", the memory is in the standby mode. In this mode, the output terminals are in the high impedance state and any input of address is prohibited. There will be no current flow except for leakage in the chip.

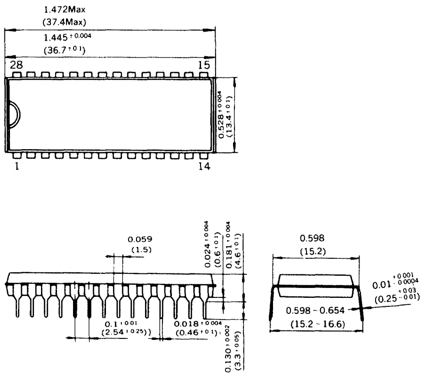
[Note] Recommendations

1. Although the SMM43100C is a CMOS mask ROM, transient current will flow at the time of transistors transition in data read operation. For protection of such transient current, it is recommended to connect a high-frequency capacitor and an electrolytic capacitor between power supply lines V_{DD} and V_{SS}.
2. Although the input and output ports of the SMM43100C are TTL compatible, when it is connected to TTL ICs, it is advisable to connect a pull-up resistor to each of the $\overline{CE}$ and the address input terminals.

PACKAGE DIMENSIONS

C28

28-pin DIP



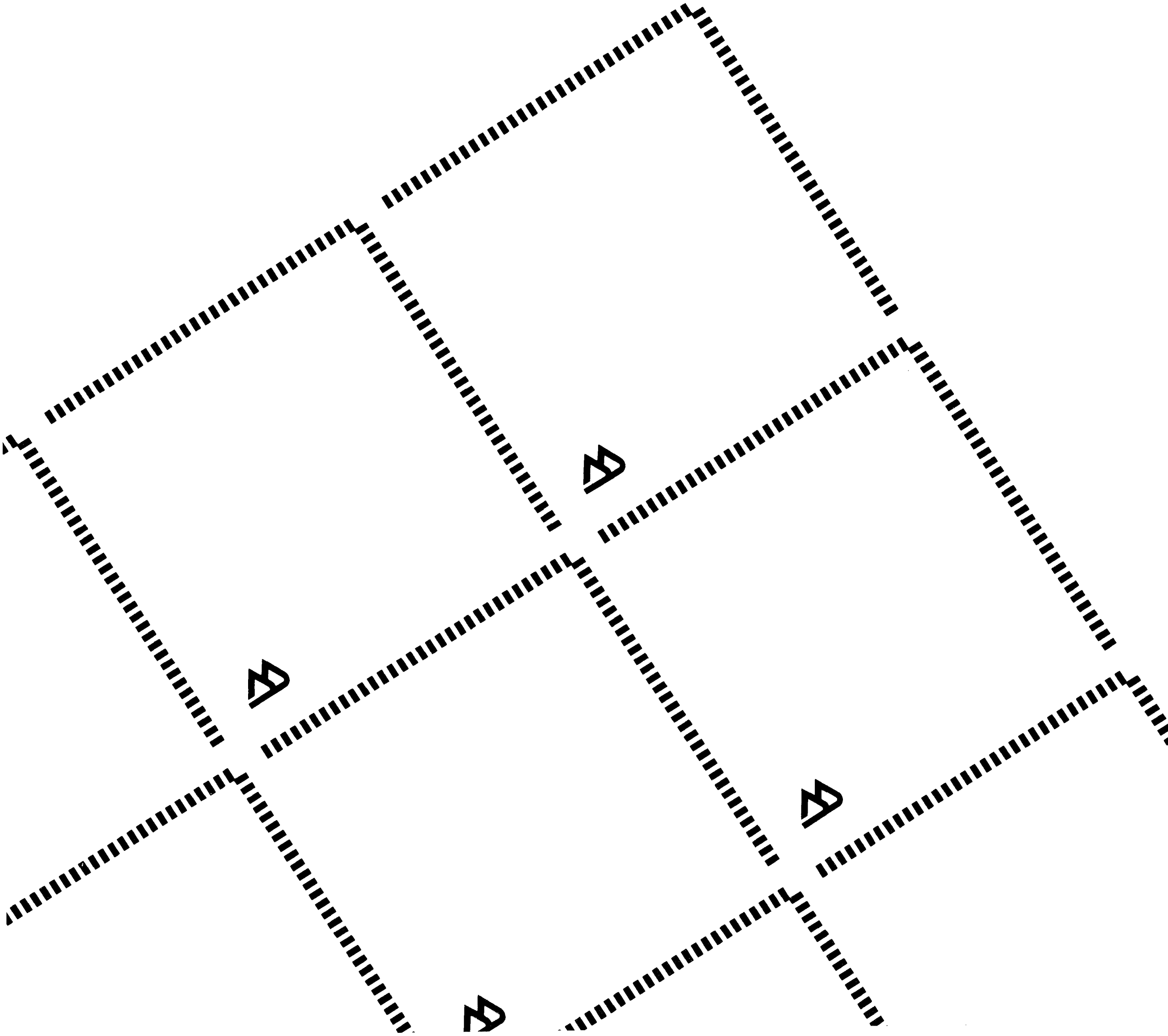
unit : inch
(mm)

■CHARACTERISTICS CURVES

Under measurment

1988/1989 CMOS DATA BOOK

B. MICROCOMPUTERS



SMC1112F

CMOS 4 BIT SINGLE CHIP MICROCOMPUTER

- **Built-in LCD Driver**
- **Single Chip**
- **Low Supply Current**

■ DESCRIPTION

The SMC1112F is a 4-bit CMOS microcomputer which integrates 2K bytes ROM, 128 words RAM, 4 bits input port, 8 bits output port, and 32 × 4 segments LCD driver, 4 bits Timer, etc. on the chip. This provides low power systems for many kinds of applications.

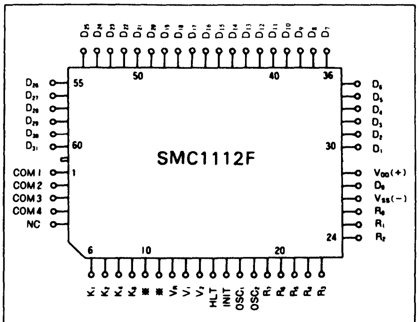
■ FEATURES

- Monolithic .... CMOS LSI
- 4 bis parallel operation
- Low power dissipation .... Typ 30 μA
- Clock frequency .... 32.768 kHz
- Instruction execution time .... 122 μsec
- Instruction set .... 54 kinds
- Mask programmable ROM .... 1920 × 8 bits (Max 2048 × 8 bits)
- Internal RAM .... 128 × 4 bits
- Input port K input .... 4 bits (with pull down resistors)
- Output port R output .... 8 bits Bit manipulate instruction
- LCD driving output .... V-3V, 1/4 duty 4 common outputs 32 segment outputs
- Built-in LCD segment memory .... 32 × 4 bits
- Built-in Timer
- Subroutine nesting .... 4 levels (commonly used for interrupt operation)
- Interrupt operatin .... Timer interrupt or K input Interrupt can be selected by programs
- Built-in oscillator .... Crystal and capacitor external
- Power supply .... VDD — VSS Typ 3V (Logic) VDD — VR Typ 3V (LCD driver)
- Package .... 60-pin QFP(plastic)

■ APPLICATION

Applicable for LCD game, cash register, POS terminal device, portable measuring equipment, automatic vending machine, electric appliance, audio system controller and multi-purpose timer, etc.

■ PIN CONFIGURATION



Top View

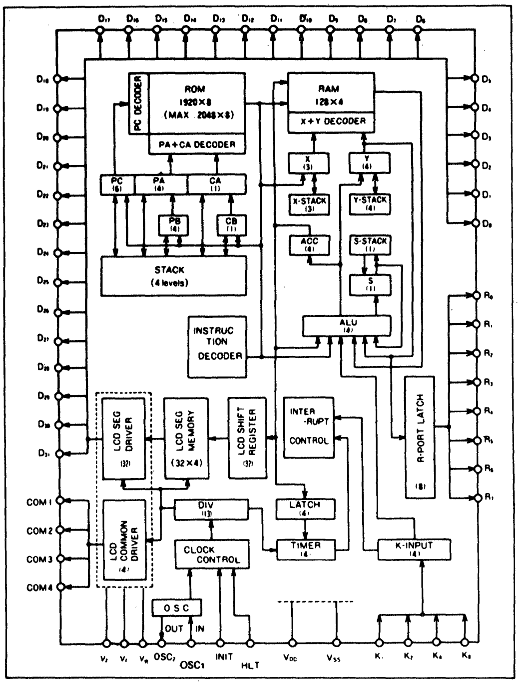
NC: No connection

* Left floating or connected to Vss

60-pin Plastic Quad Flat Package

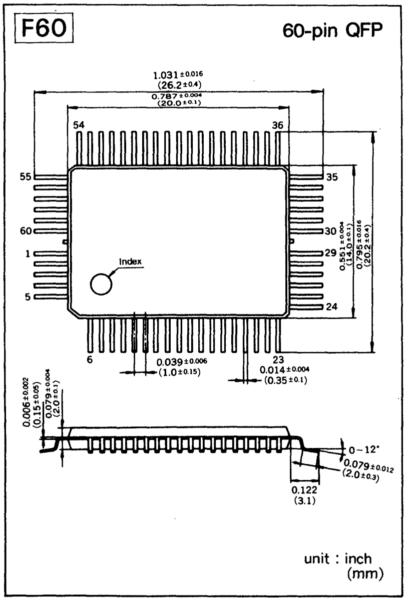
Name	Description
D_0 — D_{31}	LCD driver's segment outputs
COM1 — COM4	LCD driver's common outputs
OSC_1	Oscillator terminal (input)
OSC_2	Oscillator terminal (output)
INIT	Active high input is used to initialize the SMC1112.
HLT	Halt (Hi — stop, Lo — re-start)
K_1, K_2, K_4, K_8	K inputs
R_0 — R_7	R outputs
VDD	Power supply (+)
Vss	Power supply for logic (—)
VR , V_1 , V_2	Power supply for LCD driver (—)

■ BLOCK DIAGRAM



Symbol	Description
ALU	Arithmetic and logic unit
ACC	Accumulator
S	Status register
X	X-register
Y	Y-register
S-STACK	Status stack
X-STACK	X-stack
Y-STACK	Y-stack
PC	Program counter
PA	Page address register
CA	Chapter address register
PB	Page buffer register
CB	Chapter buffer register
STACK	ROM address stack
DIV	13-stage divider

■ PACKAGE DIMENSIONS



■ ELECTRICAL CHARACTERISTICS

1. Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Supply voltage	V_{SS}	−4.5	0.2	V
	V_R	V_{SS}	0.2	V
Input terminal voltage	V_I	$V_{SS}-0.2$	0.2	V
Operating temperature	Topr	−10	65	°C
Storage temperature	Tstg	−40	125	°C

Note: Ground is V_{DD} (= 0V).

2. Operating conditions (fosc = 32.768 kHz)

Parameter	Symbol	Min	Max	Unit
Supply voltage (Logic)	V_{SS}	−3.5	−2.5	V
Supply voltage (LCD driver)	V_R	V_{SS}	−2.5	V
External capacitor for oscillation	C_D	5	30	pF
	C_G	5	30	pF

Note: Ground is V_{DD} (= 0V).

3. Electrical characteristics ($V_{SS} = V_R = -3.0V$, $T_a = 25°C$)

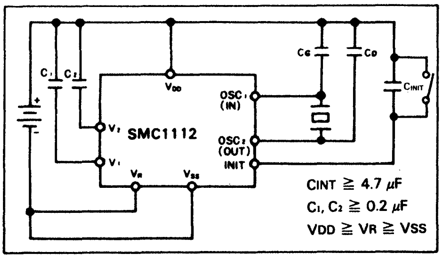
Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Terminal
"H" level input voltage	V_{IH}	−0.5			V		K_8, K_4, K_2, K_1, HLT INIT, OSC_1
"L" level input voltage	V_{IL}			$V_{SS}+0.5$	V		
"H" level output current	I_{OH}			−100	µA	$V_{OH} = -0.6V$	$R_0 - R_7$
"L" level output current	I_{OL}	200			µA	$V_{OL} = V_{SS} + 0.5V$	
LCD common output voltage	V_{CO1}	−0.2		0	V	$R_L = 5\ M\Omega$	COM1 − COM4
	V_{CO2}	−1.2	−1.0	−0.8	V		
	V_{CO3}	−2.2	−2.0	−1.8	V		
	V_{CO4}	V_R		−2.8	V		
LCD segment output voltage	V_{DO1}	−0.2		0	V	$R_L = 5\ M\Omega$	$D_0 - D_{31}$
	V_{DO2}	−1.2	−1.0	−0.8	V		
	V_{DO3}	−2.2	−2.0	−1.8	V		
	V_{DO4}	V_R		−2.8	V		
"H" level input current	I_K	0.5	1.0	3.0	µA		K_8, K_4, K_2, K_1
	I_{HLT}	0.5	1.2	5.0	µA		HLT
	I_{INIT}	5	15	25	µA		INIT
Operating current (Crystal oscillation)	$\lvert I_{SS} \rvert$		20	30	µA	fosc = 32.768 kHz	V_{SS}
	$\lvert I_R \rvert$	4	10	20	µA	No-load	V_R

Note:

- Ground is V_{DD} (= 0V).
- Current flowing into IC is positive and flowing out of IC is negative.

■ FUNDAMENTAL EXTERNAL CONNECTION

For power supply V_{DD} must be common line to V_{SS} and V_R. V_R is adjustable to the optimum voltage to drive Liquid Crystal Display (LCD). Set $V_{DD} \geqq V_R \geqq V_{SS}$ without fail.



$C_{INT} \geqq 4.7\ \mu F$

$C_1, C_2 \geqq 0.2\ \mu F$

$V_{DD} \geqq V_R \geqq V_{SS}$

■ INSTRUCTION TABLE

Function	Mnemonic	OP code	Status effect		Operation
			C	N	
Register to Register	TAY	20			ACC→Y
	TYA	23			Y→ACC
	CLA	7F			0→ACC
Register to Memory	TAM	27			ACC→M(X,Y)
	TAMIYC	25	Y		ACC→M(X,Y), Y + 1→Y
	TAMDYN	24	Y		ACC→M(X,Y),Y − 1→Y
	TAMZA	26			ACC→M(X,Y), 0→ACC
Memory to Register	TMA	21			M(X,Y)→ACC
	TMY	22			M(X,Y)→Y
	XMA	03			M(X,Y)↔ACC
Arithmetic	AMAAC	06	Y		M(X,Y) + ACC→ACC
	SAMAN	3C	Y		M(X,Y) − ACC→ACC
	IMAC	3E	Y		M(X,Y) + 1→ACC
	DMAN	07	Y		M(X,Y) − 1→ACC
	IAC	70	Y		ACC + 1→ACC
	DAN	77	Y		ACC − 1→ACC
	A6AAC	7A	Y		ACC + 6→ACC
	A8AAC	7E	Y		ACC + 8→ACC
	A10AAC	79	Y		ACC + 10→ACC
	IYC	05	Y		Y + 1→Y
	DYN	04	Y		Y − 1→Y
	CPAIZ	3D	Y		$\overline{ACC}$ + 1→ACC
Arithmetic Compare	ALEM	01	Y		ACC ≦ M(X,Y)→STATUS = 1
Logical Compare	MNEA	00		Y	M(X,Y) ≠ ACC→STATUS = 1
	MNEZ	3F		Y	M(X,Y) ≠ 0→STATUS = 1
	YNEA	02		Y	Y ≠ ACC→STATUS = 1
	YNEC	50 − 5F		Y	Y ≠ I(C)→STATUS = 1
Bits in Memory	SBIT	30 − 33			1→M(X,Y,I(B))
	RBIT	34 − 37			0→M(X,Y,I(B))
	TBIT1	38 − 3B		Y	M(X,Y,I(B)) = 1→STATUS = 1
Constants	TCY	40 − 4F			I(C)→Y
	TCMIY	60 − 6F			I(C)→M(X,Y), Y + 1→Y
Input	TKA	08			$K_{8,4,2,1}$ →ACC
	KNEZ	0E		Y	$K_{8,4,2,1}$ ≠ 0→STATUS = 1
Output	SETR	0D			1→R(Y)
	RSTR	0C			0→R(Y)
RAM'X' Addressing	LDX	28 − 2F			I(F)→X
	COMX	09			$\overline{X_{MSB}}$→X_{MSB}
ROM Addressing	LDP	10 − 1F			I(C)→PB
	COMC	0B			$\overline{CB}$→CB

Function	Mnemonic	OP code	Status effect		Operation
			C	N	
ROM Addressing	BR	80 − 8F			1 STATUS = 1 CB→CA,PB→PA,I(W)→PC 2 STATUS = 0 PC + 1→PC,1→STATUS
	CALL	C0 − FF			1 STATUS = 1 CA,PA,PC + 1→STACK, SP + 1→SP CB→CA,PB→PA,I(W)→PC 2 STATUS = 0 PC + 1→PC,1→STATUS
	RETN	0F			STACK→CA,PA,PC,PB SP − 1→SP
	INTRTN	76			STACK→CA,PA,PC,CB,PB SP − 1→SP X-STACK→X,Y-STACK→Y S-STACK→STATUS
LCD Operation	TASR	0A			ACC→LCD S/R,S/R SHIFT
	TSG1	7C			LCD S/R→ SEG.MEMORY (COM1)
	TSG2	7D			LCD S/R→ SEG.MEMORY (COM2)
	TSG3	72			LCD S/R→ SEG.MEMORY (COM3)
	TSG4	73			LCD S/R→ SEG.MEMORY (COM4)
Halt	HALT	71			CPU Stop Restart when "HLT" input goes down to "L" level.
Timer	TMSET	7B			ACC→Timer latch
Interrupt Control	INTEN	74			Enable interrupt after an instruction.
	INTDIS	75			Disable interrupt
	SELIN	78			$ACC_{0,1}$→ Flip-flop of interrupt selector 1 ACC_1 = '1'→ Timer interrupt ACC_1 = '0'→ K-input interrupt 2 ACC_0 = '1'→ Timer clock input ($fosc/2^9$) ACC_0 = '0'→ Timer clock input ($fosc/2^{13}$)

SMC4040C Series

CMOS 4 BIT SINGLE CHIP MICROCOMPUTER

- **Minimum Instruction Cycle Time : 1μs**
- **512 Byte ROM**
- **Low Supply Current**

DESCRIPTION

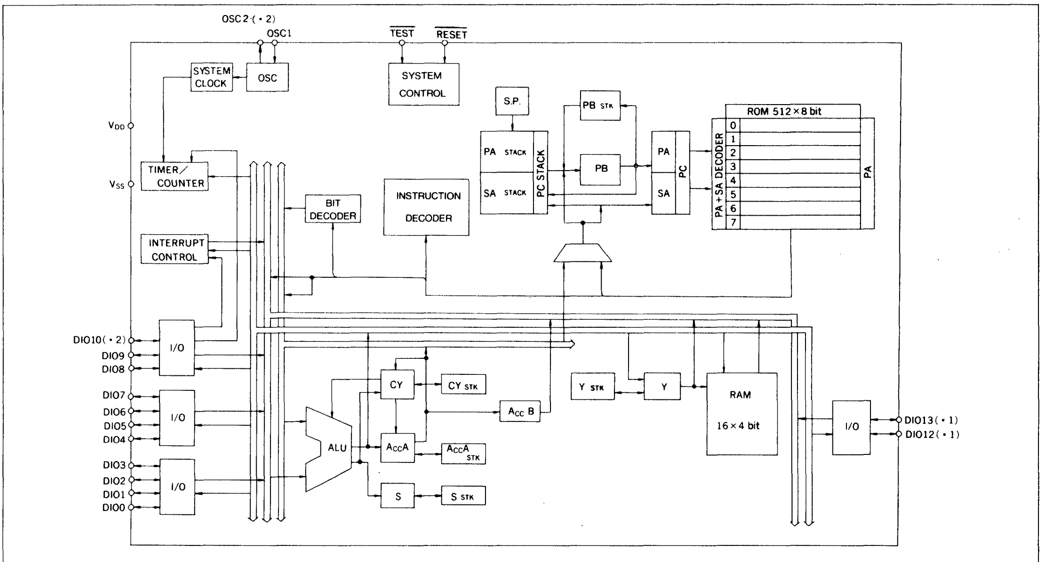
The SMC4040C series is a low supply current type CMOS 4 bit single chip microcomputer featuring high-speed operation (minimum instruction cycle time : 1μs) with a wide voltage range (4 to 6V). It incorporates a RAM, I/O ports, a timer/event counter with a prescaler, and an interrupt control on a single chip. The SMC4040C Series can be flexibly applied to a variety of control systems.

(The SMC4040C Series includes the SMC4040C, SMC4041C)

FEATURES

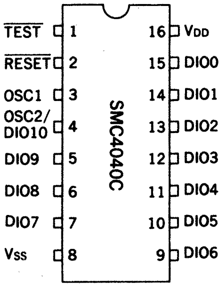
- CMOS LSI 4 bits parallel processing
- Clock frequency·············400kHz to 6MHz
- On-chip oscillator circuit : ceramic oscillator (CR oscillation also available as option)
- Instruction cycle time··············1μs Min
- Instruction set containing 44 instructions
- 512 x 8 bits ROM
- 16 x 4 bits RAM
- 10(SMC4040C) or 12(SMC4041C) I/O ports
- Timer/event counter equipped with 5 bit prescaler/4 bit preset counter
- Interrupt : 1 level (with register stack) ···interrupt by timer/event counter or external input
- Two subroutine nesting levels (common to interrupt)
- Single power supply························5V±20%
- Package·········SMC4040C 16-pin DIP (plastic)
  SMC4041C 18-pin DIP (plastic)

BLOCK DIAGRAM

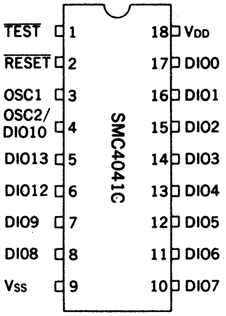


*1 SMC4040C does not connect to DIO12 and DIO13
*2 For external clock input (OSC1), DIO 10 pin can be used instead of OSC2

PIN CONFIGURATION



SMC4040C



SMC4041C

PIN NAMES AND FUNCTIONS

$\overline{\text{TEST}}$	Test input
$\overline{\text{RESET}}$	Reset input
OSC1	Oscillation input
OSC2/DIO10*1	Oscillation output
DIO0 to DIO9	Data input/output
DIO12, DIO13*2	Data input/output
V_{DD}	Power supply (+)
V_{SS}	Power supply (0V)

*1 For external clock input (OSC1), data I/O pin DIO10 can be used instead of OSC2 (by mask option).

*2 SMC4041C

ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.5 to 7.0	V
Input voltage	V_I	−0.5 to V_{DD}+0.3	V
I/O pin voltage	$V_{I/O}$	−0.5 to V_{DD}+0.3	V
Output voltage	V_O	−0.5 to V_{DD}+0.3	V
Power dissipation	P_D	0.3	W
Operating temperature	T_{opr}	−40 to 85	℃
Storage temperature	T_{stg}	−65 to 150	℃
Soldering temperature and time	T_{sol}	260℃, 10s (at lead)	—

* When the internal oscillator circuit is used, the operating temperature range is −20°C to 70°C because of the characteristics of the ceramic oscillator.

RECOMMENDED OPERATING CONDITIONS

(Ta=−40 to 85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}		4	5	6	V
	V_{SS}		—	0	—	V
Clock frequency	f_{OSC}	V_{DD}=4 to 6V	400	—	6000	kHz
Low level peak output current	$I_{OL\ PEAK}$	DIO(OUTPUT)	—	—	10	mA
Low level mean output current	$I_{OL\ AVG}$	DIO(OUTPUT)	—	—	5	mA

ELECTRICAL CHARACTERISTICS

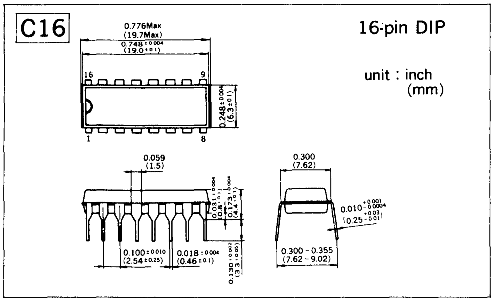
●DC Characteristics

(V_{DD}= 5 V±20%, V_{SS}= 0 V, f_{OSC}= 6 MHz, Ta=−40to85℃)

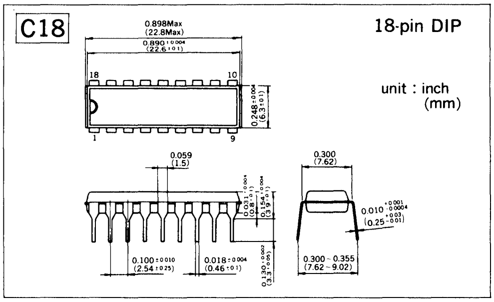
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Low level input current	I_{IL1}	OSC1	−1	—	—	μA
	I_{IL2}	$\overline{\text{RESET}}$, $\overline{\text{TEST}}$, DIO(INPUT)	−120	—	−10	μA
Low level input voltage	V_{IL1}	OSC1	0	—	0.05V_{DD}	V
	V_{IL2}		0	—	0.2V_{DD}	V
High level input voltage	V_{IH1}	OSC1	0.95V_{DD}	—	V_{DD}	V
	V_{IH2}		0.7V_{DD}	—	V_{DD}	V
Low level output current	I_{OL}	V_O=0.1V_{DD}, DIO(OUTPUT)	1.6	—	—	mA
High level output current	I_{OH}	V_O=0.9V_{DD}, DIO(OUTPUT)	—	—	−2	μA
Input leakage current	I_{LI}	V_I=V_{DD}	—	—	1	μA
Operating current	I_{DDO}	f_{OSC}=6MHz, External clock	—	3	—	mA

PACKAGE DIMENSIONS

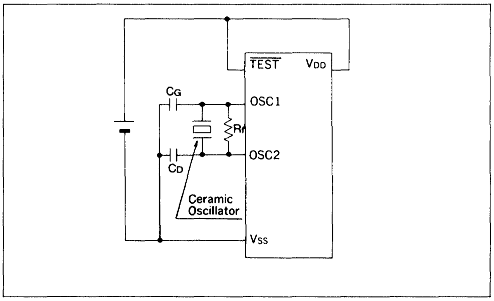
SMC4040C



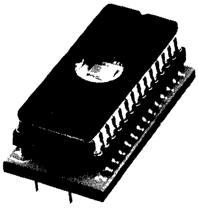
SMC4041C



EXAMPLE OF APPLICATION



Power supply is based on V_{SS}.
Example of oscillator constants
Ceramic oscillator : 6MHz (5V)
R_f : 1M ohm
C_G : 30pF
C_D : 30pF



<Piggy-back package>

SUPPORT TOOLS

The following support tools are available to the SMC4040C Series for efficient programming and debugging.

- Cross assembler: Operates in the CP/M®
- Software simulator: Operates in the CP/M®
- Evaluation chip: Piggy-back package allowing easy on board debugging. Can also be used for debugging small-volume products.
  Used the CMOS type 27C32, or 27C64 EPROM.

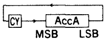
SMC4040C SERIES

Type No.	Number of I/O pins	Package
SMC4040C	10 (11)*	16-pin DIP
SMC4041C	12 (13)*	18-pin DIP

* The parenthesized number applies to the case where the DIO pin is used instead of OSC2 (by mask option) when external clock is applied.

CP/M® is a registered trademark of Digital Research.

INSTRUCTION SETS

Function	Mnemonic	Machine code								Status	Operation
		7	6	5	4	3	2	1	0		
ALU	ADC A, M	0	0	0	0	0	1	0	0	(NC)	AccA, CY ← AccA + M(Y) + CY
	ADD A, i	0	1	1	1	i3	i2	i1	i0	(NC)	AccA ← AccA + i
	ADD A, B	0	0	0	0	0	0	1	1	(NC)	AccA ← AccA + AccB
	ADD A, M	0	0	0	0	0	0	1	0	(NC)	AccA ← AccA + M(Y)
	AND A, B	0	0	0	1	0	0	1	1	(Z)	AccA ← AccA ∧ AccB
	AND A, M	0	0	0	1	0	0	1	0	(Z)	AccA ← AccA ∧ M(Y)
	AND S, M, j	0	1	0	0	1	1	j1	j0	(Z)	Mj(Y) ∧ 1
	INC M	0	0	0	1	0	0	0	1	(NC)	M(Y) ← M(Y) + 1
	INC Y	0	0	0	0	0	0	0	1	(NC)	Y ← Y + 1
	OR A, B	0	0	1	0	0	0	1	1	SET	AccA ← AccA ∨ AccB
	OR A, M	0	0	1	0	0	0	1	0	SET	AccA ← AccA ∨ M(Y)
	XOR S, A, B	0	0	0	0	0	1	0	1	(Z)	AccA ⊻ AccB
	XOR S, A, M	0	0	0	1	0	1	0	1	(Z)	AccA ⊻ M(Y)
ACC	CPL A	0	0	0	0	1	1	1	1	(Z)	AccA ← $\overline{\text{AccA}}$
	EX	0	0	0	1	1	0	0	0	SET	AccA ↔ AccB
	RRA	0	0	0	1	1	1	1	1	($\overline{\text{CY}}$)	
LOAD	LD A, i	0	1	1	0	i3	i2	i1	i0	SET	AccA ← i
	LD A, M	0	0	0	1	1	0	0	1	SET	AccA ← M(Y)
	LD A, O	0	0	1	0	0	0	0	0	SET	AccA ← OUT(Y)
	LD A, Y	0	0	0	1	0	1	1	1	SET	AccA ← Y
	LD B, A	0	0	0	0	1	0	0	0	SET	AccB ← AccA
	LD M, A	0	0	0	0	1	0	0	1	SET	M(Y) ← AccA
	LD Y, i	0	1	0	1	i3	i2	i1	i0	SET	Y ← i
	LD Y, A	0	0	0	0	0	1	1	1	SET	Y ← AccA
	SET CY	0	0	0	0	0	1	1	0	SET	CY ← 1
	RES CY	0	0	0	1	0	1	1	0	SET	CY ← 0
BIT	SET M, j	0	0	1	1	1	0	j1	j0	SET	Mj(Y) ← 1
	RES M, j	0	0	1	1	1	1	j1	j0	SET	Mj(Y) ← 0
I/O	IN A	0	0	0	0	1	0	1	0	SET	AccA ← IN(Y)
	IN M	0	0	0	1	1	0	1	0	SET	M(Y) ← IN(Y)
	OUT A	0	0	0	0	1	0	1	1	SET	OUT(Y) ← AccA
	OUT M	0	0	0	1	1	0	1	1	SET	OUT(Y) ← M(Y)
	SET O, j	0	0	1	1	0	0	j1	j0	SET	OUTj(Y) ← 1
	RES O, j	0	0	1	1	0	1	j1	j0	SET	OUTj(Y) ← 0

Function	Mnemonic	Machine code								Status	Operation
		7	6	5	4	3	2	1	0		
BRANCH	LD PA, p	0	1	0	0	0	p2	p1	p0	SET	PB ← p
	JP S, s	1	1	s5	s4	s3	s2	s1	s0	SET	if S = 1 PA ← PB SA ← s if S = 0 SA ← SA + 1
	JPA S, j	0	1	0	0	1	0	j1	j0	SET	if S = 1 PA ← PB SA5,4 ← j SA3—0 ← AccA if S = 0 SA ← SA + 1
	CALL S, s	1	0	s5	s4	s3	s2	s1	s0	SET	if S = 1 PASTACK ← PA SASTACK ← SA+1 PA ← PB SA ← s SP ← SP + 1 if S = 0 SA ← SA + 1
	RET	0	0	0	0	1	1	0	0	SET	SP ← SP—1 PA ← PB ← PASTACK SA ← SASTACK
	RETI	0	0	0	1	1	1	0	0	S STK	SP ← SP—1 PA ← PASTACK SA ← SASTACK PB ← PBSTK AccA ← AccASTK S ← SSTK Y ← YSTK CY ← CYSTK
SYSTEM	EI	0	0	0	0	1	1	0	1	SET	Interrupt enable
	DI	0	0	0	1	1	1	0	1	SET	Interrupt disable
	NOP	0	1	1	1	0	0	0	0	SET	No operation
	HALT	0	0	0	1	0	0	0	0	SET	SYSTEM Clock Stop Restart when interrupt occur

SMC4050C Series

CMOS 4 BIT SINGLE CHIP MICROCOMPUTERS

- **Minimum Instruction Cycle Time : 1μs**
- **1,024 Byte ROM**
- **Low Supply Current**

■ DESCRIPTION

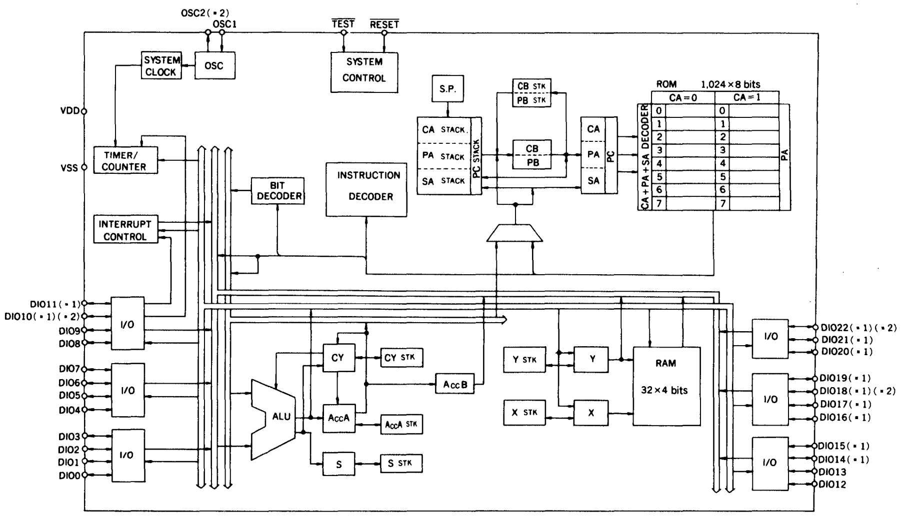
The SMC4050C series is a low supply current type CMOS 4 bit single chip microcomputer featuring high-speed operation (minimum instruction cycle time : 1 μs) with a wide voltage range (4 to 6V). It incorporates a RAM, a ROM, I/O ports, a timer/event counter with a prescaler and an interrupt control on a single chip. The SMC4050C Series can be flexibly applied to a variety of control systems.

(The SMC4050C Series includes the SMC4051C, SMC4052C/M, and SMC4053C.)

■ FEATURES

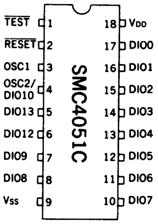
- CMOS LSI 4 bits parallel processing
- Clock frequency ············ 400kHz to 6MHz
- On-chip oscillator circuit···ceramic oscillator (CR oscillation also available as option)
- Instruction cycle time ······ 1 μs Min
- Instruction set containing 46 instructions
- 1024 x 8 bits ROM
- 32 x 4 bits RAM
- 12(SMC4051C), 18(SMC4052C/M) or 22(SMC4053C) I/O ports
- Timer/event counter equipped with 5 bit prescaler/4 bit preset counter
- Interrupt ······················1 level(with register stack) interrupt by timer/event counter or external input
- Two subroutine nesting levels (common to interrupt)
- Single power supply·····5V±20%
- Package······················18-pin DIP (SMC4051C), 24-pin DIP (SMC4052C), 24-pin SOP (SMC4052M), or 28-pin DIP (SMC4053C)

■ BLOCK DIAGRAM

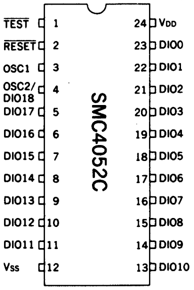


＊1 For models except the SMC4053C, these may or may not be connected to pins. (See PIN CONFIGURATION.)
＊2 For external clock input, an I/O port can be connected to the pin instead of OSC2. (See PIN CONFIGURATION.)

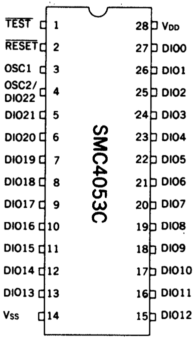
PIN CONFIGURATION



SMC4051C



SMC4052C



SMC4053C

*SMC4052M : This MFP has the same pin configuration as the SMC4052C.

PIN NAMES AND FUNCTIONS

$\overline{\text{TEST}}$	Test input
$\overline{\text{RESET}}$	Reset input
OSC1	Oscillation input
OSC2/DIOXX*1	Oscillation output
DIO0toDIO13*2	Data input/output
DIO0toDIO17*3	Data input/output
DIO0toDIO21*4	Data input/output
V_{DD}	Power supply (+)
V_{SS}	Power supply (0V)

*1 For external clock input (OSC1), data I/O pin DIOXX can be used instead of OSC2 (by mask option).
*2 SMC4051C
*3 SMC4052C/M
*4 SMC4053C

ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.5 to 7.0	V
Input voltage	V_I	−0.5 to V_{DD}+0.3	V
I/O pin voltage	$V_{I/O}$	−0.5 to V_{DD}+0.3	V
Output voltage	V_O	−0.5 to V_{DD}+0.3	V
Power dissipation	P_D	0.3	W
Operating temperature *	T_{opr}	−40 to 85	℃
Storage temperature	T_{stg}	−65 to 150	℃
Soldering temperature and time	T_{sol}	260℃, 10s (at lead)	—

*When the internal oscillator circuit is used, the operating temperature range is −20℃ to 70℃ because of the characteristics of the ceramic oscillator.

RECOMMENDED OPERATING CONDITIONS

(Ta=−40 to 85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}		4	5	6	V
	V_{SS}		—	0	—	V
Clock frequency	f_{OSC}	V_{DD}=4 to 6V	400	—	6000	kHz
Low level peak output current	$I_{OL\ PEAK}$	DIO(OUTPUT)	—	—	10	mA
Low level mean output current	$I_{OL\ AVG}$	DIO(OUTPUT)	—	—	5	mA

ELECTRICAL CHARACTERISTICS

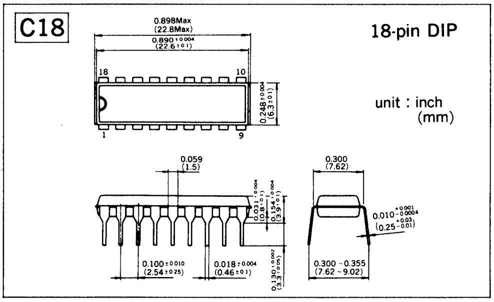
●DC Characteristics

(V_{DD}= 5 V±20%, V_{SS}= 0 V, f_{OSC}= 6 MHz, Ta=−40 to 85℃)

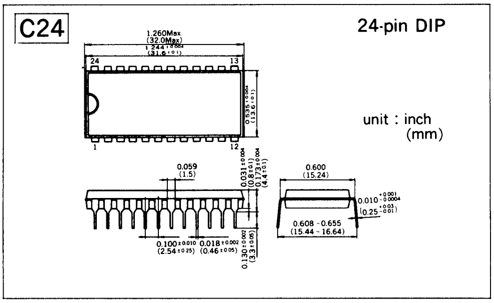
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Low level input current	I_{IL1}	OSC1	−1	—	—	μA
	I_{IL2}	$\overline{\text{RESET}}$, $\overline{\text{TEST}}$, DIO(INPUT)	−120	—	−10	μA
Low level input voltage	V_{IL1}	OSC1	0	—	0.05V_{DD}	V
	V_{IL2}		0	—	0.2V_{DD}	V
High level input voltage	V_{IH1}	OSC1	0.95V_{DD}	—	V_{DD}	V
	V_{IH2}		0.7V_{DD}	—	V_{DD}	V
Low level output current	I_{OL}	V_O=0.1 V_{DD}, DIO(OUTPUT)	1.6	—	—	mA
High level output current	I_{OH}	V_O=0.9 V_{DD}, DIO(OUTPUT)	—	—	−2	μA
Input leakage current	I_{LI}	V_I=V_{DD}	—	—	1	μA
Operating current	I_{DDO}	f_{OSC}=6MHz, External clock	—	5	—	mA

■PACKAGE DIMENSIONS

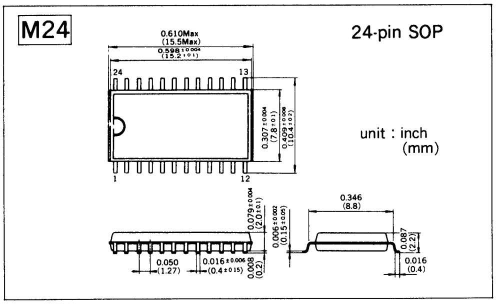
SMC4051C



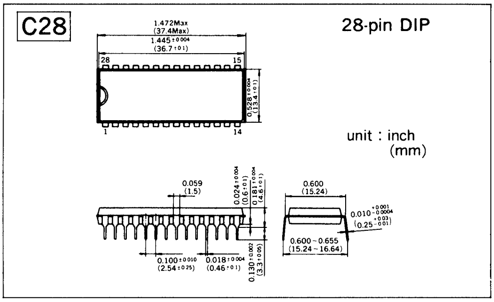
SMC4052C



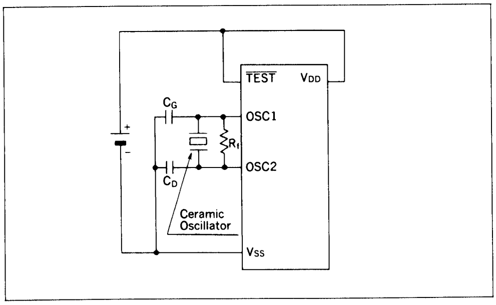
SMC4052M



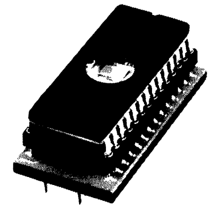
SMC4053C



■EXAMPLE OF APPLICATION



Power supply is based on Vss.
Example of oscillator constants
Ceramic oscillator : 6MHz (5V)
Rf : 1M ohm
CG : 30pF
CD : 30pF



[Piggy-back package]

■SUPPORT TOOLS

The following support tools are available to the SMC4050C Series for efficient programming and debugging:

- Cross assembler·····Operates in the CP/M®
- Software simulator··Operates in the CP/M®
- Evaluation chip·······Piggy-back package allowing easy on-board debugging. Can also be used for debugging small-volume products.
  Used the CMOS type 27C32, or 27C64 EPROM.

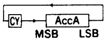
■SMC4050C SERIES

Model	Number of I/O pins	Package
SMC4051C	12 (13)*	18-pin DIP
SMC4052C/M	18 (19)*	24-pin DIP, or 24-pin SOP
SMC4053C	22 (23)*	28-pin DIP

*The parenthesized number applies to the case where the DIO pin is used instead of OSC2 (by mask option) when external clock is applied.

CP/M® is a registered trademark of Digital Research.

INSTRUCTION SETS

Function	Mnemonic	Machine code								Status	Function
		7	6	5	4	3	2	1	0		
ALU	ADC A, M	0	0	0	0	0	1	0	0	(NC)	AccA, CY ← AccA + M(X, Y) + CY
	ADD A, i	0	1	1	1	i3	i2	i1	i0	(NC)	AccA ← AccA + i
	ADD A, B	0	0	0	0	0	0	1	1	(NC)	AccA ← AccA + AccB
	ADD A, M	0	0	0	0	0	0	1	0	(NC)	AccA ← AccA + M(X, Y)
	AND A, B	0	0	0	1	0	0	1	1	(Z)	AccA ← AccA ∧ AccB
	AND A, M	0	0	0	1	0	0	1	0	(Z)	AccA ← AccA ∧ M(X, Y)
	AND S, M, j	0	1	0	0	1	1	j1	j0	(Z)	Mj(X, Y) ∧ 1
	INC M	0	0	0	1	0	0	0	1	(NC)	M(X, Y) ← M(X, Y) + 1
	INC Y	0	0	0	0	0	0	0	1	(NC)	Y ← Y + 1
	OR A, B	0	0	1	0	0	0	1	1	SET	AccA ← AccA ∨ AccB
	OR A, M	0	0	1	0	0	0	1	0	SET	AccA ← AccA ∨ M(X, Y)
	XOR S, A, B	0	0	0	0	0	1	0	1	(Z)	AccA $\veebar$ AccB
	XOR S, A, M	0	0	0	1	0	1	0	1	(Z)	AccA $\veebar$ M(X, Y)
ACC	CPL A	0	0	0	0	1	1	1	1	(Z)	AccA ← $\overline{\text{AccA}}$
	EX	0	0	0	1	1	0	0	0	SET	AccA ↔ AccB
	RRA	0	0	0	1	1	1	1	1	$\overline{\text{(CY)}}$	
LOAD	LD A, i	0	1	1	0	i3	i2	i1	i0	SET	AccA ← i
	LD A, M	0	0	0	1	1	0	0	1	SET	AccA ← M(X, Y)
	LD A, O	0	0	1	0	0	0	0	0	SET	AccA ← OUT(Y)
	LD A, Y	0	0	0	1	0	1	1	1	SET	AccA ← Y
	LD B, A	0	0	0	0	1	0	0	0	SET	AccB ← AccA
	LD M, A	0	0	0	0	1	0	0	1	SET	M(X, Y) ← AccA
	LD X, b	0	0	1	0	0	1	0	b	SET	X ← b
	LD Y, i	0	1	0	1	i3	i2	i1	i0	SET	Y ← i
	LD Y, A	0	0	0	0	0	1	1	1	SET	Y ← AccA
	SET CY	0	0	0	0	0	1	1	0	SET	CY ← 1
	RES CY	0	0	0	1	0	1	1	0	SET	CY ← 0
BIT	SET M, j	0	0	1	1	1	0	j1	j0	SET	Mj(X, Y) ← 1
	RES M, j	0	0	1	1	1	1	j1	j0	SET	Mj(X, Y) ← 0
I/O	IN A	0	0	0	0	1	0	1	0	SET	AccA ← IN(Y)
	IN M	0	0	0	1	1	0	1	0	SET	M(X, Y) ← IN(Y)
	OUT A	0	0	0	0	1	0	1	1	SET	OUT(Y) ← AccA
	OUT M	0	0	0	1	1	0	1	1	SET	OUT(Y) ← M(X, Y)
	SET O, j	0	0	1	1	0	0	j1	j0	SET	OUTj(Y) ← 1
	RES O, j	0	0	1	1	0	1	j1	j0	SET	OUTj(Y) ← 0
BRANCH	LD CA, b	0	0	1	0	1	0	0	b	SET	CB ← b
	LD PA, p	0	1	0	0	0	p2	p1	p0	SET	PB ← p
	JP S, s	1	1	s5	s4	s3	s2	s1	s0	SET	if S = 1 CA ← CB, PA ← PB SA ← s if S = 0 SA ← SA + 1
	JPA S, j	0	1	0	0	1	0	j1	j0	SET	if S = 1 CA ← CB, PA ← PB SA5,4 ← j SA3—0 ← AccA if S = 0 SA ← SA + 1
	CALL S, s	1	0	s5	s4	s3	s2	s1	s0	SET	if S = 1 CA_{STACK} ← CA PA_{STACK} ← PA SA_{STACK} ← SA + 1 CA ← CB, PA ← PB SA ← s, SP ← SP + 1 if S = 0 SA ← SA + 1
	RET	0	0	0	0	1	1	0	0	SET	SP ← SP—1 CA ← CB ← CA_{STACK} PA ← PB ← PA_{STACK} SA ← SA_{STACK}
	RETI	0	0	0	1	1	1	0	0	S STK	SP ← SP—1 CA ← CA_{STACK}, PA ← PA_{STACK} SA ← SA_{STACK}, CB ← CB_{STK} PB ← PB_{STK} AccA ← AccA_{STK} S ← S_{STK}, Y ← Y_{STK} X ← X_{STK}, CY ← CY_{STK}
SYSTEM	EI	0	0	0	0	1	1	0	1	SET	Interrupt enable
	DI	0	0	0	1	1	1	0	1	SET	Interrupt disable
	NOP	0	1	1	1	0	0	0	0	SET	No operation
	HALT	0	0	0	1	0	0	0	0	SET	SYSTEM Clock Stop Restart when interrupt occur

SMC4055C Series

CMOS 4BIT SINGLE CHIP MICROCOMPUTER

- ●IR-remote-controller Use
- ●1,024 Byte ROM
- ●Low Supply Current

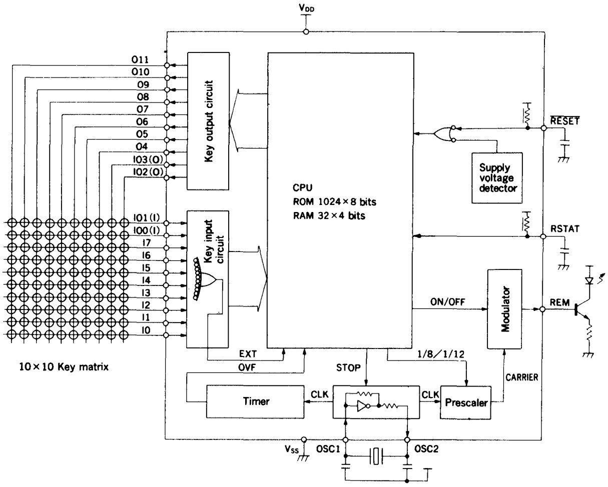
■DESCRIPTION

SMC4055C Series is a low supply current type CMOS 4bit single chip microcomputer for use IR-remote-controller. It incorporates a ROM, RAM, I ports, O ports, timer, carrier modulator with a prescaler and an interrupt controller on a single chip. So several key function types or code types can be flexibly designed by using such functions. Furthermore, it enters a standby mode when the oscillation is stopped by "STOP" instruction. Then, it can return to an operation mode by key interrupt.

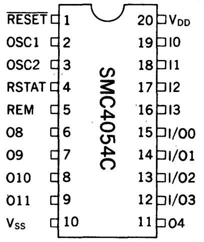
■FEATURES

- ●CMOS LSI 4bits parallel processing
- ●Clock frequency ······ 400 to 500kHz (Ceramic oscillator)
- ●Instruction cycle time···12μs (Min)
- ●On chip prescaler ·····1/8, 1/12
  Each modulation output is selected by instruction control.
  Instruction control modulation output
  1/2 duty or 1/3 duty is optional in 1/12 prescaling
- ●Timer ·····················8bits
- ●Key matrix ···············10×10 or 5×8 (with LCD 6seg output) : 28 pin package 5×8 : 20 pin package
- ●Standby mode ·········"STOP" and key interrupt control
- ●ROM ·····················1,024×8bits
- ●RAM ·····················32×4bits
- ●Instruction sets·········48
- ●Interrupt level ···········1 (Timer or key input)
- ●Subroutine nesting level································
  3 (Common to interrupt)
- ●Single power supply··2.0 to 3.5V
- ●Low supply current ···Operating (No load) : 0.3mA (Typ)
  Standby : 1μA (Typ)
- ●Operating temperature··· −20 to 80°C
- ●Package·················20-pin DIP (plastic)
  28-pin DIP (plastic)
  28-pin SOP (plastic)

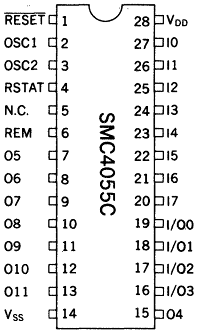
■BLOCK DIAGRAM



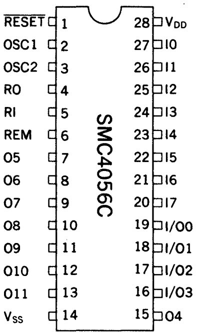
PIN CONFIGURATION



SMC4054C



SMC4055C



SMC4056C

*SMC4055M : This SOP has the same pin configuration as the SMC4055C
*SMC4056M : This SOP has the same pin configuration as the SMC4056C

PIN DESCRIPTION

RESET	Reset input
OSC1	Oscillation input
OSC2	Oscillation output
RSTAT	Restart control
O5 to O11	Data output (LCD drive available)
O4	Data output
I/O0 to I/O3	Key input/output
I0 to I7	Key input
RI, RO	CR oscillation input/output
V_{DD}	Power supply (+)
V_{SS}	Power supply (0V)
REM	Remote control signal output

ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.5 to 7.0	V
Iuput voltage	V_I	−0.5 to V_{DD}+0.3	V
I/O pin voltage	$V_{I/O}$	−0.5 to V_{DD}+0.3	V
Output voltage	V_O	−0.5 to V_{DD}+0.3	V
Power dissipation	P_D	0.3	W
Operating temperature	T_{opr}	−20 to 80	°C
Storage temperature	T_{stg}	−65 to 150	°C
Soldering temperature and time	T_{sol}	260°C, 10s (at lead)	—

RECOMMENDED OPERATING CONDITIONS

(Ta=−20 to 80°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}		2.0	3.0	3.5	V
	V_{SS}		—	0	—	V
Clock frequency	f_{OSC}	V_{DD}=2.0 to 3.5V	400	—	500	kHz

ELECTRICAL CHARACTERISTICS

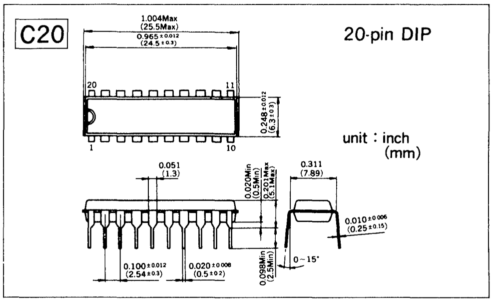
●DC Characteristics

(V_{DD}=2.0 to 3.5V, V_{SS}=0V, f_{OSC}=400 to 500kHz, Ta=−20 to 80°C)

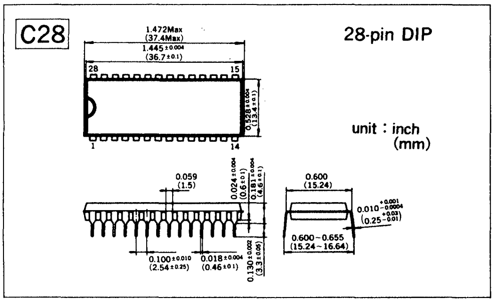
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Low level input current	I_{IL1}	OSC1	−6.5	—	—	μA
	I_{IL2}	I0 to I7, I/O (INPUT)	−35	−12	−3	μA
Low level input voltage	V_{IL1}	OSC1	0	—	0.05V_{DD}	V
	V_{IL2}	I0 to I7, I/O (INPUT)	0	—	0.3V_{DD}	V
High level input voltage	V_{IH1}	OSC1	0.95V_{DD}	—	V_{DD}	V
	V_{IH2}	I0 to I7, I/O (INPUT)	0.7V_{DD}	—	V_{DD}	V
Key ON resistance	$R_{K(ON)}$		—	—	10	kΩ
Key OFF resistance	$R_{K(OFF)}$		400	—	—	kΩ
Low level output current	I_{OL}	V_O=0.1V_{DD}	0.5	—	—	mA
High level output current	I_{OH}	V_O=0.5V_{DD}, REM	—	—	−1.2	mA
Input leakage current	I_{LI}	V_I=V_{DD}	—	—	1	μA
Operating current	I_{DDO}	Operation (No load)	—	0.3	—	mA
	I_{DDS}	Standby (STOP)	—	1	15	μA

■PACKAGE DIMENSIONS

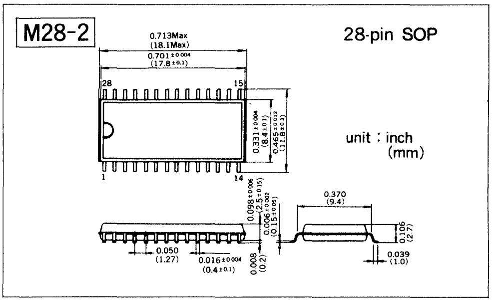
SMC4054C

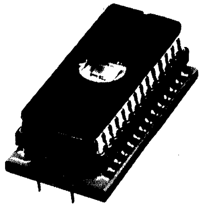


SMC4055C, SMC4056C (under developing)



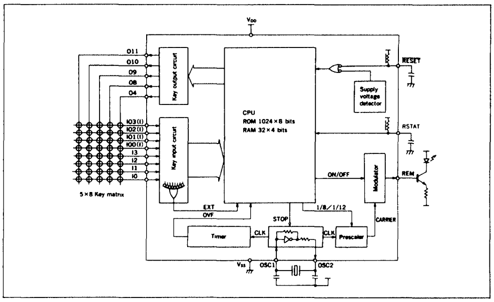
SMC4055M, SMC4056M

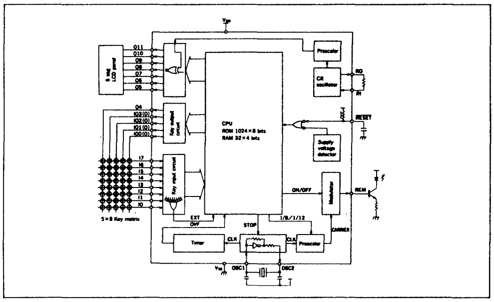




[Piggy-back package]

■EXAMPLE OF APPLICATIONS





■SUPPORT TOOLS

The following support tools are available to the SMC4054C, SMC4055C/M, SMC4056C/M for efficient programming and debugging.

- Cross assembler ·····Operates in the CP/M®
- Software simulator···Operates in the CP/M®
- Evaluation chip ······Piggy-back package allowing easy on-board debugging. Can also be used for debugging small-volume products.
  Used the CMOS type 27C32, or 27C64 EPROM.

■SMC4055C SERIES

Model	Number of I/O pins	Package
SMC4054C	5(O)×8(I)	20-pin DIP
SMC4055C/M	10(O)×10(I)	28-pin DIP, 28-pin SOP
SMC4056C/M	5(O)×8(I), 6(seg)×1(COM)	28-pin DIP, 28-pin SOP

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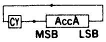
■INSTRUCTION SETS

Function	Mnemonic	Machine code								Status	Operation
		7	6	5	4	3	2	1	0		
ALU	ADC A, M	0	0	0	0	0	1	0	0	(NC)	AccA, CY ← AccA + M(X, Y) + CY
	ADD A, i	0	1	1	1	i3	i2	i1	i0	(NC)	AccA ← AccA + i
	ADD A, B	0	0	0	0	0	0	1	1	(NC)	AccA ← AccA + AccB
	ADD A, M	0	0	0	0	0	0	1	0	(NC)	AccA ← AccA + M(X, Y)
	AND A, B	0	0	0	1	0	0	1	1	(Z)	AccA ← AccA ∧ AccB
	AND A, M	0	0	0	1	0	0	1	0	(Z)	AccA ← AccA ∧ M(X, Y)
	AND S, M, j	0	1	0	0	1	1	j1	j0	(Z)	Mj(X, Y) ∧ 1
	INC M	0	0	0	1	0	0	0	1	(NC)	M(X, Y) ← M(X, Y) + 1
	INC Y	0	0	0	0	0	0	0	1	(NC)	Y ← Y + 1
	INC B	0	0	1	0	0	0	0	1	(NC)	B ← B + 1
	OR A, B	0	0	1	0	0	0	1	1	SET	AccA ← AccA ∨ AccB
	OR A, M	0	0	1	0	0	0	1	0	SET	AccA ← AccA ∨ M(X, Y)
	XOR S, A, B	0	0	0	0	0	1	0	1	(Z)	AccA $\veebar$ AccB
	XOR S, A, M	0	0	0	1	0	1	0	1	(Z)	AccA $\veebar$ M(X, Y)
ACC	CPL A	0	0	0	0	1	1	1	1	(Z)	AccA ← $\overline{\text{AccA}}$
	EX	0	0	0	1	1	0	0	0	SET	AccA ↔ AccB
	RRA	0	0	0	1	1	1	1	1	$\overline{\text{(CY)}}$	
LOAD	LD A, i	0	1	1	0	i3	i2	i1	i0	SET	AccA ← i
	LD A, M	0	0	0	1	1	0	0	1	SET	AccA ← M(X, Y)
	LD A, O	0	0	1	0	0	0	0	0	SET	AccA ← OUT(Y)
	LD A, Y	0	0	0	1	0	1	1	1	SET	AccA ← Y
	LD B, A	0	0	0	0	1	0	0	0	SET	AccB ← AccA
	LD M, A	0	0	0	0	1	0	0	1	SET	M(X, Y) ← AccA
	LD X, b	0	0	1	0	0	1	0	b	SET	X ← b
	LD Y, i	0	1	0	1	i3	i2	i1	i0	SET	Y ← i
	LD Y, A	0	0	0	0	0	1	1	1	SET	Y ← AccA
	SET CY	0	0	0	1	0	1	1	0	SET	CY ← 1
	RES CY	0	0	0	0	0	1	1	0	SET	CY ← 0
BIT	SET M, j	0	0	1	1	1	0	j1	j0	SET	Mj(X, Y) ← 1
	RES M, j	0	0	1	1	1	1	j1	j0	SET	Mj(X, Y) ← 0
I/O	IN A	0	0	0	0	1	0	1	0	SET	AccA ← IN(Y)
	IN M	0	0	0	1	1	0	1	0	SET	M(X, Y) ← IN(Y)
	OUT A	0	0	0	0	1	0	1	1	SET	OUT(Y) ← AccA
	OUT M	0	0	0	1	1	0	1	1	SET	OUT(Y) ← M(X, Y)
	SET O, j	0	0	1	1	0	0	j1	j0	SET	OUTj(Y) ← 1
	RES O, j	0	0	1	1	0	1	j1	j0	SET	OUTj(Y) ← 0

Function	Mnemonic	Machine code								Status	Operation
		7	6	5	4	3	2	1	0		
BRANCH	LD CA, b	0	0	1	0	1	0	0	b	SET	CB ← b
	LD PA, p	0	1	0	0	0	p2	p1	p0	SET	PB ← p
	JP S, s	1	1	s5	s4	s3	s2	s1	s0	SET	if S = 1 CA ← CB, PA ← PB SA ← s if S = 0 SA ← SA + 1
	JPA S, j	0	1	0	0	1	0	j1	j0	SET	if S = 1 CA ← CB, PA ← PB SA5,4 ← j SA3—0 ← AccA if S = 0 SA ← SA + 1
	CALL S, s	1	0	s5	s4	s3	s2	s1	s0	SET	if S = 1 CA_{STACK} ← CA PA_{STACK} ← PA SA_{STACK} ← SA + 1 CA ← CB, PA ← PB SA ← s, SP ← SP + 1 if S = 0 SA ← SA + 1
	RET	0	0	0	0	1	1	0	0	SET	SP ← SP—1 CA ← CB ← CA_{STACK} PA ← PB ← PA_{STACK} SA ← SA_{STACK}
	RETI	0	0	0	1	1	1	0	0	S STK	SP ← SP—1 CA ← CA_{STACK}, PA ← PA_{STACK} SA ← SA_{STACK}, CB ← CB_{STK} PB ← PB_{STK} AccA ← AccA_{STK} S ← S_{STK}, Y ← Y_{STK} X ← X_{STK}, CY ← CY_{STK}
SYSTEM	EI	0	0	0	0	1	1	0	1	SET	Interrupt enable
	DI	0	0	0	1	1	1	0	1	SET	Interrupt disable
	NOP	0	1	1	1	0	0	0	0	SET	No operation
	HALT	0	0	0	1	0	0	0	0	SET	SYSTEM Clock Stop Restart when interrupt occur
	STOP	0	0	0	0	1	1	1	0	SET	OSC Stop Restart when interrupt occur

SMC6110F Series

CMOS 4BIT SINGLE CHIP MICROCOMPUTER

- **ROM 1K WORD**
- **LCD driver confined**
- **Low power dissipation**

■DESCRIPTION

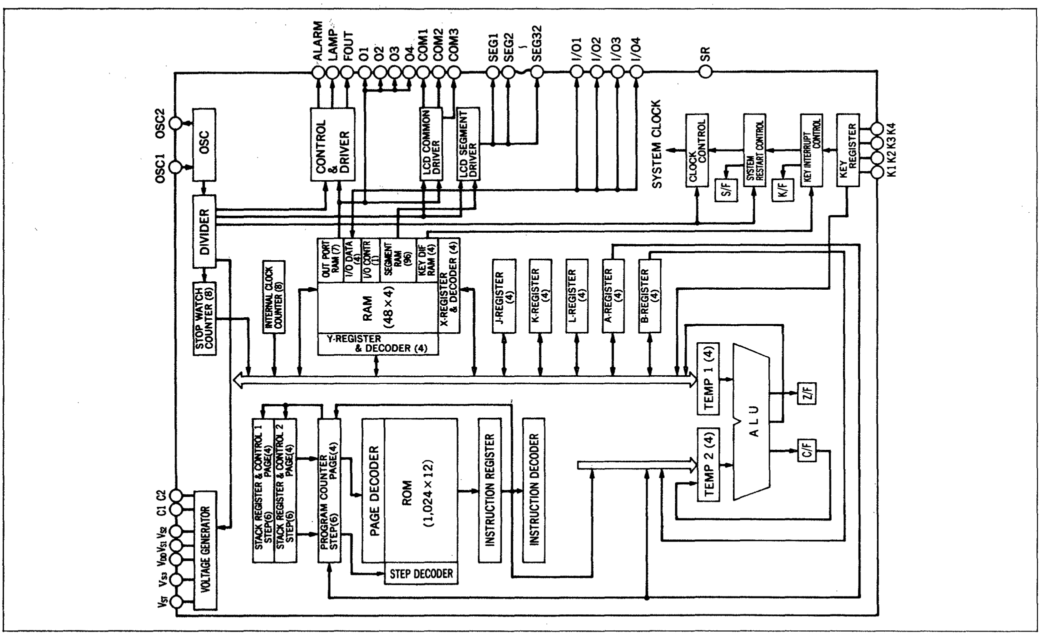
The SMC6110F series is a CMOS 4-bit single chip microcomputer. It incorporates a 1,024×12 bits ROM, a 48×4 bits RAM, a 96 segment LCD driver, restart with timer and key, and interrupt by key. The SMC6110F series applies to a variety of appliances with using LCD, low power dissipation; such as timepieces.

■FEATURES

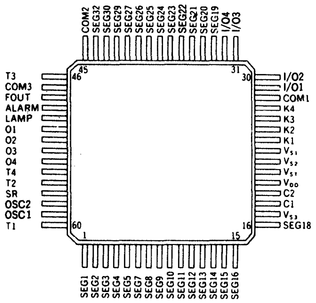
●CMOS LSI 4 bits parallel processing	
●Clock frequency (f_{OSC})	SMC6115F/6117F 32.768kHz
●Instruction cycle time	SMC6115F/6117F 122μs
●Instruction set	78 instructions
●ROM	1,024×12 bits
●RAM	48×4 bits
●Input port	4 bits*
●Output port	4 bits, 1 bit (for Alarm), 1 bit (for Lamp)
●I/O port	4 bits parallel processing*
●FOUT	Internal divided frequency output SMC6115F/6117F 512Hz to 32kHz
●Key input	16 keys available (I/O matrix method)
●LCD driver	Common: 3 terminals Segment: 32 terminals SMC6115F/6117F 1/2V-V-3/2V, 1/3 duty
●On-chip LCD segment memory	96 bits
●Timer	Chronograph counter Internal clock counter
●Subroutine nesting levels	2 levels
●Interrupt	Key input interrupt
●Programmed restart	Timer restart: SMC6115F/6117F 1 sec, 1/10 sec Key input restart
●LCD power supply circuit	Built-in: SMC6115F 1/2V halver, 3/2V booster SMC6117F Doubler, Tripler
●Supply voltage	SMC6115F 3.0V SMC6117F 1.5V
●Current consumption	SMC6115F 1.5μA (Typ) SMC6117F 3.0μA (Typ)
●Package	60-pin QFP/80-pin QFP

*pull-down resistor attachable

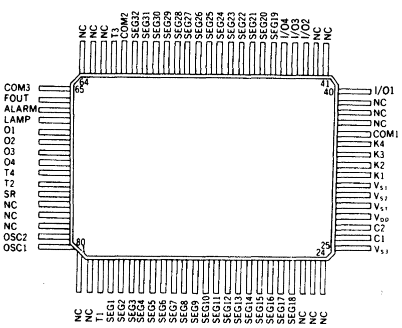
BLOCK DIAGRAM



PIN CONFIGURATION



60-pin QFP



80-pin QFP

PIN DESCRIPTION

V_{DD}	Supply voltage (0V)	K1 to K4	Input
V_{S1}	Supply voltage (−1.5V) Dropped voltage	O1 to O4	Output
V_{S2}	Supply voltage (−3.0V) Boosted voltage	COM1,COM2,COM3	LCD common driving output
V_{S3}	Boosted voltage (−4.5V)	SEG1 to SEG32	LCD segment driving output
V_{ST}	Stabilized voltage	ALARM	Alarm output
OSC1	Oscillation terminal (Input)	LAMP	Lamp output
OSC2	Oscillation terminal (Output)	FOUT	Internal divided frequency output (512Hz to 32kHz)
SR	System reset input	I/O1 to I/O4	Input/Output
C1, C2	Capacitor connection terminal for booster and regulator	TEST1 to TEST4	Test input

■ABSOLUTE MAXIMUM RATINGS

SMC6115F

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{S2}	−5.0 to 0.5	V
Input voltage	V_I	V_{S2}−0.3 to 0.5	V
Output voltage	V_O	V_{S2}−0.3 to 0.5	V
Operating temperature	T_{opr}	−20 to 80	℃
Storage temperature	T_{stg}	−65 to 150	℃
Soldering temperature and time	T_{sol}	260℃, 10s (at lead)	—

SMC6117F

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{S1}	−3.0 to 0.5	V
Input voltage	V_I	V_{S1}−0.3 to 0.5	V
Output voltage	V_O	V_{S1}−0.3 to 0.5	V
Operating temperature	T_{opr}	−20 to 80	℃
Storage temperature	T_{stg}	−65 to 150	℃
Soldering temperature and time	T_{sol}	260℃, 10s (at lead)	—

■RECOMMENDED OPERATING CONDITIONS

SMC6115F

(Ta = −20℃ to 80℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}	V_{DD}—V_{S2}	2.0	—	3.5	V
Oscillation frequency	f_{OSC}		—	32.768	—	kHz
Capacitor for booster	CE		0.047	—	—	μF
Capacitor for V_{DD}—V_{S1}	CA		0.047	—	—	μF
Capacitor for V_{DD}—V_{S3}	CC		0.047	—	—	μF
Capacitor for V_{DD}—V_{ST}	CD		0.047	—	—	μF

SMC6117F

(Ta = −20℃ to 80℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}	V_{DD}—V_{S1}	1.45	—	1.7	V
Oscillation frequency	f_{OSC}		—	32.768	—	kHz
Capacitor for booster	CE		0.047	—	—	μF
Capacitor for V_{DD}—V_{S2}	CB		0.047	—	—	μF
Capacitor for V_{DD}—V_{S3}	CC		0.047	—	—	μF

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

SMC6115F ($V_{S1}=-1.5V, V_{S2}=-3.0V, V_{S3}=-4.5V, f_{OSC}=32.768kHz$, CA=CC=CD=CE=0.047μF, Ta=25°C)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
High level input voltage	V_{IH1}		K1 to K4	−0.2	—	0	V
Low level input voltage	V_{IL1}		I/O1 to I/O4	V_{S2}	—	$V_{S2}+0.2$	V
High level input current	I_{IH1}	$V_{IH1}=0V$	K1 to K4,I/O1 to I/O4	—	—	0.5	μA
			K1 to K4,I/O1 to I/O4 with pull down resistor	2	—	10	μA
	I_{IH2}	$V_{IH2}=0V$	SR	5	—	25	μA
Low level input current	I_{IL}	$V_{IL}=-3.0V$	K1 to K4,I/O1 to I/O4	−0.5	—	—	μA
High level output current (1)	I_{OH1}	$V_{OH1}=-0.5V$	ALARM			−500	μA
Low level output current (1)	I_{OL1}	$V_{OL1}=-2.5V$	LAMP	500			μA
High level output current (2)	I_{OH2}	$V_{OH2}=-0.5V$	O1 to O4			−60	μA
Low level output current (2)	I_{OL2}	$V_{OL2}=-2.5V$		60			μA
High level output current (3)	I_{OH3}	$V_{OH3}=-0.5V$	FOUT			−60	μA
Low level output current (3)	I_{OL3}	$V_{OL3}=-2.5V$		60			μA
High level output current (4)	I_{OH4}	$V_{OH4}=-0.5V$	I/O port			−60	μA
Low level output current (4)	I_{OL4}	$V_{OL4}=-2.5V$		60			μA
Common output current	I_{OH5}	$V_{OH5}=-0.05V$	COM1, COM2, COM3			−3.0	μA
	I_{OL5}	$V_{OL5}=-2.95V$		3.0			μA
Segment output current	I_{OH6}	$V_{OH6}=-0.05V$	SEG1 to 32			−0.15	μA
	I_{OL6}	$V_{OL6}=-2.95V$		0.15			μA
Dropped output voltage	V_{S1}	1MΩ loading connected between V_{DD} and V_{S1}	V_{S1}			−1.45	V
Dropped ripple voltage	V_{rip1}					0.1	V
Boosted output voltage	V_{S3}	1MΩ loading connected between V_{DD} and V_{S3}				−4.2	V
Boosted ripple voltage	V_{rip3}					0.3	V
Current consumption	I_{S2}	No Load, Base Time Mode			0.40	0.70	μA
		No Load, Executing			1.50	2.50	
Operating voltage range	$V_{DD}-V_{S2}$	Normal		2.50	3.00	3.50	V
		Heavy Load		2.00	—	3.50	

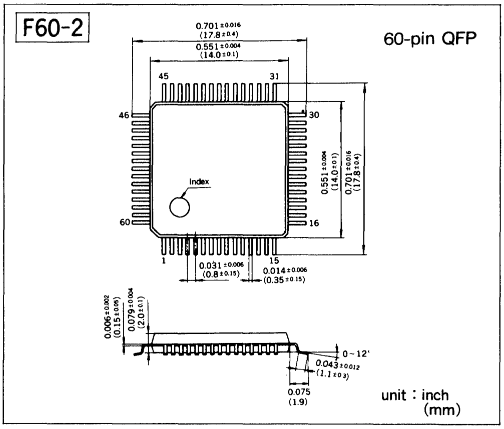
SMC6117F ($V_{S1}=-1.5V, V_{S2}=-3.0V, V_{S3}=-4.5V, f_{OSC}=32.768kHz$, CB=CC=CE=0.047μF, Ta=25°C)

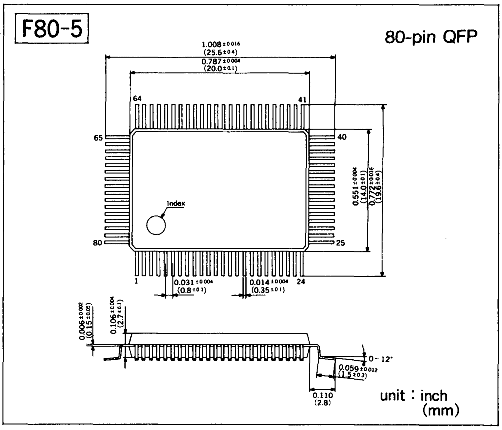
Parameter	Symbol	Conditions		Min	Typ	Max	Unit
High level input voltage	V_{IH1}		K1 to K4	−0.2		0	V
Low level input voltage	V_{IL1}		I/O1 to I/O4	V_{S1}		$V_{S1}+0.2$	V
High level input current	I_{IH1}	$V_{IH1}=0V$	K1 to K4,I/O1 to I/O4	—	—	0.5	μA
			K1 to K4,I/O1 to I/O4 with pull down resistor	2	—	10	μA
	I_{IH2}	$V_{IH2}=0V$	SR	5	—	25	μA
Low level input current	I_{IL}	$V_{IL}=-1.5V$	K1 to K4,I/O1 to I/O4	−0.5			μA
High level output current (1)	I_{OH1}	$V_{OH1}=-0.5V$	ALARM			−250	μA
Low level output current (1)	I_{OL1}	$V_{OL1}=-1.0V$	LAMP	250			μA
High level output current (2)	I_{OH2}	$V_{OH2}=-0.5V$	O1 to O4			−30	μA
Low level output current (2)	I_{OL2}	$V_{OL2}=-1.0V$		30			μA
High level output current (3)	I_{OH3}	$V_{OH3}=-0.5V$	FOUT			−30	μA
Low level output current (3)	I_{OL3}	$V_{OL3}=-1.0V$		30			μA
High level output current (4)	I_{OH4}	$V_{OH4}=-0.5V$	I/O port			−30	μA
Low level output current (4)	I_{OL4}	$V_{OL4}=-1.0V$		30			μA
Common output current	I_{OH5}	$V_{OH5}=-0.05V$	COM1, COM2, COM3			−3.0	μA
	I_{OL5}	$V_{OL5}=-1.45V$		3.0			μA

SMC6117 (continued)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Segment output current	I_{OH6}	$V_{OH6} = -0.05V$	SEG1 to 32			-0.15	μA
	I_{OL6}	$V_{OL6} = -1.45V$		0.15			μA
Boosted output voltage	V_{S2}	1MΩ loading connected between V_{DD} and V_{S2}	V_{S2}			-2.90	V
Boosted ripple voltage	V_{rip2}					0.1	V
Boosted output voltage	V_{S3}	1MΩ loading connected between V_{DD} and V_{S3}				-4.1	V
Boosted ripple voltage	V_{rip3}					0.3	V
Current consumption	I_{S1}	No Load, Base Time Mode			0.80	1.40	μA
		No Load, Executing			3.0	5.0	
Operating voltage range	$V_{DD}-V_{S1}$			1.35	1.50	1.70	V

■PACKAGE DIMENSIONS

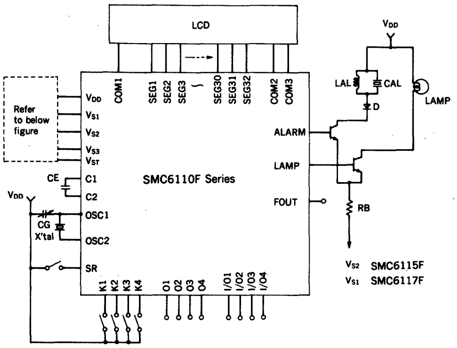


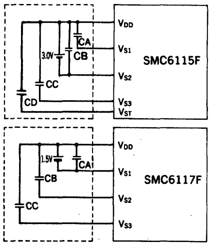


■SMC6110F SERIES

Type No.	Power Supply	Instruction Cycle	Package
SMC6115F	3.0V Li battery	122μs	60-pin QFP
SMC6117F	1.5V Ag battery	122μs	80-pin QFP

■EXAMPLE OF APPLICATION





CA : Capacitor between V_{DD} pin and V_{S1} pin CA≧0.047μF
CB : Capacitor between V_{DD} pin and V_{S2} pin CB≧0.047μF
CC : Capacitor between V_{DD} pin and V_{S3} pin CG=5 to 25pF
CD : Capacitor between V_{DD} pin and V_{ST} pin CD≧0.1μF
CE : Capasitor for booster
CG : Capacitor for trimmer
X'tal : Crystal Oscillator
RB : 150Ω
CAL : Piezoelectric buzzer
LAL : Booster coil for buzzer
D : Reverse current prevention diode

■INSTRUCTION SET

Function	Mnemonic	Machine Code												Flag				Operation
		B	A	9	8	7	6	5	4	3	2	1	0	C	Z	K	S	
System	NOP	1	1	1	1	1	1	1	1	1	1	1	1					No Operation
	HLT b	1	1	1	1	1	1	1	0	1	1	1	b					Clock stop b=0 : 1s Restart b=1 : 1/10s Restart
	EI	1	1	1	1	1	1	0	1	1	1	1	1					Enable Key Interrupt
	DI	1	1	1	1	1	1	0	1	1	1	1	0					Disable Key Interrupt
	RESW	1	1	1	1	1	1	0	0	1	1	1	1					Reset Stop Watch Counter
	CFC b	1	1	1	1	1	0	1	1	1	1	1	b	↕				Carry Flag Control b=0 reset : b=1 set
	ZFC b	1	1	1	1	1	0	1	0	1	1	1	b		↕			Zero Flag Control b=0 reset : b=1 set
ALU	ADD A, i	1	1	1	1	0	0	0	0	i3	i2	i1	i0	↕	↕			A←A+i
	ADC A, i	1	1	1	1	0	0	0	1	i3	i2	i1	i0	↕	↕			A←A+i+C
	AND A, i	1	1	1	1	0	0	1	0	i3	i2	i1	i0		↕			A←A∧i
	OR A, i	1	1	1	1	0	0	1	1	i3	i2	i1	i0		↕			A←A∨i
	ADD B, i	1	1	1	1	0	1	0	0	i3	i2	i1	i0	↕	↕			B←B+i
	ADC B, i	1	1	1	1	0	1	0	1	i3	i2	i1	i0	↕	↕			B←B+i+C
	AND B, i	1	1	1	1	0	1	1	0	i3	i2	i1	i0		↕			B←B∧i
	OR B, i	1	1	1	1	0	1	1	1	i3	i2	i1	i0		↕			B←B∨i
	CP r, i	1	1	1	0	0	r2	r1	r0	i3	i2	i1	i0	↕	↕			r−i
	FAN r, i	1	1	1	0	1	r2	r1	r0	i3	i2	i1	i0		↕			r∧i
	ADD r, A	1	0	0	1	0	r2	r1	r0	0	0	0	0	↕	↕			r←r+A
	ADC r, A	1	0	0	1	0	r2	r1	r0	0	0	0	1	↕	↕			r←r+A+C

INSTRUCTION SET (continued)

Function	Mnemonic	Machine Code												Flag				Operation
		B	A	9	8	7	6	5	4	3	2	1	0	C	Z	K	S	
ALU	SUB r, A	1	0	0	1	0	r2	r1	r0	0	0	1	0	↕	↕			r←r−A
	SBC r, A	1	0	0	1	0	r2	r1	r0	0	0	1	1	↕	↕			r←r−A−C
	AND r, A	1	0	0	1	0	r2	r1	r0	0	1	0	0		↕			r←r∧A
	OR r, A	1	0	0	1	0	r2	r1	r0	0	1	0	1		↕			r←r∨A
	CP r, A	1	0	0	1	0	r2	r1	r0	0	1	1	0	↕	↕			r−A
	FAN r, A	1	0	0	1	0	r2	r1	r0	0	1	1	1		↕			r∧A
	ADD r, B	1	0	0	1	0	r2	r1	r0	1	0	0	0	↕	↕			r←r+B
	ADC r, B	1	0	0	1	0	r2	r1	r0	1	0	0	1	↕	↕			r←r+B+C
	SUB r, B	1	0	0	1	0	r2	r1	r0	1	0	1	0	↕	↕			r←r−B
	SBC r, B	1	0	0	1	0	r2	r1	r0	1	0	1	1	↕	↕			r←r−B−C
	AND r, B	1	0	0	1	0	r2	r1	r0	1	1	0	0		↕			r←r∧B
	OR r, B	1	0	0	1	0	r2	r1	r0	1	1	0	1		↕			r←r∨B
	CP r, B	1	0	0	1	0	r2	r1	r0	1	1	1	0	↕	↕			r−B
	FAN r, B	1	0	0	1	0	r2	r1	r0	1	1	1	1		↕			r∧B
	ADD A, r	1	0	1	0	0	r2	r1	r0	0	0	0	0	↕	↕			A←r+A
	ADC A, r	1	0	1	0	0	r2	r1	r0	0	0	0	1	↕	↕			A←r+A+C
	SUBR A, r	1	0	1	0	0	r2	r1	r0	0	0	1	0	↕	↕			A←r−A
	SBCR A, r	1	0	1	0	0	r2	r1	r0	0	0	1	1	↕	↕			A←r−A−C
	AND A, r	1	0	1	0	0	r2	r1	r0	0	1	0	0		↕			A←r∧A
	OR A, r	1	0	1	0	0	r2	r1	r0	0	1	0	1		↕			A←r∨A
	ADD B, r	1	0	1	0	0	r2	r1	r0	1	0	0	0	↕	↕			B←r+B
	ADC B, r	1	0	1	0	0	r2	r1	r0	1	0	0	1	↕	↕			B←r+B+C
	SUBR B, r	1	0	1	0	0	r2	r1	r0	1	0	1	0	↕	↕			B←r−B
	SBCR B, r	1	0	1	0	0	r2	r1	r0	1	0	1	1	↕	↕			B←r−B−C
	AND B, r	1	0	1	0	0	r2	r1	r0	1	1	0	0		↕			B←r∧B
	OR B, r	1	0	1	0	0	r2	r1	r0	1	1	0	1		↕			B←r∨B
	ADDP r, A	1	0	0	1	1	r2	r1	r0	0	0	0	0	↕	↕			r←r+A Y←Y+1
	ADCP r, A	1	0	0	1	1	r2	r1	r0	0	0	0	1	↕	↕			r←r+A+C Y←Y+1
	SUBP r, A	1	0	0	1	1	r2	r1	r0	0	0	1	0	↕	↕			r←r−A Y←Y+1
	SBCP r, A	1	0	0	1	1	r2	r1	r0	0	0	1	1	↕	↕			r←r−A−C Y←Y+1
	ANDP r, A	1	0	0	1	1	r2	r1	r0	0	1	0	0		↕			r←r∧A Y←Y+1
	ORP r, A	1	0	0	1	1	r2	r1	r0	0	1	0	1		↕			r←r∨A Y←Y+1
	ADDP r, B	1	0	0	1	1	r2	r1	r0	1	0	0	0	↕	↕			r←r+B Y←Y+1
	ADCP r, B	1	0	0	1	1	r2	r1	r0	1	0	0	1	↕	↕			r←r+B+C Y←Y+1
	SUBP r, B	1	0	0	1	1	r2	r1	r0	1	0	1	0	↕	↕			r←r−B Y←Y+1
	SBCP r, B	1	0	0	1	1	r2	r1	r0	1	0	1	1	↕	↕			r←r−B−C Y←Y+1
	ANDP r, B	1	0	0	1	1	r2	r1	r0	1	1	0	0		↕			r←r∧B Y←Y+1
	ORP r, B	1	0	0	1	1	r2	r1	r0	1	1	0	1		↕			r←r∨B Y←Y+1

INSTRUCTION SET (continued)

Function	Mnemonic	Machine Code												Flag				Operation
		B	A	9	8	7	6	5	4	3	2	1	0	C	Z	K	S	
LOAD	LD r , i	1	1	0	0	0	r2	r1	r0	i3	i2	i1	i0					r←i
	LDXY x , y	1	1	0	1	x3	x2	x1	x0	y3	y2	y1	y0					X←x, Y←y
	LDP M, i	1	1	1	1	1	0	0	1	i3	i2	i1	i0					M(X, Y)←i Y←Y+1
	LD r , r′	1	0	0	0	0	r2	r1	r0	0	r′2	r′1	r′0					r←r′
	LDP r , r′	1	0	0	0	0	r2	r1	r0	1	r′2	r′1	r′0					r←r′, Y←Y+1
	LD r, SW0	1	0	0	0	1	r2	r1	r0	0	1	0	0					r←SW0
	LD r, SW1	1	0	0	0	1	r2	r1	r0	0	1	0	1					r←SW1
IN	IN r	1	0	0	0	1	r2	r1	r0	0	1	1	1					r←IN
Branch	CALL ps	0	1	p3	p2	p1	p0	s5	s4	s3	s2	s1	s0					Subroutine Call PCS+1→PCS, $\overline{SP}$→SP, then [SP=0 : PCP→STP1, PCS→STS1] [SP=1 : PCP→STP2, PCS→STS2] then p→PCP, s→PCS
	RET	1	1	0	0	1	1	0	0	1	1	1	1					Return [SP=0 : STP1→PCP, STS1→PCS] [SP=1 : STP2→PCP, STS2→PCS] then, $\overline{SP}$→SP
	RET LM, i	1	1	0	0	1	1	0	1	i3	i2	i1	i0					M(X, Y)←i, then, Return
	RET AM, i	1	1	0	0	1	1	1	0	i3	i2	i1	i0		↕			M(X, Y)←M(X, Y)∧i then, Return
	RET OM, i	1	1	0	0	1	1	1	1	i3	i2	i1	i0		↕			M(X, Y)←M(X, Y)∨i then, Return
	JP ps	0	0	p3	p2	p1	p0	s5	s4	s3	s2	s1	s0					Jump p→PCP, s→PCS
	JP C , s	1	0	1	1	0	0	s5	s4	s3	s2	s1	s0					Jump Condition IF C=1 s→PCS
	JP NC, s	1	0	1	1	0	1	s5	s4	s3	s2	s1	s0					Jump Condition IF C=0 s→PCS
	JP Z , s	1	0	1	1	1	0	s5	s4	s3	s2	s1	s0					Jump Condition IF Z=1 s→PCS
	JP NZ, s	1	0	1	1	1	1	s5	s4	s3	s2	s1	s0					Jump Condition IF Z=0 s→PCS
	JP K , s	1	0	1	0	1	0	s5	s4	s3	s2	s1	s0			↓		Jump Condition IF K=1 s→PCS Reset K
	JP S , s	1	0	1	0	1	1	s5	s4	s3	s2	s1	s0				↓	Jump Condition IF S=1 s→PCS Reset S
	JP A , j	1	1	0	0	1	0	j5	j4	1	1	1	1					Jump Indirect by A PCS5, 4←j5, 4 PCS3to0←A

NOTE : 1 r and r′ correspond to register A, B, J, K, L, X, Y, and M (X, Y). The following table shows the relationship between code and register.

Register	CODE			Register	CODE			Register	CODE		
	r2	r1	r0		r2	r1	r		r2	r1	r0
A	0	0	0	K	0	1	1	Y	1	1	0
B	0	0	1	L	1	0	0	M (X, Y)	1	1	1
J	0	1	0	X	1	0	1				

2 i refers to 4 bits Immediate Data. Co refers to 1 bit Immediate Data. P refers to 4 bits Immediate Data. S refers to 6 bits Immediate Data.

3 PCP : Program Counter Page. PCS : Program Counter Step. STP : Stack Page. STS : Stack Step. SW : Stop Watch Counter. C : Carry Flag. Z : Zero Flag. K : Key Flag. S : Second Flag.

PF362-01

SMC6214F

CMOS 4 BIT SINGLE CHIP MICROCOMPUTER

- Core CPU Architecture
- 32 KHz/455 KHz Twin Clock Operation
- Built-in BLD and Analog Comparator
- Built-in Watchdog Timer

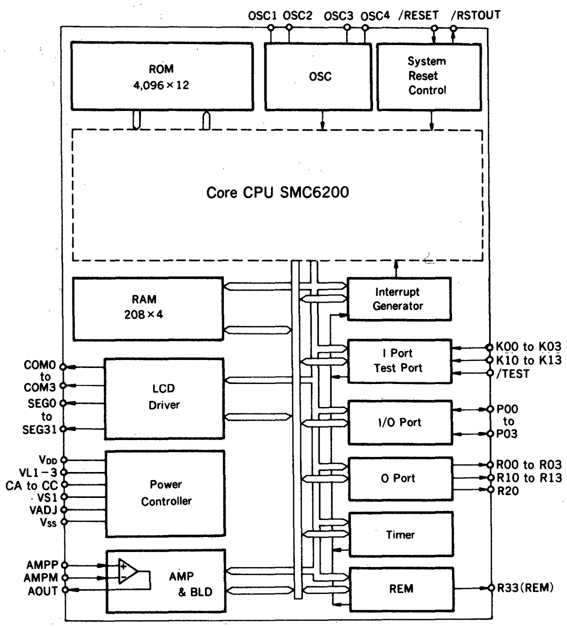
■DESCRIPTION

The SMC6214F is a CMOS 4-bit microcomputer using an SMC6200 as its core processors. It contains ROM, RAM, an LCD driver circuit, remote-control carrier output circuit, time base counter, analog comparator, watchdog timer, and other functions on a single chip. The SMC6214F provides an excellent solution for low-power system applications such as an infrared remote controller with a clock function.

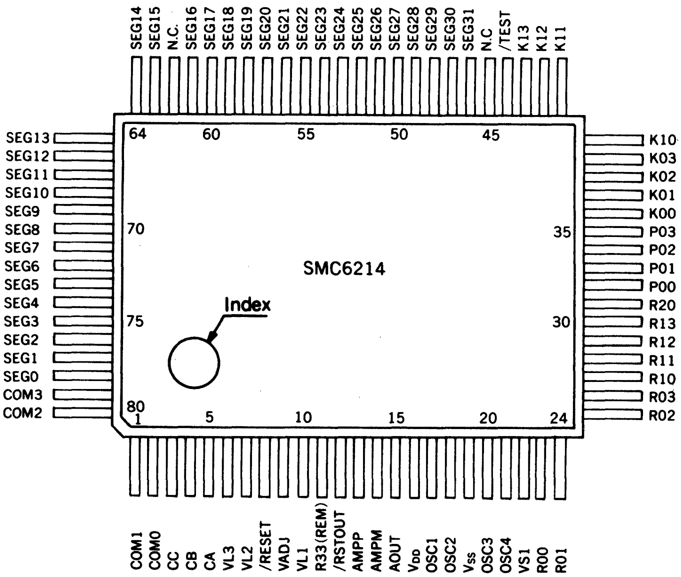
■FEATURES

●CMOS LSI 4-bit parallel processing	
●Clocks	32.768 kHz (typ.) or 455 kHz (typ.), selectable by software
●Instruction set	100 instructions
●Instruction cycle time	32kHz clock mode : 153 μsec, 214 μsec or 366 μsec 455kHz clock mode : 11 μsec, 15 μsec or 26 μsec
●ROM size	4,096×12 bits
●RAM size	208×4 bits
●Input port	8 bits (pull-up resistors available by using a mask option)
●Output port	9 bits (clock, buzzer output available by using a mask option)
●I/O port	4 bits
●REM output	1 bit (hardware timer or software timer selectable by software)
●LCD driver	32 segments×3 commons or 32 segments×4 commons (1/3 or 1/4 duty selectable by using a mask option)
●Built-in LCD power supplies	Voltage regulator, voltage doubler, and voltage tripler
●Built-in BLD circuit	2.3V (battery life detecter)
●Built-in amplifier	Operational amplifier for MOS input analog comparator
●Built-in watchdog timer	
●Interrupts	External : two input interrupts Internal : three timer interrupts (32Hz, 8Hz, 2Hz) one REM interrupt
●Supply voltage	3V (2.2 to 3.5V)
●Current dissipation	32kHz clock mode : 5μA (typ.) (basic clock mode) 455kHz clock mode : 300μA (typ.)
●Package	80-pin QFP (plastic) also available in chip form

BLOCK DIAGRAM



PIN CONFIGURATION



■PIN DESCRIPTION

Pin name	Functions
V_{DD}	Power supply (+)
V_{SS}	Power supply (−)
V_{S1}	Power supply for oscillator (generated internally)
V_{L1}	Power supply for LCD driver (generated internally)
V_{L2}	Power supply for LCD driver (doubled V_{L1})
V_{L3}	Power supply for LCD driver (tripled V_{L1})
CA to CC	Capacitor connection pins for LCD booster
VADJ	VL adjusting input pin
OSC1	Crystal oscillation input pin
OSC2	Crystal oscillation output pin (containing CD)
OSC3	Ceramic or CR oscillation input pin (selectable by using mask option)
OSC4	Ceramic or CR oscillation output pin (selectable by using mask option)
COM0 to 3	LCD common output (1/3 or 1/4 duty selectable by using mask option)
SEG0 to 31	LCD segment output (DC output available by using mask option)

Pin name	Functions
AMPP	Analog comparator non-reverse input pin
AMPM	Analog comparator reverse input pin
AOUT	Analog comparator output pin
/TEST	Test input pin
/RESET	System reset input pin
K00 to 03	Input ports
K10 to 13	Input ports
P00 to 03	Input/Output ports
R00 to 03	Output ports (R12: selectable for DC output, FOUT output or/BZ output by using mask option) (R13: selectable for DC output or BZ output by using mask option)
R10 to 13	
R20	
R33 (REM)	Remote-control output pin
/RSTOUT	System reset output pin

■ABSOLUTE MAXIMUM RATINGS

(V_{DD}=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{SS}	−5.2 to 0.5	V
Input voltage	V_I	V_{SS}−0.3 to 0.3	V
	V_{IOSC}	V_{S1}−0.3 to 0.3	V
Operating temperature	T_{opr}	−20 to 60	°C
Storage temperature	T_{stg}	−65 to 150	°C
Soldering temperature and time	T_{sol}	260°C, 10s (at leads)	—
Power dissipation	P_D	250	mW

■RECOMMENDED OPERATING CONDITIONS

(Ta=−20°C to 60°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{SS}	V_{DD}=0V	−3.5	−3.0	−2.2	V
Oscillation frequency	f_{OSC1}		—	32.768	—	kHz
	f_{OSC3}	duty : 50±5%	50	455	500	kHz
Power supply voltage for LCD driver	V_{L1}		−1.6	−1.05	—	V

■ELECTRICAL CHARACTERISTICS

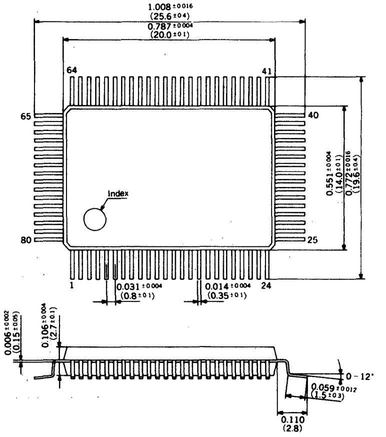
($V_{DD}=0V$, $V_{SS}=-2.2$ to $-3.5V$, $V_{L3}=-3.0V$, Ta$=-20$ to 60°C)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
High-level input voltage (1)	V_{IH1}		K00 to K13 P00 to P03	$0.2V_{SS}$	—	0	V
Low-level input voltage (1)	V_{IL1}			V_{SS}	—	$0.8V_{SS}$	V
High-level input current (2)	V_{IH2}		/RESET	$0.1V_{SS}$	—	0	V
Low-level input voltage (2)	V_{IL2}			V_{SS}	—	$0.9V_{SS}$	V
Low-level input current	I_{IL1}	$V_{IL1}=V_{SS}$,Without pull-up resistor	K00 to K13	-1	—	—	µA
	I_{IL2}	$V_{IL2}=V_{SS}$, With pull-up resistor	K00 to K13 /RESET	-5	—	-0.35	µA
	I_{IL3}	$V_{IL3}=0.2V_{SS}$		-30	—	-5	µA
	I_{IL4}	$V_{IL4}=V_{SS}$	P00 to 03 (at read mode with a built-in program)	-15	—	-2	µA
High-level input current	I_{IH1}	$V_{IH1}=0V$		—	—	1	µA
High-level output current (1)	I_{OH1}	$V_{OH1}=0.1V_{SS}$	R00 to R03 R10 to R13 /RSTOUT	—	—	-250	µA
Low-level output current (1)	I_{OL1}	$V_{OL1}=0.9V_{SS}$		1.0	—	—	mA
High-level output current (2)	I_{OH2}	$V_{OH2}=0.1V_{SS}$	R20	—	—	-1.8	mA
Low level output current (2)	I_{OL2}	$V_{OL2}=0.9V_{SS}$		1.0	—	—	mA
High-level output current (3)	I_{OH3}	$V_{OH3}=0.1V_{SS}$	P00 to P03	—	—	-100	µA
Low-level output current (3)	I_{OL3}	$V_{OL3}=0.9V_{SS}$		140	—	—	µA
High level output current (4)	I_{OH4}	$V_{OH4}=0.5V_{SS}$	R33 (REM)	—	—	-1.0	mA
Low-level output current (4)	I_{OL4}	$V_{OL4}=0.9V_{SS}$		1.0	—	—	mA
Common output current	I_{OH5}	$V_{OH5}=-0.05V$	COM0 to 3 $V_{SS}=-3.0V$	—	—	-3.0	µA
	I_{OL5}	$V_{OL5}=-2.95V$		3.0	—	—	µA
Segment output current	I_{OH6}	$V_{OH6}=-0.05V$	SEG0 to 31 $V_{SS}=-3.0V$	—	—	-3.0	µA
	I_{OL6}	$V_{OL6}=-2.95V$		3.0	—	—	µA
Internal voltages	V_{L1}	$V_{ADJ}=V_{L1}$, $I_{L1}=5\mu A$ with 1MΩ loads between V_{DD} and V_{L2} and between V_{DD} and V_{L3}		-1.13	-1.05	-0.98	V
	V_{L2}			$2 \cdot V_{L1}$	$2V_{L1}$	$2 \cdot V_{L1}+0.1$	V
	V_{L3}			$3 \cdot V_{L1}$	$3V_{L1}$	$3 \cdot V_{L1}+0.3$	V
BLD voltage	V_{BLD}	Ta=25°C		-2.4	-2.3	-2.2	V
Current dissipation	I_{opr}	At halt	OSCC=0, Ta=25°C $V_{ADJ}=V_{L1}$ No panel load	—	3	8	µA
		In Basic clock mode*		—	5	12	µA
		In 455KHz clock mode	$V_{ADJ}=V_{L1}$ No panel load Ta=25°C	—	300	450	µA

*Basic clock mode: duty cycle 10%

■PACKAGE DIMENSIONS

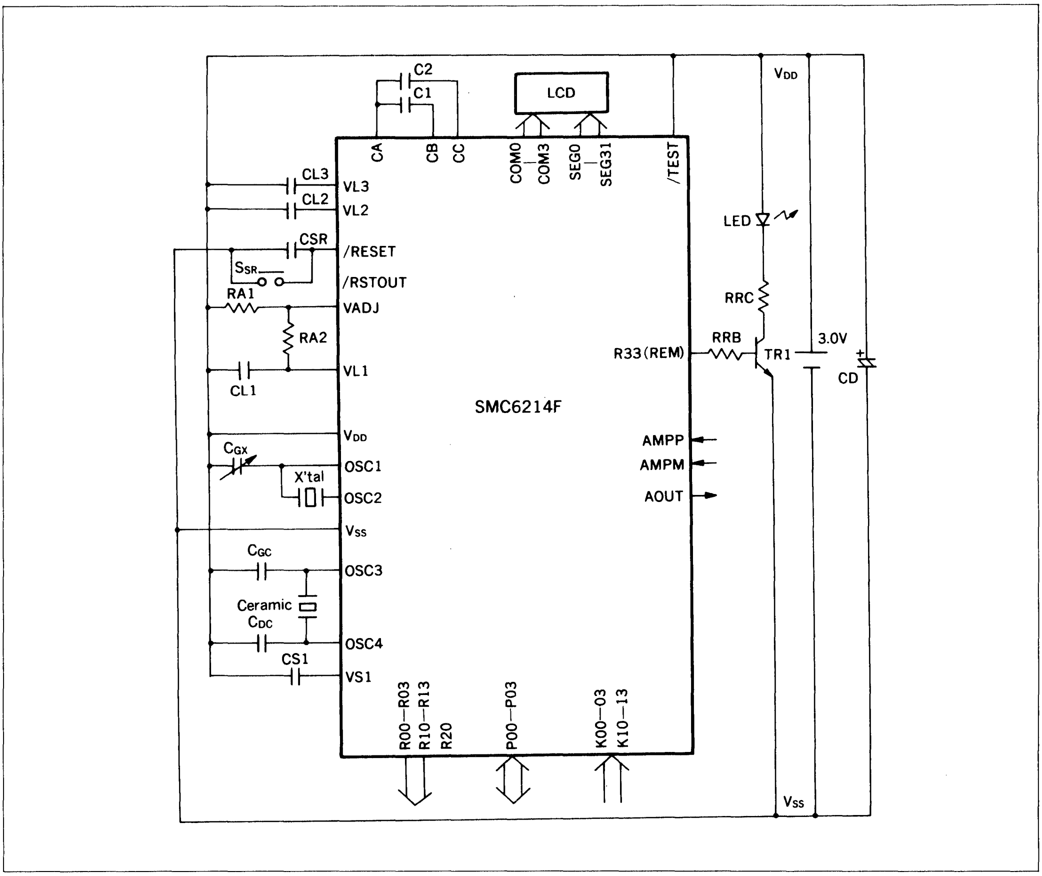
F80-5



80-pin QFP

unit : inch
(mm)

EXAMPLE OF APPLICATION



INSTRUCTION SET

Group	Mnemonic	Operand	OP code												Flag				Clock	Operation
			B	A	9	8	7	6	5	4	3	2	1	0	I	D	Z	C		
Branch	PSET	P	1	1	1	0	0	1	0	p4	p3	p2	p1	p0					5	NPB←p4, NPP←p3~0
	JP	s	0	0	0	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB←NPB, PCP←NPP, PCS←s7~0
		C, s	0	0	1	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB←NPB, PCP←NPP, PCS←s7~0 if C=1
		NC, s	0	0	1	1	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB←NPB, PCP←NPP, PCS←s7~0 if C=0
		Z, s	0	1	1	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB←NPB, PCP←NPP, PCS←s7~0 if Z=1
		NZ, s	0	1	1	1	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB←NPB, PCP←NPP, PCS←s7~0 if Z=0
	JPBA		1	1	1	1	1	1	1	0	1	0	0	0					5	PCB←NPB, PCP←NPP, PCSH←B, PCSL←A
	CALL	s	0	1	0	0	s7	s6	s5	s4	s3	s2	s1	s0					7	M(SP-1)←PCP, M(SP-2)←PCSH, M(SP-3)←PCSL+1 SP←SP-3, PCP←NPP, PCS←s7~0
	CALZ	s	0	1	0	1	s7	s6	s5	s4	s3	s2	s1	s0					7	M(SP-1)←PCP, M(SP-2)←PCSH, M(SP-3)←PCSL+1 SP←SP-3, PCP←0, PCS←s7~0
	RET		1	1	1	1	1	1	0	1	1	1	1	1					7	PCSL←M(SP), PCSH←M(SP+1), PCP←M(SP+2), SP←SP+3
	RETS		1	1	1	1	1	1	0	1	1	1	1	0					12	PCSL←M(SP), PCSH←M(SP+1), PCP←M(SP+2), SP←SP+3 PC←PC+1
	RETD	l	0	0	0	1	l7	l6	l5	l4	l3	l2	l1	l0					12	PCSL←M(SP), PCSH←M(SP+1), PCP←M(SP+2), SP←SP+3 M(X)←l3~0, M(X+1)←l7~4, X←X+2
System Control	NOP5		1	1	1	1	1	1	1	1	1	0	1	1					5	No Operation (5 clocks)
	NOP7		1	1	1	1	1	1	1	1	1	1	1	1					7	No Operation (7 clocks)
	HALT		1	1	1	1	1	1	1	1	1	0	0	0					5	Halt (stop clock)
Flag Operation	SET	F, i	1	1	1	1	0	1	0	0	i3	i2	i1	i0	↑	↑	↑	↑	7	F←F∨i3~0
	RST	F, i	1	1	1	1	0	1	0	1	i3	i2	i1	i0	↓	↓	↓	↓	7	F←F∧i3~0
	SCF		1	1	1	1	0	1	0	0	0	0	0	1				↑	7	C←1
	RCF		1	1	1	1	0	1	0	1	1	1	1	0				↓	7	C←0
	SZF		1	1	1	1	0	1	0	0	0	0	1	0			↑		7	Z←1
	RZF		1	1	1	1	0	1	0	1	1	1	0	1			↓		7	Z←0
	SDF		1	1	1	1	0	1	0	0	0	1	0	0		↑			7	D←1 (Decimal Adjust ON)
	RDF		1	1	1	1	0	1	0	1	1	0	1	1		↓			7	D←0 (Decimal Adjust OFF)
	EI		1	1	1	1	0	1	0	0	1	0	0	0	↑				7	I←1 (Enable Interrupt)
	DI		1	1	1	1	0	1	0	1	0	1	1	1	↓				7	I←0 (Disable Interrupt)

Group	Mnemonic	Operand	OP code												Flag				Clock	Operation
			B	A	9	8	7	6	5	4	3	2	1	0	I	D	Z	C		
Stack Operation	INC	SP	1	1	1	1	1	1	0	1	1	0	1	1					5	SP←SP+1
	DEC	SP	1	1	1	1	1	1	0	0	1	0	1	1					5	SP←SP−1
	PUSH	r	1	1	1	1	1	1	0	0	0	0	r1	r0					5	M(SP−1)←r, SP←SP−1
		XH	1	1	1	1	1	1	0	0	0	1	0	1					5	M(SP−1)←XH, SP←SP−1
		XL	1	1	1	1	1	1	0	0	0	1	1	0					5	M(SP−1)←XL, SP←SP−1
		YH	1	1	1	1	1	1	0	0	1	0	0	0					5	M(SP−1)←YH, SP←SP−1
		YL	1	1	1	1	1	1	0	0	1	0	0	1					5	M(SP−1)←YL, SP←SP−1
		F	1	1	1	1	1	1	0	0	1	0	1	0					5	M(SP−1)←F, SP←SP−1
	POP	r	1	1	1	1	1	1	0	1	0	0	r1	r0					5	r←M(SP), SP←SP+1
		XH	1	1	1	1	1	1	0	1	0	1	0	1					5	XH←M(SP), SP←SP+1
		XL	1	1	1	1	1	1	0	1	0	1	1	0					5	XL←M(SP), SP←SP+1
		YH	1	1	1	1	1	1	0	1	1	0	0	0					5	YH←M(SP), SP←SP+1
		YL	1	1	1	1	1	1	0	1	1	0	0	1					5	YL←M(SP), SP←SP+1
		F	1	1	1	1	1	1	0	1	1	0	1	0	↕	↕	↕	↕	5	F←M(SP), SP←SP+1
	LD	SPH, r	1	1	1	1	1	1	1	0	0	0	r1	r0					5	SPH←r
		SPL, r	1	1	1	1	1	1	1	1	0	0	r1	r0					5	SPL←r
		r, SPH	1	1	1	1	1	1	1	0	0	1	r1	r0					5	r←SPH
		r, SPL	1	1	1	1	1	1	1	1	0	1	r1	r0					5	r←SPL
Index Operation	INC	X	1	1	1	0	1	1	1	0	0	0	0	0					5	X←X+1
		Y	1	1	1	0	1	1	1	1	0	0	0	0					5	Y←Y+1
	LD	X, x	1	0	1	1	x7	x6	x5	x4	x3	x2	x1	x0					5	XH←x7~4, XL←x3~0
		Y, y	1	0	0	0	y7	y6	y5	y4	y3	y2	y1	y0					5	YH←y7~4, YL←y3~0
		XH, r	1	1	1	0	1	0	0	0	0	1	r1	r0					5	XH←r
		XL, r	1	1	1	0	1	0	0	0	1	0	r1	r0					5	XL←r
		YH, r	1	1	1	0	1	0	0	1	0	1	r1	r0					5	YH←r
		YL, r	1	1	1	0	1	0	0	1	1	0	r1	r0					5	YL←r
		r, XH	1	1	1	0	1	0	1	0	0	1	r1	r0					5	r←XH
		r, XL	1	1	1	0	1	0	1	0	1	0	r1	r0					5	r←XL
		r, YH	1	1	1	0	1	0	1	1	0	1	r1	r0					5	r←YH
		r, YL	1	1	1	0	1	0	1	1	1	0	r1	r0					5	r←YL
	ADC	XH, i	1	0	1	0	0	0	0	0	i3	i2	i1	i0			↕	↕	7	XH←XH+i3~0+C
		XL, i	1	0	1	0	0	0	0	1	i3	i2	i1	i0			↕	↕	7	XL←XL+i3~0+C
		YH, i	1	0	1	0	0	0	1	0	i3	i2	i1	i0			↕	↕	7	YH←YH+i3~0+C
		YL, i	1	0	1	0	0	0	1	1	i3	i2	i1	i0			↕	↕	7	YL←YL+i3~0+C
	CP	XH, i	1	0	1	0	0	1	0	0	i3	i2	i1	i0			↕	↕	7	XH−i3~0
		XL, i	1	0	1	0	0	1	0	1	i3	i2	i1	i0			↕	↕	7	XL−i3~0
		YH, i	1	0	1	0	0	1	1	0	i3	i2	i1	i0			↕	↕	7	YH−i3~0
		YL, i	1	0	1	0	0	1	1	1	i3	i2	i1	i0			↕	↕	7	YL−i3~0
Data Transfer	LD	r, i	1	1	1	0	0	0	r1	r0	i3	i2	i1	i0					5	r←i3~0
		r, q	1	1	1	0	1	1	0	0	r1	r0	q1	q0					5	r←q
		A, Mn	1	1	1	1	1	0	1	0	n3	n2	n1	n0					5	A←M(n3~0)
		B, Mn	1	1	1	1	1	0	1	1	n3	n2	n1	n0					5	B←M(n3~0)
		Mn, A	1	1	1	1	1	0	0	0	n3	n2	n1	n0					5	M(n3~0)←A
		Mn, B	1	1	1	1	1	0	0	1	n3	n2	n1	n0					5	M(n3~0)←B
	LDPX	MX, i	1	1	1	0	0	1	1	0	i3	i2	i1	i0					5	M(X)←i3~0, X←X+1
		r, q	1	1	1	0	1	1	1	0	r1	r0	q1	q0					5	r←q, X←X+1
	LDPY	MY, i	1	1	1	0	0	1	1	1	i3	i2	i1	i0					5	M(Y)←i3~0, Y←Y+1
		r, q	1	1	1	0	1	1	1	1	r1	r0	q1	q0					5	r←q, Y←Y+1
	LBPX	MX, l	1	0	0	1	l7	l6	l5	l4	l3	l2	l1	l0					5	M(X)←l3~0, M(X+1)←l7~4, X←X+2
Calculation	ADD	r, i	1	1	0	0	0	0	r1	r0	i3	i2	i1	i0		*	↕	↕	7	r←r+i3~0
		r, q	1	0	1	0	1	0	0	0	r1	r0	q1	q0		*	↕	↕	7	r←r+q
	ADC	r, i	1	1	0	0	0	1	r1	r0	i3	i2	i1	i0		*	↕	↕	7	r←r+i3~0+C
		r, q	1	0	1	0	1	0	0	1	r1	r0	q1	q0		*	↕	↕	7	r←r+q+C
	SUB	r, q	1	0	1	0	1	0	1	0	r1	r0	q1	q0		*	↕	↕	7	r←r−q
	SBC	r, i	1	1	0	1	0	1	r1	r0	i3	i2	i1	i0		*	↕	↕	7	r←r−i3~0−C
		r, q	1	0	1	0	1	0	1	1	r1	r0	q1	q0		*	↕	↕	7	r←r−q−C
	AND	r, i	1	1	0	0	1	0	r1	r0	i3	i2	i1	i0			↕		7	r←r∧i3~0
		r, q	1	0	1	0	1	1	0	0	r1	r0	q1	q0			↕		7	r←r∧q
	OR	r, i	1	1	0	0	1	1	r1	r0	i3	i2	i1	i0			↕		7	r←r∨i3~0
		r, q	1	0	1	0	1	1	0	1	r1	r0	q1	q0			↕		7	r←r∨q
	XOR	r, i	1	1	0	1	0	0	r1	r0	i3	i2	i1	i0			↕		7	r←r∀i3~0
		r, q	1	0	1	0	1	1	1	0	r1	r0	q1	q0			↕		7	r←r∀q
	CP	r, i	1	1	0	1	1	1	r1	r0	i3	i2	i1	i0			↕	↕	7	r−i3~0
		r, q	1	1	1	1	0	0	0	0	r1	r0	q1	q0			↕	↕	7	r−q
	FAN	r, i	1	1	0	1	1	0	r1	r0	i3	i2	i1	i0			↕		7	r∧i3~0
		r, q	1	1	1	1	0	0	0	1	r1	r0	q1	q0			↕		7	r∧q
	RLC	r	1	0	1	0	1	1	1	1	r1	r0	r1	r0			↕	↕	7	d3←d2, d2←d1, d1←d0, d0←C, C←d3
	RRC	r	1	1	1	0	1	0	0	0	1	1	r1	r0			↕	↕	5	d3←C, d2←d3, d1←d2, d0←d1, C←d0
	INC	Mn	1	1	1	1	0	1	1	0	n3	n2	n1	n0			↕	↕	7	M(n3~0)←M(n3~0)+1
	DEC	Mn	1	1	1	1	0	1	1	1	n3	n2	n1	n0			↕	↕	7	M(n3~0)←M(n3~0)−1
	ACPX	MX, r	1	1	1	1	0	0	1	0	1	0	r1	r0		*	↕	↕	7	M(X)←M(X)+r+C, X←X+1
	ACPY	MY, r	1	1	1	1	0	0	1	0	1	1	r1	r0		*	↕	↕	7	M(Y)←M(Y)+r+C, Y←Y+1
	SCPX	MX, r	1	1	1	1	0	0	1	1	1	0	r1	r0		*	↕	↕	7	M(X)←M(X)−r−C, X←X+1
	SCPY	MY, r	1	1	1	1	0	0	1	1	1	1	r1	r0		*	↕	↕	7	M(Y)←M(Y)−r−C, Y←Y+1
	NOT	r	1	1	0	1	0	0	r1	r0	1	1	1	1			↕		7	r←r̄

SMC8360F Series

CMOS 8 BIT SINGLE CHIP MICROCOMPUTER

- **Minimum Instruction Cycle Time : 1μs**
- **On-chip Gate Array**
- **4KB ROM**

■DESCRIPTION

The SMC8360F Series is a high-performance low power CMOS 8 bit single chip microcomputer (minimum machine cycle time: 1μs). It contains a ROM, a RAM, I/O ports, a timer/counter, and a gate array (SMC8362/SMC8367: 2 input NAND × 848 gates).

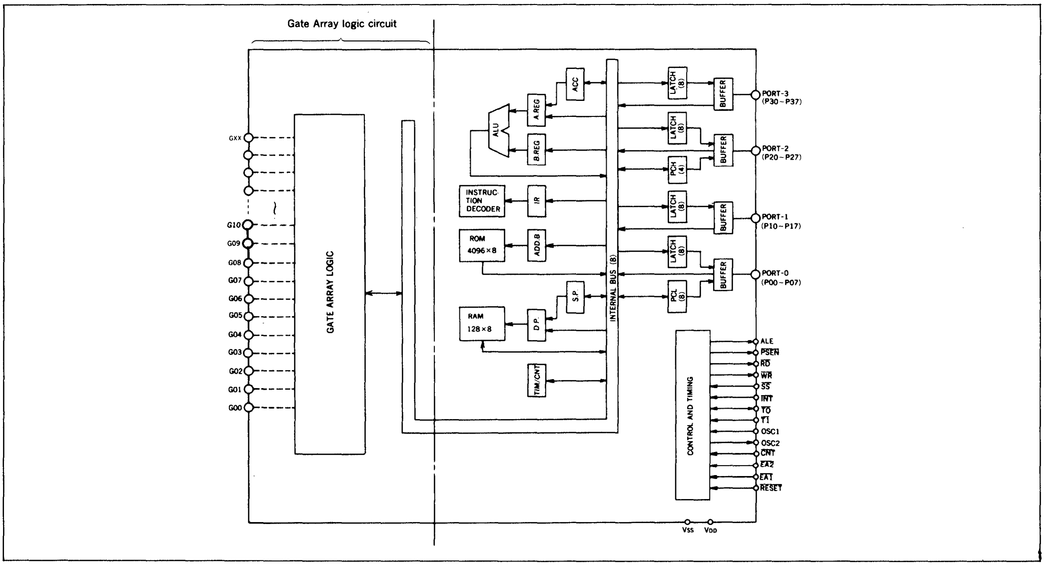
The major features include:

- High flexibility due to built-in gate array
- Reduce software overhead and faster processing.
- The capability of implementing a general-purpose controller for peripherals of the processor, by implementing a bus interface circuit.

■FEATURES

- CPU·································CMOS LSI 8 bits
- On-chip oscillator circuit···········50kHz to 4MHz
- Instruction cycle time·····················1μs (Min)
- Instruction set·································104 sets
- ROM···4k × 8 bits
- RAM···128 × 8 bits
- Built-in gate array
  SMC8362/SMC8367 : 2 input NAND × 848 gates
- Gate array ·············SLA6000 Series Equivalent
- I/O ports·······························4 ports × 8 bits
  Gate array SMC8362/SMC8367 : 33 I/O (Max)
- Extension of external program ROM (Gate array option)
- Release from STOP mode circuit (Gate array option)
- Interrupts : External interrupt ·························
  $\overline{\text{INT}}$, $\overline{\text{T1}}$, and $\overline{\text{T0}}$ OR logic
  Internal interrupt ··························
  timer/counter overflow
- Nesting levels···················8 subroutines (Max)
- Operational modes·········RUN, HALT, and STOP
- Single power supply ······5V ± 10% or 2.5 to 6.0V
- Package·························80-pin QFP (plastic)

■BLOCK DIAGRAM



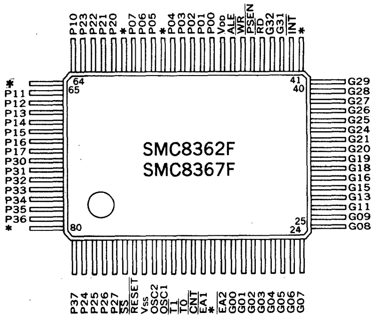
SMC8360F SERIES

Model	Gate	PORT-1(P10~P17)	Max gate array I/O	Package
SMC8362	848 gates	Input port or Output port	33	80-pin QFP (plastic)
SMC8367	848 gates	Address bus	33	80-pin QFP (plastic)

PIN CONFIGURATION

80-pin QFP (plastic)

F80-5



＊ : Left floating

PIN DESCRIPTION

P00—P07	Bus interface bi-directional port
P10—P17	I/O port or 8 bit address bus
P20—P27	I/O port
P30—P37	I/O port
ALE	Address latch enable
$\overline{\text{WR}}$	Write
$\overline{\text{RD}}$	Read
$\overline{\text{EA1,EA2}}$	Control mode pin
$\overline{\text{CNT}}$	Counter input
$\overline{\text{RESET}}$	System reset
$\overline{\text{SS}}$	Single step
OSC1	Crystal oscillator input pin
OSC2	Crystal oscillator output pin
$\overline{\text{INT}}$	Interrupt input
$\overline{\text{T1}}$	Interrupt input
$\overline{\text{T0}}$	Interrupt input/clock output
G00—GXX	Gate array I/O pin

ABSOLUTE MAXIMUM RATINGS

(V_{SS}=GND)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	$V_{SS}-0.3$ to 7.0	V
Input voltage	V_I	$V_{SS}-0.3$ to $V_{DD}+0.3$	V
Output voltage	V_O	$V_{SS}-0.3$ to $V_{DD}+0.3$	V
Output current/pin	I_O	±10	mA
Power dissipation	P_D	0.5	W
Operating temperature	T_{opr}	−40 to 85	℃
Storage temperature	T_{stg}	−65 to 150	℃
Soldering temperature and time	T_{sol}	260℃, 10sec (Lead only)	—

RECOMMENDED OPERATING CONDITIONS

(Ta= −40~85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}	f_{OSC}=50kHz to 1MHz	2.5	—	6.0	V
		f_{OSC}=50kHz to 4MHz	4.5	5	5.5	V
	V_{SS}		0	—	0	V
Input voltage	V_I		V_{SS}	—	V_{DD}	V
Operating frequency	f_{OSC}	V_{DD}=5V±10%	50	—	4000	kHz

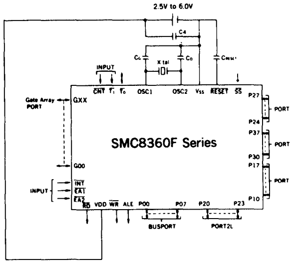
■ELECTRICAL CHARACTERISTICS

●DC Characteristics (CPU)

(V_{SS}=GND, Ta = −40 to 85°C)

Parameter	Symbol	Conditions		V_{DD}=5V±10%			V_{DD}=2.5 to 6.0V			Unit
				Min	Typ	Max	Min	Typ	Max	
Low level input voltage	V_{IL}			V_{SS}	—	0.8	V_{SS}	—	0.18V_{DD}	V
High level input voltage	V_{IH}	Except $\overline{\text{RESET}}$, $\overline{\text{SS}}$, OSC1		2.0	—	V_{DD}	0.6V_{DD}	—	V_{DD}	V
	V_{IH1}	$\overline{\text{RESET}}$, $\overline{\text{SS}}$, OSC1		V_{DD}−1	—	V_{DD}	0.8V_{DD}	—	V_{DD}	V
Low level output voltage	V_{OL}	I_{OL}=2.0mA		—	—	0.45	—	—	—	V
		I_{OL}=1.0mA		—	—	—	—	—	0.45	V
High level output voltage	V_{OH}	I_{OH}=−1.0mA		2.4	—	—	—	—	—	V
		I_{OH}=−100μA		—	—	—	0.8V_{DD}	—	—	V
Input current	I_{IP}	V_I=V_{SS} Input pin with pull-up resistor		−250	−100	−30	−300	—	−6	μA
	I_{IL}	V_I=V_{SS} Latch input pin		−3	—	3	−3	—	3	μA
	I_{IP2}	V_I=V_{SS} $\overline{\text{SS}}$ pin	RUN mode	−125	−50	−15	−150	—	−3	μA
			STOP mode	−3	0	3	−3	—	3	
Input leakage current	I_{LI1}	V_I=V_{DD}		−3	—	3	−3	—	3	μA
	I_{LI2}	V_I=V_{DD} $\overline{\text{SS}}$ pin	RUN mode	−3	0	3	−3	—	3	μA
			STOP mode	60	500	1500	12	—	1800	
Output leakage current	I_{LOP}	When at high impedance V_O=V_{SS} (with pull-up resistor)		−250	−100	−30	−300	—	−6	μA
	I_{LOL}	When at high impedance V_O=V_{SS} (with latch input)		−3	—	3	−3	—	3	μA
	I_{LOH}	When at high impedance V_O=V_{DD}		−3	—	3	−3	—	3	μA
Standby current	I_{DDS1}	HALT mode	V_{DD}=5V±10% (f=4MHz, Tcy=1μs)	—	2	10	—	—	—	mA
			V_{DD}=6V (f=4MHz, Tcy=1μs)	—	—	—	—	2.4	11	mA
			V_{DD}=3V (f=1MHz, Tcy=4μs)	—	—	—	—	0.3	1.4	mA
	I_{DDS2}	STOP mode	V_{DD}=5V±10%	—	—	20	—	—	—	μA
			V_{DD}=6V	—	—	—	—	—	50	μA
			V_{DD}=3V	—	—	—	—	—	20	μA
Operating current	I_{DDO}	RUN mode	V_{DD}=5V±10% (f=4MHz, Tcy=1μs)	—	6	20	—	—	—	mA
			V_{DD}=6V (f=4MHz, Tcy=1μs)	—	—	—	—	7	22	mA
			V_{DD}=3V (f=1MHz, Tcy=4μs)	—	—	—	—	0.9	3	mA
Data holding voltage	V_{DDR}	STOP mode (no rapid voltage change allowed)		3.0	—	—	—	—	—	V

■TYPICAL CIRCUIT



[NOTE 1] Crystal: 4MHz (V_{DD}=5V)
C_G=C_D≃50pF

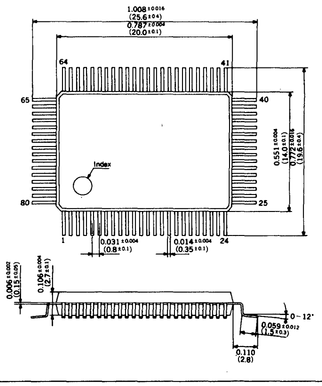
[NOTE 2] Ceramic oscillation is also applicable.

*System clock: external clock
Clock is supplied to the OSC1 pin from outside the system.

■PACKAGE DIMENSIONS

80-pin QFP (plastic)

F80-5



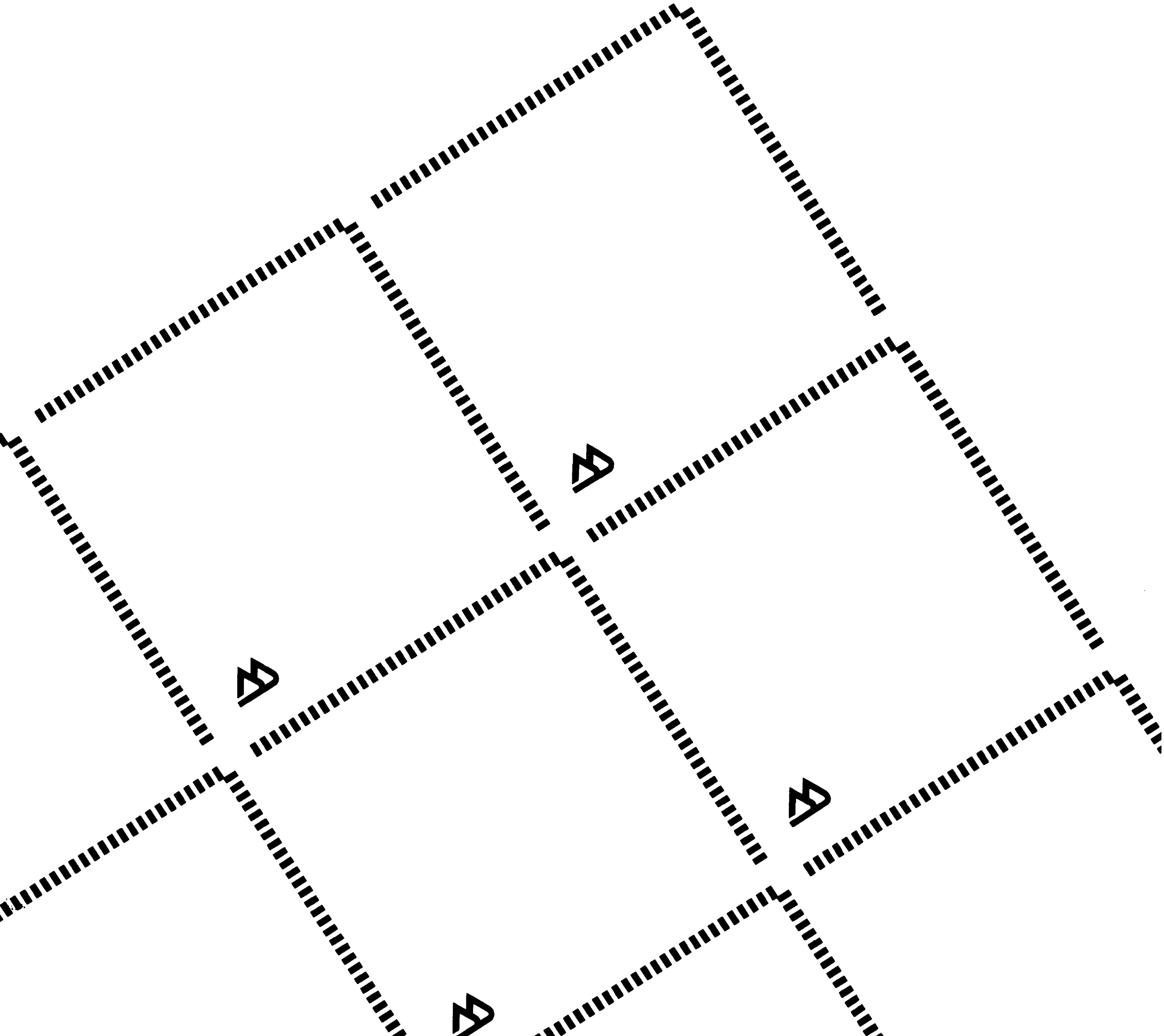
unit : inch
(mm)

INSTRUCTION SET

No.	Function	Mnemonic	Bytes	Machine cycle	Operation
1	Operational Instruction	ADD A,Rr	1	1	A ← A+Rr r=0 to 7
2		ADD A,(Rr)	1	1	A ← A+(Rr) r=0, 1
3		ADD A,#n	2	2	A ← A+$n_{7\text{ to }0}$
4		ADC A,Rr	1	1	A ← A+Rr+CY r=0 to 7
5		ADC A,(Rr)	1	1	A ← A+(Rr)+CY r=0, 1
6		ADC A,#n	2	2	A ← A+$n_{7\text{ to }0}$+CY
7		AND A,Rr	1	1	A ← A ∧ Rr r=0 to 7
8		AND, A,(Rr)	1	1	A ← A ∧ (Rr) r=0, 1
9		AND A,#n	2	2	A ← A ∧ $n_{7\text{ to }0}$
10		OR A,Rr	1	1	A ← A ∨ Rr r=0 to 7
11		OR A,(Rr)	1	1	A ← A ∨ (Rr) r=0, 1
12		OR A,#n	2	2	A ← A ∨ $n_{7\text{ to }0}$
13		XOR A,Rr	1	1	A ← A ∀ Rr r=0 to 7
14		XOR A,(Rr)	1	1	A ← A ∀ (Rr) r=0, 1
15		XOR A,#n	2	2	A ← A ∀ $n_{7\text{ to }0}$
16		ADD (Rr),A	1	1	(Rr) ← (Rr)+A r=0, 1
17		ADC (Rr),A	1	1	(Rr) ← (Rr)+A+CY r=0, 1
18		AND (Rr),A	1	1	(Rr) ← (Rr) ∧ A r=0, 1
19		OR (Rr),A	1	1	(Rr) ← (Rr) ∨ A r=0, 1
20		INC A	1	1	A ← A+1
21		DEC A	1	1	A ← A−1
22		CLR A	1	1	A ← 0
23		CPL A	1	1	A ← $\overline{A}$
24		DA A	1	1	Converts accumulator data into 2-digit BCD
25		SWAP A	1	1	$A_{7\text{ to }4}$ ↔ $A_{3\text{ to }0}$
26		RL A	1	1	A_{n+1} ← A_n, A_0 ← A_7 n=0 to 6
27		RLC A	1	1	A_{n+1} ← A_n, A_0 ← CY, CY ← A_7 n=0 to 6
28		RR A	1	1	A_n ← A_{n+1}, A_7 ← A_0 n=0 to 6
29		RRC A	1	1	A_n ← A_{n+1}, A_7 ← CY, CY ← A_0 n=0 to 6
30		INC Rr	1	1	Rr ← Rr+1 r=0 to 7
31		INC (Rr)	1	1	(Rr) ← (Rr) +1 r=0, 1
32		DEC Rr	1	1	Rr ← Rr−1 r=0 to 7
33		DEC (Rr)	1	1	(Rr) ← (Rr)−1 r=0, 1
34	Flag manipulation instructions	RES C	1	1	CY ← 0
35		CPL C	1	1	CY ← $\overline{CY}$
36		RES F0	1	1	F0 ← 0
37		CPL F0	1	1	F0 ← $\overline{F0}$
38		RES F1	1	1	F1 ← 0
39		CPL F1	1	1	F1 ← $\overline{F1}$
40	Transfer instructions	LD A,Rr	1	1	A ← Rr r=0 to 7
41		LD A,(Rr)	1	1	A ← (Rr) r=0, 1
42		LD A,#n	2	2	A ← $n_{7\text{ to }0}$
43		LD Rr,A	1	1	Rr ← A r=0 to 7
44		LD (Rr),A	1	1	(Rr) ← A r=0, 1
45		LD Rr,#n	2	2	Rr ← $n_{7\text{ to }0}$ r=0 to 7
46		LD (Rr),#n	2	2	(Rr) ← $n_{7\text{ to }0}$ r=0, 1
47		LD A,SRG	1	1	A ← SRG
48		LD SRG,A	1	1	SRG ← A
49		LDX A,(Rr)	1	2	A ← (Rr) r=0, 1
50		LDX (Rr),A	1	2	(Rr) ← A r=0, 1
51		LDPR A,(A)	1	2	A ← (PC11—8, A)
52		LDP3 A,(A)	1	2	A ← (0011, A)
53		EX A,Rr	1	1	A↔Rr r=0 to 7
54		EX A,(Rr)	1	1	A↔(Rr) r=0, 1
55		EXN A,(Rr)	1	1	$A_{3\text{ to }0}$ ↔ $(Rr)_{3\text{ to }0}$ r=0, 1
56,	Branch instructions	JP n	2	2	PC_{11} ← MR, $PC_{10\text{ to }8}$ ← $n_{10\text{ to }8}$ $PC_{7\text{ to }0}$ ← $n_{7\text{ to }0}$
57		JP A	1	2	$PC_{7\text{ to }0}$ ← A
58		DJNZ Rr, n	2	2	Rr ← Rr−1 r=0 to 7 if Rr ≠ 0
59		JP C, n	2	2	if CY=1 JUMP
60		JP NC, n	2	2	if CY=0 JUMP
61		JP Z, n	2	2	if A=0 JUMP
62		JP NZ, n	2	2	if A≠0 JUMP
63		JBT Ab, n	2	2	if Ab=1 JUMP b=7 to 0
64		JP F1, n	2	2	if F1=1 JUMP
65		JP F0, n	2	2	if F0=1 JUMP
66		JP TF, n	2	2	if TF=1 JUMP & TF ← 0
67		JP INTF, n	2	2	if INTF =1 JUMP & INTF ← 0
68		JP T1F;n	2	2	if T1F=1 JUMP & T1F ← 0
69		JP T1, n	2	2	if $\overline{T1}$='H' JUMP
70		JP T0, n	2	2	if $\overline{T0}$='H' JUMP
71		JP NT0, n	2	2	if $\overline{T0}$='L' JUMP
72		JBT Mb, n	2	2	if Mb=1 JUMP b=7 to 0
73	Subroutine call instructions	CALL n	2	2	(SP) ← PC, SRG, SP ← SP+1 PC_{11} ← MR $PC_{10\text{ to }8}$ ← $n_{10\text{ to }8}$ $PC_{7\text{ to }0}$ ← $n_{7\text{ to }0}$
74		RET	1	2	SP ← SP−1, PC ← (SP)
75		RETR	1	2	SP ← SP−1, PC ← (SP), SRG ← (SP)
76	I/O instructions	IN A, Pp	1	2	A ← Pp p=0 to 3
77		OUT Pp, A	1	2	Pp ← A p=0 to 3
78		AND Pp, #n	2	2	Pp ← Pp ∧ $n_{7\text{ to }0}$ p=0 to 3
79		OR Pp, #n	2	2	Pp ← Pp ∨ $n_{7\text{ to }0}$ p=0 to 3
80		IN A, P0	1	2	A ← P0
81		OUT P0, A	1	2	P0 ← A
82		AND P0, #n	2	2	P0 ← P0 ∧ $n_{7\text{ to }0}$
83		OR P0, #n	2	2	P0 ← P0 ∨ $n_{7\text{ to }0}$
84	Timer/counter instructions	LD A, TC	1	1	A ← TC
85		LD TC, A	1	1	TC ← A
86		STRT T	1	1	Start timer
87		STRT C	1	1	Start Event Counter
88		STOP TC	1	1	Stop timer/Counter
89		EI TC	1	1	Internal interrupt enable
90		DI TC	1	1	Internal interrupt disenable
91	Control instructions	EI EXT	1	1	External interrupt enable
92		DI EXT	1	1	External interrupt disenable
93		CHG ALT0	1	1	ALT ← 0
94		CHG ALT1	1	1	ALT ← 1
95		CHG MR0	1	1	MR ← 0
96		CHG MR1	1	1	MR ← 1
97		OUTT0 CLK	1	1	CLOCK is supplied from $\overline{T0}$
98		HALT	1	1	CPU Halt
99		STOP	1	1	Stop CPU
100		NOP	1	1	NO OPERATION
101	Gate array control instructions	LD Gn, A	1	1	Gn ← A n=0 to 3
102		LD A, Gn	1	1	A ← Gn n=0 to 3
103		GST Xn	1	1	Timing signal n=0 to 3
104		GST Yn	1	1	Timing signal n=0 to 3

1988/1989 CMOS DATA BOOK

C. PERIPHERALS



SMC82C37AC/-4/-5

CMOS PROGRAMMABLE DMA CONTROLLER

●Four DMA Channels

●Low Supply Current

■DESCRIPTION

The SMC82C37AC/-4/-5 is an enhanced CMOS version of a programmable 4-channel Direct Memory Access (DMA) controller. The device is designed to improve system performance by permitting the CPU to off-load the task of moving blocks of data to and from memory via one of the DMA channels.

■FEATURES

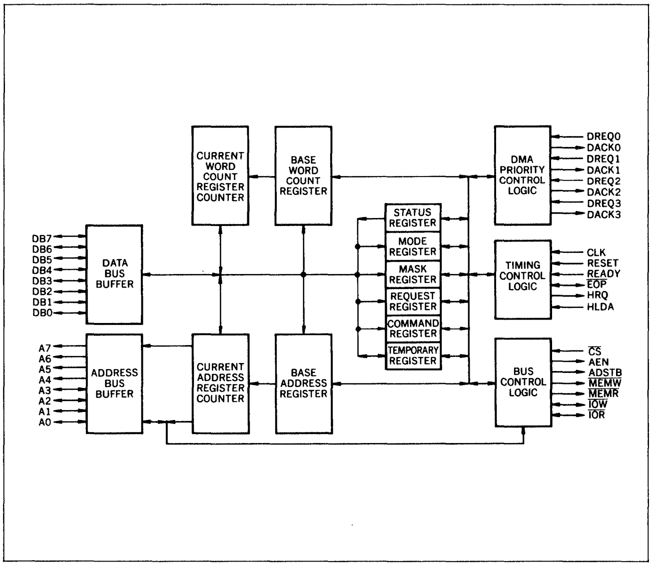
- ●Four DMA channels
- ●High data transfer rates ; up to 1.6M bytes/second
- ●Enable/disable control of DMA request
- ●Programmable features ·······Logic polarity of DREQ and DACK
  Fixed or rotating priority
  Address increment or decrement
- ●Automatic features ············Channel initialization
- ●External DMA termination
- ●Single power supply ·········5V±10%
- ●Package····························40-pin DIP (plastic)

●Clock frequency

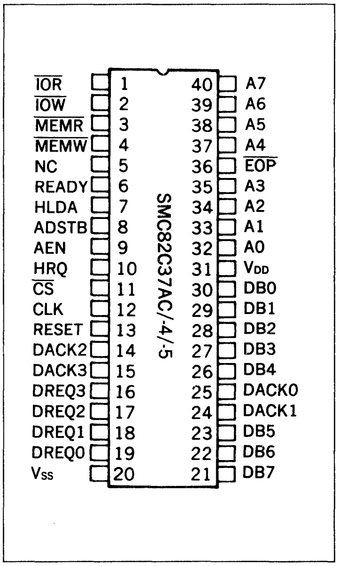
–SMC82C37AC	: 3.1MHz
–SMC82C37AC-4	: 4MHz
–SMC82C37AC-5*	: 5MHz

*Under development

■BLOCK DIAGRAM



■PIN CONFIGURATION



■ABSOLUTE MAXIMUM RATINGS

($V_{SS}=0V$)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.3 to 7	V
Input voltage	V_I	−0.3 to $V_{DD}+0.3$	V
Output voltage	V_O	−0.3 to $V_{DD}+0.3$	V
Operating free-air temperature range	T_{opr}	0 to 70	°C
Storage temperature range	T_{stg}	−65 to 150	°C

■RECOMMENDED OPERATING CONDITIONS

(Ta=0 to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}	—	4.5	5	5.5	V
Supply voltage	V_{SS}	—	—	0	—	V

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

($V_{DD}=5V\pm10\%$, $V_{SS}=0V$, Ta=0 to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Low level input voltage	V_{IL}		−0.3	—	0.8	V
High level input voltage	V_{IH}		2.0	—	$V_{CC}+0.3$	V
Low level output voltage	V_{OL}	$I_{OL}=2.0mA$ (data bus) $I_{OL}=3.2mA$ (other outputs)	—	—	0.45	V
High level output voltage	V_{OH}	$I_{OH}=-200\mu A$	2.4	—	—	V
		$I_{OH}=-100\mu A$ (HRQ only)	3.2	—	—	V
Input current	I_I	$V_I=0$ to V_{DD}	−10	—	10	μA
Off state output current	I_{OZ}	$V_I=0$ to V_{DD}	−10	—	10	μA
Supply current from V_{DD}	I_{DD}	$V_{IH}=V_{DD}, V_{IL}=V_{SS}, f_{CLK}=1/t_{cy}$ Min	—	—	15	mA

●AC Electrical Characteristics

○Slave mode

($V_{DD}=5V\pm10\%$, $V_{SS}=0V$, Ta=0 to 70°C)

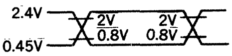
Parameter	Symbol	Conditions	SMC82C37AC		SMC82C37AC-4		SMC82C37AC-5		Unit
			Min	Max	Min	Max	Min	Max	
Address or $\overline{CS}$ setup time before read	t_{AR}	—	0	—	0	—	0	—	ns
$\overline{CS}$ setup time before write rising edge	t_{CW}	—	200	—	150	—	150	—	ns
Address setup time before write rising edge	t_{AW}	—	200	—	150	—	150	—	ns
Data setup time before write rising edge	t_{DW}	—	200	—	150	—	100	—	ns
Address or $\overline{CS}$ hold time after read	t_{RA}	—	0	—	0	—	0	—	ns
$\overline{CS}$ hold time after write	t_{WC}	—	0	—	0	—	0	—	ns
Address hold time after write	t_{WA}	—	0	—	0	—	0	—	ns
Data hold time after write	t_{WD}	—	0	—	0	—	0	—	ns
Read pulse width	t_{RW}	—	300	—	250	—	200	—	ns
Write pulse width	t_{WWS}	—	200	—	200	—	160	—	ns
Reset pulse width	t_{RSTW}	—	300	—	300	—	300	—	ns
Supply voltage setup time before reset	t_{RSTD}	—	500	—	500	—	500	—	ns
Reset setup time before read or write	t_{RSTS}	—	$2t_{CY}$	—	$2t_{CY}$	—	$2t_{CY}$	—	ns
Data output enable after read	t_{RDE}	—	—	200	—	200	—	140	ns
Data output disable after read	t_{RDF}	—	0	100	0	100	0	70	ns

○DMA mode

($V_{DD}=5V\pm10\%$, $V_{SS}=0V$, Ta=0 to 70°C)

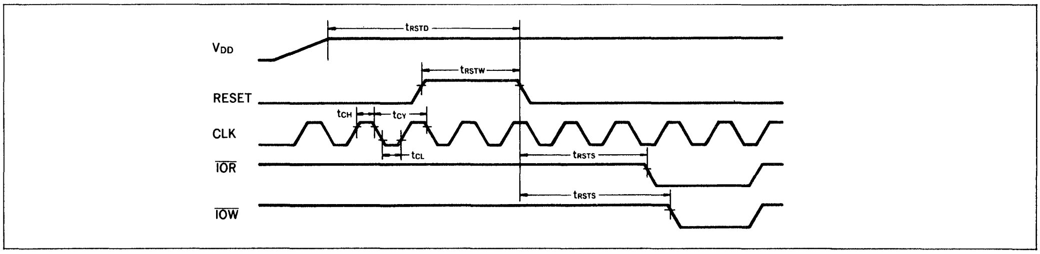
Parameter	Symbol	Conditions	SMC82C37AC		SMC82C37AC-4		SMC82C37AC-5		Unit
			Min	Max	Min	Max	Min	Max	
Propagation time from clock to AEN	t_{AEL}	—	—	300	—	225	—	200	ns
Propagation time from clock to AEN	t_{AET}	—	—	200	—	150	—	130	ns
Propagation time from clock to address active	t_{FAAB}	—	—	250	—	190	—	170	ns
Propagation time from clock to address stable	t_{ASM}	—	—	250	—	190	—	170	ns
Propagation time from clock to address floating	t_{AFAB}	—	—	150	—	120	—	90	ns
Propagation time from clock to data active	t_{FADB}	—	—	300	—	225	—	200	ns
Propagation time from clock to data floating	t_{AFDB}	—	—	250	—	190	—	170	ns
Propagation time from clock to ADSTB	t_{STL}	—	—	200	—	150	—	130	ns
Propagation time from clock to ADSTB	t_{STT}	—	—	140	—	110	—	90	ns
Data setup time before ADSTB	t_{ASS}	—	100	—	100	—	100	—	ns
Data hold time after ADSTB	t_{AHS}	—	50	—	40	—	30	—	ns
Propagation time from clock to read or write active	t_{FAC}	—	—	200	—	150	—	150	ns
Propagation time from clock to read or write	t_{DCL}	—	—	270	—	200	—	190	ns
Propagation time from clock to read	t_{DCTR}	—	—	270	—	210	—	190	ns
Propagation time from clock to write	t_{DCTW}	—	—	200	—	150	—	130	ns
Propagation time from clock to read or write floating	t_{AFC}	—	—	150	—	120	—	120	ns
Address hold time after read	t_{AHR}	—	$t_{CY}-100$	—	$t_{CY}-100$	—	$t_{CY}-100$	—	ns
Address hold time after write	t_{AHW}	—	$t_{CY}-50$	—	$t_{CY}-50$	—	$t_{CY}-50$	—	ns
Data setup time before $\overline{MEMW}$	t_{ODV}	—	200	—	125	—	125	—	ns
Data hold time after $\overline{MEMW}$	t_{ODH}	—	20	—	20	—	10	—	ns
Propagation time from clock to DACK	t_{AK}	—	—	250	—	220	—	170	ns
Propagation time from clock to $\overline{EOP}$ output		—	—	250	—	190	—	170	ns
Propagation time from clock to HRQ “H” 2.0V	t_{DQ}	—	—	160	—	120	—	120	ns
“H” 3.3V		—	—	250	—	190	—	120	
Clock high width	t_{CH}	—	120	—	100	—	80	—	ns
Clock low width	t_{CL}	—	150	—	110	—	68	—	ns
Clock period	t_{CY}	—	320	—	250	—	200	—	ns
External $\overline{EOP}$ setup time before clock	t_{EPS}	—	60	—	45	—	40	—	ns
External $\overline{EOP}$ pulse width	t_{EPW}	—	300	—	225	—	220	—	ns
DREQ setup time before clock	t_{QS}	—	0	—	0	—	0	—	ns
Ready setup time before clock	t_{RS}	—	100	—	60	—	60	—	ns
Ready hold time after clock	t_{RH}	—	20	—	20	—	20	—	ns
HLDA setup time before clock	t_{HS}	—	100	—	75	—	75	—	ns
Data setup time before $\overline{MEMR}$	t_{IDS}	—	250	—	190	—	170	—	ns
Data hold time after $\overline{MEMR}$	t_{IDH}	—	0	—	0	—	0	—	ns

Notes : AC testing waveform		Reference level	
Input pulse level	0.45V to 2.4V	input	$V_{IH}=2V$, $V_{IL}=0.8V$
Input pulse rise time	10ns	output	$V_{OH}=2V$, $V_{OL}=0.8V$
Input pulse fall time	10ns		

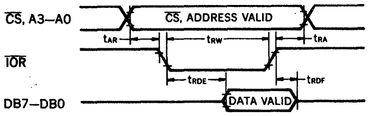


●Timing Chart

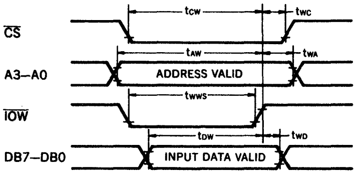
Reset Timing



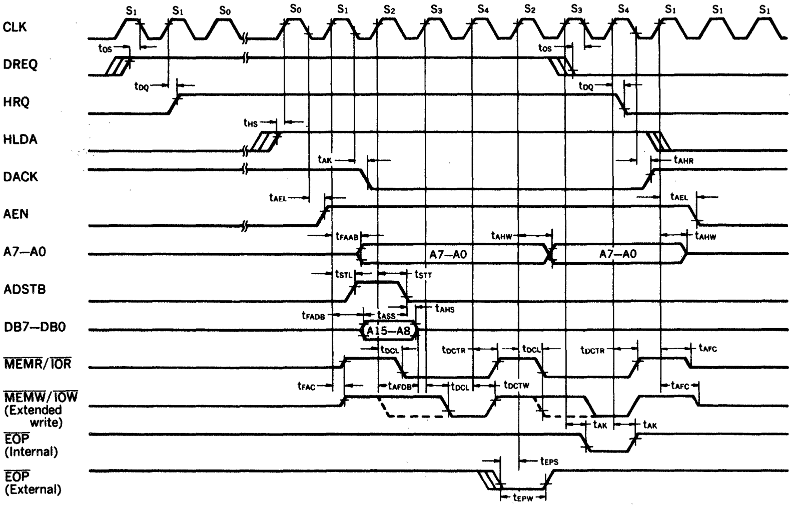
Slave Mode Timing (READ)



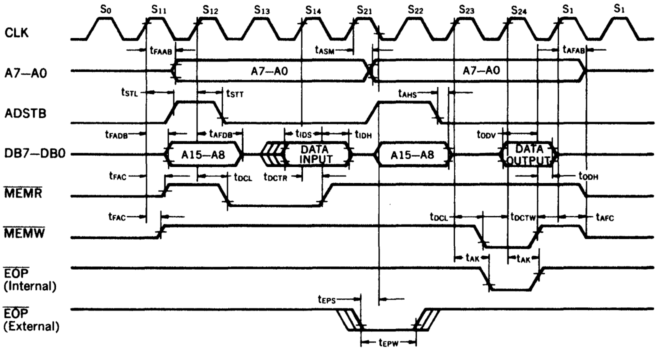
Slave Mode Timing (WRITE)



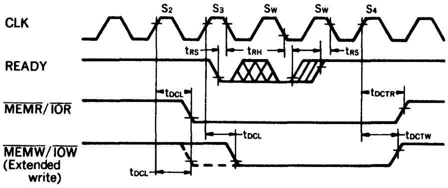
DMA Transfer



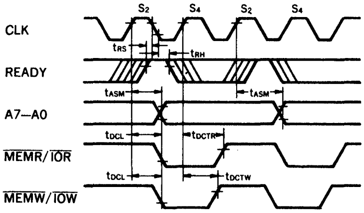
Memory to Memory Transfer



Ready Input Timing



Compressed Transfer Timing



■FUNCTIONS

The SMC82C37AC/-4/-5 is a programmable 4-channel DMA controller. The device offers a variety of programmable control features that can be dynamically reconfigured under program control. There are three programmable transfer modes: single, block and demand. There is also a full 64K address and word count capability per channel.

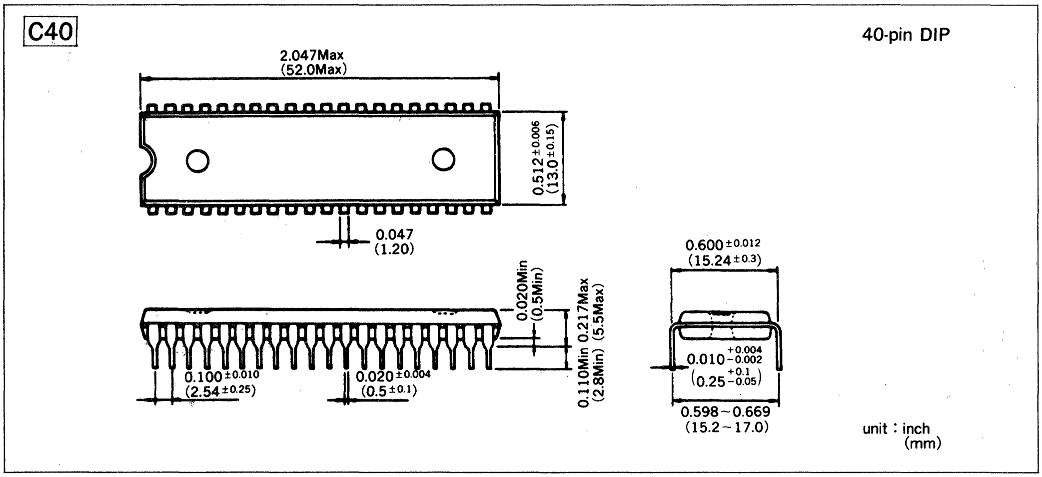
The device consists of three basic control blocks: the timing control block, the program command control block and the priority encoder block. To start a DMA operation, set a start address, an end address, a mode, and commands. The device requests control of the system bus when HRQ=1 is valid. The CPU acknowledges that it has relinquished control of the system bus via the hold acknowledge pin (HLDA=1) to the SMC 82C37AC/-4/-5. A DACK signal is then sent to the highest priority channel and DMA operation begins.

In the process of the DMA operation, addressing is performed in two bytes. The low byte is outputs A7–A0 and the high byte is outputs DB7–DB0; the high byte is sent to an external address latch. After the address is transmitted, the read/write control signals are sent to memory ($\overline{\text{MEMR}}$/$\overline{\text{MEMW}}$) or to a peripheral ($\overline{\text{IOR}}$/$\overline{\text{IOW}}$).

■APPLICATIONS

DMA control of peripheral equipment such as floppy disks and CRT terminals that require high-speed data transfer.

■PACKAGE DIMENSIONS



SMC82C51AC

CMOS PROGRAMMABLE COMMUNICATION INTERFACE

- ●**Synchronous/Asynchronous Receiver/Transmitter**
- ●**Baud Rate -- DC to 64Kbps**
- ●**Low Power**

■DESCRIPTION

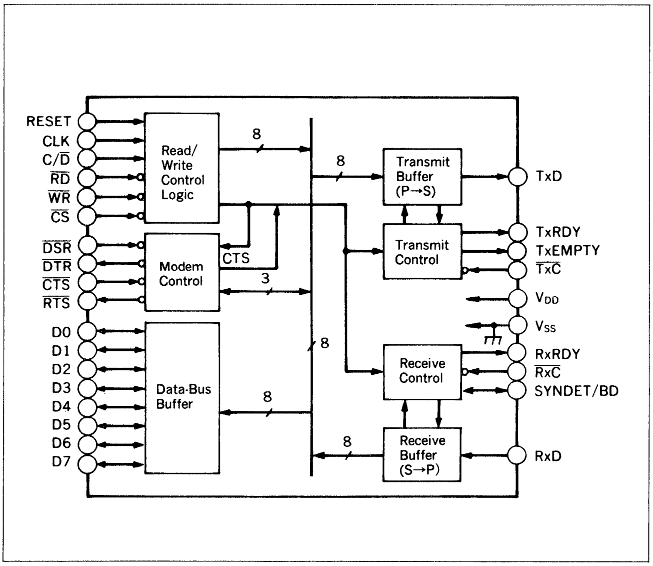
The SMC82C51AC is the enhanced CMOS version of the industry standard Universal Synchronous/Asynchronous Receiver/Transmitter (USART) designed for data communications.

■FEATURES

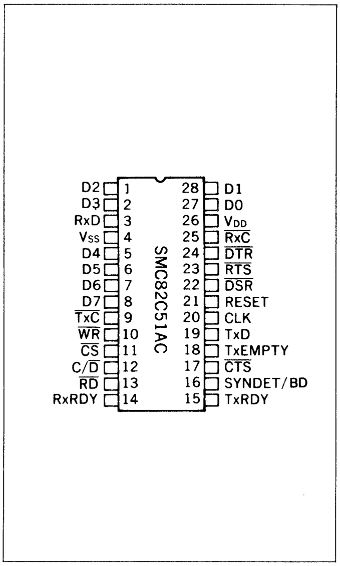
- ●Synchronous 5 to 8-bit character operation
  - – Internal or external character synchronization
  - – Automatic SYNC character insertion
  - – Synchronous baud rate : DC to 64K baud
- ●Asynchronous 5 to 8-bit character operation
  - – Clock rate of 1, 16, or 64 times baud rate
  - – 1, 1.5 or 2 stop bits
  - – False start bit detection
  - – Automatic break detection and handling
- ●Baud rate : DC to 64K Baud
- ●Full-duplex, double-buffered transmitter and receiver
- ●Error detection : parity, overrun and framing
- ●Single 5V (±10%) power supply
- ●Package··························28-pin DIP
  28-pin SOP*

*Under development

■BLOCK DIAGRAM



■PIN CONFIGURATION



■ABSOLUTE MAXIMUM RATINGS

($V_{SS}=0V$, $Ta=25°C$)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}	With respect to V_{SS}	-0.3 to 7	V
Input voltage	V_I		-0.3 to $V_{DD}+0.3$	V
Output voltage	V_O		-0.3 to $V_{DD}+0.3$	V
Operating temperature	T_{opr}	—	-20 to 75	°C
Storage temperature	T_{stg}	—	-65 to 150	°C
Soldering temperature and time	T_{sol}	—	260°C, 10s (at lead)	—

■RECOMMENDED OPERATING CONDITIONS

($Ta=-20$ to $75°C$, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}	—	4.5	5	5.5	V
Power-supply voltage	V_{SS}	—	—	0	—	V

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

($Ta=-20$to$75°C$, $V_{DD}=5V\pm10\%$, $V_{SS}=0V$, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High-level input voltage	V_{IH}	—	2	—	$V_{DD}+0.3$	V
Low-level input voltage	V_{IL}	—	-0.3	—	0.8	V
High-level output voltage	V_{OH}	$I_{OH}=-400\mu A$	2.4	—	—	V
Low-level output voltage	V_{OL}	$I_{OL}=2.2mA$	—	—	0.45	V
Supply current from V_{DD}	I_{DD}	—	—	—	5	mA
High-level input current	I_{IH}	$V_I=V_{DD}$	-10	—	10	μA
Low-level input current	I_{IL}	$V_I=0V$	-10	—	10	μA
Off-state input current	I_{OZ}	$V_{SS}=0V$, $V_I=0V$ to V_{DD}	-10	—	10	μA
Input capacitance	C_I	$V_{DD}=V_{SS}$, $f=1MHz$, $25mV_{rms}$, $Ta=25°C$	—	—	10	pF
Input/output capacitance	$C_{I/O}$	$V_{DD}=V_{SS}$, $f=1MHz$, $25mV_{rms}$, $Ta=25°C$	—	—	20	pF

●AC Electrical Characteristics

○ Timing Requirements

($Ta=-20$ to $75°C$, $V_{DD}=5V\pm10\%$, $V_{SS}=0V$, unless otherwise noted.)

Parameter		Symbol	Alternative Symbol	Conditions	Min	Typ	Max	Unit
Clock cycle time *1, 2		$t_{C(\phi)}$	t_{CY}		320	—	1350	ns
Clock high pulse width		$t_{W(\phi)}$	t_{ϕ}		120	—	$t_{C(\phi)}-90$	ns
Clock low pulse width		$t_{W(\bar{\phi})}$	$t_{\bar{\phi}}$		90	—	—	ns
Clock rise time		t_r	t_R		—	—	20	ns
Clock fall time		t_f	t_F		—	—	20	ns
Transmitter input clock frequency	1X baud rate	f_{TX}	f_{TX}		DC	—	64	kHz
	16X baud rate		f_{TX}		DC	—	310	kHz
	64X baud rate		f_{TX}		DC	—	615	kHz
Transmitter input clock low pulse width	1X baud rate	$t_{W(TPWL)}$	t_{TPW}		12	—	—	$t_{C(\phi)}$
	16X,64X baud rate		t_{TPW}		1	—	—	$t_{C(\phi)}$
Transmitter input clock high pulse width	1X baud rate	$t_{W(TPWH)}$	t_{TPD}		15	—	—	$t_{C(\phi)}$
	16X,64X baud rate		t_{TPD}		3	—	—	$t_{C(\phi)}$
Receiver input clock frequency	1X baud rate	f_{RX}	f_{RX}		DC	—	64	kHz
	16X baud rate		f_{RX}		DC	—	310	kHz
	64X baud rate		f_{RX}		DC	—	615	kHz
Receiver input clock low pulse width	1X baud rate	$t_{W(RPWL)}$	t_{RPW}		12	—	—	$t_{C(\phi)}$
	16X,64X baud rate		t_{RPW}		1	—	—	$t_{C(\phi)}$
Receiver input clock high pulse width	1X baud rate	$t_{W(RPWH)}$	t_{RPO}		15	—	—	$t_{C(\phi)}$
	16X,64X baud rate		t_{RPO}		3	—	—	$t_{C(\phi)}$
Address setup time before read ($\overline{CS}$, $C/\overline{D}$) *3		$t_{SU(A-R)}$	t_{AR}		0	—	—	ns
Address hold time after read ($\overline{CS}$, $C/\overline{D}$) *3		$t_{h(R-A)}$	t_{RA}		0	—	—	ns

Parameter	Symbol	Alternative Symbol	Conditions	Min	Typ	Max	Unit
Read pulse width	$t_{w(R)}$	t_{RR}		200	—	—	ns
Address setup time before write	$t_{SU(A-W)}$	t_{AW}		0	—	—	ns
Address hold time after write	$t_{h(W-A)}$	t_{WA}		0	—	—	ns
Write pulse width	$t_{w(W)}$	t_{WW}		200	—	—	ns
Data setup time before write	$t_{SU(DQ-W)}$	t_{DW}		100	—	—	ns
Data hold time after write	$t_{h(W-DQ)}$	t_{WD}		0	—	—	ns
E•SYNDET setup time before $\overline{\text{RxC}}$	$t_{SU(ESD-RxC)}$	t_{ES}		18	—	—	$t_{C(\phi)}$
Control setup time before read	$t_{SU(C-R)}$	t_{CR}		20	—	—	$t_{C(\phi)}$
Write recovery time between writes*4	t_{RV}	t_{RV}		6	—	—	$t_{C(\phi)}$
RxD setup time before internal sampling pulse	$t_{SU(RxD-IS)}$	t_{SRx}		2	—	—	μs
RxD hold time after internal sampling pulse	$t_{h(IS-RxD)}$	t_{HRx}		2	—	—	μs

*1 The $\overline{\text{TxC}}$ and $\overline{\text{RxC}}$ frequencies have the following limitations with respect to CLK.
For 1X baud rate f_{TX}, $f_{RX} \leqq 1/(30t_{C(\phi)})$. For 16X, 64X baud rate f_{TX}, $f_{RX} \leqq 1/(4.5t_{C(\phi)})$

*2 Reset pulse width $= 6t_{C(\phi)}$ minimum. System clock must be running during reset.

*3 $\overline{\text{CS}}$,C/$\overline{\text{D}}$ are considered as address.

*4 This recovery time is for mode initialization only. Write data is allowed only when TxRDY=1. Recovery time between writes for asynchronous mode is $8t_{C(\phi)}$, and that for synchronous mode is $16t_{C(\phi)}$.

○ Switching Characteristics

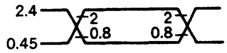
(Ta = −20 to 75°C, $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.)

Parameter	Symbol	Alternative symbol	Conditions*7	Min	Typ	Max	Unit
Output data enable time after read*5	$t_{PZV(R-DQ)}$	t_{RD}	$C_L = 150pF$	—	—	170	ns
Output data disable time after read	$t_{PVZ(R-DQ)}$	t_{DF}		10	—	100	ns
TxD enable time after falling edge of $\overline{\text{TxC}}$	$t_{PZV(TxC-TxD)}$	t_{CTx}		—	—	1	μs
Propagation time from center of last bit to TxRDY clear *6	$t_{PLH(CLB-TxR)}$	t_{TxRDY}		—	—	8	$t_{C(\phi)}$
Propagation time from write data to TxRDY *6	$t_{PHL(W-TxR)}$	$t_{TxRDY\ CLEAR}$		—	—	400	ns
Propagation time from center of last bit to RxRDY *6	$t_{PLH(CLB-RxR)}$	t_{RxRDY}		—	—	26	$t_{C(\phi)}$
Propagation time from read data to RxRDY clear *6	$t_{PHL(R-RxR)}$	$t_{RxRDY\ CLEAR}$		—	—	400	ns
Propagation time from rising edge of $\overline{\text{RxC}}$ to internal SYNDET *6	$t_{PLH(RxC-SYD)}$	t_{IS}		—	—	26	$t_{C(\phi)}$
Propagation time from center of last bit to TxEMPTY *6	$t_{PLH(CLB-TxE)}$	$t_{TxEMPTY}$		20	—	—	$t_{C(\phi)}$
Propagation time from rising edge of $\overline{\text{WR}}$ to control *6	$t_{PHL(W-C)}$	t_{WC}		8	—	—	$t_{C(\phi)}$

*5 Assumes that address is vaild before falling edge of $\overline{\text{RD}}$.

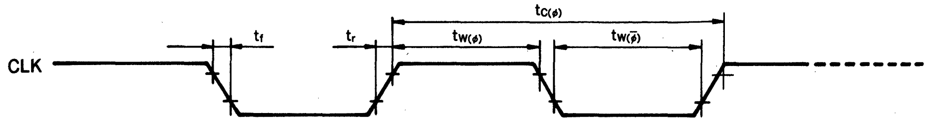
*6 Status-up data can have a maximum delay of 28 clock periods from the event affecting the status.

*7 Input pulse level 0.45 to 2.4V Reference level Input $V_{IH} = 2V$, $V_{IL} = 0.8V$
Input pulse rise time 20ns Output $V_{OH} = 2V$, $V_{OL} = 0.8V$
Input pulse fall time 20ns

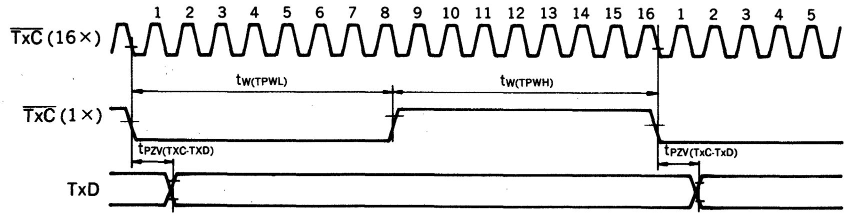


●Timing Chart

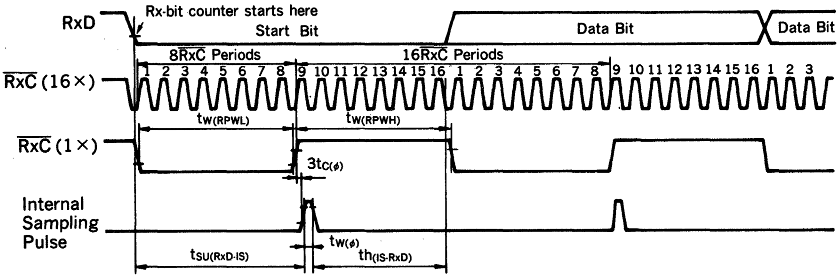
○System clock (CLK)



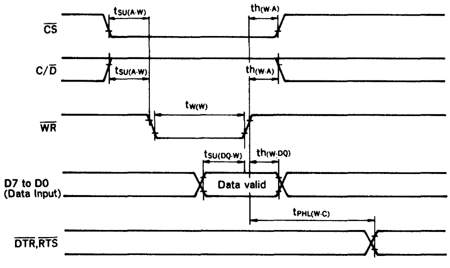
○Transmitter clock & data



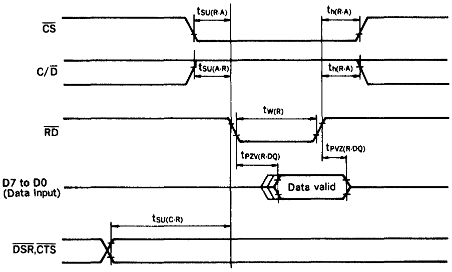
○Receiver clock & data



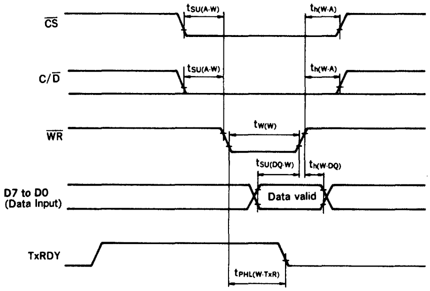
○Write control cycle (CPU → USART)



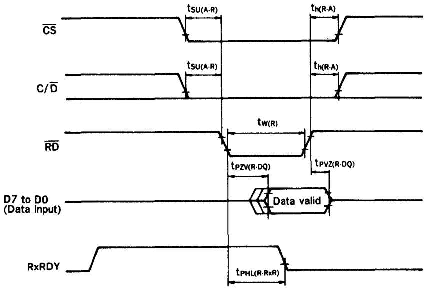
○Read control cycle (USART → CPU)



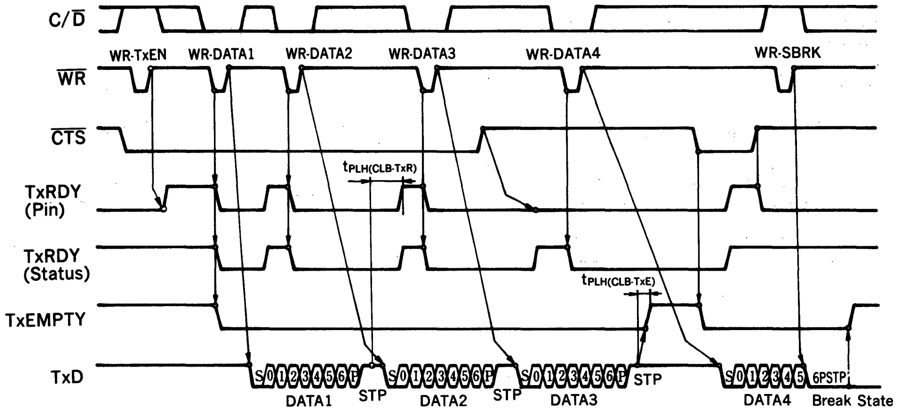
○Write data cycle (CPU → USART)



○Read data cycle (USART → CPU)

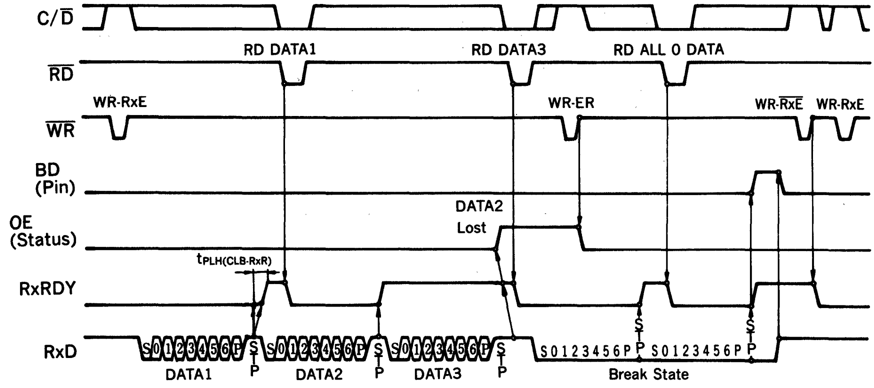


○Transmitter control & flag timing (async mode)



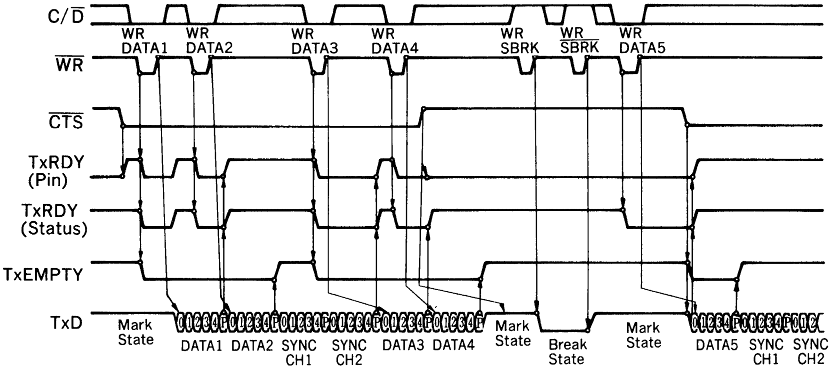
* 8 Example format = 7 bits/character with parity & 2 stop bits
* 9 TxRDY(pin) = 1 ← (Transmit-data buffer is empty)·(TxEN = 1)·($\overline{\text{CTS}}$ = L) = 1
*10 TxRDY(status) = 1 ← (Transmit-data buffer is empty) = 1

○Receiver control & flag timing (async mode)



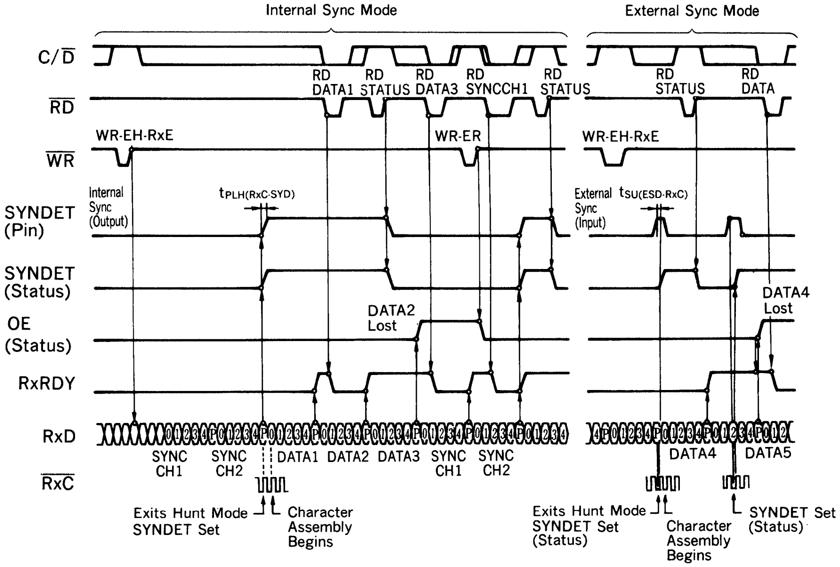
*11 Example format = 7 bits/character with parity

○ Transmitter control & flag timing (sync mode)



* Example format = 5 bits/character with parity, bi-sync characters.

○ Receiver control & flag timing (sync mode)



* Example format = 5 bits/character with parity, bi-sync characters.

■FUNCTIONS

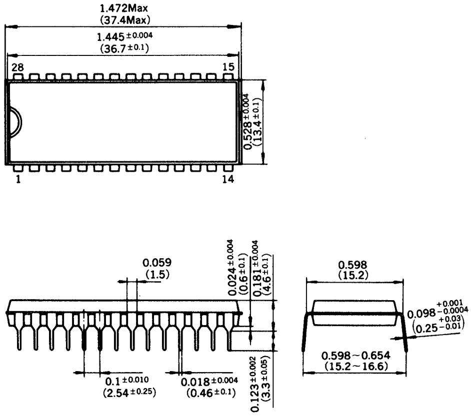
The SMC 82C51AC is used as a peripheral device and programmed to interface a CPU with virtually all serial data transmission techniques presently in use. Including IBM's "bi-sync". The SMC82C51AC can accept data characteristics from the CPU in parallel format, convert the data into a serial stream and transmit the data via the TxD pin. It can also receive data in a serial stream via the RxD pin, convert the data into a parallel format and transmit the data to the CPU. The SMC82C51AC, upon receipt of parallel or serial data, will flag the CPU using the TxRDY or RxRDY signals. The CPU can also poll the SMC82C51AC status with $C/\overline{D}=1$. The status which may be read contains Information such as data transmission error, parity error, overrun error or frame error.

■APPLICATIONS

In 8-bit microcomputer applications, modem control of data communications.
Control of CRT, TTY and other terminal equipment.

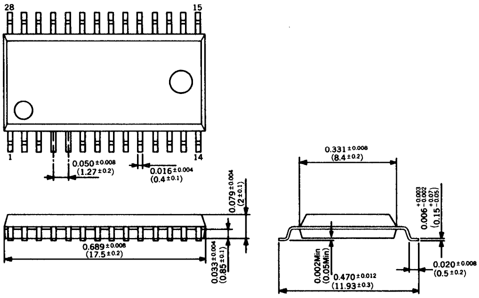
■PACKAGE DIMENSIONS

C28-8 28-pin DIP



unit : inch
(mm)

M28-8 28-pin SOP



unit : inch
(mm)

PF173-03

SMC82C54C/-6

CMOS PROGRAMMABLE INTERVAL TIMER

- **3 Independent 18-bit Counters**
- **6 Programmable Counter Modes**
- **Low Power**

■DESCRIPTION

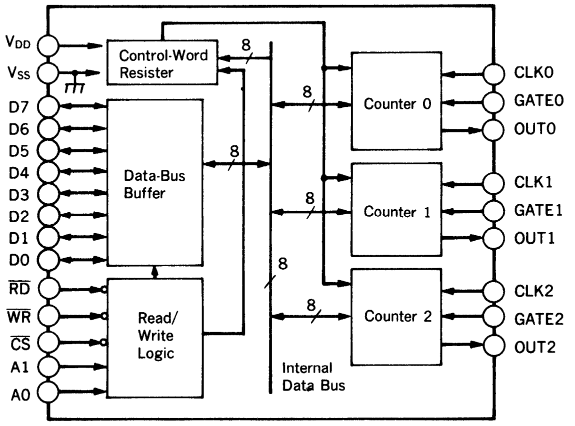
The SMC82C54C[*1]/-6 is a CMOS Programmable Timer/Counter. It is designed to provide a flexible solution to Timer/Counter requirements in microcomputer systems. The device provides three independent 18-bit counters. Each counter is capable of handling clock inputs up to 8 MHz. This Timer/Counter has six programmable modes.

■FEATURES

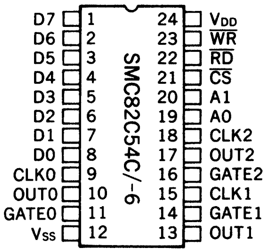
- Compatible with most 8-bit microprocessors
- Three independent 16-bit counters
- Clock input ······················ SMC82C54C[*1] DC to 8MHz
  SMC82C54C-6 DC to 6MHz
- Binary or decimal counter
- Six programmable counter modes
- Status poll feature
- Single 5V (±10%) power supply
- Package ·························· 24-pin DIP
  24-pin SOP[*2]

[*1] SMC82C54C : Under development
[*2] Under development

■BLOCK DIAGRAM



■PIN CONFIGURATION



■ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V, Ta=25°C)

Parameter	Symbol	Ratings	Unit
Power supply voltage	V_{DD}	−0.3 to 7	V
Input voltage	V_I	−0.3 to V_{DD}+0.3	V
Output voltage	V_O	−0.3 to V_{DD}+0.3	V
Operating temperature	T_{opr}	−20 to 75	°C
Storage temperature	T_{stg}	−65 to 150	°C
Soldering temperature and time	T_{sol}	260°C, 10s (at lead)	—

■RECOMMENDED OPERATING CONDITIONS

(Ta=−20 to 75°C, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power supply voltage	V_{DD}	—	4.50	5	5.50	V
Supply voltage (GND)	V_{SS}	—	—	0	—	V

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

(Ta=−20 to 75°C, V_{DD}=5V±10%, unless otherwise noted)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
High-level input voltage	V_{IH}	—		2.0	—	V_{DD}+0.3	V
Low-level input voltage	V_{IL}	—		−0.3	—	0.8	V
High-level output voltage	V_{OH}	V_{SS}=0V, I_{OH}=−400μA		2.4	—	—	V
Low-level output voltage	V_{OL}	V_{SS}=0V, I_{OL}=2.0mA		—	—	0.45	V
High-level input current	I_{IH}	V_{SS}=0V, V_I=5.50V		—	—	±10	μA
Low-level input current	I_{IL}	V_{SS}=0V, V_I=0V		—	—	±10	μA
Off-state output current	I_{OZ}	V_{SS}=0V, V_I=0 to V_{DD}		—	—	±10	μA
Power supply Current	I_{DD}	SMC82C54C	V_{SS}=0V, f=8MHz	—	—	10	mA
		SMC82C54C-6	V_{SS}=0V, f=6MHz				
Power supply current during STAND BY	I_{DDS}	V_{SS}=0V, other inputs are V_{SS} or V_{DD}		—	—	10	μA
Input capacitance	C_I	V_{IL}=V_{SS}, f=1MHz, 25mVrms, Ta=25°C		—	—	10	pF
Input/output capacitance	$C_{I/O}$	$V_{I/OL}$=V_{SS}, f=1MHz, 25mVrms, Ta=25°C		—	—	20	pF

●AC Electrical Characteristics

○Timing Requirements

(Ta=−20 to 75°C, V_{DD}=5V±10%, V_{SS}=0V, unless otherwise noted)

Read cycle

Parameter	Symbol	Alternative symbol	Conditions	Min	Typ	Max	Unit
Read pulse width	$t_{w(R)}$	t_{RR}	C_L=150pF	150	—	—	ns
$\overline{CS}$ setup time before read	$t_{SU(S\text{-}R)}$	t_{SR}		0	—	—	ns
Address setup time before read	$t_{SU(A\text{-}R)}$	t_{AR}		45	—	—	ns
Address hold time after read	$t_{h(R\text{-}A)}$	t_{RA}		0	—	—	ns
Read recovery time	$t_{rec(R)}$	t_{RV}		200	—	—	ns

Write cycle

Parameter	Symbol	Alternative Symbol	Conditions	Min	Typ	Max	Unit
Write pulse width	$t_{w(W)}$	t_{WW}	C_L=150pF	150	—	—	ns
$\overline{CS}$ setup time before write	$t_{SU(S\text{-}W)}$	t_{SW}		0	—	—	ns
Address setup time before write	$t_{SU(A\text{-}W)}$	t_{AW}		0	—	—	ns
Address hold time after write	$t_{h(W\text{-}A)}$	t_{WA}		0	—	—	ns
Data setup time before write	$t_{SU(D\text{-}W)}$	t_{DW}		100	—	—	ns
Data hold time after write	$t_{h(W\text{-}D)}$	t_{WD}		0	—	—	ns
Write recovery time	$t_{rec(W)}$	t_{RV}		200	—	—	ns

○Clock and gate timing

Parameter		Symbol	Alternative symbol	Conditions	Min	Typ	Max	Unit
Clock high pulse width	SMC82C54C	$t_{W(\phi H)}$	t_{PWH}	$C_L=150pF$	60	—	—	ns
	SMC82C54C-6				55	—	—	
Clock low pulse width	SMC82C54C	$t_{W(\phi L)}$	t_{PWL}		60	—	—	ns
	SMC82C54C-6				110	—	—	
Clock cycle time	SMC82C54C	$t_{C(\phi)}$	t_{CLK}		125	—	—	ns
	SMC82C54C-6				165	—	—	
Clock rise time		$t_{r(\phi)}$	t_R		—	—	100	ns
Clock fall time		$t_{f(\phi)}$	t_F		—	—	100	ns
Gate high pulse width		$t_{W(GH)}$	t_{GW}		50	—	—	ns
Gate low pulse width		$t_{W(GL)}$	t_{GL}		50	—	—	ns
Gate setup time before clock		$t_{SU(G\text{-}\phi)}$	t_{GS}		50	—	—	ns
Gate hold time after clock		$t_{h(\phi\text{-}G)}$	t_{GH}		50	—	—	ns

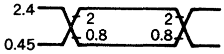
○Switching Characteristics

(Ta = −20 to 75°C, $V_{DD}=5V\pm10\%$, $V_{SS}=0V$, unless otherwise noted)*

Parameter		Symbol	Alternative symbol	Conditions	Min	Typ	Max	Unit
Propagation time from address to output		$t_{PZV(A\text{-}Q)}$	t_{AD}	$C_L=150pF$	—	—	220	ns
Propagation time from read to output	SMC82C54C	$t_{PZV(R\text{-}Q)}$	t_{RD}		—	—	120	ns
	SMC82C54C-6				—	—	170	
Propagation time from read to output floating		$t_{PVZ(R\text{-}Q)}$	t_{DF}		5	—	90	ns
Propagation time from gate to output		$t_{PXV(G\text{-}Q)}$	t_{ODG}		—	—	120	ns
Propagation time from clock to output		$t_{PXV(\phi\text{-}Q)}$	t_{OD}		—	—	150	ns

* A.C Testing waveform

Input pulse level	0.45 to 2.4V
Input pulse rise time	10ns
Input pulse fall time	10ns
Reference level input	$V_{IH}=2V$, $V_{IL}=0.8V$
Output	$V_{OH}=2V$, $V_{OL}=0.8V$

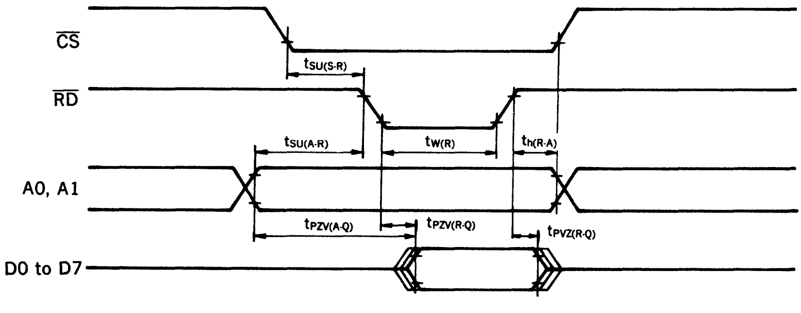


■FUNCTIONS

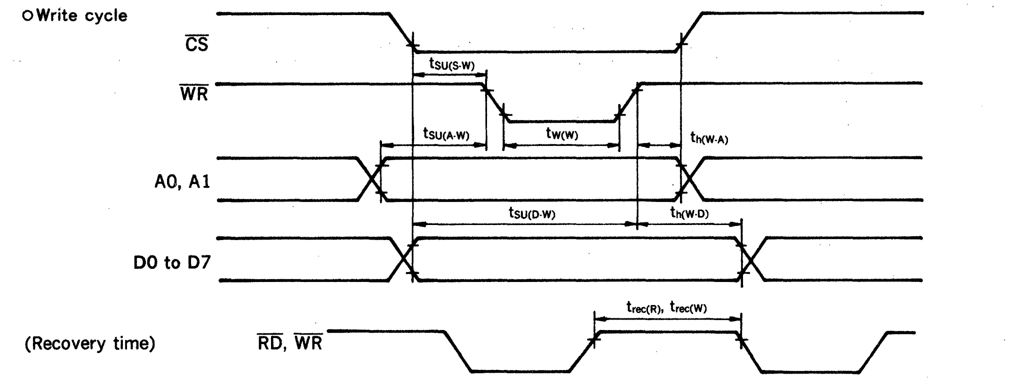
There are three independent programmable 16-bit counters. Each counter can operate in any of the six programmable counter modes. Mode 0(Interrupt on Terminal Count) is typically used for event counting. Mode 1 is a retriggerable one shot. Modes 2 and 3 are typically used as rate generators. Modes 4 and 5 are used as triggered strobes. With software and hardware triggered, respectively. Each counter's status can be monitored by polling via the read back command.

■TIMING CHART (Reference voltage : High = 2.0V Low = 0.8V)

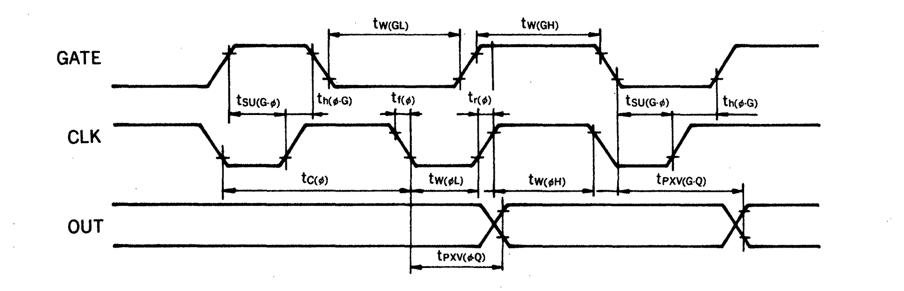
○Read cycle



○Write cycle



○Clock and gate cycle

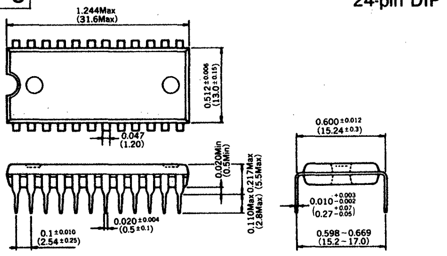


■APPLICATION

Delayed time setting, pulse counting and rate generation in microcomputers.

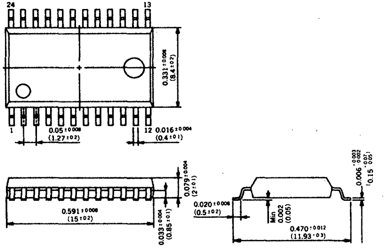
■PACKAGE DIMENSIONS

C24-8 24-pin DIP



unit : inch
(mm)

M24-8 24-pin SOP



unit : inch
(mm)

SMC82C55AC-5

CMOS PROGRAMMABLE PERIPHERAL INTERFACE

- **24 Bit Input/Output**
- **Improved DC Driving Capability**
- **Low Power**

■DESCRIPTION

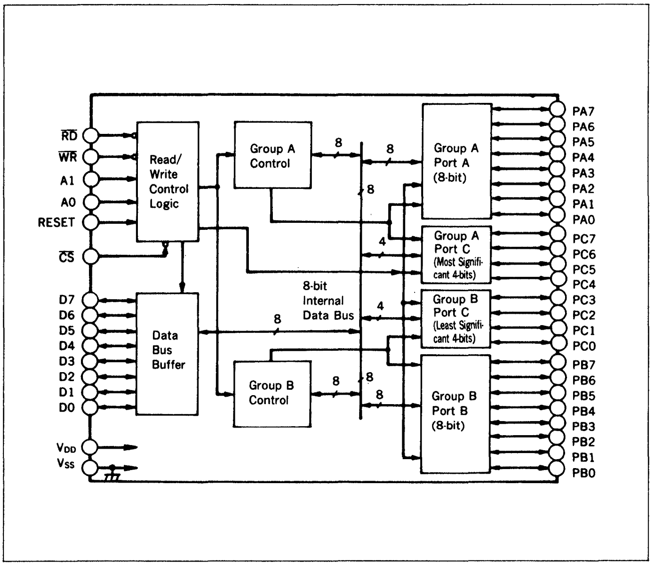
The SMC82C55AC-5 is a CMOS General Purpose Programmable I/O device designed for use with an 8/16 bit CPU. The device has 24 programmable I/O pins that can be individually programmed in two groups of 12.

■FEATURES

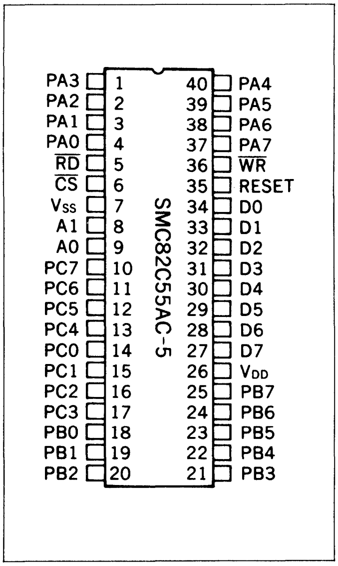
- 24 programmable I/O pins
- Compatible with 80XX series of microprocessors
- Direct bit set/reset capability
- Improved DC driving capability
- Single 5V (±10%) power supply
- TTL compatible
- Package··························40-pin DIP
  40-pin SOP*

*Under development

■BLOCK DIAGRAM



■PIN CONFIGURATION



■ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V, Ta=25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}	With respect to V_{SS}	−0.3 to 7	V
Input voltage	V_I		−0.3 to V_{DD}+0.3	V
Output voltage	V_O		−0.3 to V_{DD}+0.3	V
Operating temperature	T_{opr}	—	−20 to 75	°C
Storage temperature	T_{stg}	—	−65 to 150	°C
Soldering temperature and time	T_{sol}	—	260°C, 10s (lead)	—

■RECOMMENDED OPERATING CONDITIONS

(Ta=−20 to 75°C, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}	—	4.5	5	5.5	V
Supply voltage	V_{SS}	—	—	0	—	V

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

(Ta=−20 to 75°C, V_{DD}=5V±10%, V_{SS}=0V, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High-level input voltage	V_{IH}	—	2.0	—	V_{DD}+0.3	V
Low-level input voltage	V_{IL}	—	−0.3	—	0.8	V
Output high voltage*2	V_{OH}	I_{OH}=−400μA	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL}=2.5mA	—	—	0.45	V
Supply current from V_{DD}	I_{DD}	V_{SS}=0V. All input mode. RESET=0V. Other pins=V_{DD}	—	—	10	μA
Input leak current	I_{LI}	V_{SS}=0V, V_I=0V, V_{DD}	—	—	±10	μA
Off-state output current	I_{OZ}	V_{SS}=0V, V_I=0V, V_{DD}	—	—	±10	μA
Input capacitance	C_I	V_{IL}=V_{SS}, f=1MHz, 25mVrms Ta=25°C	—	—	10	pF
Input/output terminal capacitance	$C_{I/O}$	$V_{I/OL}$=V_{SS}, f=1MHz, 25mVrms, Ta=25°C	—	—	20	pF

*1 Current flowing into an IC is positive, out is negative.
*2 The sum total I_{OH} current must be less than −64mA on port B, C, and −32mA on Port A.

●AC Electrical Characteristics

○Timing Requirements

(Ta=−20 to 75°C, V_{DD}=5V±10%, V_{SS}=0V, unless otherwise noted)

Parameter	Symbol	Alternative symbol	Conditions	Min	Typ	Max	Unit
Read pulse width	$t_{w(R)}$	t_{RR}		200	—	—	ns
Peripheral setup time before read	$t_{SU(PE-R)}$	t_{IR}		0	—	—	ns
Peripheral hold time after read	$t_{h(R-PE)}$	t_{HR}		0	—	—	ns
Address setup time before read	$t_{SU(A-R)}$	t_{AR}		0	—	—	ns
Address hold time after read	$t_{h(R-A)}$	t_{RA}		0	—	—	ns
Write pulse width	$t_{w(W)}$	t_{WW}		200	—	—	ns
Data setup time before write	$t_{SU(DQ-W)}$	t_{DW}		100	—	—	ns
Data hold time after write	$t_{h(W-DQ)}$	t_{WD}		0	—	—	ns
Address setup time before write	$t_{SU(A-W)}$	t_{AW}		0	—	—	ns
Address hold time after write	$t_{h(W-A)}$	t_{WA}		0	—	—	ns
Acknowledge pulse width	$t_{w(ACK)}$	t_{AK}		300	—	—	ns
Strobe pulse width	$t_{w(STB)}$	t_{ST}		350	—	—	ns
Peripheral setup time before strobe	$t_{SU(PE-STB)}$	t_{PS}		0	—	—	ns
Peripheral hold time after strobe	$t_{h(STB-PE)}$	t_{PH}		150	—	—	ns
Read/write cycle time	$t_{C(RW)}$	t_{RV}		850	—	—	ns

●Switching Characteristics

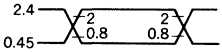
(Ta = −20 to 75°C, V_{DD} = 5V ± 10%, unless otherwise noted)

Parameter	Symbol	Alternative symbol	Conditions	Min	Typ	Max	Unit
Propagation time from read to data output	$t_{PZX(R \cdot DQ)}$	t_{RD}	C_L = 150pF			170	ns
Propagation time from read to data floating *3	$t_{PXZ(R \cdot DQ)}$	t_{DF}		10		100	ns
Propagation time from write to output	$t_{PHL(W \cdot PE)}$ $t_{PLH(W \cdot PE)}$	t_{WB}				350	ns
Propagation time from strobe to IBF flag	$t_{PLH(STB \cdot IBF)}$	t_{SIB}				300	ns
Propagation time from strobe to interrupt	$t_{PLH(STB \cdot INTR)}$	t_{SIT}				300	ns
Propagation time from read to interrupt	$t_{PHL(R \cdot INTR)}$	t_{RIT}				400	ns
Propagation time from read to IBF flag	$t_{PHL(R \cdot IBF)}$	t_{RIB}				300	ns
Propagation time from write to interrupt	$t_{PHL(W \cdot INTR)}$	t_{WIT}				450	ns
Propagation time from write to $\overline{OBF}$ flag	$t_{PHL(W \cdot OBF)}$	t_{WOB}				650	ns
Propagation time from acknowledge to $\overline{OBF}$ flag	$t_{PLH(ACK \cdot OBF)}$	t_{AOB}				350	ns
Propagation time from acknowledge to interrupt	$t_{PLH(ACK \cdot INTR)}$	t_{AIT}				350	ns
Propagation time from acknowledge to data output	$t_{PZX(ACK \cdot PE)}$	t_{AD}				300	ns
Propagation time from acknowledge to data floating *3	$t_{PXZ(ACK \cdot PE)}$	t_{KD}		20		250	ns

*3 Test conditions are not applied.

*4 A.C Testing waveform

Input pulse level	0.45 to 2.4V
Input pulse rise time	10ns
Input pulse fall time	10ns
Reference level input	V_{IH}=2V, V_{IL}=0.8V
Output	V_{OH}=2V, V_{OL}=0.8V



■FUNCTIONS

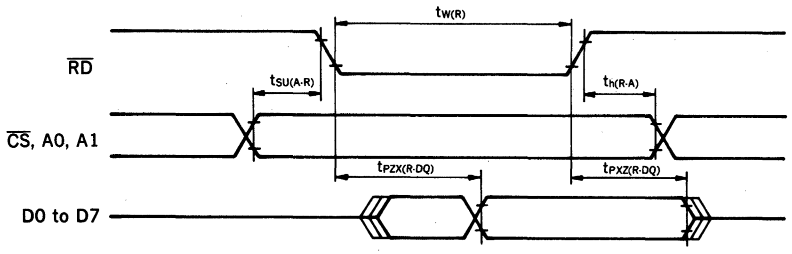
The SMC82C55AC-5 has programmable I/O pins that interface peripheral equipment to the CPU. The system software programs the functional configuration of the device.

The 24 programmable I/O pins may be individually configured in two groups of 12. Each group has three major modes of operation : 0, 1 and 2. In mode 0, each group of 12 I/O pins may be programmed in sets of four inputs or outputs. In mode 1, each group of 12 I/O pins may be grouped as one 8-bit I/O data port and one 4-bit control/status port. Mode 2 is used in Group A only, as one 8-bit bidirectional port and one 5-bit control /status port.

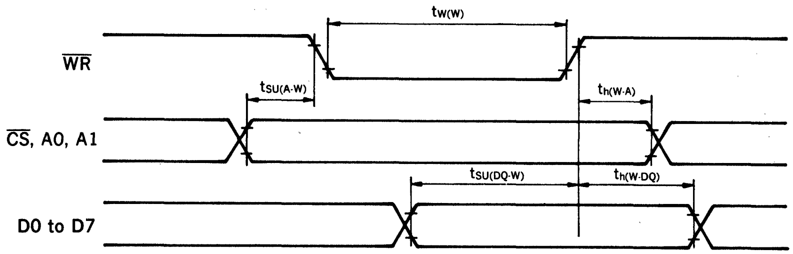
In mode 1 or 2, the control/status port bits can be set or reset by the CPU. A RESET pin is provided to clear all internal registers and set all ports to an input mode.

●Timing Chart

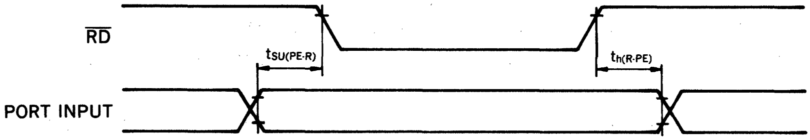
○Data bus read operation



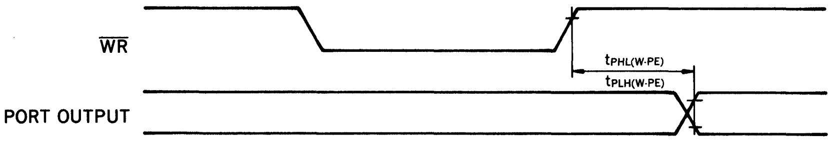
○Data bus write operation



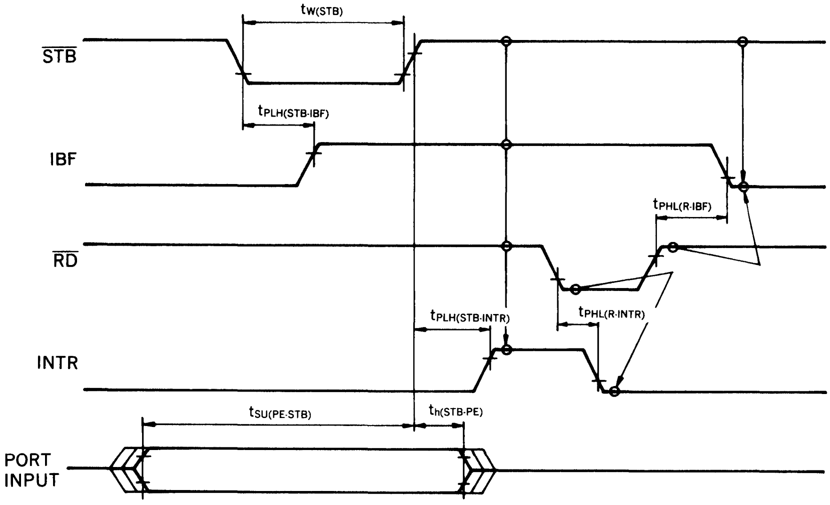
○Mode 0 Port input



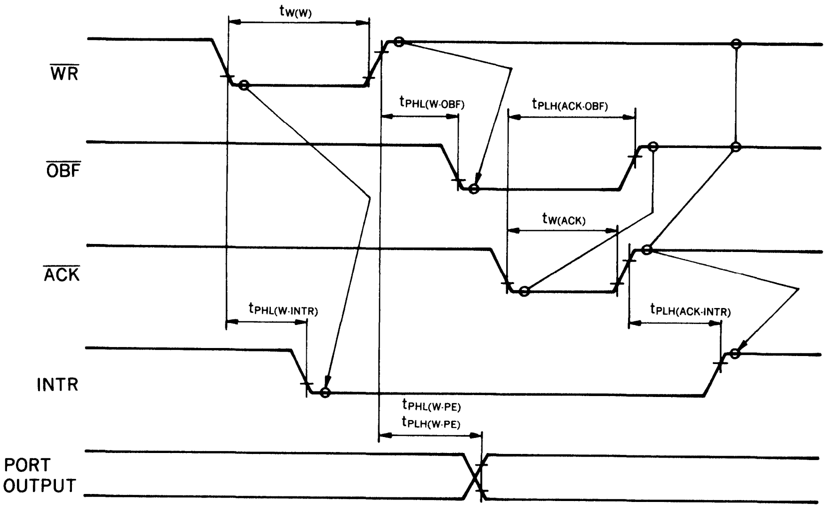
○Mode 0, 1 Port output



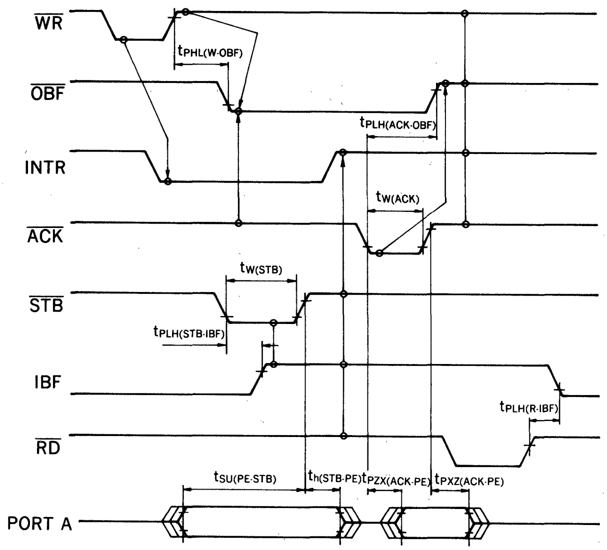
○Mode 1 Strobed input



○Mode 1 Strobed output



○ Mode 2 Bidirectional



$*5\ \ INTR = IBF \cdot \overline{MASK} \cdot \overline{STB} \cdot \overline{RD} + \overline{OBF} \cdot \overline{MASK} \cdot \overline{ACK} \cdot \overline{WR}$

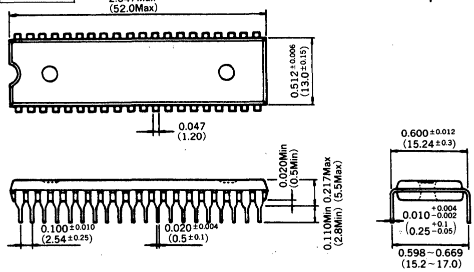
■APPLICATION

The SMC 82C55AC-5 is used as a general purpose programmable I/O device designed to interface peripheral equipment to the 80XX series of microprocessors.

■PACKAGE DIMENSIONS

C40-8

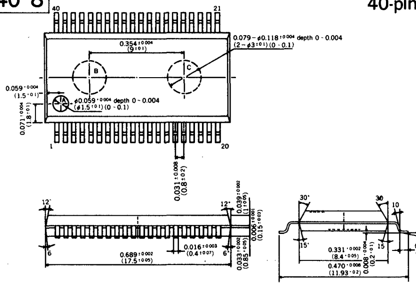
40-pin DIP



unit : inch
(mm)

M40-8

40-pin SOP



unit : inch
(mm)

SMC82C59AC

CMOS PROGRAMMABLE INTERRUPT CONTROLLER

- **Supports 8 Levels of Interrupt**
- **Many Functions for Interrupt**
- **Low Power**

■DESCRIPTION

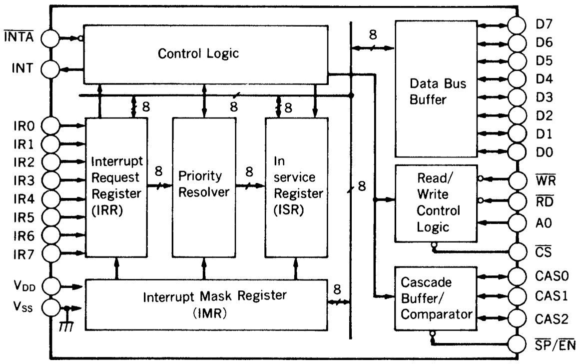
The SMC82C59AC is a CMOS Programmable Interrupt Controller. The device is designed to minimize the system software overhead required to handle multi-level interrupts. The device requires no clock inputs.

■FEATURES

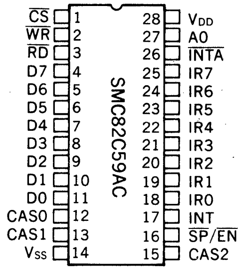
- Supports eight levels of interrupt
- Cascadable up to 64 levels
- Programmable
  - Priority
  - Mask Capability
  - Vectored Address
- Single 5V (±10%) power supply
- Package··························28-pin DIP
  28-pin SOP*

*Under development

■BLOCK DIAGRAM



■PIN CONFIGURATION



■ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V, Ta=25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Power-supply voltage	V_{DD}	With respect to V_{SS}	−0.3 to 7	V
Input voltage	V_I		−0.3 to V_{DD}+0.3	V
Output voltage	V_O		−0.3 to V_{DD}+0.3	V
Operating temperature	T_{opr}	—	−20 to 75	°C
Storage temperature	T_{stg}	—	−65 to 150	°C
Soldering temperature and time	T_{sol}	—	260°C, 10s (lead)	—

■RECOMMENDED OPERATING CONDITIONS

(Ta=−20 to 75°C, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}	—	4.5	5	5.5	V
Supply voltage	V_{SS}	—	—	0	—	V

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

(Ta=−20 to 75°C, V_{DD}=5V±10%, V_{SS}=0V, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High-level input voltage	V_{IH}	—	2	—	V_{DD}+0.3	V
Low-level input voltage	V_{IL}	—	−0.3	—	0.8	V
High-level output voltage	V_{OH}	I_{OH}=−400μA	2.4	—	—	V
High-level output voltage, interrupt request output	$V_{OH(INT)}$	I_{OH}=−100μA	3.5	—	—	V
Low-level output voltage	V_{OL}	I_{OL}=2.2mA	—	—	0.45	V
Standby supply current from V_{DD}	I_{DDS}	V_{DD}=5.5V, V_I=V_{DD} or GND output open	—	—	10	μA
High-level input current	I_{IH}	V_I=V_{DD}	−10	—	10	μA
Low-level input current	I_{IL}	V_I=0V	−10	—	10	μA
Off-state output current	I_{OZ}	V_{SS}=0, V_I=0.45 to 5.5V	−10	—	10	μA
High-level input current, interrupt request inputs	$I_{IH(IR)}$	V_I=V_{DD}	—	—	10	μA
Low-level input current, interrupt request inputs	$I_{IL(IR)}$	V_I =0V	−300	—	—	μA
Input capacitance	C_I	V_{DD}=V_{SS}, f=1MHz, 25mVrms, Ta=25°C	—	—	10	pF
Input/output capacitance	$C_{I/O}$	V_{DD}=V_{SS}, f=1MHz, 25mVrms, Ta=25°C	—	—	20	pF

●AC Electrical Characteristics

○Timing Requirements

(Ta=−20 to 75°C, V_{DD}=5V±10%, V_{SS}=0V, unless otherwise noted)

Parameter	Symbol	Alternative symbol	Conditions	Min	Typ	Max	Unit
Write pulse width	$t_{w(W)}$	t_{WLWH}		200	—	—	ns
Address setup time before write	$t_{SU(A-W)}$	t_{AHWL}		0	—	—	ns
Address hold time after write	$t_{h(W-A)}$	t_{WHAX}		0	—	—	ns
Data setup time before write	$t_{SU(DQ-W)}$	t_{DVWH}		100	—	—	ns
Data hold time after write	$t_{h(W-DQ)}$	t_{WHDX}		0	—	—	ns
Read pulse width	$t_{w(R)}$	t_{RLRH}		200	—	—	ns
Address setup time before read	$t_{SU(A-R)}$	t_{AHRL}		0	—	—	ns
Address hold time after read	$t_{h(R-A)}$	t_{RHAX}		0	—	—	ns
Interrupt request input width, low-level time, edge triggered mode	$t_{w(IR)}$	t_{JLJH}		100	—	—	ns
Cascade setup time before $\overline{INTA}$ (slave)	$t_{SU(CAS-INTA)}$	t_{CVIAL}		55	—	—	ns
Write recovery time	$t_{rec(W)}$	t_{WHRL}		190	—	—	ns
Read recovery time	$t_{rec(R)}$	t_{RHRL}		160	—	—	ns

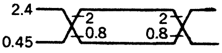
●Switching Characteristics

(Ta = −20 to 75°C, V_{DD}=5V±10%, V_{SS}=0V, unless otherwise noted)

Parameter	Symbol	Alternative symbol	Conditions	Min	Typ	Max	Unit
Data output enable time after read	$t_{PZV(R-DQ)}$	t_{RLDV}		—	—	170	ns
Data output disable time after read	$t_{PVZ(R-DQ)}$	t_{RHDZ}		10	—	100	ns
Data output enable time after address	$t_{PZV(A-DQ)}$	t_{AHDV}		—	—	200	ns
Propagation time from read to enable signal output	$t_{PHL(R-EN)}$	t_{RLEL}		—	—	125	ns
Propagation time from read to disable signal output	$t_{PLH(R-EN)}$	t_{RHEH}		—	—	150	ns
Propagation time from interrupt request input to interrupt request output	$t_{PLH(IR-INT)}$	t_{JHIH}		—	—	350	ns
Propagation time from $\overline{\text{INTA}}$ to cascade output (master)	$t_{PLV(INTA-CAS)}$	t_{IALCV}		—	—	565	ns
Data output enable time after cascade output (slave)	$t_{PZV(CAS-DQ)}$	t_{CVDV}		—	—	300	ns

*1 $\overline{\text{INTA}}$ signal is considered read signal
$\overline{\text{CS}}$ signal is considered address signal

Input pulse level	0.45 to 2.4V
Input pulse rise time	10ns
Input pulse fall time	10ns
Reference level Input	V_{IH}=2V, V_{IL}=0.8V
Output	V_{OH}=2V, V_{OL}=0.8V
Load capacitance	C_L=100pF, where $\overline{\text{SP}}/\overline{\text{EN}}$ pin is 15pF



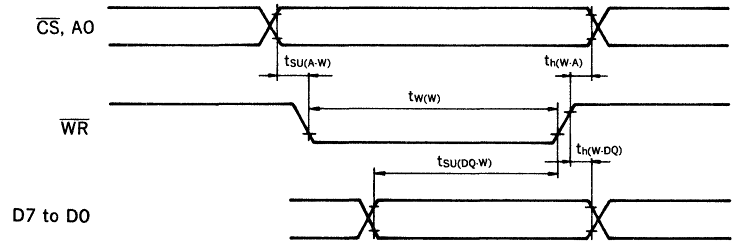
■FUNCTIONS

The SMC82C59AC is able to handle up to eight vectored priority interrupts for a CPU. The device is designed for real time use and thus reduces system software overhead. The priority and interrupt mask can be reconfigured as required by the system software.

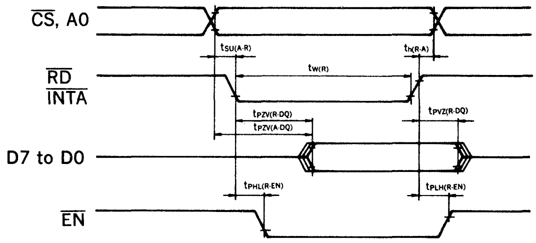
When a peripheral requires servicing an interrupt is generated by the peripheral. The SMC82C59AC based on the mask and the priority of the interrupt will issue an interrupt request (INT) to the CPU. After the CPU acknowledges ($\overline{\text{INTA}}$) the interrupt ; the SMC82C59AC can "point" the Program Counter to the service routine associated with the peripheral interrupt request. This "pointer" is a programmed vector address in the device and is released via the data bus.

●Timing Chart

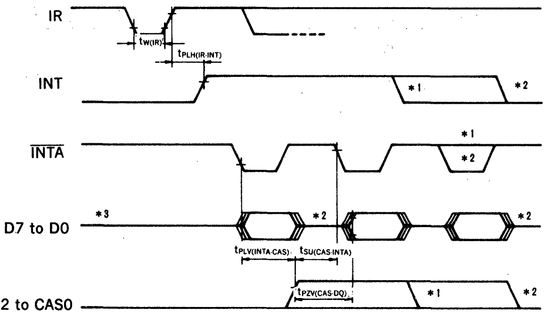
○Write Mode



○Read Mode

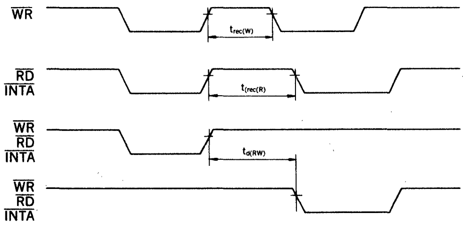


○Interrupt Sequence



＊1 8086 mode
＊2 8085 mode
＊3 8086 mode is in high-impedance state, pointer is released during the next $\overline{INTA}$. When in single 8085 mode, data is released by all $\overline{INTA}$s. When master, CALL instruction is released during the first $\overline{INTA}$, high impedance state during the second and third $\overline{INTA}$. When slave, high impedance state during the first $\overline{INTA}$, vectored address is released during the second and third $\overline{INTA}$.

○Other Timing



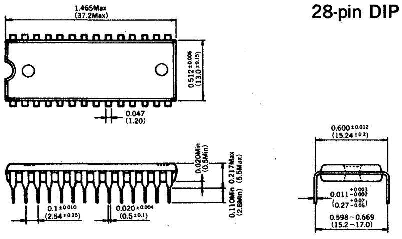
■APPLICATION

The SMC82C59AC can be used as an interrupt controller for most CPUs and specifically the 80XX series micro computers.

■PACKAGE DIMENSIONS

C28-8

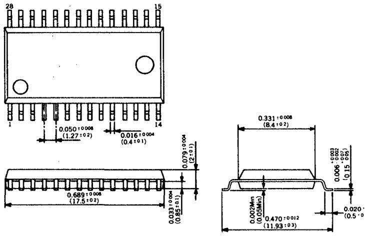
28-pin DIP



unit : inch
(mm)

M28-8

28-pin SOP



unit : inch
(mm)

SMC5242C

CMOS REAL TIME CLOCK

- **Microprocessor Direct Bus Connection**
- **Function of Hours, Minutes, Seconds, Days of Month, Months, Years, Days of Week**
- **Low Supply Current (Power Down Mode)**

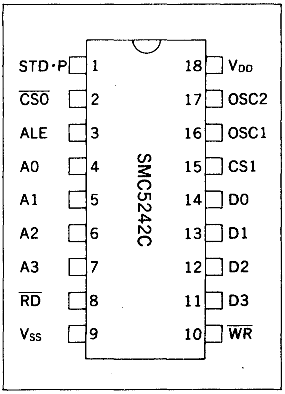
DESCRIPTION

The SMC5242C is a CMOS real time clock IC with calendar information designed to operate in bus oriented microprocessor applications. Standard quartz crystal (32.768kHz) is applicable.

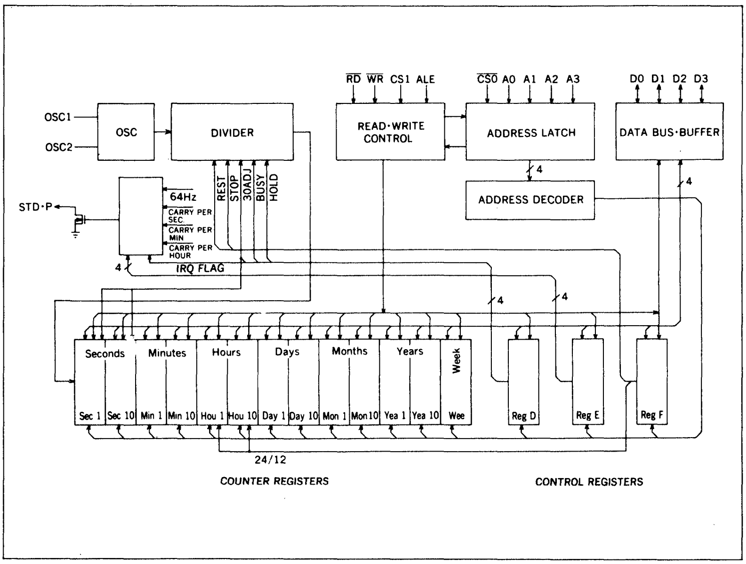
FEATURES

- 4 bit bi-directional DATA BUS and 4bit ADDRESS BUS
- 12-hour/24-hour operation (selecitive)
- BCD format code from seconds to years
- ±30 seconds error correction with software
- Selective interrupt output/periodical clock output
- Start/stop function
- Automatic distinction of Leap year
- ALE input pin for 8048 8051 8085CPU
- Low supply current······5μA MAX at $V_{DD}=2V$ (Power Down Mode)
  10μA MAX at $V_{DD}=5V$
- Power·······················$V_{DD}=5V\pm20\%$, (Power down mode $V_{DD}=2\sim6V$)
- Package···················18-pin DIP (plastic)

PIN CONFIGURATION



BLOCK DIAGRAM



PIN DESCRIPTION

D0 to D3	DATA BUS
A0 to A3	ADDRESS BUS
ALE	ADD. LATCH ENABLE
WR	WRITE
RD	READ
CS0	CHIP SELECT 0
CS1	CHIP SELECT 1
STD·P	STANDARD PULSE OUTPUT
OSC1, OSC2	CRYSTAL OSC
V_{DD}	POWER SUPPLY (+5V)
V_{SS}	POWER SUPPLY (0V)

■FUNCTION OF TERMINALS

Pin Name	Pin No.	Direction	Function
D0 to D3	11 to 14	Bi-direction	〔4 bit Data Bus〕 Bi-directional data bus pins, are connected to microprocessor data bus lines. Using this bus, any data is read from or written to the internal counter-register.
A0 to A3	4 to 7	Input	〔4 bit Address Bus〕 Input pins for address, are connected to microprocessor address bus lines. Address information select the internal register. (This bus is also used with ALE.)
ALE	3	Input	〔Address Latch Enable〕 This is input pin for reading address data and $\overline{\text{CS0}}$. When ALE=H, the address data and $\overline{\text{CS0}}$ are read into the IC. The address data and $\overline{\text{CS0}}$ are latched at negative-going of ALE. For microprocessors that don't have ALE output, this pin should be "H".
$\overline{\text{WR}}$	10	Input	〔Write〕 At $\overline{\text{WR}}$=L, the data on data bus (D0 to D3) is written into the register appointed by address lines (A0 to A3).
$\overline{\text{RD}}$	8	Input	〔Read〕 At $\overline{\text{RD}}$=L, the data from the register appointed by address lines (A0 to A3) is outputed to data bus (D0 to D3).
$\overline{\text{CS0}}$	2	Input	〔Chip Select 0〕 $\overline{\text{CS0}}$=L makes this IC active, and this pin is able to be used with ALE also.
CS1	15	Input	〔Chip Select 1〕 Input pin, makes this IC stand-by or operating. When CS1=H this pin makes this IC active. (When CS1=L this pin makes IC stand-by.)
STD•P	1	Output	〔Standard Pulse〕 STD•p is output pin of N-ch open drain. This pin outputs periodical interrupt wave or periodical pulse wave. When STD•P=L, this is active. $\overline{\text{CS0}}$, CS1 don't inhibit this output.
OSC1 OSC2	16 17	Input	〔Oscillation〕 Terminals for 32.768kHz quartz crystal oscillation.
V_{DD} V_{SS}	18 9	—	〔Power〕 V_{DD} supply terminal (+5V), V_{SS} supply terminal (0V-GND).

■TRUTH TABLE

$\overline{\text{CS0}}$	CS1	$\overline{\text{RD}}$	$\overline{\text{WR}}$	Mode	D0 to D3
L	H	L	H	Output Mode	Read Data
L	H	H	L	Input Mode	Write Data
—	—	L	L	Inhibit	—
H	—	—	—	Not Selected	Hi-Z
—	L	—	—	Not Selected	Hi-Z

Note 1) — : "H" or "L"
Note 2) Upper table is at ALE=H

■ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}	GND=0V	−0.3 to 7	V
Input voltage	V_I		GND−0.3 to V_{DD}+0.3	V
Output voltage	V_O		GND−0.3 to V_{DD}+0.3	V
Operating temperature	T_{opr}		−30 to 85	℃
Storage temperature	T_{stg}		−55 to 150	℃

■RECOMMENDED OPERATING CONDITIONS

(Ta = −30 to 85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}	—	4.5	5.0	5.5	V
Input voltage (ex. CS1)	V_{IH}	—	2.2	—	$V_{DD}+0.3$	V
	V_{IL}	—	−0.3	—	0.8	V
Input voltage (CS1)	V_{IH}	—	$V_{DD}\times0.8$	—	$V_{DD}+0.3$	V
	V_{IL}	—	−0.3	—	$V_{DD}\times0.2$	V
Time keeping source voltage	V_{CLK}	—	2.0	—	6.0	V
Crystal frequency	f_{OSC}	—	—	32.768	—	kHz

Note : Time keeping source voltage guarantee crystal oscillation and time counting.

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

(Ta = −30 to 85°C, V_{DD} = 5V ± 10%)

Parameter	Symbol	Conditions	Applicable pin	Min	Typ	Max	Unit
Input leakage current	I_{LI}	$V_I=0$ to V_{DD}	except D0 to D3	−1	—	1	μA
Input leakage current	I_{LI}		D0 to D3	−10	—	10	μA
Low level output voltage	V_{OL}	$I_{OL}=2.5mA$	D0 to D3	—	—	0.4	V
High level output voltage	V_{OH}	$I_{OH}=-400\mu A$		2.4	—	—	V
Low level output voltage	V_{OL}	$I_{OL}=2.5mA$	STD·P	—	—	0.4	V
Off state output current	I_{OZ}	$V_O=0$ to V_{DD}		−10	—	10	μA
Operating supply current	I_{DDO}	$V_{DD}=5V$, f = 32kHz	V_{DD}	—	—	10	μA

●Terminal Capacitance

(Ta = 25°C)

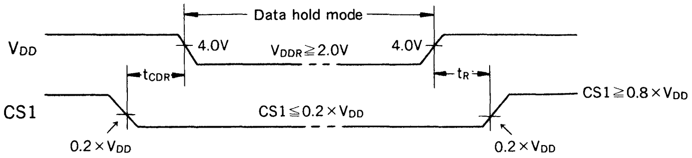
Parameter	Symbol	Conditions	Applicable pin	Min	Typ	Max	Unit
Input Capacitance	C_I	f = 1MHz	except D0 to D3	—	—	10	pF
I/O Capacitance	$C_{I/O}$	f = 1MHz	D0 to D3, STD·P	—	—	20	pF

●Data Retention Characteristic with Low Voltage Power Supply

(Ta = −30 to 85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDR}	$CS1\leqq0.2\times V_{DD}$	2.0	—	6.0	V
Data retention current	I_{DDR}	$V_{DD}=2V$, $CS1\leqq0.2\times V_{DD}$	—	—	5	μA
Chip select data hold time	t_{CDR}	See following figure	2	—	—	μs
Operation recovery time	t_R		2	—	—	μs

Data retention timing



Note : When retaining data in the stand-by mode, supply voltage can be lowered within a certain range. Read or write cycle cannot be performed while the supply voltage is low.

●AC Electrical Characteristics

○Read Mode (ALE = V_{DD} Connect)

(V_{DD}=5V±10%, V_{SS}=0V, Ta=−30 85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
CS1 setup time	$t_{SU(CS1)}$	—	1000	—	—	ns
CS1 hold time	$t_{h(CS1)}$	—	1000	—	—	ns
Address setup time before read	$t_{SU(A-R)}$	—	50	—	—	ns
Address hold time after read	$t_{h(R-A)}$	—	10	—	—	ns
RD access time	$t_{PZV(R-Q)}$	C_L=150pF	—	—	120	ns
Output floating time after read	$t_{PVZ(R-Q)}$	—	0	—	70	ns
Read recovery time	$t_{rec(R)}$	—	200	—	—	ns

○Read Mode (ALE use)

(V_{DD}=5V±10%, V_{SS}=0V, Ta=−30 to 85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
CS1 setup time	$t_{SU(CS1)}$	—	1000	—	—	ns
Address setup time before ALE	$t_{SU(A-ALE)}$	—	50	—	—	ns
Address hold time after ALE	$t_{h(ALE-A)}$	—	50	—	—	ns
ALE pulse width	$t_{W(ALE)}$	—	80	—	—	ns
ALE setup time before read	$t_{SU(ALE-R)}$	—	0	—	—	ns
ALE setup time after read	$t_{SU(R-ALE)}$	—	50	—	—	ns
RD access time	$t_{PZV(R-Q)}$	C_L=150pF	—	—	120	ns
Output floating time after read	$t_{PVZ(R-Q)}$	—	0	—	70	ns
Read recovery time	$t_{rec(R)}$	—	200	—	—	ns
CS1 hold time	$t_{h(CS1)}$	—	1000	—	—	ns

○Write Mode (ALE = V_{DD} Connect)

(V_{DD}=5V±10%, V_{SS}=0V, Ta=−30 to 85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
CS1 setup time	$t_{SU(CS1)}$	—	1000	—	—	ns
CS1 hold time	$t_{h(CS1)}$	—	1000	—	—	ns
Address setup time before write	$t_{SU(A-W)}$	—	50	—	—	ns
Address hold time after write	$t_{h(W-A)}$	—	10	—	—	ns
Write pulse width	$t_{W(W)}$	—	120	—	—	ns
Data input setup time before write	$t_{SU(D-W)}$	—	80	—	—	ns
Data input hold time after write	$t_{h(W-D)}$	—	10	—	—	ns
Write recovery time	$t_{rec(W)}$	—	200	—	—	ns

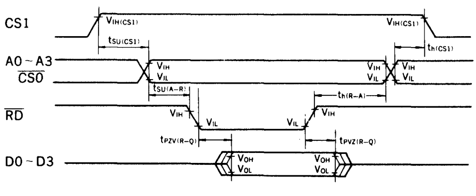
○Write Mode (ALE use)

(V_{DD}=5V±10%, V_{SS}=0V, Ta=−30 to 85°C)

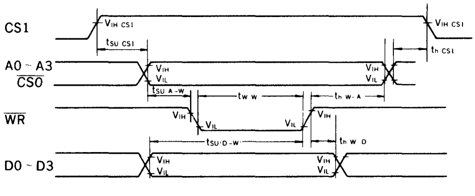
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
CS1 setup time	$t_{SU(CS1)}$	—	1000	—	—	ns
Address setup time before ALE	$t_{SU(A-ALE)}$	—	50	—	—	ns
Address hold time after ALE	$t_{h(ALE-A)}$	—	50	—	—	ns
ALE pulse width	$t_{W(ALE)}$	—	80	—	—	ns
ALE setup time before write	$t_{SU(ALE-W)}$	—	0	—	—	ns
Write pulse width	$t_{W(W)}$	—	120	—	—	ns
ALE setup time after write	$t_{SU(W-ALE)}$	—	50	—	—	ns
Data input setup time before write	$t_{SU(D-W)}$	—	80	—	—	ns
Data input hold time after write	$t_{h(W-D)}$	—	10	—	—	ns
CS1 hold time	$t_{h(CS1)}$	—	1000	—	—	ns
Write recovery time	$t_{rec(W)}$	—	200	—	—	ns

●Timing Chart

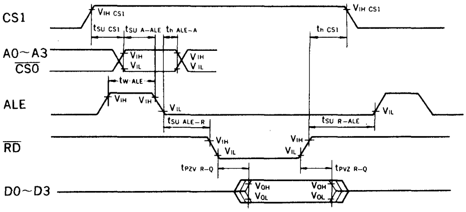
○Read Mode (ALE=V_{DD})



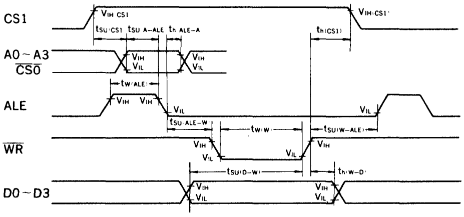
○Write Mode (ALE=V_{DD})



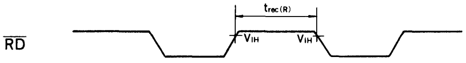
○Read Mode (ALE use)



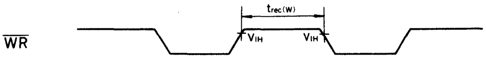
○Write Mode (ALE use)



○Read Recovery Time



○Write Recovery Time



Note : Conditions of V_{IH}, V_{IL}, V_{OH}, V_{OL} (READ MODE)

$V_{IH}=2.2V$ (ex. CS1), $V_{IH}(CS1)=\frac{4}{5}V_{DD}$, $V_{OH}=2.4V$

$V_{IL}=0.8V$ (ex. CS1), $V_{IL}(CS1)=\frac{1}{5}V_{DD}$, $V_{OL}=0.4V$

Note : Conditions of V_{IH}, V_{IL} (WRITE MODE)

$V_{IH}=2.2V$ (ex. CS1), $V_{IH}(CS1)=\frac{4}{5}V_{DD}$

$V_{IL}=0.8V$ (ex. CS1), $V_{IL}(CS1)=\frac{1}{5}V_{DD}$

■FUNCTION EXPLANATION

●Register's Function Table

Address of Registers and bit-content

Address	A3	A2	A1	A0	Name of Registers	Data				Count	Comment
						D3	D2	D1	D0		
0	0	0	0	0	Sec 1	S_8	S_4	S_2	S_1	0 to 9	1 second register
1	0	0	0	1	Sec 10	*	S_{40}	S_{20}	S_{10}	0 to 5	10 seconds register
2	0	0	1	0	Min 1	Mi_8	Mi_4	Mi_2	Mi_1	0 to 9	1 minute register
3	0	0	1	1	Min 10	*	Mi_{40}	Mi_{20}	Mi_{10}	0 to 5	10 minutes register
4	0	1	0	0	Hou 1	H_8	H_4	H_2	H_1	0 to 9	1 hour register
5	0	1	0	1	Hou 10	*	PM/AM	H_{20}	H_{10}	0 to 2 or 0 to 1	PM/AM, 10 hours register
6	0	1	1	0	Day 1	D_8	D_4	D_2	D_1	0 to 9	1 day register
7	0	1	1	1	Day 10	*	*	D_{20}	D_{10}	0 to 3	10 days register
8	1	0	0	0	Mon 1	Mo_8	Mo_4	Mo_2	Mo_1	0 to 9	1 month register
9	1	0	0	1	Mon 10	*	*	*	Mo_{10}	0 to 1	10 months register
A	1	0	1	0	Yea 1	Y_8	Y_4	Y_2	Y_1	0 to 9	1 year register
B	1	0	1	1	Yea 10	Y_{80}	Y_{40}	Y_{20}	Y_{10}	0 to 9	10 years register
C	1	1	0	0	Wee	*	W_4	W_2	W_1	0 to 6	Week Register
D	1	1	0	1	Reg D	30sec ADJ	IRQ FLAG	BUSY	HOLD	—	Control Register D
E	1	1	1	0	Reg E	t_1	t_0	ITRPT/STND	MASK	—	Control Register E
F	1	1	1	1	Reg F	TEST	24/12	STOP	RESET	—	Control Register F

Note 1) * bit : "H", "L" is writable but when read state "L" is valid only.
Note 2) BUSY bit : Output only.
Note 3) IRQ FLAG : "H", "L" is writable but "L" is valid only, when read state "H" or "L" is valid.

Data (=D0 to D3) of counter-register (=address 0 to C) has BCD code.

SMC5242C has read pin ($\overline{RD}$), write pin ($\overline{WR}$), chip selects ($\overline{CS0}$, $\overline{CS1}$), address bus and data bus, therefore usage of this IC is similar to normal RAMs.

Data bits of each register indicate the data as positive logic.

PM/AM, ITRPT/STND, 24/12, these data bits have the following table format.

	PM/AM	ITRPT/STND	24/12
H	PM	ITRPT	24
L	AM	STND	12

●**Functions of Registers** (See Block Diagram and Register's Function Table)

○ Counter-Register

The counter-register consists of a total of 13 registers with addresses from O to C.
Functions of these Registers are timekeeping (seconds, minutes, hours) and calendar (days of month, months, years, days of week).
Each counter uses BCD notation. The registers use positive logic for writing and reading on the data bus.

1) $\mathrm{Hou_1} \cdot \mathrm{Hou_{10}}$ Register (1 hour, 10 hours, PM/AM register)

These registers are used for counting hours, and are also used for operating the 12/24 hours format counting. The [24/12] use of Reg F (control register F) selects this operation.

- 24-hour operation : 0 to 23 hours counting
- 12-hour operation : AM12 to AM11 hours counting
  PM12 to PM11 hours counting

2) Year Register and Leap Year Distinction

This register is for counting years and distincting leap years automatically untill 2,099 A. D.

- Example 80, 84, 88············00 are leap years

3) Wee Register (Week Register)

This counter is constructed with limits of 0 to 6. User can set the contents of the week-register related with days of week freely.

- Setting Examples

	Sun.	Mon.	Tue.	Wed.	Thu.	Fri.	Sat.
W_1	L	H	L	H	L	H	L
W_2	L	L	H	H	L	L	H
W_4	L	L	L	L	H	H	H

○ Control-Registers

The addresses of these registers are D, E, F and these functions monitor the internal condition, such as the 30 seconds error adjustment.

1) Reg D (Register D)

a. HOLD, BUSY

HOLD bit is used with BUSY bit when data is read from and written to control-register.
BUSY is a status bit which indicate that carry is occurring or not to second-counter when HOLD bit is set to logical "H".
BUSY bit is only used for reading.

- Procedure for reading and writing data to counter or control register (except Reg. D)

HOLD bit	Status of BUSY bit	WRITE, READ	Register
H setting	H	inhibit	carry occurring
	L	able	carry not occurring*

Note : * Carry occurring to second-counter during HOLD=H, it can be corrected once automatically when HOLD bit is set "L". Be carefull to set HOLD bit to "L" immediately after writing/reading operation.

b. IRQ FLAG

This is the status bit which corresponds to the STD·P output. It is used to indicate that a request of the interrupt to the microprocessor is occurring.

- STD·P Output with IRQ FLAG (When IRQ FLAG is read)

ITRPT/STND Mode	STD·P Output	IRQ FLAG Status
H (Interrupt Mode)	L	H
	H (OPEN)	L
L (Constant-Period Output Mode)	L	H (during 7.8125ms)
	H (OPEN)	L

Note. "L" can be written to IRQ FLAG from outside and at this time STD·P output "H" (OPEN), "L" is same as upper table too.

c. 30 sec ADJ.

This bit is used for second adjusting.

- When 30 sec ADJ bit is set to "H"

  Seconds=at 30 to 59 sec.······Occurring cary to minute, Seconds become 00

  Seconds=at 01 to 29 sec.······Not occurring carry to minute, Seconds become 00

- Automatic Return of 30 sec ADJ bit

  After writing "H", this bit hold "H" during 76.3μs, then it will automatically return to "L".

  While holding "H", writing "L" and operating other registers is inhibited.

2) Reg E (Register E)

a. MASK

The MASK bit control the STD·P output

- STD·P Output with MASK bit (When "H", "L" is written to MASK bit)

ITRPT/STND Mode	MASK	STD·P Output
H (Interrupt Mode)	H	Not Become "L" (Inhibit interrupt output)
	L	Cancel MASK Operation
L (Constant-Period Output Mode)	H	Not Become "L" (7.8125ms pulse not output)
	L	Cancel MASK Operation

Note : In Interrupt mode and at IRQ FLAG=H (STD·P=L), if MASK is set to "H", STD·P will be "H" while MASK=H.
In Constant-Period Output mode, at IRQ FLAG=H (STD·P=L), if MASK is set to "H", but STD. P will not be "H", moreover 7.8125ms pulse output.

b. ITRPT/STND

This bit is used for mode selection of the STD·P output.

- STD·P output mode with ITRPT/STND bit

ITRPT/STND Writing	STD·P Output Mode	Remarks
H	Interrupt mode	—
L	Constant-period output mode	Pulse width : 7.8125ms

Note: Output period is selected by t_0, t_1 (Both mode).

c. t_0, t_1

These bits select the output period from STD·P output terminal.

- Selecting Period with t_0, t_1

			Pulse width	
t_1	t_0	period	periodical output mode	interrupt mode
L	L	1/64 second	7.8125ms	depend on usage
L	H	1 second	7.8125ms	depend on usage
H	L	1 minute	7.8125ms	depend on usage
H	H	1 hour	7.8125ms	depend on usage

Note: Output-timing at 1 second, 1 minute or 1 hour period is carry occurring timing of its counter.

3) Reg F (Register F)

a. REST

Bit for reseting that reset divider counter from 256Hz to under a second.
While "H", reseting is continual. When it is set to "L", reseting is canceled.
If CS1 is "L", this REST bit will also be "L" automatically.

b. STOP

This bit inhibits the counting into the 8,192Hz divider stage and after.
"H" write : STOP "L" write : restart

c. 24/12

"H" write : 24 hours Operation
"L" write : 12 hours Operation (with AM, PM)
Should a user changes this bit, then the data of the upper register from the hour counter will be interrupted, therefore, it will be necessary to rewrite.

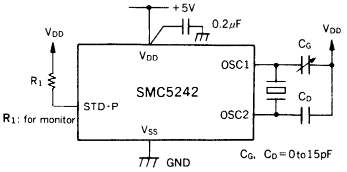
d. TEST

Please convert this terminal to "L".

■OSCILLATION CIRCUIT

Use only a quartz crystal (32.768kHz, impedance : under 30kΩ) and connect crystal to OSC1, OSC2.
In order to adjust frequency, C_G and C_D are needed as shown in the following figure, and also setting the control register is needed as shown in the following table.
C_G is used for regulating frequency.
The STD·P termimal is used for monitor purposes.

●Circuit Construction



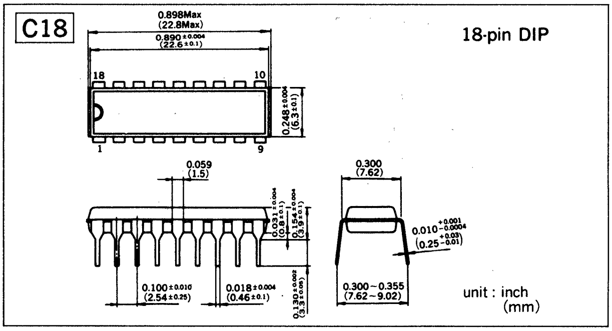
Note : If C_G, C_D are too large, when power is on at a lower temperature, the oscillation may be impossible.

●Control-Register Setting for Adjusting Frequency

	D3	D2	D1	D0
Reg D	L	L	—	L
Reg E	t_1	t_0	L	L
Reg F	L	L	L	L

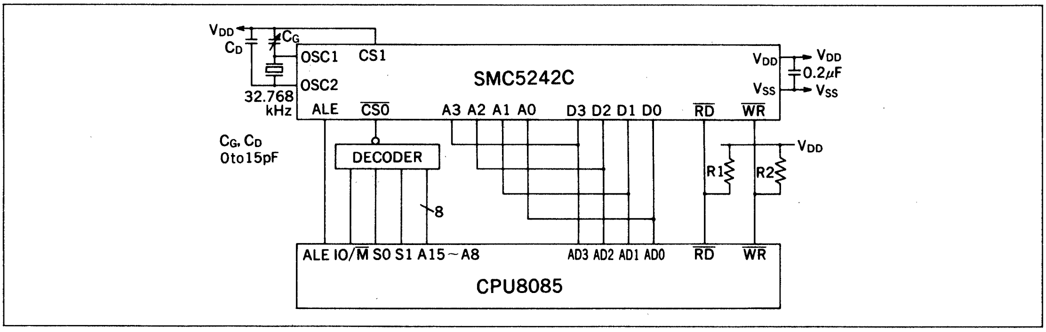
t_0, t_1 select period.

■PACKAGE DIMENSIONS

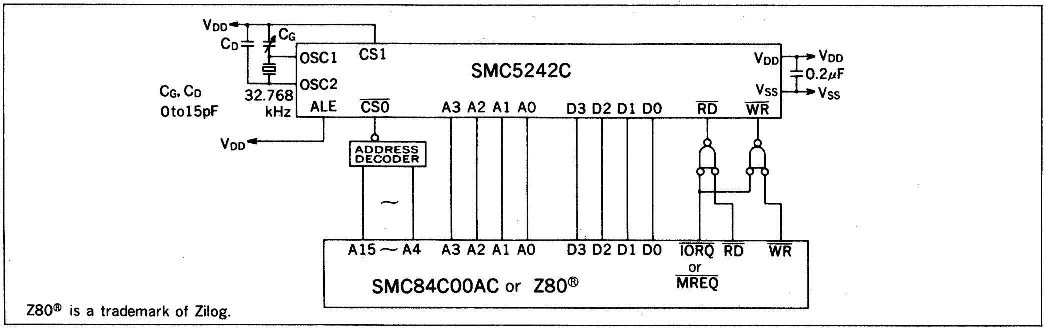


■EXAMPLE OF APPLICATION

●Using CPU 8085



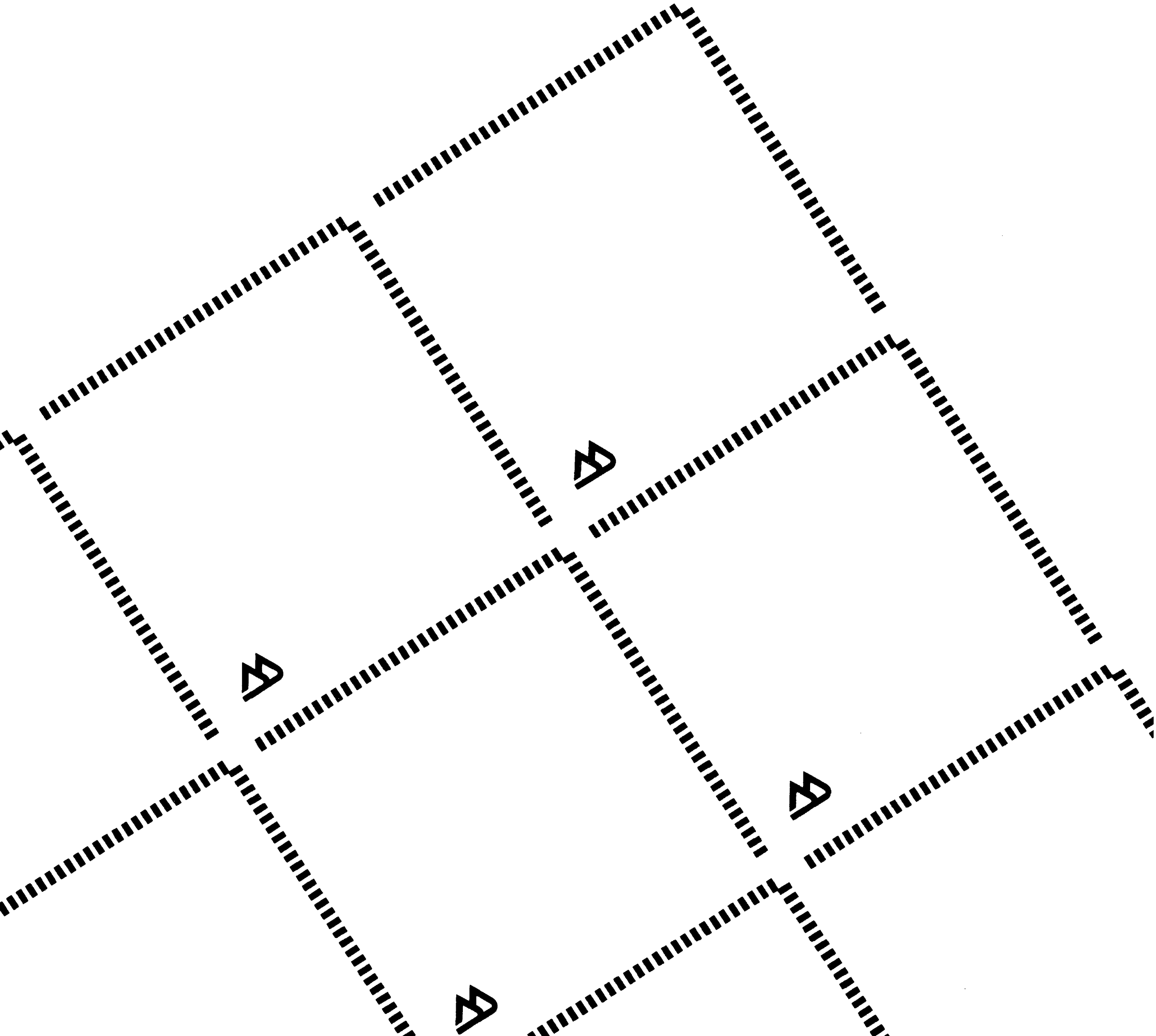
●Using SMC84C00AC or Z80®



Z80® is a trademark of Zilog.

1988/1989 CMOS DATA BOOK

D. GATE ARRAYS/STANDARD CELLS



SLA100L Series

CMOS LOW VOLTAGE GATE ARRAY

●Low Voltage Operation··0.9V Min to 6.0V Max

●CMOS I/O Compatible

●Gate Densities From 1,600 to 8,000 Gates

■DESCRIPTION

The SLA100L Series is a CMOS master slice, low voltage gate array fabricated using a low threshold process. It includes six models, with a gate capacity range of 1,600 to 8,000 gates.

The low voltage design enables this series to operate from a single 1.5V or 3V battery. It is well suited for portable products and standard 5V applications.

The SLA100L Series is also available with MSI cell libraries and can be designed with the same tools as the SLA6000 and SLA7000 Series.

■FEATURES

- ●Low voltage operation······························0.9V Min (Operating voltage: 0.9 to 6.0V)
- ●Six models covering a gate capacity of 1,600 to 8,000 gates
- ●Suitable for portable product applications
- ●Short turn-around time

■SLA100L SERIES

Series / Parameter		SLA116L	SLA122L	SLA134L	SLA149L	□ SLA162L	□ SLA180L
Gates (2-input NAND)		1,632	2,232	3,432	4,900	6,210	8,000
Technology		SILICON GATE CMOS 2 LAYER METALLIZATION					
I/O level		CMOS					
Delay time	Internal gate	8.5ns (1.5V Standard) 3.0ns (3.0V Standard)					
	Input buffer	12.0ns (1.5V Standard) 4.0ns (3.0V Standard)					
	Output buffer	40.0ns (1.5V Standard) 14.0ns (3.0V Standard) $C_L=15$pF					
Coefficient of delay		For the SLA100L Series, the coefficient of delay is the typical value with $V_{DD}=1.5$V in the MSI cell library, multiplied by the maximum and minimum coefficients at the minimum and maximum operating voltages. For the applicable coefficient, contact us.					
Total ports for I/O		70	82	104	128	150	170
Total ports for Power/GND (Max)		8	8	8	8	8	8
Output mode		Normal, Open-drain, 3-state, Bi-directional					

□: Under development

■ABSOLUTE MAXIMUM RATINGS

($V_{SS}=0V$)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.3 to 6.5	V
Input voltage	V_I	−0.3 to $V_{DD}+0.3$	V
Output voltage	V_O	−0.3 to $V_{DD}+0.3$	V
Storage temperature	T_{stg}	−65 to 150	℃

■RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}	1.5V (Standard)	1.35	1.50	1.65	V
	V_{DD}	3V (Standard)	2.70	3.00	3.30	V
Operating voltage	V_{DD}		0.90	—	6.00	V
Operating temperature	T_{opr}		0	—	70	℃

■ELECTRICAL CHARACTERISTICS

(Ta=0 to 70℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply current	I_{DD}	Stand-by, $V_{DD}=1.5V$	—	—	2.0	μA
	I_{DD}	Stand-by, $V_{DD}=3.0V$	—	—	2.0	μA
High level output voltage	V_{OH}	$V_{DD}=1.5V$, $I_{OH}=-0.23mA$	1.3	—	—	V
	V_{OH}	$V_{DD}=3.0V$, $I_{OH}=-0.6mA$	2.7	—	—	V
Low level output voltage	V_{OL}	$V_{DD}=1.5V$, $I_{OL}=0.7mA$	—	—	0.2	V
	V_{OL}	$V_{DD}=3.0V$, $I_{OL}=1.7mA$	—	—	0.3	V
High level input voltage	V_{IH}	$V_{DD}=1.5V$	1.1	—	—	V
	V_{IH}	$V_{DD}=3.0V$	2.0	—	—	V
Low level input voltage	V_{IL}	$V_{DD}=1.5V$	—	—	0.4	V
	V_{IL}	$V_{DD}=3.0V$	—	—	1.0	V
Input leakage current	I_{LI}		−200	—	200	nA

■PACKAGE LIST

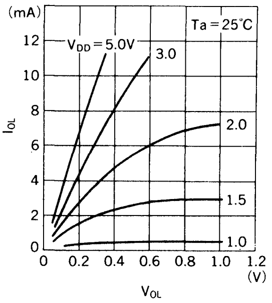
Type	Pin No.	Package name	SLA116L	SLA122L	SLA134L	SLA149L	SLA162L	SLA180L
Plastic DIP	28pin	C28	○	○	○	□		
	40pin	C40	○	○	□	□		
	42pin	C42	□	○	○	□		
Plastic shrink DIP	64pin	S64	○	○	○	○	○	
Plastic QFP	44pin	F44-2	○	○	○			
	60pin	F60-2	□	○	○	○	○	
	60pin	F60-5	○	□	○	○	□	
	64pin	F64-5	□	□	□	□	□	
	80pin	F80-5	○	○	○	○	○	
	100pin	F100-5		○	○	○	○	
	128pin	F128-8			○	○	○	○
	144pin	F144-8					○	○
	160pin	F160-8				○	○	○
Plastic PGA	89pin	G89		□	□	□	□	
	132pin	G132		□	□	□	□	□
	176pin	G176					□	□
	208pin	G208						□
PLCC	44pin	J44	□	○	○	○	○	
	68pin	J68	□	○	○	○	○	
	84pin	J84				○	○	○
Ceramic PGA	72pin	P72		□	○	○	○	
	132pin	P132		□	○	○	○	○
	176pin	P176					□	□
	208pin	P208						□

○: Available, □: Under development

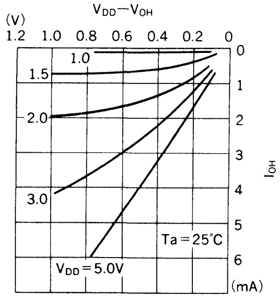
■PERFORMANCE CURVES

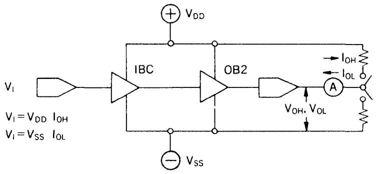
●Output Current

$I_{OL}-V_{OL}$



$(V_{DD}-V_{OH})-I_{OH}$

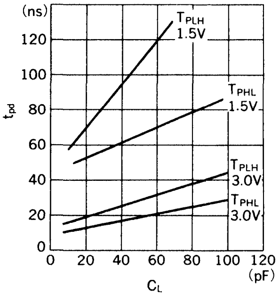




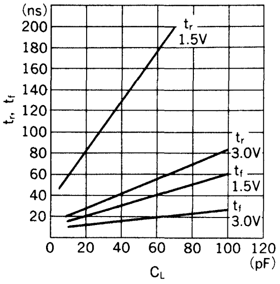
Measuring Circuit

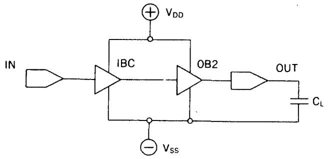
●t_{pd}, t_r, t_f-C_L

$t_{pd}-C_L$

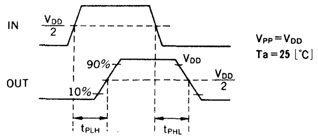


t_r, t_f-C_L



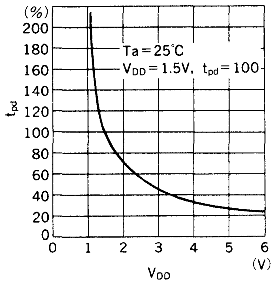


Measuring Circuit

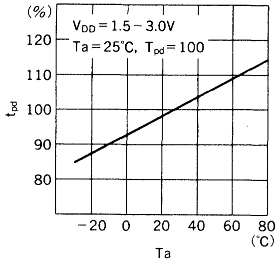


●Delay Time, Power Dissipation

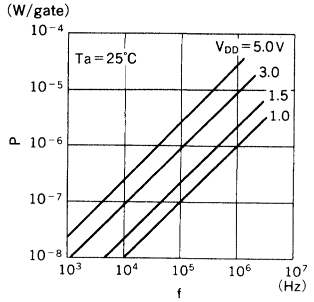
$t_{pd}-V_{DD}$



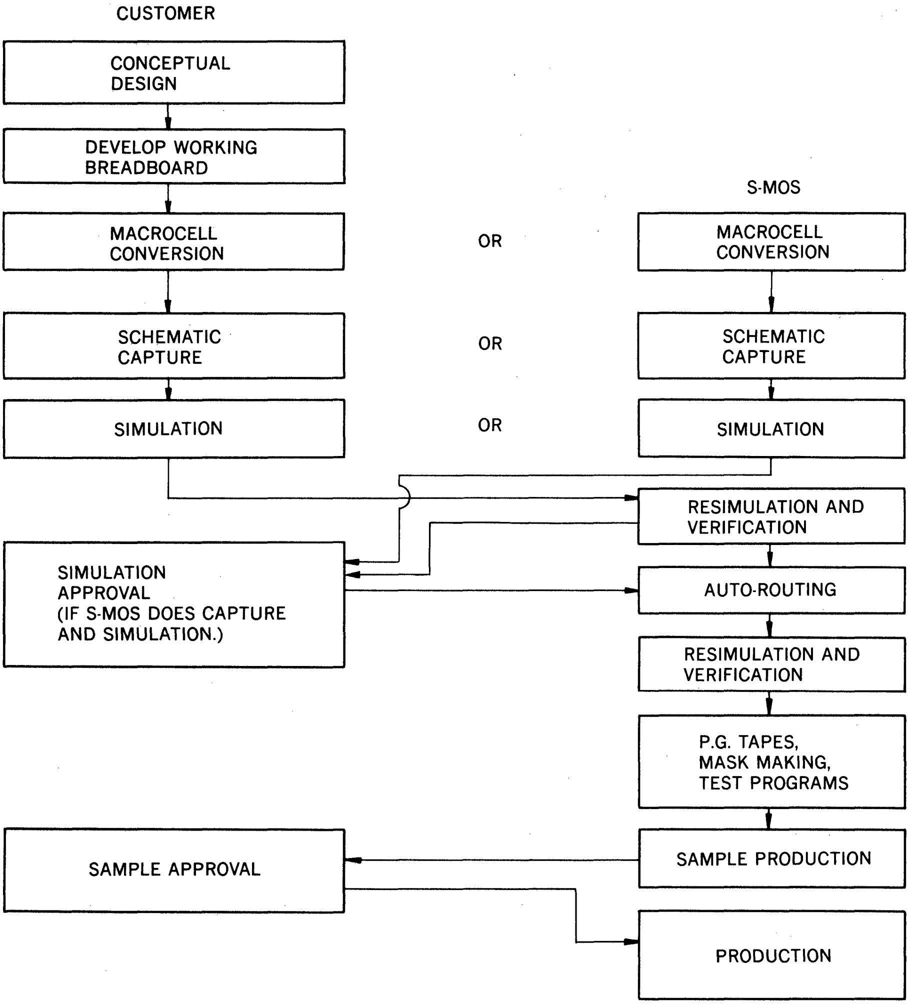
$t_{pd}-Ta$



P−f



■ GATE ARRAY DESIGN FLOW



SLA6000Series

CMOS HIGH SPEED GATE ARRAY

- **2 Micron Dual Layer Metal**
- **8 Sizes**
- **Fast Design Cycle**

■ DESCRIPTION

The SLA6000 Series consists of a group of 8 CMOS Gate arrays with gate counts from 513 to 6,206 gates. The series is fabricated utilizing our 2 micron high speed CMOS silicon gate technology to achieve propagation delays of 1.8ns for the internal gates and 3ns-8ns for the I/O buffers. All I/O buffers are TTL and CMOS compatible which make this series an ideal choice for replacing existing discrete logic as well as for new designs.

■ FEATURES

- High speed silicon gate CMOS technology
- TTL and CMOS I/O compatible
- High output drivercapability
- Gate densities from 513 to 6,206 gates
  "Hard" MSI macrocells for superior AC performance
- Cell libraries, software, and documentation available for IBM® PC compatibles with Future Net or OrCAD and Daisy and Mentor systems

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■ SLA 6000

Parameter \ Series		SLA6050	SLA6080	SLA6140	SLA6170	SLA6270	SLA6330	SLA6430	SLA6620
Gates (2-input NAND)		513	820	1,394	1,746	2,667	3,312	4,342	6,206
Technology		SILICON GATE CMOS 2 LAYER METALLIZATION							
I/O level		TTL, CMOS							
Delay time	Internal gate *1	1.8ns (standard)							
	Input buffer *1, *2	t_{pLH} = 3 ns, t_{pHL} = 4 ns (standard)							
	Output buffer *2	t_{pLH} = 6 ns, t_{pHL} = 8 ns (standard) C_L=30pF							
Total ports for I/O (Terminals only for input port)		48 (6)	60 (6)	74 (6)	82 (6)	100 (6)	110 (6)	126 (6)	154 (8)
Output mode		Normal, Open-drain, 3-state, Bi-directional							

*1 Typical fanout 2, 1 mm of interconnect
*2 Standard I/O cell

■ ABSOLUTE MAXIMUM RATINGS

($V_{SS}=0$ V)

Parameter	Symbol	Ratings	Unit
Supply Voltage	V_{DD}	−0.3 to 7.0	V
Input Voltage	V_I	−0.3 to $V_{DD}+0.3$	V
Output Voltage	V_O	−0.3 to $V_{DD}+0.3$	V
Storage Temperature	T_{stg}	−65 to 150	°C

■ RECOMMENDED OPERATING CONDITIONS

($V_{SS}=0$V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	—	4.75	5.00	5.25	V
Operating Temperature	T_{opr}	—	0	—	70	°C

■ ELECTRICAL CHARACTERISTICS

($V_{DD}=5$V±5%, $V_{SS}=0$V, Ta=0 to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Current	I_{DD}	Standby	—	2	—	μA
High level output voltage	V_{OH}	$V_{DD}=4.75$ V $I_{OH}=-6$ mA	2.4	—	—	V
Low level output voltage	V_{OL}	$V_{DD}=4.75$ V $I_{OL}=6$ mA	—	—	0.4	V
High level input voltage	V_{IH}	$V_{DD}=5.25$ V	2.0	—	—	V
Low level input voltage	V_{IL}	$V_{DD}=4.75$ V	—	—	0.8	V
Input leakage current	I_{LI}	—	−1	—	1	μA

■ PACKAGE LIST

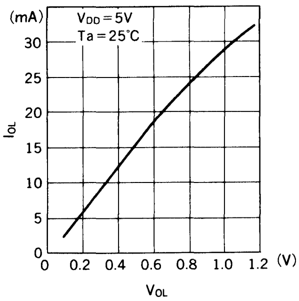
Type	Pin No.	Package name	SLA6050	SLA6080	SLA6140	SLA6170	SLA6270	SLA6330	SLA6430	SLA6620
Plastic DIP	14pin	C14	○	○						
	16pin	C16	○	○						
	18pin	C18	○	○						
	24pin	C24	○	○	○	○				
	28pin	C28	○	○	○	○	○			
	40pin	C40	○	○	○	○	○			
	42pin	C42	○	○	○	○	○			
Plastic QFP	44pin	F44-2		○	○	○	○			
	46pin	F46-5	○	○	○	○	○	○	○	
	60pin	F60-2	○	○	○	○	○	○		
	60pin	F60-5	○	○	○	○	○	○	○	
	80pin	F80-5			○	○	○	○	○	
	100pin	F100-5				○	○	○	○	
Ceramic QFP	148pin	H148						○	○	○
Plastic SOP	24pin	M24	○	○	○					
	28pin	M28-2		○	○					
Shrink DIP	28pin	S28		○						
	42pin	S42								
	64pin	S64			○	○	○			
Ceramic PGA	64pin	P64			○	○	○	○		
	72pin	P72				○	○	○		
	132pin	P132					○	○	○	○
PLCC	44pin	J44	○	○	○	○	○	○	○	
	68pin	J68			○	○	○	○	○	○
	84pin	J84				○	○	○	○	○

○ : Available

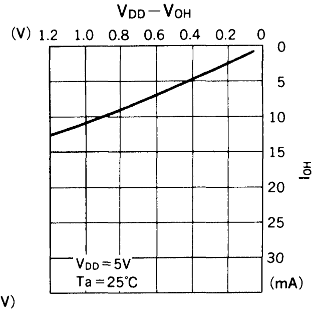
■ PERFORMANCE CURVES

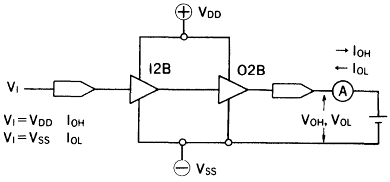
● Output Current

I_{OL}—V_{OL}



(V_{DD}—V_{OH})—I_{OH}

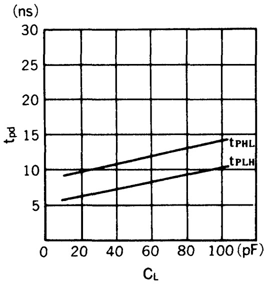




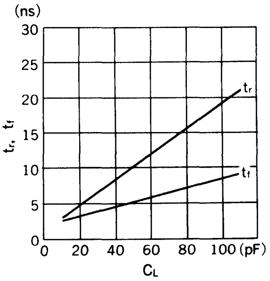
Measuring Circuit

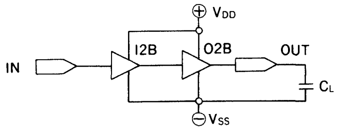
● t_{pd}, t_r, t_f—C_L

t_{pd} − C_L

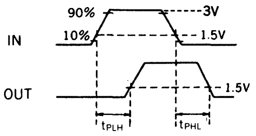


t_r, t_f − C_L





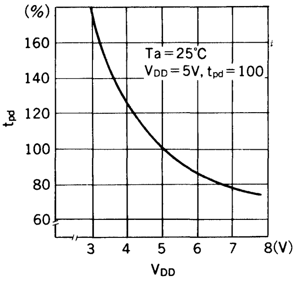
Measuring Circuit



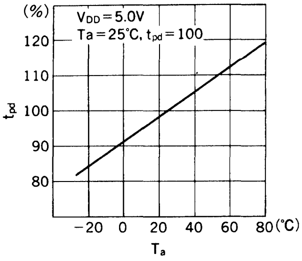
V_{PP} = 3 [V]
t_r, t_f = 10 [ns]
V_{DD} = 5 [V]
Ta = 25 [°C]

● Delay Time

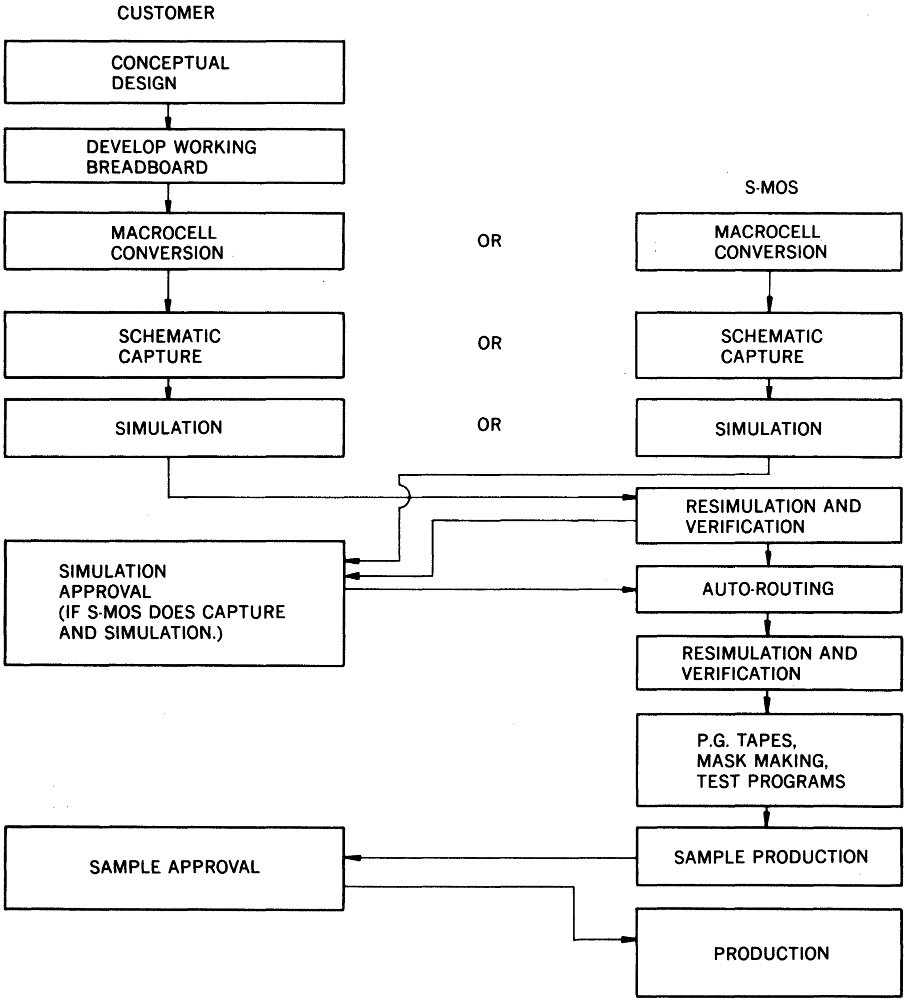
t_{pd}—V_{DD}



t_{pd}—T_a



■ GATE ARRAY DESIGN FLOW



SLA7000Series

CMOS HIGH SPEED GATE ARRAY

- **1.5 Micron Dual Layer Metal**
- **7 Sizes**
- **Fast Design Cycle**
- **Bipolar Speeds**

■DESCRIPTION

The SLA7000 series consists of a group of 6 CMOS gate arrays with gate counts from 1,632 to 16,250 gates. The series is fabricated utilizing our 1.5 micron high speed CMOS silicon gate technology to achieve propagation delays of 1.0ns for the internal gates. All I/O buffers are TTL and CMOS compatible which makes this series an ideal choice for replacing existing discrete logic as well as for new designs requiring very high speed and/or high gate counts.

■FEATURES

- Very high speed silicon gate CMOS technology
- TTL and CMOS I/O compatible
- High output drivercapability
- Gate densities from 1,632 to 16,250 gates
- "Hard" MSI macrocells for superior AC performance
- Cell libraries, software, and documentation available for IBM® PC compatibles with Future Net or OrCAD and Daisy and Mentor systems

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■SLA7000 SERIES

Parameter \ Series		SLA7160	SLA7220	SLA7340	SLA7490	SLA7620	SLA7800	SLA790S*3
Gates (2-input NAND)		1,632	2,232	3,432	4,900	6,210	8,000	16,250
Technology		SILICON GATE CMOS 2 LAYER METALLIZATION						
I/O level		TTL, CMOS						
Delay time	Internal gate *1	1.0ns						
	Input buffer *1, *2	tp_{LH}=1.9ns, tp_{HL}=3.4ns						
	Output buffer *2	tp_{LH}=5.5ns, tp_{HL}=4.7ns, C_L=30pF						
Total ports for I/O		70	82	104	128	150	170	188
Total ports for Power/GND (Max)		8	8	8	8	8	8	8
Output mode		Normal, Open-drain, 3-state, Bi-directional						

*1 Typical fanout of 2, 1mm of interconnect.
*2 Standard I/O cell.
*3 Sea of Gates (approx 8K usable gates.)

■ABSOLUTE MAXIMUM RATINGS

($V_{SS}=0V$)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.3 to 7.0	V
Input voltage	V_I	−0.3 to $V_{DD}+0.3$	V
Output voltage	V_O	−0.3 to $V_{DD}+0.3$	V
Storage temperature	T_{stg}	−65 to 150	℃

■RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}	—	4.75	5.00	5.25	V
Operating temperature	T_{opr}	—	0	—	70	℃

■ELECTRICAL CHARACTERISTICS

($V_{DD}=5V\pm5\%$, Ta=0 to 70℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply current	I_{DD}	Standby	—	2	—	μA
High level output voltage	V_{OH}	$V_{DD}=4.75V$ $I_{OH}=-6mA$	2.4	—	—	V
Low level output voltage	V_{OL}	$V_{DD}=4.75V$ $I_{OL}=6mA$	—	—	0.4	V
High level input voltage	V_{IH}	$V_{DD}=5.25V$	2.0	—	—	V
Low level input voltage	V_{IL}	$V_{DD}=4.75V$	—	—	0.8	V
Input leakage current	I_{LI}	—	−1	—	1	μA

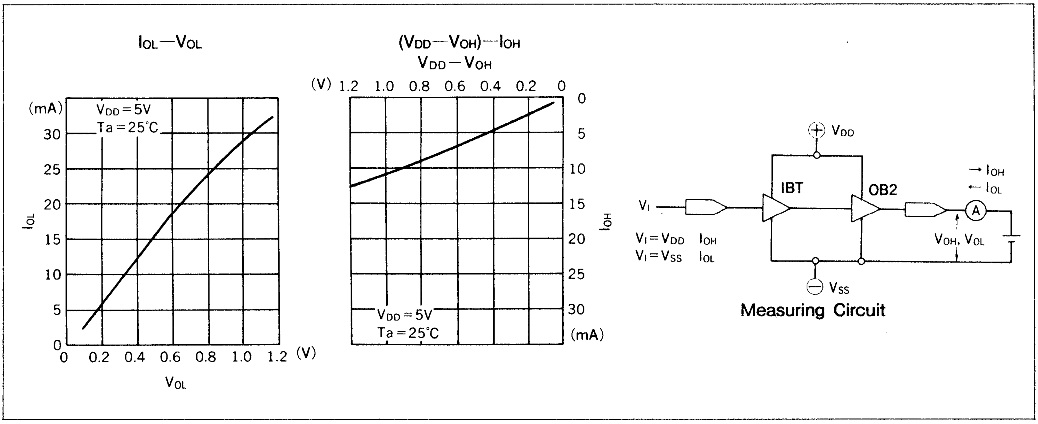
■PACKAGE TYPES

Type	Pin No.	Package name	SLA7160	SLA7220	SLA7340	SLA7490	SLA7620	SLA7800	SLA790S
Plastic DIP	28pin	C28	○	○	○	□			
	40pin	C40	○	○	□	□			
	42pin	C42	□	○	○	□			
Plastic shrink DIP	64pin	S64	○	○	○	○	○		
Plastic QFP	44pin	F44-2	○	○	○				
	60pin	F60-2	□	○	○	○	○		
	60pin	F60-5	○	□	○	○	□		
	64pin	F64-5	□	□	□	□	□		
	80pin	F80-5	○	○	○	○	○		
	100pin	F100-5		○	○	○	○		
	128pin	F128-8			○	○	○	○	○
	144pin	F144-8					○	○	○
	160pin	F160-8				○	○	○	○
Plastic PGA	89pin	G89		□	□	□	□		
	132pin	G132		□	□	□	□	□	□
	176pin	G176					□	□	□
	208pin	G208						□	□
PLCC	44pin	J44	□	○	○	○	○		
	68pin	J68	□	○	○	○	○		
	84pin	J84				○	○	○	○
Ceramic PGA	72pin	P72		□	○	○	○		
	132pin	P132		□	○	○	○	○	○
	176pin	P176					□	□	□
	208pin	P208						□	□

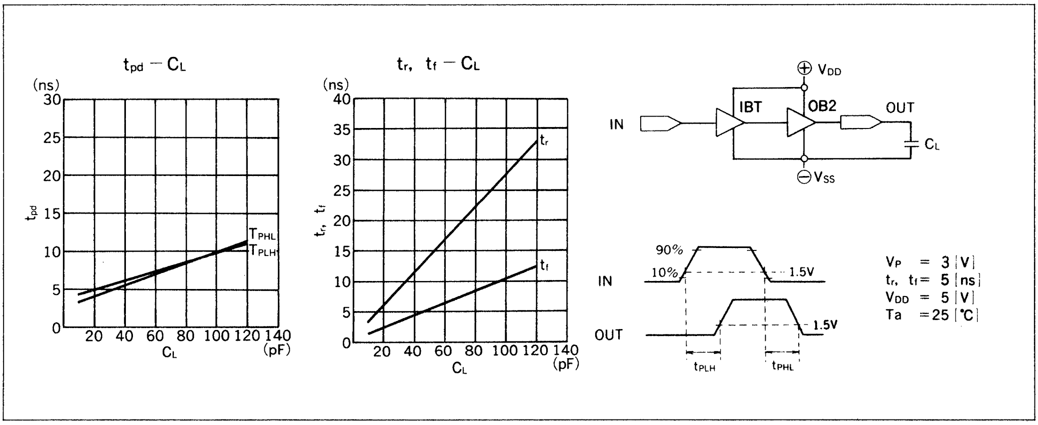
○ : Available □:Under Development

■PERFORMANCE CURVES

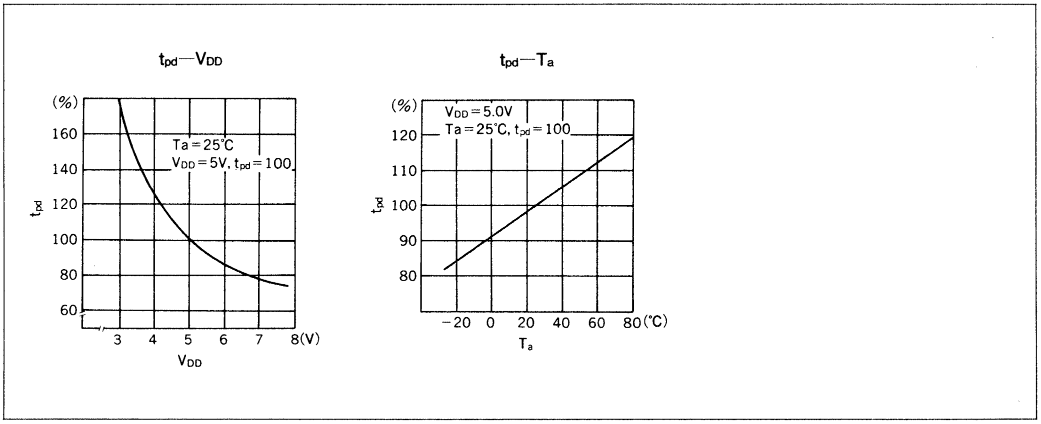
●Output Current



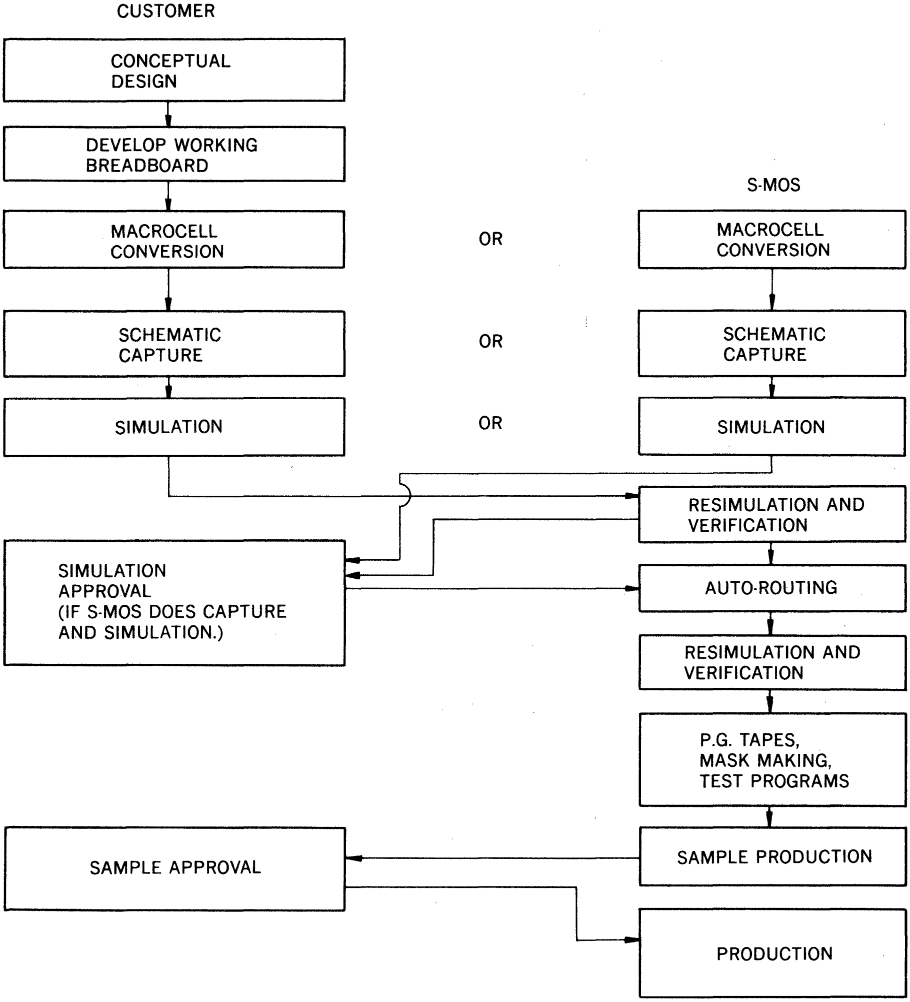
●t_{pd}, t_r, t_f—C_L



●Delay Time



GATE ARRAY DESIGN FLOW



SLA700B Series

CMOS HIGH SPEED & HIGH OUTPUT GATE ARRAY

- **High Output Drive Capability**
- **Adaptable to CMOS and STTL Applications**
- **TTL and CMOS I/O Compatible**
- **Gate Densities from 800 to 2,400 Gates**

■DESCRIPTION

The SLA700B series is a multi-pin, high output CMOS gate array, an enhanced version of the SLA7000 series. The series is fabricated using our advanced 1.5 micron CMOS technology and can deliver up to 24mm I_{OL}.

■FEATURES

- Multiple I/O pin configuration
- High output drive capability (I_{OL}=24mA)
- Very high speed operation (typical delay time: 1.0ns)
- Adaptable to CMOS and STTL applications
- Library compatibility with our SLA7000 series
- Cell libraries, software, and documentation available for IBM® PC compatibles with Future Net or OrCAD and Daisy and Mentor systems

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■SLA700B SERIES

Parameter \ Series		SLA708B	SLA715B	SLA724B
Gates (2-input NAND)		825	1,500	2,482
Technology		SILICON GATE CMOS 2 LAYER METALLIZATION		
I/O level		TTL, CMOS		
Delay time	Internal gate *1	1.0ns		
	Input buffer *1, *2	tp_{LH}=1 9ns, tp_{HL}=3.4ns		
	Output buffer *2	tp_{LH}=5.5ns, tp_{HL}=4.7ns C_L=30pF		
Total ports for I/O		84	100	122
Total ports for Power/GND (Max)		8 (16)	8 (16)	8 (16)
Output mode		Normal, Open-drain, 3-state, Bi-directional		

*1 Typical fanout 2, lmm of interconnect
*2 Standard I/O cell

■ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.3 to 7.0	V
Input voltage	V_I	−0.3 to V_{DD}+0.3	V
Output voltage	V_O	−0.3 to V_{DD}+0.3	V
Storage temperature	T_{stg}	−65 to 150	°C

■RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}	—	4.75	5.00	5.25	V
Operating temperature	T_{opr}	—	0	—	70	°C

■ELECTRICAL CHARACTERISTICS

(V_{DD}=5V±5%, Ta=0 to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply current	I_{DD}	Standby	—	2	—	μA
High level output voltage	V_{OH}	V_{DD}=4.75V I_{OH}=−24mA	2.4	—	—	V
Low level output voltage	V_{OL}	V_{DD}=4.75V I_{OL}=24mA	—	—	0.4	V
High level input voltage	V_{IH}	V_{DD}=5.25V	2.0	—	—	V
Low level input voltage·	V_{IL}	V_{DD}=4.75V	—	—	0.8	V
Input leakage current	I_{LI}	—	−1	—	1	μA

■PACKAGE LIST

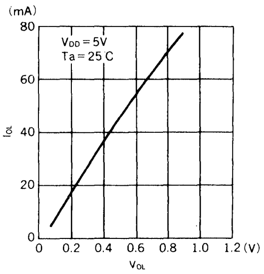
Type	Pin No.	Package name	SLA708B	SLA715B	SLA724B
Plastic DIP	28pin	C28			
	40pin	C40			
	42pin	C42			
Plastic shrink DIP	64pin	S64	○	○	○
Plastic QFP	44pin	F44-2			
	60pin	F60-2			
	60pin	F60-5			
	64pin	F64-5			
	80pin	F80-5	○	○	○
	100pin	F100-5	○	○	○
	128pin	F128-8		○	□
	144pin	F144-8			□
	160pin	F160-8			
Plastic PGA	89pin	G89	□	□	□
	132pin	G132	□	□	□
	176pin	G176			
	208pin	G208			
PLCC	44pin	J44			
	68pin	J68	○	○	○
	84pin	J84	○	○	○
Ceramic PGA	72pin	P72	□	□	□
	132pin	P132	○	○	○
	176pin	P176			
	208pin	P208			

○: Available □: Under development

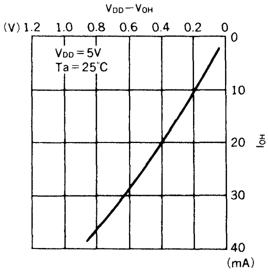
■PERFORMANCE CURVES

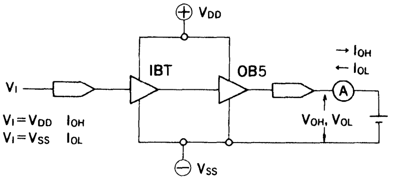
●Output Current

I_{OL}—V_{OL}



(V_{DD}—V_{OH})—I_{OH}

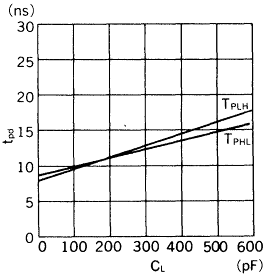




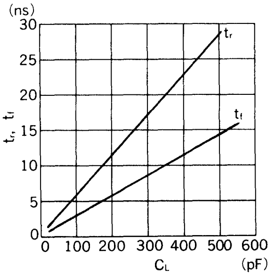
Measuring Circuit

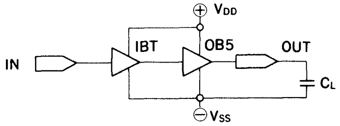
●t_{pd}, t_r, t_f—C_L

t_{pd}—C_L

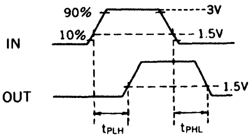


t_r, t_f—C_L





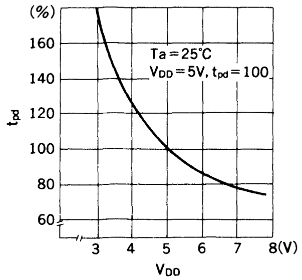
Measuring Circuit



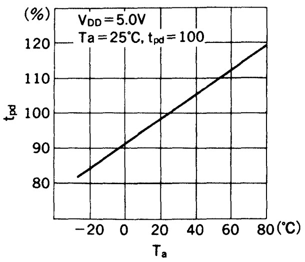
V_{PP} = 3 [V]
t_r, t_f = 5 [ns]
V_{DD} = 5 [V]
Ta = 25 [°C]

●Delay Time

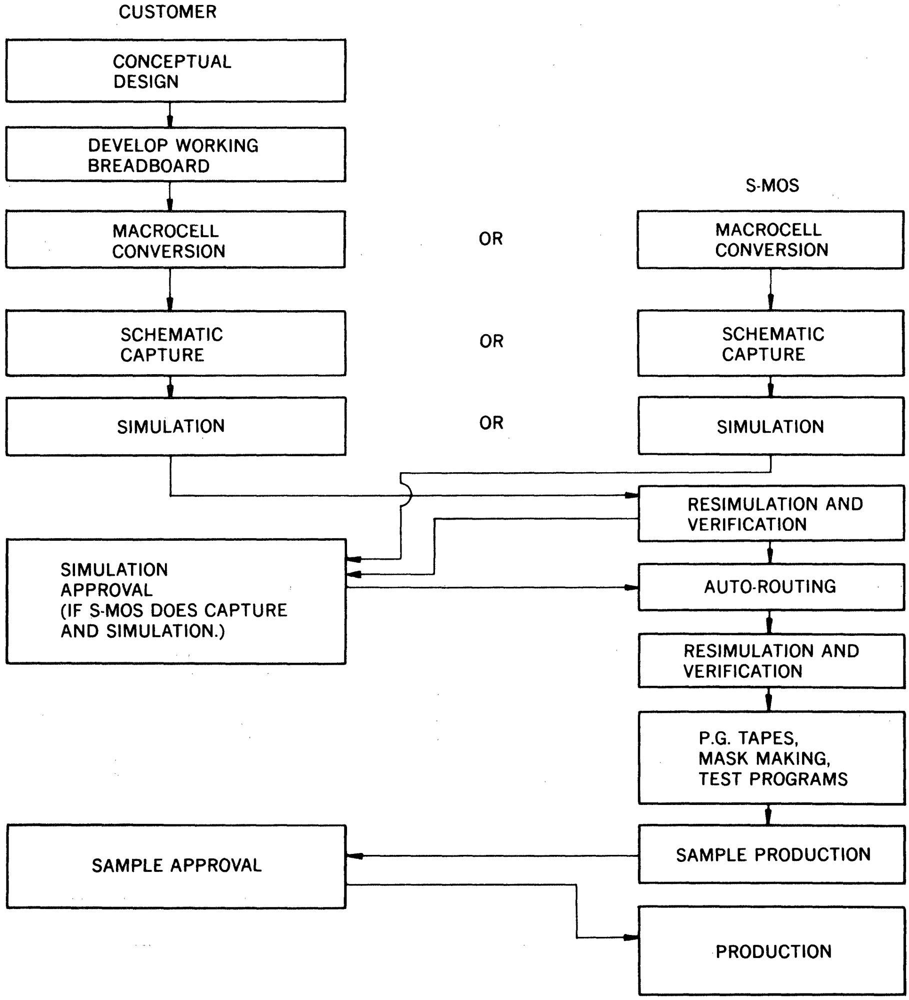
t_{pd}—V_{DD}



t_{pd}—Ta



GATE ARRAY DESIGN FLOW



SLA8000Series

CMOS HIGH SPEED GATE ARRAY

- **High Speed Silicon Gate CMOS Technology**
- **TTL and CMOS I/O Compatible**
- **High Output Drive Capability**
- **Gate Densities From 5,304 to 38,550 Gates (Sea of Gates)**

DESCRIPTION

The SLA8000 Series is a super-high-speed, densely-packaged master slice CMOS gate array (sea of gates). The SLA8000 Series comes in seven models. They can accommodate up to 16K usable gates to meet a variety of logical design requirements in special processor and controller applications.

FEATURES

- Super-high speed: t_{pd} (typ) = 0.8ns/gate
- High performance applicable to LSTTL application area
- 24mA (Max) current available with 3 I/O cell in parallel
- Input cells and Bi-directional cells are provided with pull-up/pull-down resistor
- SRAM, ROM cells library are available
- Mega-cells capability
- Gate densities from 5,304 to 38,550 gates
- Actual ability for routing: 40 to 50% of total gates.

SLA8000 SERIES

Parameter \ Series		SLA827S	SLA847S	SLA872S	SLA890S	SLA8B3S	SLA8F0S	SLA8J3S
Gates (2-input NAND)		5,304	9,416	14,336	18,300	22,680	30,000	38,550
Technology		SILICON GATE CMOS 2 LAYER METALLIZATION, SEA OF GATES						
I/O level		TTL, CMOS						
Delay time	Internal gate *1	0.8ns (Typ)						
	Input buffer *1, *2	1.4ns (Typ)						
	Output buffer *2	3.5ns (Typ) $C_L = 15pF$						
Total ports for I/O		82	108	136	152	168	194	222
Total ports for Power/GND (Max)		4	4	4	4	4	4	4
Output mode		Normal, Open-drain, 3-state, Bi-directional						

*1 Typical fanout of 2, lmm of interconnect
*2 Standard I/O cell.

■ABSOLUTE MAXIMUM RATINGS

($V_{SS}=0V$)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.3 to 7.0	V
Input voltage	V_I	−0.3 to $V_{DD}+0.3$	V
Output voltage	V_O	−0.3 to $V_{DD}+0.3$	V
Storage temperature	T_{stg}	−65 to 150	℃

■RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}	—	4.75	5.00	5.25	V
Operating temperature	T_{opr}	—	0	—	70	℃

■ELECTRICAL CHARACTERISTICS

($V_{DD}=5V\pm5\%$, Ta=0 to 70℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply current	I_{DD}	Stand-by	—	2	—	μA
High level output voltage	V_{OH}	$V_{DD}=4.75V$ $I_{OH}=-6mA$	2.4	—	—	V
Low level output voltage	V_{OL}	$V_{DD}=4.75V$ $I_{OL}=6mA$	—	—	0.4	V
High level input voltage	V_{IH}	$V_{DD}=5.25V$	2.0	—	—	V
Low level input voltage	V_{IL}	$V_{DD}=4.75V$	—	—	0.8	V
Input leakage current	I_{LI}	—	−1	—	1	μA

■PACKAGE LIST

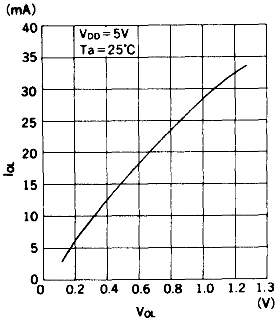
Type	Pin No.	Package Name	SLA827S	SLA847S	SLA872S	SLA890S	SLA8B3S	SLA8F0S	SLA8J3S
Plastic DIP	28pin	C28	○	○	□				
	40pin	C40	○	□	□				
	42pin	C42	○	○	□				
Plastic shrink DIP	64pin	S64	○	○	○	○	○		
Plastic QFP	44pin	F44-2	○	○	□	□	□		
	60pin	F60-2	□	○	○	○	○		
	60pin	F60-5	○	○	○	□	□		
	64pin	F64-5	□	□	□	□	□		
	80pin	F80-5	○	○	○	○	○		
	100pin	F100-5	○	○	○	○	○	□	
	128pin	F128-8			□	□	○	○	□
	144pin	F144-8			□	□	○	○	○
	160pin	F160-8					○	○	○
	196pin	F196-9					□	□	□
	230pin	F230-9						□	□
Plastic PGA	89pin	G89	□	□	□	□	□		
	132pin	G132	□	□	□	□	□	□	
	176pin	G176					□	□	□
	208pin	G208						□	□
	240pin	G240					□	□	□
PLCC	44pin	J44	○	○	○	○	○		
	68pin	J68	○	○	○	○	○		
	84pin	J84	○		○	○	○	○	
	132pin	J132							□
Ceramic PGA	132pin	P132	□	○	○	○	○	○	
	176pin	P176					□	□	□
	208pin	P208						□	□

○ : Available　□ : Under development

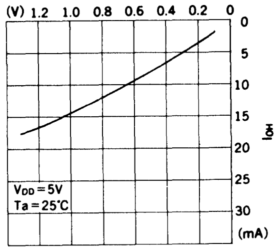
■PERFORMANCE CURVES

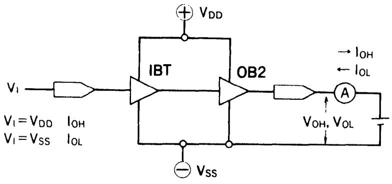
●Output Current

I_{OL}—V_{OL}



I_{OH}—(V_{DD}—V_{OH})

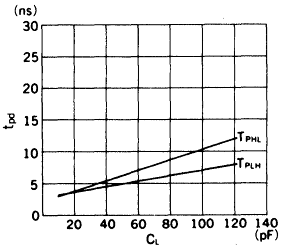




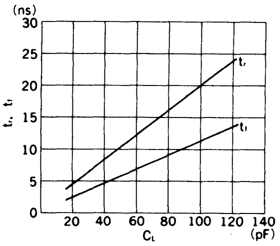
Measuring Circuit

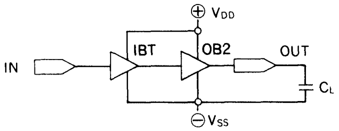
●t_{pd}, t_r, t_f—C_L

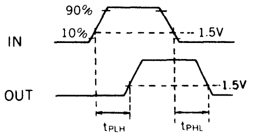
t_{pd} — C_L



t_r, t_f — C_L



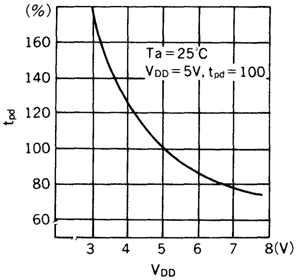




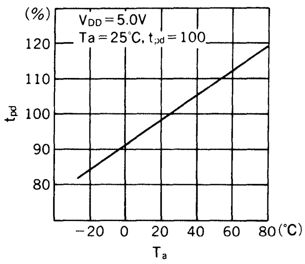
V_P = 3 [V]
t_r, t_f = 5 [ns]
V_{DD} = 5 [V]
Ta = 25 [°C]

●Delay Time

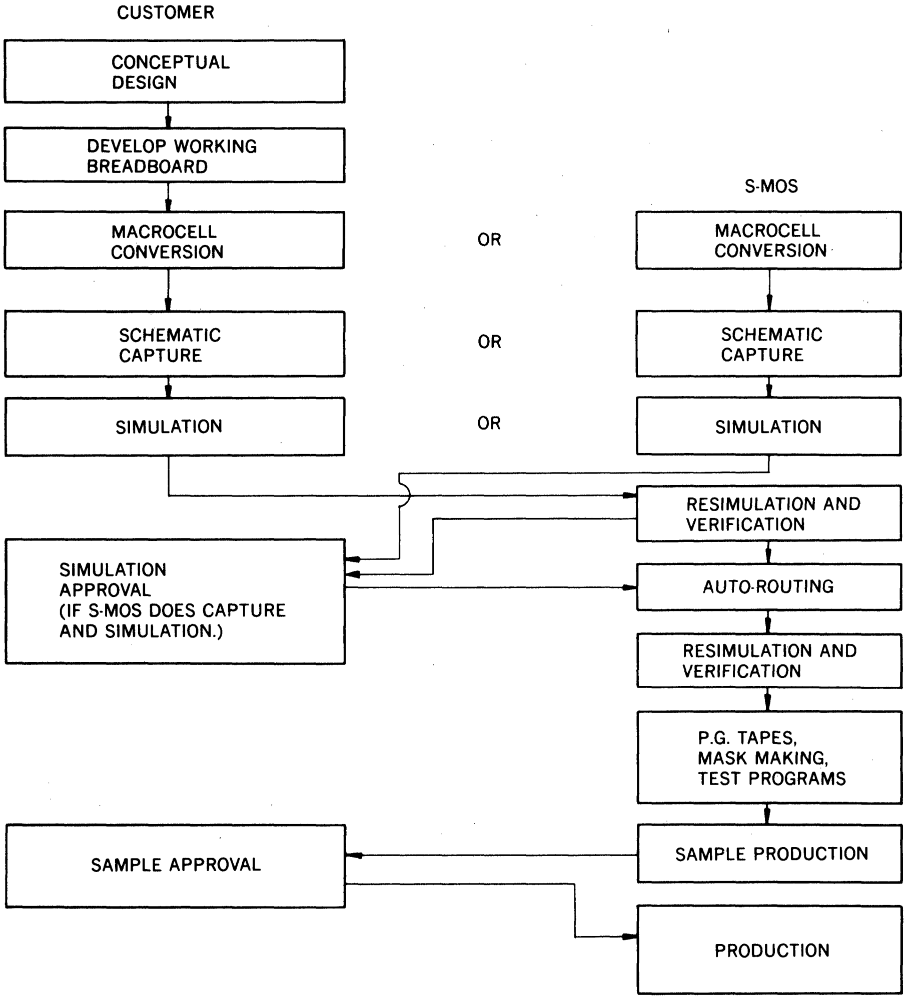
t_{pd}—V_{DD}



t_{pd}—T_a



■ GATE ARRAY DESIGN FLOW



SSC1000 Series

CMOS STANDARD CELL

- **Gate Densities Up To 12,000 Gates**
- **A Large Cell Library**
- **Minimal Delay Time Variance for Consistent Performance**

■DESCRIPTION

The SSC1000 Standard Cell Series consists of 20 basic master chips. A system utilizing up to 12,000 gates can be implemented on a single chip.

This family is fabricated using our advanced 1.8 micron dual layer metal CMOS process which results in very low power and very high speed performance.

The functions of the cell library are compatible with those of the SLA Gate Array Series and easy conversion from SLA6000 Series Gate Array design is possible.

The minimal delay time variance between the internal cells simplifies the design stage, and allows the speed to be as high as the TTL74S Series.

■FEATURES

- Usable for designs up to 12,000 gate complexity
- Very high speed (Typical delay time : 1.4ns)
- Cell functions compatible with the SLA gate array series
- Cell functions correspond to TTL74 Series
- Minimal delay time variance between cells
- I/O compatible with TTL or CMOS
- I/O high switching speed
- High output drive
- Low voltage operation at $V_{DD}=2.4V$ possible
- SRAM, ROM cells are available

■SSC1000 SERIES

Parameter \ Series		SSC1010 to SSC1200
Gates (2-input NAND)		12,000 gates (Max)
Technology		SILICON GATE CMOS 2 LAYER METALLIZATION
I/O level		TTL, CMOS
Delay time	Internal gate	1.4ns (2-input NAND F.O.=2, l=2mm)
	Input buffer	3 to 4 ns (standard)
	Output buffer	4 to 6 ns $C_L=30pF$ (standard)
Total ports for I/O		192 (Max)
Input mode		TTL, CMOS, Pull—up, Schmidt (Buffer & Inverter)
Output mode		Normal, Open-drain, 3-state, Bi-directional $I_{OL}=4mA$, 6mA, 14mA

■ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V, Ta=25℃)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.3 to 7.0	V
Input voltage	V_I	−0.3 to V_{DD}+0.3	V
Output voltage	V_O	−0.3 to V_{DD}+0.3	V
Output current/pin	I_O	±10*	mA
Power dissipation	P_D	250	mW
Supply current	I_{DD}/I_{SS}	50	mA
Storage temperature	T_{stg}	−65 to 150	℃

*Apply 4mA, 6mA DRIVER

■RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	TTL Input level			CMOS Input level			Low voltage operating			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supply voltage	V_{DD}	4.75	5.0	5.25	4.5	5.0	5.5	2.4	—	5.5	V
Input voltage	V_I	V_{SS}	—	V_{DD}	V_{SS}	—	V_{DD}	V_{SS}	—	V_{DD}	V
Operating temperature	T_{opr}	0	—	70	−20	—	80	−20	—	85	℃

*f_{MAX}= 1MHz at low voltage operation

■ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply current	I_{DDS}	Standby	—	—	10	μA
High level output voltage	V_{OH}	I_{OH}=2, 4, 8mA* V_{DD}=4.75V	V_{DD}−0.4	—	—	V
Low level output voltage	V_{OL}	I_{OL}=4, 6, 14mA* V_{DD}=4.75V	—	—	V_{SS}+0.4	V
High level input voltage (TTL)	V_{IH1}	V_{DD}=5.25V	2.0	—	—	V
Low level input voltage (TTL)	V_{IL1}	V_{DD}=4.75V	—	—	0.8	V
High level input voltage (CMOS)	V_{IH2}	V_{DD}=5.5V	3.5	—	—	V
Low level input voltage (CMOS)	V_{IL2}	V_{DD}=4.5V	—	—	1.0	V
Input leakage current	I_{LI}		−1	—	1	μA

*selective

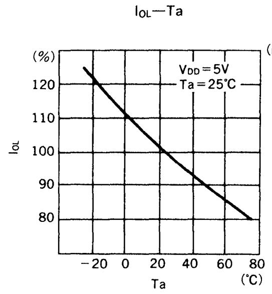
■PACKAGE LIST

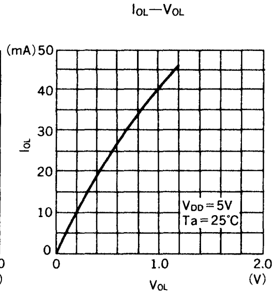
Series			SSC1010	SSC1020	SSC1030	SSC1040	SSC1050	SSC1060	SSC1070	SSC1080	SSC1090	SSC1100	SSC1110	SSC1120	SSC1130	SSC1140	SSC1150	SSC1160	SSC1170	SSC1180	SSC1190	SSC1200
PADS			40	44	48	60	64	72	80	84	92	100	112	120	124	132	148	160	172	180	188	192
Type	Pins	Name																				
Plastic DIP	16	C16	○		○																	
	18	C18	○	○																		
	24	C24	○	○	○	○	□	○	○	○	○	○										
	28	C28				○	○							○	○							
	40	C40			○	○	□	○			○	○	○									
	42	C42								○	□	○	○									
Plastic QFP	60	F60					○	○	○	○	□	○	○	○	○	○	○					
	80	F80					○	○	○	○	○	○	○	□	○	○	○					
	100	F100-5									○	□	□	○	○	○	○					
	128	F128-8											○	□	□	□	○	□	○			
	144	F144-8													□	□	□	□	□	○	□	○
	160	F160-8																○	○	○	□	○
Plastic SOP	28	M28	○	○	○	○	○	○	○													
PGA	64	P64												□	□	□	□	□				
	72	P72															□	□				
	88	P88						□	□	□							□	□				
	96	P96															□	□				
	120	P120															□	□				
	132	P132															□	□				
PLCC	44	J44		○	○	○	○	○	○	○	○	○	○	○	○	○						
	68	J68				○	○	○	○	○	○	○	○	○	○	○	○	○	○			
	84	J84								○	○	○	○	○	○	○	○	○	○	○		

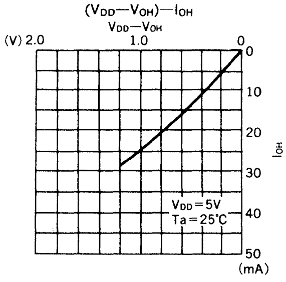
○ : Available □ : Under development

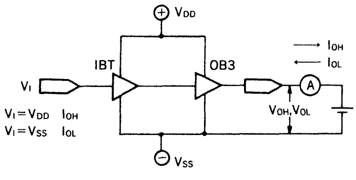
■CHARACTERISTICS CURVES

●Output Current


I_{OL}—Ta

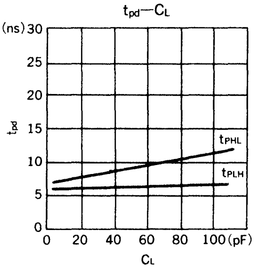

I_{OL}—V_{OL}

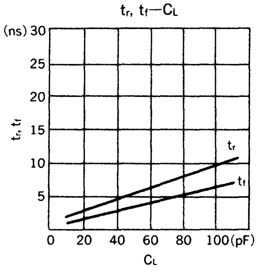

(V_{DD}—V_{OH})—I_{OH}

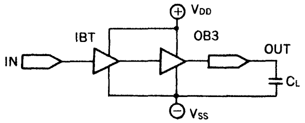


Measuring Circuit

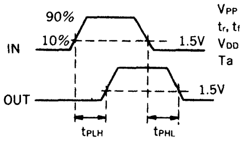
● t_{pd}, t_r, t_f—C_L


t_{pd}—C_L


t_r, t_f—C_L

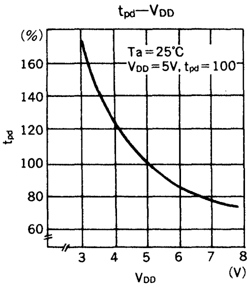


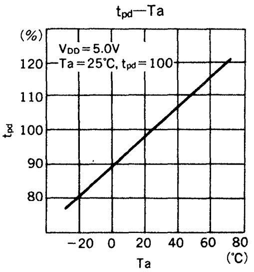
Measuring Circuit

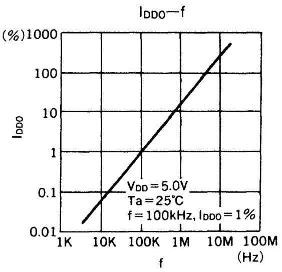


V_{PP} = 3 [V]
t_r, t_f = 5 [ns]
V_{DD} = 5 [V]
Ta = 25 [°C]

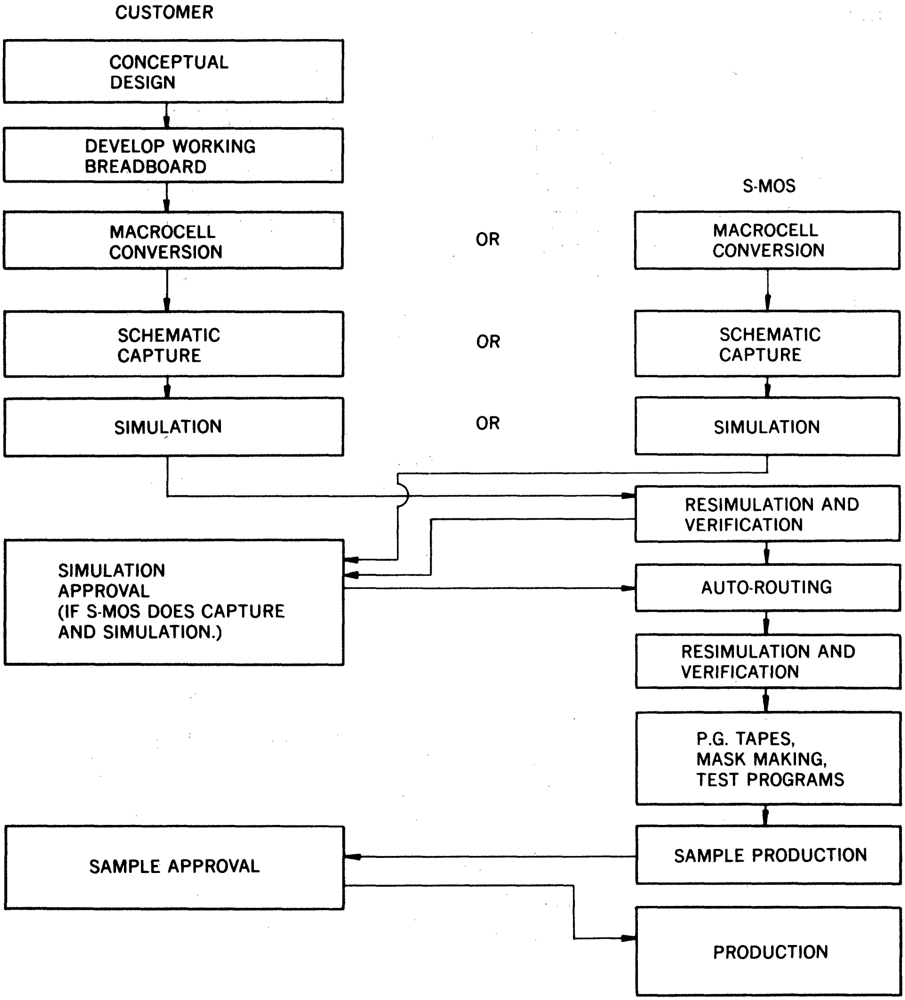
●Delay Time


t_{pd}—V_{DD}


t_{pd}—Ta

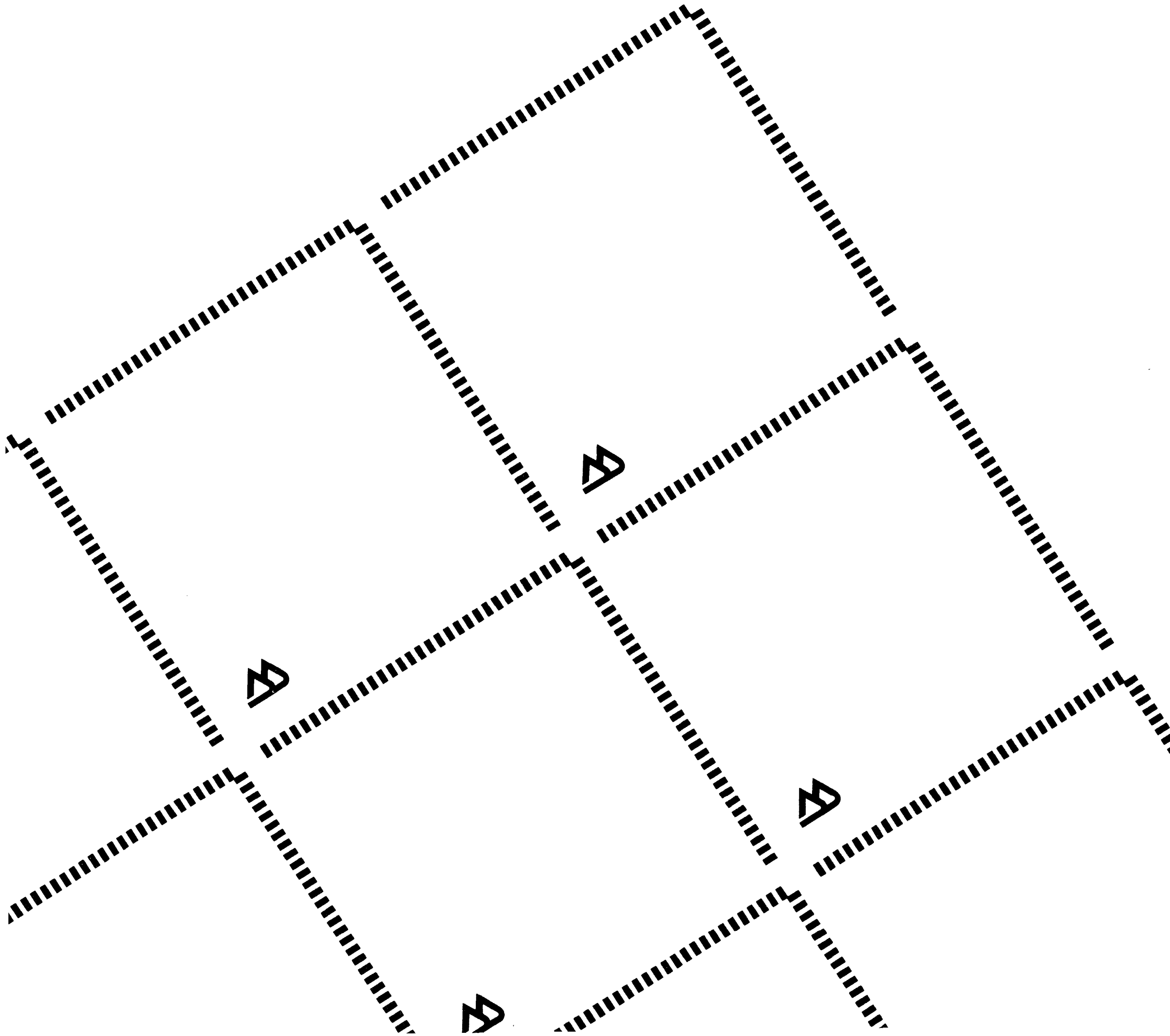

I_{DDO}—f

■GATE ARRAY DESIGN FLOW



1988/1989 CMOS DATA BOOK

E. DRIVERS/CONTROLLERS



SED1180F/SED1181F

CMOS DOT MATRIX HIGH DUTY LCD DRIVER

●64-bit High Voltage Resistant Output
●1/64 to 1/128 in Display Duty
●COMS High Voltage Resistant Process

■DESCRIPTION

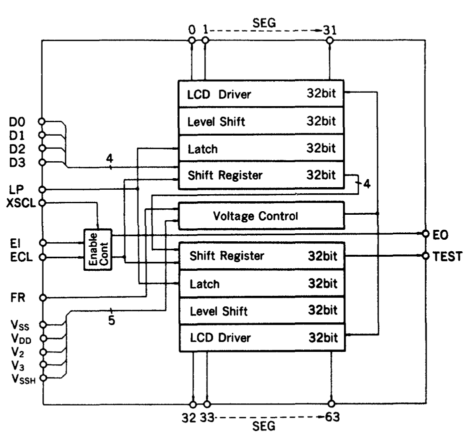
The SED1180F and SED1181F are LCD Segment drivers which are used in conjunction with the SED1190F and SED1191F (LCD common drivers).
They can drive a large dot-matrix LCD display with a duty ratio of 1/64 or higher.

■FEATURES

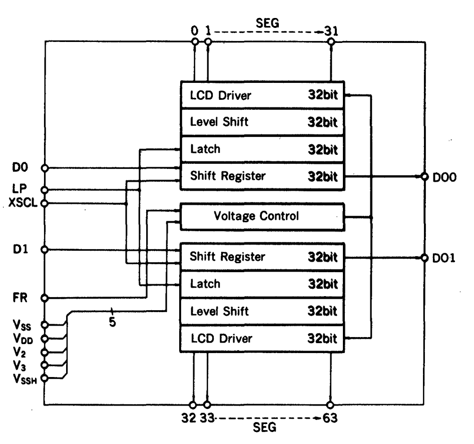
- ●Display duty ··1/64 to 1/128
- ●64-bit high voltage resistant output, LCD driver (Segment driver)
- ●Rightward shift suitable for a 1/64-duty panel
- ●Allows cascade-connection. Dasy-chain connection of enable pins can be used to minimize power consumption. (SED1180F only)
- ●Power supply for the logic······················ −5V±10%
- ●CMOS high-voltage-resistant process·········25V (Max)
- ●SED1180F ··4-bit bus data transfer
- ●SED1181F ··Independent serial data input for each 32 segment
- ●Package··80-pin QFP (plastic)

■BLOCK DIAGRAM

SED1180F



SED1181F



PIN DESCRIPTION

SED1180F

Pin Name	Functions
SEG0 to 63	Outputs to Segment pins of LCD Output level changes at each latch pulse LP falling-edge.
XSCL	Shift clock for displayed data Falling-edge trigger
LP	Latch pulse for displayed data Falling-edge trigger
FR	LCD display frame signal
EI	Enable input; enabled on "H", disabled on "L"
ECL	A clock pulse for propagation of enable signals Falling-edge trigger
EO	Enable output In cascade connection, EO of nth driver is connected to EI of (n+1)-th driver.
D0 to D3	4-bit display data input
TEST	Outputs shifted data input from D3
V_{DD}, V_{SS}	Power supply for the logic, V_{DD}: 0V (GND), V_{SS}: -5.0V
V_2, V_3, V_{SSH}	Power supply for driving LCD, $V_{DD} > V_2 > V_3 > V_{SSH}$

SED1181F

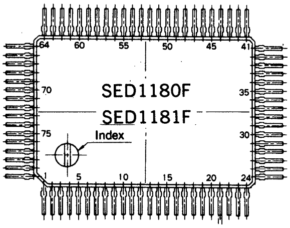
Pin Name	Functions
SEG0 to 63	Outputs to Segment pins of LCD Output level changes at each latch pulse LP falling-edge
XSCL	Shift clock for displayed data Falling-edge trigger
LP	Latch pulse for displayed data Falling-edge trigger
FR	LCD display frame signal
DO0	Outputs serial display data input from D0.
DO1	Outputs serial display data input from D1.
D0, D1	Input 2-bit serial display data (Data read at a XSCL falling-edge)
V_{DD}, V_{SS}	Power supply for the logic, V_{DD}: 0V (GND), V_{SS}: -5.0V
V_2, V_3, V_{SSH}	Power supply for driving LCD, $V_{DD} > V_2 > V_3 > V_{SSH}$

Note:

D0: serial display data corresponds to SEG0 to SEG31.

D1: serial display data corresponds to SEG32 to SEG63.

PIN CONFIGURATION



SED1180F

No.	NAME	No.	NAME	No.	NAME	No.	NAME
1	SEG27	21	SEG 7	41	SEG36	61	SEG56
2	SEG26	22	SEG 6	42	SEG37	62	SEG57
3	SEG25	23	SEG 5	43	SEG38	63	SEG58
4	SEG24	24	SEG 4	44	SEG39	64	SEG59
5	SEG23	25	SEG 3	45	SEG40	65	SEG60
6	SEG22	26	SEG 2	46	SEG41	66	SEG61
7	SEG21	27	SEG 1	47	SEG42	67	SEG62
8	SEG20	28	SEG 0	48	SEG43	68	SEG63
9	SEG19	29	EO	49	SEG44	69	V_{SSH}
10	SEG18	30	D3	50	SEG45	70	V_2
11	SEG17	31	D2	51	SEG46	71	V_3
12	SEG16	32	D1	52	SEG47	72	V_{SS}
13	SEG15	33	D0	53	SEG48	73	V_{DD}
14	SEG14	34	XSCL	54	SEG49	74	TEST
15	SEG13	35	LP	55	SEG50	75	EI
16	SEG12	36	FR	56	SEG51	76	ECL
17	SEG11	37	SEG32	57	SEG52	77	SEG31
18	SEG10	38	SEG33	58	SEG53	78	SEG30
19	SEG 9	39	SEG34	59	SEG54	79	SEG29
20	SEG 8	40	SEG35	60	SEG55	80	SEG28

SED1181F

No.	NAME	No.	NAME	No.	NAME	No.	NAME
1	SEG27	21	SEG 7	41	SEG36	61	SEG56
2	SEG26	22	SEG 6	42	SEG37	62	SEG57
3	SEG25	23	SEG 5	43	SEG38	63	SEG58
4	SEG24	24	SEG 4	44	SEG39	64	SEG59
5	SEG23	25	SEG 3	45	SEG40	65	SEG60
6	SEG22	26	SEG 2	46	SEG41	66	SEG61
7	SEG21	27	SEG 1	47	SEG42	67	SEG62
8	SEG20	28	SEG 0	48	SEG43	68	SEG63
9	SEG19	29	DO0	49	SEG44	69	V_{SSH}
10	SEG18	30	NC	50	SEG45	70	V_2
11	SEG17	31	NC	51	SEG46	71	V_3
12	SEG16	32	D1	52	SEG47	72	V_{SS}
13	SEG15	33	D0	53	SEG48	73	V_{DD}
14	SEG14	34	XSCL	54	SEG49	74	DO1
15	SEG13	35	LP	55	SEG50	75	NC
16	SEG12	36	FR	56	SEG51	76	NC
17	SEG11	37	SEG32	57	SEG52	77	SEG31
18	SEG10	38	SEG33	58	SEG53	78	SEG30
19	SEG 9	39	SEG34	59	SEG54	79	SEG29
20	SEG 8	40	SEG35	60	SEG55	80	SEG28

■ABSOLUTE MAXIMUM RATINGS

($V_{DD}=0V$)

Parameter	Symbol	Ratings	Unit
Supply voltage (1)	V_{SS}	−7.0 to 0.3	V
Supply voltage (2)	V_{SSH} V_2, V_3	−28.0 to 0.3	V
Input voltage	V_I	$V_{SS}-0.3$ to 0.3	V
Operating temperature	T_{opr}	−20 to 75	°C
Storage temperature	T_{stg}	−65 to 150	°C
Soldering temperature and time	T_{sol}	260°C · 10s (at lead)	—

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

($V_{DD}=0V$, $V_{SS}=-5V\pm10\%$, Ta = −20 to 75°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage (1)	V_{SS}		−5.5	−5.0	−4.5	V
Supply voltage (2)	V_2		V_{SSH}	—	V_{DD}	V
	V_3		V_{SSH}	—	V_{DD}	V
	V_{SSH}	Recommended V_{SSH}	−25.0	—	−14.0	V
		Operable V_{SSH}*	−25.0	—	−5.0	V
High level input voltage	V_{IH}		$0.2V_{SS}$	—	$V_{DD}+0.3$	V
Low level input voltage	V_{IL}		$V_{SS}-0.3$	—	$0.8V_{SS}$	V
High level output voltage	V_{OH}	$I_{OH}=-0.6mA$	−0.4	—	—	V
Low level output voltage	V_{OL}	$I_{OL}=0.6mA$	—	—	$V_{SS}+0.4$	V
Input leak current	I_{LI}	$0_V \leqq V_I \leqq V_{SS}$	—	0.05	2.0	µA
Output leak current	I_{LO}	$0_V \leqq V_O \leqq V_{SS}$	—	0.05	5.0	µA
Shift clock	XSCL		—	—	6.0	MHz
Frame signal	FR		—	1/60	—	s
Input capacitance	C_I	Ta = 25°C	—	5.0	8.0	pF
Segment output on resistance	R_{SEG}	$V_{OH}=V_{DD}-0.5V$ $V_{OL}=V_{SSH}+0.5V$ SEG /bit $V_{SSH}=-20.0V$	—	1.9	2.9	kΩ
		$V_{SSH}=-14.0V$	—	2.4	3.9	
		$V_{SSH}=-9.0V$	—	3.6	7.0	
		$V_{SSH}=-5.0V$	—	11.5	500.0	
Quiescent current	I_Q	$V_{SSH}=-25V$, $V_{SS}=-5.5V$ $V_I=V_{DD}$	—	0.05	30	µA
Operating current for the logic	I_{SSO}	SED 1180 FR cycle = 16.7ms ECL cycle = 13µs $V_{SS}=-5.0V$ $V_{IH}=V_{DD}$, $V_{IL}=V_{SS}$ LP cycle = 130µs XSCL = 1.5MHz (duty50%) All data input reversed bit by bit. All output pins are opened.	—	90	200	µA
		SED 1181 FR cycle = 130µs (duty50%)	—	850	1200	
Operating current for LCD	I_{SSHO}	SED 1180 FR cycle = 16.7ms ECL cycle = 13µs $V_{SS}=-4.5V$, $V_2=-4.0V$ $V_3=-16.0V$, $V_{SSH}=-20.0V$ $V_{IH}=V_{DD}$, $V_{IL}=V_{SS}$ LP cycle = 130µs XSCL = 1.5MHz (duty50%) All data input reversed bit by bit. All output pins are opened.	—	40	80	µA
		SED 1181 FR cycle = 130µs (duty50%)	—	70	100	

*Operable V_{SSH} indicates its functionally operable range although the driver output ON resistance becomes higher than with recommended V_{SSH}.
To determine the voltage, we recommend to test the driver with a liquid crystal panel.

●AC Electrical Characteristics

($V_{DD}=0V$, $V_{SS}=-5.0V\pm10\%$, $Ta=-20$ to 75°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Shift clock cycle	t_{CLC}		166	—	—	ns
Shift clock "H" width	t_{WCLH}		63	—	—	ns
Shift clock "L" width	t_{WCLL}		63	—	—	ns
Data setup time	t_{DS}		50	—	—	ns
Data hold time	t_{DH}		30	—	—	ns
Enable clock "H" width	t_{WECH}	*3	100	—	—	ns
Enable clock "L" width	t_{WECL}	*3	100	—	—	ns
Enable data setup time	t_{EDS}	*3	50	—	—	ns
Enable data hold time	t_{EDH}	*3	20	—	—	ns
Enable clock delay time	t_{EDR}	*3	−10	—	—	ns
Enable clock setup time	t_{ECS}	*3	70	—	—	ns
Latch pulse "H" width	t_{WLPH}	*1	110	—	—	ns
Latch pulse "L" width	t_{WLPL}		220	—	—	ns
Latch timing	t_{LT}		100	—	—	ns
Latch hold time	t_{LH}		0	—	—	ns
Latch pulse data setup time	t_{LDS}	*2, *3	140	—	—	ns
Latch pulse data hold time	t_{LDH}	*2, *3	50	—	—	ns
Permissible frame signal delay	t_{DFR}		−500	—	500	ns
Input signal rise time	t_r		—	—	*4	
Input signal fall time	t_f		—	—	*4	
Enable output delay	t_{PD}	*3	20	—	150	ns
Serial data output delay	t_{PO}		20	—	150	ns

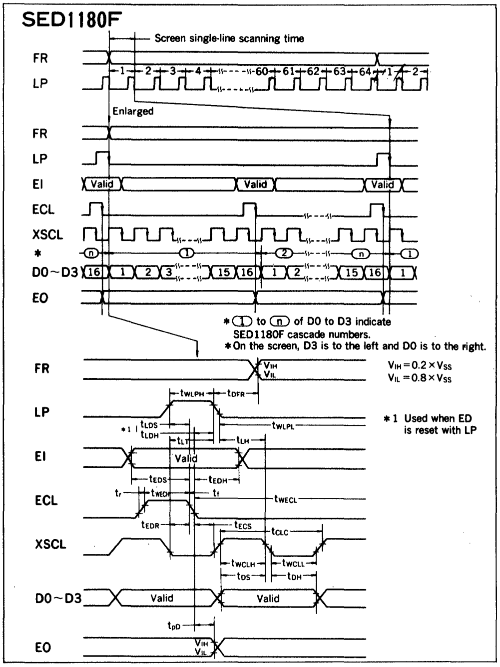
*1 $t_{WLPH}=160ns$ (Min) when LP is used as EI data.

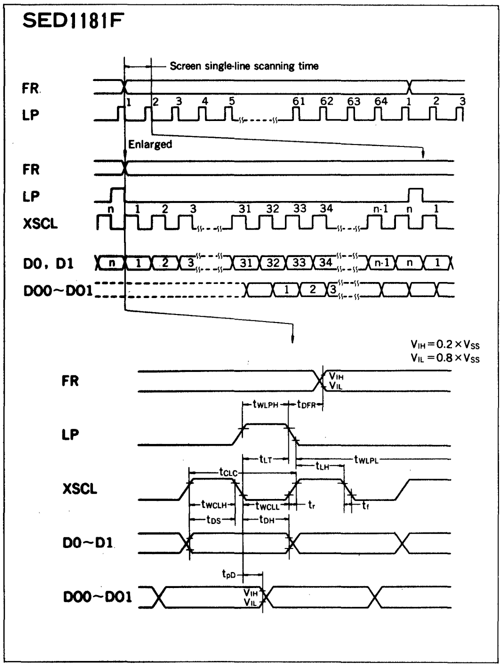
*2 $t_{WLPH}=250ns$ (Min) when EO output is reset with LP. ($tr=tf=25ns$)

*3 Applicable to SED1180F only.

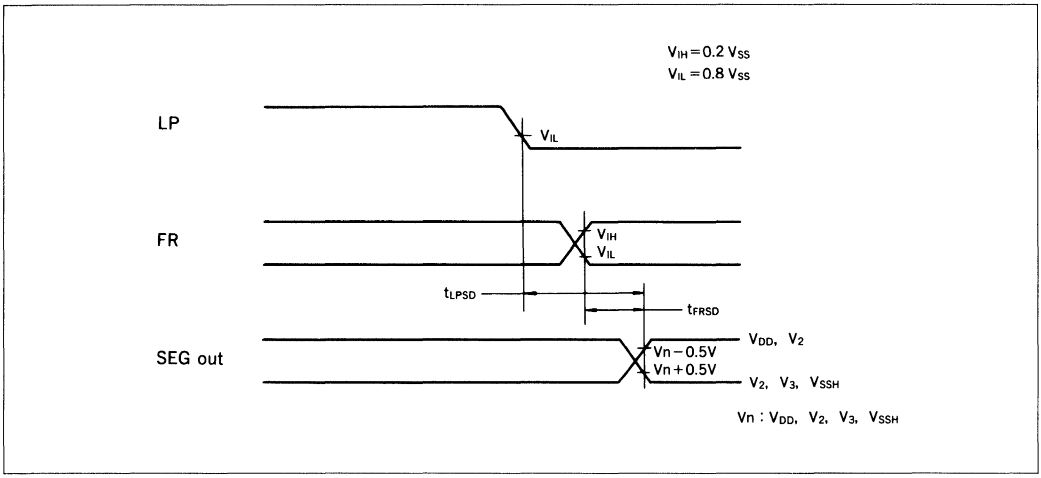
*4 tr, tf$<(t_{CLC}-t_{WCLH}-t_{WCLL})/2$, where tr, tf$\leq$50ns.

●Timing Chart


SED1180F


SED1181F

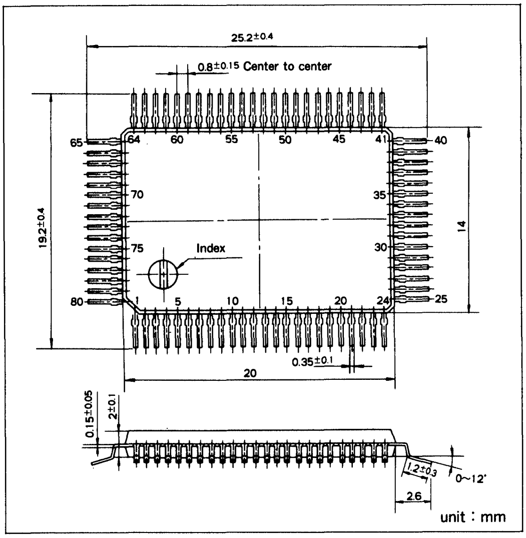
●SEG Output Signal Timing Characteristics



(V_{DD}=0V, V_{SS}= −5V±10%, Ta= −20 to 75°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
LP-SEG output delay time	t_{LPSD}	$V_{SSH}= -14.0$ to -25.0V $C_L=100$pF	—	—	4.5	μs
FR-SEG output delay time	t_{FRSD}		—	—	4.5	μs

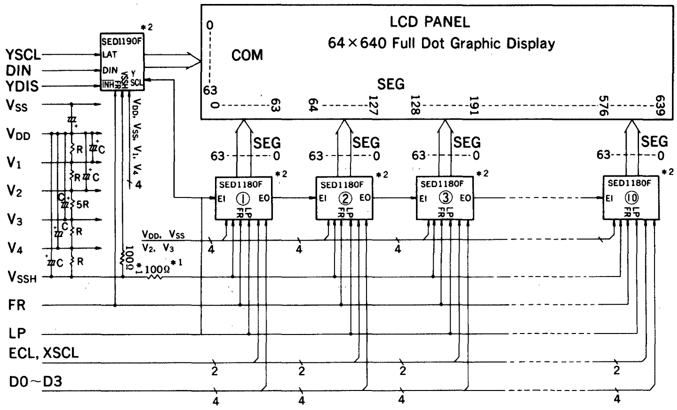
■PACKAGE DIMENSIONS



*Drawing is applicable to SED1180F0A/SED1181F0B.
*SED1180F5A/SED1181F5A are 2.7mm thick.

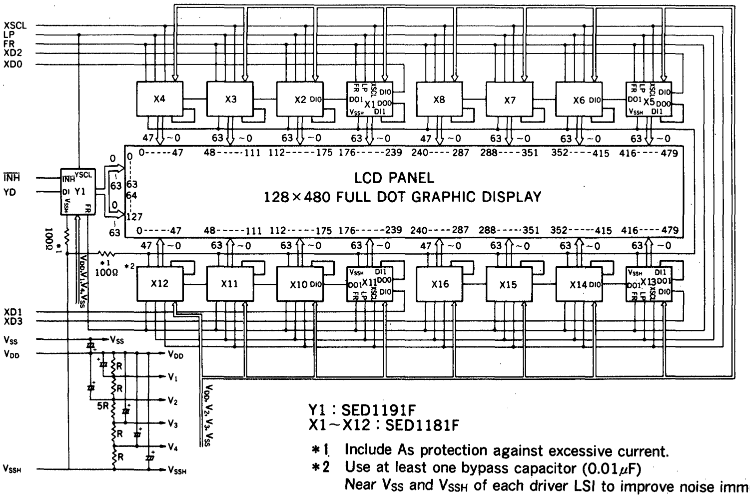
■EXAMPLE OF APPLICATION

SED1180F (64×640 dot, 1/64 duty, 1/9 bias)



*1 Use to protect against excessive current.
*2 Use at least one bypass capacitor (0.01μF)
Near V_{SS} and V_{SSH} of each driver LSI to improve noise immunity.

SED1181F (128×480 dot, 1/64 duty, 1/9 bias)



Y1 : SED1191F
X1~X12 : SED1181F
*1 Include As protection against excessive current.
*2 Use at least one bypass capacitor (0.01μF)
Near V_{SS} and V_{SSH} of each driver LSI to improve noise immunity.

PF322-02

SED1190F/SED1191F

CMOS DOT MATRIX HIGH DUTY LCD DRIVER

- **64-bit High Voltage Resistant Output**
- **1/64 to 1/128 in Display Duty**
- **CMOS High Voltage Resistant Process**

DESCRIPTION

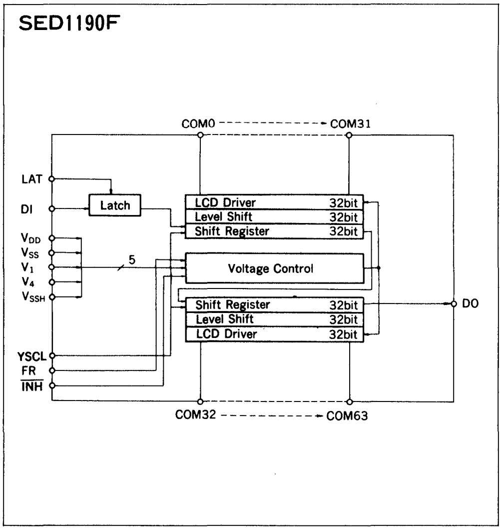
The SED1190F and SED1191F are LCD Common drivers which are used in conjunction with SED1180F and SED1181F (LCD Segment drivers).

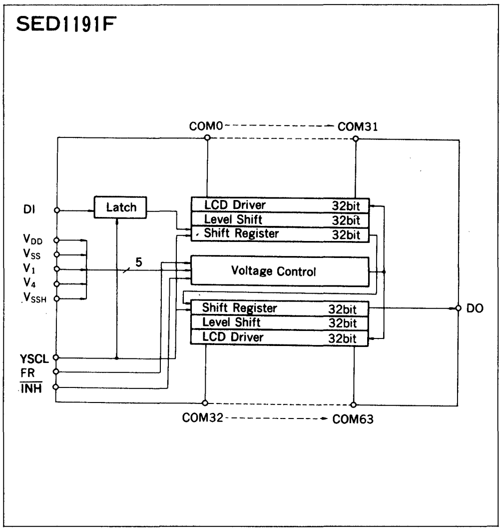
They can drive a large dot-matrix LCD display with a duty ratio of 1/64 or higher.

FEATURES

- Display duty ···1/64 to 1/128
- Provides inhibit function for instantaneous display blanking
- 64-bit high-voltage resistant output, LCD driver (Common driver)
- Rightward shift suitable for a 1/64-duty LCD panel
- Cascade-connection makes high duty drive possible
- Power supply for the logic························−5V±10%
- CMOS high-voltage-resistant process·········25V (Max)
- Connectable to a general purpose LCD controller (SED1191F only)
- Provides for data read and data shift by a single clock
- Package··80-pin QFP (plastic)

BLOCK DIAGRAM





■PIN DESCRIPTION

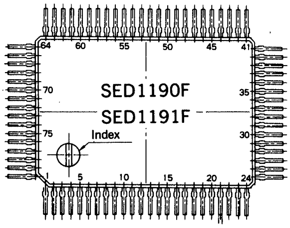
SED1190F

Pin Name	Functions
COM0 to 63	Outputs to Common pins of LCD Output level changes at each shift clock YSCL falling-edge.
LAT	The latch pulse input for the shift data DI is pulled up internally. Normally used in the opened state.
YSCL	Serial data shift clock, Falling edge trigger
FR	LCD display frame signal
DI	Serial shift data input
$\overline{\text{INH}}$	A control signal which turns all Common outputs to a non-selectable waveform. "L" active
DO	Serial shift data output Outputs serial data at shift clock falling-edge.
V_{DD}, V_{SS}	Power supply for the logic, V_{DD}: 0V, V_{SS}: −5.0V
V_1, V_4, V_{SSH}	Power supply for driving LCD, $V_{DD} > V_1 > V_4 > V_{SSH}$

SED1191F

Pin Name	Functions
COM0 to 63	Outputs to Common pins of LCD Output level changes at each shift clock YSCL falling-edge.
YSCL	Serial data shift clock, Falling edge trigger
FR	LCD display frame signal
DI	Serial shift data input Reads data at each YSCL rising edge.
$\overline{\text{INH}}$	A control signal which turns all common outputs to a non-selectable waveform. "L" active
DO	Serial shift data output Outputs serial data in sync with shift clock falling-edge.
V_{DD}, V_{SS}	Power supply for the logic, V_{DD}: 0V, V_{SS}: −5.0V
V_1, V_4, V_{SSH}	Power supply for driving LCD, $V_{DD} > V_1 > V_4 > V_{SSH}$

■PIN CONFIGURATION



SED1190F

No.	NAME	No.	NAME	No.	NAME	No.	NAME
1	COM31	21	COM11	41	COM40	61	COM60
2	COM30	22	COM10	42	COM41	62	COM61
3	COM29	23	COM 9	43	COM42	63	COM62
4	COM28	24	COM 8	44	COM43	64	COM63
5	COM27	25	COM 7	45	COM44	65	DO
6	COM26	26	COM 6	46	COM45	66	V_{SSH}
7	COM25	27	COM 5	47	COM46	67	V_4
8	COM24	28	COM 4	48	COM47	68	NC
9	COM23	29	COM 3	49	COM48	69	NC
10	COM22	30	COM 2	50	COM49	70	NC
11	COM21	31	COM 1	51	COM50	71	NC
12	COM20	32	COM 0	52	COM51	72	V_1
13	COM19	33	COM32	53	COM52	73	V_{SS}
14	COM18	34	COM33	54	COM53	74	V_{DD}
15	COM17	35	COM34	55	COM54	75	NC
16	COM16	36	COM35	56	COM55	76	DI
17	COM15	37	COM36	57	COM56	77	LAT
18	COM14	38	COM37	58	COM57	78	$\overline{\text{INH}}$
19	COM13	39	COM38	59	COM58	79	FR
20	COM12	40	COM39	60	COM59	80	YSCL

SED1191F

No.	NAME	No.	NAME	No.	NAME	No.	NAME
1	COM31	21	COM11	41	COM40	61	COM60
2	COM30	22	COM10	42	COM41	62	COM61
3	COM29	23	COM 9	43	COM42	63	COM62
4	COM28	24	COM 8	44	COM43	64	COM63
5	COM27	25	COM 7	45	COM44	65	DO
6	COM26	26	COM 6	46	COM45	66	V_{SSH}
7	COM25	27	COM 5	47	COM46	67	V_4
8	COM24	28	COM 4	48	COM47	68	NC
9	COM23	29	COM 3	49	COM48	69	NC
10	COM22	30	COM 2	50	COM49	70	NC
11	COM21	31	COM 1	51	COM50	71	NC
12	COM20	32	COM 0	52	COM51	72	V_1
13	COM19	33	COM32	53	COM52	73	V_{SS}
14	COM18	34	COM33	54	COM53	74	V_{DD}
15	COM17	35	COM34	55	COM54	75	NC
16	COM16	36	COM35	56	COM55	76	DI
17	COM15	37	COM36	57	COM56	77	YSCL
18	COM14	38	COM37	58	COM57	78	$\overline{\text{INH}}$
19	COM13	39	COM38	59	COM58	79	FR
20	COM12	40	COM39	60	COM59	80	NC

■ABSOLUTE MAXIMUM RATINGS

(V_{DD}=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage (1)	V_{SS}	−7.0 to 0.3	V
Supply voltage (2)	V_{SSH}	−28.0 to 0.3	V
	V_1, V_4		
Input voltage	V_I	V_{SS}−0.3 to 0.3	V
Operating temperature	T_{opr}	−20 to 75	°C
Storage temperature	T_{stg}	−65 to 150	°C
Soldering temperature and time	T_{sol}	260°C · 10s (at lead)	—

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

(V_{DD}=0V, V_{SS}=−5V±10%, Ta=−20 to 75°C)

Parameter	Symbol	Conditions			Min	Typ	Max	Unit
Supply voltage (1)	V_{SS}				−5.5	−5.0	−4.5	V
Supply voltage (2)	V_1				V_{SSH}	—	V_{DD}	V
	V_4				V_{SSH}	—	V_{DD}	V
	V_{SSH}	Recommended V_{SSH}			−25.0	—	−14.0	V
		Operable V_{SSH}*			−25.0	—	−5.0	V
High level input voltage	V_{IH}				0.2V_{SS}	—	V_{DD}+0.3	V
Low level input voltage	V_{IL}				V_{SS}−0.3	—	0.8V_{SS}	V
High level output voltage	V_{OH}	I_{OH}=−0.6mA			−0.4	—	—	V
Low level output voltage	V_{OL}	I_{OL}= 0.6mA			—	—	V_{SS}+0.4	V
Input leak current	I_{LI}	0v≧V_I≧V_{SS}			—	0.05	2.0	μA
Output leak current	I_{LO}	0v≧V_O≧V_{SS}			—	0.05	5.0	μA
Shift clock	YSCL				—	—	2.5	MHz
Frame signal	FR				—	1/60	—	s
Input capacitance	C_I	Ta=25°C			—	5.0	8.0	pF
Common output on resistance	R_{COM}	V_{OH}=V_{DD}−0.5V V_{OL}=V_{SSH}−0.5V COM/bit		V_{SSH}=−20.0V	—	0.8	1.0	kΩ
				V_{SSH}=−14.0V	—	0.9	1.3	
				V_{SSH}=− 9.0V	—	1.3	2.0	
				V_{SSH}=− 5.0V	—	3.0	30.0	
Quiescent current	I_Q	SED 1190	V_{SSH}= −25.0V	V_{SS}=−5.5V V_I=V_{DD}	—	0.05	30	μA
		SED 1191	V_{SSH}= −25.0V					
Operating current for the logic	I_{SSO}	SED 1190	FR cycle= 16.7ms	V_{SS}=−5.0V V_{IH}=V_{DD}, V_{IL}=V_{SS} YSCL cycle=130μs (duty 50%) All "H" output. Output terminals are opened at every data input of 1/128 duty.	—	3.0	8.0	μA
		SED 1191	FR cycle= 130μs		—	850	1200	
Operating current for LCD	I_{SSHO}	SED 1190	FR cycle= 16.7ms	V_{SS}=−4.5V, V_1=−2.0V V_4=−18.0V, V_{SSH}=−20.0V YSCL cycle=130μs (duty 50%) All "H" output. Output terminals are opened at every data input of 1/128 duty.	—	3.0	8.0	μA
		SED 1191	FR cycle= 130μs		—	70	100	
Pull up MOS current (applicable to SED1190 only)	$-I_p$	V_{SS}=−5.0V, V_{IL}=−5.0V Applicable to LAT input terminals			10.0	25.0	50.0	μA

* Operable V_{SSH} indicates its functionally operable range although the driver output on resistance becomes higher than with recommended V_{SSH}.
To determine the voltage, we recommend to test the driver with a liquid crystal panel.

●AC Electrical Characteristics

($V_{DD}=0V$, $V_{SS}=-5V\pm10\%$, Ta=−20 to 75°C)

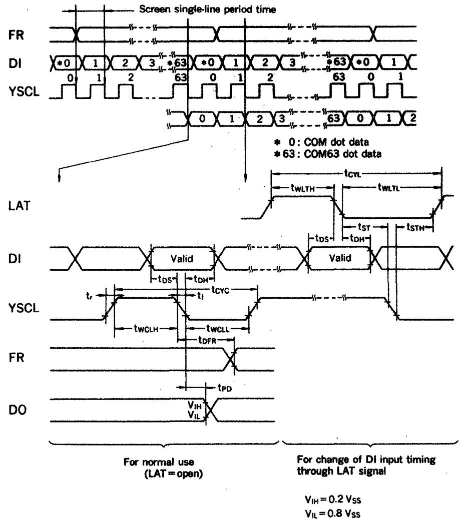
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Latch pulse cycle time	t_{CYL}		400	—	—	ns
Latch pulse "H" width*1	t_{WLTH}		180	—	—	ns
Latch pulse "L" width*1	t_{WLTL}		180	—	—	ns
Shift lock cycle time	t_{CYC}		400	—	—	ns
Shift lock "H" width	t_{WCLH}		110	—	—	ns
Shift lock "L" width	t_{WCLL}		110(240)	—	—	ns
Data setup time	t_{DS}		100(70)	—	—	ns
Data hold time	t_{DH}		30	—	—	ns
Data shift timing*1	t_{ST}		0	—	—	ns
Data shift hold time*1	t_{STH}		125	—	—	ns
Permissible frame signal delay	t_{DFR}		−500	0	500	ns
Iuput signal rise time	t_r		—	—	*2	ns
Input signal fall time	t_f		—	—	*2	ns
Data output delay time	t_{pD}	$C_L=15pF$	30	—	170	ns

*1 Applicable to SED1190F only. Values in parenthesis are for SED1191F.

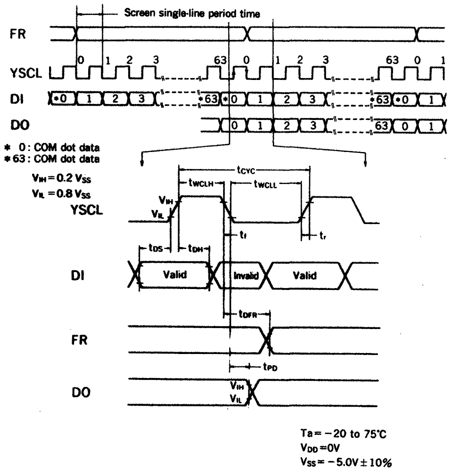
*2 t_r, $t_f=(t_{CYL}-t_{WLH}-t_{WLTL}/2$, where t_r, $t_f\leqq50ns$.

●Timing Chart

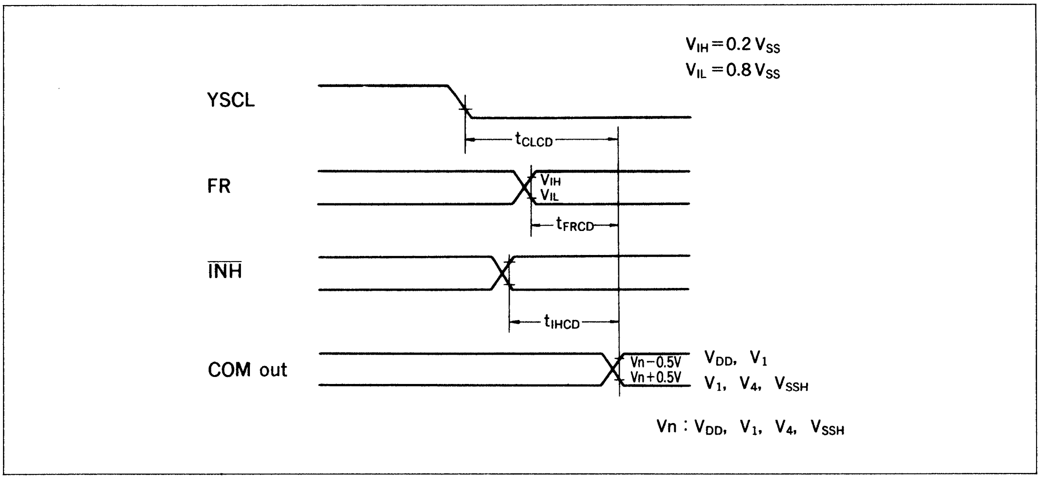
SED1190F



SED1191F



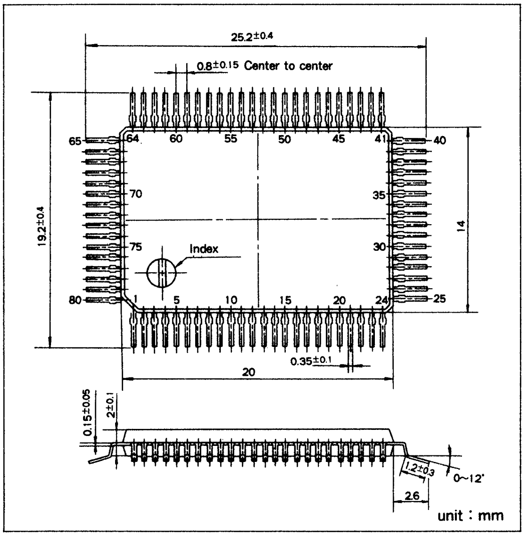
●COM Output Signal Timing Characteristics



(V_{DD}=0V, V_{SS}=−5V±10%, Ta=−20 to 75°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
YSCL-COM output delay time	t_{CLCD}	V_{SSH}=−14.0 to −25.0V C_L=100pF	—	—	3.0	μs
RF-COM output delay time	t_{FRCD}		—	—	3.0	μs
INH-COM output delay time	t_{IHCD}		—	—	3.0	μs

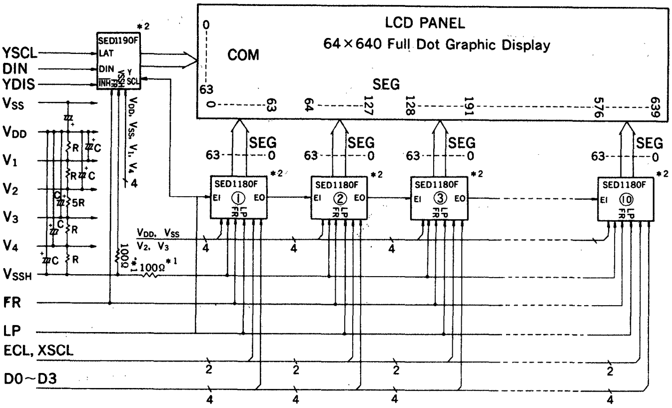
■PACKAGE DIMENSIONS



*Drawing is applicable to SED1190F$_{0A}$/SED1191F$_{0B}$.
*SED1190F$_{5A}$/SED1191F$_{5B}$ are 2.7mm thick.

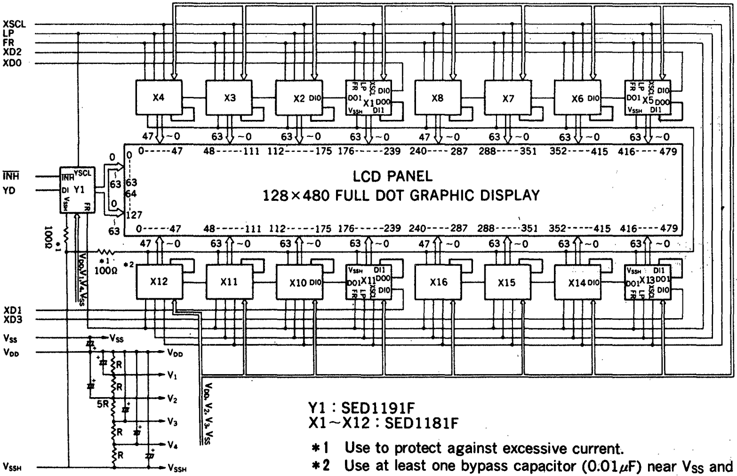
EXAMPLE OF APPLICATION

SED1190F (64×640 dots, 1/64 duty, 1/9 bias)



*1 Use to protect against excessive current.
*2 Use at least one bypass capacitor (0.01μF) near Vss and VSSH of each driver LSI to improve noise immunity.

SED1191F (128×480 dots, 1/64 duty, 1/9 bias)



Y1 : SED1191F
X1~X12 : SED1181F

*1 Use to protect against excessive current.
*2 Use at least one bypass capacitor (0.01μF) near Vss and VSSH of each driver LSI to improve noise immunity.

SED1600F

CMOS DOT MATRIX HIGH DUTY LCD DRIVER

- 80-bit High Voltage Resistant Output
- 1/100 to 1/300 in Display Duty
- CMOS High Voltage Resistant Process

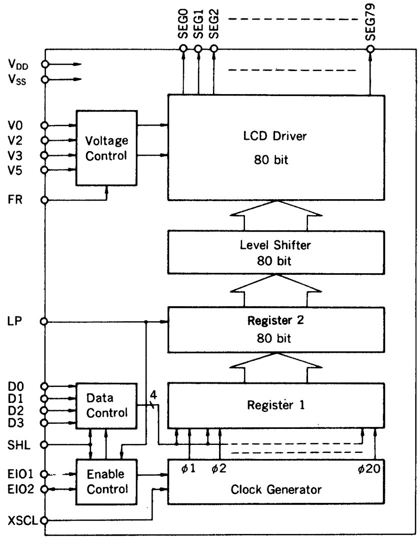
■DESCRIPTION

The SED1600F is an 80 output segment (column) driver, used to driver large-capacity dot matrix LCD panels with a duty ratio of 1/300 (from 1/100). It is used in conjunction with the SED1610F or SED1630F common (row) drivers. The SED1600F has a wide range of drive voltages. The maximum voltage V0 is isolated from V_{DD} to enable the application of any external LCD driving bias voltage from outside to the SED1600F. These unique features enable the SED1600F to operate with a wide variety of LCD panels. The SED1600F requires no enable signal to implement an enable chain technology which provides low power dissipation. This offers simpler interface with the LCD controller SED1330F/SED1341F or a microprocessor.

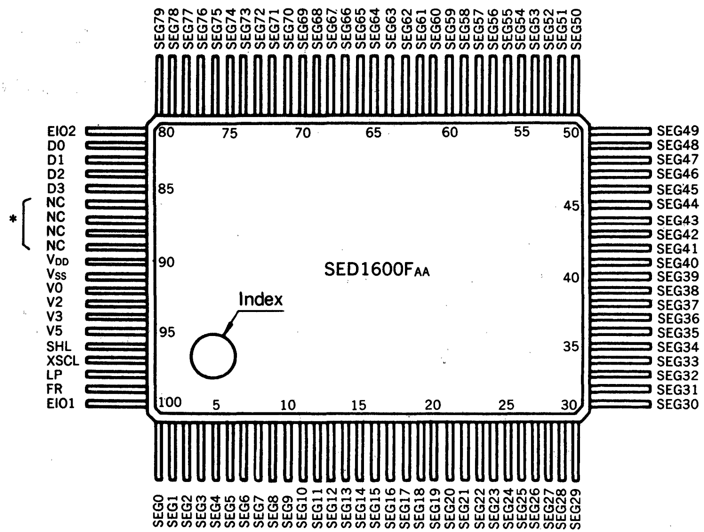
■FEATURES

- 80 LCD driving outputs
- Display capacity ································640×200×3 dots when combined with SED1610F (SED1630F)
- Wide range of LCD driving voltages ·········12 to 28V
  (Absolute maximum voltage·········30V)
- High-speed, low-power data transfer by 4-bit bus enable chain technology
  Shift clock·········6MHz Max
- Enable auto-transfer function to allow cascade connection and low power dissipation (requiring no enable signal to be furnished by a controller)
- Output shift direction pin selectable
- Ability to adjust offset bias of LCD source from V_{DD}
- Power supply for the logic······················ −5V±10%
- Si gate CMOS process
- Package··100-pin QFP (plastic)

■BLOCK DIAGRAM



PIN CONFIGURATION



*NC: No Connection

PIN DESCRIPTION

<table>
<tr><th>Pin name</th><th>I/O</th><th>Functions</th></tr>
<tr><td>SEG0 to SEG79</td><td>O</td><td>LCD driving segment (column) outputs.
Each output changes at the falling edge of LP.</td></tr>
<tr><td>D0 to D3</td><td>I</td><td>Display data inputs.</td></tr>
<tr><td>XSCL</td><td>I</td><td>Shift clock of display data (falling edge trigger).</td></tr>
<tr><td>LP</td><td>I</td><td>Latch pulse of display data (falling edge trigger).</td></tr>
<tr><td>EIO1, EIO2</td><td>I/O</td><td>Enable I/O, which is controlled by SHL input. Output is reset by LP, and automatically falls when 80 bits of data are taken in.</td></tr>
<tr><td>SHL</td><td>I</td><td>Shift direction selection and EIO pin I/O control.
When data (a, b, c, d) (e, f, g, h)……(w, x, y, z) are input to pins (D3, D2, D1, D0) respectively, the following relation is established between the data and segment outputs:
<table>
<tr><th rowspan="2">SHL</th><th colspan="13">SEG</th><th colspan="2">EIO</th></tr>
<tr><th>79</th><th>78</th><th>77</th><th>76</th><th>75</th><th>74</th><th>73</th><th>72</th><th>……</th><th>3</th><th>2</th><th>1</th><th>0</th><th>1</th><th>2</th></tr>
<tr><td>L</td><td>a</td><td>b</td><td>c</td><td>d</td><td>e</td><td>f</td><td>g</td><td>h</td><td>……</td><td>w</td><td>x</td><td>y</td><td>z</td><td>Output</td><td>Input</td></tr>
<tr><td>H</td><td>z</td><td>y</td><td>x</td><td>w</td><td>v</td><td>u</td><td>t</td><td>s</td><td>……</td><td>d</td><td>c</td><td>b</td><td>a</td><td>Input</td><td>Output</td></tr>
</table></td></tr>
<tr><td>FR</td><td>I</td><td>AC signal of LCD driving outputs.</td></tr>
<tr><td>V_{DD}, V_{SS}</td><td>Power supplies</td><td>Logic circuit power. V_{DD}: 0V (GND)
V_{SS}: −5.0V</td></tr>
<tr><td>V0, V2, V3, V5</td><td>Power supplies</td><td>LCD driving power. V5: −12 to −28V
$V_{DD} \geqq V0 \geqq V2 > V3 \geqq V5$</td></tr>
</table>

■ABSOLUTE MAXIMUM RATINGS

(V_{DD}=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage (1)	V_{SS}	−7.0 to +0.3	V
Supply voltage (2)	V5	−30.0 to +0.3	V
Supply voltage (2)	V0,V2,V3*	V5−0.3 to +0.3	V
Input voltage (1)	V_I	V_{SS}−0.3 to +0.3	V
Output voltage (1)	V_O	V_{SS}−0.3 to +0.3	V
Output current (1)	I_O	20	mA
Output current (2)	I_{OSEG}	20	mA
Allowable power dissipation	P_D	300	mW
Operating temperature	T_{opr}	−20 to +75	°C
Storage temperature	T_{stg}	−65 to +150	°C
Soldering temperature·time	T_{sol}	260°C, 10s (at lead)	—

*V0, V2 and V3 must always satisfy the condition: $V_{DD} \geqq V0 \geqq V2 \geqq V3 \geqq V5$.

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

(Unless otherwise specified, V_{DD}=V0=0V, V_{SS}=−5.0V±10%, and Ta=−20 to 75°C)

Parameter	Symbol	Conditions		Pin	Min	Typ	Max	Unit
Operating voltage (1)	V_{SS}			V_{SS}	−5.5	−5.0	−4.5	V
Recommended operating voltage Minimum operating voltage	V5			V5	−28.0	—	−12.0 −8.0	V
Operating voltage (2)	—	Recomended value		V0	−2.5	—	0	V
Operating voltage (3)	V2	Recomended value		V2	3/9·V5	—	V0	V
Operating voltage (4)	V3	Recomended value		V3	V5	—	6/9·V5	V
"H" input voltage	V_{IH}			EI01,EI02,XSCL, LP,D0 to D3,FR,SHL	0.2V_{SS}	—	—	V
"L" input voltage	V_{IL}				—	—	0.8V_{SS}	V
"H" output voltage	V_{OH}	I_{OH}=−0.6mA		EI01, EI02	−0.4	—	—	V
"L" output voltage	V_{OL}	I_{OL}=0.6mA			—	—	V_{SS}+0.4	V
Input leakage current	I_{LI}	$V_{SS} \leqq V_I \leqq 0V$		D0 to D3,XSCL, LP,SHL,FR	—	—	2.0	μA
	$I_{LI/O}$	$V_{SS} \leqq V_I \leqq 0V$		EI01, EI02	—	—	5.0	μA
Stand-by current	I_{DDS}	V5=−12.0 to −28.0V V_{IH}=V_{DD}, V_{IL}=V_{SS}		V_{DD}	—	—	25	μA
Output resistance	R_{SEG}	|ΔV_{on}|=0.5V	V5 −20.0V	SEG0 to SEG79	—	1.5	3.5	kΩ
			V5 −14.0V		—	2.0	4.5	
			V5 −8.0V		—	3.0	8.0	
Current dissipation (1)	I_{SSO1}	V_{SS}=−5.0V, V_{IH}=V_{DD}, V_{IL}=V_{SS}, f_{XSCL}=1.92MHz f_{LP}=12kHz, Frame period=60Hz Input data: Inverted bit by bit No-load		V_{SS}	—	120	500	μA
Current dissipation (2)	I_{SSO2}	V_{SS}=−5.0V, V2=−4.0V V3=−16.0V, V5=−20.0V All other conditions are same as I_{SSO1}.		V5	—	20	100	μA
Input capacitance	C_I	Ta=25°C		D0 to D3,XSCL, LP,FR,SHL	—	—	8.0	pF
	$C_{I/O}$			EI01, EI02	—	—	15.0	pF

●AC Electrical Characteristics

($V_{SS}=-5.0\pm10\%$, Ta = −20 to 75°C)

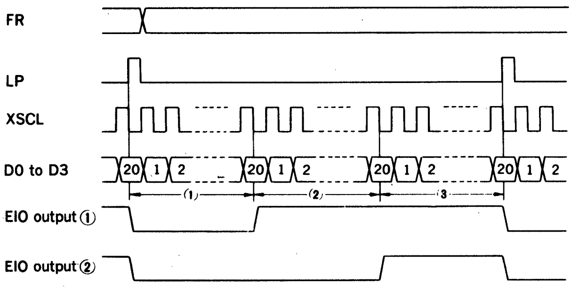
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
XSCL period	t_{CCL}	t_r, $t_f \leqq 10$ns	166	—	—	ns
XSCL "H" pulse width	t_{WCLH}		70	—	—	ns
XSCL "L" pulse width	t_{WCLL}		70	—	—	ns
Data setup time	t_{DS}		60	—	—	ns
Data hold time	t_{DH}		40	—	—	ns
XSCL-rise to LP-rise time	t_{LD}		0	—	—	ns
XSCL-fall to LP-fall time	t_{SL}		70	—	—	ns
LP-rise to XSCL-rise time	t_{LS}		70	—	—	ns
LP-fall to XSCL-fall time	t_{LH}		70	—	—	ns
LP "H" pulse width	t_{WLPH}		70	—	—	ns
LP "L" pulse width	t_{WLPL}		230	—	—	ns
Alloable FR delay time	t_{DFR}		−500	—	500	ns
Enable "H" setup time	t_{suEIH}		40	—	—	ns
Enable "H" hold time	t_{hEIH}		0	—	—	ns
Enable "L" setup time	t_{suEIL}		0	—	—	ns
Enable "L" hold time	t_{hEIL}		0	—	—	ns
Input signal rise time	t_r		—	—	50*	ns
Input signal fall time	t_f		—	—	50*	ns

*The specifications for t_r and t_f are provided to prevent a malfunction which may occur when noise is mixed with a slow-down signal. To assure high-speed XSCL, both t_r and t_f must satisfy the following relation:

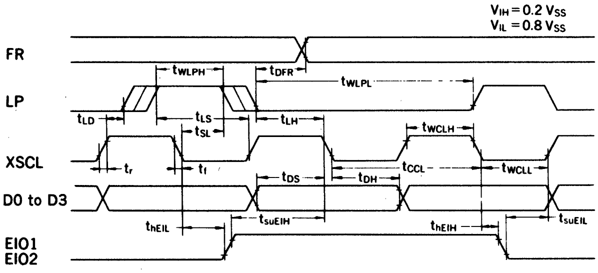
$$t_r,\ t_f < \frac{t_{CCL}-(t_{WCLH}+t_{WCLL})}{2}$$

●Timing Chart

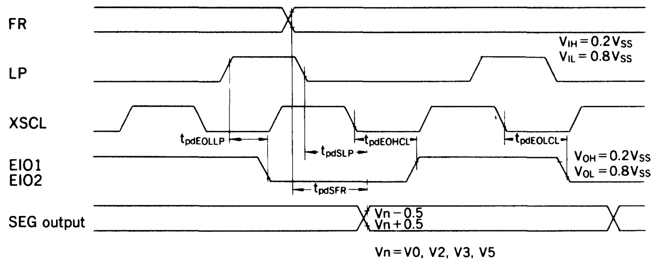
○Input Timing



① through ③ each show a cascade number of the driver.



○ Output Timing



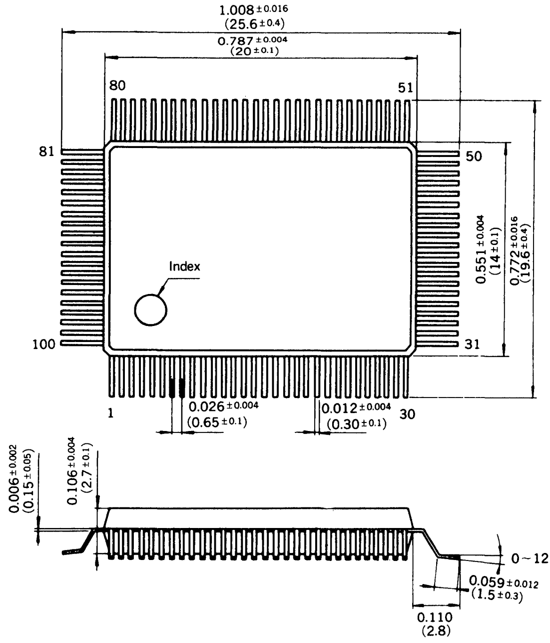
($V_{SS} = -5.0 \pm 10\%$, Ta = −20 to 75°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
(LP-rise to disable) time	$t_{pdEOLLP}$	XSCL = "L" $C_L = 15$pF	—	—	70	ns
(XSCL-fall to disable) time	$t_{pdEOLCL}$	LP = "H"	—	—	70	ns
(XSCL-fall to enable) time	$t_{pdEOHCL}$		—	—	100	ns
(LP-fall to SEG output) time	t_{pdSLP}	V5 = −12.0 to −28.0V $C_L = 100$pF	—	—	4.5	μs
(FR to SEG output) delay time	t_{pdSFR}		—	—	4.5	μs

■PACKAGE DIMENSIONS

F100-5

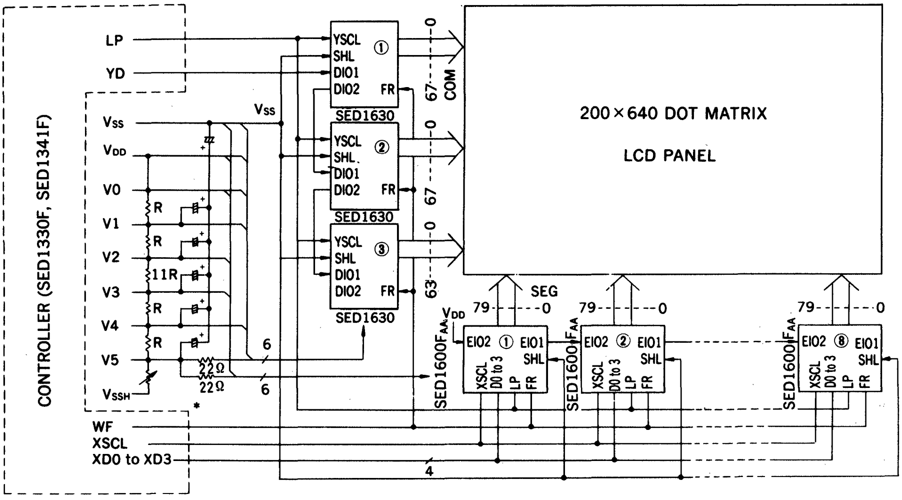
100-pin QFP



unit : inch
(mm)

■EXAMPLE OF APPLICATION (SED1600F$_{AA}$)

for 200×640 DOT MATRIX LCD



*Be sure to connect a current limitter resistor. Also, connect decoupling capacitors (0.01ΩF) near pins Vss and V5 of each LSI for noise protection.

PF365-01

SED1610F

CMOS DOT MATRIX HIGH DUTY LCD DRIVER

●86-bit High Voltage Resistant Output
●Max 1/200 in Display Duty
●CMOS High Voltage Resistant Process

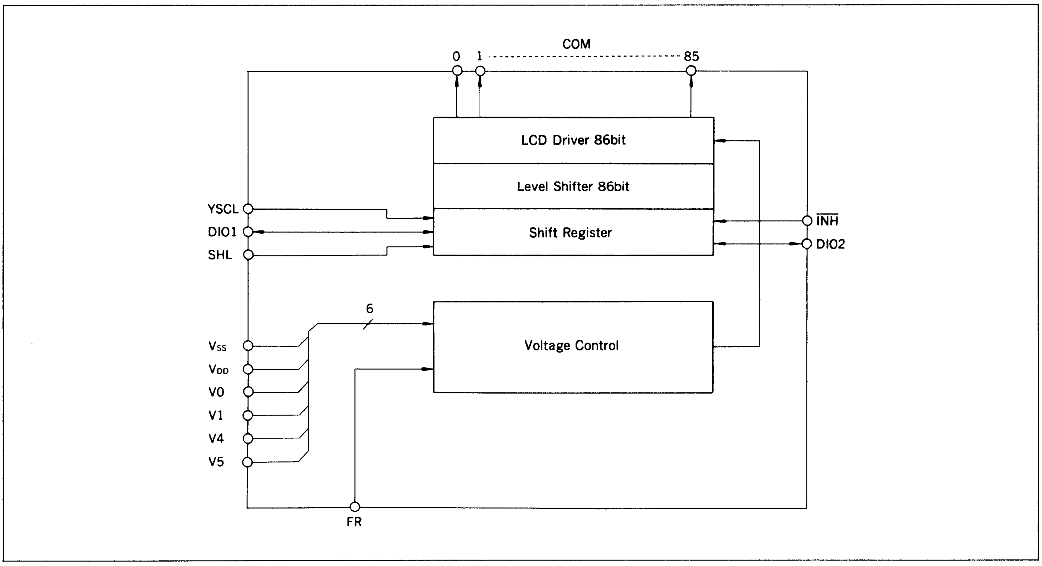
■DESCRIPTION

The SED1610F is an 86 output common (row) driver, used to driver large-capacity dot matrix LCD panels with a duty ratio of up to 1/200. It is used in conjuction with the SED1600F. The SED1610F has a wide range of drive voltages. The maximum voltage V0 is isolated from V_{DD} to enable the application of any external LCD driving bias voltage from outside to the SED1610F. These unique features enable the SED1610F to operate with a wide variety of LCD panels.

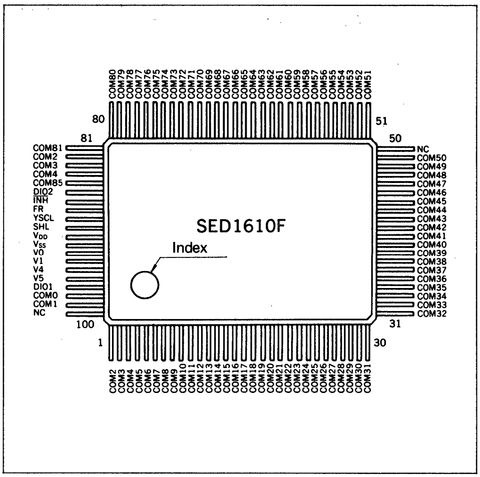
■FEATURES

●86 LCD driving outputs
●Display capacity ·································640×200×3 dots when combined with SED1600F
●Wide range of LCD driving voltages ·········12 to 28V
  (Absoulte maximum voltage··············30V)
  (Display duty ratio··························1/ {2×(n+1)}, where n = 1, 2, ······ positive integer)
●Output shift direction pin selectable
●Momentary display blanking by inhibit function
●Power supply for the logic·······················5V±10%
●Ability to adjust offset bias of LCD source from V_{DD}
●Silicon gate CMOS process
●Package···100-pin QFP (plastic)

■BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

<table>
<tr><th>Pin name</th><th>Functions</th></tr>
<tr><td>COM0 to COM85</td><td>LCD driving common (row) outputs.
Each output changes at the falling edge of YSCL.</td></tr>
<tr><td>$\overline{\text{INH}}$</td><td>Controls all common outputs to nonselect level (V4 when FR=L, V1 when FR=H) (low active)</td></tr>
<tr><td>YSCL</td><td>Shift clock of serial data (falling edge trigger).</td></tr>
<tr><td>DIO1, DIO2</td><td>Serial transfer data I/O, which is controlled by SHL input. Output changes at falling edge of YSCL.</td></tr>
<tr><td>SHL</td><td>Shift direction selection and DIO pin control.
<table>
<tr><th rowspan="2">SHL</th><th rowspan="2">COM output shift direction</th><th colspan="2">DIO</th></tr>
<tr><th>1</th><th>2</th></tr>
<tr><td>L</td><td>85 ←——— 0</td><td>Input</td><td>Output</td></tr>
<tr><td>H</td><td>85 ———→ 0</td><td>Output</td><td>Input</td></tr>
</table></td></tr>
<tr><td>FR</td><td>AC signal of LCD driving outputs.</td></tr>
<tr><td>V_{DD}, V_{SS}</td><td>Logic circuit power. V_{DD}: 0V (GND)
V_{SS}: −5.0V</td></tr>
<tr><td>V0, V1, V4, V5</td><td>LCD driving power. V5: −12 to −28V
$V_{DD} \geqq V0 > V1 > V4 > V5$</td></tr>
</table>

ABSOLUTE MAXIMUM RATINGS

(V_{DD}=0V)

Parameter	Symbol	Ratings	Unit	Parameter	Symbol	Ratings	Unit
Supply voltage (1)	V_{SS}	−7.0 to +0.3	V	Output current (2)	I_{OSEG}	20	mA
Supply voltage (2)	V5	−30.0 to +0.3	V	Operating temperature	T_{opr}	−20 to +75	℃
Supply voltage (2)	V0,V1,V4	V5−0.3 to +0.3	V	Storage temperature	T_{stg}	−65 to +150	℃
Input voltage (1)	V_I	V_{SS}−0.3 to +0.3	V	Soldering temperature·time	T_{sol}	260℃, 10s (at lead)	—
Output voltage (1)	V_O	V_{SS}−0.3 to +0.3	V	Allowable power dissipation	P_D	300	mW
Output current (1)	I_O	20	mA				

ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

(Unless otherwise specified, V_{DD}=V0=0V, V_{SS}=−5.0V±10%, and Ta=−20 to 75℃)

Parameter	Symbol	Conditions			Pin	Min	Typ	Max	Unit
Operating voltage (1)	V_{SS}				V_{SS}	−5.5	−5.0	−4.5	V
Recommended operating voltage Minimum operating voltage	V5				V5	−28.0	—	−12.0 −8.0	V
Operating voltage (2)	V0				V0	−2.5	—	0	V
"H" input voltage	V_{IH}				DIO1, DIO2, YSCL, FR, SHL, $\overline{\text{INH}}$	0.2V_{SS}	—	—	V
"L" input voltage	V_{IL}					—	—	0.8V_{SS}	V
"H" output voltage	V_{OH}	I_{OH}=−0.6mA			DIO1, DIO2	−0.4	—	—	V
"L" output voltage	V_{OL}	I_{OL}=0.6mA				—	—	V_{SS}+0.4	V
Input leakage current	I_{LI}	$V_{SS} \leqq V_I \leqq 0V$			YSCL, SHL, $\overline{\text{INH}}$, FR	—	—	2.0	μA
	$I_{LI/O}$	$V_{SS} \leqq V_I \leqq 0V$			DIO1, DIO2	—	—	5.0	μA
Stand-by current	I_{DDS}	V5=−12.0 to −28.0V $V_{IH}=V_{DD}$, $V_{IL}=V_{SS}$			V_{DD}	—	—	25	μA
Output resistance	R_{SEG}	$\lvert \Delta V_{on} \rvert$=0.5V	V5	−20.0V	COM0 to COM85	—	1.1	1.8	KΩ
				−14.0V		—	1.2	2.0	
				−8.0V		—	2.0	4.0	

continued

Parameter	Symbol	Condition	Pin	Min	Typ	Max	Unit
Current dissipation (1)	I_{SSO1}	$V_{SS}=-5.0V$, $V_{IH}=V_{DD}$, $V_{IL}=V_{SS}$, $f_{YSCL}=7.7KHz$ Frame period=60Hz Input data: "H" every 1/128 duty No-load	V_{SS}	—	7	15.0	μA
Current dissipation (2)	I_{SSO2}	$V_{SS}=-5.0V$, $V1=-2.0V$ $V4=-18.0V$, $V5=-20.0V$ All other conditions are same as I_{SSO1}	V5	—	7	15.0	μA
Input capacitance	C_I	Ta=25°C	YSCL, SHL, $\overline{INH}$, FR	—	—	8.0	pF
	$C_{I/O}$		DIO1, DIO2	—	—	15.0	pF

●AC Characteristics

○Input Timing

($V_{SS}=-5.0V\pm10\%$, Ta=−20 to 75°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
YSCL period	t_{CCL}		500	—	—	ns
YSCL "H" pulse width	t_{WCLH}		70	—	—	ns
YSCL "L" pulse width	t_{WCLL}		330	—	—	ns
Data setup time	t_{DS}		100	—	—	ns
Data hold time	t_{DH}		10	—	—	ns
Allowable FR delay time	t_{DFR}		−500	—	500	ns
Input signal rise time	t_r		—	—	50	ns
Input signal fall time	t_f		—	—	50	ns

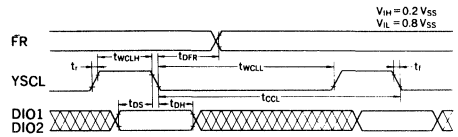
○Output Timing

($V_{SS}=-5.0V\pm10\%$, Ta=−20 to 75°C)

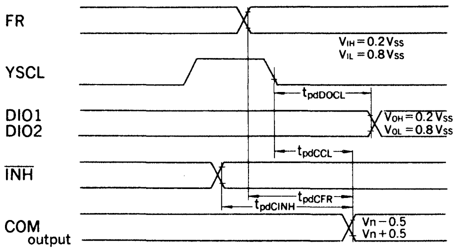
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
(YSCL-fall to DIO) Delay time	t_{pdDOCL}	$C_L=15pF$	30	—	300	ns
(YSCL-fall to COM output) Delay time	t_{pdCCL}	$V5=-12.0$ to $-28.0V$ $C_L=100pF$	—	—	3.0	μs
($\overline{INH}$ to COM output) Delay time	t_{pdCINH}					
(FR to COM output) Delay time	t_{pdCFR}		—	—	3.0	μs

●Timing Chart

○Input Timing

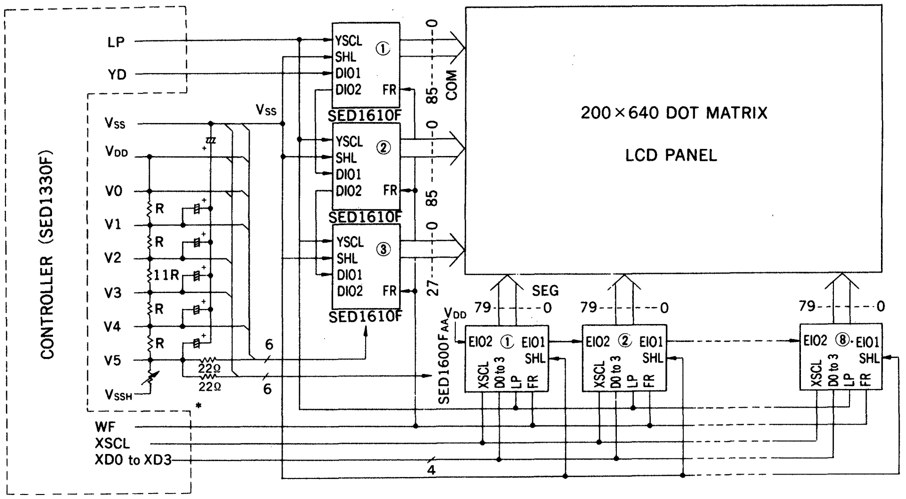


○Output Timing



■EXAMPLE OF APPLICATION

for 200×640 DOT MATRIX LCD

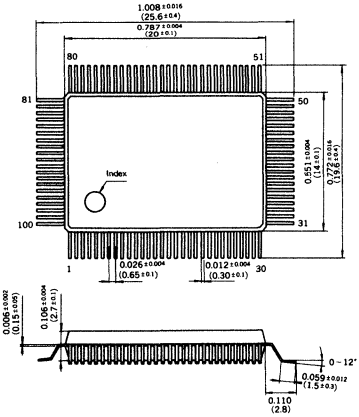


*Be sure to connect a current limitter resistor. Also, connect decoupling capacitors (0.01μF) near pins Vss and V5 of each LSI for noise protection.

■PACKAGE DIMENSIONS

F100-5

100-pin QFP



unit : inch
(mm)

SED1200F$_{\text{OB}}$

CMOS DOT MATRIX LCD CONTROLLER DRIVER

- 1/8 or 1/16 Duty Cycle Dot Matrix Drive
- 20 Character Simultaneous Display
- Built in Character Generator ROM and RAM

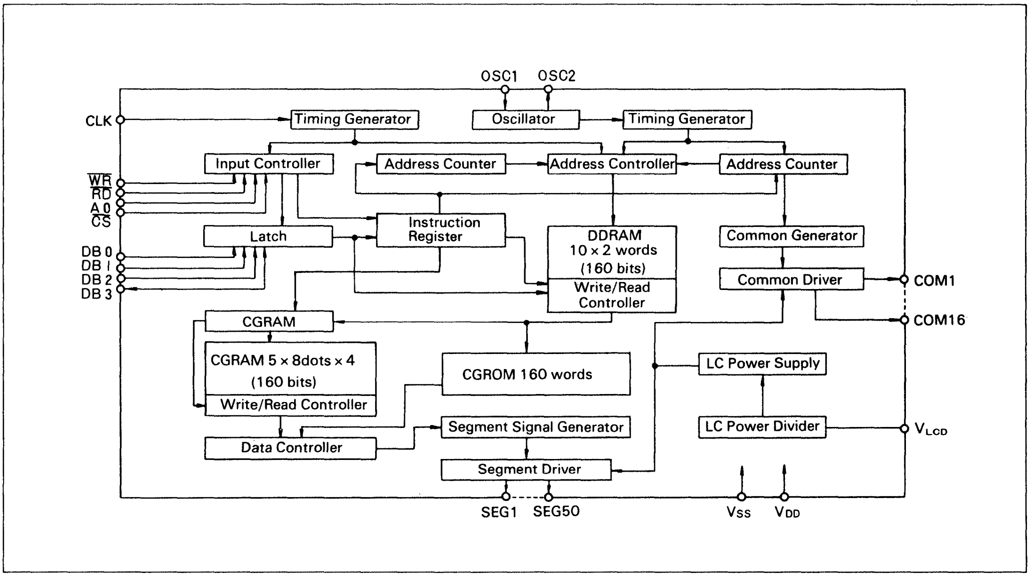
■ DESCRIPTION

The SED1200F$_{\text{OB}}$ is a dot matrix LCD controller/driver with a built in CG (character generator).
The circuit consists of a CG ROM which contains 160 different characters, 4 words CG RAM, 20 words display data RAM and logic functions to operate a 20 character display. Additional characters may be used by writing CG data to the 4 words CG RAM.
The device also contains the resistor array for the LCD power supply. The SED1200F$_{\text{OB}}$ is fabricated Silicon Gate CMOS process and features very low power dissipation. This makes the device very desirable for applications in hand held, portable and other battery powered instruments.

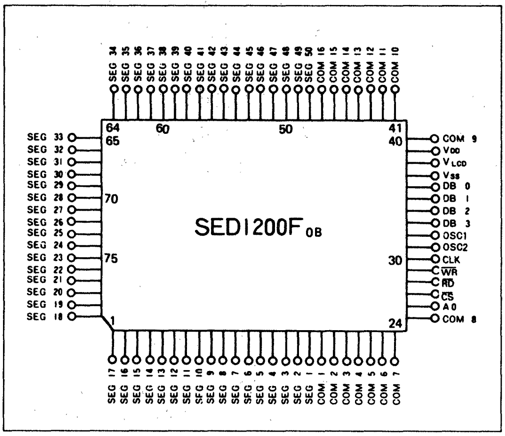
■ FEATURES

- 1/8 or 1/16 Duty cycle dot matrix drive
- 20 Character simultaneous display
- Built in character generator ROM and RAM
- Built in CR oscillator
- Built in resistor array for LCD power supply
- Compatible with 4 or 8 bit microprocessors
- TTL Compatible
- 5 x 7 + Cursor line or 5 x 8 character font
- Package·······80-pin QFP (plastic)

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



■ PIN DESCRIPTION

Pin No.	Pin Name	I/O	Functions
18 to 25 40 to 47	COM1 to COM16	O	LCD Common output
17 to 1 80 to 48	SEG1 to SEG50	O	LCD Segment output
27	$\overline{\text{CS}}$	I	Chip select input (active "Low")
28	$\overline{\text{RD}}$	I	Read enable input (active "Low")
29	$\overline{\text{WR}}$	I	Write enable input (active "Low" to "High")
26	A0	I	"High"; Set character code, "Low"; Command
36 to 33	DB0 to DB3	I, I/O	Data input (except DB3; Data input/output)
30	CLK	I	Clock for command
32, 31	OSC1, OSC2	–	Connect oscillation resistor
39	VDD	–	Supply voltage (+5V) for logic
37	VSS	–	GND (0V)
38	VLCD	–	Supply voltage for LCD

■ ABSOLUTE MAXIMUM RATINGS

(Vss = 0V)

Parameter	Symbol	Ratings	Unit
Supply voltage (1)	V_{DD}	−0.3 to +7.0	V
Supply voltage (2)	V_{LCD}	V_{DD} −7.0 to V_{DD} +0.3	V
Input voltage	V_I	−0.3 to V_{DD} +0.3	V
Output voltage	V_O	−0.3 to V_{DD} +0.3	V
Operating temperature	T_{opr}	−10 to +70	℃
Storage temperature	T_{stg}	−65 to +150	℃

■ ELECTRICAL CHARACTERISTICS

● AC Characteristics (Read cycle)

(V_{DD} = 5V ± 10%, Vss = 0V, Ta = −10 to +70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
A0 setup time to $\overline{\text{RD}}$	t_{AR}		0	–	–	ns
$\overline{\text{CS}}$ setup time to $\overline{\text{RD}}$	t_{CR}		0	–	–	ns
Output delay time from $\overline{\text{RD}}$	t_{RD}		–	–	250	ns
A0 hold time after $\overline{\text{RD}}$	t_{RA}		20	–	–	ns
$\overline{\text{CS}}$ hold time after $\overline{\text{RD}}$	t_{RC}		20	–	–	ns
Data hold time	t_{RH}		10	–	–	ns
Read pulse width	t_{RP}		350	–	–	ns
Input fall time	t_{HL}		–	–	50	ns
Input rise time	t_{LH}		–	–	50	ns

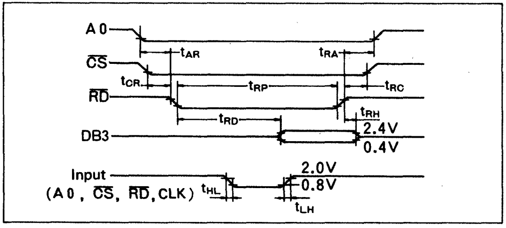
● AC Characteristics (Write cycle)

(V_{DD} = 5V ± 10%, Vss = 0V, Ta = −10 to +70°C)

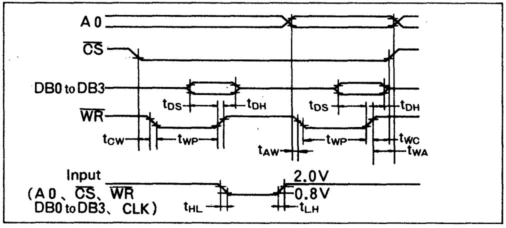
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
A0 setup time to $\overline{\text{WR}}$	t_{AW}		0	–	–	ns
$\overline{\text{CS}}$ setup time to $\overline{\text{WR}}$	t_{CW}		0	–	–	ns
Data setup time	t_{DS}		120	–	–	ns
A0 hold time after $\overline{\text{WR}}$	t_{WA}		20	–	–	ns
$\overline{\text{CS}}$ hold time after $\overline{\text{WR}}$	t_{WC}		20	–	–	ns
Data hold time	t_{DH}		20	–	–	ns
Write pulse width	t_{WP}		200	–	–	ns
Input fall time	t_{HL}		–	–	50	ns
Input rise time	t_{LH}		–	–	50	ns

● Timing Chart

(Read cycle)



(Write cycle)



● DC Characteristics

(V_{SS} = 0V, Ta = −10 to +70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Logic operating voltage	V_{DD}		4.5	5	5.5	V
LCD operating voltage	V_{LCD}		V_{DD}−5.5	–	V_{DD}−4	V
Resistor for oscillator	Rf	V_{DD} = 5V, f_{OSC} = 100kHz	240	310	380	kΩ
Input voltage ; High (1)	V_{IH1}	V_{DD} = 4.5 to 5.5V *1	2.0	–	V_{DD}	V
Input voltage ; Low (1)	V_{IL1}	V_{DD} = 4.5 to 5.5V *1	0	–	0.8	V
Input leakage current ; High	I_{LIH}	V_{DD} = 5.5V, V_{IH} = 5.5V *2	–	–	1.0	μA
Input leakage current ; Low	I_{LIL}	V_{DD} = 5.5V, V_{IL} = 0V *2	–	–	1.0	μA
Input voltage ; High (2)	V_{IH2}	V_{DD} = 4.5 to 5.5V *3	0.8V_{DD}	V_{DD}	V_{DD}	V
Input voltage ; Low (2)	V_{IL2}	V_{DD} = 4.5 to 5.5V *3	0	0	0.2V_{DD}	V
Output current ; High	I_{OH}	V_{DD} = 5V, V_{OH} = 2.4V *4	1.0	–	–	mA
Output current ; Low	I_{OL}	V_{DD} = 5V, V_{OL} = 0.4V *4	1.6	–	–	mA
Input pull up current	I_{IPU}	V_{IL} = 0V, V_{DD} = 5V *5	3	10	30	μA
Resistor as power divider	Rd		30	130	300	kΩ
Operating frequency (1)	fosc	V_{DD} = 4.5 to 5.5V	–	100	300	kHz
Operating frequency (2)	CLK	V_{DD} = 4.5 to 5.5V	–	–	3.2	MHz
Operating current	I_{DD}	V_{DD} = 5V, V_{LCD} = 0V *6 fosc = 100KHz, CLK = 1MHz	–	80	150	μA
Command execution time	t_{COMD}		–	–	16/CLK (MHz)	μs
Common output current (1)	$\|I_{OH}\ V_{DDC}\|$	V_{DD} = 4.5V V_{LCD} = 1.0V 1/16 duty drive Voltage drop by 0.5V When one terminal is measured, the others are open.	20	–	–	μA
Common output current (2)	$I_{OL}\ V_{LCDC}$		20	–	–	μA
Common output current (3)	$\|I_{OL}\ V_{L1C}\|$		8	–	–	μA
Common output current (4)	$\|I_{OL}\ V_{L4C}\|$		8	–	–	μA
Segment output current (1)	$\|I_{OL}\ V_{DDS}\|$		12	–	–	μA
Segment output current (2)	$I_{OL}\ V_{LCDS}$		12	–	–	μA
Segment output current (3)	$\|I_{OL}\ V_{L2S}\|$		4	–	–	μA
Segment output current (4)	$\|I_{OL}\ V_{L3S}\|$		4	–	–	μA

*1. Terminal: $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, A0, DB0 to DB3, CLK

*2. Terminal: CLK, OSC1, DB0 to DB3

*3. Terminal: OSC1 (for external clock)

*4. Terminal: DB3

*5. Terminal: $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, A0

*6. $\overline{CS}$ = $\overline{RD}$ = $\overline{WR}$ = A0 = 5.0V, (open output terminals)

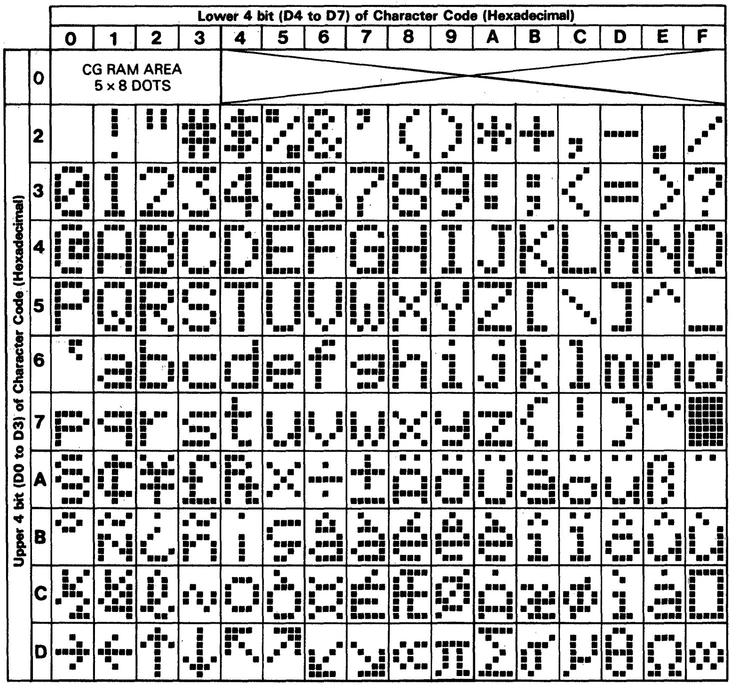
■ DISPLAY COMMAND

Command Name		$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	A0	1st input				2nd input				Note
						DB3 (D7)	DB2 (D6)	DB1 (D5)	DB0 (D4)	DB3 (D3)	DB2 (D2)	DB1 (D1)	DB0 (D0)	
SET CURSOR DIRECTION		0	0	1	0	0	0	0	0	0	1	0	D/I	D0 = 1 : Decrement D0 = 0 : Increment
CURSOR ADDRESS −1/+1		0	0	1	0	0	0	0	0	0	1	1	−1/+1	D0 = 1 : −1 D0 = 0 : +1
CURSORFONT SELECT		0	0	1	0	0	0	0	0	1	0	0	A/U	D0 = 1 : All dots blinking D0 = 0 : Under line
CURSOR BLINK ON/OFF		0	0	1	0	0	0	0	0	1	0	1	ON/OFF	D0 = 1 : ON D0 = 0 : OFF
DISPLAY ON/OFF		0	0	1	0	0	0	0	0	1	1	0	ON/OFF	D0 = 1 : ON D0 = 0 : OFF
CURSOR ON/OFF		0	0	1	0	0	0	0	0	1	1	1	ON/OFF	D0 = 1 : ON D0 = 0 : OFF
SYSTEM RESET		0	0	1	0	0	0	0	1	0	0	0	0	Except data RAM and CGRAM
LINE SELECT		0	0	1	0	0	0	0	1	0	0	1	2/1	D0 = 1 : 2 line display (1/16 duty) D0 = 0 : 1 line display (1/ 8 duty)
SET CURSOR ADDRESS	1st LINE	0	0	1	0	1	0	(N figure −1) B						
	2nd LINE	0	0	1	0	1	1	(N figure −1) B						
SET CHARACTER CODE		0	0	1	1	(CHARACTER CODE)								
BUSY FLAG CHECK		0	1	0	0	BF	*	*	*	BF	*	*	*	D7(D3) = 1 : Busy D7(D3) = 0 : Not Busy
SET CGRAM ADDRESS		0	0	1	0	0	0	1	0	(Set lower address)				
SET CGRAM DATA		0	0	1	0	0	1	0	(Set CGRAM data)					

* = High impedance

Note: Misoperation may be caused when any command other than that listed in the above table is inputted.

CHARACTER CODE MAP (SED1200F0B)



Lower 4 bit (D4 to D7) of Character Code (Hexadecimal)

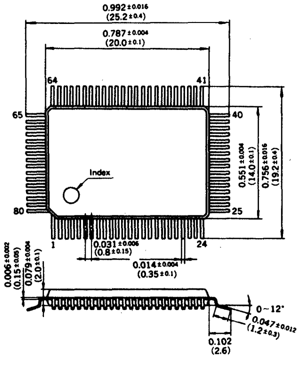
Upper 4 bit (D0 to D3) of Character Code (Hexadecimal)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	CG RAM AREA 5 × 8 DOTS															
2		!	"	#	$	%	&	'	(	)	*	+	,	-	.	/
3	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
4	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
5	P	Q	R	S	T	U	V	W	X	Y	Z	[	\	]	^	_
6	`	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
7	p	q	r	s	t	u	v	w	x	y	z	{	|	}	~	█
A	§	¢	¥	£	₧	×	÷	±	Ä	Ö	Ü	ä	ö	ü	ß	¨
B	°	Ñ	¿	ñ	¡	ç	â	à	é	ê	è	î	ï	ô	û	ù
C	[illegible]	[illegible]	[illegible]	[illegible]	o	ò	ø	É	Æ	ø	ô	æ	φ	ì	à	□
D	→	←	↑	↓	↖	↗	↙	↘	α	π	Σ	τ	μ	θ	Ω	ω

PACKAGE DIMENSIONS

F80

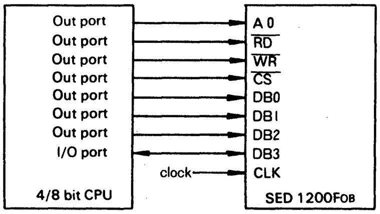
80-pin QFP



unit : inch
(mm)

APPLICATION FOR CPU

The SED1200F0B can connect to the address bus or the data bus directly or alternatively, a peripheral interface unit. An example is shown below.



SED1210F$_{\mathrm{OB}}$

CMOS DOT MATRIX LCD CONTROLLER DRIVER

●1/8 or 1/16 Duty Cycle Dot Matrix Drive
●Built-in Character Generator ROM and RAM
●Maximum Simultaneous Display of 40 Characters (When Accompanied with SED1181F$_{\mathrm{LA}}$)

■DESCRIPTION

The SED1210F$_{\mathrm{0B}}$ is a dot matrix LCD controller/driver with a built in CG (character generator).

The circuit consists of a CG ROM which contains 160 different characters, 4 characters CG RAM, 40 words display data RAM and logic functions to operate a 40 character display. Additional characters may be used by writing CG data to the 4 characters CG RAM.

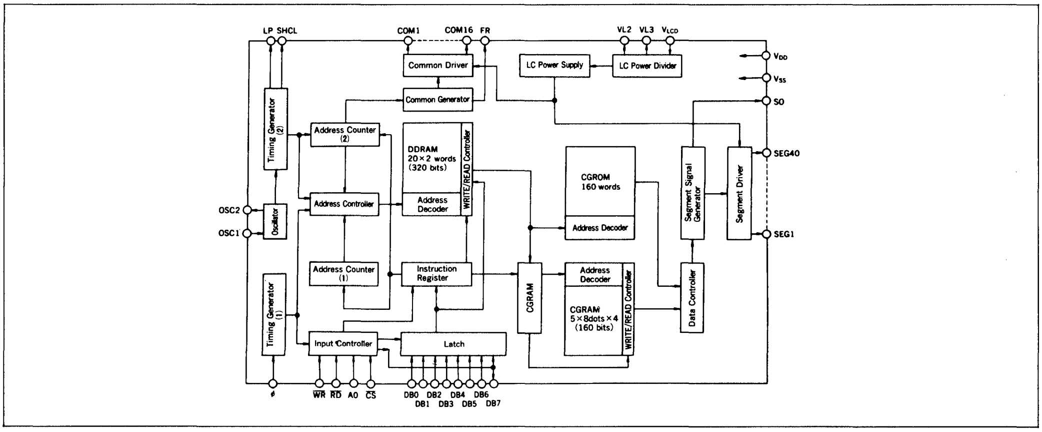
The device also contains the resistor array for the LCD power supply. The SED1210F$_{\mathrm{0B}}$ is fabricated Silicon Gate CMOS process and features very low power dissipation. This makes the device very desirable for applications in hand held, portable and other battery powered instruments.

Since 1210F$_{\mathrm{0B}}$ consists of 40 segment drivers and 16 common drivers on one chip, at most 16 characters are displayed, Accompanied with SED1181F$_{\mathrm{LA}}$, number of characters can be expanded to 40 characters at most.

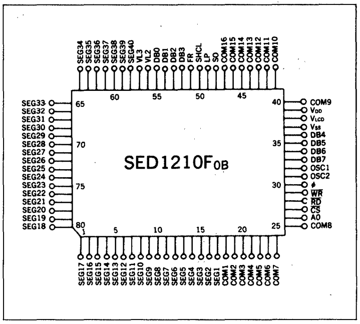
■FEATURES

- CMOS LSI
- Built in display data RAM ······················40×8 bits : 40 characters (Max)
- Built in character generator ROM (160 different characters) and CGRAM (4 words)
- Built in CR oscillator circuit (External Resistance)
- Built in resistor array for LCD power supply
- Maximum display dimension ····················20 characters×2 lines or 40 characters×1 line (with SED1181F$_{\mathrm{LA}}$ accompanied)
- 1/8 or 1/16 duty cycle dot matrix drive (fixed by command)
- Capable of interfacing to 4 or 8 bit CPU
- 13 simple commands for operation
- 5×7+Cursor line or 5×8 character font
- Cursor font···Underline or all dots blinking
- Low power dissipation
- Single power supply ····························2.5V to 5.5V (Logic)
- Package···80-pin QFP (plastic)

■BLOCK DIAGRAM



■PIN CONFIGURATION



■PIN DESCRIPTION

Pin Name	Functions	No. of Pin	Pin Name	Functions	No. of Pin
COM1 to 16	LCD common output	16	SO	Serial output for Segment driver	1
SEG1 to 40	LCD segment output	40	LP	Latch output for Segment driver	1
$\overline{CS}$	Chip select input (active "Low")	1	SHCL	Shift clock for Segment driver	1
$\overline{RD}$	Read enable input (active "Low")	1	FR	Frame output for Segment driver	1
$\overline{WR}$	Write enable input (active "Low" to "High")	1	VL2, VL3	Supply voltage for Segment driver	2
A0	"High" ; Set character code "Low" ; Command	1	V_{DD}	Supply voltage (2.5V to 5.5V) for logic	1
DB0 to 7	Data input (except DB7 ; Data input/output)	8	V_{SS}	GND (0V)	1
ϕ	Clock for command	1	V_{LCD}	Supply voltage for LCD $3.5V \leqq V_{DD}-V_{LCD} \leqq 5.5V$	1
OSC1, OSC2	Connect oscillation resistor between OSC1 and OSC2. OSC1 also can be external clock input.	2			

■ABSOLUTE MAXIMUM RATINGS

($V_{SS}=0V$, $Ta=25°C$)

Parameter	Symbol	Ratings	Unit
Supply voltage (1)	V_{DD}	-0.3 to 7.0	V
Supply voltage (2)	V_{LCD}	$V_{DD}-7.0$ to $V_{DD}+0.3$	V
Input voltage	V_I	-0.3 to $V_{DD}+0.3$	V
Output voltage	V_O	-0.3 to $V_{DD}+0.3$	V
Operating temperature	T_{opr}	-20 to 70	°C
Storage temperature	T_{stg}	-65 to 150	°C
Soldering temperature and time	T_{sol}	260°C·10s (at lead)	—

■ELECTRICAL CHARACTERISTICS

●DC Characteristics

($V_{SS}=0V$, $Ta=-20$ to $75°C$)

Parameter	Symbol	Conditions	Terminal	Min	Typ	Max	Unit
Logic operating voltage	V_{DD}		V_{DD}	2.5	5.0	5.5	V
LCD operating voltage	V_{LCD}		V_{LCD}	$V_{DD}-5.5$	—	$V_{DD}-3.5$	V
Resistor for oscillator	R_f	$V_{DD}=5.0V$, $f_{OSC}=100kHz$	OSC1	240	310	380	kΩ
Operating frequency (1) (of oscillation or external clock)	f_{OSC}	$V_{DD}=4.5$ to $5.5V$	OSC2	—	100	300	kHz
Operating frequency (2)	ϕ		ϕ	—	—	3.2	MHz
External clock duty			OSC1, ϕ	45	50	55	%
Input voltage ; High (1)	V_{IH1}		$\overline{CS}$, $\overline{RD}$ $\overline{WR}$, A0 DB0 to 7 ϕ	2.0	—	V_{DD}	V
Input voltage ; Low (1)	V_{IL1}			0	—	0.8	V
Input voltage ; High (2)	V_{IH2}		OSC1	$0.8V_{DD}$	V_{DD}	V_{DD}	V
Input voltage ; Low (2)	V_{IL2}			0	0	$0.2V_{DD}$	V
Input leakage current ; High	$\lvert I_{LIH}\rvert$	$V_{DD}=5.5V$, $V_{IH}=5.5V$	ϕ, OSC1	—	—	1.0	μA
Input leakage current ; Low	$\lvert I_{LIL}\rvert$	$V_{DD}=5.5V$, $V_{IL}=0V$	DB0 to 7	—	—	1.0	μA
Input pull up current	I_{IPU}	$V_{DD}=5.0V$, $V_{IL}=0V$	$\overline{CS}$, $\overline{RD}$ $\overline{WR}$, A0	3.0	10	30	μA
Output current ; High	$\lvert I_{OH1}\rvert$	$V_{DD}=4.5$ to $5.5V$, $V_{OH}=2.4V$	DB7	1.0	—	—	mA
Output current ; Low	I_{OL1}	$V_{DD}=4.5$ to $5.5V$, $V_{OL}=0.4V$		1.6	—	—	mA
Output current ; High	$\lvert I_{OH2}\rvert$	$V_{DD}=4.5V$, $V_{OH}=4.0V$	FR, LP	200	—	—	μA
Output current ; Low	I_{OL2}	$V_{DD}=4.5V$, $V_{OL}=0.5V$	XSCL SO	200	—	—	μA
Common output current (1)	$\lvert I_{OH}V_{DDC}\rvert$	• $V_{DD}=4.5V$ • $V_{LCD}=1.0V$ • When resistance array is in low impedance • 1/16 duty drive • Voltage drop by 0.5V When one terminal is measured, the others are open.	COM1 to COM16	20	—	—	μA
Common output current (2)	$I_{OL}V_{LCDC}$			20	—	—	μA
Common output current (3)	$\lvert I_{OL}V_{L1C}\rvert$			8	—	—	μA
Common output current (4)	$\lvert I_{OL}V_{L4C}\rvert$			8	—	—	μA
Segment output current (1)	$\lvert I_{OH}V_{DDS}\rvert$		SEG1 to SEG40	12	—	—	μA
Segment output current (2)	$I_{OL}V_{LCDS}$			12	—	—	μA
Segment output current (3)	$\lvert I_{OL}V_{L2S}\rvert$			4	—	—	μA
Segment output current (4)	$\lvert I_{OL}V_{L3S}\rvert$			4	—	—	μA

●AC Characteristics

○Read Cycle

(V_{DD}=5V±10%, Ta=−20 to 75°C)

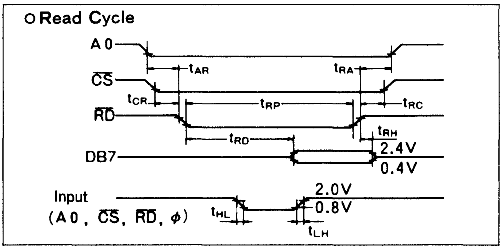
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
A0 setup time to $\overline{\text{RD}}$	t_{AR}		0	—	—	ns
$\overline{\text{CS}}$ setup time to $\overline{\text{RD}}$	t_{CR}		0	—	—	ns
Output delay time from $\overline{\text{RD}}$	t_{RD}	C_L=100pF	—	—	250	ns
A0 hold time after $\overline{\text{RD}}$	t_{RA}		20	—	—	ns
$\overline{\text{CS}}$ hold time after $\overline{\text{RD}}$	t_{RC}		20	—	—	ns
Data hold time	t_{RH}		10	—	—	ns
Read pulse width	t_{RP}		350	—	—	ns
Input fall time	t_{HL}		—	—	50	ns
Input rise time	t_{LH}		—	—	50	ns

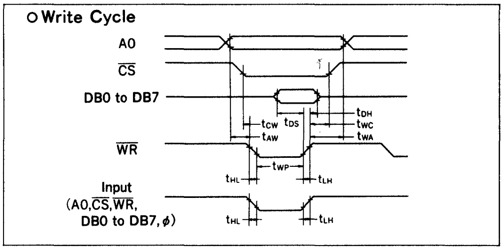
○Write Cycle

(V_{DD}=5V±10%, Ta=−20 to 75°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Address allowance time	t_{AW}		0	—	—	ns
Chip select time	t_{CW}		0	—	—	ns
Data setup time	t_{DS}		120	—	—	ns
A0 hold time after $\overline{\text{WR}}$	t_{WA}		20	—	—	ns
$\overline{\text{CS}}$ hold time after $\overline{\text{WR}}$	t_{WC}		20	—	—	ns
Data hold time	t_{DH}		20	—	—	ns
Write pulse width	t_{WP}		200	—	—	ns
Input fall time	t_{HL}		—	—	50	ns
Input rise time	t_{LH}		—	—	50	ns

● Timing Chart


○Read Cycle


○Write Cycle

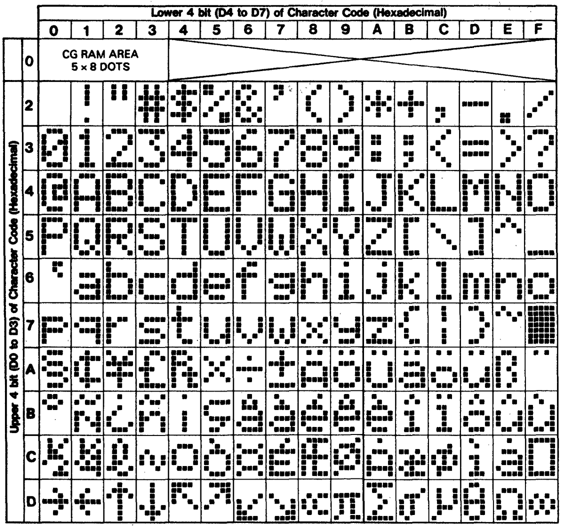
■DISPLAY COMMAND

Command Name	$\overline{\text{CS}}$	$\overline{\text{WR}}$	$\overline{\text{RD}}$	A0	D7	D6	D5	D4	D3	D2	D1	D0	Note
SET CURSOR DIRECTION	0	0	1	0	0	0	0	0	0	1	0	D/I	D0=1 : Decrement D0=0 : Increment
CURSOR ADDRESS −1/+1	0	0	1	0	0	0	0	0	0	1	1	−1/+1	D0=1 : −1 D0=0 : +1
CURSOR FONT SELECT	0	0	1	0	0	0	0	0	1	0	0	A/U	D0=1 : All dots blinking D0=0 : Under line
CURSOR BLINK ON/OFF	0	0	1	0	0	0	0	0	1	0	1	ON/OFF	D0=1 ON D0=0 OFF
DISPLAY ON/OFF	0	0	1	0	0	0	0	0	1	1	0	ON/OFF	
CURSOR ON/OFF	0	0	1	0	0	0	0	0	1	1	1	ON/OFF	
SYSTEM RESET	0	0	1	0	0	0	0	1	0	0	0	0	Except data RAM and CGRAM
LINE SELECT	0	0	1	0	0	0	0	1	0	0	1	2/1	D0=1 : 2 line display (1/16 duty) D0=0 : 1 line display (1/8 duty)
SET CGRAM ADDRESS	0	0	1	0	0	0	1	0	A3	A2	A1	A0	Upper address is fixed to 0H
SET CGRAM DATA	0	0	1	0	0	1	0	D4	D3	D2	D1	D0	
SET CURSOR ADDRESS	0	0	1	0	1	2nd/1st	A5	A4	A3	A2	A1	A0	D6=1 : N figure for second line D6=0 : N figure for first line
SET CHARACTER CODE	0	0	1	1	D7	D6	D5	D4	D3	D2	D1	D0	
BUSY FLAG CHECK	0	1	0	0	BF	*	*	*	*	*	*	*	

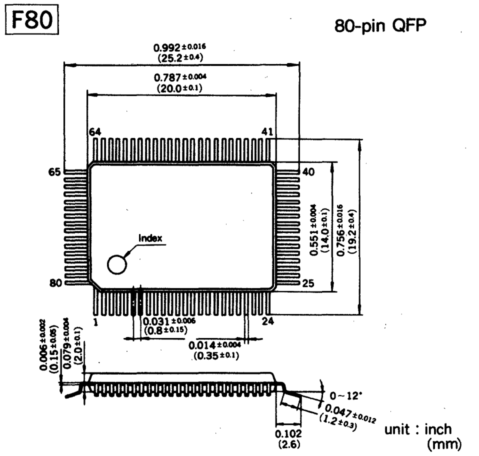
* =High impedance

Note : Misoperation may be caused when any command other than that listed in the above table is inputted.

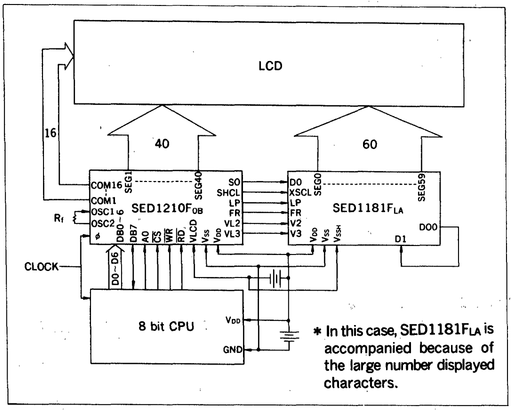
■CHARACTER CODE MAP (SED1210F$_{OB}$)



■PACKAGE DIMENSIONS



■EXAMPLE OF APPLICATION (20 characters×2 lines display)



* In this case, SED1181F$_{LA}$ is accompanied because of the large number displayed characters.

SED1210F$_{OB}$ can connect to the address bus or the data bus directly or alternatively, a peripheral interface unit.

SED1278F

CMOS DOT MATRIX LCD CONTROLLER DRIVER

- 1/8, 1/11 or 1/16 Duty Cycle Dot Matrix Drive
- Built-in Character Generator ROM and RAM (ROM 240 characters / RAM 8 characters)
- Maximum Simultaneous Display of 80 Characters (When Accompanied with SED1181FLA)

DESCRIPTION

The SED1278F is a dot matrix LCD controller/driver which is dedicated to character display. It is capable of displaying up to 80 characters under 4-bit/8-bit MPU control.

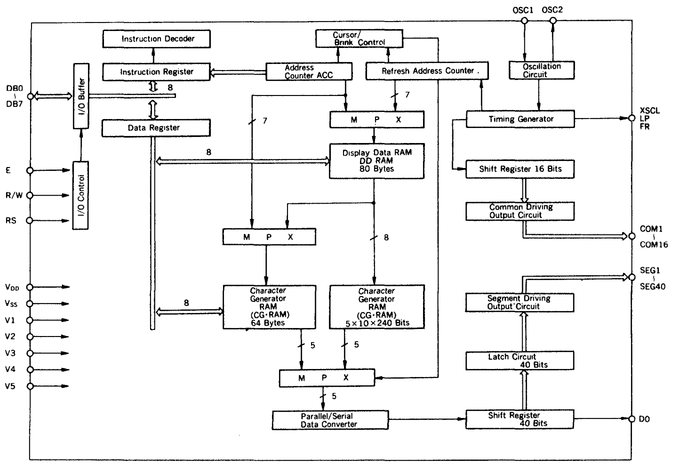
The built-in character generator ROM has an extended capacity of 240 different characters, each being generated in a 5×10 dots font compatible with a 1/11 duty. In addition, the SED1278F contains 64 bytes of character generator RAM in which the user can store 8 different characters, each consisting of 5×8 dots. These memory features offer high flexibility in character display.

The guaranteed minimum LCD driving voltage is 3V, and this makes the SED1278F suitable for driving low voltage LCDs.

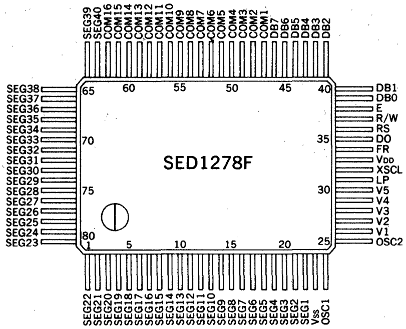
FEATURES

- Display RAM··········80 bytes (80 characters)
- Character generator ROM··········240 characters (Able to 256 characters)
- Character generator RAM··········8 characters
- Built-in CR oscillator, Built-in power-on reset circuit
- Maximum display dimension··········80 characters×1 line, 40 characters×2 lines (When accompanied with SED1181FLA)
- 1/8, 1/11 or 1/16 duty cycle matrix drive (fixed by command)
- 2 flame AC wave-form drive
- High-speed bus interface with 4-bit/8-bit MPU
- Powerful display control instructions
- Character font··········5×7 dots+Cursor line (5×8 dots also possible)
  5×10 dots+Cursor line
- Single power supply··········5V±10% (Logic)
- Low LCD driving voltage··········$V_{DD}-V_5 \geq 3.0V$
- Package··········80-pin QFP (plastic)

BLOCK DIAGRAM



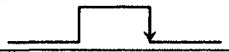
■PIN CONFIGURATION



■PIN DESCRIPTION

Symbol	No. of signals	Functions	
RS	1	Register select signal	*1
R/W	1	Read/write select signal	
E	1	Read/write execute signal	
DB0 to DB7	8	Data bus	
LP	1	Data latching pulse	
XSCL	1	Data transfer clock	
FR	1	LCD AC driving signal	
DO	1	Serial data	
COM1 to COM16	16	Common outputs COM9 to COM16 : non-select for 1/8 duty COM12 to COM16 : non-select for 1/11 duty	
SEG1 to SEG40	40	Segment outputs	
V1 to V5	5	LCD driving power ($V5 \geqq V_{SS}$)	
V_{DD}	1	+5V	
V_{SS}	1	0V (GND)	
OSC1	2	Used to connect resistor (typ. 91K-ohms) for oscillation; OSC1 is for external clock input.	
OSC2			

*1

RS	R/W	E	Operation
0	0		Instruction write cycle
0	1	1	Busy flag read cycle Address counter read cycle
1	0		DD RAM or CG RAM data write cycle
1	1	1	DD RAM or CG RAM data read cycle

■ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V, Ta=25°C)

Parameter	Symbol	Ratings	Unit
Supply voltage (1)	V_{DD}	−0.3 to 7.0	V
Supply voltage (2)	V1 to V5	−0.3 to V_{DD}+0.3	V
Input voltage	V_I	−0.3 to V_{DD}+0.3	V
Output voltage	V_O	−0.3 to V_{DD}+0.3	V
Power dissipation	P_D	300	mW
Operating temperature	T_{opr}	−20 to 75	°C
Storage temperature	T_{stg}	−65 to 150	°C
Soldering temperature and time	T_{sol}	260°C·10s (at lead)	—

Note) The following condition must always hold true: $V_{DD} \geqq V1 \geqq V2 \geqq V3 \geqq V4 \geqq V5$

■ELECTRICAL CHARACTERISTICS

●DC Characteristics

(V_{DD}=5.0V±10%, V_{SS}=0V, Ta=−20 to 75°C)

Parameter	Symbol	Conditions	Applicable Pin	Min	Typ	Max	Unit
"H" level input voltage (1)	V_{IH1}		DB0~DB7	2.0	—	V_{DD}	V
"L" level input voltage (1)	V_{IL1}		RS, R/W, E	V_{SS}	—	0.8	V
"H" level input voltage (2)	V_{IH2}		OSC1	$V_{DD}-1.0$	—	V_{DD}	V
"L" level input voltage (2)	V_{IL2}			V_{SS}	—	1.0	V
"H" level output voltage (1)	V_{OH1}	$I_{OH}=-0.205$mA	DB0~DB7	2.4	—	—	V
"L" level output voltage (1)	V_{OL1}	$I_{OL}=1.6$mA		—	—	0.4	V
"H" level output voltage (2)	V_{OH2}	$I_{OH}=-0.04$mA	XSCL LP DO	$0.9V_{DD}$	—	—	V
"L" level output voltage (2)	V_{OL2}	$I_{OL}=0.04$mA		—	—	$0.1V_{DD}$	V
Driver-on resistor (COM)	R_{COM}	$\lvert V_{COM}-V_n\rvert=0.5$V	COM1~16	—	2	10	kΩ
Driver-on resistor (SEG)	R_{SEG}	$\lvert V_{SEG}-V_n\rvert=0.5$V	SEG1~40	—	2.5	10	kΩ
I/O leakage current	I_{IL}	V_I=0 to V_{DD}		—	—	1	μA
Pull-up MOS current	$-I_P$	V_{DD}=5V		50	125	250	μA
Supply current	I_{op}	Rf oscillation, external clock V_{DD}=5V, $f_{osc}=f_{CP}$=270kHz	V_{DD}	—	0.5	0.8	mA
External clock operation							
External clock operating frequency	f_{EXTCL}			125	250	350	kHz
External clock duty	Duty			45	50	55	%
External clock rise time	tr_{EXTCL}			—	—	0.2	μs
External clock fall time	tf_{EXTCL}			—	—	0.2	μs
Internal clock operation (Rf oscillation)							
Internal clock oscillation frequency	f_{OSC}	R_f=91kΩ±2%		190	270	350	kHz
LCD driving voltage	V_{LCD}	$V_{DD}-V5$		3.0	—	V_{DD}	V

●AC Characteristics

○Read Cycle

(V_{DD}=5.0V±10%, V_{SS}=0V, Ta=−20 to 75°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Enable cycle time	t_{cycE}		500	—	—	ns
Enable "H" level pulse width	t_{WEH}		220	—	—	ns
Enable rise/fall time	t_{rE}, t_{fE}		—	—	25	ns
RS, R/W setup time	t_{AS}		40	—	—	ns
RS, R/W address hold time	t_{AH}		10	—	—	ns
Read data output delay	t_{RD}	C_L=100pF	—	—	120	ns
Read data hold time	t_{DHR}		20	—	—	ns

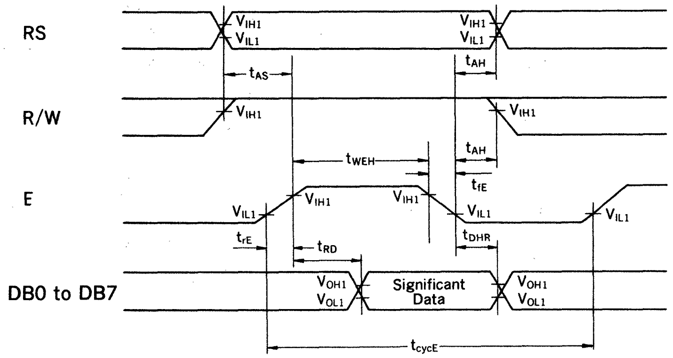
○Write Cycle

(V_{DD}=5.0V±10%, V_{SS}=0V, Ta=−20 to 75°C)

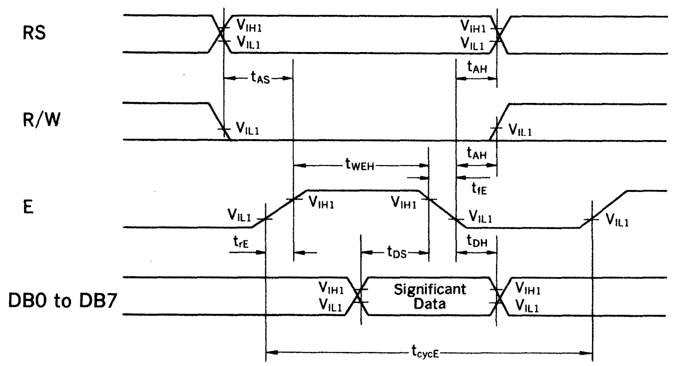
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Enable cycle time	t_{cycE}		500	—	—	ns
Enable "H" level pulse width	t_{WEH}		220	—	—	ns
Enable rise/fall time	t_{rE}, t_{fE}		—	—	25	ns
RS, R/W setup time	t_{AS}		40	—	—	ns
RS, R/W address hold time	t_{AH}		10	—	—	ns
Data setup time	t_{DS}		60	—	—	ns
Write data hold time	t_{DH}		10	—	—	ns

●Timing Chart

○Read Cycle



○Write Cycle



■DISPLAY COMMAND

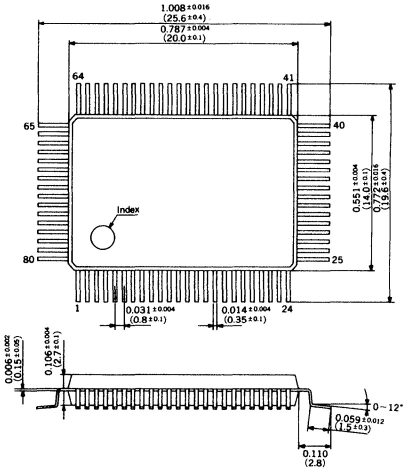
COMMAND	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Note
CLEAR DISPLAY	0	0	0	0	0	0	0	0	0	1	
CURSOR HOME	0	0	0	0	0	0	0	0	1	*	
ENTRY MODE SET	0	0	0	0	0	0	0	1	I/D	S	DB1=1 : Increment, DB1=0 : Decrement DB0=1 : The display is shifted. DB0=0 : The display is not shifted.
DISPLAY ON/OFF	0	0	0	0	0	0	1	D	C	B	DB2=1 : Display on DB2=0 : Display off DB1=1 : Cursor on DB1=0 : Cursor off DB0=1 : Brinking on DB0=0 : Brinking off
CURSOR/DISPLAY SHIFT	0	0	0	0	0	1	S/C	R/L	*	*	DB3=1 : Shifts display one character DB2=1 : Right shift, DB2=0 : Left shift
SYSTEM SET	0	0	0	0	1	DL	N	F	*	*	DB4=1 : 8 bits, DB4=0 : 4 bits DB3=1 : 2 lines display (1/16 duty), DB3=0 : 1 line display (DB2=1 : 5×10 dots, 1/11 duty DB2=0 : 5×7 dots, 1/8 duty)
SET CGRAM ADDRESS	0	0	0	1	ACG						The address length that can be set is 64 addresses.
SET DDRAM ADDRESS	0	0	1	ADD							The address length that can be set is 80 addresses.
READ BUSY FLUG/ ADDRESS COUNTER	0	1	BF	AC							DB7=1 : Busy (instruction not accepted) DB7=0 : Ready (instruction accepted)
WRITE DATA	1	0	Write Data								
READ DATA	1	1	Read Data								

*Don't care

PACKAGE DIMENSIONS

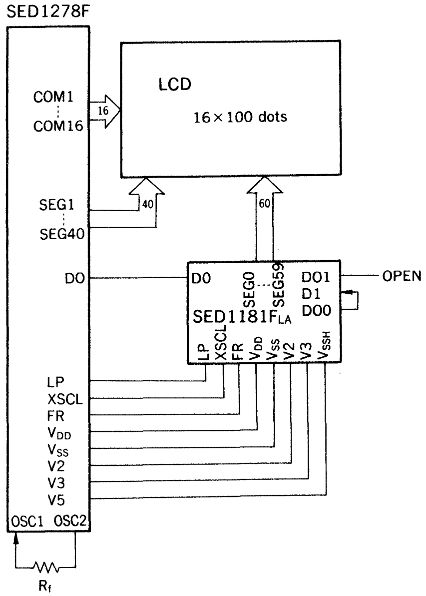
F80-5

80-pin QFP



unit : inch
(mm)

EXAMPLE OF APPLICATION (2 lines × 20 characters)



SED1278F is usually connected to 8-bit MPU via I/O ports.

■CHARACTER CODE MAP (SED1278F$_{0A}$)

	Higher 4bit (D4 to D7) of Character Code (Hexadecimal)															
Lower 4bit (D0 to D3) of Character Code (Hexadecimal)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	CG RAM (1)			0	@	P	`	p				ー	タ	ミ	α	p
1	CG RAM (2)		!	1	A	Q	a	q			。	ア	チ	ム	ä	q
2	CG RAM (3)		"	2	B	R	b	r			「	イ	ツ	メ	β	θ
3	CG RAM (4)		#	3	C	S	c	s			」	ウ	テ	モ	ε	∞
4	CG RAM (5)		$	4	D	T	d	t			、	エ	ト	ヤ	μ	Ω
5	CG RAM (6)		%	5	E	U	e	u			・	オ	ナ	ユ	σ	ü
6	CG RAM (7)		&	6	F	V	f	v			ヲ	カ	ニ	ヨ	ρ	Σ
7	CG RAM (8)		'	7	G	W	g	w			ァ	キ	ヌ	ラ	g	π
8	CG RAM (1)		(	8	H	X	h	x			ィ	ク	ネ	リ	√	x̄
9	CG RAM (2)		)	9	I	Y	i	y			ゥ	ケ	ノ	ル	⁻¹	y
A	CG RAM (3)		*	:	J	Z	j	z			ェ	コ	ハ	レ	j	千
B	CG RAM (4)		+	;	K	[	k	{			ォ	サ	ヒ	ロ	ˣ	万
C	CG RAM (5)		,	<	L	¥	l	|			ャ	シ	フ	ワ	¢	円
D	CG RAM (6)		-	=	M	]	m	}			ュ	ス	ヘ	ン	£	÷
E	CG RAM (7)		.	>	N	^	n	→			ョ	セ	ホ	゛	ñ	
F	CG RAM (8)		/	?	O	_	o	←			ッ	ソ	マ	゜	ö	█

*Character codes (00H-0FH) of SED1278F are assigned to the area of character generator RAM (CG RAM).
The CG ROM of the SED1278F is masked; if you wish to have your own CG ROM, consult Seiko Epson Marketing Department for conversion of the masked ROM.

SED1500F Series

CMOS DOT MATRIX LCD DRIVER

- **Duty 1/7—1/16 LCD Driver**
- **Single Chip LCD Driver (with Built in Display Data RAM)**

■DESCRIPTION

The SED1500F Series is a dot matrix LCD driver CMOS LSI with the ability of alpha numeric and graphic display. Because of a built-in display data RAM, the necessary operation for drive is only writing of display data. Moreover, this LSI can be connected directly to the bus line of a 4 bits/8 bits microcomputer. Therefore the combinations of CMOS microcomputer and the SED1500F Series make it easier to systematize the handy instruments requiring low power dissipation.

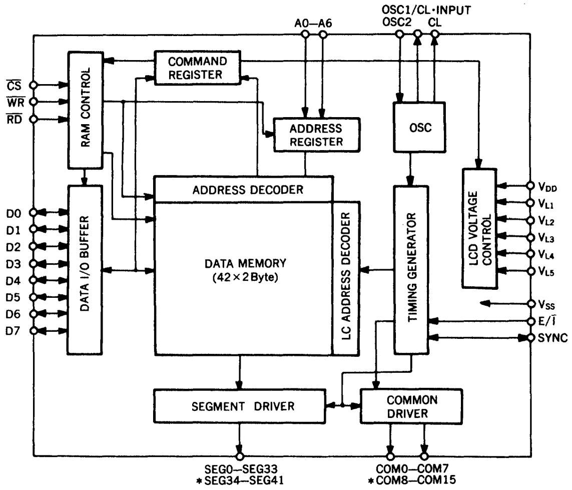
■FEATURES

- Built-in display data RAM
- Built-in driver for LCD segment and LCD common

  Dot drive capability: Common-single system 336 to 544 dots (per chip)

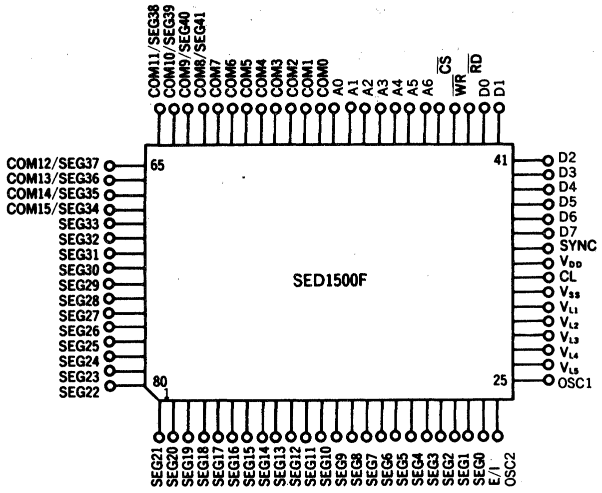
  Common-multi system 336 to 672 dots (per chip)
- Direct connection capability to the bus line of a 4 bits/8 bits microcomputer.
- Duty 1/7—1/16 setting capability (mask option)
- Built-in CR oscillation circuit (without resistor)
- Low power dissipation
- Package··80-pin QFP (plastic)

■BLOCK DIAGRAM



*Those terminals can be used as either SEG or COM terminals.

PIN CONFIGURATION



*Terminal (Pin No. 61—No. 68) can be used as either SEG or COM terminal.

PIN DESCRIPTION

A0 to A6	RAM Address
D0 to D7	Data Input/Output
$\overline{RD}$	Read Enable
$\overline{WR}$	Write Enable
OSC1, OSC2	Oscillation Circuit
$\overline{CS}$	Chip Select Input
CL	Clock Output
E/$\overline{I}$	Master/Slave Selection
SYNC	Slave Synchronous Input/Output
COM0 to COM15	LCD Common (Y) Drive Output
SEG0 to SEG41	LCD Segment (X) Drive Output
V_{L1} to V_{L5}	LCD Drive Power Supply
V_{DD}	Power Supply (+)
V_{SS}	Logic Power Supply (−)

ABSOLUTE MAXIMUM RATINGS

($V_{DD}=0V$)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{SS}	−7.0 to 0.3	V
	V_{L1} to V_{L5}	−13.0 to 0.3	V
Input voltage	V_I	$V_{SS}-0.3$ to $V_{DD}+0.3$	V
Operating temperature	T_{opr}	−20 to 75	℃
Storage temperature	T_{stg}	−65 to 150	℃
Soldering temperature and time	T_{sol}	260℃, 10s (at lead)	—

ELECTRICAL CHARACTERISTICS

●DC Characteristics

($V_{DD}=0V$)

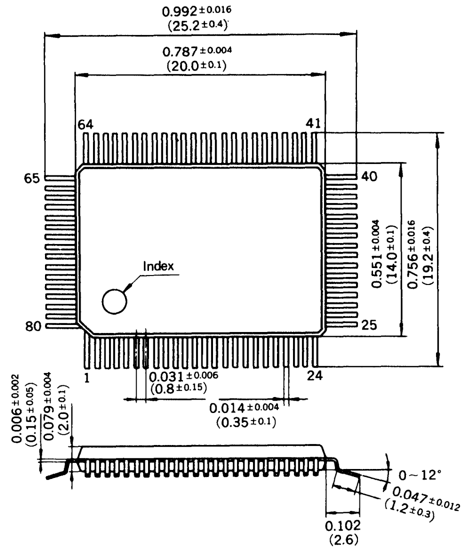
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{SS}		−4.5	*1	−5.5	V
Supply voltage	V_{L5}		−3.5	—	−10	V
Operating dissipation	I_{OP1}	$V_{SS}=-5.5V$ $\overline{CS}=H$ $V_{L5}=-10.0V$ $Rf=1.0M\Omega$	—	60	100	μA
Oscillation start voltage	V_{STA}	$Rf=1.0M\Omega$	—	—	−2.0	V
Oscillation stop voltage	V_{STP}	$Rf=1.0M\Omega$	—	—	−2.0	V
Read cycle time	$t_{c(RD)}$	$V_{SS}=-5V$ $V_{IH}=V_{OH}=-2.0V$ $V_{IL}=V_{OL}=V_{SS}+0.8V$ $C_L=100pF+1TTL$	1,000	—	—	ns
Write cycle time	$t_{c(WR)}$		1,000	—	—	ns
Access time	t_a		—	—	800	ns

*1 In the case of operating voltage V_{SS} at $V_{DD}-3.0V$, inquire of IC SALES DEPT.

■PACKAGE DIMENSIONS

F80

80-pin QFP



unit : inch
(mm)

■SED1500F SERIES

The capacity of the SED1500F Series is varid as follows with a duty of LCD multiplex drive.

● Common-single series

*1

Duty	Type	No. of COM output	No. of SEG output
1/7	SED1507F	7	42
1/8	SED1500F	8	42
1/10	SED1501F	10	40
1/11		11	39
1/12		12	38
1/13		13	37
1/14		14	36
1/15		15	35
1/16	SED1502F	16	34

● Common-multi series

Duty	Type	No. of COM output	No. of SEG output
1/8		4	42
1/9		5	42
1/10		5	42
1/11		6	42
1/12		6	42
1/13		7	42
1/14		7	42
1/15		8	42
1/16	SED1503F	8	42

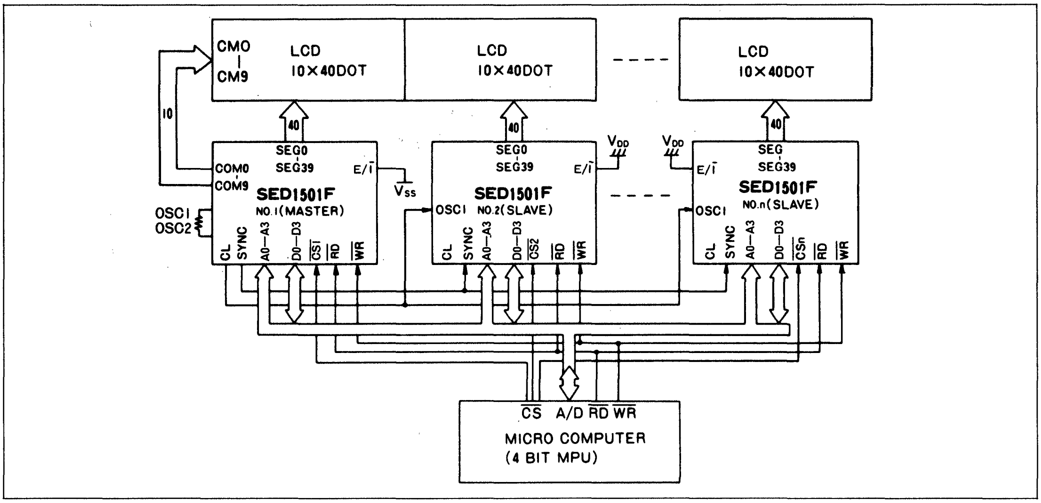
*1 The driver is open-ended by the cascade connection.

*2 Above-mentioned Duties are all realized by the mask option. Listed types are already available. As to other ones, please inquire of our IC Sales Dept.

■EXAMPLE OF APPLICATIONS (Connection among the SED1500F Series, LCD and MPU)

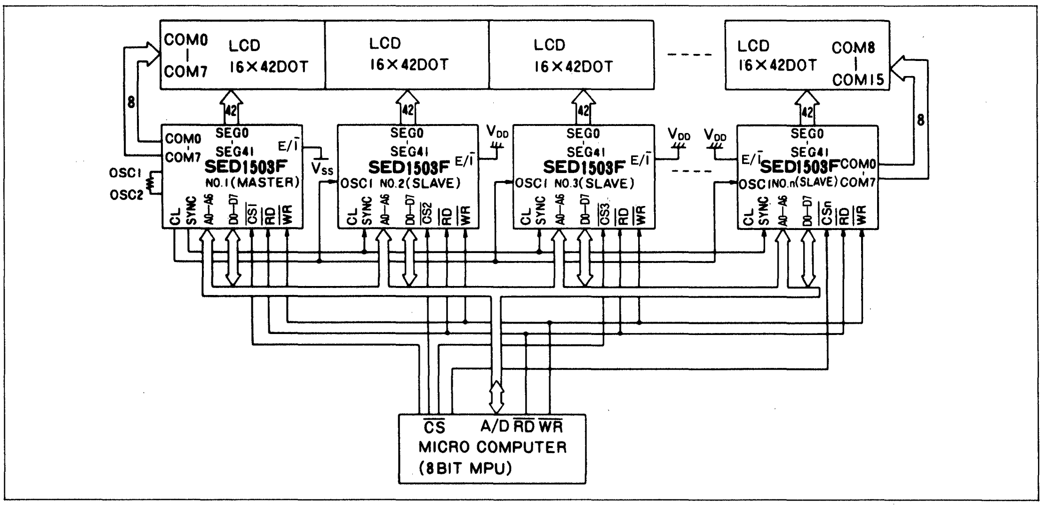
●An example of multichip composition by the common-single series.

Number of display dots=10×40×n n=1−10 (in the case of SED1501F)



●An example of multichip composition by the common-multi series.

Number of display dots=16×42×n n=2−10 (in the case of SED1503F)



SED2020F$_{0A}$/SED2020F$_{0B}$

CMOS VFD DRIVER

- ●High-voltage CMOS Driver (70V: 10mA/bit)
- ●Transfer Clock (4MHz Max)
- ●Shift Registers and Latch Circuits are Built-in

■DESCRIPTION

The SED2020F$_{OA}$ is a 20 bits (10 bits × 2) driver for vacuum fluorescent displays (VFD). The SED2020F$_{OA}$ is designed to drive both the anode and grid of the VFD. A cascade connection of multiple SED2020F$_{OA}$s allows to expand characters and segments.

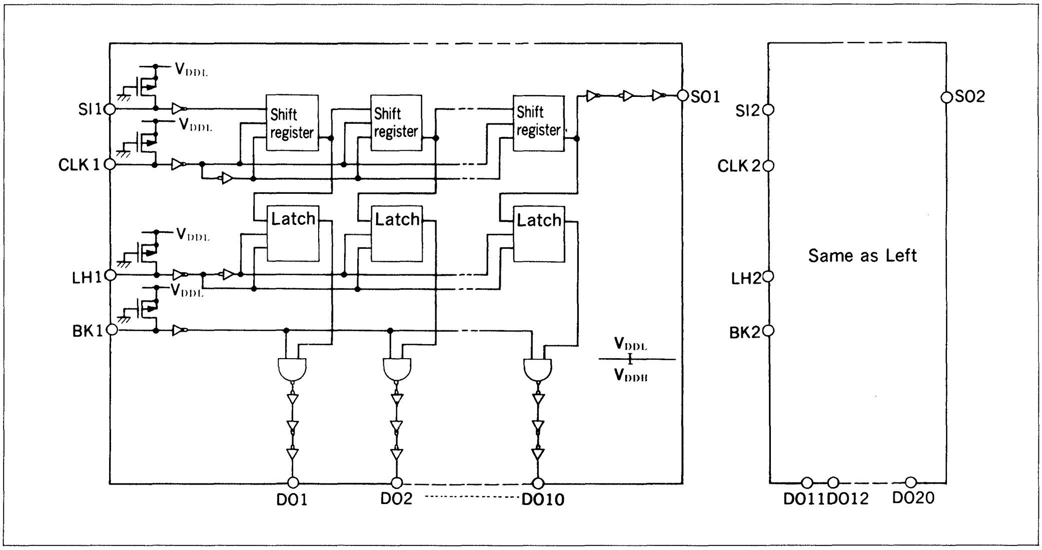
High voltage (70V Max) CMOS designed output circuit eliminates the external pull-down resistors to the output. The fast rise/fall time (1μs Max) enables a clear display which is free from afterglow.

The input circuit has a CMOS structure (logic level: 1.55V) with pull-up resistors, and can be directly driven by a standard logic IC such as TTL, LSTTL, CMOS, or HSCMOS.

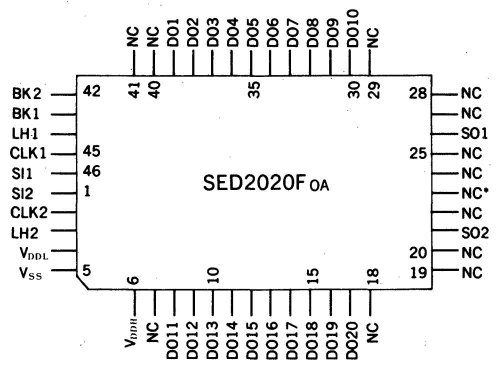
■FEATURES

- ●High-voltage CMOS driver (70V: 10mA/bit)
- ●Anode/Grid driver for VFD
- ●On-chip serial input 10 bits shift register × 2 (20 bits in total)
- ●Transfer clock ··················4MHz
- ●Logic supply voltage ·········V_{DDL} = 5V±10%
- ●Package···························46-pin QFP (plastic)/44-pin QFP (plastic)

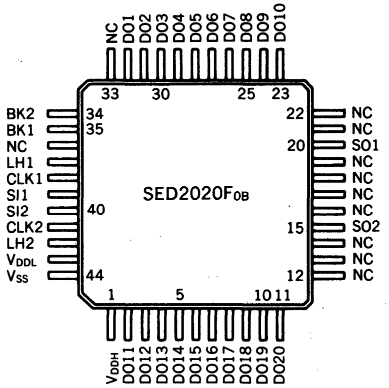
■BLOCK DIAGRAM



PIN CONFIGURATION



NC : NO Connection
NC* : MUST BE OPEN



NC : NO Connection

PIN DESCRIPTION

Symbol	Pin Name	Function
CLK1	Clock input	Data is read from SI during "L" of CLK; data shifts to SO at rising edge of CLK.
CLK2		
SI1	Data input	Serial data input to shift registers
SI2		
SO1	Data output	Serial data output from shift registers
SO2		
LH1	Latch clock input	Data of shift register are read during "H" of LH; data of shift register are latched at falling edge of the signal.
LH2		
BK1	Blanking	Entire display can be turned off during "H".
BK2		
DO	Driver output	High-voltage CMOS output
V_{SS}	Power supply	GND (0V)
V_{DDL}	Power supply	Supply for logic (5V)
V_{DDH}	Power supply	Supply for driver (70V)

ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V, Ta=−10 to 70°C)

Parameter	Symbol	Ratings	Unit
Supply voltage (driver)	V_{DDH}	−0.3 to 70	V
Supply voltage (logic)	V_{DDL}	−0.3 to 7	V
Driver output voltage	V_{DO}	$V_{SS}-0.3$ to $V_{DDH}+0.3$	V
Input/output voltage	$V_{I/O}$	$V_{SS}-0.3$ to $V_{DDL}+0.3$	V
Driver high level output current	I_{OHDO}	−15 to 0	mA
Driver low level output current	I_{OLDO}	0 to 3	mA
Power dissipation	P_D	0 to 250	mW
Operating temperature	T_{opr}	−10 to 70	℃
Storage temperature	T_{stg}	−65 to 150	℃
Soldering temperature and time	T_{sol}	260℃, 10s (at lead)	—

■RECOMMENDED OPERATING CONDITIONS

($V_{SS}=0V$)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage (driver)	V_{DDH}		30	60	70	V
Supply voltage (logic)	V_{DDL}		4.5	5.0	5.5	V
Input voltage	V_I		0	—	V_{DDL}	V
Input logic level	V_{LL}	TTL input level	—	1.55	—	V
Driver High level output current	I_{OHDO}	Grid output	—	−10	—	mA
		Anode output	—	−0.5	—	mA
Clock frequency	f_{clock}	Cascade connection	0	—	4	MHz
Clock pulse width	t_{wclock}		125	—	—	ns
Setup time	t_{setup}		125	—	—	ns
Hold time	t_{hold}		0	—	—	ns
Latch pulse width	t_{wlatch}		250	—	—	ns

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

($V_{DDL}=5V$, $V_{DDH}=60V$, $V_{SS}=0V$, $Ta=25°C$)

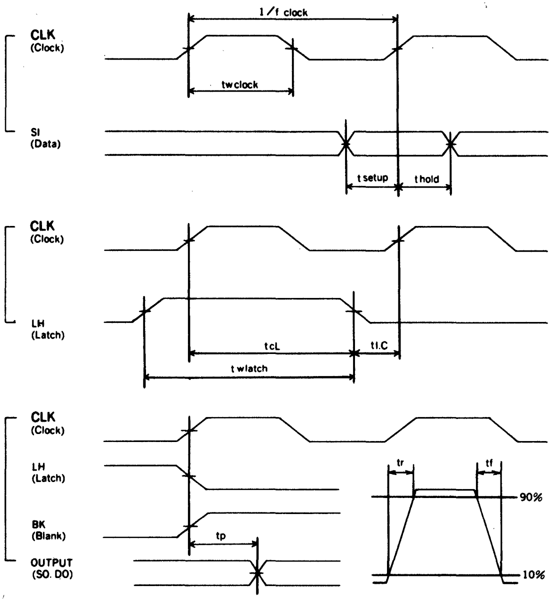
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High level input voltage	V_{IH}		2.4	—	V_{DDL}	V
Low level input voltage	V_{IL}		0	—	0.7	V
High level input current	I_{IH}	$V_{IH}=5.3V$	—	33	100	μA
Low level input current	I_{IL}	$V_{IL}=0V$	−160	−100	—	μA
High level output current	I_{OH}(SO)	$V_{OH}=4.6V$	—	−1.4	−0.44	mA
Low level output current	I_{OL}(SO)	$V_{OL}=0.4V$	1.6	2.1	—	mA
Supply current (V_{DDL})	I_{DDL}	f clock=4MHz	—	—	5	mA
Supply current (V_{DDH})	I_{DDH}	At all drivers output "H"	—	—	2.0	mA
Driver high level output current	I_{OHDO}	$V_{OHDO}=55V$ at output "H"	—	—	−10	mA
Driver low level output current	I_{OLDO}	$V_{OLDO}=5V$ at output "L"	1	—	—	mA

●AC Electrical Characteristics

($V_{DDL}=5V$, $V_{DDH}=60V$, $V_{SS}=0V$, $Ta=25°C$)

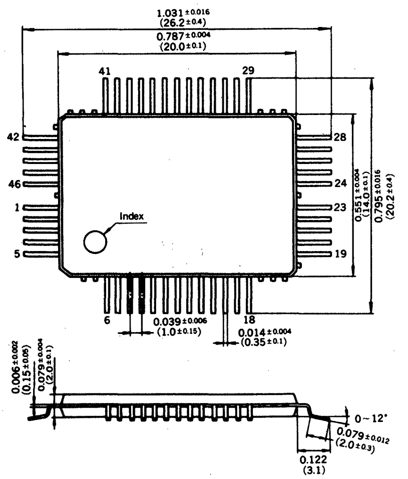
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Clock-latch delay time	t_{CL}	1 . Input signal conditions (1) Amplitude: 0—5V (2) Rise/fall time should be 15ns or less. (3) Measuring voltage should be 2.5V. 2 . Output signal conditions (1) Standard loads are: 13pF, 10MΩ (2) Measuring voltage should be 2.5V or 1/2 of the amplitude.	125	—	—	ns
Latch-clock delay time	t_{LC}		0	—	—	ns
Output(SO) rise time	tr (SO)		—	—	50	ns
Output(SO) fall time	tf (SO)		—	—	50	ns
Clock(SO) delay time	tp (SO)		—	—	125	ns
Output(DO) rise time	tr (DO)		—	—	1	μs
Output(DO) fall time	tf (DO)		—	—	1	μs
BK-DO transfer time	tp (DO)		—	—	2	μs

●Timing Chart



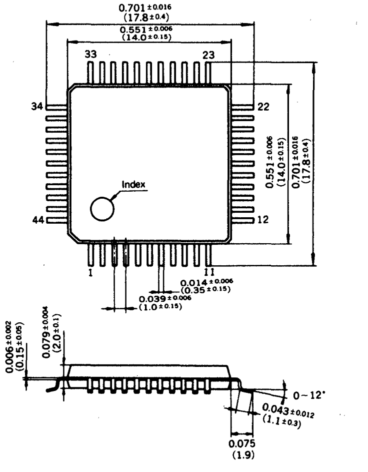
■PACKAGE DIMENSIONS

F46 46-pin QFP



unit : inch
(mm)

F44-2 44-pin QFP

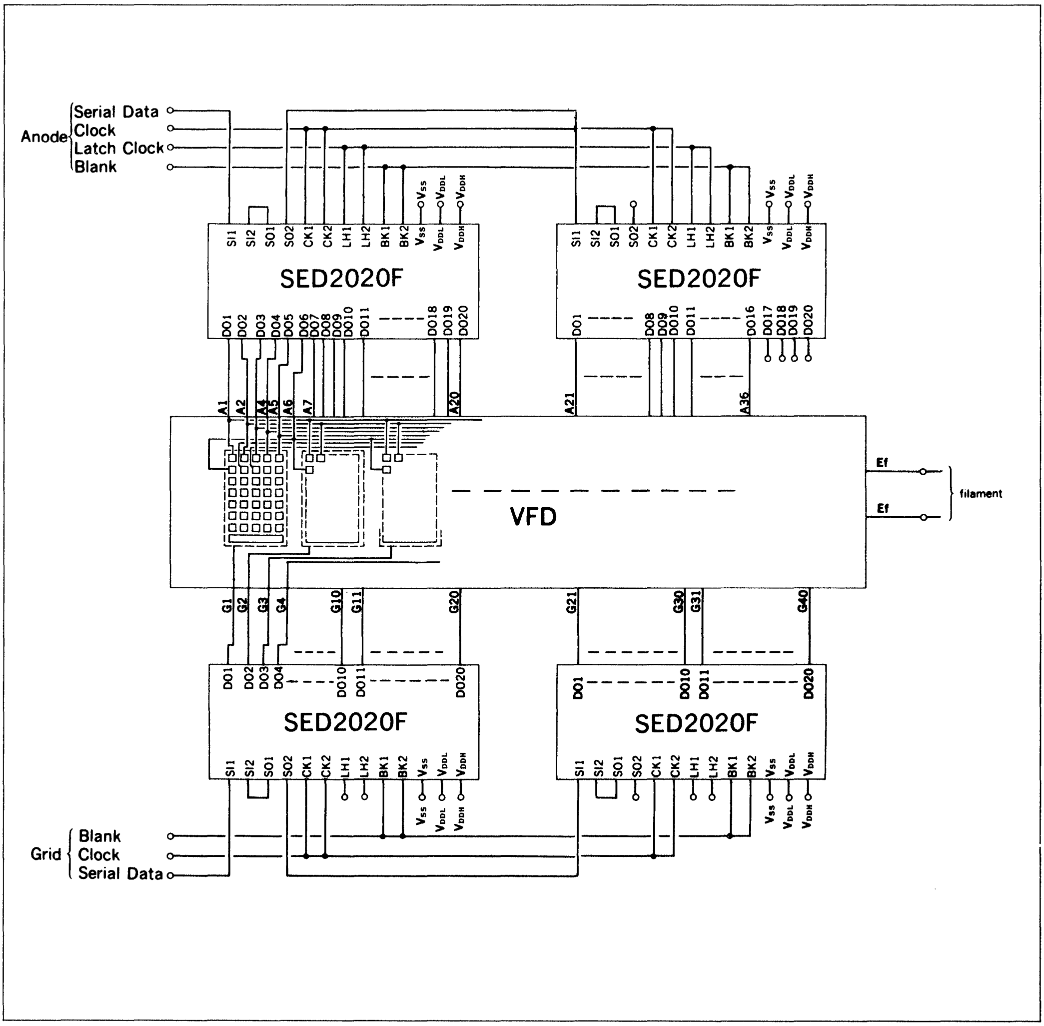


unit : inch
(mm)

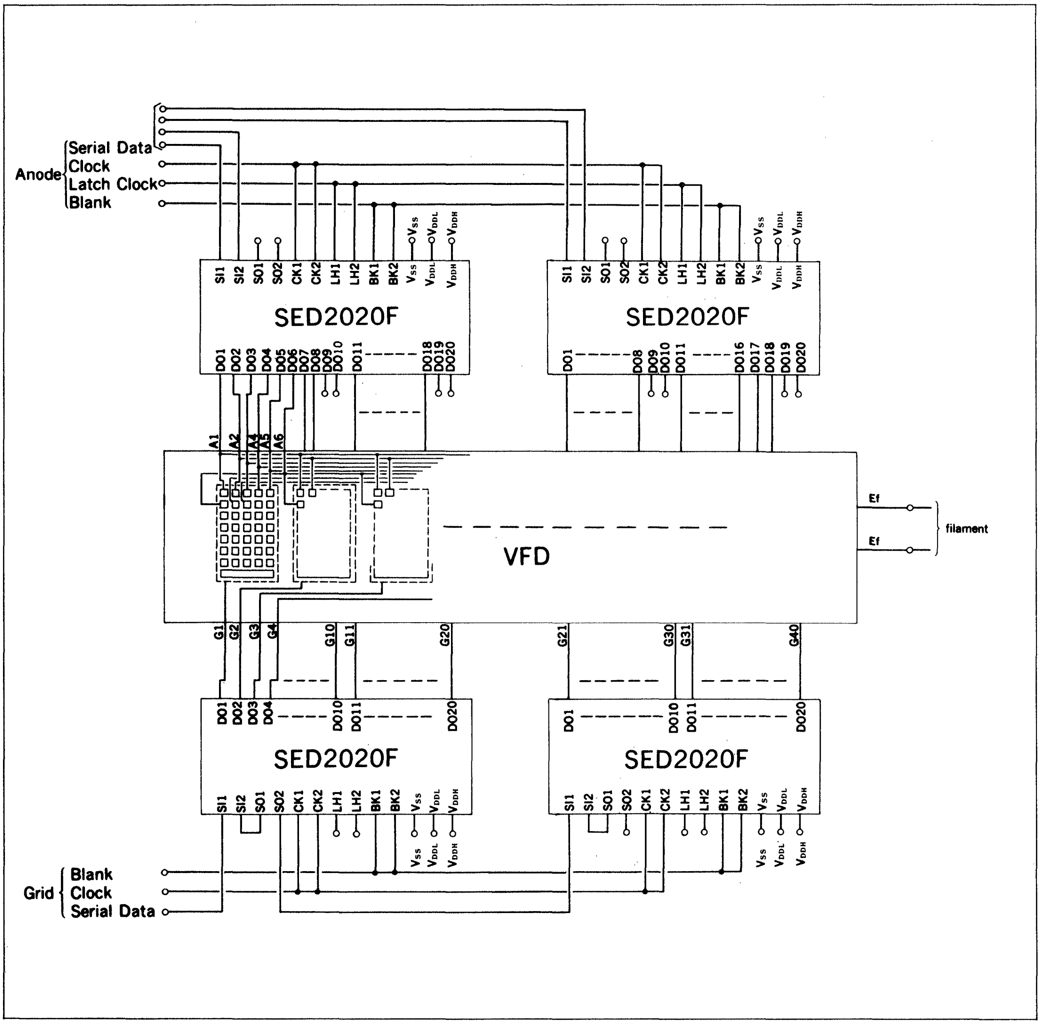
■TYPICAL CONNECTIONS

●Example of connecting SED2020F's to VFD (1)

⟨1 bit serial⟩



●Example of connecting
SED2020F's to VFD (2)
⟨4bits serial⟩



SED2032F$_{0B}$

CMOS VFD DRIVER

- **High-voltage CMOS Driver (70V: 10mA/bit)**
- **Transfer Clock (4MHz Max)**
- **Shift Registers and Latch Circuits are Built-in**

■DESCRIPTION

The SED2032F$_{0B}$ is a 32 bits (16 bits × 2) driver for vacuum fluorescent displays (VFD). The SED2032F$_{0B}$ is designed to drive both the anode and grid of the VFD. A cascade connection of multiple SED2032F$_{0B}$ allows to expand characters and segments.

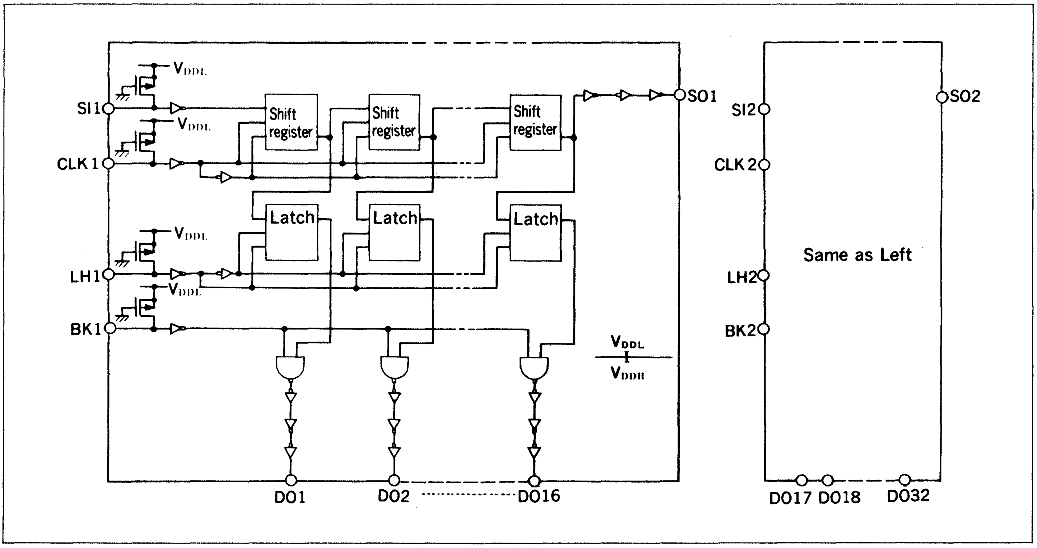
High voltage (70V Max) CMOS designed output circuit eliminates the external pull-down resistors to the output. The fast rise/fall time (1μs Max) enables a clear display which is free from afterglow.

The input circuit has a CMOS structure (logic level: 1.55V) with pull-up resistors, and can be directly driven by a standard logic IC such as TTL, LSTTL, CMOS, or HSCMOS.

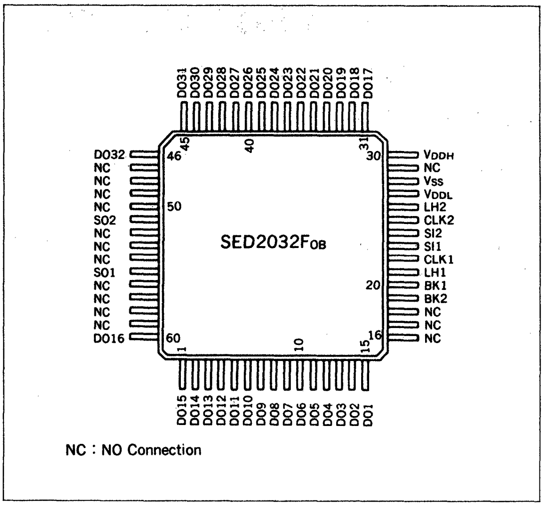
■FEATURES

- High-voltage CMOS driver (70V: 10mA/bit)
- Anode/Grid driver for VFD
- On-chip serial input 16 bits shift register × 2 (32 bits in total)
- Transfer clock ··················4MHz
- Logic supply voltage ·········V_{DDL} = 5V±10%
- Package·························60-pin QFP (plastic)

■BLOCK DIAGRAM



PIN CONFIGURATION



NC : NO Connection

PIN DESCRIPTION

Pin No.	Symbol	Pin Name	Functions
22	CLK1	Clock input	Data is read from SI during "L" of CLK; data shifts to SO at rising edge of CLK.
25	CLK2		
23	SI1	Data input	Serial data input to shift registers
24	SI2		
51	SO1	Data output	Serial data output from shift registers
55	SO2		
21	LH1	Latch clock input	Data of shift register are read during "H" of LH; data of shift register are latched at falling edge of the signal.
26	LH2		
20	BK1	Blanking	Entire display can be turned off during "H"
19	BK2		
15 to 1, 60 31 to 46	DO	Driver output	High-voltage CMOS output
28	V_{SS}	Power supply	GND (0V)
27	V_{DDL}	Power supply	Supply for logic (5V)
30	V_{DDH}	Power supply	Supply for driver (70V)

ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V, Ta=−10 to 70°C)

Parameter	Symbol	Ratings	Unit
Supply voltage (driver)	V_{DDH}	−0.3 to 70	V
Supply voltage (logic)	V_{DDL}	−0.3 to 7	V
Driver output voltage	V_{DO}	$V_{SS}-0.3$ to $V_{DDH}+0.3$	V
Input/output voltage	$V_{I/O}$	$V_{SS}-0.3$ to $V_{DDL}+0.3$	V
Driver high level output current	I_{OHDO}	−15 to 0	mA
Driver low level output current	I_{OLDO}	0 to 3	mA
Power dissipation	P_D	0 to 250	mW
Operating temperature	T_{opr}	−10 to 70	°C
Storage temperature	T_{stg}	−65 to 150	°C
Soldering temperature and time	T_{sol}	260°C, 10s (at lead)	—

RECOMMENDED OPERATING CONDITIONS

(V_{SS}=0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage (driver)	V_{DDH}		30	60	70	V
Supply voltage (logic)	V_{DDL}		4.5	5.0	5.5	V
Input voltage	V_I		0	—	V_{DDL}	V
Input logic level	V_{LL}	TTL input level	—	1.55	—	V
Driver High level output current	I_{OHDO}	Grid output	—	−10	—	mA
		Anode output	—	−0.5	—	mA
Clock frequency	fclock	Cascade connection	0	—	4	MHz
Clock pulse width	twclock		125	—	—	ns
Setup time	tsetup		125	—	—	ns
Hold time	thold		0	—	—	ns
Latch pulse width	twlatch		250	—	—	ns

ELECTRICAL CHARACTERISTICS

DC Electrical Characteristics

($V_{DDL}=5V$, $V_{SS}=0V$, $V_{DDH}=60V$, Ta=25°C)

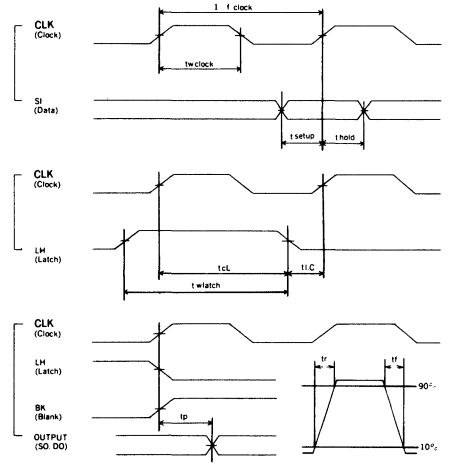
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High level input voltage	V_{IH}		2.4	—	V_{DDL}	V
Low level input voltage	V_{IL}		0	—	0.7	V
High level input current	I_{IH}	$V_{IH}=5.3V$	—	33	100	μA
Low level input current	I_{IL}	$V_{IL}=0V$	−160	−100	—	μA
High level output current	I_{OH}(SO)	$V_{OH}=4.6V$	—	−1.4	−0.44	mA
Low level output current	I_{OL}(SO)	$V_{OL}=0.4V$	1.6	2.1	—	mA
Supply current (V_{DDL})	I_{DDL}	f clock=4MHz	—	—	5	mA
Supply current (V_{DDH})	I_{DDH}	At all drivers output "H"	—	—	3	mA
Driver high level output current	I_{OHDO}	$V_{OHDO}=55V$ at output "H"	—	—	−10	mA
Driver low level output current	I_{OLDO}	$V_{OLDO}=5V$ at output "L"	1	—	—	mA

AC Electrical Characteristics

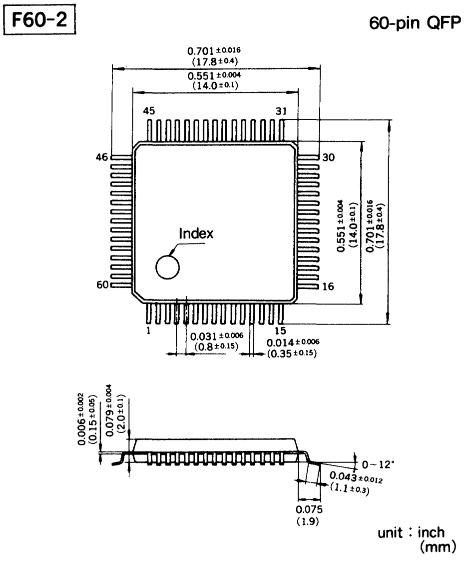
($V_{DDL}=5V$, $V_{SS}=0V$, $V_{DDH}=60V$, Ta=25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Clock-latch delay time	t_{CL}	1. Input signal conditions (1) Amplitude: 0—5V (2) Rise/fall time should be 15ns or less. (3) Measuring voltage should be 2.5V. 2. Output signal conditions (1) Standard loads are: 13pF, 10MΩ (2) Measuring voltage should be 2.5V or 1/2 of the amplitude.	125	—	—	ns
Latch-clock delay time	t_{LC}		0	—	—	ns
Output(SO) rise time	tr (SO)		—	—	50	ns
Output(SO) fall time	tf (SO)		—	—	50	ns
Clock(SO) delay time	tp (SO)		—	—	125	ns
Output(DO) rise time	tr (DO)		—	—	1	μs
Output(DO) fall time	tf (DO)		—	—	1	μs
BK-DO transfer time	tp (DO)		—	—	2	μs

Timing Chart

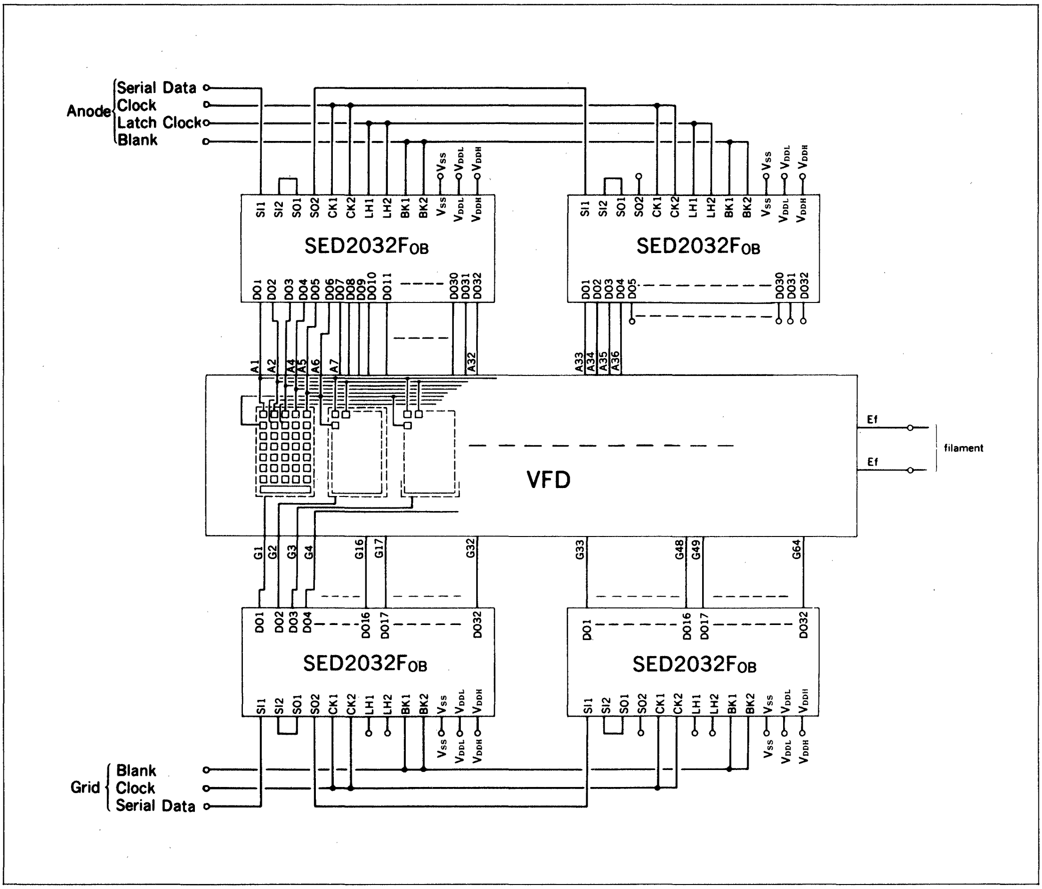


PACKAGE DIMENSIONS



■TYPICAL CONNECTIONS

●Example of connecting
SED2032F's to VFD
⟨1 bit serial⟩



The SED2032F can be efficiently used as dot matrix LCD driver.

SED5031C$_{OC}$

CMOS 12 BIT THERMAL HEAD DRIVER

●Built in 12bit static shift register

●12bit latch circuits

●Output control circuits and built in 12bit driver

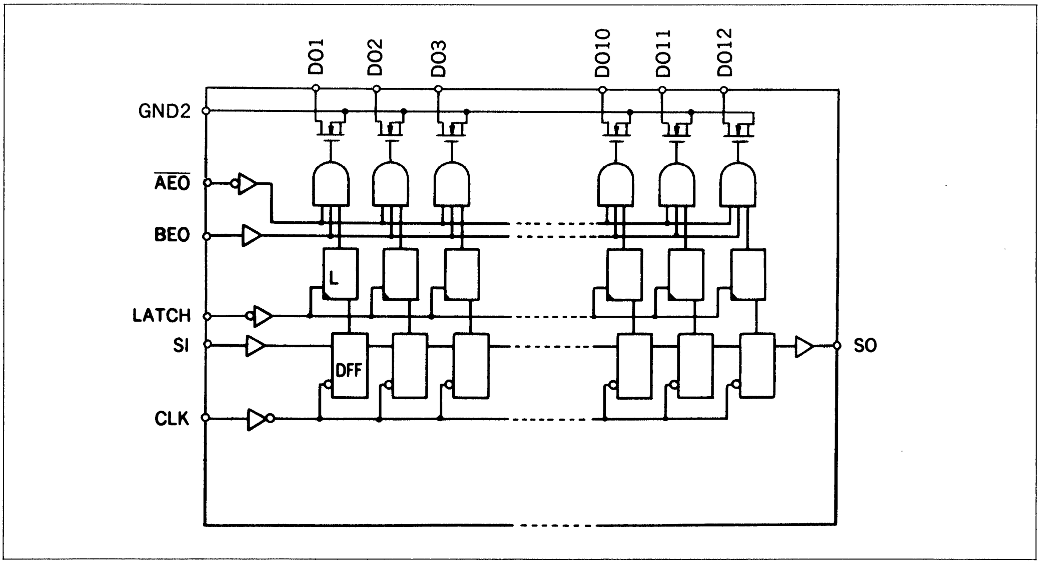
■DESCRIPTION

The SED5031C$_{OC}$ is a low power CMOS 12bit thermal head driver. It contains a 12bit high speed shift register, 12bit latch, output control circuit and 12bit driver with a drive capability of 28V/150mA allowing direct connection with thermal heads.

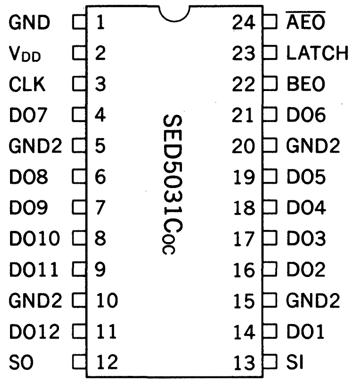
■FEATURES

- Built in 12bit static shift register
- Built in 12bit latch
- Built in output control circuit and 12bit driver
- High supply voltage for driver ···················28V (Max)
- High output current ································150mA (Max)
- Low supply current ································0.3mA/2MHz (Typ)
- High speed operation ·····························7MHz (Max)
- Si gate CMOS process
- Package···24-pin DIP (plastic)

■BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

Pin No.	Pin Name	Function
CLK	3	Clock input for static shift register.
SI	13	Serial data input to shift register.
SO	12	Serial data output from shift register.
LATCH	23	Latch signal input. Data in the shift register is latched when this signal goes low.
$\overline{AEO}$	24	Output enable A. Latched data is enabled for output to the driver when this signal is low. DO terminals are in the high impedance state when this signal is high.
BEO	22	Output enable B. Latched data is enabled for output when this signal is high. DO terminals are in the high impedance state when this signal is low.
DO_n	14, 16~19, 21 4, 6~9, 11	Parallel data output terminals. (Open drain NMOS transistor output)
V_{DD}	2	Power supply (+5V)
GND	1	Signal ground for input: 0V
GND2	5, 10, 15, 20	Ground for driver output terminals: 0V

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.5 to 7.0	V
Voltage supplied to driver	B_{VDO}	28	V
Driver output current	I_{OLDO}	150	mA
Input voltage	V_I	−0.5 to V_{DD}+0.5	V
Input current	I_I	−20 to 20	mA
Output voltage	V_O	−0.5 to V_{DD}+0.5	V
Power dissipation	P_D	0.65 (Ta=80℃)	W
Operating temperature	T_{opr}	−10 to 80	℃
Storage temperature	T_{stg}	−65 to 150	℃
Soldering temperature and time	T_{sol}	260℃, 10s (at lead)	—

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
Input voltage	V_I		0	—	V_{DD}	V
Output high voltage DO_n	V_{OHDO}		0	12	24	V
Driver output current	I_{OLDO}		—	120	150	mA
Clock frequency	f_{CLK1}		—	2	7	MHz
	f_{CLK2}*	*for cascade connection	—	2	5	MHz
Clock pulse width	t_{WCLK}		70	—	—	ns
Setup time SI-CLK	t_{setup}		50	—	—	ns
Setup time CLK-LATCH	t_{CL}		100	—	—	ns
Hold time SI-CLK	t_{hold}		10	—	—	ns
Latch pulse width	t_{WLATCH}		50	—	—	ns

■ ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

(V_{DD}=5V, Ta=25°C)

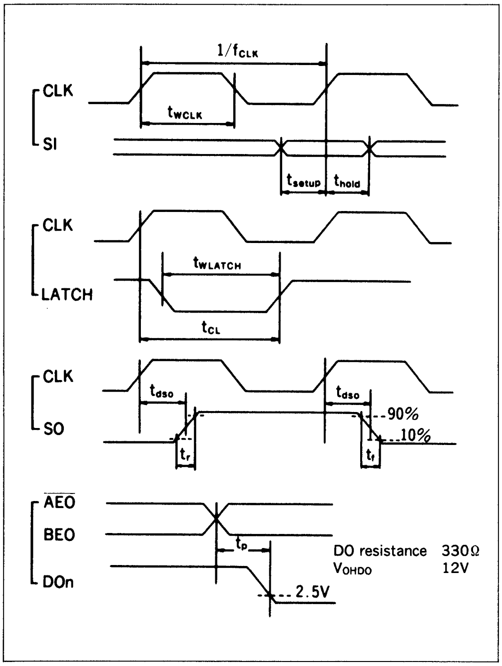
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input high voltage	V_{IH}		3.5	—	5.0	V
Input low voltage	V_{IL}		0	—	1.5	V
Input high current	I_{IH}	$V_{IH}=5.3V$	—	—	0.5	μA
Input low current	I_{IL}	$V_{IL}=-0.3V$	—	—	0.5	μA
Output high voltage (SO)	V_{OHSO}	$V_{DD}=4.5V$	4.45	—	—	V
Output low voltage (SO)	V_{OLSO}	$V_{DD}=4.5V$	—	—	0.05	V
Output high current (SO)	I_{OHSO}	$V_{OH}=4.2V$	0.5	2.5	—	mA
Output low current (SO)	I_{OLSO}	$V_{OL}=0.4V$	0.5	1.5	—	mA
Driver output voltage (DO_n)	V_{OLDO}	$I_{OLDO}=120mA$	—	0.7	1.0	V
Driver output current (DO_n)	I_{OLDO}	$V_{OLDO}=1.0V$	120	160	—	mA
V_{DD} supply current	I_{DD}	$V_{DD}=5.5V$, $f_{CLK}=5MHz$	—	1.5	5	mA
Output leakage	I_{LO}	$V_{DD}=4.5V$, $V_{OH}=24V$	—	—	50	μA

●AC Electrical Characteristics

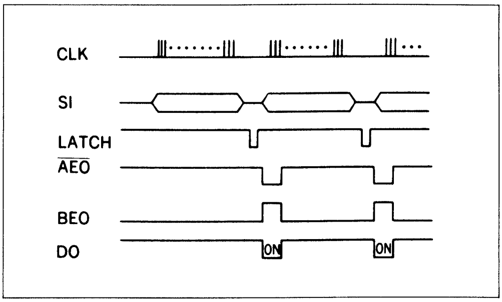
(V_{DD}=5V, Ta=80°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output rise time	t_r	$C_L=13pF$	—	20	35	ns
Output fall time	t_f		—	20	35	ns
Output (SO) delay time	t_{dso}		—	70	120	ns
Low level propagation time	t_p		—	0.2	1	μs

●Timing Chart

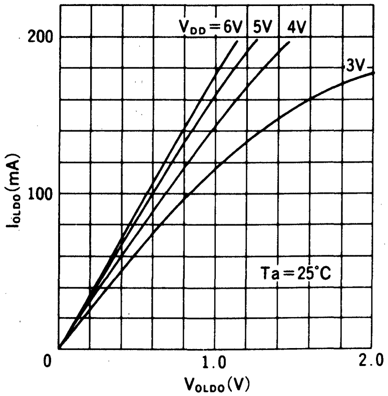


●Signal Sequence

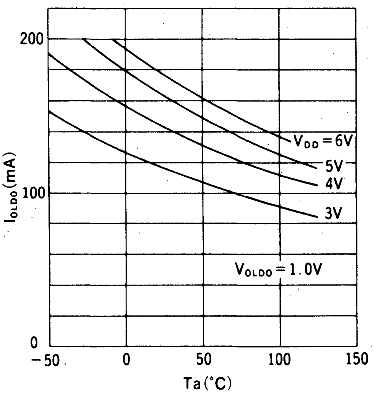


■PERFORMANCE CURVES

Driver output current (IOLDO)—Driver output voltage (VOLDO)



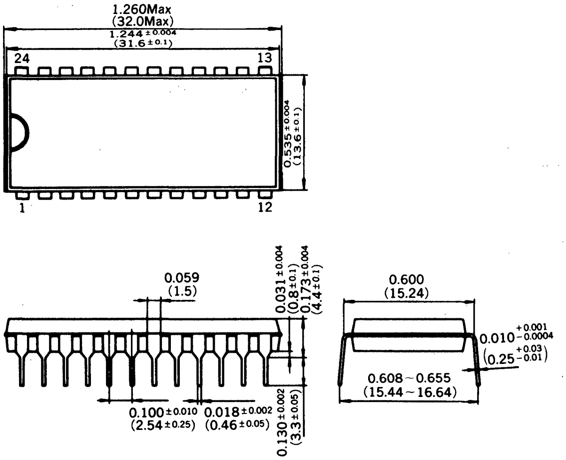
Driver output current (IOLDO)—Ambient temperature (Ta)



■ PACKAGE DIMEMSIONS

C24

24-pin DIP



unit : inch
(mm)

SED1330F

CMOS GRAPHIC LCD CONTROLLER

- **For Large-scale LCD**
- **Few External Circuits**
- **Virtual Screen Display RAM**
- **Enhanced Control Function**

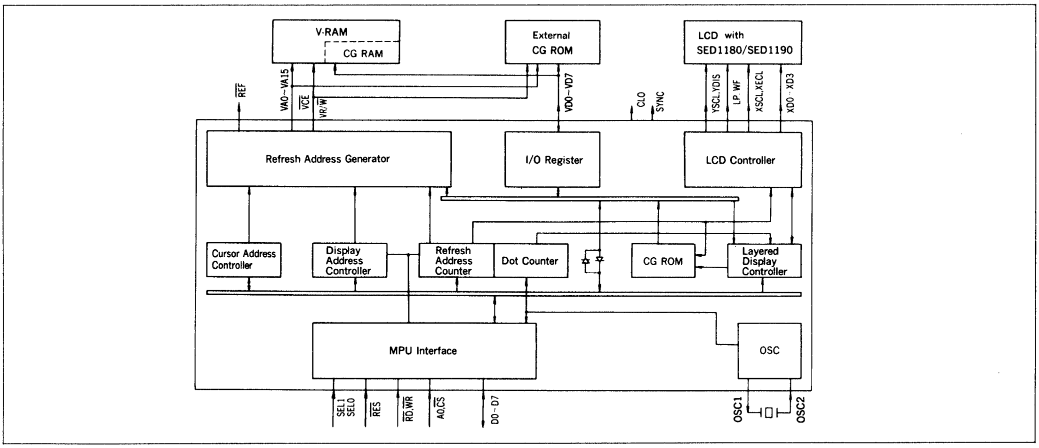
■DESCRIPTION

The SED1330F is a Graphic and Character display controller for large-scale dot matrix liguid crystal displays. The external frame buffer stores the character code and/or bit image data from a microprocessor. The data is periodically read out and outputted as the converted bit image data for the display. The SED1330F's enhanced control functions allow layered displays of the character and graphic screens, flexible scrolling and devision of the display. The built-in external memory timing circuit, LCD module control circuit and high speed character generator make it easier to design an LCD control block requiring few external circuits.

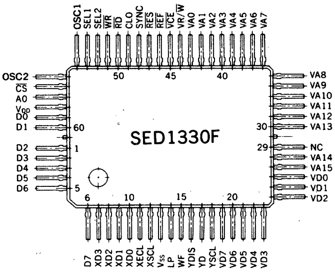
■FEATURES

●Automatic cursor shift function	4 directions, up, down, right and left
●Flexible scrolling function	Free scrolling of the display window of character/graphic screen Smooth scrolling to right and left
●3 modes of display	Character mode, Graphic mode, 2-screen layered mode
●Display dots	Character mode : 80 characters x 32 lines plus layered graphic screen Graphic mode : 256 x 640 dots x 3 screen
●Frame buffer memory space	64K bytes
●Built-in Character Generator	160 characters (5 x 7 dot matrix, mask programmable)
●External Character Generators	CGRAM : 64 characters (8 x 16 dot matrix) CGROM : 256 characters (8 x 16 dot matrix)
●LCD drive duty ratio	Static to 1/256 duty (programmable)
●80 series or 68 series MPU interface (selectable)	
●Low supply current	Operation : 5mA (Typ), Standby : 0.05μA (Typ)
●Single power supply	5V±10%
●Package	60 pin QFP (Plastic)

■BLOCK DIAGRAM



■PIN CONFIGURATION



■PIN DESCRIPTION

Pin Name	Pin No.	Functions	Pin Name	Pin No.	Functions
OSC1	54	Oscillator terminal (Input)	VA0 to VA15	27, 28 30 to 43	VRAM address bus
OSC2	55	Oscillator terminal (Output)	VD0 to VD7	19 to 26	VRAM data bus
V_{DD}	58	Power supply (+5V)	VR/$\overline{W}$	44	VRAM R/$\overline{W}$ signal
V_{SS}	13	Power supply (GND)	$\overline{VCE}$	45	Memory control signal
SEL1,2	53, 52	MPU interface format selection	$\overline{REF}$	46	Refresh signal for DRAM
D0 to D7	59,60 1 to 6	Data bus	XD0toXD3	7-10	Dot data output bus to X driver
A0	57	Data type selection	XSCL	12	Dot data shift clock for X driver
$\overline{RD}$	50	80 series Read strobe signal 68 series "E" clock	XECL	11	Chip enable shift clock for X driver
$\overline{WR}$	51	80 Series Write strobe signal 68 series R/$\overline{W}$ signal	LP	14	Dot data latch pulse
$\overline{CS}$	56	Chip select	WF	15	Frame signal
$\overline{RES}$	47	Reset	YSCL	18	Scan data shift clock for Y driver
SYNC	48	I/O pin for synchronization signal	YD	17	Scan data output
CLO	49	Synchronized clock input for slave GLC	YDIS	16	Power down signal when display OFF

■ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.3 to 7.0	V
Input voltage	V_I	−0.5 to V_{DD}+0.5	V
Power dissipation	P_D	0.3	W
Operating temperature	T_{opr}	−20 to 75	°C
Storage temperature	T_{stg}	−60 to 150	°C
Soldering temperature and time	T_{sol}	260°C, 10s (at lead)	—

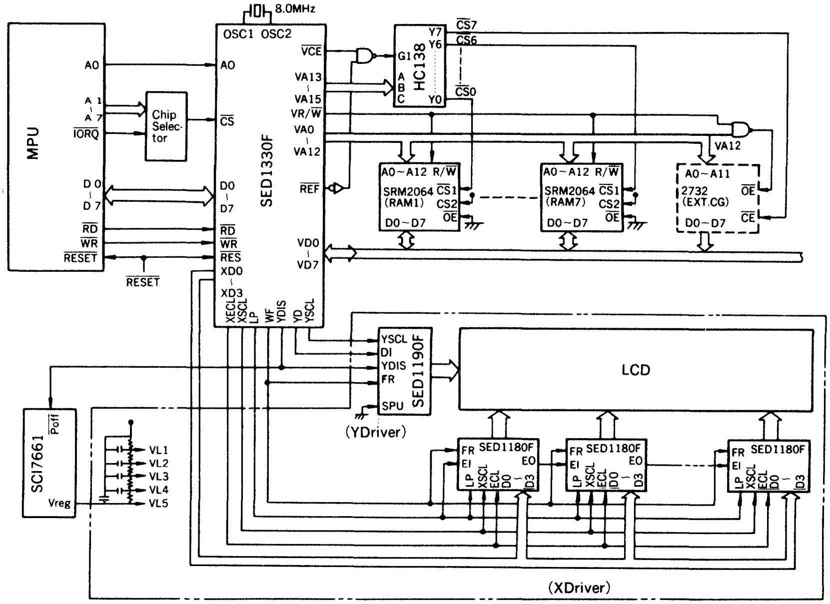
■ELECTRICAL CHARACTERISTICS

(V_{DD}=5V±10%, V_{SS}=0V, Ta=−20 to 75°C)

	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
	Operating voltage	V_{DD}		4.5	5.0	5.5	V
	Register data retention voltage	V_{DH}		2.0	—	6.0	V
TTL	High level input voltage	V_{IHT}	D0toD7, A0, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, VD0toVD7, IOH=−5.0mA, IOL=5.0mA, VR/$\overline{W}$, $\overline{VCE}$, $\overline{REF}$	2.2	—	V_{DD}+0.3	V
	Low level input voltage	V_{ILT}		−0.3	—	0.8	V
	High level output voltage	V_{OHT}		2.4	—	—	V
	Low level output voltage	V_{OLT}		—	—	0.4	V
CMOS	High level input voltage	V_{IHC}	IOH=1.6mA, IOL=−1.6mA, SEL1, 2, SYNC, YD, XD0to XD3, XSCL, XECL, LP, FR, YSCL, YDIS, OSC1, OSC2	0.8V_{DD}	—	—	V
	Low level input voltage	V_{ILC}		—	—	0.2V_{DD}	V
	High level output voltage	V_{OHC}		V_{DD}−0.4	—	—	V
	Low level output voltage	V_{OLC}		—	—	0.4	V
SCHMITT	Positive trigger threshold voltage	V_{T+}	$\overline{RES}$ *	0.5V_{DD}	0.7V_{DD}	0.8V_{DD}	V
	Negative trigger threshold voltage	V_{T-}		0.2V_{DD}	0.3V_{DD}	0.5V_{DD}	V
	Input leakage current	I_{LI}	V_I=V_{DD} or V_{SS}	—	0.05	2.0	μA
	Output leakage current	I_{LO}		—	0.10	5.0	μA
	Average operating current	I_{DDA}	fosc=6.0MHz, No load (No external V-RAM)	—	5.0	6.5	mA
	Standby current	I_{DDS}	OSC1=$\overline{CS}$=V_{DD}	—	0.05	20	μA
	Oscillation frequency	f_{OSC}	AT X'tal OSC1, OSC2	1.0	—	10.0	MHz
	External clock frequency	f_{CLK}		—	—	10.0	MHz
	Feed back resistance	R_f		0.5	1.0	7.0	MΩ

* $\overline{RES}$ input pulse should be longer than 1.0ms.
V_{L5} should be OFF when $\overline{RES}$ is "L".

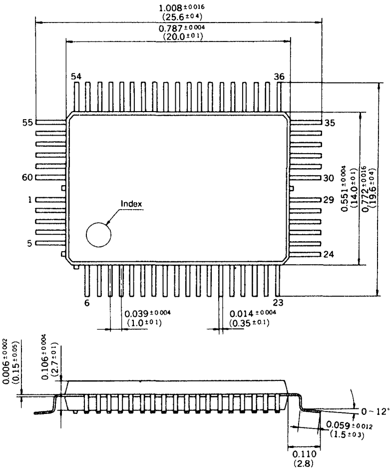
EXAMPLE OF APPLICATION



PACKAGE DIMENSIONS

F60-5

60-pin QFP



unit : inch
(mm)

CHARACTER CODE TABLE (BUILT-IN CHARACTER GENERATOR)

	Lower 4 bit (D0 to D3) of Character Code (Hexadecimal)															
Higher 4 bit (D4 to D7) of Character Code (Hexadecimal)	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**A**	**B**	**C**	**D**	**E**	**F**
2		!	"	#	$	%	&	'	(	)	*	+	,	-	.	/
3	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
4	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
5	P	Q	R	S	T	U	V	W	X	Y	Z	[	¥	]	^	_
6	`	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
7	p	q	r	s	t	u	v	w	x	y	z	{	|	}	→	←
A		｡	｢	｣	､	･	ｦ	ｧ	ｨ	ｩ	ｪ	ｫ	ｬ	ｭ	ｮ	ｯ
B	ｰ	ｱ	ｲ	ｳ	ｴ	ｵ	ｶ	ｷ	ｸ	ｹ	ｺ	ｻ	ｼ	ｽ	ｾ	ｿ
C	ﾀ	ﾁ	ﾂ	ﾃ	ﾄ	ﾅ	ﾆ	ﾇ	ﾈ	ﾉ	ﾊ	ﾋ	ﾌ	ﾍ	ﾎ	ﾏ
D	ﾐ	ﾑ	ﾒ	ﾓ	ﾔ	ﾕ	ﾖ	ﾗ	ﾘ	ﾙ	ﾚ	ﾛ	ﾜ	ﾝ	ﾞ	ﾟ
1	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨

Note : ▨ means all dots of 6 x 8 matrix are on.

PF366-01

SED1351F

CMOS GRAPHIC LCD CONTROLLER

●Operation Under the Control of 8Bits or 16Bits MPU
●Cycle Steal Mode for MPU's Access to VRAM
●Maximum Display Capacity 1,024×512 Dots (524,288 Dots)

■DESCRIPTION

The SED1351F is a high-duty dot matrix graphic display LCD controller. It can interface with an 8bits or 16bits MPU having a READY ($\overline{\text{WAIT}}$) input pin. Cycle steal mode is used to have the MPU access the VRAM so that the display is not disturbed. The SED1351F contains circuits that control all data and addresses for cycle steal operations and requires no external data/address control circuit. Furthermore, the device has a chip select output pin for VRAM. This makes it possible to directly connect up to eight 64K SRAMs or two 256K SRAMs to the SED1351F without using an external decoder.

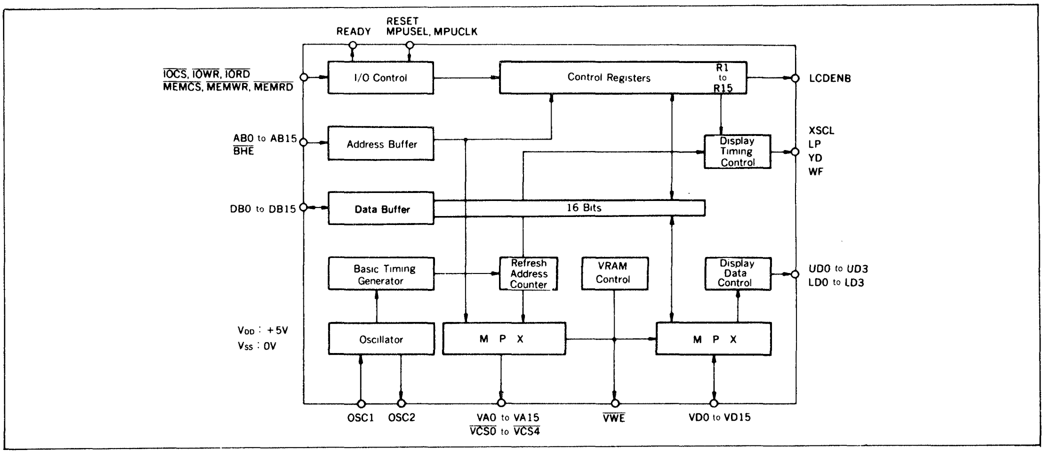
The VRAM addresses are mapped in the MPU memory space. This feature enables the MPU to directly address any display data for efficient data manipulation especially when the user is drawing a picture.

The SED1351F is available with two display modes to choose from, binary mode (on/off only) and gray mode (on/off and two gray steps). Use of the full 64K bytes capacity of VRAM makes it possible to display a maximum of 524,288 dots in the binary mode and 262,144 dots in the gray mode.

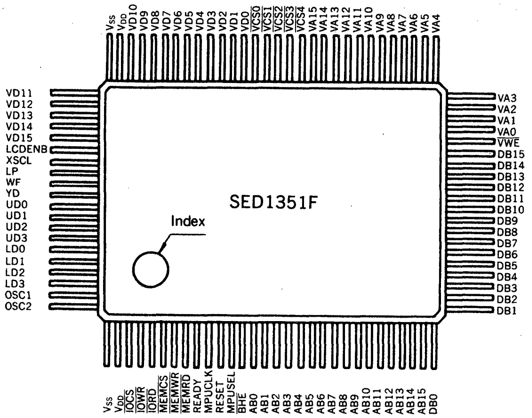
■FEATURES

●VRAM capacity	64K bytes (Mapping : MPU memory space)
●LCD display modes	Binary (ON/OFF only) Gray (ON/OFF+two gray steps)
●LCD panel	1-screen configuration (4bits or 8bits data transfer) 2-screen configuration (4bits data transfer for each display)
●Maximum number of horizontal	256 characters 2,048 dots (Binary display mode) / 1,024 dots (Gray display mode)
●Maximum number of vertical lines	1,024 lines (1-screen drive) / 2,048 lines (2-screen drive)
●Panel division/OR function	Either to be selected in 1-screen drive mode
●Interface with MPU through use of READY ($\overline{\text{WAIT}}$) signal	
●Capability of using virtual display panel	
●Smooth vertical scrolling	
●Chip select output for VRAM	
●Single power supply	5V±10%
●Package	100pin QFP (Plastic)

■BLOCK DIAGRAM



■PIN CONFIGURATION



■PIN DESCRIPTION

Pin Name	Pin No.	Functions
DB0 to DB15	30 to 45	MPU data bus
AB0 to AB15	14 to 29	MPU address bus
$\overline{\text{BHE}}$	13	Bus high enable
$\overline{\text{IOCS}}$	3	Control register chip select
$\overline{\text{IOWR}}$	4	Control register write enable signal input
$\overline{\text{IORD}}$	5	Control register read enable signal input
$\overline{\text{MEMCS}}$	6	VRAM control chip select
$\overline{\text{MEMWR}}$	7	VRAM control write enable signal input
$\overline{\text{MEMRD}}$	8	VRAM control read enable signal input
READY	9	Ready ($\overline{\text{wait}}$) signal
MPUCLK	10	MPU clock
MPUSEL	12	MPU selection (16bits/8bits)
RESET	11	Reset signal
VD0 to VD15	68 to 78 81 to 85	VRAM data bus
VA0 to VA12	47 to 59	VRAM address bus
VA13/$\overline{\text{VCS7}}$ to VA15/$\overline{\text{VCS5}}$	60 to 62	VRAM address/chip select

Pin Name	Pin No.	Functions
$\overline{\text{VCS0}}$ to $\overline{\text{VCS4}}$	67 to 63	VRAM chip select
$\overline{\text{VWE}}$	46	VRAM write enable signal output
UD0 to UD3	91 to 94	Upper panel dot data
LD0/UD4 to LD3/UD7	95 to 98	Lower/upper panel dot data
XSCL	87	Dot data shift clock
LP	88	Dot data latch pulse
WF	89	Frame signal (LCD AC signal)
YD	90	Scan data output
LCDENB	86	LCD control signal
OSC1	99	Oscillator terminal (Input)
OSC2	100	Oscillator terminal (Output)
V_{DD}	2	Supply voltage (+5V)
V_{SS}	1	GND

■ABSOLUTE MAXIMUM RATINGS

($V_{SS}=0V$)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	$V_{SS}-0.3$ to 7.0	V
Input voltage	V_I	$V_{SS}-0.3$ to $V_{DD}+0.3$	V
Output voltage	V_O	$V_{SS}-0.3$ to $V_{DD}+0.3$	V
Output current/pin	I_O	±10	mA
Power dissipation	P_D	200	mW
Supply current	I_{DD}/I_{SS}	±40	mA
Storage temperature	T_{stg}	−65 to 150	℃
Soldering temperature and time	T_{sol}	260℃, 10s (at lead)	—

■RECOMMENDED OPERATING CONDITIONS

($V_{SS}=0V$)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
Input voltage	V_I		V_{SS}	—	V_{DD}	V
Operating temperature	T_{opr}		−20	—	75	℃

■ELECTRICAL CHARACTERISTICS

●DC Characteristics

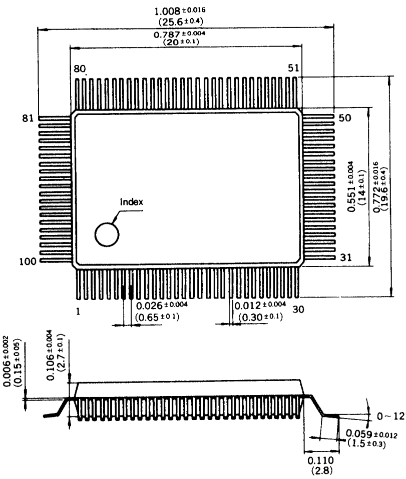
(Ta = −20℃ to 75℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Static current	I_{DDS}	$V_{IN}=V_{DD}, V_{SS}$ $I_{OH}=I_{OL}=0$	—	—	100	μA
Input leakage current	I_{L1}	$V_{DD}=5.5V$ $V_{IH}=V_{DD}$ $V_{IL}=V_{SS}$	−10	—	10	μA
High level input voltage 1	V_{IH1}	$V_{DD}=5.5V$	3.5	—	—	V
Low level input voltage 1	V_{IL1}	$V_{DD}=4.5V$	—	—	1.0	V
High level input voltage 2	V_{IH2}	$V_{DD}=5.5V$	2.0	—	—	V
Low level input voltage 2	V_{IL2}	$V_{DD}=4.5V$	—	—	0.8	V
High level input voltage 3	V_T+	$V_{DD}=5.5V$	—	—	4.0	V
Low level input voltage 3	V_T-	$V_{DD}=4.5V$	0.8	—	—	V
Hysteresis voltage	V_H	$V_{DD}=5V$	0.3	—	—	V
High level output voltage 1	V_{OH1}	$V_{DD}=4.5V$ $I_{OH}=-2mA$ $I_{OL}=6mA$	$V_{DD}-0.4$	—	—	V
Low level output voltage 1	V_{OL1}		—	—	$V_{SS}+0.4$	V
High level output voltage 2	V_{OH2}	$V_{DD}=4.5V$ $I_{OH}=-50\mu A$ $I_{OL}=50\mu A$	$V_{DD}-0.4$	—	—	V
Low level output voltage 2	V_{OL2}		—	—	$V_{SS}+0.4$	V

■PACKAGE DIMENSIONS

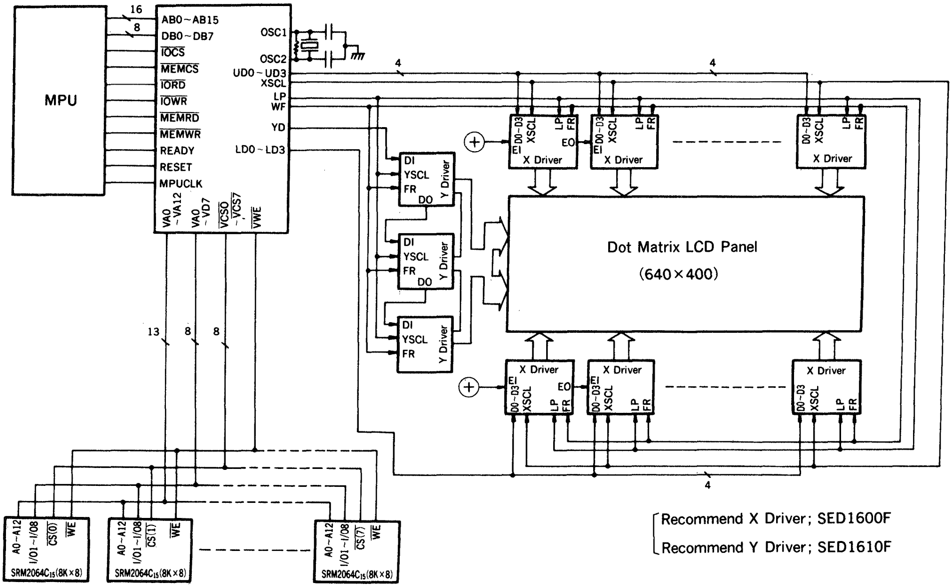
F100-5

100-pin QFP



unit : inch
(mm)

■EXAMPLE OF APPLICATION (When using an 8bits MPU)



Recommend X Driver; SED1600F
Recommend Y Driver; SED1610F

*Depend on the screen size of LCD, number of frame buffer memory will be changed.

PF286-02

SED1341F$_{0C}$

CMOS VIDEO-LCD INTERFACE (VLI)

- **Video/LCD Signal Converter LSI**
- **Simplified Screen Alignment**
- **Internal Oscillator for LCD Display Operation (Independent of Video Signal)**

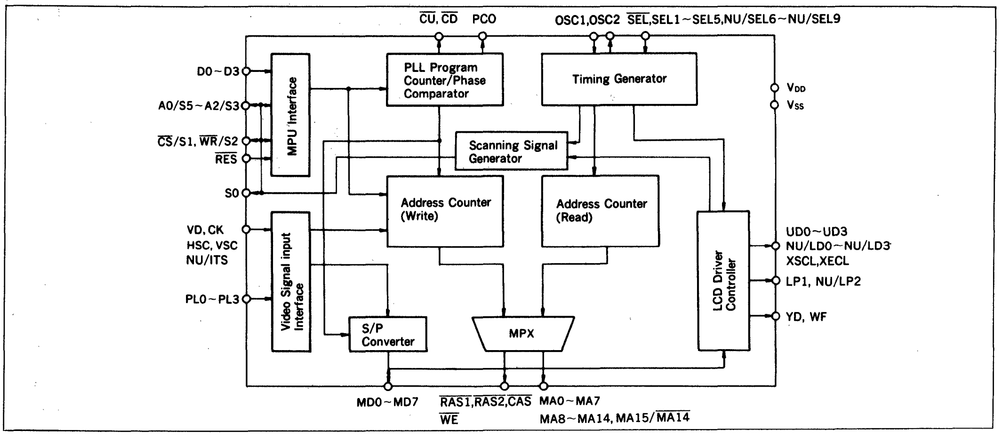
■DESCRIPTION

The SED1341F VLI (Video-LCD Interface) converts a split composite video signal used to drive CRT displays into a data format necessary to drive dot-matrix liquid crystal displays. With the addition of a sync signal/ data separator composite signals can also be processed, making it is possible to replace a CRT display (without brightness gradation) with a liquid crystal display panel, needing no special software or hardware. A frame buffer allows the VLI to accurately match the higher frequency video signals to the lower frequency operation of the LCD unit. In addition, the VLI has a screen alignment function for fine adjustment. These functions make it easy to create an LCD terminal that is plug-compatible with CRT display connectors.

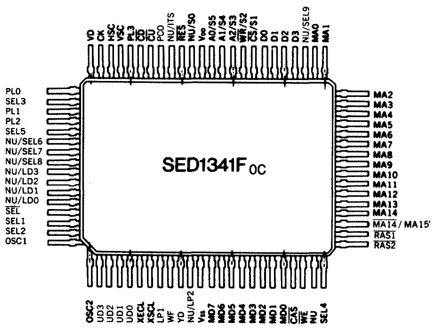
■FEATURES

- Makes LCD monitor plug-compatible with CRT connectors
- Screen size : 640 × 200 dots, 640 × 350 dots, 640 × 400 dots, 640 × 480 dots
- LCD Interface
  - ○ Internal oscillator enables setting of frame frequency to match LCD unit f_{OSC}=11.2MHz (Max)
  - ○ Duty ratio ……………… 1/100, 1/200, 1/400, 1/175, 1/350, 1/102, 1/202, 1/402, 1/177, 1/352, 1/104, 1/208, 1/416, 1/183, 1/366, 1/240, 1/480, 1/242, 1/482, 1/248, 1/496
  - ○ Scan mode ……………… 1-screen drive, 2-screen drive
  - ○ X-driver interface ……………… 4-bit bus, 4-bit × 2 bus, 8-bit bus, Enable-chain type
  - ○ LCD drive method ……………… 2-frame AC
- Video signal interface ……………… Horizontal scan frequency : 15.69kHz (Typ), 24.83kHz (Typ)
  - ○ TTL-compatible separate signal input
    Video data, horizontal sync signal, vertical sync signal, dot clock
  - ○ Internal PLL (Phase lock loop circuit) program counter (1/706~1/961), Internal phase comparator
    Dot clock generation via PLL : 14.32MHz (Typ), 21.05MHz (Typ), f_{CK}=34MHz (Max)
  - ○ Screen alignment fine adjustment …… Register program method via 4-bit bus
- Direct control of 64K DRAM/SRAM, 256K SRAM for frame buffer memory (40K × 8 bits Max)
- Pin compatible with SED1341F$_{0A,0B}$
- Single power supply ……………… 5V±5%
- Package ……………… 80-pin QFP (plastic)

■BLOCK DIAGRAM



■PIN CONFIGURATION



NU : NOT USE

■PIN DESCRIPTION

Pin Name	Pin No.	Functions
V_{DD} V_{SS}	53 12	Supply voltage (+5V) GND
OSC1 OSC2	80 1	Oscillator terminal (Input) Oscillator terminal (Output)
UD0 to UD3, NU/LD0 to NU/LD3 XECL XSCL LP1, NU/LP2 WF YD	5 to2,76 to 73 6 7 8, 11 9 10	X driver data bus output X driver enable shift clock output X driver shift clock output Latch pulse output AC wave form output for the LCD Row scanning start data output for Y driver
VD CK HSC VSC NU/ITS	64 63 62 61 56	Video data input Dot clock input Horizontal sync signal input Vertical sync signal input ITS (Half tone) signal input
MA0 to MA14,$\overline{\mathrm{MA14}}$/MA15 MD0 to MD7 $\overline{\mathrm{RAS1}}$, $\overline{\mathrm{RAS2}}$ $\overline{\mathrm{CAS}}$ $\overline{\mathrm{WE}}$	42 to 28,27 20 to 13 26, 25 21 22	Address bus output to frame buffer memory Data bus I/O to frame buffer memory Row address strobe signal output Column address strobe signal output Write enable signal output

Pin Name	Pin No.	Functions	
D0 to D3	47 to 44	Data input for screen position register	
		SEL5="L"	SEL5="H"
NU/S0	54	NU	Scan signal output for digital switch
A0/S5 to A2/S3	52 to 50	Address bus input	Scan signal output for digital switch
$\overline{\text{CS}}$/S1	48	Chip select signal input	Scan signal output for digital switch
$\overline{\text{WR}}$/S2	49	Write signal input	Scan signal output for digital switch
$\overline{\text{RES}}$	55	Reset signal input	
$\overline{\text{SEL}}$	77	When $\overline{\text{SEL}}$ is "L", SEL6 to SEL9, ITS are enabled	
SEL1	78	Drive mode select input (1-screen drive/2-screen drive)	
SEL2	79	SCREEN SIZE select input > 640×200, 640×350, 640×400, 640×480	
SEL3	66	SCREEN SIZE select input	
SEL4	24	Frame buffer memory select input (SRAM/DRAM)	
SEL5	69	Screen alignment method select input (SW/MPU)	
NU/SEL6	70	Select input for Vertical back porch (invalid/valid)	
NU/SEL7	71	Timing select input for Latch pulse output (edge/level)	
NU/SEL8	72	X driver interface select input (4 bit bus/4 bit×2 bus, 8 bit bus)	
NU/SEL9	73	Line select input for back porch (8, 16 lines/2, 4 lines)	
PL0 to PL3	65,67,68,60	Polarity select input for video signal	
PCO	57	Program counter output in PLL Section	
$\overline{\text{CU}}$, $\overline{\text{CD}}$	58, 59	Phase comparator output in PLL Section (connect to charge pump)	

*If terminal No.77 ($\overline{\text{SEL}}$) is set to the "H" level, terminal No.70 to No.72 and No.56 become the NU terminal, and all the inputs of SEL6 to SEL8 are considered as "H" level.
For this reason, the pins are compatible with those in SED1341F$_{0A}$.

■ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Supply voltage*	V_{DD}	−0.3 to 7.0	V
Input voltage*	V_I	−0.3 to V_{DD}+0.3	V
Output voltage*	V_O	−0.3 to V_{DD}+0.3	V
I/O voltage*	$V_{I/O}$	−0.3 to V_{DD}+0.3	V
Output current	I_O	−10 to 10	mA
Power dissipation	P_D	250	mW
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−65 to 150	°C
Soldering temperature and time	T_{sol}	260°C, 10s (at lead)	—

* Vss=0V

■RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}		4.75	5.00	5.25	V
Supply voltage	V_{SS}		—	0	—	V

■ELECTRICAL CHARACTERISTICS

●DC Characteristics

(Ta=0 to 70°C, V_{DD}=5V±5%, V_{SS}=0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Oscillation frequency	f_{OSC}	f_{CK}=14.3MHz f_{CK}=21MHz	f_{CK}/3.6	4.5 9	11.2 and f_{CK}/2.28	MHz
Average operating current consumption	I_{OPR}	f_{CK}=32MHz, f_{OSC}=11MHz	—	—	40	mA
High level input voltage 1	V_{IH1}	*1	2.0	—	V_{DD}+0.3	V
Low level input voltage 1	V_{IL1}		−0.3	—	0.8	V
High level input voltage 2	V_{IH2}	*2	4.0	—	V_{DD}+0.3	V
Low level input voltage 2	V_{IL2}		−0.3	—	0.8	V
High level input voltage 3	V_{IH3}	*3	3.0	—	V_{DD}+0.3	V
Low level input voltage 3	V_{IL3}		−0.3	—	0.6	V
High level output voltage	V_{OH}	I_{OH}=−2mA*4	4.35	—	—	V
Low level output voltage	V_{OL}	I_{OL}=6mA*4	—	—	0.4	V
Input current leakage	I_{LI}	V_I=0V to V_{DD}	−1	—	1	μA
I/O current leakage	$I_{LI/O}$	$V_{I/O}$=0V to V_{DD}	−1	—	1	μA

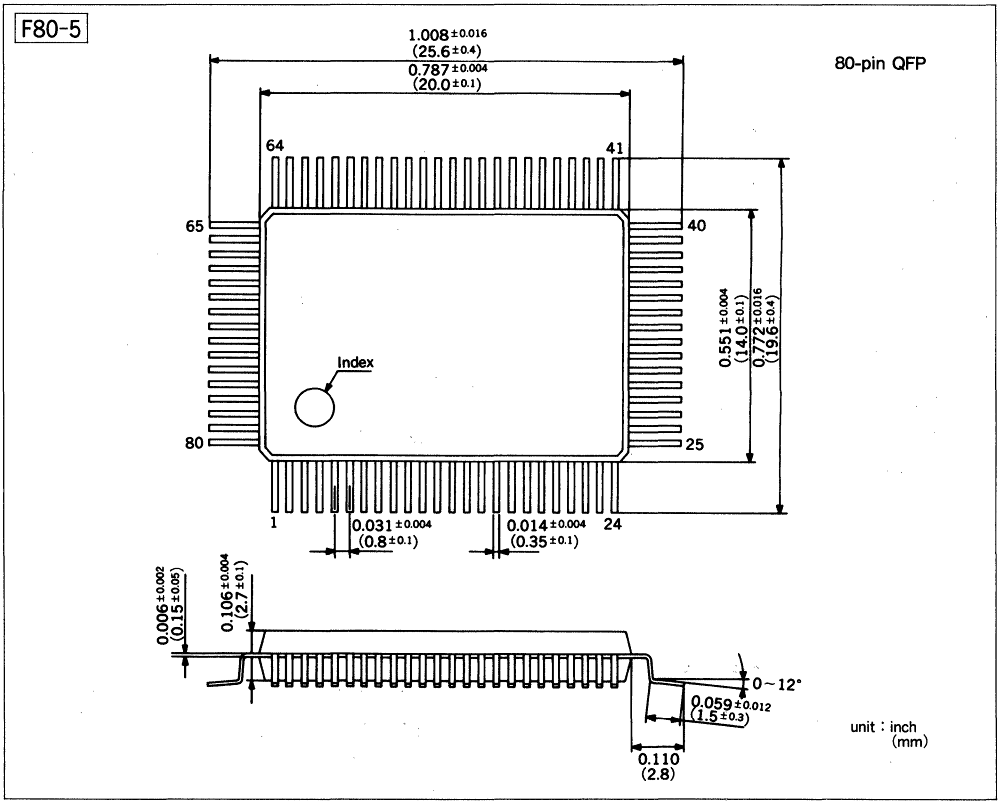
*1 Terminal: VD, CK, HSC, VSC, NU/ITS, MD0 to MD7, A0 to A2, $\overline{\text{CS}}$, $\overline{\text{WR}}$, NU/SEL9

*2 Terminal: $\overline{\text{SEL}}$, SEL1 to SEL5, PL0 to PL3, NU/SEL6 to NU/SEL8, D0 to D3

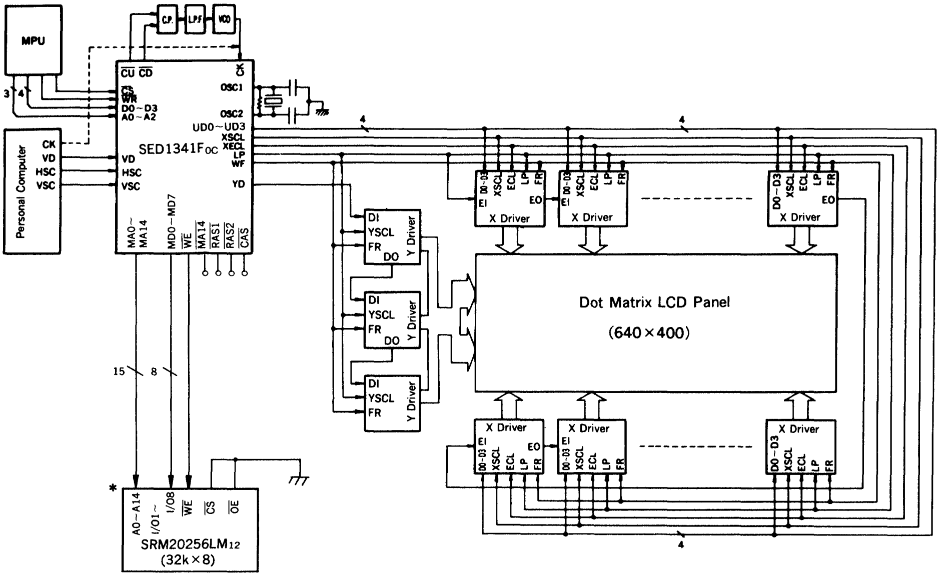
*3 Terminal: $\overline{\text{RES}}$

*4 Terminal: (except OSC2 pin)

■PACKAGE DIMENSIONS



■EXAMPLE OF APPLICATION



Recommend X Driver ; SED1180F, SED1600F
Recommend Y Driver ; SED1190F, SED1610F

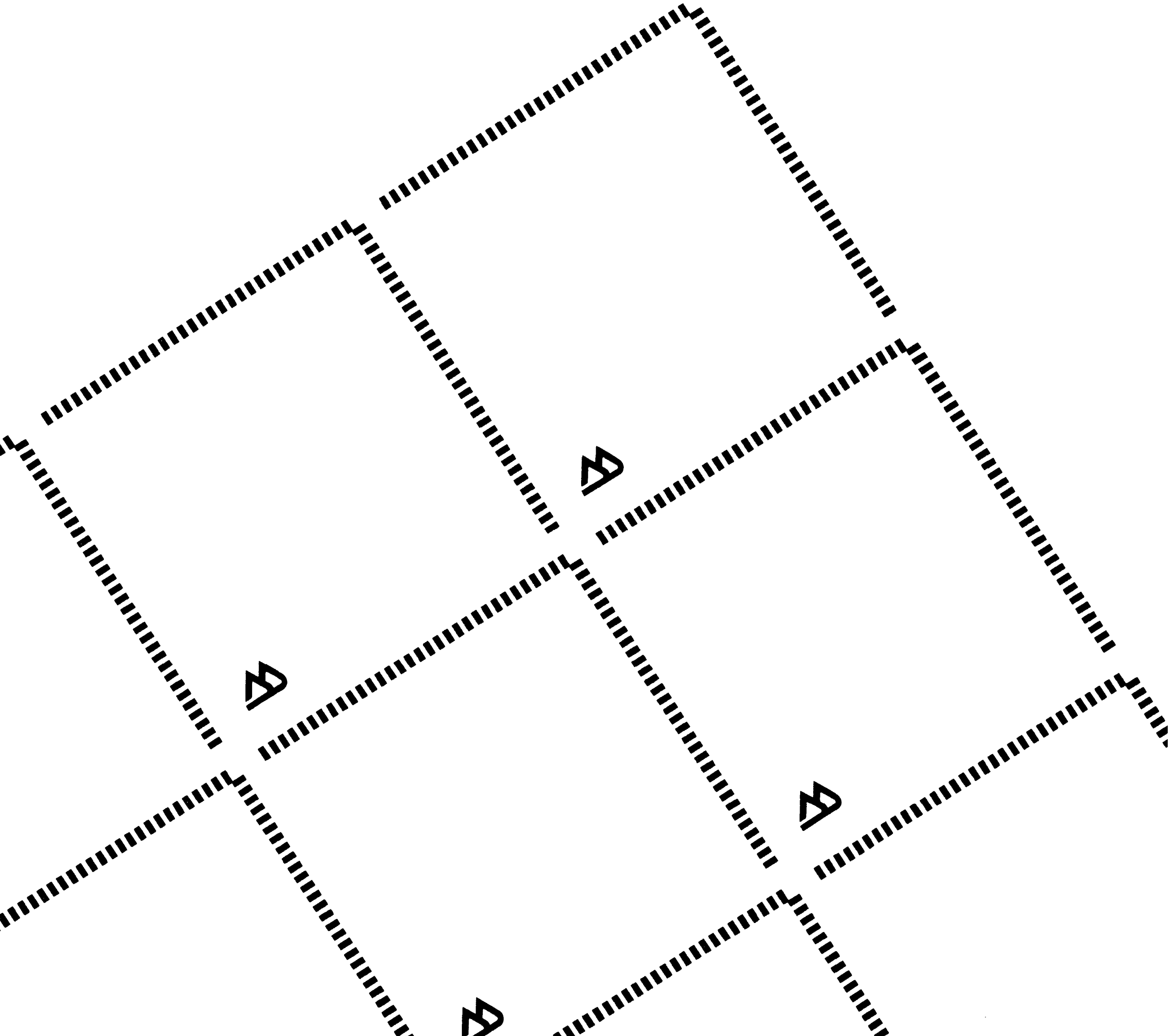
* Depend on the screen size of LCD, number of frame buffer memory will be changed.

640×200dots→2pieces (64KSRAM or 64KDRAM)

640×350dots→64KSRAM 4 pieces or 256KSRAM 1 piece
640×480dots→64KSRAM 1 piece and 256KSRAM 1 piece

1988/1989 CMOS
DATA BOOK

F. TELECOMMUNICATION PRODUCTS



STC9430C Series

CMOS 300bps FSK SINGLE CHIP MODEM

- ●High Data Quality
- ●Low Supply Current
- ●5V Single Power Supply

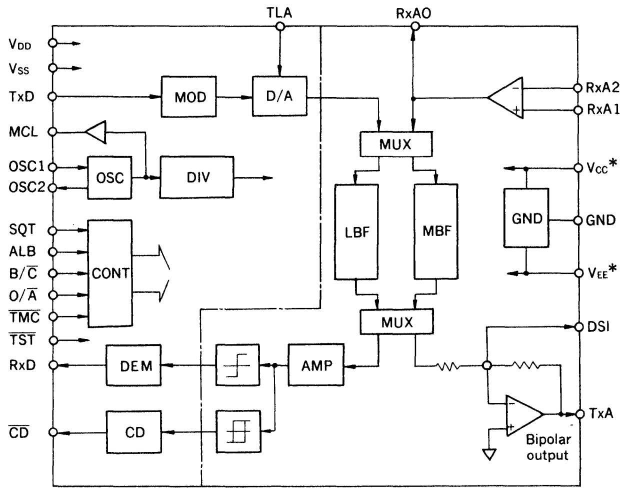
■DESCRIPTION

The STC9430C Series LSI is a CMOS 300bps FSK full-duplex modem operating on a single 5V supply. It provides all functions needed for a modem compatible with the Bell 103J specifications and the CCITT recommendations. The STC9430C also incorporates a power-saving function and a transmit-receive buffer amplifier which can be configured adaptively to any line interface the user desires. These excellent features offer a high-performance solution to home security, telemetering terminal, and other modem applications.

■FEATURES

●0-300bps FSK full duplex modem	Bell 103J, CCITT V.21
●Built-in line interface	Built-in buffer amplifier for hybrid circuit. (Outputs bipolar signals.)
●Full duplex band pass filter	Built-in leap frog SCF
●High data quality	Bit error rate (Receive level −30dBm) Bell mode : 1×10^{-5}Max (S/N≧6dB) CCITT mode : 1×10^{-5}Max (S/N≧5dB)
●Low supply current	Operation : 75mW (Typ) Stand-by : 10μW (Max)
●Supply voltage	5V single power supply
●Digital I/O level	TTL compatible
●Built-in oscillation circuit	3.579545MHz : Externally connected X'tal & capacitor
●Test function	Built-in Analog loop back test mode
●Package	20-pin DIP (plastic)/24-pin DIP (plastic)/24-pin SOP (plastic)

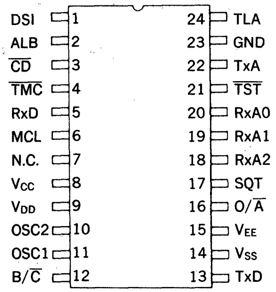
■BLOCK DIAGRAM



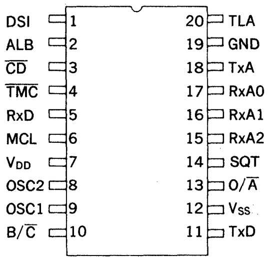
* The STC9430C0A has no V_{EE} and V_{CC} pins.

PIN CONFIGURATION

24-pin DIP/24-pin SOP



20-pin DIP



N.C.: No connection

PIN DESCRIPTION

Pin name	Pin No.		I/O	Functions
	20 pin	24 pin		
DSI	1	1	I	[Transmit Buffer Amplifier Inverted Signal] Receives DTMF (Dual Tone Multi-Frequency) and other external signals.
ALB	2	2	I_1	[Analog Loop-Back] When this signal goes high, the send output turns to a receive input and the system enters the LSI self-test mode. If both ALB and SQT go high, the power-saving mode results.
$\overline{\text{CD}}$	3	3	O	[Carrier Detect] This signal goes low when a specified level of energy is detected within the receive frequency band.
$\overline{\text{TMC}}$	4	4	I_1	[Timer Select] Selects a carrier detection timer response time. Short : High level Long : Low level
RxD	5	5	O	[Receive Data] Outputs demodulated output. Mark : High level Space : Low level
MCL	6	6	O	[Master Clock] Outputs the master clock (3.579545MHz) for supply to a tone dialer or other external circuits
V_{CC}	—	8	—	[V_{CC} Power] +5V (24 pin type : Analog, positive)
V_{DD}	7	9	—	[V_{DD} Power] +5V (24 pin type : Digital, positive) (20 pin type : Analog/digital, positive)
OSC2	8	10	O	[Oscillation Output] A crystal oscillator (3.579545MHz) and, an oscillation capacitor are connected to this pin.
OSC1	9	11	I	[Oscillation Output] A crystal oscillator (3.579545MHz) and an oscillation capacitor are connected to this pin (If external oscillation is used, it enters through this pin.)
B/$\overline{\text{C}}$	10	12	I_1	[Bell/CCITT Select] Selects the Bell or CCITT mode. Bell : High level CCITT : Low level
TxD	11	13	I_1	[Send Data] Receives send data. Mark : High level Space : Low level
V_{SS}	12	14	—	[V_{SS} Power] 0V (24 pin type : Digital, negative) (20 pin type : Analog/digital, negative)

(Continue)

The input pin has an on-chip pull-up resistor. If not used, however, it should preferably be fixed to V_{DD} level for protection against noise.

Pin name	Pin No.		I/O	Functions
	20 pin	24 pin		
V_{EE}	—	15	—	[V_{EE} Power] 0V (24 pin type: Analog, negative)
$O/\overline{A}$	13	16	I_1	[Originate/Answer Mode Select] Originate mode: High level Answer mode: Low level
SQT	14	17	I_1	[Transmit Carrier Squelch] Controls send carrier on/off. Off: High level On: Low level
RxA2	15	18	I	[Receive Buffer Amplifier Inverted Signal]
RxA1	16	19	I	[Receive Buffer Amplifier Non-inverted Signal]
RxA0	17	20	O	[Receive Buffer Amplifier Output]
$\overline{TST}$	—	21	I_1	[LSI Test Signal]
TxA	18	22	O	[Transmit Buffer Amplifier Signal] Outputs bipolar signals.
GND	19	23	O	[Signal Ground Output] Outputs the intermediate potential of an analog signal. ($V_{GND} \simeq 1/2\ V_{CC}$)
TLA	20	24	I	[Transmit Level Control]

I_1 The input pin has an on-chip pull-up resistor. If not used, however, it should be fixed to the V_{DD} level for protection against noise.

■STC9430C SERIES

Name	Package	
	Pin	Type
STC9430C$_{0A}$	20	DIP (plastic)
STC9435C$_{0A}$	24	DIP (plastic)
STC9435M$_{0A}$	24	SOP (plastic)

■ABSOLUTE MAXIMUM RATINGS

($V_{EE}{}^{*1} = V_{SS} = 0V$)

Parameter		Symbol	Ratings	Unit
Supply voltage	Digital	V_{DD}	0 to 7	V
	Analog	$V_{CC}{}^{*1}$	0 to 7	V
Input voltage	Digital	$V_{ID}{}^{*2}$	$V_{SS}-0.3$ to $V_{DD}+0.3$	V
	Analog	$V_{IA}{}^{*3}$	$V_{EE}-0.3$ to $V_{CC}+0.3$	V
Power dissipation		P_D	500	mW
Storage temperature		T_{stg}	−65 to 150	℃
Soldering temperature and time		T_{sol}	260℃, 10s (at lead)	—

*1 The STC9430C$_{0A}$ has no V_{EE} and V_{CC} pins.
*2 ALB, $\overline{TMC}$, OSC1, $B/\overline{C}$, TxD, $O/\overline{A}$, SQT, $\overline{TST}$, TLA
*3 DSI, RxA1, RxA2

■RECOMMENDED OPERATING CONDITIONS

($V_{EE}{}^{*1} = V_{SS} = 0V$, $f_{OSC} = 3.579545MHz$)

Parameter		Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	Digital	V_{DD}	—	4.5	5.0	5.5	V
	Analog	$V_{CC}{}^{*1}$	—	4.5	5.0	5.5	V
Input voltage	Digital	$V_{ID}{}^{*2}$	—	V_{SS}	—	V_{DD}	V
	Analog	$V_{IA}{}^{*3}$	—	V_{EE}	—	V_{CC}	V
Operating temperature		T_{opr}	—	−10	25	70	℃
Osc. frequency offset		Δf_{OSC}	X'tal/Ext. clock	−0.1	0	+0.1	%

*1 The STC9430C$_{0A}$ has no V_{EE} and V_{CC} pins.
*2 ALB, $\overline{TMC}$, OSC1, $B/\overline{C}$, TxD, $O/\overline{A}$, SQT, $\overline{TST}$, TLA
*3 DSI, RxA1, RxA2

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

(V_{CC}*1 = V_{DD} = 5V, V_{EE}*1 = V_{SS} = 0V, Ta = 25°C)

Parameter	Symbol	Conditions			Min	Typ	Max	Unit
Average operating current	I_{DDA}	ALB or SQT = "L"	$\mathrm{STC9430C_{0A}}$		—	15	30	mA
			$\mathrm{STC9435C_{0A}}$	Digital	—	5	10	mA
			$\mathrm{STC9435M_{0A}}$	Analog	—	10	20	mA
Stand-by current	I_{DDS}	ALB = SQT = "H"	$\mathrm{STC9430C_{0A}}$		—	—	2	μA
			$\mathrm{STC9435C_{0A}}$	Digital	—	—	1	μA
			$\mathrm{STC9435M_{0A}}$	Analog	—	—	1	μA
High level input voltage (1)	V_{IH1}	Digital input except OSC1			2.4	—	V_{DD}	V
Low level input voltage (1)	V_{IL1}				V_{SS}	—	0.8	V
High level input current	I_{IH}	Digital input except OSC1			—	—	1	μA
Low level input current	I_{IL}				5	10	30	μA
High level input voltage (2)	V_{IH2}	OSC1 Ext. clock input condition			4.0	—	V_{DD}	V
Low level input voltage (2)	V_{IL2}				V_{SS}	—	1.0	V
Input frequency	f_{IN}*2				−0.1	(f_{OSC})	+0.1	%
Clock duty	T_1/T_0				35	50	65	%
High level output current (1)	I_{OH1}	V_{OH} = 4.5V	$\overline{\text{CD}}$, RxD		4	6.5	—	mA
Low level output current (1)	I_{OL1}	V_{OL} = 0.5V			6	11.5	—	mA
High level output current (2)	I_{OH2}	V_{OH} = 4.5V	MCL		2	3.5	—	mA
Low level output current (2)	I_{OL2}	V_{OL} = 0.5V			3.5	5.5	—	mA
Analog output impedance	Z_{RxA0}	$V_{SG}-1.2 \leqq V_{RxA0}(V) \leqq V_{SG}+1.2$			4	—	—	kΩ
	Z_{TxA}	$V_{SG}-1.2 \leqq V_{TxA}(V) \leqq V_{SG}+1.2$			1.1	—	—	kΩ
	Z_{SG}	$-0.2 \leqq \Delta V_{SG}$*3 $\leqq +0.2$			3	—	—	kΩ
Receive buffer input impedance	Z_{RxA1}	RxA0 open, f = 0Hz			5	—	—	MΩ
	Z_{RxA2}	RxA0 open, f = 0Hz			5	—	—	MΩ
Transmit buffer feedback resistance	R_{FB}	SQT = "H", ALB = "L"			20	25	30	kΩ
TLA input leakage current	I_{TLA}	$V_{TLA} = V_{SS}$			20	30	45	mA
		$V_{TLA} = V_{DD}$			50	80	140	

*1 The $\mathrm{STC9430C_{0A}}$ has no V_{EE} and V_{CC} pins.
*2 f_{OSC} = 3.579545MHz
*3 Output impedance calculation conditions.

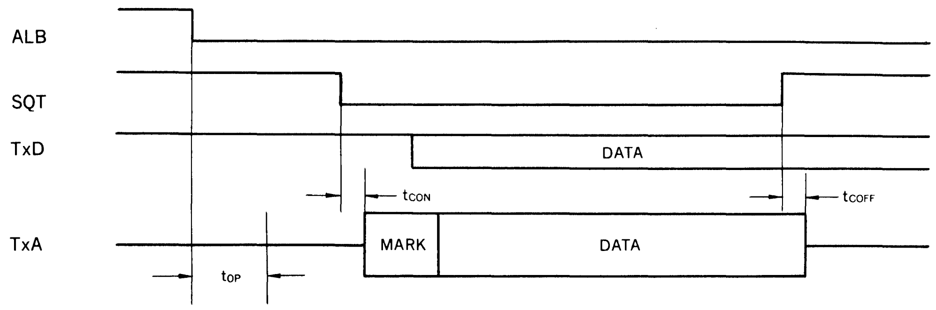
●AC Electrical Characteristics

(f_{OSC} = 3.579545MHz, Ta = 25°C)

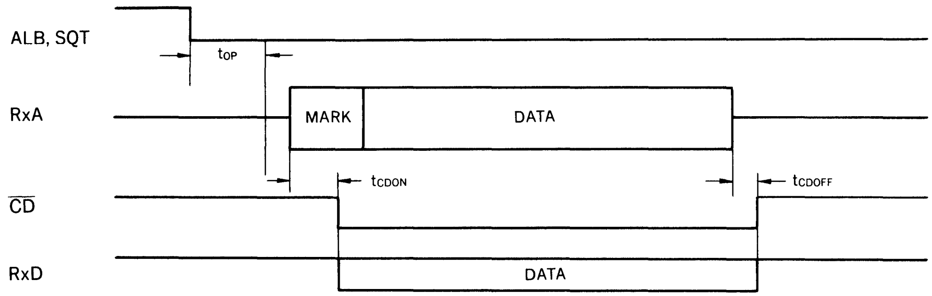
Parameter	Symbol	Conditions		Min	Typ	Max	Unit
After cancel stand-by, operation time	t_{OP}	Transmit & Receive		—	60	100	ms
Carrier on time	t_{CON}	SQT = "H" → "L"		—	3	5	ms
Carrier off time	t_{COFF}	SQT = "L" → "H"		—	—	1	ms
Carrier detect responce time	t_{CDON}	OFF→ON	$\overline{\text{TMC}}$ = "H"	4	15	26	ms
			$\overline{\text{TMC}}$ = "L"	410	435	460	
	t_{CDOFF}	ON→OFF	—	28	36	44	ms

●Timing Chart

○Send Operation



○Receive Operation



●Analog Electrical Characteristics

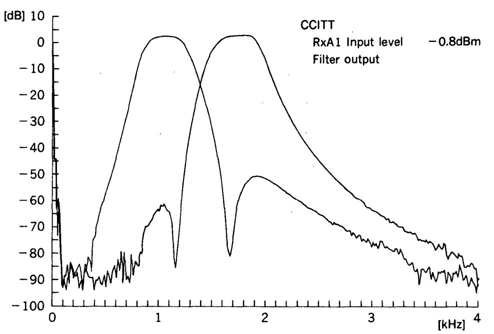
(V_{CC}*1 $= V_{DD} = 5V$, V_{EE}*1 $= V_{SS} = 0V$, $Ta = 25°C$)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
TX signal output level	P_T	TxA open, $R_{TLA} = \infty\ \Omega$		−13	−12	−11	dBm
		TxA open, $R_{TLA} = 0\Omega$		−1	0	+1	
RX signal level	D_R	Receive buffer amp. gain 0dB		−40	—	0	dBm
Carrier detect level	L_{ON}	OFF→ON: On level	Receive buffer amp. gain=0dB	—	−43	−42	dBm
	L_{OFF}	ON→OFF: Off level		−48	−46	—	
	L_H	Hysteresis		2	3	4	dB
Center frequency	f_O*2	CCITT V.21	Low Band	—	1,080	—	Hz
			High Band	—	1,750	—	
		Bell 103J	Low Band	—	1,170	—	
			High Band	—	2,125	—	
Pass bandwidth	f_{BWL}*2	CCITT V.21	Low Band f_O	—	±150	—	Hz
			High Band f_O	—	±150	—	
		Bell 103J	Low Band f_O	—	±150	—	
			High Band f_O	—	±150	—	

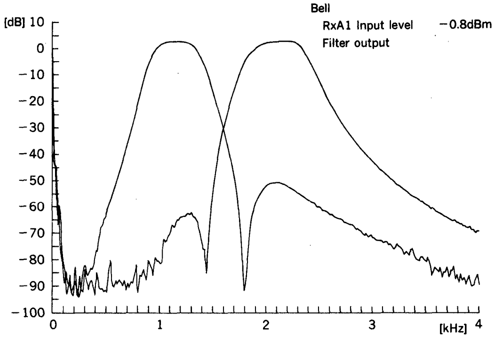
*1 The STC9430C0A has no V_{EE} and V_{CC} pins.
*2 $f_{OSC} = 3.579545MHz$

●Filter Characteristics

○CCITT V.21



○Bell 103J



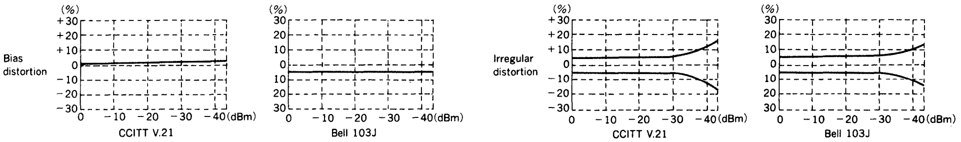
●Data Quality

($V_{CC}{*}^{1}=V_{DD}=5V$, $V_{EE}{*}^{1}=V_{SS}=0V$, $Ta=25°C$)

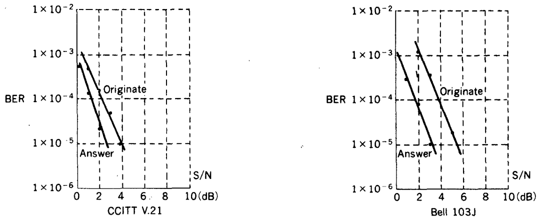
Parameter		Symbol	Conditions	Min	Typ	Max	Unit
Code distortion	Bias distortion	D_B	at ALB	0	—	±4	%
			Receive level : −40dBm	0	—	±4	
	Irregular distortion	D_J	at ALB	—	—	±6	%
			Receive level : −40dBm	—	—	±12	
Bit error rate		BER	CCITT V.21 : S/N=5dB	—	—	1×10^{-5}	—
			Bell 103J : S/N=6dB	—	—	1×10^{-5}	

*1 The STC9430C$_{0A}$ has no V$_{EE}$ and V$_{CC}$ pins.

○Dependence of code distortion on receive input level

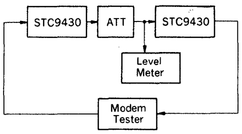


○Bit error rate (Receive level : −30dBm)

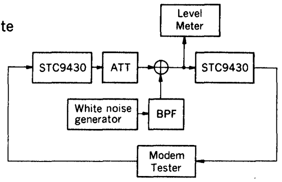


[Accuracy of data measuring circuit]

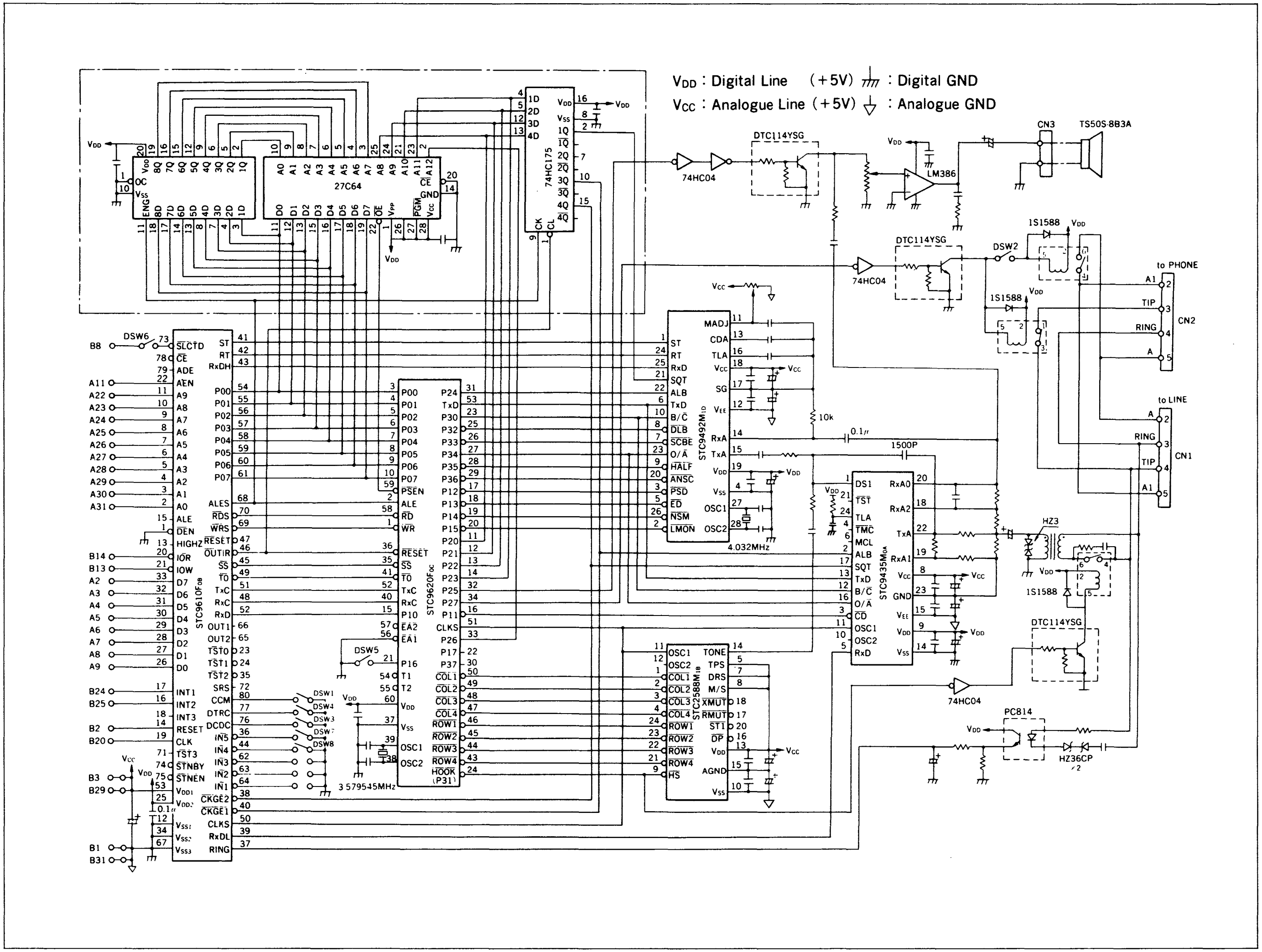
○Code distortion



○Bit error rate

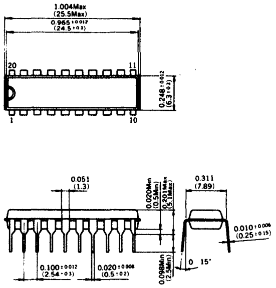


■EXAMPLE OF APPLICATION



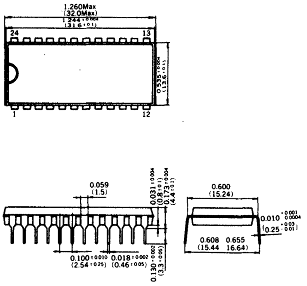
■PACKAGE DIMENSIONS

C20 20-pin DIP



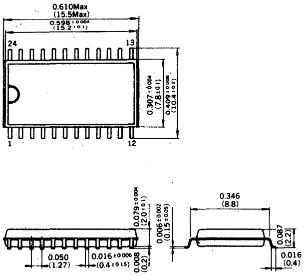
unit : inch
(mm)

C24 24-pin DIP



unit : inch
(mm)

M24 24-pin SOP



unit : inch
(mm)

STC9492C Series

CMOS 1,200bps PSK SINGLE CHIP MODEM

- **Compatible with Bell212A (High speed)/CCITT V.22**
- **Tone Generator Incorporated**
- **Call Progress Tone Detection Function Provided**

DESCRIPTION

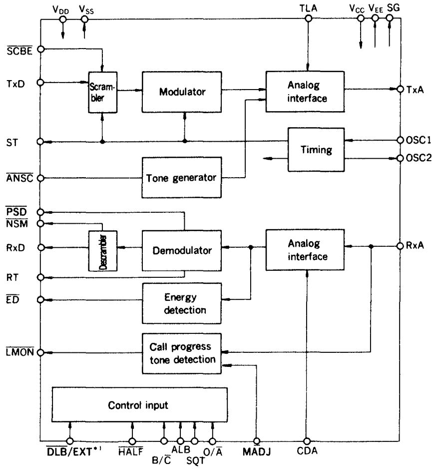
The STC9492C Series is a Bell 212A (high speed)/CCITT V.22 compatible, single chip, 1,200 bps CMOS LSI for a PSK MODEM. The built-in additional functions include answer and guard tones generation functions and a call progress tone detection function.

The high quality switched capacitor circuits and the adaptive equalizing algorithm are adopted in the signal processing, so that they realize highly reliable data quality.

FEATURES

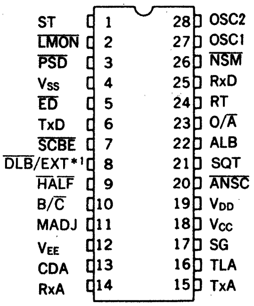
- Compatible with Bell 212A (high speed), CCITT V.22
- Built-in Tone Generator (2,225Hz/2,100Hz/1,800Hz)
- Call Progress Tone Detector On Chip
- Adaptive Equalizer On Chip
- 4.032MHz Crystal Oscillation ······ Quartz oscillator and capacitors externally connected
- Test Function ······ Analog Loop-back Test
  Digital Remote Loop-back Test
- Low Power Consumption ······ Operation : 120mW (Typ)
  Power down : 10μW (Max)
- Input/Output Interface ······ CMOS level
- Single Power Supply ······ 5V ±10%
- Package ······ 28-pin DIP (plastic)/28-pin SOP (plastic)

BLOCK DIAGRAM



*1 is optionally available.

PIN CONFIGURATION (This also applies to DIP and SOP.)



*1 Optionally available.

PIN DESCRIPTION

Pin Name	Pin No.	I/O	Functions
ST	1	O	[Transmit timing output] Outputs a transmit timing signal synchronized with the internal operation.
$\overline{\text{LMON}}$	2	O	[Call progress tone detection output] Detects call progress tones generated during line connection, and outputs their energy envelope.
$\overline{\text{PSD}}$	3	O	[PSK signal detection output] When detects the PSK carrier in a receive signal, this produces low level.
V_{SS}	4	—	[V_{SS} supply for the digital section] 0V
$\overline{\text{ED}}$	5	O	[Carrier detection output] When detects the appointed energy within receive band, this produces low level.
TxD	6	I* *1	[Transmit data input] Inputs transmit data for PSK moduration. Mark : High level Space : Low level
$\overline{\text{SCBE}}$	7	I*	[Scrambler control input] The low level input enables the scrambler active. This should be high level for transmitting non-scrambled data.
$\overline{\text{DLB}}$	8 *2	I*	[Digital remote loop-back test input] The low level input sets a remote digital loop. RxD produces mark continuously during this test mode.
EXT		I*	[External transmit timing input] The external transmit timing can be input to this terminal. Tolerance : within ±0.01% of data transmit speed
$\overline{\text{HALF}}$	9	I*	[1,200bps/600bps selection input] Selects the transmit speed. 1,200bps : High level 600bps : Low level
B/$\overline{\text{C}}$	10	I*	[Bell/CCITT mode selection input] Controls answer tone or guard tone connected with Bell/CCITT mode. Bell : High level CCITT : Low level
MADJ	11	I	[Call progress tone detection level adjust] The call progress tone detection level can be adjusted by supplied voltage. When unused, this should be connected to SG, V_{CC} or V_{EE}.
V_{EE}	12	—	[V_{EE} supply for the analog section] 0V

1 I has a built-in pull-up resistor. *2 Optional selection

Pin Name	Pin No.	I/O	Functions
CDA	13	I/O	[Carrier detection level adjust] Can adjust a carrier detection level by potential difference with SG. (when opened, produces $\simeq V_{SG}+1.0V$)
RxA	14	I	[Receive analog input] Inputs the receive analog signal.
TxA	15	O	[Transmit analog output] Outputs the transmit analog signal.
TLA	16	I/O	[Transmit level adjust] Can adjust a transmit signal output level by potential difference with SG. (When opened, produces$\simeq V_{SG}+1.0V$)
SG	17	O	[Signal ground] Outputs a reference potential of an analog signal. (When opened, produces$\simeq$2.5V)
V_{CC}	18	—	[V_{CC} supply for the analog section] +5V
V_{DD}	19	—	[V_{DD} supply for the digital section] +5V
$\overline{\text{ANSC}}$	20	I* *1	[Answer tone control input] The low level input enables answer tone generation during SQT is high level.
SQT	21	I*	[Squelch transmitter] The high level input squelches the carrier transmitting.
ALB	22	I*	[Analog loop-back test input] The high level input leads to connection of modulated output to demodulated input, so that enables the analog loop-back test. Both ALB and SQT are made high, the power-down mode is established.
O/$\overline{\text{A}}$	23	I*	[Originate or Answer mode selection input] Originate mode : High level Answer mode : Low level
RT	24	O	[Receive timing output] Outputs a receive timing signal.
RxD	25	O	[Receive data output] Outputs the PSK demodurated serial data. This produces high level continuously when $\overline{\text{PSD}}$ is high level or $\overline{\text{DLB}}$ is low level. Mark : High level Space : Low level
$\overline{\text{NSM}}$	26	O	[Non-scrambled mark detection output] Outputs low level when 64 or more continuous mark signals are detected in the input of the descrambler.
OSC1	27	I	[Oscillation input/output] Connects a 4.032MHz crystal oscillator and capacitors.
OSC2	28	O	

1 I has a built-in pull-up resistor.

■STC9492C SERIES

Name	Optional Selection (#8 pin)	Package
$\text{STC9492C}_{\text{ID}}$	$\overline{\text{DLB}}$	28-pin DIP
$\text{STC9492M}_{\text{ID}}$		28-pin SOP
$\text{STC9492C}_{\text{IE}}$	EXT	28-pin DIP
$\text{STC9492M}_{\text{IE}}$		28-pin SOP

■ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Ratings	Unit
Supply voltage		V_{CC}	7	V
		V_{DD}	7	V
Input voltage	Analog input	V_{IA}*1	$V_{EE}-0.3$ to $V_{CC}+0.3$	V
	Digital input	V_{ID}*2	$V_{SS}-0.3$ to $V_{DD}+0.3$	V
Power dissipation		P_D	500	mW
Storage temperature		T_{stg}	−65 to 150	℃
Soldering temperature and time		T_{sol}	260℃, 10s (at lead)	—

*1……TLA, CDA, RxA, MADJ
*2……OSC1, TxD, SQT, ALB, O/$\overline{\text{A}}$, $\overline{\text{ANSC}}$, $\overline{\text{SCBE}}$, $\overline{\text{HALF}}$, $\overline{\text{DLB}}$, B/$\overline{\text{C}}$, EXT

■RECOMMENDED OPERATING CONDITIONS

($f_{OSC}=4.032$MHz, $V_{SS}=V_{EE}=0$V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage for analog section	V_{CC}	—	4.75	5.0	5.25	V
Supply voltage for digital section	V_{DD}	—	4.75	5.0	5.25	V
Analog input voltage	V_{IA}	—	V_{EE}	—	V_{CC}	V
Digital input voltage	V_{ID}	—	V_{SS}	—	V_{DD}	V
Operating temperature	T_{opr}	—	−10	25	70	℃
Oscillating frequency tolerance	Δf_{OSC}	Crystal/External clock	−0.01	0	+0.01	%

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

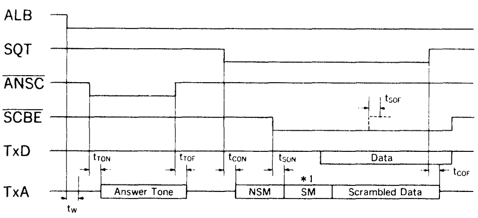
($V_{DD}=5.0$V, $V_{SS}=V_{EE}=0$V, Ta=25℃)

Parameter		Symbol	Conditions	Min	Typ	Max	Unit
Digital section operating current	Operating	I_{DDO}	SQT or ALB="L"	—	3	5	mA
	Power-down	I_{DDS}	SQT=ALB="H"	—	—	1	μA
High level input voltage		V_{IH}	*1	3.5	—	V_{DD}	V
Low level input voltage		V_{IL}		V_{SS}	—	1.5	V
High level input current		I_{IH}	*1	—	—	1	μA
Low level input current		I_{IL}		5	10	30	μA
High level output current		I_{OH}	$V_{OH}=4.5$V*2	—	3.5	—	mA
Low level output current		I_{OL}	$V_{OL}=0.5$V*2	—	3.5	—	mA
Analog section operating current	Operating	I_{CCO}	SQT or ALB="L"	—	20	30	mA
	Power-down	I_{CCS}	SQT=ALB="H"	—	—	1	μA
Output DC impedance		Z_{SG}	SG	—	70	150	Ω
		Z_{TxA}	TxA	—	150	250	Ω
Reference voltage generator output impedance		Z_{TLA}	$V_{TLA}-V_{SG}\geqq 1.0$V	20	—	500	kΩ
		Z_{CDA}	$V_{CDA}-V_{SG}\geqq 1.0$V	20	—	500	kΩ
Input DC impedance		Z_{RxA}	RxA	5	—	—	MΩ
		Z_{MADJ}	MADJ	5	—	—	MΩ

*1 Digital input terminal except for OSC1. (pull-up resistor is built-in)
*2 ST, $\overline{\text{LMON}}$, $\overline{\text{PSD}}$, $\overline{\text{ED}}$, RT, RxD, $\overline{\text{NSM}}$

●AC Electrical Characteristics

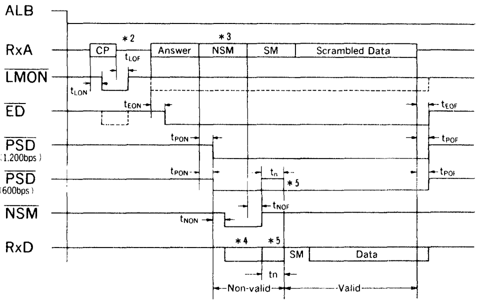
○Transmit



*1 The scramble start in Bell mode (B/$\overline{\text{C}}$="H") requires the training signal (voluntary serial data including "0") to TxD after $\overline{\text{SCBE}}$→"L".

NSM : Non Scrambled Mark
SM : Scrambled Mark

○Receive



*2 Call Progress Tone
*3 Non Scrambled Mark
*4 During $\overline{\text{NSM}}$="L" ; RxD→"H"(fixed) when B/$\overline{\text{C}}$="H"
RxD→"L"(fixed) when B/$\overline{\text{C}}$="L"
*5 RxD output or $\overline{\text{PSD}}$ output are invalid because the demodulator is capturing.

○Transmitter

(f_{OSC}=4.032MHz, $V_{DD}=V_{CC}$=5.0V, Ta=25°C)

Delay time	Trigger signal	Symbol	Min	Typ	Max	Unit
Power-on	ALB or SQT→"L"	t_W	—	50	100	ms
Answer tone transmit	SQT="H", $\overline{\text{ANSC}}$→"L"	t_{TON}	—	—	2	ms
Answer tone stop	SQT="H", $\overline{\text{ANSC}}$→"H"	t_{TOF}	—	—	2	ms
Carrier transmit	SQT→"L"	t_{CON}	—	—	2	ms
Carrier stop	$\overline{\text{ANSC}}$="H", SQT→"H"	t_{COF}	—	—	2	ms
Scrambler start	SQT="L", $\overline{\text{SCBE}}$→"L"	t_{SON}	—	—	70*6	ms
Scrambler stop	SQT="L", $\overline{\text{SCBE}}$→"H"	t_{SOF}	—	—	10	ms

*6 In case of CCITT mode, 1,200 bps

○Receiver

(f_{OSC}=4.032MHz, $V_{DD}=V_{CC}$=5.0V, Ta=25°C)

Delay time	Input signal	Symbol	Min	Typ	Max	Unit
Call progress tone detection time	Call progress tone	t_{LON}	—	—	150	ms
		t_{LOF}	—	—	150	ms
Carrier detection time	Signal within receive band	t_{EON}	—	—	20	ms
		t_{EOF}	—	40	70	ms
PSK energy detection time	Phase shifted signal (600 baud)	t_{PON}	—	200	300	ms
		t_{POF}	—	—	100	ms
Non-scrambled mark detection time	Non-scrambled mark	t_{NON}	—	—	60	ms
		t_{NOF}	—	—	10	ms
Settling time	Scrambled data	tn	—	—	600	ms

●Analog Characteristics

○Transmitter (V_{CC}=5.0V, Ta=25°C, TLA is opened)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Tone frequency	f_r	Bell Answer tone	2,205	2,225	2,245	Hz
		CCITT Answer tone	2,090	2,100	2,110	
		CCITT Guard tone	1,790	1,800	1,810	
Transmit level	P	Answer tone	−12.0	−10.5	−9.0	dBm
		PSK carrier	−13.5	−12.0	−10.5	
Unexpected transmit level	P_E	f=4 to 8kHz	—	—	P-20	dBm
		f=8 to 12kHz	—	—	P-40	
		f≧12kHz	—	—	P-60	

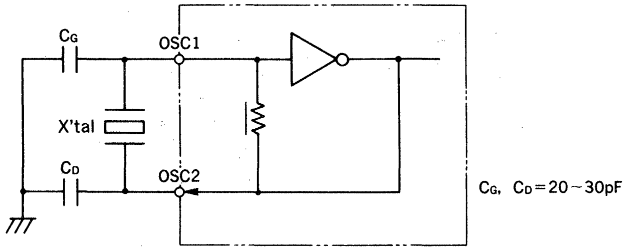
○Receiver (V_{CC}=5.0V, Ta=25°C, CDA is opened)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Allowable input range	DR	at RxA	−40	—	−5	dBm
Carrier detection level	L_{ON}	OFF→ON (On level)	−43	—	—	dBm
	L_{OFF}	ON→OFF (Off level)	—	—	−48	dBm
	L_H	Hysteresis width	1	2	—	dB
Call progress tone detection level	L_D	$V_{EE} \leqq V_{MADJ} \leqq V_{CC}$	—	—	−32	dBm
	L_{AR}	L_D(Max)−L_D(Min)	10	—	—	dB

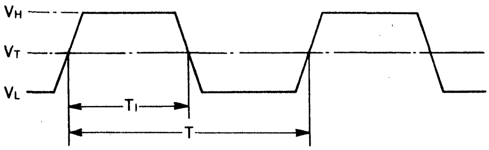
■FUNCTIONS

●Oscillating Circuit

○Crystal quartz oscillation



○External clock into OSC1



Parameter	Symbol	Condition	Tolerance
Amplitude	V_H	$\geqq V_{DD}-1.0V$	—
	V_L	$\leqq V_{SS}+1.0V$	—
Frequency	1/T	4.032MHz	±0.01%
Duty	T_1/T	50%	±15%

●Operation Mode

ALB	SQT	Mode
High level	Low level	Normal mode (transmission enable)
	High level	Transmission disable mode
Low level	Low level	Analog loop-back test mode
	High level	Power-down mode

○Power-down mode

During both ALB and SQT are high level, oscillation stops and operating current is to be below 2μA.

○Analog loop-back test mode

In the analog loop-back test mode, the functional test (including LSI) should be easily done, because transmission data into TxD are sent to the demodulator through the modulator automatically and appear from RxD again.

During this mode, transmit buffer so operates that test signal can be monitored, and, input signal into RxD is ignored by the demodulator but call progress tone can be detected.

○Transmission disable mode

In this mode, the transmitter stops it's operation but the receiver operates.

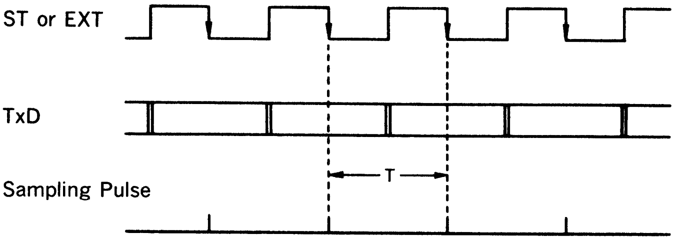
And the answer tone should be transmitted by $\overline{\text{ANSC}}$ being low level.

○Normal mode

Both the transmitter and the receiver become active, the PSK modulated signal which has a center frequency of 1,200Hz or 2,400Hz (depend on O/$\overline{\text{A}}$ input) can be transmitted, and a 1,800±10Hz guard tone can be transmitted when $\overline{\text{ANSC}}$="L" and CCITT answer mode are selected.

●Transmitter

○Relation between input data and transmit timing signal



1/T : Data transmission speed (1,200bps/600bps)

In case of using an external transmit timing (EXT), the frequency tolerance of EXT should be less than ±0.01% of data transmission speed.

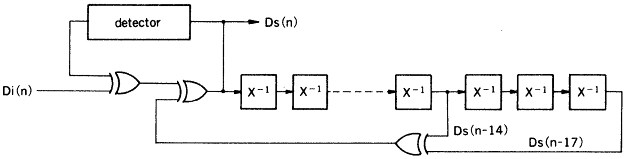
○ Scrambler

[Scrambler control]

Transmit data	$\overline{SCBE}$	Algorithm
Scrambled	Low level	$Ds(n)=Di(n)+Ds(n-14)+Ds(n-17)$
Non-scrambled	High level	$Ds(n)=Di(n)$

- $Di(n)$; Input data (TxD)
- $Ds(n-k)$; Scrambler output (k is output data of k times before)
- $+$; Logical addition (mod 2)

[Construction]



- x^{-1} ; 1 bit delay circuit
- detector ; In the CCITT mode (B/$\overline{C}$="L"), if it detects 64 or more continuous mark data in the output of the scrambler, this inverts the polarity of the following input data.
  In the Bell mode (B/$\overline{C}$="H"), the detector output becomes invalid, so that the training signal (voluntary serial data including "0") are required into TxD to start the scrambler.

○ Modulation

[Base-band modulation]

- 4-phase differential modulation

1,200bps	600bps	Phase shift (deg)
0 0	0	+ 90
0 1	—	+ 0
1 1	1	+270
1 0	—	+180

- Roll off characteristic ·········75% cosine roll off

[Transmit carrier frequency]

Originate mode····················1,200Hz ± 0.01%
Answer mode·····················2,400Hz ± 0.01%

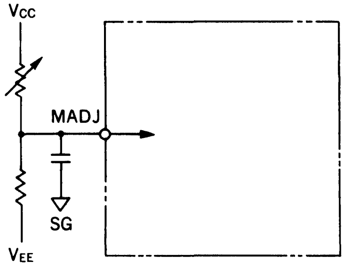
○ Tone Generator

Name	SQT	$\overline{ANSC}$	O/$\overline{A}$	B/$\overline{C}$	Frequency
Answer tone	"H"	"L"	—	"L"	2,100Hz ± 10Hz
				"H"	2,225Hz ± 20Hz
Guard tone	"L"	"H"	"L"	"L"	1,800Hz ± 10Hz

●Receiver

○Call progress tone detection

The definitions of the call progress tone are different in each country, so that an appropriate detection level can be adjusted by some external voltage through the MADJ terminal.



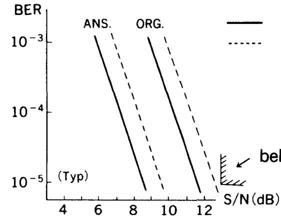
○Demodulation

[Demodulated carrier frequency]

Mode	O/$\overline{A}$	Carrier frequency	Tolerance
Originate	H	2,400Hz	±0.01%
Answer	L	1,200Hz	±0.01%

[Data reliability]

- Bit error rate (BER)



—— 1,200bps, CCITT mode (In case of Bell originate mode, S/N should be improved about 1dB because the guard tone is not transmitted.)

------ 600bps

⟨note⟩ Equivalent noise band width ; f =0.3 to 3.4kHz
Signal level ; S= −30dBm

below 1×10^{-5} at S/N=13dB

- Allowable range of the factor which makes the line characteristic worse

Factor	Symbol	Range	Unit
Frequency offset	Δf	± 7	Hz
Phase jitter	θj	±20	deg

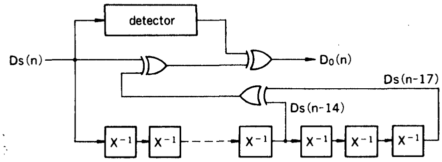
○Descrambler

[Algorithm]

Do(n) = Ds(n) + Ds(n − 14) + Ds(n − 17)

- Do(n) ; Output data (RxD)
- Ds(n − k) ; Descrambler input (k is input data of k times before)
- \+ ; Logical addition (mod 2)

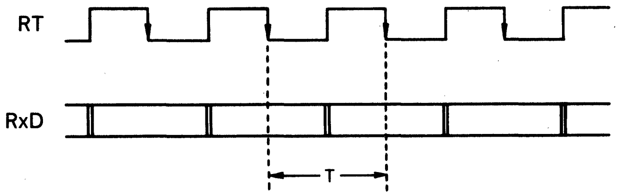
[Construction]



- x^{-1} : 1 bit delay circuit
- detector : In the CCITT mode (B/$\overline{C}$="L"), if it detects 64 or more continuous mark data in the input of the descrambler, this inverts the polarity of the following output data and outputs low level to $\overline{NSM}$.

  In the Bell mode (B/$\overline{C}$="H"), the detector output is invalid for the descrambler, but valid for the $\overline{NSM}$ output.

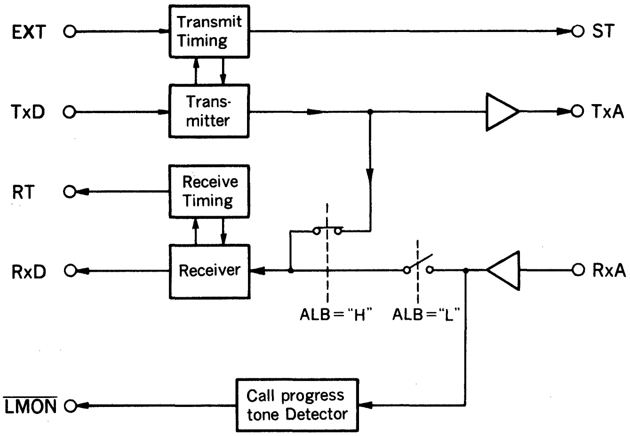
○ **Relation between output data (RxD) and receive timing output (RT)**



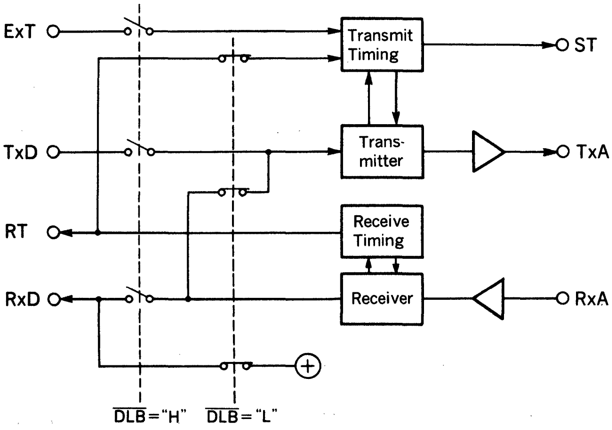
1/T : Data transmission speed (1,200bps/600bps)

■TEST FUNCTIONS

●Analog loop-back test

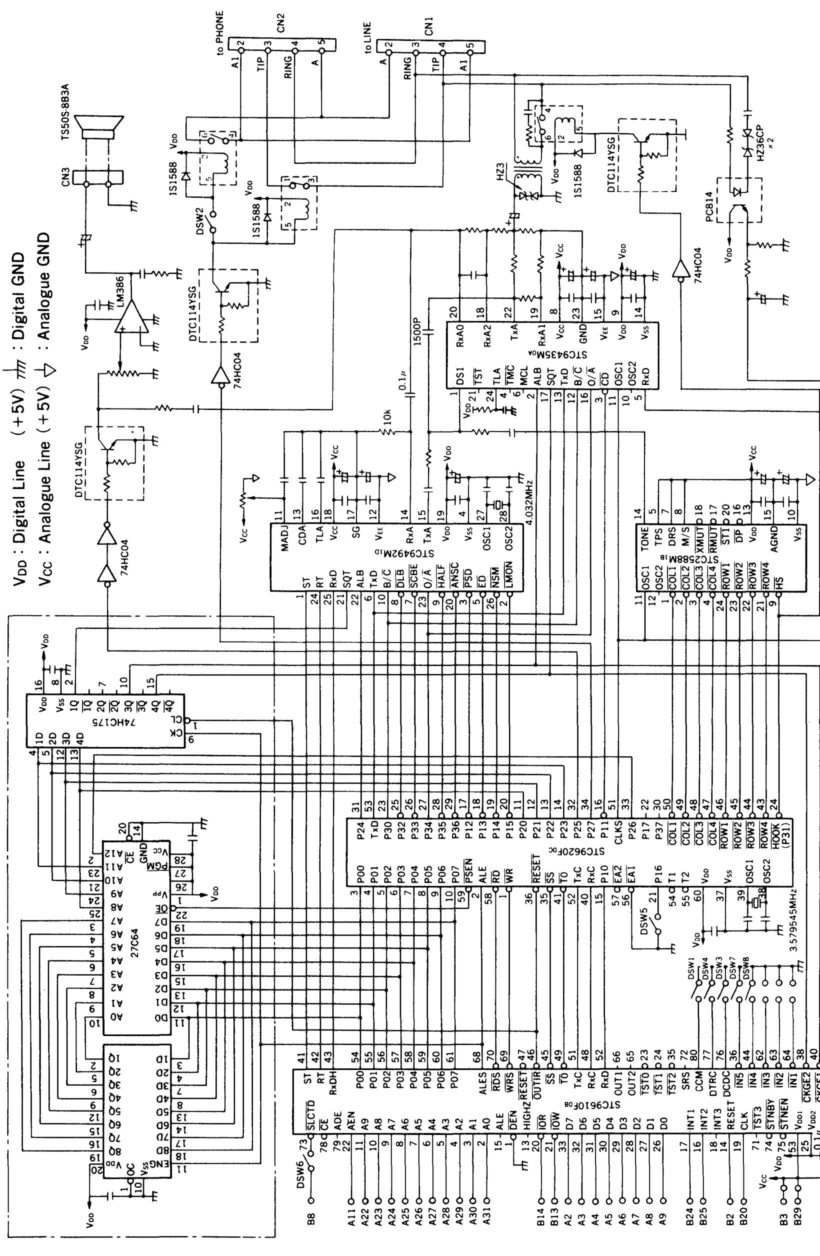


●Digital remote loop-back test



■EXAMPLE OF APPLICATIONS

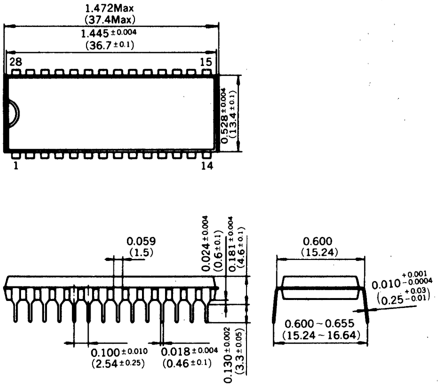
●Circuit for intelligent MODEM card



■PACKAGE DIMENSIONS

C28

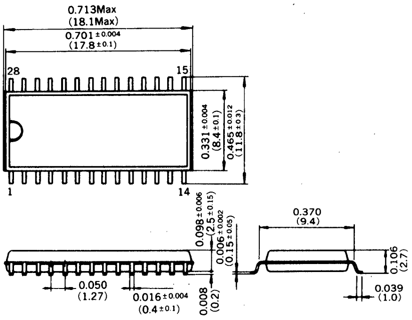
28-pin DIP



unit : inch
(mm)

M28-2

28-pin SOP



unit : inch
(mm)

STC9610F$_{0B}$

CMOS ASYNCHRONOUS COMMUNICATION INTERFACE

- **8250 A/B Function Compatible**
- **Abundant Addressing Modes**
- **300/110 bps Baud-rate Generator Incorporated**

■DESCRIPTION

The STC9610F$_{0B}$ is an interface LSI with the protocol controller and the 8086 group host CPU, and supports the serial data I/O function at the asynchronous communication, as an external data memory of the protocol controller.

The host CPU interface is function compatible with the asynchronous communication adaptor 8250A/B, and especially the STC9610F$_{0B}$ has all interface functions for the system-bus of the IBM® PC-XT/AT.

■FEATURES

- Host CPU interface …… Function compatible with the asynchronous communication adaptor 8250A/B.
  Address control register : 8 bits × 16
  Abundant addressing mode : Address decoding function
  Address data separating function
  Can be controlled by an external address decoder.
- Protocol controller interface ………………… Address control register : 8 bits × 8
- Built-in 300/110 bps baud-rate generator (Protocol controller clock = 3.579545MHz)
  Transmit clock : baud-rate × 1
  Receive clock : baud-rate × 8
- Built-in expansive input function for the protocol controller (5 inputs)
- Built-in stand-by control function for the protocol controller
- Single power supply ………………………… 5V
- Package ……………………………………… 80-pin QFP (plastic)

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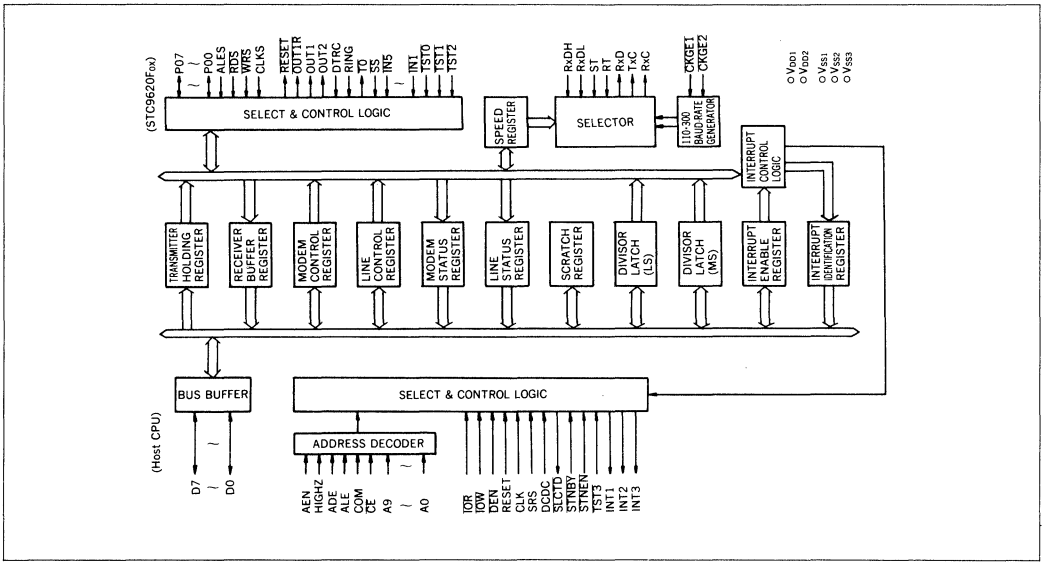
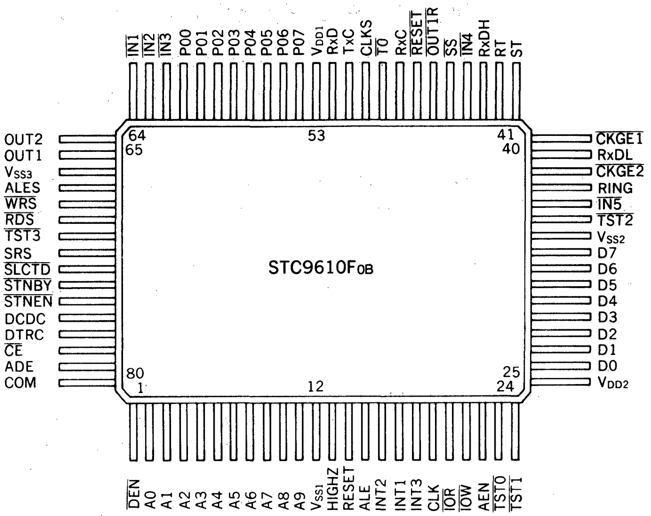
■BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

Pin name	Pin No.	I/O	Functions
$\overline{\text{DEN}}$	1	I	Inputs a signal which indicates that the bus data are valid, when the host system-bus is a multiplex bus. In this case, $\overline{\text{DEN}}$=L makes the $\overline{\text{IOR}}$ and $\overline{\text{IOW}}$ active. Should be fixed to low level, when not used.
A0—A9	2—11	I	Input the addresses of the host CPU.
V_{SS1}	12	—	V_{SS} power supply : 0V
V_{SS2}	34		
V_{SS3}	67		
HIGHZ	13	I*	Can be used when the decoded result of the high-ranking addresses (A10—A15) of the host CPU should be utilized. HIGHZ=L causes that the addresses are not decoded. Should be opened or fixed to high level, when not used.
RESET	14	I	Inputs the host reset signal. The high level input clears all registers (except for the Transmitter holding register, the Receiver buffer register and the Divisor latch register) and the control logic. And, it leads the following state ; (INT1, INT2)→high impedance (INT3, OUT1, OUT2)→low level
ALE	15	I*	Inputs the address latch timing signal ALE, when the host system-bus is a multiplex bus. Should be opened or fixed to high level, when not used.

Note ; I is a floating input so that it should always be given high level or low level.
I* has a built-in pull-up resistor.

Pin name	Pin No.	I/O	Functions
INT2	16	O	3 state output Outputs an interrupt signal which is enabled in the case of COM=H and OUT2=1, to the host CPU. (The OUT2 is a bit3 of the MODEM control register.) Outputs the high impedance state in the case of COM=L or OUT2=0. Connects to the IRQ3 pin when the host CPU is the IBM® PC.
INT1	17	O	3 state output Outputs an interrupt signal which is enabled in the case of COM=L and OUT2=1, to the host CPU. (The OUT2 is a bit3 of the MODEM control register.) Outputs the high impedance state in the case of COM=H or OUT2=0. Connects to the IRQ4 pin when the host CPU is the IBM® PC.
INT3	18	O	Outputs an interrupt signal to the host CPU. Should be used when the OUT2 is not utilized as an enable register for the interrupt line.
CLK	19	I	Inputs the host system clock.
$\overline{\text{IOR}}$	20	I	Inputs the host read signal.
$\overline{\text{IOW}}$	21	I	Inputs the host write signal.
AEN	22	I	Inputs a signal which indicates that the DMA controller is using the bus. AEN=H causes that the addresses from being decoded. Should be fixed to low level, when not used.
$\overline{\text{TST0}}$	23	I*	LSI test inputs. Should be opened normally.
$\overline{\text{TST1}}$	24		
$\overline{\text{TST2}}$	35		
$\overline{\text{TST3}}$	71		
V_{DD2}	25	—	V_{DD} power supply : +5V
V_{DD1}	53		
D0—D7	26—33	I/O	3 state I/O terminals Connect to the data-bus of the host CPU.
$\overline{\text{IN5}}$ $\overline{\text{IN4}}$ $\overline{\text{IN3}}$—$\overline{\text{IN1}}$	36 44 62—64	I*	Can be used as the expansive input ports for the protocol controller.
RING	37	I	Inputs the ringing detection signal. ringing : high level not ringing : low level
$\overline{\text{CKGE2}}$	38	I	Enable the built-in baud-rate generator. The baud-rate generator is halted in the case of $\overline{\text{CKGE1}}$=$\overline{\text{CKGE2}}$=H, and operates when either of these pins is low level.
$\overline{\text{CKGE1}}$	40		
RxDL	39	I	Inputs the receive data of a low speed MODEM. Outputs the input signal into the RxDL to the RxD at the low speed mode.*1
ST	41	I	Inputs the transmit timing clock of a synchronous MODEM. Outputs the input signal into the ST to the TxC at the high speed mode.*1
RT	42	I	Inputs the receive timing clock of a synchronous MODEM. Outputs the input signal into the RT to the RxC at the high speed mode.*1
RxDH	43	I	Inputs the receive data of a high speed MODEM. Outputs the input signal into the RxDH to the RxD at the high speed mode.*1

Note ; I is a floating input so that it should always be given high level or low level.
I* has a built-in pull-up resistor.
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*1…Control register 2 (CR2) bit7=1 makes the high speed mode, and the bit7=0 makes low speed mode.

Pin name	Pin No.	I/O	Functions
$\overline{\text{SS}}$	45	I	These 4 terminals are used to construct a system which lets the protocol controller have the stand-by mode. When this function is not utilized, the $\overline{\text{SS}}$ should be fixed to low level or high level and $\overline{\text{T0}}$, $\overline{\text{STNBY}}$ and $\overline{\text{STNEN}}$ should be opened. $\overline{\text{STNBY}}$; Inputs the stand-by control signal. $\overline{\text{STNEN}}$; Inputs the clock signal for writing into the $\overline{\text{STNBY}}$ register. The value into the $\overline{\text{STNBY}}$ is written into the bit0 of the Control register 3 (CR3), at the rising edge of the $\overline{\text{STNEN}}$. normal operation : bit0 = 1 stand-by mode : bit0 = 0 $\overline{\text{T0}}$; Outputs the interrupt signal for cancelling the stand-by mode. Outputs low level at the time when bit0 of CR3 changes from 0 to 1 . Returns to high level when the protocol controller reads the Control register 1 (CR1) after this state. $\overline{\text{SS}}$; Inputs the inhibit signal for cancelling the stand-by mode. When the $\overline{\text{SS}}$ is low level, it does not output low level to the $\overline{\text{T0}}$, even though the bit0 of CR3 changes from 0 to 1.
$\overline{\text{T0}}$	49	O	
$\overline{\text{STNBY}}$	74	I*	
$\overline{\text{STNEN}}$	75	I*	
$\overline{\text{OUT1R}}$	46	O	Outputs a reset signal to the protocol controller. Outputs low level in the case of RESET = H or OUT1 = 1. (The OUT1 is the bit2 of MODEM control register.) Should be used when the software-reset is utilized together with the hardware-reset.
$\overline{\text{RESET}}$	47	O	Outputs a reset signal to the protocol controller. Outputs an inverted level of the RESET input. Should be used when only the hardware-reset is utilized.
RxC	48	O	Outputs the RT input at the high speed mode. Outputs the receive timing clock generated from the built-in baud-rate generator at the low speed mode.*1
CLKS	50	I	Inputs the protocol controller clock. Should be input a 3.579545MHz clock when the built-in baud-rate generator is utilized.
TxC	51	O	Outputs the ST input at the high speed mode.*1 Outputs the transmit timing clock generated from the built-in baud-rate generator at the low speed mode.*1
RxD	52	O	Outputs the RxDH input at the high speed mode.*1 Outputs the RxDL input at the low speed mode.*1
P07—P00	54—61	I/O	Connects the address-data bus of protocol controller.
OUT2	65	O	Outputs the value of the OUT2 (bit3 of the MODEM control register).
OUT1	66	O	Outputs the value of the OUT1 (bit2 of the MODEM control register).
ALES	68	I	Inputs the address latch timing signal of the protocol controller.
$\overline{\text{WRS}}$	69	I	Inputs the write signal of the protocol controller.
$\overline{\text{RDS}}$	70	I	Inputs the read signal of the protocol controller.
SRS	72	I*	Selects the register of address 7(A2 = A1 = A0 = 1) controlled by the host CPU to be a Scratch register or a Speed indicator register. Scratch register : high level Speed indicator : low level
$\overline{\text{SLCTD}}$	73	O	Becomes necessary when the system (includes this STC9610F_{0A}) is used into the half-slot of the IBM® PC-XT. Outputs the $\overline{\text{IOR}}$ input according that the host CPU reads the register.

Note ; I is a floating input so that it should always be given high level or low level.
I* has a built-in pull-up resistor.
*1···Control register 2(CR2) bit7 = 1 makes high speed mode and the bit7 = 0 makes low speed mode.
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Pin name	Pin No.	I/O	Functions
DCDC	76	I*	Controls the bit7 of MODEM status register read by the host CPU. The bit7 is a data carrier detection (DCD), and is utilized to inform that the protocol controller is detecting the receive carrier, to the host CPU. At DCDC=L ; The bit7 outputs the DCD value set by the protocol controller. At DCDC=H ; The bit7 outputs always 1 regardless of the value set by the protocol controller.
DTRC	77	I*	Controls the bit6 of Control register 3 (CR3) read by the protocol controller. The bit6 is a data terminal ready (DTR), and is utilized to inform that the host CPU is in the transmit enable state to the protocol controller. At DTRC=L ; The bit6 outputs the DTR value set by the host CPU. At DTRC=H ; The bit6 outputs always 1 regardless of the value set by the host CPU.
$\overline{\mathrm{CE}}$	78	I*	Inputs the decoded result when the external address decoder is utilized. (Low active) In this case, the host CPU can utilize the register designated by A2, A1 and A0 during $\overline{\mathrm{CE}}$=L.
ADE	79	I*	Inputs an enable signal for the internal address decoder. Should be opened or fixed to high level when the internal address decoder is utilized. When the internal address decoder is not utilized, the ADE should be low level and the A9—A3 should be 1 or 0.
COM	80	I*	Inputs a signal to designate the decoded address of address decoder, and to select the terminal for the interruption output. At COM=L ; Decoded address=3F8—3FF (H) Interruption output=INT1 (The INT2 becomes high impedance.) At COM=H ; Decoded address=2F8—2FF (H) Interruption output=INT2 (The INT1 becomes high impedance.)

Note ; I* has a built-in pull-up resistor.

■ABSOLUTE MAXIMUM RATINGS

($V_{SS1}=V_{SS2}=V_{SS3}=0V$)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}*1	-0.3 to 7.0	V
Input voltage	V_I	-0.3 to $V_{DD}+0.3$*1	V
Output voltage	V_O	-0.3 to $V_{DD}+0.3$*1	V
Output current	I_O	±10*2	mA
Power dissipation	P_D	100	mW
Power supply current	I_{DD}/I_{SS}	±40*2	mA
Storage temperature	T_{stg}	-65 to 150	℃
Soldering temperature and time	T_{sol}	260℃, 10s (at lead)	—

*1 $V_{DD}=V_{DD1}$ or V_{DD2}
*2 The sign + or − shows the current flow direction.
(+…inflow direction, −…outflow direction)

■RECOMMENDED OPERATING CONDITIONS

($V_{SS1}=V_{SS2}=V_{SS3}=0V$)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
Input voltage	V_I		V_{SS}*1	—	V_{DD}*2	V
Operating temperature	Ta		0	—	70	℃

*1 $V_{SS}=V_{SS1}$, V_{SS2} or V_{SS3}
*2 $V_{DD}=V_{DD1}$ or V_{DD2}

■ELECTRICAL CHARACTERISTICS

●DC Characteristics

($V_{DD}=V_{DD1}$ or V_{DD2}, $V_{SS}=V_{SS1}$, V_{SS2} or $V_{SS3}=0V$, Ta=0 to 70℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Standby supply current	I_{DDS}	$V_I=V_{DD}$ or V_{SS}, $I_{OH}=I_{OL}=0$	—	—	10	μA
Input leakage current	I_{LI}	$V_{DD}=5.5V$, $V_{IH}=V_{DD}$, $V_{IL}=V_{SS}$*1	−1	0	1	μA
High level input voltage	V_{IH1}	$V_{DD}=5.5V$*2	2.2	—	—	V
	V_{IH2}	$V_{DD}=5.5V$, $\overline{SS}$	3.5	—	—	
Low level input voltage	V_{IL1}	$V_{DD}=4.5V$*2	—	—	0.6	V
	V_{IL2}	$V_{DD}=4.5V$, $\overline{SS}$	—	—	1.0	
High level trigger voltage	V_{T+}	$V_{DD}=5.5V$, RESET, RING	—	—	4.0	V
Low level trigger voltage	V_{T-}	$V_{DD}=4.5V$, RESET, RING	0.8	—	—	V
Pull-up resistor	R_{PL}	$V_{DD}=5.0V$*3	100	—	900	kΩ
High level output voltage	V_{OH}	$V_{DD}=4.5V$, $I_{OH}=-2mA$*4	$V_{DD}-0.4$	—	—	V
Low level output voltage	V_{OL}	$V_{DD}=4.5V$, $I_{OL}=6mA$*4	—	—	0.4	V
Off-state leak current	I_{OZ}	$V_{DD}=5.5V$, $V_{OH}=V_{DD}$, $V_{OL}=V_{SS}$*5	−1	0	1	μA

*1 All input terminals which have no pull-up resistor.
[$\overline{DEN}$, A0-A9, RESET, CLK, $\overline{IOR}$, $\overline{IOW}$, AEN, (D0-D7), RING, $\overline{CKGE2}$, RxDL, $\overline{CKGE1}$, ST, RT, RxDH, $\overline{SS}$, CLKS, (P00-P07), ALES, $\overline{WRS}$, $\overline{RDS}$]
*2 All input terminals except for the schmidt inputs (RESET, RING) and the $\overline{SS}$.
*3 Input terminals with the pull-up resistors.
[HIGHZ, ALE, $\overline{TST0}$, $\overline{TST1}$, $\overline{TST2}$, $\overline{IN5}$, $\overline{IN4}$, $\overline{IN3}$, $\overline{IN2}$, $\overline{IN1}$, $\overline{TST3}$, SRS, $\overline{STNBY}$, $\overline{STNEN}$, DCDC, DTRC, $\overline{CE}$, ADE, COM]
*4 All output terminals including the 3 state output.
*5 3 state output terminals. [INT2, INT1, (D0-D7), (P00-P07)]

●AC Characteristics and Timing Chart

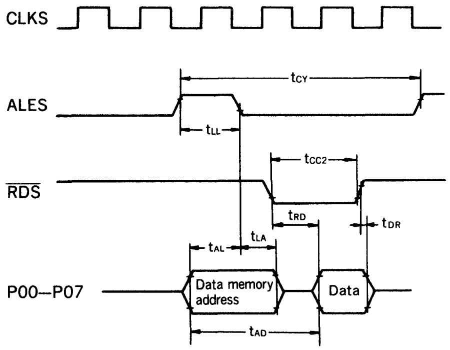
○Interface With The Protocol Controller

(1) AC Characteristics (${V_{DD}}=5V\pm10\%$, $V_{SS}=0V$, $f_{CLKS}=3.579545MHz$, $Ta=0$ to 70°C)

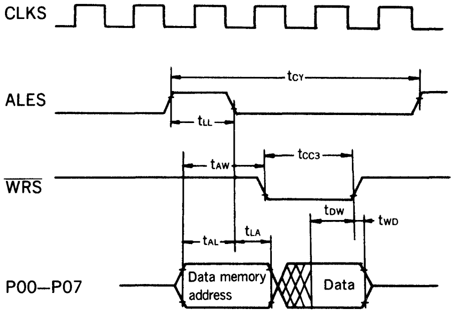
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Cycle time	t_{CY}		—	1.117	—	μs
Pulse width of ALES	t_{LL}		200	—	—	ns
Address set-up time	t_{AL}		100	—	—	ns
Address hold time	t_{LA}		50	—	—	ns
Pulse width of $\overline{RDS}$	t_{CC2}		300	—	—	ns
Pulse width of $\overline{WRS}$	t_{CC3}		300	—	—	ns
Delay time of data input	t_{RD}		—	—	150	ns
Read data hold time	t_{DR}		0	—	100	ns
Write data set-up time	t_{DW}		250	—	—	ns
Write data hold time	t_{WD}		5	—	—	ns
$\overline{WRS}$ delay time	t_{AW}		200	—	—	ns
Delay time of data input	t_{AD}		—	—	450	ns

(2) Timing Chart

○Data output cycle to the protocol controller



○Data input cycle from the protocol controller



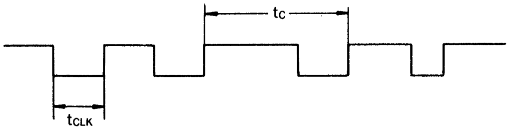
○Interface With The Host CPU

(1) AC Characteristics ($V_{SS1}=V_{SS2}=V_{SS3}=0V$, $V_{DD1}=V_{DD2}=5V\pm10\%$, $Ta=0$ to $70°C$)

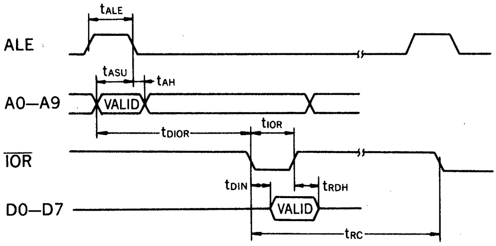
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Pulse width of ALE	t_{ALE}		90	—	—	ns
Address set-up time	t_{ASU}		90	—	—	ns
Address hold time	t_{AH}		0	—	—	ns
Delay time of $\overline{IOR}$	t_{DIOR}		80	—	—	ns
Pulse width of $\overline{IOR}$	t_{IOR}		175	—	350	ns
Delay time of data-in	t_{DIN}		—	—	175	ns
Read data hold time	t_{RDH}		100	—	—	ns
Read cycle time	t_{RC}		755	—	—	ns
Delay time of $\overline{IOW}$	t_{DIOW}		80	—	—	ns
Pulse width of $\overline{IOW}$	t_{IOW}		175	—	350	ns
Write data set-up time	t_{WSU}		90	—	—	ns
Write data hold time	t_{WDH}		60	—	—	ns
Write cycle time	t_{WC}		755	—	—	ns
Pulse width of CLK	t_{CLK}		20	—	350	ns
CLK period	t_C		—	—	400	ns

(2) Timing Chart

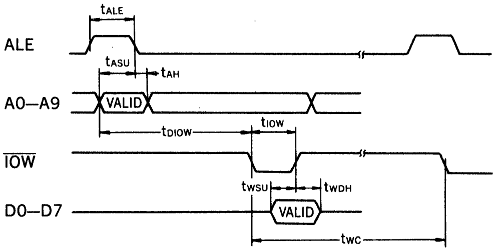
○Clock input into the CLK



○Read cycle



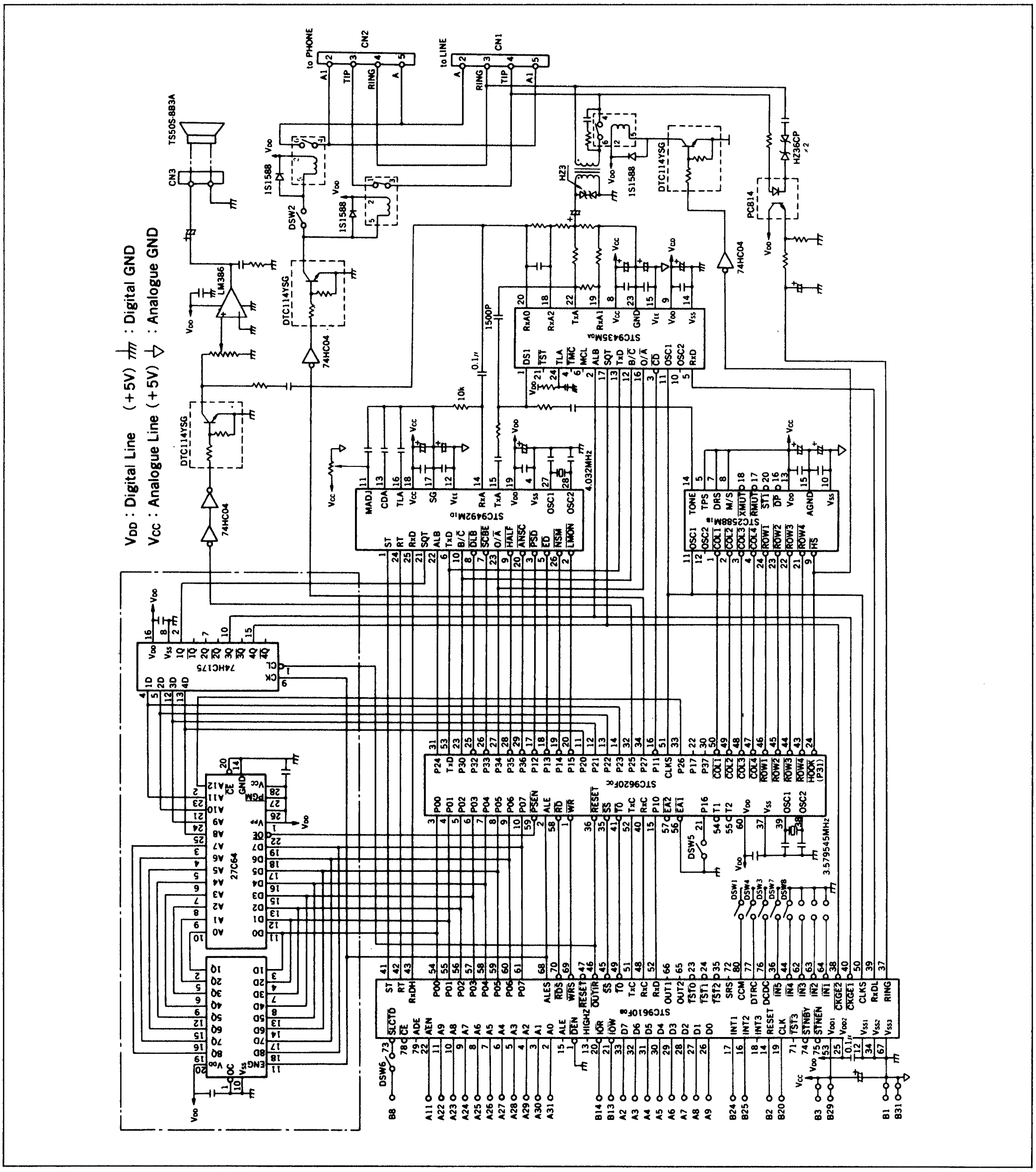
○Write cycle



■EXAMPLE OF APPLICATIONS

This schema shows an example of the system-bus interface type intelligent MODEM, combining the STC 9610F$_{\mathrm{OB}}$ with the following LSIs ;

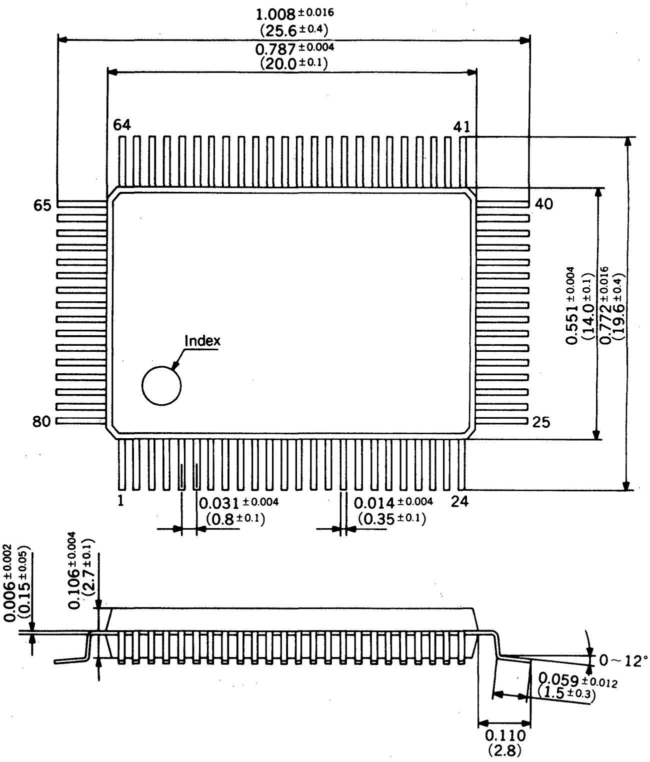
Protocol controller ································STC9620F Series
High speed MODEM (1,200bps PSK) ············STC9492M Series
Low speed MODEM (300bps FSK)···············STC9435M Series
DTMF dialer···STC2588M Series



■PACKAGE DIMENSIONS

F80-5

80-pin QFP



unit : inch
(mm)

PF263-03

STC9620F Series

CMOS COMMUNICATION PROTOCOL CONTROLLER

- **Compatible with "AT Command" System**
- **Ports for Interface with Modem and Host CPU**
- **On-chip Data Parallel/Serial Conversion Circuit**

■DESCRIPTION

The STC9620F Series asynchronous Communication Protocol Controller runs on a host CPU via an external data memory (registers) and controls a modem LSI or dialer to provide an intelligent communication function. The protocol controller is stored in the program memory of the STC9620F, and can be changed as required to support a specific communication protocol.
In order for the user to understand the functions of the STC9620F Series more realistically, this document focuses on the STC9620F$_{0B}$ that provides programmed intelligent functions compatible with the "AT Command" system.

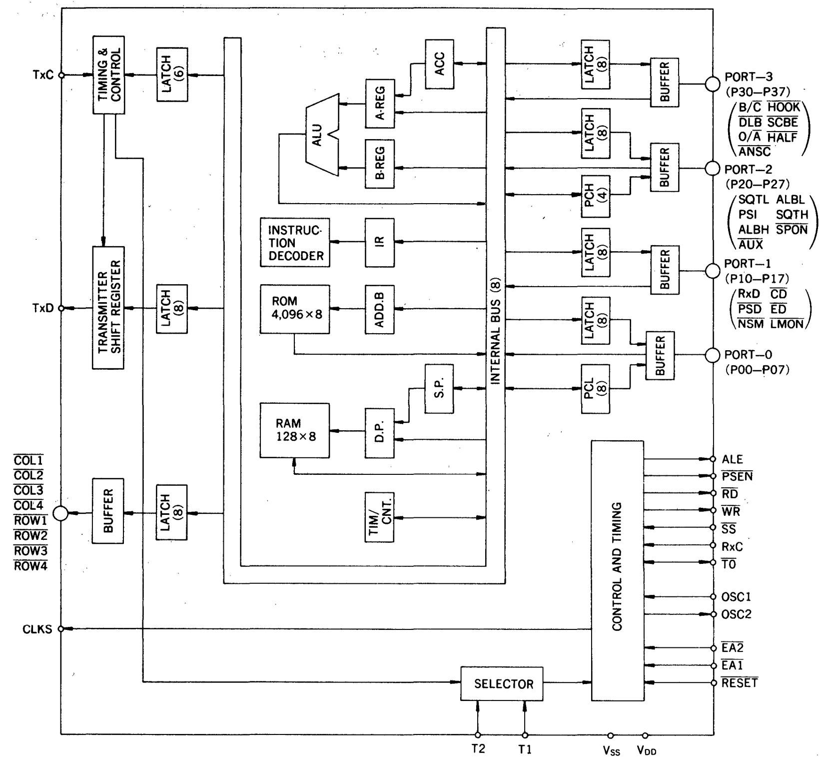
The STC9620F$_{0B}$ contains a parallel/serial data conversion circuit. The STC9620F$_{0B}$ enables the designer to easily configure a system bus interface based intelligent modem when combined with :

1,200 bps PSK full-duplex modem LSI	STC9492C$_{1D}$ (STC9492M$_{1D}$)
300 bps FSK full-duplex modem LSI	STC9424C$_{0A}$ (STC9424M$_{0A}$)
DTMF dialer	STC2588C$_{1B}$ (STC2588M$_{1B}$)
System bus interface LSI (external data memory)	STC9610F$_{0A}$

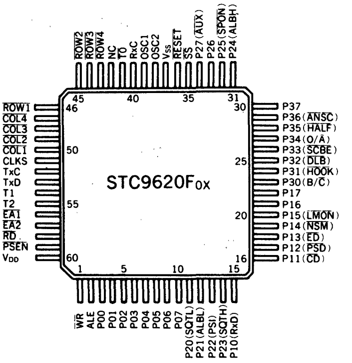
■FEATURES

- Compatible with "AT Command" system
- Can be used with Bell 212A/103 or CCITT V.22/(V.21) protocol (V.21 optional)
- On-chip asynchronous (start-stop synchronous) communication parallel/serial data conversion
- Interface with host CPU ························Programmable registers
  External data memory : 8 × 8 bits
- Modem control interface ·······················Function assignment I/O ports
  Data : Format : Asynchronous serial (Start-stop synchronous)
  Length : 7 or 8 bits
  Parity : None, even, odd, mark, space
  Stop bit length : 1 or 2 bits
  Break signal : Generation/detection function
- Power supply ···································Single 5V
- Package···60-pin QFP (plastic)

■BLOCK DIAGRAM



■PIN CONFIGURATION



( ) : STC9620F0C

PIN DESCRIPTION

Pin name	Pin No.	I/O	Functions
$\overline{\text{WR}}$	1	O^{*1}	Provides a timing signal for writing data to external data memory.
ALE	2	O^{*1}	The address of external data memory or external program memory is latched at the falling edge of the output provided at this pin.
P00—P07	3—10	I/O^{*2}	I/O ports for external data memory or external program memory. Each of these pins provides the address of external data memory synchronously with the ALE signal, then reads or writes data synchronously with the $\overline{\text{RD}}$ or $\overline{\text{WR}}$ signal. Also, it provides the low-order 8 bits of the address of external program memory synchronously with the ALE signal, then fetches the addressed instruction synchronously with the $\overline{\text{PSEN}}$ signal.
P20—P23 P24—P27	11—14 31—34	O$^{*2}_{*3}$	Output only ports used to control the modem. The P20—P23 provide the high-order 4 bits of the address of external program memory when it is connected.
[SQTL]	[11]		[Controls the squelch transmitter (SQT) pin of STC9430 Series.]
[ALBL]	[12]		[Controls the analog loopback test (ALB) pin of STC9430C Series.]
[PSI]	[13]		[Controls the power save control (PSI) pin of STC9430C Series.]
[SQTH]	[14]		[Controls the squelch transmitter (SQT) pin of STC9492C$_{\text{ID}}$.]
[ALBH]	[31]		[Controls the analog loopback test (ALB) pin of STC9492C$_{\text{ID}}$.]
[$\overline{\text{SPON}}$]	[32]		[Turns on/off the speaker to monitor DTMF tone or send/receive signal. Speaker ON···low level Speaker OFF···high level]
	[33]		[For STC9620F$_{\text{0B}}$, this pin must be opened as the device does not use P26.]
[$\overline{\text{AUX}}$]	[34]		[Provides an output for driving the relay which determines whether the modem or handset is to be connected to the telephone line. Modem connected···low level Handset connected···high level]
P10—P17	15—22	I^{*2}	Input only ports to control the modem.
[RxD]	[15]		[STC9430C Series or STC9492C$_{\text{ID}}$ receive data (RxD) input]
[$\overline{\text{CD}}$]	[16]		[STC9430C Series carrier detection signal ($\overline{\text{CD}}$) input]
[$\overline{\text{PSD}}$]	[17]		[STC9492C$_{\text{ID}}$ PSK energy detection signal ($\overline{\text{PSD}}$) input]
[$\overline{\text{ED}}$]	[18]		[STC9492C$_{\text{ID}}$ carrier detection signal ($\overline{\text{ED}}$) input]
[$\overline{\text{NSM}}$]	[19]		[STC9492C$_{\text{ID}}$ non-scramble mark detection signal ($\overline{\text{NSM}}$) input]
[$\overline{\text{LMON}}$]	[20]		[STC9492C$_{\text{ID}}$ call progress tone detection signal ($\overline{\text{LMON}}$) input]
	[21] [22]		[For STC9620F$_{\text{0B}}$, these pins must be opened as the device does not use P16/P17.]
P30—P37	23—30	O^{*2}	Output only ports for modem control.
[B/$\overline{\text{C}}$]	[23]		[Controls the Bell/CCITT (B/$\overline{\text{C}}$) pin of STC9492C$_{\text{ID}}$.]
[$\overline{\text{HOOK}}$]	[24]		[Controls the hook switch ($\overline{\text{HS}}$) pin of STC2588C$_{\text{IB}}$. Also drives the relay which is used to select on-hook or off-hook for the telephone circuit. Off-hook···low level On-hook···high level]
[$\overline{\text{DLB}}$]	[25]		[Controls the digital remote loopback test ($\overline{\text{DLB}}$) pin of STC9492C$_{\text{ID}}$.]
[$\overline{\text{SCBE}}$]	[26]		[Controls the scramble control ($\overline{\text{SCBE}}$) pin of STC9492C$_{\text{ID}}$.]
[O/$\overline{\text{A}}$]	[27]		[Controls the originate/answer mode select (O/$\overline{\text{A}}$) pin of STC9430C Series or STC9492C$_{\text{ID}}$.]
[$\overline{\text{HALF}}$]	[28]		[Controls the 1,200/600 bps data transfer speed select ($\overline{\text{HALF}}$) pin of STC9492C$_{\text{ID}}$.]
[$\overline{\text{ANSC}}$]	[29]		[Controls the answer tone send control ($\overline{\text{ANSC}}$) pin of STC9492C$_{\text{ID}}$.]
	[30]		[For STC9620F$_{\text{0B}}$, this pin must be opened as the device does not use P37.]
$\overline{\text{SS}}$	35	I	This signal is used to execute one instruction after another. The pin contains a pull-up resistor (about 100k-ohms), and pulled down (about 10k-ohms) when the device is in stop mode. [For STC9620F$_{\text{0B}}$, the $\overline{\text{SS}}$ pin must be opened as the device does not use it.]
$\overline{\text{RESET}}$	36	I	Resets the internal CPU into stand-by mode. (A pull-up resistor is incorporated.) Stand-by mode···low level Normal run mode···high level In stand-by mode, the set-up of each function is as follows: • Program counter set to "0" • Pin $\overline{\text{T0}}$ set to entry mode • Stack pointer set to "0" • External interrupts disabled • Program memory area set to addresses 0 through 2047 • Internal interrupts disabled • Pin TxD set to "1" • Ports P0—P3 set to entry mode • Timer/counter off

Remarks: The descriptions enclosed in [ ] give functions of the STC9620F$_{\text{0B}}$.

<table>
<tr><th>Pin name</th><th>Pin No.</th><th>I/O</th><th>Functions</th></tr>
<tr><td>V$_{SS}$</td><td>37</td><td>—</td><td>Power supply, 0V</td></tr>
<tr><td>OSC2</td><td>38</td><td>O</td><td rowspan="2">A crystal oscillator (3.579545MHz) is connected between the two pins and capacitors (C_G, C_D) between each of the pins and the power supply pin to make reference signal sources.</td></tr>
<tr><td>OSC1</td><td>39</td><td>I</td></tr>
<tr><td>RxC</td><td>40</td><td>I</td><td>Receive clock is entered at this pin. (A pull-up resistor is incorporated.)
Data is read from P10 [RxD] synchronously with the falling edge of the receive clock entered.</td></tr>
<tr><td>$\overline{\text{T0}}$</td><td>41</td><td>I</td><td>This pin receives the stand-by clear signal. (A pull-up resistor is incorporated.)
If at least 2 cycles of low level are applied to this pin with an external interrupt enabled, an interrupt occurs to clear the stand-by mode.
[For STC9620F$_{0B}$, the $\overline{\text{T0}}$ pin must be opened as the device does not use it.]</td></tr>
<tr><td>NC</td><td>42</td><td>—</td><td>As this pin is used for special operation verification, it must be held open.</td></tr>
<tr><td>$\overline{\text{ROW4}}$—$\overline{\text{ROW1}}$</td><td>43—46</td><td rowspan="2">O</td><td rowspan="2">Controls key entry for the DTMF dialer.
A combination of these outputs enables access to keys 0—9, ∗, and #.
[Controls the STC2588C$_{1B}$ key input ($\overline{\text{ROW4}}$—$\overline{\text{ROW1}}$, $\overline{\text{COL4}}$—$\overline{\text{COL1}}$) pins.]</td></tr>
<tr><td>$\overline{\text{COL4}}$—$\overline{\text{COL1}}$</td><td>47—50</td></tr>
<tr><td>CLKS</td><td>51</td><td>O</td><td>System clock output.
In normal run mode, a system clock of 3.579545MHz (the oscillation circuit frequency) is output via the buffer.
[The system clock is supplied as the reference signal source for STC9424C$_{0A}$, STC2588C$_{1B}$ or STC9610F$_{0A}$.]</td></tr>
<tr><td>TxC</td><td>52</td><td>I</td><td>Transmit clock input.
The TxD pin provides transmit data which becomes stable at the falling edge of the transmit clock entered to the TxC pin.</td></tr>
<tr><td>TxD</td><td>53</td><td>O</td><td>Transmit data output.
Transmit data written into the external data memory according to the format information stored by the host CPU is supplied in serial data form at the baud rate of the transmit clock entered to the TxC pin.
[Transmit data is supplied to the STC9430C Series or STC9492C$_{1D}$ transmit data input (TxD) pin.]</td></tr>
<tr><td>T1</td><td>54</td><td>I</td><td>Interrupt control signal input. (A pull-up resistor is incorporated.)
When high level is applied to this pin, internal interrupt mode results and the input to pin T2 is nullified.
For low level, external interrupt mode results and an interrupt signal entered to pin T2 becomes valid.
[For STC9620F$_{0B}$, the T1 pin must be opened as the device does not use it.]</td></tr>
<tr><td>T2</td><td>55</td><td>I</td><td>External interrupt signal input. (A pull-up resistor is incorporated.)
In external interrupt mode, an external interrupt is enabled at the falling edge of the input to pin T2.
[For STC9620F$_{0B}$, the T2 pin must be opened as the device does not use it.]</td></tr>
<tr><td>$\overline{\text{EA1}}$</td><td>56</td><td>I</td><td rowspan="2">A combination of these two pin inputs determines control mode.
(Pull-up resistors are incorporated.)
<table>
<tr><th>$\overline{\text{EA2}}$</th><th>$\overline{\text{EA1}}$</th><th>Control mode</th></tr>
<tr><td>H</td><td>H</td><td>Normal run mode</td></tr>
<tr><td>H</td><td>L</td><td>External program memory mode</td></tr>
<tr><td>L</td><td>H</td><td>Internal program memory data read mode</td></tr>
<tr><td>L</td><td>L</td><td>Internal program memory addressing mode</td></tr>
</table></td></tr>
<tr><td>$\overline{\text{EA2}}$</td><td>57</td><td>I</td></tr>
<tr><td>$\overline{\text{RD}}$</td><td>58</td><td>O</td><td>Provides a timing signal at which data is read from external data memory.</td></tr>
<tr><td>$\overline{\text{PSEN}}$</td><td>59</td><td>O</td><td>Provides a timing signal at which an instruction is taken from external program memory.</td></tr>
<tr><td>V$_{DD}$</td><td>60</td><td>—</td><td>Power supply, +5V</td></tr>
</table>

Remarks: The descriptions enclosed in [ ] give functions of the STC9620F$_{0B}$.

Notes ∗1 Each control signal holds high level when the device is in the stand-by mode or stop mode, or when the program halts in a single step mode.

∗2 In the stand-by mode (system reset), all of P00—P07, P10—P17, P20—P27 and P30—P37 work as input ports.

∗3 With external program memory used, no data can be derived from P20—P23.

ABSOLUTE MAXIMUM RATINGS

($V_{SS}=0V$)

Parameter	Symbol	Ratings	Unit
Power supply voltage	V_{DD}	-0.3 to 7.0	V
Input voltage	V_I	-0.3 to $V_{DD}+0.3$	V
Output voltage	V_O	-0.3 to $V_{DD}+0.3$	V
Power Dissipation	P_D	0.5	W
Operating temperature	T_{opr}	-10 to 70	℃
Storage temperature	T_{stg}	-65 to 150	℃
Soldering temperature and time	T_{sol}	260℃, 10s (at lead)	—

RECOMMENDED OPERATING CONDITIONS

($V_{SS}=0V$, $f_{OSC}=3.579545MHz$, $Ta=-10$ to 70℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating voltage	V_{DD}		4.5	5	5.5	V
Operating frequency	f_{OSC}	$V_{DD}=5V\pm10\%$	50	—	4,000	kHz

ELECTRICAL CHARACTERISTICS

DC Characteristics

($V_{DD}=5V\pm10\%$, $V_{SS}=0V$, $f_{OSC}=3.579545MHz$, $Ta=-10$ to 70℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Low level input voltage	V_{IL}		0	—	0.8	V
High level input voltage	V_{IH1}	Except for $\overline{RESET}$, $\overline{SS}$, OSC1	2.0	—	V_{DD}	V
	V_{IH2}	$\overline{RESET}$, $\overline{SS}$, OSC1	$V_{DD}-1$	—	V_{DD}	V
Low level output voltage	V_{OL}	$I_{OL}=2.0mA$	—	—	0.45	V
High level output voltage	V_{OH}	$I_{OH}=-1.0mA$	2.4	—	—	V
Input current	I_{ILP1}	$V_{ILP1}=V_{SS}$, Input terminal with pull-up	-250	-100	-30	μA
	I_{ILL}	$V_{ILL}=V_{SS}$, Latch input terminal	-3	0	3	
	I_{ILP2}	$V_{ILP2}=V_{SS}$, $\overline{SS}$ RUN	-125	-50	-15	
		STOP	-3	0	3	
Input leakage current	I_{LI1}	$V_{LI1}=V_{DD}$, Except for $\overline{SS}$	-3	0	3	μA
	I_{LI2}	$\overline{SS}$ terminal open	-3	0	3	
Output leakage current (at High-impedance)	I_{LOP}	$V_{LOP}=V_{SS}$, I/O port with pull-up	-250	-100	-30	μA
	I_{LOL}	$V_{LOL}=V_{SS}$, I/O port with latch	-3	0	3	
	I_{LOH}	$V_{LOH}=V_{DD}$, Output terminal	-3	0	3	
Standby supply current	I_{DDS}	$t_{CY}=1\mu s$, Stand-by or stop mode	—	—	20	μA
Operating supply current	I_{DDO}	$t_{CY}=1\mu s$, RUN mode	—	6	20	mA
Data retention voltage	V_{DDR}	STOP mode. Without sudden fluctuation of voltage	3.0	—	—	V

AC Characteristics

($V_{DD}=5V\pm10\%$, $V_{SS}=0V$, $f_{OSC}=3.579545MHz$, $Ta=-10$ to 70℃)

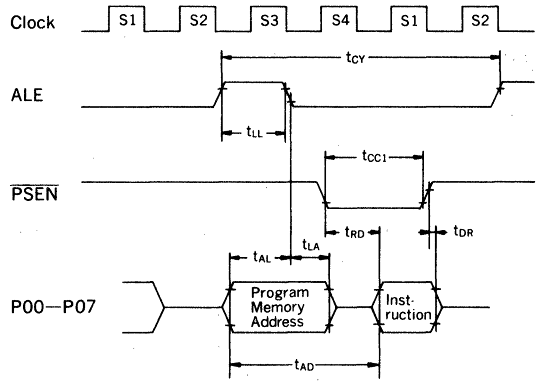
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Cycle time	t_{CY}		—	1.117	—	μs
ALE pulse width	t_{LL}		200	—	—	ns
Address set up time	t_{AL}		100	—	—	ns
Address hold time	t_{LA}		50	—	—	ns
$\overline{PSEN}$ pulse width	tcc1		300	—	—	ns
$\overline{RD}$ pulse width	tcc2		300	—	—	ns
$\overline{WR}$ pulse width	tcc3		300	—	—	ns
Data-in delay time	t_{RD}		—	—	150	ns
Read data hold time	t_{DR}		0	—	100	ns

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Write data set up time	t_{DW}		250	—	—	ns
Write data hold time	t_{WD}		5	—	—	ns
$\overline{\text{WR}}$ delay time	t_{AW}		200	—	—	ns
Data-in delay time	t_{AD}		—	—	450	ns

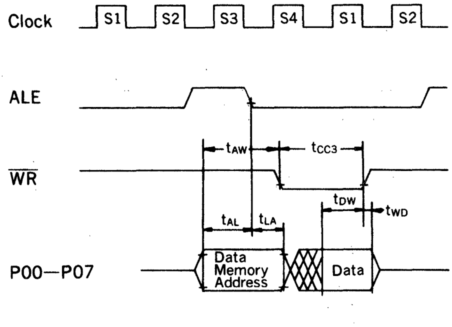
Note 1 : The load capacitance of the control pins (ALE, $\overline{\text{PSEN}}$, $\overline{\text{RD}}$ and $\overline{\text{WR}}$) is 80pF.
Note 2 : The load capacitance of port P0 is 150pF.
Note 3 : AC data measuring conditions
Input : V_{IH}=2.4V, V_{IL}=0.6V
Timing check voltage : Input··················V_{IH}=2.2V, V_{IL}=0.8V
Output···············V_{OH}=2.2V, V_{OL}=0.8V
Output load capacitance : Control pins·······80pF
Data pins ··········150pF

●Timing Chart

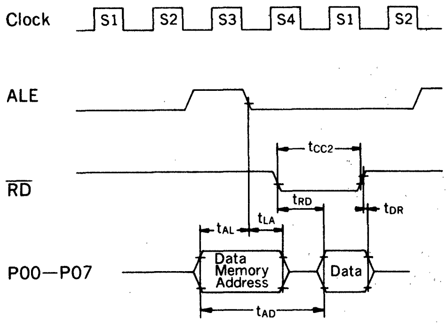
○External Program Memory Fetch Cycle



○External Data Memory Write Cycle

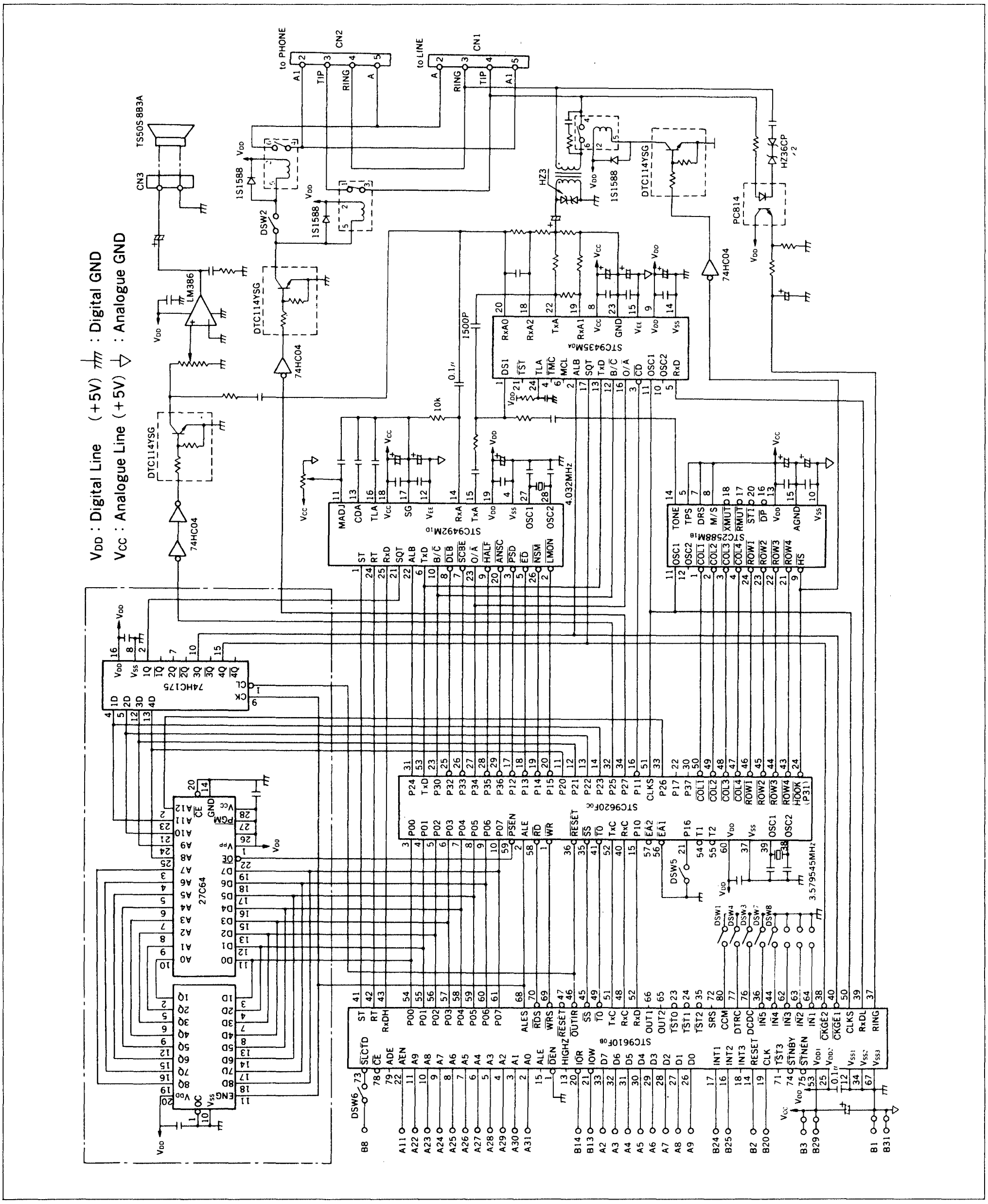


○External Data Memory Read Cycle



■EXAMPLE OF APPLICATIONS

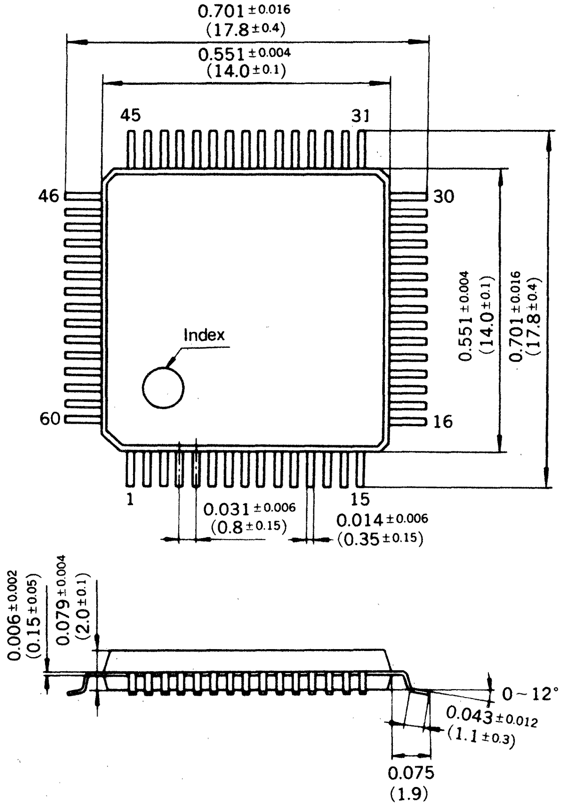
The configuration shown below is a system bus interface based intelligent modem which uses an STC9620F0B in combination with four chips: STC9610F0B, STC9492C1D (STC9492M1D), STC9435C0A (STC9435M0A) and STC2588C1B (STC2588M1B).



■PACKAGE DIMENSIONS

F60-2

60-pin QFP



unit : inch
(mm)

STC9630C$_{\mathrm{0A}}$/M$_{\mathrm{0A}}$

CMOS ASYNC-SYNC CONVERTER

- **●Compatible with Bell 212A/CCITT V.22**
- **●Selectable Character Length 8/9/10/11 Bits**
- **●Low Supply Current**

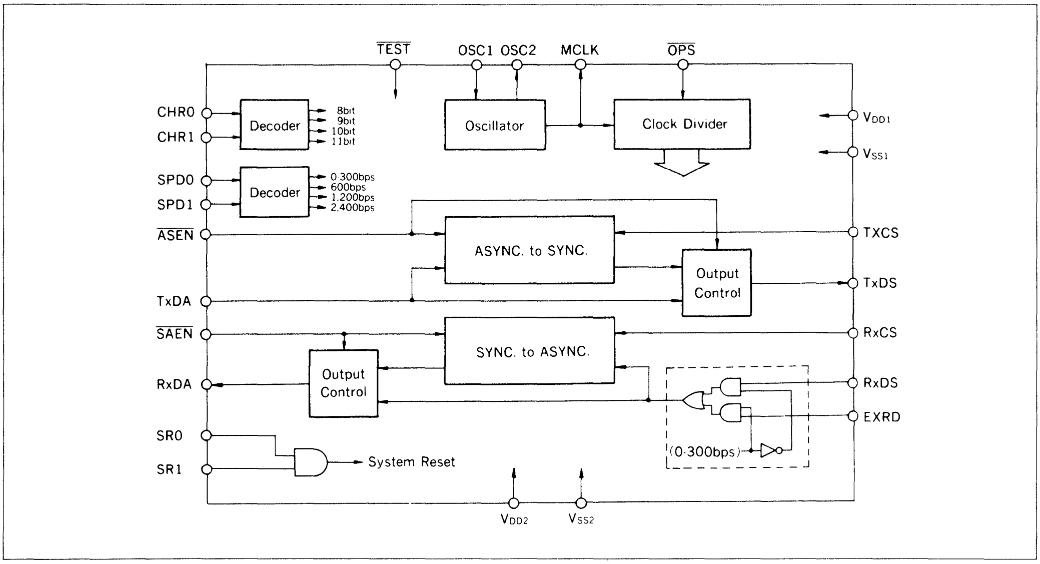
■DESCRIPTION

The STC9630C$_{\mathrm{0A}}$/M$_{\mathrm{0A}}$ LSI converts data for serial transfer between a data circuit terminating equipment (DCE) and a data terminal equipment (DTE) in either transparent mode or async/sync conversion mode.

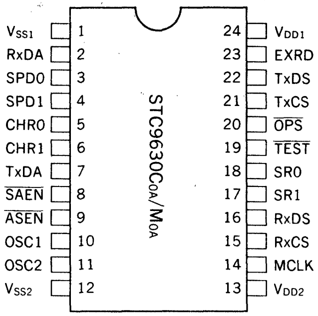
■FEATURES

- ●Full duplex data transfer (compatible with Bell 212A and CCITT V.22)
- ●Async/Sync, Sync/Async conversion
- ●Character length : 8/9/10/11 bits
- ●Built-in crystal oscillation circuit ··············4.032MHz (X'tal, R_F, C_G, C_D externally connected)
- ●Low supply current ································Operation : 5mA (Typ)
  Stand-by : 1μA (Max)
- ●Digital I/O level·······································TTL compatible
- ●Single power supply ······························5V
- ●Package··24-pin DIP (plastic)/24-pin SOP (plastic)

■BLOCK DIAGRAM



■PIN CONFIGURATION (This also applied to DIP and SOP.)



■PIN DESCRIPTION

Pin Name	Pin No.	I/O	Functions
V_{SS1}	1	—	− power (GND)
RxDA	2	O	Receive start-stop sync data output (to DTE)
SPD0	3	I*	Data speed selection Speed 0-300 600 1,200 2,400 (bps) SPD0 0 1 0 1 SPD1 0 0 1 1
SPD1	4	I*	
CHR0	5	I*	Word length selection Character length 8 9 10 11 (bits) CHR0 0 1 0 1 CHR1 0 0 1 1
CHR1	6	I*	
TxDA	7	I*	Transmit start-stop sync data input (from DTE)
$\overline{SAEN}$	8	I*	Sync → Async conversion enable
$\overline{ASEN}$	9	I*	Async → Sync conversion enable
OSC1	10	I	Oscillation pins (4.032MHz X'tal, R_F, C_G, C_D externally connected)
OSC2	11	O	
V_{SS2}	12	—	− power (GND)
V_{DD2}	13	—	+ power (+5V)
MCLK	14	O	4.032MHz output pin
RxCS	15	I*	Receive sync clock input (from DCE)
RxDS	16	I*	Receive sync data input (from DCE)
SR1	17	I*	System reset (When using STC9492, connect this pin to SQT.)
SR0	18	I*	System reset (When using STC9492, connect this pin to ALB.)
$\overline{TEST}$	19	I*	LSI test pin (normally set at NC)
$\overline{OPS}$	20	I*	Option speed selection Basic········· 1 Extended········· 0
TxCS	21	I*	Transmit sync clock input (from DTE)
TxDS	22	O	Transmit sync data output (to DCE)
EXRD	23	I*	Nonsimultaneous data input 0-300 bps
V_{DD1}	24	—	+ power (+5V)

Note) The input pin (I*) contains a pull-up resistor.

■ABSOLUTE MAXIMUM RATINGS

($V_{SS}=0V$)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.3 to 7.0	V
Input voltage	V_I	−0.3 to V_{DD}+0.3	V
Output voltage	V_O	−0.3 to V_{DD}+0.3	V
Storage temperature	T_{stg}	−65 to 150	℃
Soldering temperature and time	T_{sol}	260℃, 10s (at lead)	—

■RECOMMENDED OPERATING CONDITIONS

($V_{SS}=0V$)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}		4.75	5.00	5.25	V
Operating temperature	T_{opr}		0	—	70	℃

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

($V_{DD}=5.0V$, $V_{SS}=0V$, $Ta=25℃$)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating current	I_{DDO}	Operating ($C_L \leqq 20pF$)	3	5	10	mA
	I_{DDS}	Stand-by except OSC1, OSC2	—	—	1	μA
High level input voltage	V_{IH}	$V_{DD}=5.25V$	2.0	—	—	V
Low level input voltage	V_{IL}	$V_{DD}=4.75V$	—	—	0.8	V
High level input current	I_{IH}	except OSC1	−1	—	1	μA
Low level input current	I_{IL}	except OSC1	−50	−12.5	−5	μA
High level output voltage	V_{OH}	$V_{DD}=4.75V$, $I_{OH}=-6mA$	2.4	—	—	V
Low level output voltage	V_{OL}	$V_{DD}=4.75V$, $I_{OL}=6mA$	—	—	0.4	V

●AC Electrical Characteristics

($V_{DD}=5.0V$, $V_{SS}=0V$, $Ta=25℃$, $f_{OSC}=4.032MHz$, SPD0=Low, SPD1=High)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
TxDA Baud rate *2	f_{TxDA}	$\overline{\text{ASEN}}$=Low, $\overline{\text{OPS}}$=High	1,170(−2.5%)	1,200	1,212(+1.0%)	bps
		$\overline{\text{ASEN}}$=Low, $\overline{\text{OPS}}$=Low	1,170(−2.5%)	1,200	1,227(+2.3%)	bps
RxDA Baud rate *2	f_{RxDA}	$\overline{\text{ASEN}}$=Low, $\overline{\text{OPS}}$=High	—	1,219	—	Hz
		$\overline{\text{ASEN}}$=Low, $\overline{\text{OPS}}$=Low	—	1,219	*1	bps
MCLK Output frequency	f_{MCLK}	$V_{DD}=5.0V$, $V_{SS}=0V$	—	4.032	—	MHz

*1 In the option speed mode ($\overline{\text{OPS}}$ low), 12.5% (maximum) of stop bits may be deleted to allow an overspeed (+2.3%) on the transmit side.

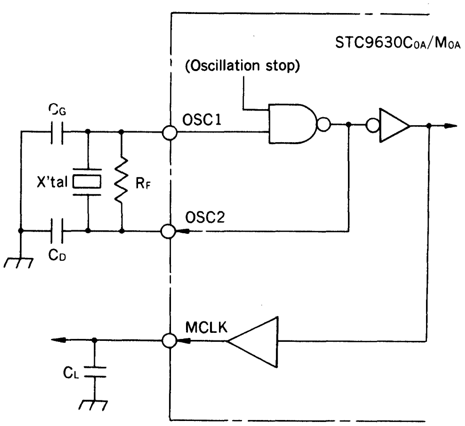
*2 If the speed is set at 600 bps or 2,400 bps, the transfer rate is one half or twice the listed value.

■FUNCTIONS

●Oscillation Circuit

○Crystal quartz oscillation

A crystal oscillator (4.032MHz), a feedback resistor (R_F) and two capacitors (C_G, C_D) are connected to the oscillation pins (OSC1, OSC2).

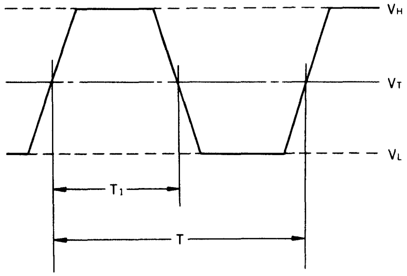


X'tal : 4.032MHz
R_F : 470kΩ (Typ)
C_G, C_D : 20 to 30pF
C_L : 50pF (Max)

When both SR0 and SR1 go high or both SPD0 and SPD1 go low, the oscillation cycle stops and the MCLK pin is fixed to high level.

○External clock into OSC1

In supplying a 4.032MHz clock pulse from an external circuit to the OSC1 pin, make sure that the MCLK output fulfills the AC characteristics shown in Figure.

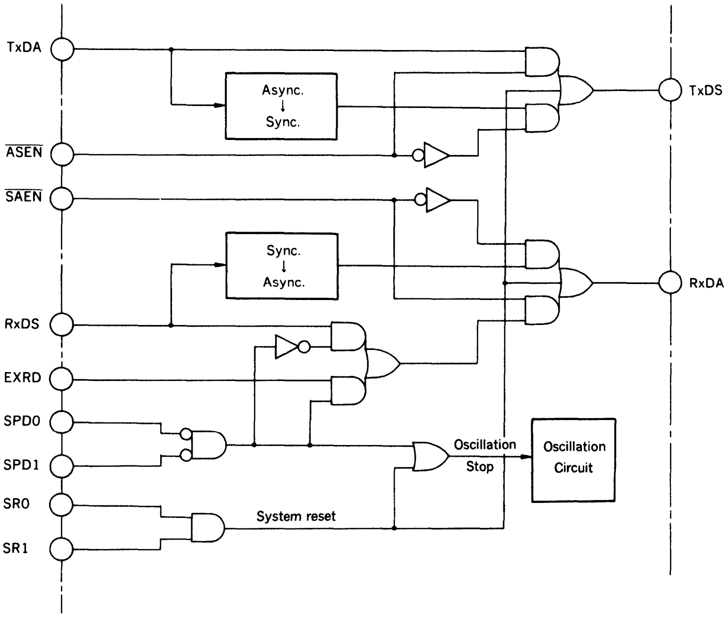


High level input voltage	$V_H \geqq V_{DD} - 1.0V$
Low level input voltage	$V_L \leqq V_{SS} + 1.0V$
Input frequency	$1/T = 4.032MHz \pm 0.01\%$
Clock duty	$T_1/T = 50 \pm 15\%$

$\left(\text{at } V_T = \frac{1}{2} V_{DD}\right)$

■I/O CONTROL FUNCTION

The STC9630C$_{0A}$/M$_{0A}$ I/O control circuit provides the transmit/receive circuits with the output data listed in the table below with each I/O pin set as shown in the figure below.



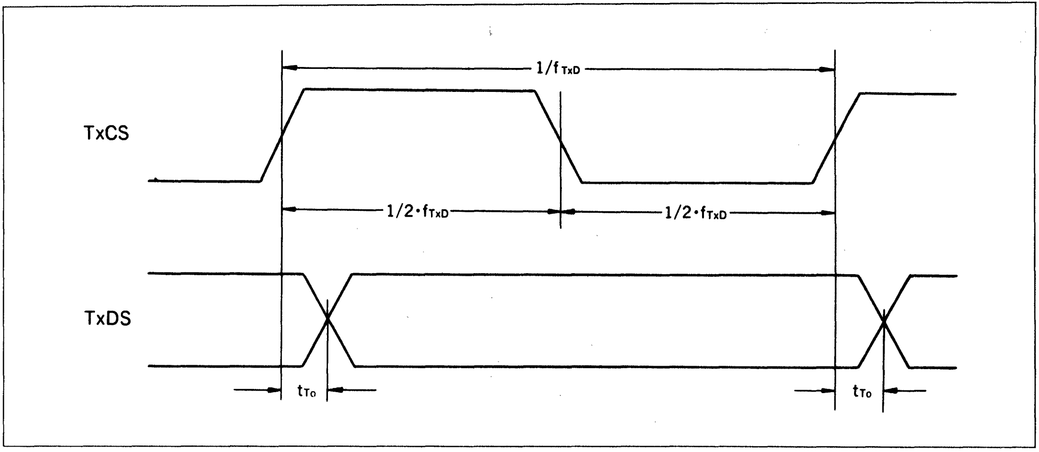
Operating mode	Terminal set						Output data		Oscillator
	SR0	SR1	$\overline{\text{ASEN}}$	$\overline{\text{SAEN}}$	SPD0	SPD1	TxDS	RxDA	
System reset	"H"	"H"	*1	*1	*1	*1	"H"	"H"	Stop
Unclocked data transfer	*2	*2	*1	*1	"L"	"L"	TxDA	EXRD	
Sync data transfer	*2	*2	"H"	"H"	*3	*3	TxDA	RxDS	Operation
Async data transfer	*2	*2	"L"	"L"	*3	*3	A→S	S→A	

*1 Don't care
*2 Other than (H, H)
*3 Other than (L, L)

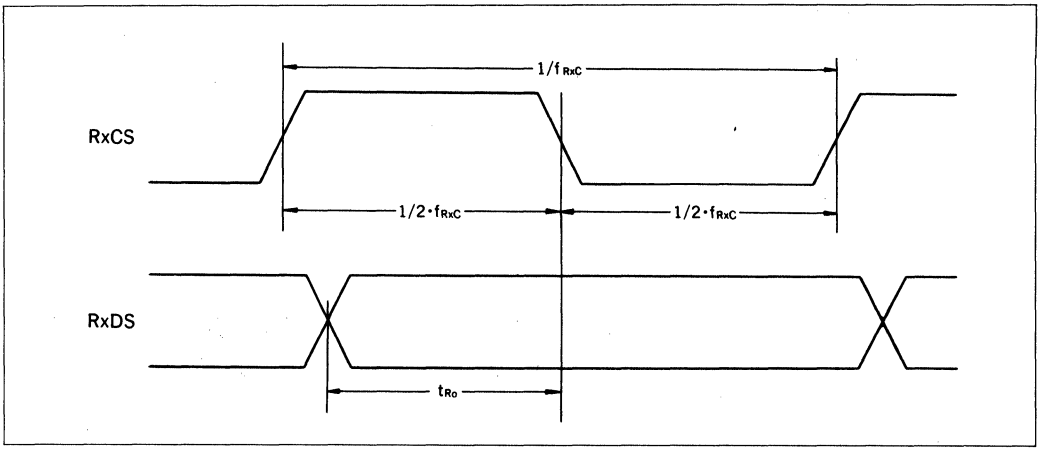
Note) $\overline{\text{ASEN}}$ and $\overline{\text{SAEN}}$ can be individually controlled.

■TIMING CHART

●Transmit Sync Data Timing Chart



●Receive Sync Data Timing Chart

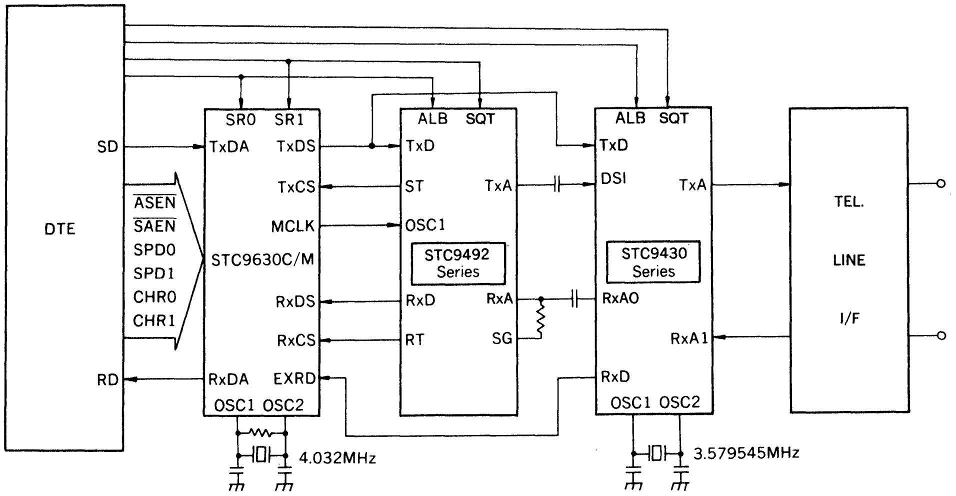


(V_{DD}=4.75V, Ta=25℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Transmit data delay time	t_{TO}	Sync data enable	—	—	100	ns
Receive data set up time	t_{RO}	Sync data enable	50	—	—	ns

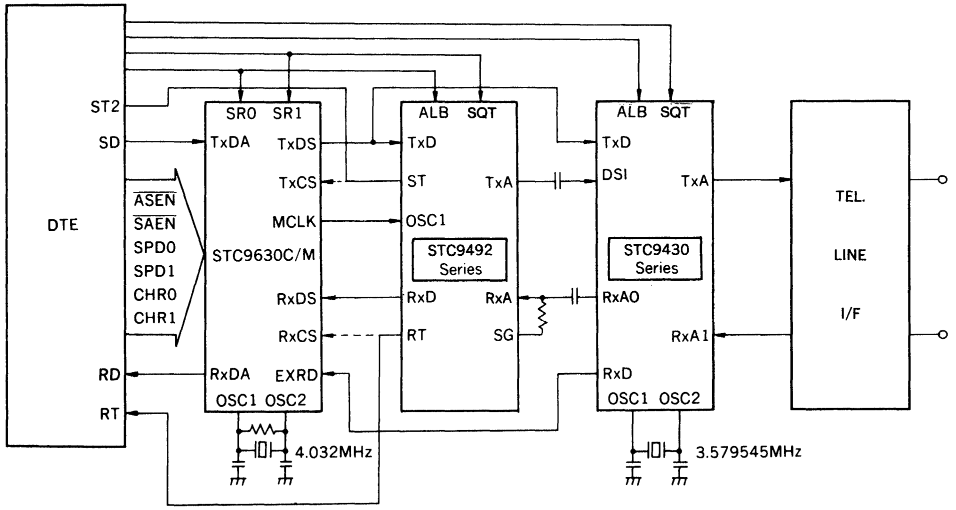
■EXAMPLE OF APPLICATIONS

●Transfer of data between sync modem and async terminal



NOTE : $\overline{\text{ASEN}}$ = "L", $\overline{\text{SAEN}}$ = "L"

●Transfer of data between sync modem and async terminal

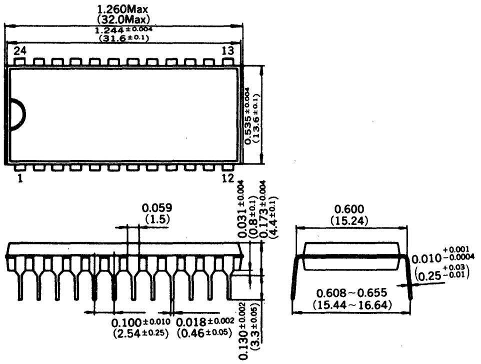


NOTE : $\overline{\text{ASEN}}$ = "H", $\overline{\text{SAEN}}$ = "H"

■PACKAGE DIMENSIONS

C24

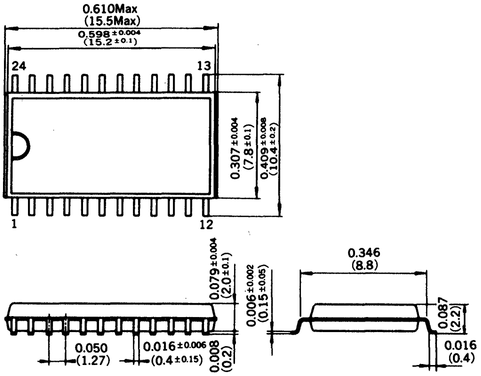
24-pin DIP



unit : inch
(mm)

M24

24-pin SOP



unit : inch
(mm)

STC9120C/M

CMOS 1,200 bps MSK MODEM

- **Minimum External Parts Required**
- **1200 bps for Full-duplex or Half-duplex System**
- **Low Supply Current**
- **On-chip Carrier Detector**

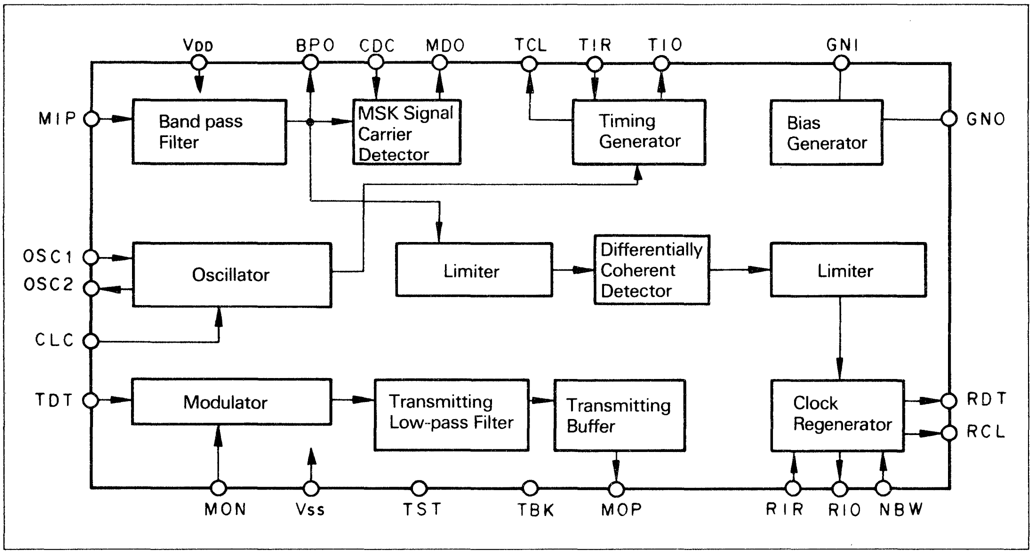
■ DESCRIPTION

The STC9120C/M is a single chip CMOS 1200 bps MSK MODEM for full-duplex or half-duplex radio communication equipment. The modulator provides a low-distrotion sinusoidal output and a sync clock output. A receiving low-pass filter, a differentially coherent detector and a clock regenerator makes up the demodulator incorporating a MSK signal carrier detector, the STC9120C/M offers a high-performance MSK MODEM with a minimum of external parts.

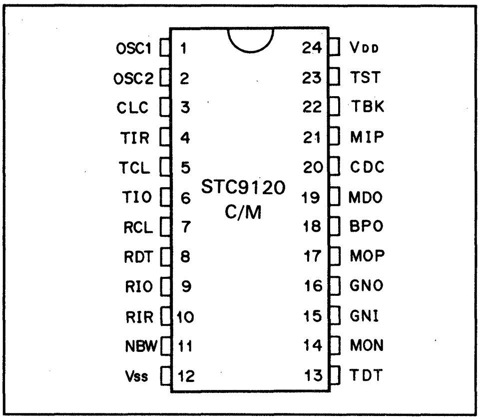
■ FEATURES

- 1200 bps full-duplex/half-duplex MSK MODEM
- Low supply current
- 5.5296 MHz crystal oscillator, or external 5.5296 MHz clock input
- Minimized external parts
- Built-in MSK signal carrier detect circuit
- TTL compatible input/output (except for terminals OSC1, OSC2, CLC, TBK and TST)
- Transmitting/receiving filter based on SCF (Switched Capacitor Filter) technology
- Little group delay distortion at the pass band
- Single power supply (+5V)
- Package····STC9120C 24-pin DIP(plastic)
  STC9120M 24-pin SOP(plastic)

■ BLOCK DIAGRAM



■ PIN CONFIGURATION (common to DIP and SOP)



■ PIN DESCRIPTION

Pin name	Pin No.	Functions
OSC1	1	5.5296 MHz (CLC = "L") or 2.7648 MHz (CLC = "H") crystal oscillator circuit or external clock input terminal.
OSC2	2	Crystal oscillator output terminal
CLC*1	3	Input teminal for oscillator frequency division control (with pull-down resistor)
TIR*2	4	Input terminal that resets the 1-bit data transmit interruption flip-flop (without pull-down resistor)
TCL	5	Transmit data sync clock signal output terminal
TIO	6	Output terminal for the 1-bit data transmit interruption flip-flop
RCL	7	Output terminal of sync clock signals regenerated from demodulated data
RDT	8	Output terminal of demodulated receive data
RIO	9	Output terminal for the 1-bit data receive interruption flip-flop
RIR*2	10	Input terminal that resets the 1-bit data receive interruption flip-flop (without pull-down resistor)
NBW*2	11	Input terminal that controls selection of DPLL circuit lock-in range (narrow/wide) (without pull-down resistor) Narrow..... high level Wide..... low level
Vss	12	Supply voltage (0V)
TDT*2	13	Input terminal of NRZ signals to be transmitted (without pull-down resistor)
MON*2	14	Input terminal for MSK signal transmit control (without pull-down resistor)
GNI	15	Input terminal of intermediate point reference voltage for power supply
GNO	16	Output terminal of intermediate point reference voltage for built-in operational amplifier
MOP	17	MSK signal output terminal
BPO	18	Receiving band low-pass filter output monitor terminal (normally non-connected)
MDO	19	MSK signal carrier detector output terminal
CDC	20	Input terminal for application of offset voltage to set MSK signal carrier detection threshold value (with C-R connected externally)
MIP	21	MSK signal input terminal
TBK*1	22	Function test terminal (normally non-connected; with pull-down resistor)
TST*1	23	Function test terminal (normally non-connected; with pull-down resistor)
VDD	24	Supply voltage (+5V)

*1 These input terminals are pulled down with a resistor, typically 500 kΩ. It is recommended that they are directly pulled down to V_{DD}' not left open, when they are not used, regarding to noise effect.

*2 These input terminals are input gate floating type. When not used, they must be directly pulled down to V_{SS}' not left open.

■ ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0V, Ta = 25°C)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.3 to 8.0	V
Input voltage*	V_I	−0.3 to V_{DD} +0.3	V
Output voltage	V_O	−0.3 to V_{DD} +0.3	V
Power dissipation	P_D (Max)	500	mW
Operating temperature	Topr	−25 to 70	°C
Storage temperature	Tstg	−65 to 150	°C
Soldering temperature and time	Tsol	260°C, 10 s (at lead)	−

■ ELECTRICAL CHARACTERISTICS

● DC Characteristics

(V_{DD} = 5.0V, V_{SS} = 0V and Ta = 25°C unless otherwise specified)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Supply voltage	V_{DD}			4.5	5.0	5.5	V
Supply current	I_{DD}	fosc = 5.5296 MHz		–	6	12	mA
"L" level input voltage	V_{IL1}	OSC1		Vss	–	Vss +0.3	V
"H" level input voltage	V_{IH1}			VDD −0.3	–	VDD	V
Input frequency	F_{I1}			–	5.5296	–	MHz
Input current	I_{I1}		V_{IH1} = 5V	–	0.5	–	μA
"L" level input voltage	V_{IL2}	CLC, TBK, TST		Vss	–	Vss +0.3	V
"H" level input voltage	V_{IH2}			VDD −0.3	–	VDD	V
Pull-down resistance	R_{12}			200	500	1250	KΩ
"L" level input voltage	V_{IL3}	NBW, RIR*3, RIE*3 TDT, MON		0	–	0.8	V
"H" level input voltage	V_{IH3}			2.4	–	VDD	V
Input impedance	R_{14}	MIP		70	120	190	kΩ
Input signal voltage	V_{14}		Sinewave input	–	1.0	2.0*4	Vp-p
"L" level output voltage	V_{OL1}	RCL, RDT RIO, MDO TCL, TIO	I_{OL1}=2.6mA	Vss	–	0.5	V
"H" level output voltage	V_{OH1}		I_{OH1}=−0.2 mA	4.6	–	VDD	V
Mark output voltage	V_{OM}	Load resistance: Min 10 kΩ		0.9	1.0	1.1	Vp-p
Space signal output voltage	V_{OS}			0.9	1.0	1.1	Vp-p

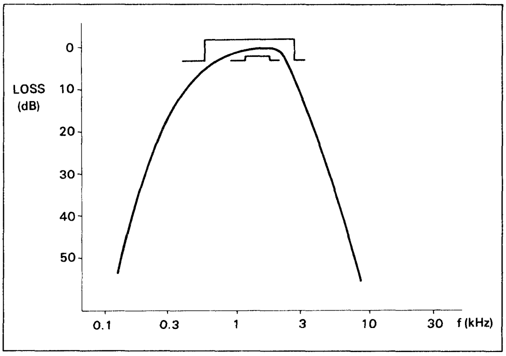
*3 The reset pulse width must be at least 1 μs.

*4 The maximum input level should be adjusted not so as to happen a malfunction.

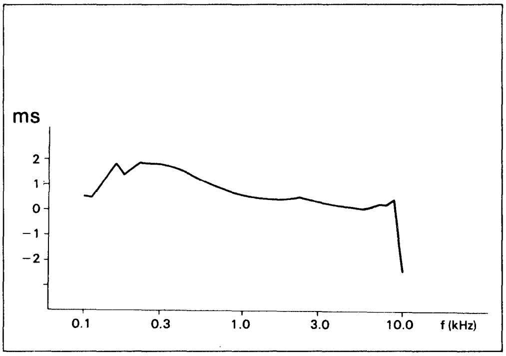
● Filter Specifications

(V_{DD} = 5.0V, V_{SS} = 0V and Ta = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
3 dB band width (Low Band)	F_{CL1}	Receiving band-pass filter	600	700	800	Hz
3 dB band width (High Band)	F_{CH1}	Butterworth	2000	2400	2800	Hz
Insertion loss	L_{B1}	10 order	−2	0	2	dB
3 dB band width (High Band)	F_{C2}	Transmitting low band-pass	4250	5000	5750	Hz
Insertion loss	L_{B2}	filter Butterworth 5 order	−2	0	2	dB
3 dB band width (High Band)	F_{C3}	Receiving low band-pass filter	1000	1200	1400	Hz
Insertion loss	L_{B3}	Butterworth 3 order	−2	0	2	dB



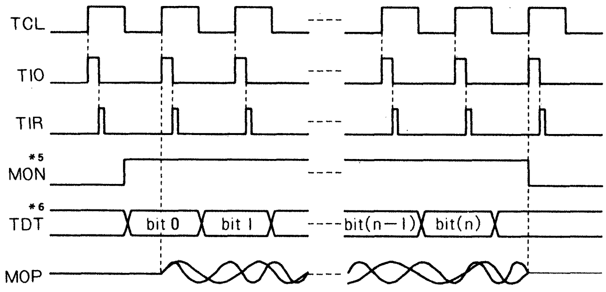
Band Pass Filter Frequency Characteristics



Band Pass Filter Group Delay Characteristics

■ DATA INPUT/OUTPUT TIMING CHART

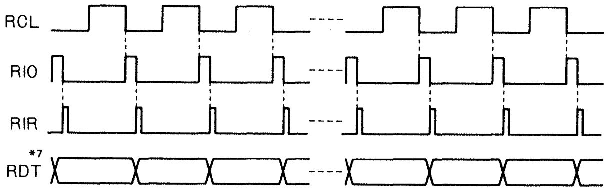
● Data Transmit Timing Chart



*5 When data transmission starts, MON must go to "H" level within about 833 μs following the leading edge of the TCL. When the data transmission ends, MON must go to "L" level at the leading edge of the next TCL following the transmission of the last bit of MOP.

*6 For TDT, data must be set within about 833 μs after the occurrence of an interrupt.

● Data Receive Timing Chart

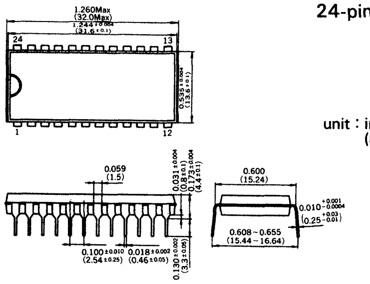


*7 RDT must be read within about 833 μs following the leading edge of RCL.

■ PACKAGE DIMENSIONS

C24

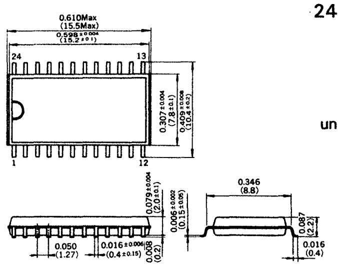
24-pin DIP



unit : inch
(mm)

M24

24-pin SOP



unit : inch
(mm)

KF060
PF347-02

STC2530C Series

CMOS TONE/PULSE DIALER WITH LCD DRIVER

- DTMF/Pulse Output Switch
- 10 Digit LCD Driver
- Ten 18-digit Repertory Memories and 24-digit Redial Memory

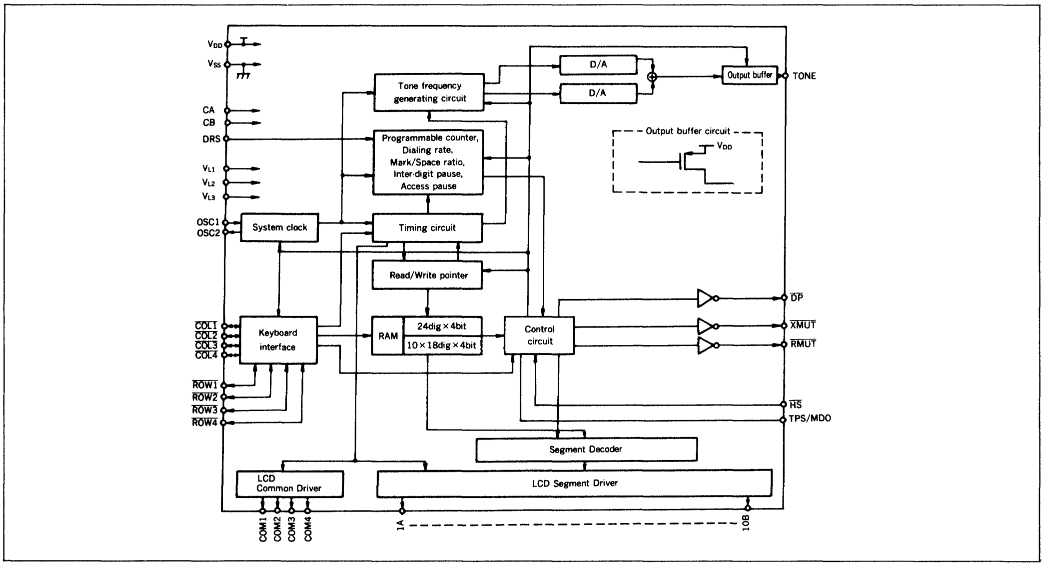
■DESCRIPTION

The STC2530C series is CMOS LSI which is provided with a memory and LCD display driver for telephone numbers, and can selectively output either dual tone multi-frequency (DTMF) signals or a dialing pulse (DP) train. The LSI contains the DA conversion system used in a conventional tone dialer by connecting the minimum necessary interface circuit, the dialing pulse can also drive a telephone line.

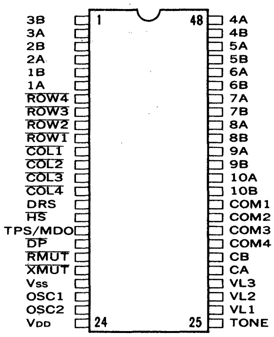
■FEATURES

- Low-voltage operation and low power dissipation due to CMOS process.
- A built-in 10 digit LCD drivers for telephone numbers. (V−3V, 1/4duty)
- A built-in Ten 18-digit repertory memories and 24-digit redial memory.
- A built-in DA conversion system makes possible a DTMF signal.
- 0.6sec Hooking (Flash) can be accessed directly by Flash key.
- This LSI can be connected to a standard 2 of 8 keyboard.
- The built-in signal generator requires 3.58MHz TV crystal oscillator.
- Package·········48 pin DIP (plastic)

■BLOCK DIAGRAM



■PIN CONFIGURATION



■STC2530C Series

Type	Write to repartory memory	Tone/pulse output selection	Dial pulse mark/space
STC2531C$_{0A}$	OFF-Hook	Key	33.3/66.6
STC2531C$_{0B}$			40/60
STC2532C$_{0A}$	ON-Hook	Key	33.3/66.6
STC2532C$_{0B}$			40/60
STC2533C$_{0A}$	OFF-Hook	External pin	33.3/66.6
STC2533C$_{0B}$			40/60
STC2534C$_{0A}$	ON-Hook	External pin	33.3/66.6
STC2534C$_{0B}$			40/60

■PIN DESCRIPTION

Pin Name	Pin No.	Function
$\overline{\text{ROW1}}$ to $\overline{\text{ROW4}}$	7 to 10	[Scanning input/output of matrix keyboard]
$\overline{\text{COL1}}$ to $\overline{\text{COL4}}$	11 to 14	
TPS/MDO	17	[DTMF/DP mode select input] /[DTMF/DP mode signal output]
DRS	15	[Pulse rate select input in DP mode]
$\overline{\text{HS}}$	16	[Hook switch]
V$_{SS}$	21	[Power supply terminal (−)]
OSC1	22	[3.579545MHz crystal oscillator terminal]
OSC2	23	
V$_{DD}$	24	[Power supply terminal (+)]
TONE	25	[DTMF signal output]
$\overline{\text{DP}}$	18	[Dialing pulse output]
$\overline{\text{RMUT}}$	19	[Receiver mute output]
$\overline{\text{XMUT}}$	20	[Transmitter mute output]
VL1	26	[Doubler & Tripller capacitor]
VL2	27	
VL3	28	
CA	29	
CB	30	
COM1 to COM4	31 to 34	[Common Driver output]
1A to 10A 1B to 10B	1 to 6 35 to 48	[Segment Driver output]

■ABSOLUTE MAXIMUM RATINGS

($V_{SS}=0V$)

Parameter	Symbol	Ratings	Unit
Power supply voltage	V_{DD}	-0.3 to 7.5	V
Input voltage	V_I	-0.3 to $V_{DD}+0.3$	V
Output voltage	V_O	-0.3 to $V_{DD}+0.3$	V
Operating temperature	T_{opr}	-20 to 70	℃
Storage temperature	T_{stg}	-65 to 150	℃
Soldering temperature and time	T_{sol}	260℃, 10s (at lead)	—

■ELECTRICAL CHARACTERISTICS

●DC Characteristics

($V_{SS}=0V$, $Ta=25℃$)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Operating voltage	V_{DD}	DP mode		1.5	—	6.0	V
		DTMF mode		2.5	—	6.0	
Data retention voltage	V_{DDR}	Stand-by mode		1.0	—	6.0	V
Average operating current	I_{DDA}	$V_{DD}=3.0V$, $Ta=25℃$ $\overline{HS}=V_{SS}$ $\overline{DP}$, TONE, $\overline{RMUT}$ and $\overline{XMUT}$ not loaded	Key input stand-by status	—	—	200	μA
			In DP mode dial pulse being output	—	—	400	μA
			In DTMF mode DTMF signal being output	—	—	1.5	mA
LCD operating voltage	V_{L2}	$V_{L1}>V_{L2}>V_{L3}$		—	$V_{DD}-2\times V_{L1}$	—	V
	V_{L3}			—	$V_{DD}-3\times V_{L1}$	—	

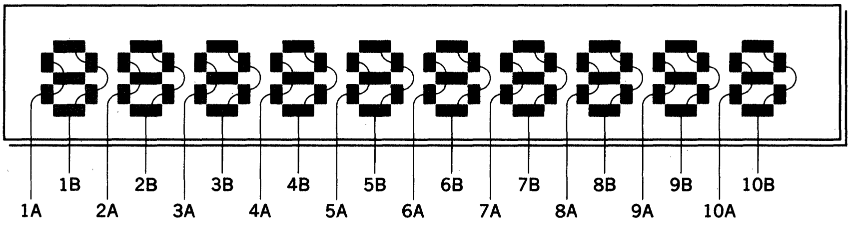
●AC Characteristics

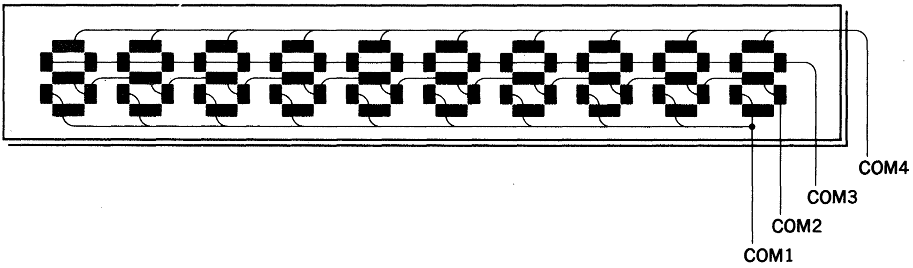
($V_{SS}=0V$, $Ta=25℃$, $f_{OSC}=3.579545MHz$)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Dial pulse rate	—	$DRS=V_{DD}$		—	19.42	—	pps
	—	$DRS=V_{SS}$		—	9.71	—	
Inter digit pause	t_{IDP1}	DP mode	Dial rate =19.42pps	—	463.4	—	ms
			Dial rate =9.71pps	—	823.9 (617.9)*	—	
	t_{IDP2}	DTMF mode auto dialing		—	—	112.9 (61.4)*	
DTMF make time	t_{TM}	DTMF mode auto dialing		93.1	—	—	ms
Oscillator frequency	t_{OSC}			—	3.579545	—	MHz
Tone output voltage	Vt_{one}	COL	$V_{DD}=2.5V$ to $6.0V$	—	-11.7	—	dBm
		ROW		—	-14.2	—	
Tone distortion	%DIS	$V_{DD}=3.5V$		—	—	10	%
Hooking (flash)	t_{HK}			—	617.5 (82.0)*	—	ms

Note: *Mask option

■LCD PATTERN LAYOUT





■PACKAGE DIMENSIONS

C48

48-pin DIP

Under Development

STC2560C

CMOS PULSE DIALER

- **Low Voltage Operation (Min 1.25V)**
- **20-digit Memory for Redial**
- **Pin Compatible to AMI S2560A**

■DESCRIPTION

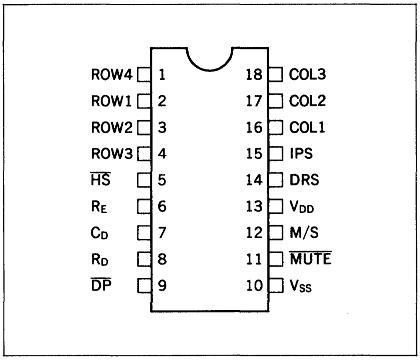
The STC2560C Pulse Dialer is a CMOS IC that converts push-button inputs to a series of pulses suitable for telephone dialing. It requires no independent external power supply but can be driven on the power supplied from telephone lines.

The STC2560C has two output terminals : one for the transmission of dial pulses and the other for providing signals to mute the receiver during the dial pulsing.

■FEATURES

- Directly operation from the telephone lines
- Low power CMOS process. (1.25V to 3.5V)
- Inexpensive RC oscillator built-in
- Mark/space ratio selectable
- Dial rate selectable
- 20-digit memory for Redial by "#" key

■PIN CONFIGURATION



■PIN DESCRIPTION

<table>
<tr><th>Pin Name</th><th>Pin No.</th><th>Functions</th></tr>
<tr><td>Keyboard
ROW1 to ROW4
COL1 to COL3</td><td>
1 to 4
16 to 18</td><td>4×3 matrix input terminals on keyboard. Selected depending on whether ROW and COL reach V_{DD} or connect with each other. Input is detected through chattering killer. The keyboard scan begins when a key is pressed and starts the oscillator.</td></tr>
<tr><td>$\overline{HS}$ (Hook Switch)</td><td>5</td><td>Input terminal which detects that the telephone set has become active when the handset is hooked off.
"OFF-HOOK" corresponds to V_{SS} condition.</td></tr>
<tr><td>R_E, C_D, R_D</td><td>6 to 8</td><td>Terminals for oscillation.</td></tr>
<tr><td>$\overline{DP}$ (Dial Pulse Out)</td><td>9</td><td>Dial pulse output terminal</td></tr>
<tr><td>V_{DD} (Power Supply)
V_{SS} (Power Supply)</td><td>13
10</td><td>Power terminals. The device is designed to operate from 1.25V to 3.5V</td></tr>
<tr><td>$\overline{MUTE}$ (Mute Out)</td><td>11</td><td>Output terminal to prevent handset noise from entering the line during dialing.</td></tr>
<tr><td>M/S (Mark/Space)</td><td>12</td><td>Terminal for selecting a mark/space ratio.
<table>
<tr><th>Input Logic Level</th><th>Mark</th><th>Space</th></tr>
<tr><td>V_{DD}</td><td>40</td><td>60</td></tr>
<tr><td>V_{SS}</td><td>100/3</td><td>200/3</td></tr>
</table></td></tr>
<tr><td>DRS (Dial Rate Select)</td><td>14</td><td>Terminal for selecting a dial pulse rate.
<table>
<tr><td>V_{DD}</td><td>20pps</td></tr>
<tr><td>V_{SS}</td><td>10pps</td></tr>
</table></td></tr>
<tr><td>IPS (Inter-digit Pause Select)</td><td>15</td><td>Terminal for selecting a dial pulse pause time between digits.
<table>
<tr><th>Input Logic Level</th><th>DR 20pps</th><th>DR 10pps</th></tr>
<tr><td>V_{DD}</td><td>470ms</td><td>620ms</td></tr>
<tr><td>V_{SS}</td><td>400ms</td><td>800ms</td></tr>
</table></td></tr>
</table>

■ABSOLUTE MAXIMUM RATINGS

($V_{SS}=0V$)

Parameter	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	−0.3	5.0	V
Operating temperature	T_{opr}	−30	70	℃
Storage temperature	T_{stg}	−55	125	℃
Input voltage	V_I	$V_{SS}-0.3$	$V_{DD}+0.3$	V

■ELECTRICAL CHARACTERISTICS

●DC Characteristics

($V_{SS}=0V, Ta=-30$ to 70℃)

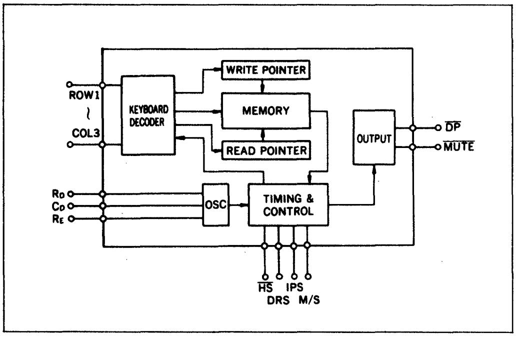
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}		1.25	—	3.5	V
Operating current	I_{OP}	$V_{OP}=3.5V$	—	—	200	μA
Data retention voltage	V_{DR}		1.0	—	—	V
Data retention current	I_{DR}	$V_{DR}=1.0V$	—	—	0.75	μA
$\overline{DP}$ sink current	I_{PL}	$V_{OP}=3.5V, V_O=0.4V$	1.0	—	—	mA
$\overline{DP}$ source current	I_{PH}	$V_{OP}=3.5V, V_O=2.5V$	1.0	—	—	mA
$\overline{Mute}$ sink current	I_{ML}	$V_{OP}=3.5V, V_O=0.4V$	1.0	—	—	mA
$\overline{Mute}$ source current	I_{MH}	$V_{OP}=3.5V, V_O=2.5V$	1.0	—	—	mA
Logic " 1 "	V_H		80% of V_{OP}	—	—	V
Logic " 0 "	V_L		—	—	20% of V_{OP}	V

●AC Characteristics

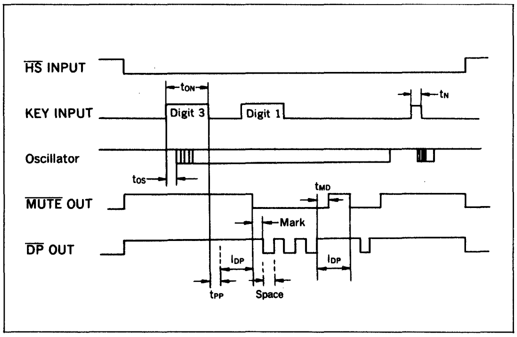
($f_{OSC}=2.4kHz$)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Pre-pause	t_{PP}		4.58	6.25	7.92	ms
Time for valid key entry	t_{ON}		28.34	—	—	ms
Oscillator start up time	t_{OS}		—	—	1.0	ms
Mute delay	t_{MD}		—	9.17	—	ms
Approval noise pulse width	t_N		—	—	13.3	ms

■BLOCK DIAGRAM



●Timing Chart



STC2565C

CMOS PULSE DIALER

- Low Voltage Operation
- 20-digit Memory for Redial
- Crystal Oscillation (32.768 KHz)

■ DESCRIPTION

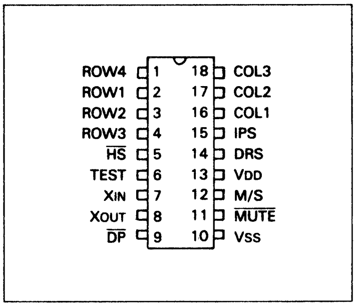
The STC2565C Pulse Dialer is a CMOS IC that converts push-button inputs to a serial pulses of telephone dialing. It requires no independent external power supply but can be driven on the power supplied from telephone lines.

The STC2565C has same functions and pin configuration as the STC2560C except the oscillation circuit.

■ FEATURES

- Directly Operation from the telephone lines
- Low power CMOS process. (1.3V to 3.5V)
- High accuracy crystal oscillation (32.768 KHz)
- Mark/space ratio selectable
- Dial rate selectable
- 20-digit memory for Redial by "#" key

■ PIN CONFIGURATION



■ PIN DESCRIPTION

<table>
<tr><th>Pin Name</th><th>Pin No.</th><th>Functions</th></tr>
<tr><td>Keyboard
ROW1 to ROW4
COL1 to COL3</td><td>1to4
16to18</td><td>4 x 3 matrix input terminals on keyboard. Selected depending on whether ROW and COL reach VDD or connect with each other. Input chatter – protection circuit is built – in. The keyboard scan begins when a key is pressed and starts the oscillator.</td></tr>
<tr><td>HS (Hook Switch)</td><td>5</td><td>Input terminal which detects that the telephone set has become active when the handset is hooked off.
"OFF-HOOK" corresponds to VSS condition.</td></tr>
<tr><td>TEST</td><td>6</td><td>Test terminal for IC testing (Pull – downed to VSS internally)</td></tr>
<tr><td>XIN, XOUT</td><td>7,8</td><td>Terminals for oscillation. (Connect only a crystal between 2 terminals)</td></tr>
<tr><td>DP (Dial Pulse Out)</td><td>9</td><td>Dial pulse output terminal</td></tr>
<tr><td>VDD (Power Supply)
VSS (Power Supply)</td><td>13
10</td><td>Power terminals. The device is designed to operate from 1.3V to 3.5V</td></tr>
<tr><td>MUTE (Mute Out)</td><td>11</td><td>Output terminal to prevent handset noise from entering the line during dialing.</td></tr>
<tr><td>M/S (Mark/Space)</td><td>12</td><td>Terminal for selecting a mark/space ratio.
<table>
<tr><th>Input Logic Level</th><th>Mark</th><th>Space</th></tr>
<tr><td>VDD</td><td>40</td><td>60</td></tr>
<tr><td>VSS</td><td>100/3</td><td>200/3</td></tr>
</table></td></tr>
<tr><td>DRS (Dial Rate Select)</td><td>14</td><td>Terminal for selecting a dial pulse rate.
<table>
<tr><td>VDD</td><td>19.50 pps</td></tr>
<tr><td>VSS</td><td>9.75 pps</td></tr>
</table></td></tr>
<tr><td>IPS (Inter-digit Pause Select)</td><td>15</td><td>Terminal for selecting a dial pulse pause time between digits.
<table>
<tr><th>Input Logic Level</th><th>DR 19.50 pps</th><th>DR 9.75 pps</th></tr>
<tr><td>VDD</td><td>410.16 ms</td><td>820.31 ms</td></tr>
<tr><td>VSS</td><td>481.93 ms</td><td>635.74 ms</td></tr>
</table></td></tr>
</table>

■ ABSOLUTE MAXIMUM RATINGS

(Vss=0V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{DD}	–0.3	5.0	V
Operating Temperature	T_{opr}	–30	70	°C
Storage Temperature	T_{stg}	–55	125	°C
Input Voltage	V_I	Vss–0.3	VDD+0.3	V

■ ELECTRICAL CHARACTERISTICS

● DC Characteristics

(Vss=0V, Ta=–30°C to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	T_{OP}=0 to 70°C T_{OP}=–30 to 0°C	1.30 1.50	– –	3.50 3.50	V
Operating Current	I_{OP}	V_{OP}=1.8V, T_{OP}=25°C	–	2.00	5.00	μA
Data Retention Voltage	V_{DR}		1.00	–	–	V
Data Retention Current	I_{DR}	V_{OP}=1.0V	–	–	0.75	μA
$\overline{DP}$ Sink Current	I_{PL}	V_{OP}=3.5V, V_O=0.4V	1.00	–	–	mA
$\overline{DP}$ Source Current	I_{PH}	V_{OP}=3.5V, V_O=2.5V V_{OP}=1.5V, V_O=1.0V	1.00 130	– –	– –	mA μA
$\overline{Mute}$ Sink Current	I_{ML}	V_{OP}=3.5V, V_O=0.4V	1.00	–	–	mA
$\overline{Mute}$ Source Current	I_{MH}	V_{OP}=3.5V, V_O=2.5V V_{OP}=1.5V, V_O=1.0V	1.00 130	– –	– –	mA μA

● AC Characteristics

(fosc=32.768 kHz)

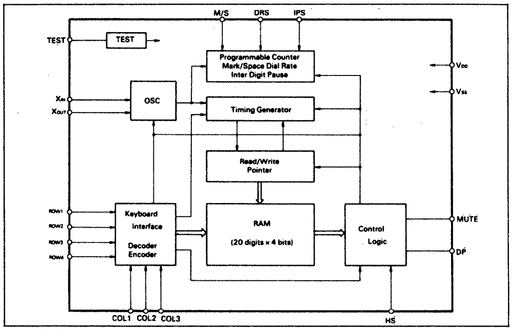
Symbol	Parameter : Conditions	Min	Typ	Max	Unit
t_{ON}	Time for Valid Key Entry	29.06	–	–	msec
t_{OFF}	Time for Valid Key Down	1.72	–	–	msec
t_{PP}	Pre-Pause	4.70	6.41	8.12	msec
t_{MD}	Mute Delay	–	9.40	–	msec
t_N	Approval Noise Pulse Width	–	–	13.64	msec

● Oscillation Characteristics

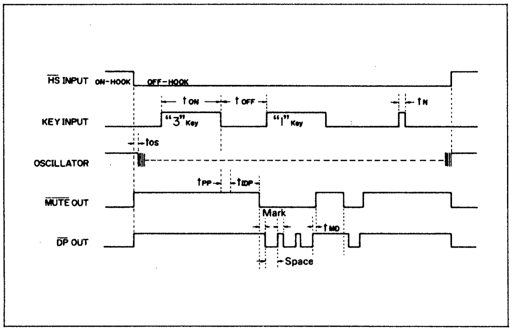
(Ta=–30°C to 70°C)

Symbol	Parameter : Conditions	Min	Typ	Max	Unit
f_o	Frequency of Oscillation	–0.05	32768 Hz	+0.05	%
V_{STA}	Oscillator Start up Voltage T=–30 to 0°C T=0 to 70°C	– –	– –	1.50 1.30	V
V_{STP}	Oscillator Stop Voltage T=–30 to 0°C T=0 to 70°C	– –	– –	1.30 1.10	V
t_{os}	Oscillator Start up Time $C_I \leqq 40K\Omega$, T=–20 to 70°C	–	200	600	msec
$\Delta f/f_o$	$1.2V \leqq V_{DD} \leqq 3.5V$	–	–	100	PPm

■ BLOCK DIAGRAM



● Timing Chart



PF290-02

STC2570C Series

CMOS REPERTORY DIALER

- **Low Voltage Driving, Low Supply Current**
- **Twenty 18-digit Repertory Memories on Chip**
- **Last Number Redial (22-digit) Memory on Chip**

■DESCRIPTION

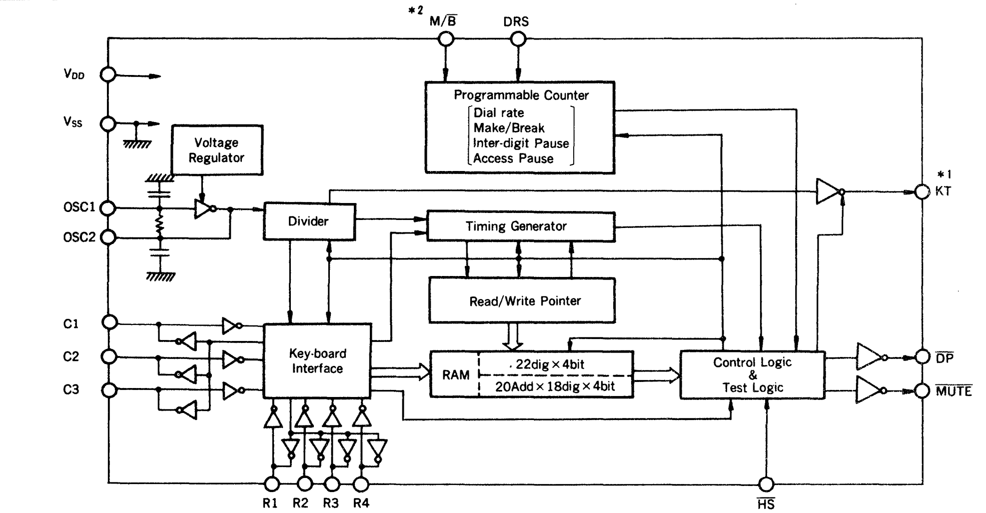
STC2570C series is CMOS LSI for conversion between push button and dial pulse. It has built-in memories which memorize telephone numbers as abbreviated dial numbers. In addition to the basic movement as repertory dialer, there are some optional mechanisms to be selected by mask conversion for better use.

■FEATURES

- Low voltage CMOS process, Low supply current
- Twenty 18-digit number memories plus last number redial (22-digit) memory on chip
- Selection of dialing rates (10 pps/20 pps)
- Four types of dialing ·····························normal dialing, redialing, repertory dialing, and mixed dialing
- Able to inhibit dialing
- Selection of make and break (1/2 or 2/3)*1
- Built in call disconnect mechanism*1
- Manual pause for access pause (HALT)*1
- Auto pause for access pause (3.59 sec)*2
- Built-in Hooking mechanism (Hooking time 0.5 sec)*2
- Built-in sound generator for key operation confirmation*2
- Built-in crystal oscillation circuit, External connection between crystal oscillator (f_0-32.768kHz) only
- Interface with standard 2 of 7 key board
- Package···16-pin DIP (plastic)

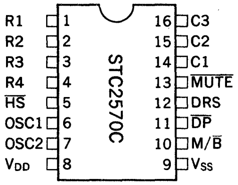
*1 For STC2570C only
*2 For STC2571C only

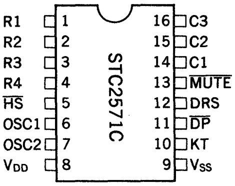
■BLOCK DIAGRAM



*1 This terminal does not apply to 2570C.
*2 This terminal does not apply to 2571C.

PIN CONFIGURATION





PIN DESCRIPTION

Pin Name	Pin No.	Functions
C1—C3 R1—R4	14—16 1 — 4	I/O pins for scanning the 2-of-7 matrix keyboard. A key is selected when V_{DD} level is applied to both the appropriate COL and ROW pins.
$\overline{\text{HS}}$	5	Input pin for detecting the status of the hook switch (OFF-hook: V_{SS} level). If $\overline{\text{HS}}=V_{DD}$ level (ON-hook), only writing to the repertory memory is enabled. If $\overline{\text{HS}}=V_{SS}$ level (OFF-hook), a dial pulse is generated when an appropriate key is pressed. Since this input pin is a floating type, it must always be supplied with either V_{DD} level or V_{SS} level.
OSC1	6	Only a 32.768kHz crystal oscillator is connected between these two pins to form a crystal oscillation circuit (the reference signal source).
OSC2	7	
V_{DD}	8	Power pin (+)
V_{SS}	9	Power pin (−)
M/$\overline{\text{B}}$*1	10	Keying confirmation tone output pin. It generates a confirmation tone only when a valid key is pressed (except during a hooking operation). Confirmation tone duration: 26.49msec Confirmation tone frequency: 910.22Hz During absence of confirmation tone: high impedance output.
KT*2	10	Dial pulse make/break ratio select pin. V_{SS} level: 100/3 or 200/3 V_{DD} level: 40/60 Since this input pin is a floating type, it must always be supplied with either V_{DD} level or V_{SS} level.
$\overline{\text{DP}}$	11	Dial pulse output pin, which generates V_{SS} level during an ON-hook or call-disconnect, or during an OFF-hook with no call. It outputs V_{DD} level during a make, and V_{SS} level during a break.
DRS	12	Dial pulse rate select pin. V_{SS} level: 10pps (9.752pps) V_{DD} level: 20pps (19.505pps) Since this pin is a floating type, it must always be supplied with either V_{DD} level or V_{SS} level. The inter-digit pause is fixed for each dial rate: IDP=615.2msec at DR=10pps IDP=461.4msec at DR=20pps
$\overline{\text{MUTE}}$	13	Mute output pin, which generates V_{SS} level during an ON-hook or call-disconnect and V_{DD} level during an OFF-hook with no call. It outputs V_{SS} level while dial pulses are being sent. (Not intermittent between digits)

*1 For STC2570C only *2 For STC2571C only

STC2570C SERIES

Series Name	Functions	
STC2570C$_{0A}$	• Make/break (1/2 or 2/3) selectable • On-chip call disconnect function • Manual access pause	IDP=615.2msec at DR=10pps IDP=461.4msec at DR=20pps
STC2571C$_{0A}$	• On-chip keying confirmation tone function • On-chip hooking function • Auto access pause	
STC2570C$_{0B}$	• Make/break (1/2 or 2/3) selectable • On-chip call disconnect function • Manual access pause	IDP=820.3msec at DR=10pps IDP=410.2msec at DR=20pps
STC2571C$_{0B}$	• On-chip keying confirmation tone function • On-chip hooking function • Auto access pause	

■ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V, Ta=25°C)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.3 to 7.5	V
Input voltage	V_I	V_{SS}−0.3 to V_{DD}+0.3	V
Output voltage	V_O	V_{SS}−0.3 to V_{DD}+0.3	V
Operating temperature	T_{opr}	−25 to 70	°C
Storage temperature	T_{stg}	−65 to 150	°C
Soldering temperature and time	T_{sol}	260°C, 10s (at lead)	—

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

(f_{OSC}=32.768kHz, Ta=25°C, V_{SS}=0V)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Supply voltage	V_{DD}	—		1.3	—	6.0	V
Data retention voltage	V_{DDR}	$\overline{HS}$=V_{DD}		1.0	—	—	V
Average operating current	I_{DDA}	V_{DD}=1.8V	C1—C3, R1—R4, $\overline{DP}$, $\overline{MUTE}$= open $\overline{HS}$, M/$\overline{B}$, DRS=V_{DD}	—	2	5	μA
		V_{DD}=2.4V		—	2.5	—	
High level input voltage	V_{IH}	C1—C3, R1—R4 $\overline{HS}$, M/$\overline{B}$, DRS		0.8V_{DD}	—	V_{DD}	V
Low level input voltage	V_{IL}	C1—C3, R1—R4 $\overline{HS}$, M/$\overline{B}$, DRS		V_{SS}	—	0.2V_{DD}	V
High level input current (1)	I_{IH1}	$\overline{HS}$, M/$\overline{B}$, DRS V_{DD}=6.0V, V_{IH1}=V_{DD}		—	—	0.1	μA
Low level input current (1)	I_{IL1}	$\overline{HS}$, M/$\overline{B}$, DRS V_{DD}=6.0V, V_{IL1}=V_{SS}		—	—	0.1	μA
High level input current (2)	I_{IH2}	C1—C3, R1—R4, V_{DD}=2.4V, V_{IH2}=V_{DD}		—	4.5	10	μA
Low level input current (2)	I_{IL2}	C1—C3, R1—R4, V_{DD}=2.4V, V_{IL2}=V_{SS}		90	200	—	μA
High level output current	I_{OH}	$\overline{DP}$, $\overline{MUTE}$ V_{DD}=2.4V, V_{OH}=2.0V		0.45	1.4	—	mA
Low level output current	I_{OL}	$\overline{DP}$, $\overline{MUTE}$ V_{DD}=2.4V, V_{OL}=0.8V		1.0	5	—	mA

●AC Electrical Characteristics

(Common to STC2570C and STC2571C) (f_{OSC}=32.768kHz, Ta=25°C, V_{SS}=0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Key input ON time	T_{on}	Excl. chattering time	21.0	—	—	msec
Key input OFF time	T_{off}	Excl. chattering time	3.42	—	—	msec
Allowable noise pulse width of key input pin	T_n	Width of one noise pulse	—	—	15.38	msec
Key judgement time	T_{kj1}	Normal dialing	33.73	33.75	33.77	msec
	T_{kj2}	Redialing or repertory dialing	26.90	26.92	26.94	
	T_{kj3}	Access pause cancelled	24.77	25.63	26.49	
	T_{kj4}	Writing to repertory memory	10.37	25.63	40.90	
Mute delay time	T_{md}	— *1	—	9.83	—	msec
Redial memory write time	T_{mw}	— *1	—	0.85	—	msec
Rate of data transfer to repertory memory	T_{dt}	— *1	—	3.42	—	msec/digit
Dial pulse transfer rate	DR	DRS=V_{SS} *1	—	9.752	—	pps
		DRS=V_{DD} *1	—	19.505	—	
Inter-digit pause	IDP	DRS=V_{SS} (10pps) *1	—	615.2*2/820.3*3	—	msec
		DRS=V_{DD} (20pps) *1	—	461.4*2/410.2*3	—	
Oscillation start time	T_{os}	V_{DD}=1.8V, CI≦40kΩ	—	500	—	msec
Voltage deviation of oscillation frequency	$\Delta f/f$	V_{DD}=1.3 to 2.0V	−6	—	+6	ppm/0.1V
		V_{DD}=2.0 to 6.0V	−10	—	+10	ppm/V

(STC2570C only)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Time difference between two keys when pressed at a time	T_{dk1}	When call disconnected (*,#)	—	—	8.54	msec
Dial pulse make/break ratio	M/B	M/$\overline{B}$=V_{SS} *1	—	1/2	—	—
		M/$\overline{B}$=V_{DD} *1	—	2/3	—	

(STC2571C only)

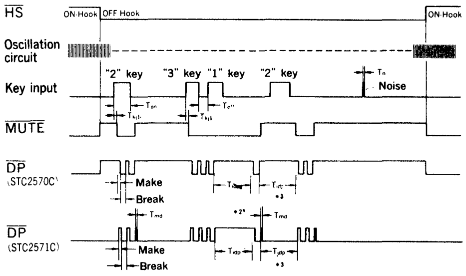
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Dial pulse make/break ratio	M/B	— *1	—	1/2	—	—
Hooking time	T_{hk}	— *1	—	499.02	—	msec
Auto access pause	T_{ap}	— *1	—	3.589	—	sec
Keying confirmation tone ON time	T_{kt}	Valid key input *1	—	26.49	—	msec
Keying confirmation tone frequency	f_{kt}	Valid key input *1	—	910.22	—	Hz

*1 All specifications take constant values logically.
The deviation is only a change of the oscillation frequency.

*2 STC2570C$_{OA}$ and STC2571C$_{OA}$
*3 STC2570C$_{OB}$ and STC2571C$_{OB}$

●Timing Chart

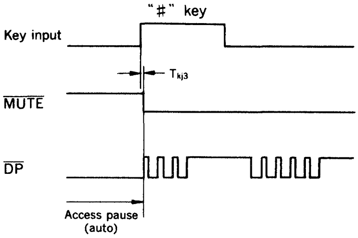
○ Normal dialing (DP mode) *2, *3



*2 If a key is pressed earlier than the transmission of a dial pulse, the MUTE continues on until all dial pulses corresponding to the buffered key input data have been transmitted.

3 The inter-digit pause stays valid even if a key is pressed immediately after the last dial pulse has been transmitted. As system assumes that dial pulses are being transmitted during the inter-digit pause, entry of the "" key is ignored.

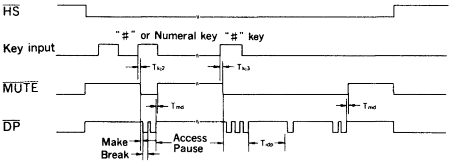
○ Access pause (auto pause)*4, *5
STC2571C



*4 Even in the normal dialing mode, pressing the "#" key causes an auto pause. The timing diagram for this operation is the same as in the redialing or repertory dialing.

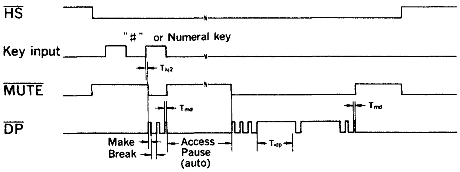
*5 Clearing the auto pause (common to normal dialing, redialing and repertory dialing)

○ Redialing or repertory dialing *6
STC2570C



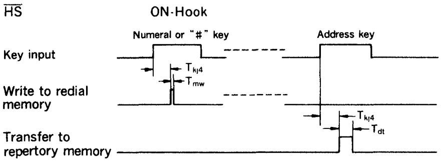
*6 During mixed dialing (e.g., redialing+normal, or repertory+normal), the inter-digit pause stays valid even if a key is pressed immediately after the last dial pulse of redialing or repertory dialing has been transmitted. As system assumes that dial pulses are being transmitted during the inter-digit pause, entry of any key is ignored.

○ Redialing or repertory dialing*7
STC2571C



*7 During mixed dialing (e.g., redialing+normal, or repertory+normal), the inter-digit pause stays valid even if a key is pressed immediately after the last dial pulse of redialing or repertory dialing has been transmitted. As system assumes that dial pulses are being transmitted during the inter-digit pause, entry of any key is ignored.

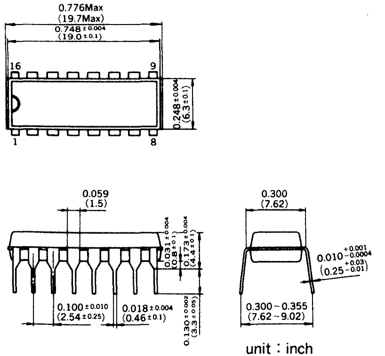
○ Registration to repertory memory
STC2570C/STC2571C



■PACKAGE DIMENSIONS

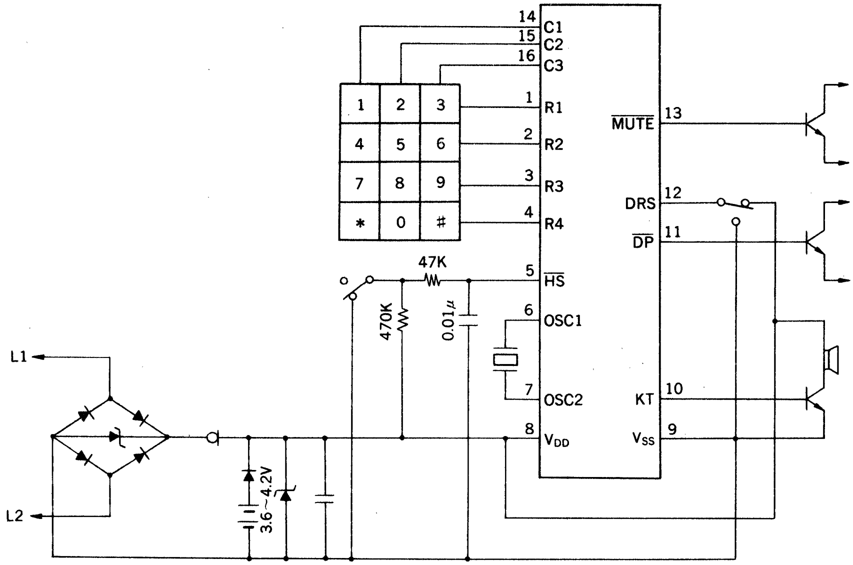
C16

16-pin DIP



unit : inch
(mm)

■EXAMPLE OF APPLICATION



STC2580C$_{0C}$ Series

CMOS TONE/PULSE DIALER

- **DTMF/Pulse Output Swich**
- **Low Distortion**
- **Ten 18-digit Repertory Memoies and 24-digit Redial Memory**

DESCRIPTION

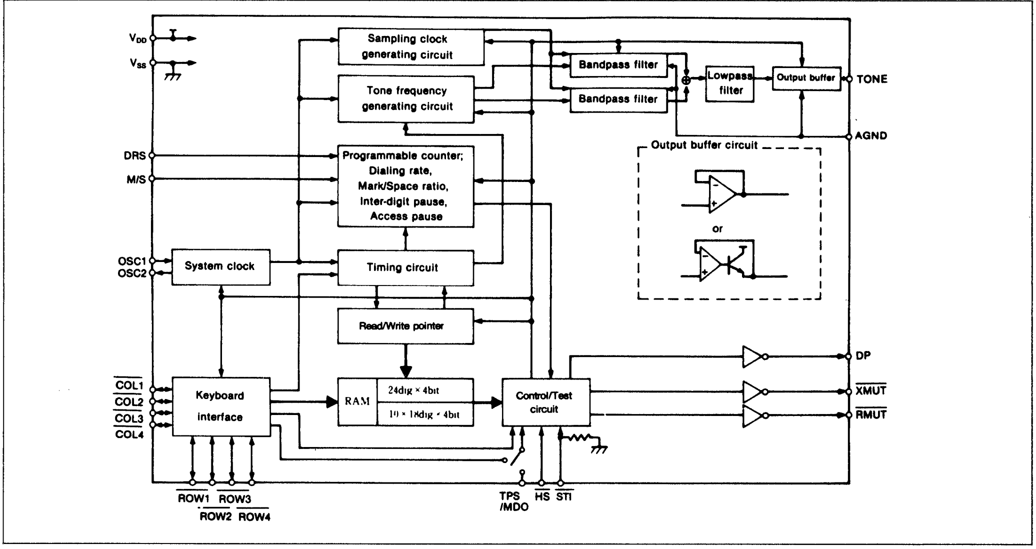
The STC2580C$_{0C}$ series is a CMOS LSI which is provided with a memory for telephone numbers, and can selectively output either dual tone multi-frequency (DTMF) signals or a dialing pulse (DP) train.

The LSI contains Band Pass Filters (BPF) and smoothing filter by switched capacitor filter (SCF) technology, so that the DTMF output has less distortion than the DA conversion system used in a conventional tone dialer. It also incorporates an emitter-follower NPN transistor, enabling the DTMF output to directly drive a telephone line. By connecting the minimum necessary interface circuit, the dialing pulse output can also drive a telephone line.

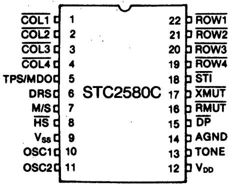
FEATURES

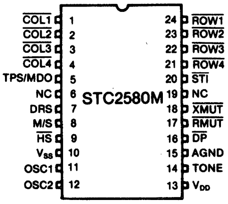
- Low-voltage operation and low power dissipation due to CMOS process.
- A built-in SCF-type BPF makes possible a DTMF signal with low THD (typically 2.5% at 5 V) without the use of external filters.
- The LSI contains redialing memory for a 24-digit numbers and repertory memory for ten 18-digit numbers which can be used in either the tone or pulse mode.
- DP mode : Permits selection of dialing pulse rate (10/20 pps) and mark/space ratio (40/60, 33.3/66.6). (The inter-digit pause is fixed for each dialing rate ··········617.9 ms for 10 pps or 463.4 ms for 20 pps.)
- DTMF mode ···Make=93.1 ms and inter-digit pause=61.4 ms.
- When sending to an external line, the access pause can be set to auto pause (3.97s) using the pause key. This function can also be canceled during sending.
- This LSI can be connected to a standard 2 of 8 keyboard.
- The built-in reference signal generator requires only an inexpensive and easily-obtainable 3.58 MHz crystal oscillator for the TV color burst signal.
- Package···22-pin DIP (plastic) / 24-pin SOP (plastic)

BLOCK DIAGRAM



■PIN CONFIGURATION





■PIN DESCRIPTION

Pin name	Pin No.		Functions
	STC2580C	STC2580M	
$\overline{\mathrm{ROW4}}$-$\overline{\mathrm{ROW1}}$	19—22	21—24	[Scanning input/output of matrix keyboard] Keys are selected by short-circuiting ROW and COL.
$\overline{\mathrm{COL1}}$-$\overline{\mathrm{COL4}}$	1—4	1—4	
TPS*¹/MDO	5	5	[TPS : DTMF/DP mode select input] (for STC2585C to STC2588C) In this case, $\boxed{\mathrm{T/P}}$ on the keypad is an invalid input. [MDO : DTMF/DP mode display output] (for STC2581C to STC2584C) Outputs whether the DTMF or DP mode has been selected using $\boxed{\mathrm{T/P}}$ key.
DRS*¹	6	7	[Pulse rate select input in DP mode] Ignores input switching performed during a pulse output (including auto dialing) as well as inputs made in the DTMF mode. The inter-digit pause is fixed for each pulse rate.
M/S*¹	7	8	[Pulse mark/space ratio in DP mode] Like DRS, this pin ignores inputs made during a pulse output or in the DTMF mode. OFF-Hook : V_{SS} level
$\overline{\mathrm{HS}}$*¹	8	9	[Hook switch] Determines the ON/OFF status of the hook switch.
V_{SS}	9	10	[Power supply terminal (−)]
CSC1	10	11	These pins are connected across the terminals of a 3.579545 MHz crystal oscillator which is used for the reference signal generator.
OSC2	11	12	
V_{DD}	12	13	[Power supply terminal (+)]
TONE	13	14	[DTMF signal output] This pin enables either an NPN emitter-follower output or a CMOS OP-Amp output to be selected.
AGND	14	15	[Grounding point output of analog circuit (SCF section)] By connecting a capacitor to this point, the level is stabilized.
$\overline{\mathrm{DP}}$	15	16	[Dialing pulse output] While the dialing pulse is not output, the output level is V_{SS} during ON-Hook and V_{DD} during OFF-Hook.
$\overline{\mathrm{RMUT}}$	16	17	[Receiver mute output] This output is valid in the DP mode. In the DTMF mode, muting is not applied. The level of this pin is : DP mode : During mute or ON-Hook → V_{SS} level DTMF mode : During ON-Hook → V_{SS} level ; During OFF-Hook → V_{DD} level.
$\overline{\mathrm{XMUT}}$	17	18	[Transmitter mute output] Mute signal for transmitter usable in both the DP mode and the DTMF mode. During mute or ON-Hook status → V_{SS} level
$\overline{\mathrm{STI}}$*²	18	20	[Single tone generating mode select] The single tone generating mode is selected by applying the V_{DD} level. To generate a single tone for $\overline{\mathrm{COL1}}$, $\overline{\mathrm{COL2}}$, or $\overline{\mathrm{COL3}}$, press two or three keys in the corresponding column simultaneously, and to generate a single tone for $\overline{\mathrm{ROW1}}$, $\overline{\mathrm{ROW2}}$, $\overline{\mathrm{ROW3}}$, or $\overline{\mathrm{ROW4}}$, press the two keys of $\overline{\mathrm{COL1}}$ and $\overline{\mathrm{COL2}}$ in the corresponding row simultaneously.
NC		6, 19	[No connection]

*1 Because DRS, M/S, $\overline{\mathrm{HS}}$, and TPS are open pins, be sure to apply V_{DD} or V_{SS} from outside the LSI.

*2 Pin $\overline{\mathrm{STI}}$ is connected to a built-in pull-down resistor which puts the LSI in the single tone inhibit mode during normal use, even when the pin is open. To provide noise immunity, however, it is recommended that this pin be fixed at V_{SS} level externally.

■STC2580C$_{OC}$ SERIES

Type *¹	Write to repertory memory	DTMF output *²	Tone/pulse output selection	Type *¹	Write to repertory memory	DTMF output *²	Tone/pulse output selection
STC2581C$_{OC}$	OFF Hook	Bip	Key	STC2585C$_{OC}$	OFF Hook	Bip	External pin
STC2582C$_{OC}$	ON Hook	Bip	Key	STC2586C$_{OC}$	ON Hook	Bip	External pin
STC2583C$_{OC}$	OFF Hook	CMOS	Key	STC2587C$_{OC}$	OFF Hook	CMOS	External pin
STC2584C$_{OC}$	ON Hook	CMOS	Key	STC2588C$_{OC}$	ON Hook	CMOS	External pin

*1 This LSI can also be provided in a mini-flat package. In this case, C becomes M (e.g. STC2581M). The characteristics are same as those of the DIP type.

*2 This is the CMOS OP-Amp output or Bipolar emitter-follower output.

■ABSOLUTE MAXIMUM RATINGS

($V_{SS}=0V$)

Parameter	Symbol	Ratings	Unit
Power supply voltage	V_{DD}	−0.3 to 7.5	V
Input voltage	V_I	−0.3 to $V_{DD}+0.3$	V
Output voltage	V_O	−0.3 to $V_{DD}+0.3$	V
Operating temperature	T_{opr}	−20 to 70	℃
Storage temperature	T_{stg}	−65 to 150	℃
Soldering temperature and time	T_{sol}	260℃, 10s (at lead)	—

■ELECTRICAL CHARACTERISTICS

●DC Characteristics

($V_{SS}=0V$, Ta = −20 to 70℃)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Operating voltage	V_{DD}	DP mode		1.5	—	6.0	V
		DTMF mode		2.5	—	6.0	
Data retention voltage	V_{DDR}	$\overline{HS}=V_{DD}$		1.0	—	6.0	V
Average operating current	I_{DDA}	$V_{DD}=5.0V$ $\overline{HS}=V_{SS}$ $\overline{DP}$, TONE, $\overline{RMUT}$, $\overline{XMUT}$ and MDO not loaded	Key input stand-by status	—	—	800	μA
			in DP mode dial pulse being output	—	—	1.0	mA
			in DTMF mode DTMF signal being output	—	—	8.0	mA
Data retention current	I_{DDR}	$V_{DD}=1.0V$, $\overline{HS}=V_{DD}$, $\overline{STI}=V_{SS}$, TPS = DRS = M/S = V_{DD} or V_{SS}		—	—	0.75	μA
High level input voltage	V_{IH}	TPS, DRS, M/S, $\overline{HS}$, $\overline{STI}$		$V_{DD}-0.4$	—	V_{DD}	V
Low level input voltage	V_{IL}	TPS, DRS, M/S, $\overline{HS}$, $\overline{STI}$		V_{SS}	—	$V_{SS}+0.4$	V
High level input voltage (1)	I_{IH1}	TPS, DRS, M/S, $\overline{HS}$, $V_{DD}=5.0V$, $V_{IH1}=V_{DD}$		—	—	0.1	μA
High level input voltage (2)	I_{IH2}	STI, $V_{DD}=5.0V$, $V_{IH2}=V_{DD}$		—	—	300	μA
Low level input current	I_{IL1}	TPS, DRS, M/S, $\overline{HS}$, $\overline{STI}$, $V_{DD}=5.0V$, $V_{IL1}=V_{SS}$		—	—	0.1	μA
Low level input current	I_{IL2}	$\overline{COL1}$−$\overline{COL4}$, $\overline{ROW1}$−$\overline{ROW4}$, $V_{DD}=5.0V$, $V_{IL2}=V_{SS}$		10	23	50	μA
High level output current (Source)	I_{OH1}	$\overline{DP}$, $\overline{XMUT}$, $\overline{RMUT}$, MDO $V_{DD}=5.0V$, $V_{OH1}=4.0V$		4.0	—	—	mA
Low level output current (Sink)	I_{OL2}	$\overline{DP}$, $\overline{XMUT}$, $\overline{RMUT}$, MDO $V_{DD}=5.0V$, $V_{OL2}=0.5V$		4.0	—	—	mA

●AC Characteristics

($V_{SS}=0V$, $Ta=25°C$, $f_{OSC}=3.579545MHz$)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Key input ON effective period	t_{ON1} *1	DP and DTMF mode non-normal dialing	Excluding chattering	15.45	—	—	ms
	t_{ON2} *2	DTMF mode normal dialing		77.24	—	—	
Key input OFF effective period	t_{OFF}	Excluding chattering		1.72	—	—	ms
Pulse width of allowable noise at input terminal	t_N			—	—	14.37	ms
Oscillator start-up time	t_{OS}	$V_{DD}=5.0V$ $Cl<100\Omega$		—	—	2.0	ms
Key judgement time	t_{Kj1}	DP mode normal dialing		30.25	30.90	31.97	ms
	t_{Kj2}	DTMF mode normal dialing		17.37	18.02	19.10	
	t_{Kj3}	DP/DTMF mode auto dialing*3		19.95	20.60	21.67	
Pre-mute time	t_{MP1}	DTMF mode normal dialing		—	9.01	—	ms
	t_{MP2}	DTMF mode auto dialing		—	9.87	—	
Mute delay time	t_{MD1}	DP and DTMF mode auto dialing		—	9.87	—	ms
	t_{MD2}	DTMF mode normal dialing		9.22	9.33	9.44	
Dial pulse mark/space	—	$M/S=V_{DD}$		—	40/60	—	—
	—	$M/S=V_{SS}$		—	33.3/66.6	—	
Dial pulse rate	—	$DRS=V_{DD}$		—	19.42	—	pps
	—	$DRS=V_{SS}$		—	9.71	—	
Inter-digit pause	t_{IDP1}	DP mode	Dial rate=19.42pps	—	463.4	—	ms
			Dial rate=9.71pps	—	617.9	—	
	t_{IDP2}	DTMF mode auto dialing		—	61.36	—	
DTMF make time	t_{TM}	DTMF mode auto dialing		—	93.12	—	ms
Auto access pause	t_{AP}			—	3.965	—	s
Oscillator frequency	f_{OSC}			—	3.579545	—	MHz
Oscillator frequency/voltage variance	$\Delta f/f$	$V_{DD}=1.5$ to $6.0V$		—	—	30	ppm/v
Tone output voltage (single tone)	V_{TONE}	$\overline{COL}$	$V_{DD}=5.0V$	—	−10	—	dBm
		$\overline{ROW}$	Operational amplifier load=10 Kohms; Bipolar transistor load=120 ohms	—	−11	—	
COL-ROW tone output voltage ratio*4	d_{BCR}	$V_{DD}=3.0$ to $6.0V$		—	—	2	dB
Tone distortion	$\%_{DIS}$	$V_{DD}=2.5V$		—	—	7.0	%
Tone output frequency	f_{R1}	$\overline{ROW1}$		—	699.13	—	Hz
	f_{R2}	$\overline{ROW2}$		—	766.17	—	
	f_{R3}	$\overline{ROW3}$		—	847.43	—	
	f_{R4}	$\overline{ROW4}$		—	947.97	—	
	f_{C1}	$\overline{COL1}$		—	1215.88	—	
	f_{C2}	$\overline{COL2}$		—	1331.68	—	
	f_{C3}	$\overline{COL3}$		—	1471.85	—	
Minimum assured key detection time	t_{MOP}	$t_{ON1}<t_{MOP}$ Excluding chattering		42.91	44.63	46.35	ms

*1 Key input ON effective time
When writing data to the repertory memory while in ON-Hook status (STC2582C, STC2584C, STC2586C, and STC2588C), it is necessary to add the oscillator starting time to the effective time t_{ON3}. $t_{ON3}=t_{ON1}+t_{OS}$ (no key chattering)

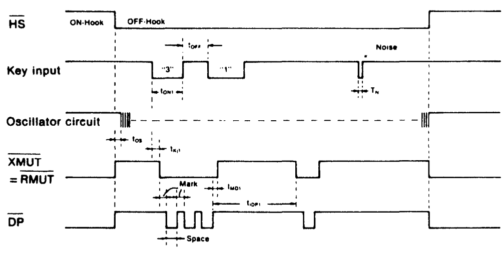
*2 Key input ON effective time (DTMF mode normal dialing)
This is the key read time + mute time + NTT engineering reference signal sending time of 50 ms.

*3 Auto dialing
Indicates redialing and repertory dialing.

*4 COL-ROW tone output voltage ratio
The output gain of COL is higher than that of ROW.

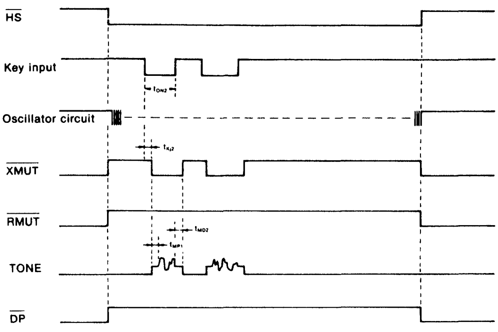
●Timing Chart

○Normal dialing (DP mode)

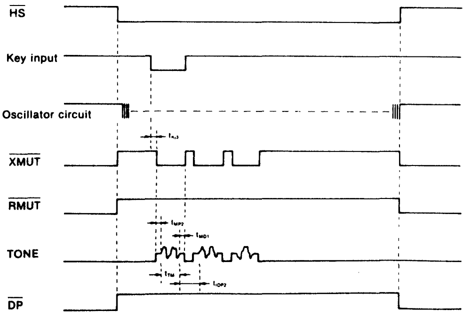


TONE---High Impedance

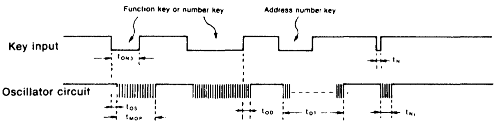
○Normal dialing (DTMF mode)



○Redialing and repertory dialing (DTMF mode)



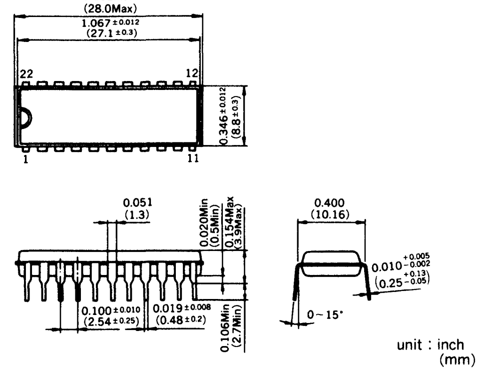
○Storage in repertory memory in ON-Hook mode (STC2582C, STC2584C, STC2586C, STC2588C)



■PACKAGE DIMENSIONS

C22

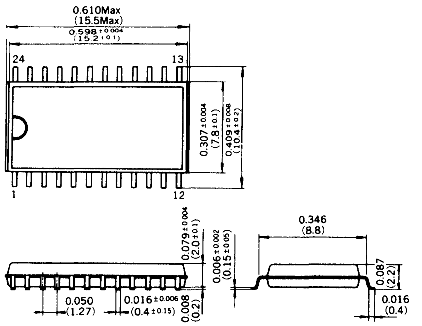
22-pin DIP



unit : inch
(mm)

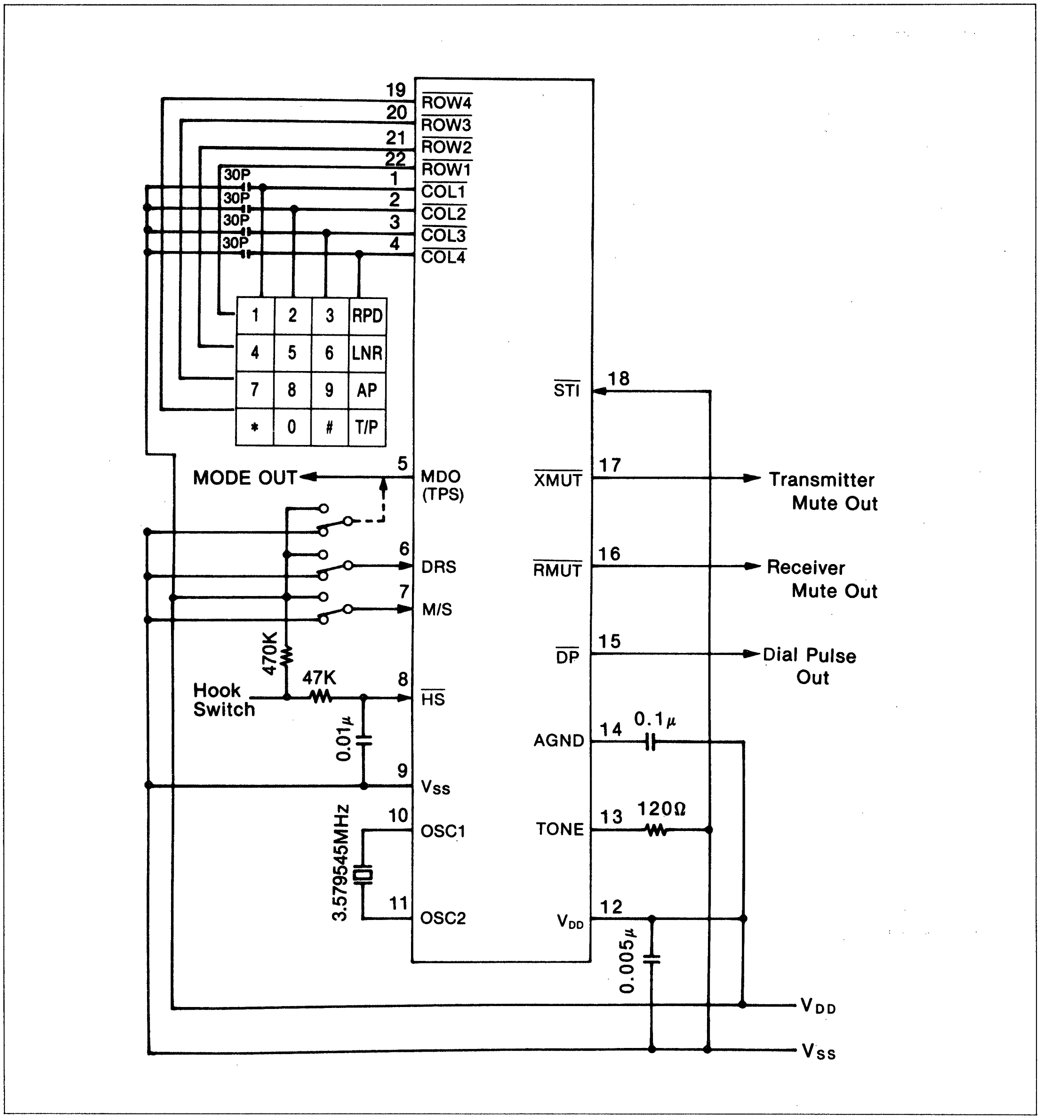
M24

24-pin SOP



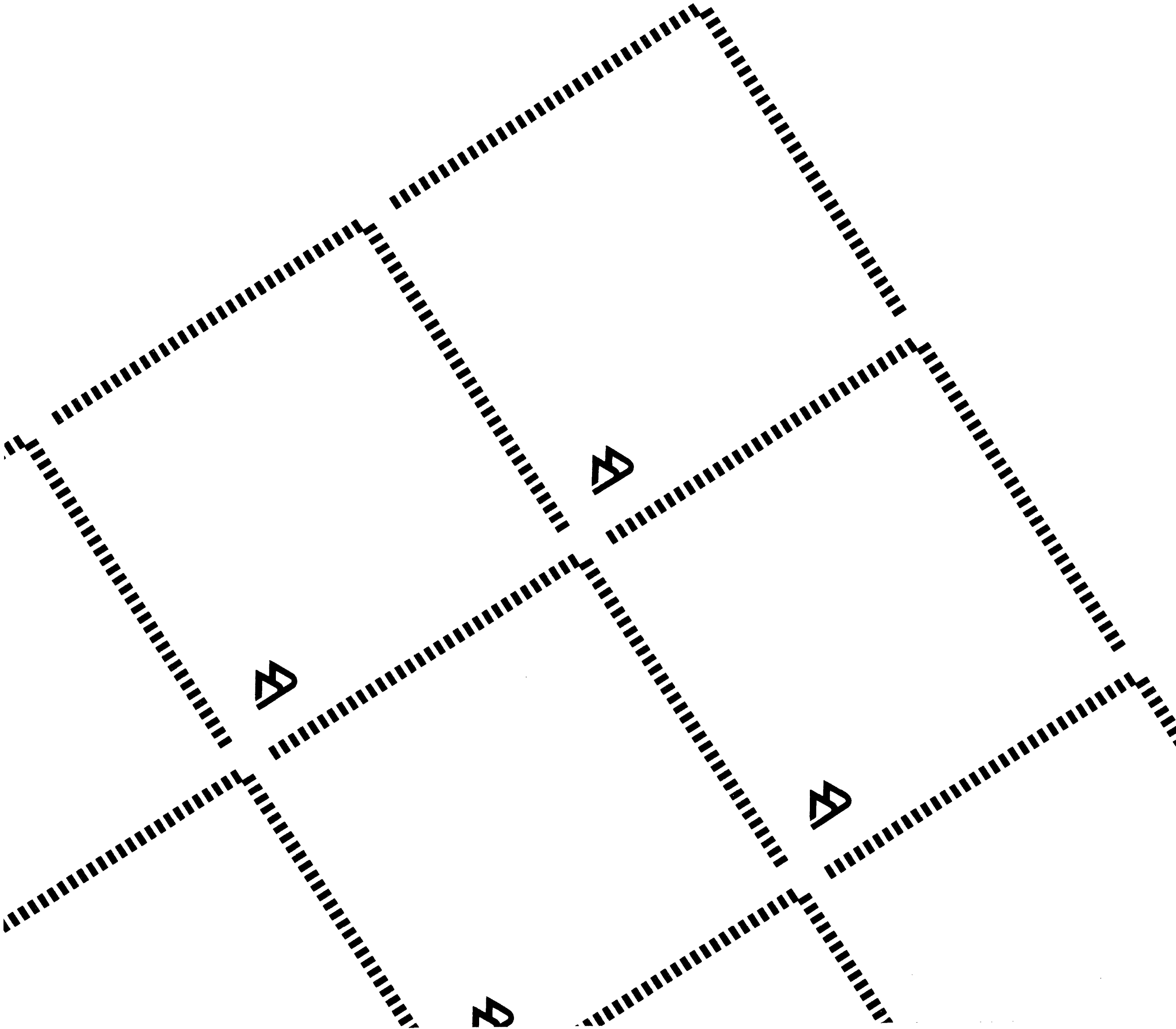
unit : inch
(mm)

■EXAMPLE OF APPLICATIONS



1988/1989 CMOS DATA BOOK

G. MELODY ICs



▷ MELODY IC TABLE*

Series	Type No.	Maximum Number of Tunes (Number of note)	Tune Selection		Accompaniment	Preamplifier(internal)	BUSY END Signal	Transducer			Envelope		Oscillation		Tune mode			Power Supply			Package	Note
			Binary Code	Serial Trigger				Dynamic SP	Magnetic	Piezo	External CR	Digital Envelope	CR self	External Clock	Level hold	One-shot	Stop	1.5V	3V	5V	pin (DIP)	
	7910 series #	2 (128)	○	—	○	○	—	○	—	—	○	—	○	○	☆		—	○	○	—	16	•High quality tone •2 Alarms(pinpon/pipipi) •Dynamic SP Drive
	7920 series	1 (64)	—		—	—	—	○	—	—	○	—	☆		☆		—	○	○	—	8	•Dynamic SP Drive (External)
	7930 series	1 (64)	—		—	○	—	○	—	—	○	—	☆		☆		—	○	○	—	14	•Dynamic SP Drive
SVM7940 Series	SVM7940	8 (512)	—	○	—	—	—	—	○	○	—	—	—	○	○	—	—	○	○	—	16	•Multi melody type •High impedance transducer drive
	SVM7941														—	○	○					
	SVM7942												○	—	○	—	—					
	SVM7943														—	○	○					
	SVM7944	4 (512)	○	—									—	○	○	—	—					
	SVM7945														—	○	○					
	SVM7946												○	—	○	—	—					
	SVM7947														—	○	○					
SVM7950 Series	SVM7950	1 (64)	—		—	○	—	—	○	○	—	—	—	○	○	—	—	○	○	—	16	•High impedance transducer drive
	SVM7951														—	○	○					
	SVM7952							○	—	—	○				○	—	—					
	SVM7953														—	○	○					
	SVM7954							—	○	○	—		○	—	○	—	—					
	SVM7955														—	○	○					
	SVM7956							○	—	—	○				○	—	—					
	SVM7957														—	○	○					
SVM7960 Series	SVM7960	4 (127)	○	—	○	○	○	○	—	—	○	—	—	○	○	—	—				16	•High quality tone •Dynamic SP Drive •1.5(V)/5(V) *1 Address start
	SVM7961														—	○						
	SVM7962												○	—	○	—						
	SVM7963														—	○						
	SVM7964	3 (127)	*1										—	○	○	—						
	SVM7965														—	○						
	SVM7966												○	—	○	—						
	SVM7967														—	○						
SVM7970 Series	SVM7970	8 (640)	—	○	○	○	○	○	—	—	☆		—	○	*3		○	☆			18	•Multi melody type •High quality tone •Dynamic SP Drive •1.5(V)/5(V) *2 Binary coder plus serial trigger *3 Selectable at each tune
	SVM7971												○	—								
	SVM7972	8 (640)	○	—									—	○								
	SVM7973												○	—								
	SVM7974	11 (640)	*2										—	○								
	SVM7975												○	—								
SVM7990 Series	SVM7990	8 (512)	—	○	—	○	—	○	—	—	○	—	—	○	○	—	—	○	○	—	16	•Multi melody type •Dynamic SP Drive
	SVM7991														—	○	○					
	SVM7992												○	—	○	—	—					
	SVM7993														—	○	○					
	SVM7994	4 (512)	○	—									—	○	○	—	—					
	SVM7995														—	○	○					
	SVM7996												○	—	○	—	—					
	SVM7997														—	○	○					
SVM7900 Series #	SVM7900	1 (64)	—		—	—	—	—	○	○	—	—	—	○	○	—	—	○	○	—	8	•High impedance transducer drive *4 OSC. resistor is built in (Mask option)
	SVM7901														—	○						
	SVM7902												*4 ○	—	○	—						
	SVM7903														—	○						

☆Mask option   # Ongoing user service product   (Continue)

*Minimum melody IC order is 100,000 pieces. Please consult S-MOS for specific availability.

Type No.		Maximum Number of Tunes (Number of note)	Tune Selection		Accompaniment	Preamplifier(internal)	BUSY END Signal	Transducer			Envelope		Oscillation		Tune mode		Stop	Power Supply			Package	Note
			Binary Code	Serial Trigger				Dynamic SP	Magnetic	Piezo	External CR	Digital Envelope	CR self	External Clock	Level hold	One-shot		1.5V	3V	5V	pin (DIP)	
SVM7800 Series	SVM7800	1 (63)	—		—	—	—	—	○	○	—	—	○	—	○ *5		—	○	○	—	8	•High impedance transducer drive ***5 Level hold or** one shot pin selection *6 One shot retrigger function
	SVM7801												—	○								
	SVM7802												○	—								
	SVM7803												—	○								
	SVM7804												○	—								
	SVM7805												—	○								
	SVM7806												○	—	—	○	○					
	SVM7807												—	○								
	SVM7808												○	—		○ *6						
	SVM7809												—	○								
SVM7820 Series	SVM7820	1 (63)	—		—	—	—	—	○	○	—	—	○	—	○ *7		—	—	○	—	—	•LED drive •High impedance transducer drive *7 Level hold or one shot pin selection *8 One shot retrigger function
	SVM7821												—	○								
	SVM7822												○	—								
	SVM7823												—	○								
	SVM7824												○	—								
	SVM7825												—	○								
	SVM7826												○	—	—	○	○					
	SVM7827												—	○								
	SVM7828												○	—		○ *8						
	SVM7829												—	○								
SVM7860 series	SVM7860	1 (127)	—		○	—	—	○	—	—	○	—	○	—	○	—	—	☆			8	•High quality tone •Dynamic SP Drive (External)
	SVM7861												—	○								

☆ Mask option

▷STANDARD MELODY LIST

Code No.	Song Title
7910C	Holdilidia
7910E	Two Minuets
	Dark eyebrows
7910G	Melodia A
	Melodia B
7910I	Home on the range
	Green Sleeves
7910K	lullaby (two songs)
7910N	Musunde Hiraite
	Cho-cho
∗79100	Westminster (two tunes)
∗7910P	Westminster (accompaniment)
7910Q	Wiegenlied (Brahms)
	Rock a bye Baby
7910CE	Nocturne
	Minuet
7910T	Jingle Bells
7910CF	For Elise
	A maiden's prayer
7910CG	Romance de Amor
	Petrouchka
★7910CH	Westminster
	Ave Maria
★7910CM	Westminster
	Whittington
7910CN	Holdilidia
	Home on the range
7910CP	Silent lake-side
	Mountain Musician
7910CQ	Mary's little lamb
	De camptown races
7910CR	Lorelei
	Landler tanz
7910CS	Amaryllis
	Symphony ♯ 40 (Mozart)
7910CU	Jingle Bells
	Silent night
7910CV	Joy to the world
	The first noel
7910CW	O Tannenbaum
	Frosty the snow man
7920A	The cuckoos waltz
7920B	Home sweet home
7920C	Jingle Bells
★7920M	Wedding march
★7920Q	Victory Song
7920AH	Wiegenlied (Brahms)
7930B	Home sweet home
7930C	Holdilidia
7930D	Lorelei
★7930E	Westminster
7930GA	Yurikago no uta
7930GB	Jingle Bells
7930GC	We wish you a merry X'mas
7930GD	Rudolph, the red-nosed Reindeer
7930GE	For Elise
7942COT	Holdilidia
	Minuet (Bach)
	Green Sleeves
	Symphony ♯ 40 (Mozart)
	Home on the range
	Silent lake-side
	Mountain Musician
	Happy birthday to you
☆7943COE	Green Sleeves
	De camptown races
	For Elise

Code No.	Song Title
☆7943COE	Romance de amor
	O sole mio
	Die Lorelei
	The cuckoos waltz
	Old folk at home
☆7943COS	Spring
	Hymne a Lamour
	La Mer
	Farandolles
	Yesterday
	L' eau Vive
	O Tannenbaum
	Symphony ♯ 40 (Mozart)
☆7943CON	Hymne a lamour
	Santa lucia
	Hey Jude
	L'eau Vive
	Romance de amor
	Yesterday
	Happy birthday to you
	Wedding march
7942DAN	Jingle Bells
	Joy to the world
	O Tannenbaum
	We wish you a Merry X'mas
	Silent Night
	The First Noel
	Frosty the snow man
	Rudolph the red nosed reindeer
7950COB	Les ferilles mortos
7950COD	Blue bell of Scotland
7950COF	Yodel
7950COH	Cantate ♯ 147 (Bach)
☆7951COC	Mexican hat dance
☆7951COQ	Cantate ♯ 147 (Bach)
7952COG	Cantate ♯ 147 (Bach)
7954CAR	Green Sleeves
☆7955COJ	O'sole mio
☆7955COL	Happy birthday to you
☆7955COX	Saint go'in march'in in
☆7955COY	Music box dancer
☆7955CAF	Mountain Musician
☆7955CAN	Jingle Bells
☆7955CBC	Wedding March
7962COA	Green Sleeves
	Home on the range
	Ding Dong
	Two Minuets
7975COB	Landler tanz
	Amaryllis
	Home on the range
	Green Sleeves
	For Elise
	A maiden's prayer
	Mountain Musician
	Yodel
	Ding Dong
	Beep sound
	Westminster
7992COA	X'mas song medley (8 tunes)
☆7993COC	Green Sleeves
	De camptown races
	For Elise
	Romance de amor
	O sole mio
	Lorelei
	The cuckoos waltz

Code No.	Song Title
☆7993COC	Mountain Musician
7993CON	Westminster
	A maiden's prayer
	For Elise
	Romance de amor
	Amaryllis
	Symphony ♯ 40 (Mozart)
	Dark eyebrows
	De camptown races
7993DAC	Yellow Rose of Texas-Dixie Land
	Stars and Stripes forever-Anchors Awaign
	She wore a yellow ribbon-Twinkle twinkle little star
	London Bridge is falling down-Mountain musician
	Row row row a boat-It's a small world
	Home sweet home-Wiegenlied
7993DAE	Rudolph, The red nosed reindeer-Santa Claus is coming to town
	We wish you a Merry X'mas-Frosty the snow man
	Jingle Bells-Silent Night
	Joy to the world-The first Noel
	O christmas tree-Hark the herald Angels sing
	O tannenbaum-Oh little town of Bethlehem
7902COA	X'mas song medley. Red nosed reindeer. O Tannenbaum Jingle bells.
⍟7903COB	Happy birthday
✪7903COC	Wedding March
★7903COE	Happy birthday
★7903COG	Hymne a lamour
☆7903COH	The Alphabet Song
☆7903COJ	Rock a bye Baby
☆7903COK	Old Macdonald Had a Farm
✪7903COS	Mountain Musician
★7903COY	Jingle Bells
★7903CAA	Love me tender
★7903CAB	Love Story
★7903CAC	Wedding March
★7903CAE	Congratulations
★7903CAH	Silent Night
★7903CAL	Saint go'in march'in in
★7903CAN	Jingle bells, Red nosed reindeer, Joy to the world.
★7903CAP	Music box dancer
★7903CAR	Wedding march (Long version)
★7903CAS	Let me call you my Sweet heart
☆7903CBA	Jingle Bells.
☆7903CBB	Silent Night
☆7903CBN	Hymne a lamour
★7903CBP	Mother of mine
☆7903DBQ	Happy birthday
☆7903DBR	Music box dancer
☆7903DBS	Wedding March
☆7903DBT	Jingle Bells, Red Nosed Reindeer, Joy to the world
☆7903DBY	For Elise
7902DCF	Christmas song medley
★7903DCK	Easter Paradise
7902DCS	Rock A bye baby
★7903DCT	Santa Claus is coming to town
★7903DCV	The First Noel
★7903DCY	When you wish up on a star
★7903DEA	You light up my life
★7903DEB	Wargner's Wedding March
7902DEC	Christmas Medley
☆7903DEH	Congratulation

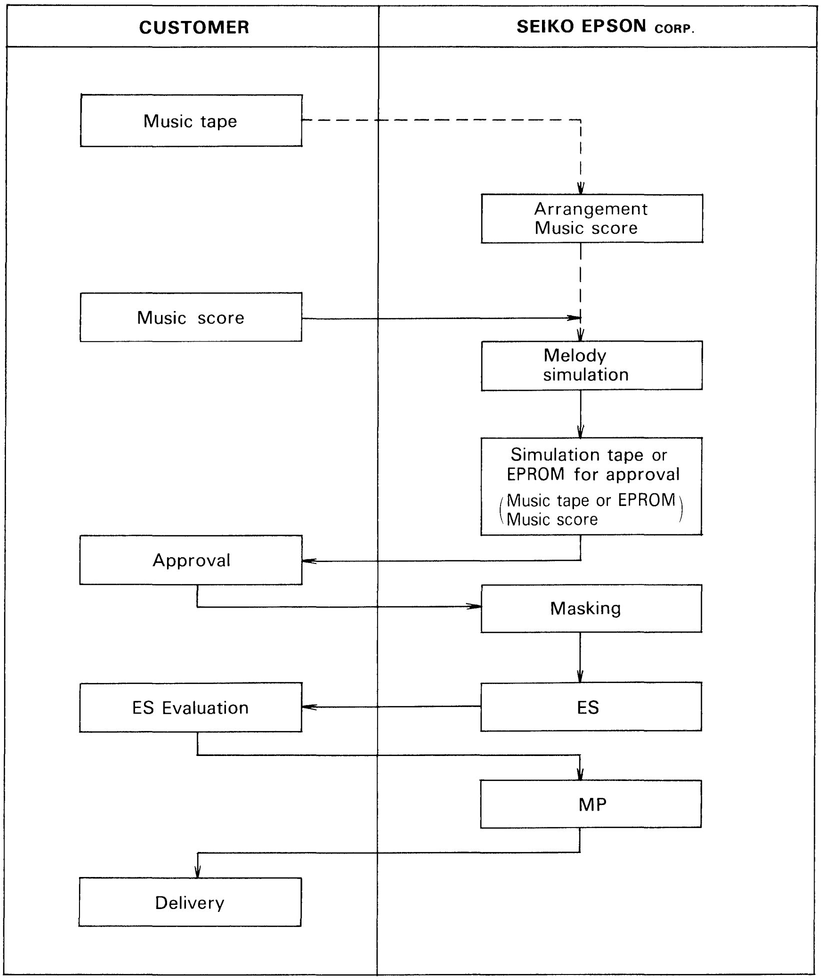
∗Type 7910P will be used as accompaniment with type 79100.
Note : 7910 Series and SVM7900 Series are ongoing user service products.

☆One shot mode. (A type)
★One shot mode (B type)
⍟,✪OSC, resistor is not included on IC

▷STANDARD MELODY LIST

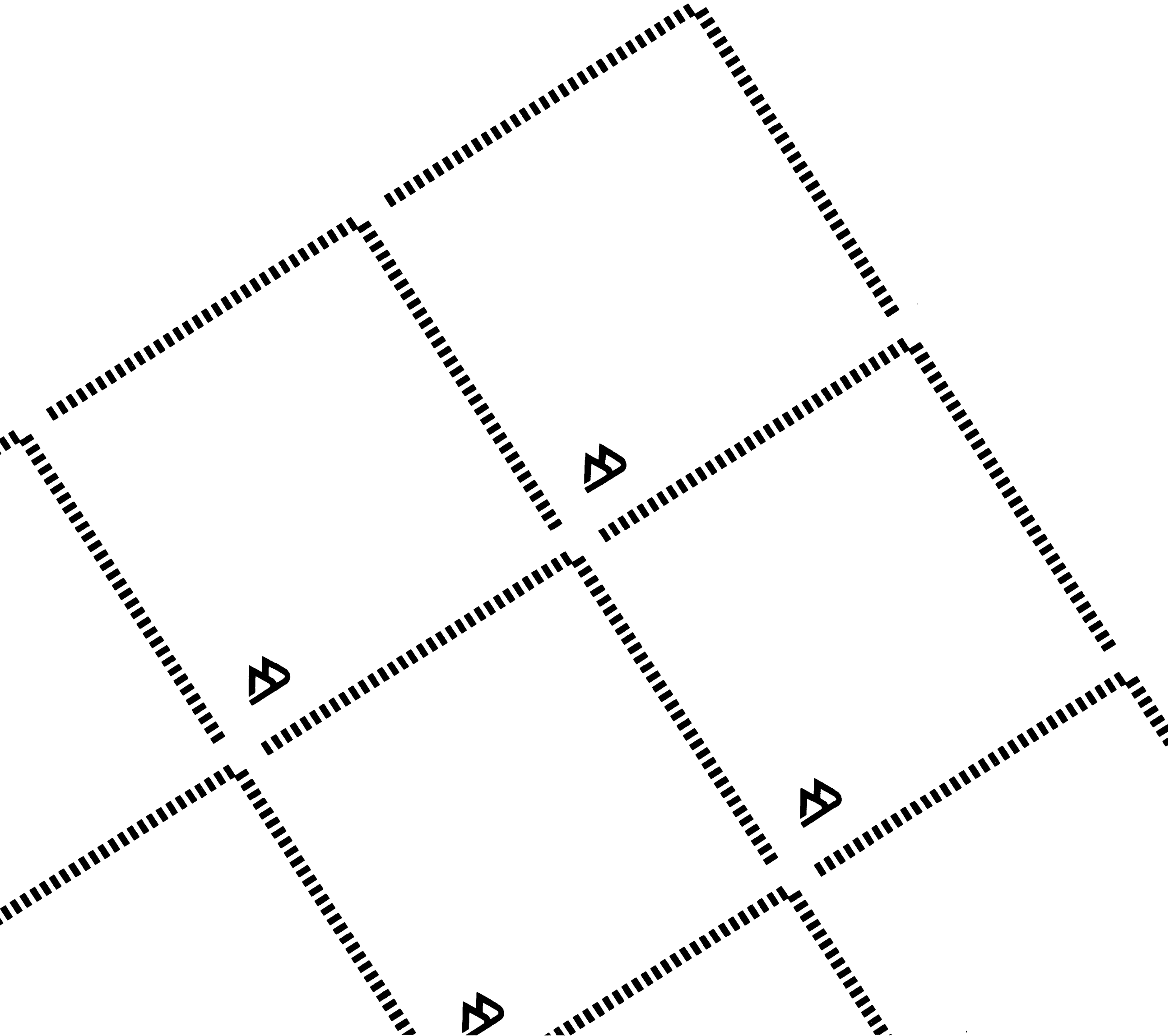
Code No	Song Title	Code No	Song Title	Code No	Song Title
7800DCS	Silent Night	7820DSB	Jingle Bells Medley		
7800DCT	Rock a Bye Baby	7820DSC	Music Box Dancer		
7800DCV	If You Love Me	7820DSE	Jingle Bells		
7800DCY	Brahms' Lullaby	7820DSF	Silver Bells		
7800DEA	Love Story	7820DSG	It's a Small World		
7800DEB	Happy Birthday to You	7820DSH	Over The Rainbow		
7800DEC	Jingle Bells	7820DSJ	Easter Parade / Peter Cottontail		
7800DEN	Old Macdonald				
7800DEP	Twinkle Twinkle Little Star				
7800DEQ	Romance D'amor				
7800DER	White Christmas				
7800DES	Wedding March (Wagner)				
7800DET	Wedding March (Mendelssohn)				
7800DEV	You are my Sunshine				
7800DFB	O Tannenbanm / Silent Night				
7800DFC	Silver Bells				
7800DFF	Aure Lee				
7800DFG	Let me call you my sweet heart				
7800DFL	Mary Had a Little Lamb				
7800DFP	Jesus Loves Me				
7800DFT	Yesterday				
7800DFV	Music Box Dancer				
7800DFY	My Way				
7800DGA	Easter Parade / Peter Cottontail				
7800DGB	Love Me Tender / Let Me Call You My Sweet	7860CSB	Nocturne		
7802DFE	For Elise	7860CSC	Minuet		
		7860CSE	Home on the Range		
		7860CSF	Green Sleeves		
		7860CSG	The Entertainer		
		7860CSH	Lorelei		
		7860CSK	For Elise		
		7860C6C	Tableaux d'une Exposition(Promenade)		
		7860C6E	Je te Veux		
		7860C6F	The Jewels of the Madonna		
		7860C6G	When I'm Sixty–four		
		7860C6H	Minuet (Boccherini)		

MELODY IC DESIGN FLOW



1988/1989 CMOS DATA BOOK

H. SUB-ASSEMBLIES



SHB2112B$_{1A/1B}$

CMOS 1M-BIT HYBRID STATIC RAM

- ●Low Supply Current
- ●Access Time 100ns
- ●131,072 Words × 8 Bits Asynchronous

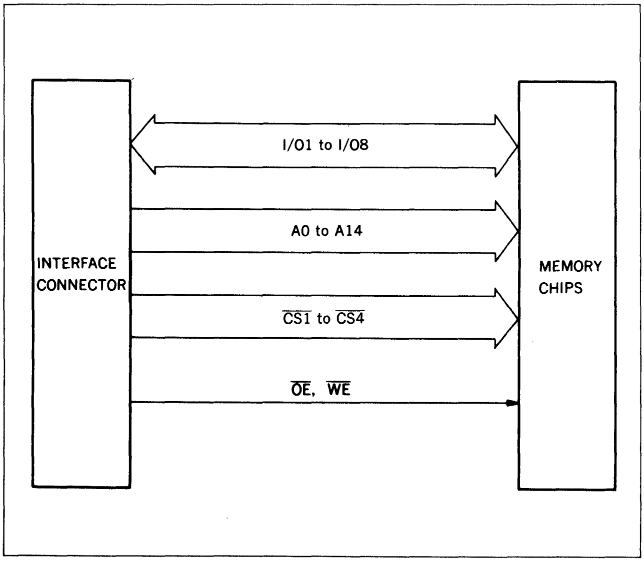
■DESCRIPTION

The SHB2112B$_{1A/1B}$ is a 131,072-word × 8-bit hybrid LSI module with four 256K SRAM (SRM20256LM). With low power consumption, the module can be used with applications which require a battery back-up. Since it is a static device, it does not requires a clock or refresh circuitry. The I/O control provides 3-state output, for data bus connection. These features provide solutions for a wide variety of applications, including microcomputers and other peripheral equipments.

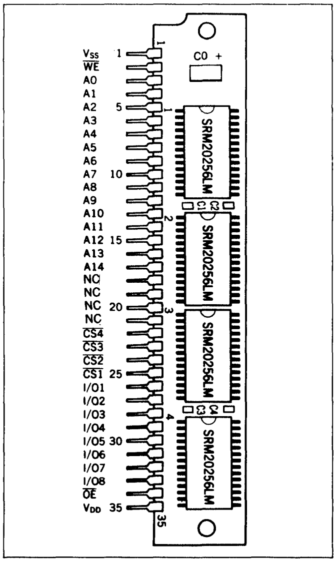
■FEATURES

- ●Hybrid CMOS LSI
- ●131,072-word × 8-bit memory density
- ●Mounting 4 pcs. of 256K static RAM (SRM20256LM$_{10}$)
- ●Access time 100ns Max.
- ●Single power supply-5volt
- ●Printed-circuit-board (PCB) size 17.5mm × 101.6mm × 4.77mm (except pins)
- ●PCB……SHB 2112B$_{1A}$ 35-pin SIP (Single inline package)
  SHB 2112B$_{1B}$ 35-pin SIM (Single inline module)

■BLOCK DIAGRAM



■PIN CONFIGURATION



■PIN DESCRIPTION

Pin name	Pin No.	Functions
V_{SS}	1	Grounding pin. This GND is common in signal.
$\overline{WE}$	2	<Write Enable> Data write signal line (negative logic). Data is written to the memory module at the positive edge of $\overline{WE}$. When $\overline{WE}$ is "H", this module is read operation.
A0 to A14	3 to 17	<Address Input> 15-bit address input pin. (Positive logic)
NC	18 to 21	<No connection>
$\overline{CS1}$ $\overline{CS2}$ $\overline{CS3}$ $\overline{CS4}$	25 24 23 22	<Chip Select> These signal line (negative active) are module select line. These line should be selected each one at read and write operation. Each $\overline{CS}$ is available for each 32kB RAM. That is to say, 128kB is divide by 4 $\overline{CS}$ signal. EX. Data will be valid to read and write when $\overline{CS1}$ is "L" and $\overline{CS2}$ to $\overline{CS4}$ are "H". If $\overline{CS1}$ to $\overline{CS4}$ are "H", this module is non-selected mode (I_{DD} is stand-by mode)
I/O1 to I/O8	26 to 33	<Data I/O> Inputs or outputs 8-bit of data. This pin provides an input with $\overline{WE}$ low and an output with $\overline{WE}$ high. Also, it has low impedance with $\overline{OE}$ low and high impedance with $\overline{OE}$ high.
$\overline{OE}$	34	<Output Enable> Data read signal line (negative logic) from equipment to the memory module. As Data I/O terminals are hi-impedance when $\overline{OE}$="H", the contention of data memory output bus can be avoided.
V_{DD}	35	Positive power supply pin. (5V±10%) Normally, 5V is supplied.

■ABSOLUTE MAXIMUM RATINGS

($V_{SS}=0V$)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.5 to 7.0	V
Input voltage	V_I	−0.5* to 7.0	V
I/O voltage	$V_{I/O}$	−0.5* to V_{DD}+0.3	V
Operating temperature	T_{opr}	0 to 70	℃
Storage temperature	T_{stg}	−40 to 100	℃
Soldering temperature and time	T_{sol}	260℃, 10s (Lead only)	—

* V_I, $V_{I/O}$ (Min.) = −1.0V at pulse width less than 50ns

■DC RECOMMENDED OPERATING CONDITIONS

($V_{SS}=0V$, Ta=0 to 70℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
	V_{SS}		0	0	0	V
Input voltage	V_{IH}		2.4	—	V_{DD}+0.3	V
	V_{IL}		−0.3*	0	0.8	V

* V_{IL} (Min.) = −1.0V at pulse width less than 50ns

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

(V_{DD}=5V±10%, V_{SS}=0V, Ta=0 to 70℃)

Parameter	Symbol	Conditions	Min	Typ*	Max	Unit
Input leakage current	I_{LI}	V_I=0 to V_{DD}	−2	—	2	μA
Stand-by supply current	I_{DDS}	$\overline{CS1}$ to CS4=V_{IH} Non-selected	—	6	12	mA
	I_{DDS1}	$\overline{CS1}$ to $\overline{CS4}$≥V_{DD}−0.2V, V_I=V_{DD}−0.2V or 0.2V	—	—	400	μA
Average operating current	I_{DDA}	V_I=V_{IL}, V_{IH} $I_{I/O}$=0mA t_{cyc}=Min	—	60	75	mA
Output leakage current	I_{LO}	$\overline{CS1}$ to $\overline{CS4}$=V_{IH} or $\overline{WE}$=V_{IL} or $\overline{OE}$=V_{IH} $V_{I/O}$=0 to V_{DD}	−2	—	2	μA
High level output voltage	V_{OH}	I_{OH}=−1.0mA	2.4	—	—	V
Low level output voltage	V_{OL}	I_{OL}=2.1mA	—	—	0.4	V

* Ta=25℃, V_{DD}=5.0V

●Terminal Capacitance

(f=1MHz, Ta=25℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C_I		—	—	50	pF
Input/output capacitance	$C_{I/O}$		—	—	50	pF

● AC Electrical Characteristics

○ Read cycle

(V_{DD}=5V±10%, V_{SS}=0V, Ta=0 to 70°C)

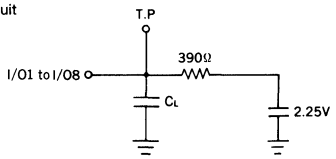
Parameter	Symbol	Conditions	Min	Max	Unit
Read cycle time	t_{RC}	*1	100	—	ns
Address access time	t_{ACC}		—	100	ns
$\overline{CS}$ access time	t_{ACS} *3		—	100	ns
$\overline{OE}$ access time	t_{OE}		—	55	ns
$\overline{CS}$ output set time	t_{CLZ} *3		10	—	ns
$\overline{CS}$ output floating time	t_{CHZ} *3	*2	—	40	ns
$\overline{OE}$ output set time	t_{OLZ}	*1	5	—	ns
$\overline{OE}$ output floating time	t_{OHZ}	*2	—	40	ns
Output hold time	t_{OH}	*1	10	—	ns

○ Write cycle

(V_{DD}=5V±10%, V_{SS}=0V, Ta=0 to 70°C)

Parameter	Symbol	Conditions	Min	Max	Unit
Write cycle time	t_{WC}	*1	100	—	ns
Chip select time	t_{CW} *3		90	—	ns
Address valid time	t_{AW}		90	—	ns
Address setup time	t_{AS}		0	—	ns
Write pulse width	t_{WP}		75	—	ns
Address hold time	t_{WR}		0	—	ns
Input data setup time	t_{DW}		45	—	ns
Input data hold time	t_{DH}		0	—	ns
$\overline{WE}$ output floating time	t_{WHZ}	*2	—	40	ns
$\overline{WE}$ output setup time	t_{OW}	*1	10	—	ns

*1 Test Conditions
1. Input pulse level: 0.6V to 2.4V
2. t_r=t_f=10ns
3. Input and output timing reference levels: 1.5V
4. Output load: C_L=100pF
5. Output load: C_L=100pF (Include scope & jig capacitance)
6. Circuit



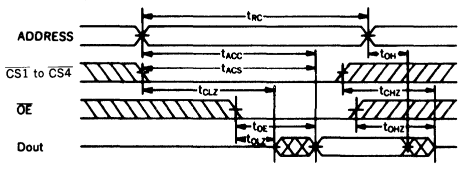
C_L = (Include jig capacitance)

*2 t_{CHZ}, t_{OHZ}, t_{WHZ} Test Conditions
1. Input pulse level: 0.6V to 2.4V
2. t_r=t_f=10ns
3. Input timing reference levels: 1.5V
4. Output timing reference levels: ±200V (the level displaced from stable output voltage level)

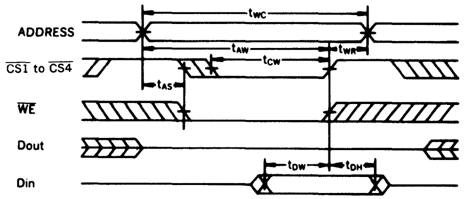
*3 $\overline{CS1}$ to $\overline{CS4}$

● Timing Chart

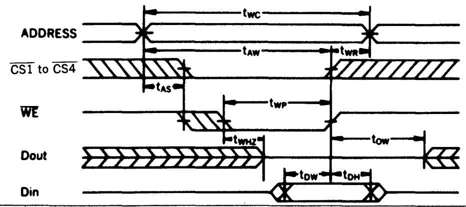
○ Read Cycle *1



○ Write Cycle 1 ($\overline{CS1}$ to $\overline{CS4}$ Control) *2



○ Write Cycle ($\overline{WE}$ Control) *3



*1 During read cycle time, $\overline{WE}$ should be high.

*2 During write cycle that is controlled by $\overline{CS1}$ to $\overline{CS4}$, the output buffer changes to high impedance. $\overline{CS1}$ to $\overline{CS4}$ should be selected each one at read and write operation.

*3 During write cycle that is controlled by $\overline{WE}$, the output buffer changes to high impedance. ($\overline{OE}$="H")

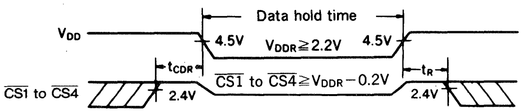
DATA RETENTION CHARACTERISTICS WITH LOW VOLTAGE POWER SUPPLY

$V_{SS}=0V$, $Ta=0$ to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDR}	$\overline{CS1}$ to $\overline{CS4} \geqq V_{DDR}-0.2V$	2.2	—	5.5	V
Data retention current	I_{DDR}	$V_{DDR}=3.0V$, $\overline{CS1}$ to $\overline{CS4} \geqq V_{DDR}-0.2V$ $V_I=V_{DDR}-0.2V$ or $0.2V$	—	—	200	μA
Chip select data hold time	t_{CDR}		0	—	—	ns
Operating recovery time	t_R		t_{RC}*	—	—	ns

*t_{RC} = Read cycle time

Data retention timing ($\overline{CS1}$ to $\overline{CS4}$ Control)



NOTE : When retaining data in stand-by mode the supply voltage can be lowered within a certain range.
The read or write cycle are disabled when the supply voltage is low.

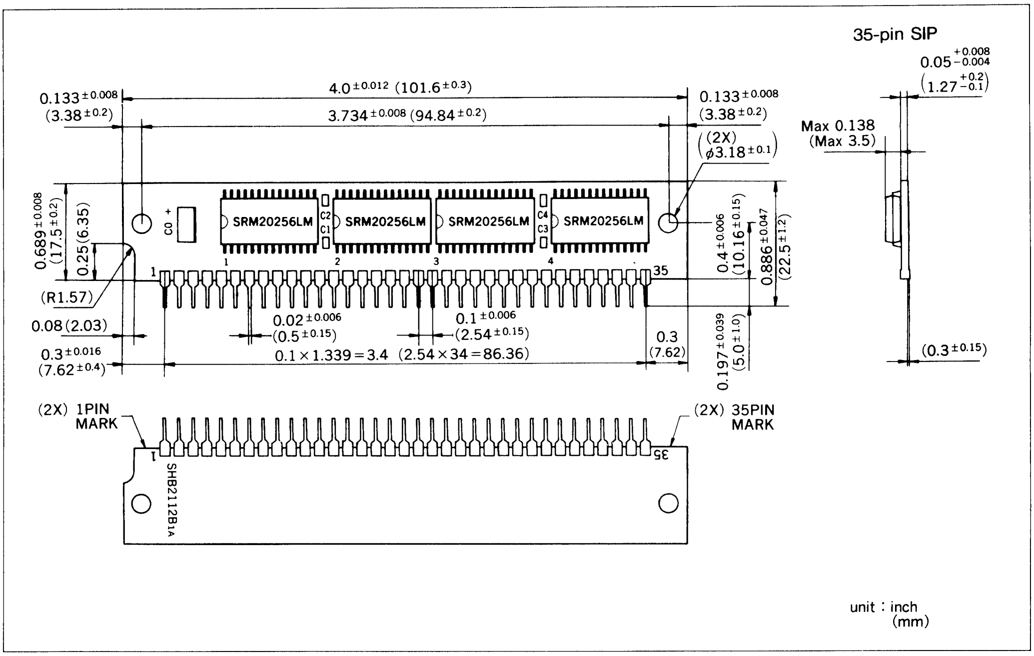
FUNCTION

●Truth Table

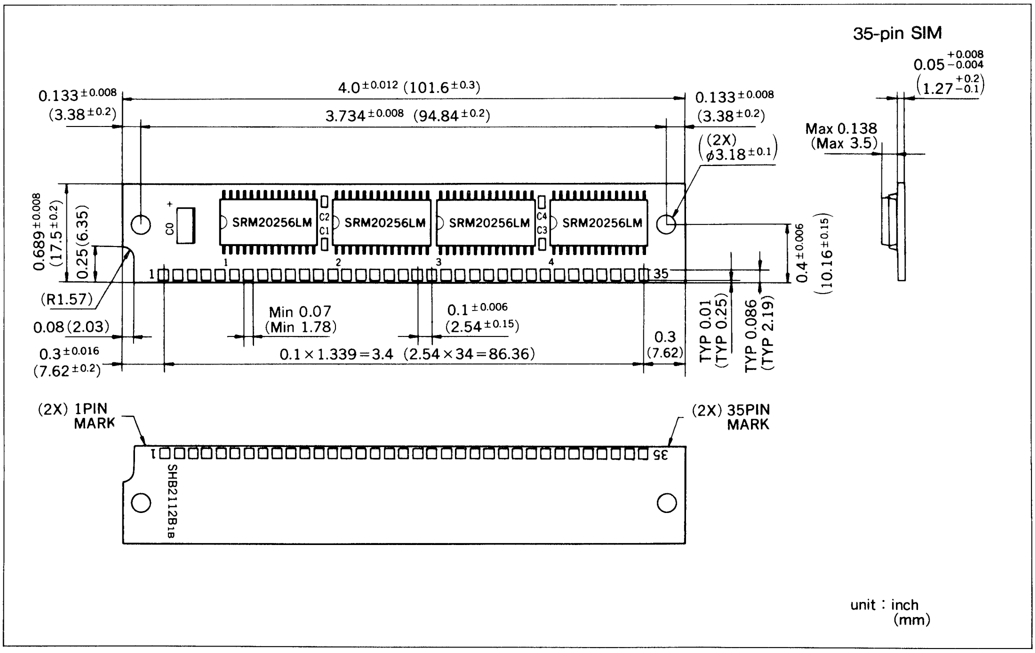
$\overline{CS1}$ to $\overline{CS4}$ *	$\overline{OE}$	$\overline{WE}$	A0 to A14	DATA I/O	MODE	I_{DD}
H	×	×	×	Hi-Z	Not selected	I_{DDS}, I_{DDS1}, I_{DDR}
Stable *	×	L	Stable	Data in	Write	I_{DDA}
Stable *	L	H	Stable	Data out	Read	I_{DDA}
Stable *	H	H	Stable	Hi-Z	Output disable	I_{DDA}

× : "H" or "L"
* : These lines should be selected each one at read and write operation.

■PACKAGE DIMENSIONS



SHB 2112B1A



SHB 2112B1B

■CHARACTERISTICS CURVES

Under measurement

SHB2212B$_{1A/1B}$

CMOS 1M-BIT HYBRID STATIC RAM

- ●Low Supply Current
- ●Access Time 120ns
- ●131,072 Words × 8 Bits Asynchronous
- ●Included Decoder

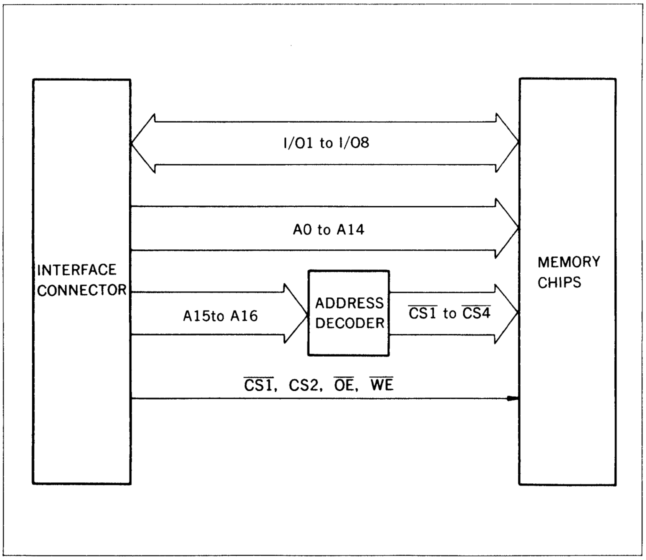
■DESCRIPTION

The SHB2212B$_{1A/1B}$ is a 131,072-word × 8-bit hybrid LSI module with four 256K SRAM (SRM20256LM) and a 3-8Line decoder. With low power consumption, the module can be used with applications which require a battery back-up. Since it is a static device, it does not requires a clock or refresh circuitry. The I/O control provides 3-state, output, for data bus connection. These features provide solutions for a wide variety of applications, including microcomputers and other peripheral equipments.

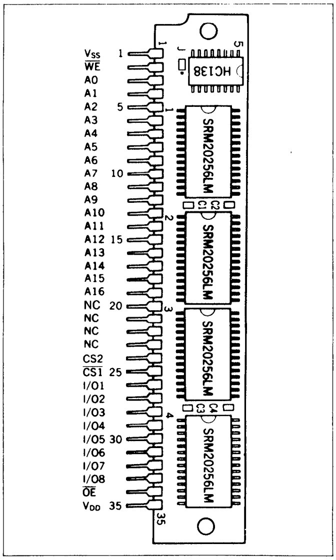
■FEATURES

- ●Hybrid CMOS LSI (with address decoder)
- ●131,072-word × 8-bit memory density
- ●Mounting 4 pcs. of 256K static RAM (SRM20256LM$_{10}$)
- ●3-8 line decoder
- ●Access time 120ns (Max.)
- ●Single power supply-5volt
- ●3-State output, with wired-or capability
- ●Printed-circuit-board (PCB) size 17.5mm × 101.6mm × 8.27mm (except pins)
- ●PCB ··················SHB 2212B$_{1A}$ 35 pin SIP (Single inline package)
  SHB 2212B$_{1B}$ 35 pin SIM (Single inline module)

■BLOCK DIAGRAM



■PIN CONFIGURATION



PIN DESCRIPTION

Pin name	Pin No.	Functions
V_{SS}	1	Grounding pin. This GND is common in signal.
$\overline{WE}$	2	<Write Enable> Data write signal line (negative logic). Data is written to the memory module at the positive edge of $\overline{WE}$. When $\overline{WE}$ is "H", this module is read operation.
A0 to A16	3 to 19	<Address Input> 17-bit address input pin. (Positive logic)
NC	20 to 23	<No Connection>
$\overline{CS1}$ CS2	25 24	<Chip Select> Memory module select signal line. Data is valid to read and write when $\overline{CS1}$ is "L" (negative logic) and CS2 is "H" (positive logic). When $\overline{CS1}$ is "H" or CS2 is "L" level, the module is in the non-selected mode. (I_{DD} is stand-by mode.)
I/O1 to I/O8	26 to 33	<Data I/O> 8-bit bi-directional data signal bus. (Positive logic) This bus carries data for transfer between the equipment and the memory module.
$\overline{OE}$	34	<Output Enable> Data read signal line (negative logic) from the equipment to the memory module. As Data I/O terminals are hi-impedance when $\overline{CS1}$ = "L", CS2 = "H", $\overline{OE}$ = "H", the contention of data memory output bus can be avoided.
V_{DD}	35	Positive power supply pin. (5V ± 10%) Normally, 5V is supplied.

ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.5 to 7.0	V
Input voltage	V_I	−0.5* to 7.0	V
I/O voltage	$V_{I/O}$	−0.5* to V_{DD}+0.3	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−40 to 100	°C
Soldering temperature and time	T_{sol}	260°C, 10s (Lead only)	—

* V_I, $V_{I/O}$ (Min.) = −1.0V at pulse width less than 50ns

DC RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0V, Ta = 0 to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
	V_{SS}		0	0	0	V
Input voltage	V_{IH}		3.85*2 2.4*3	—	V_{DD}+0.3	V
	V_{IL}		−0.3*1	0	0.8	V

*1 V_{IL} (Min.) = −1.0V at pulse width less than 50ns *2 A15, A16, $\overline{CS1}$, CS2 *3 Others except A15, A16, $\overline{CS1}$, CS2

ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

(V_{DD} = 5V ± 10%, V_{SS} = 0V, Ta = 0 to 70°C)

Parameter	Symbol	Conditions	Min	Typ*	Max	Unit
Input leakage current	I_{LI}	V_I = 0 to V_{DD}	−2	—	2	μA
Stand-by supply current	I_{DDS}	$\overline{CS1}$ = V_{IH}, CS2 = V_{IL} Non-selected	—	—	7	mA
	I_{DDS1}	$\overline{CS1} \geq V_{DD}-0.2V$, $CS2 \leq 0.2V$, $V_I = V_{DD}-0.2V$ or 0.2V	—	—	400	μA
Average operating current	I_{DDA}	V_I = V_{IL}, V_{IH} $I_{I/O}$ = 0mA t_{cyc} = Min	—	65	80	mA
Output leakage current	I_{LO}	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = 0 to V_{DD}	−2	—	2	μA
High level output voltage	V_{OH}	I_{OH} = −1.0mA	2.4	—	—	V
Low level output voltage	V_{OL}	I_{OL} = 2.1mA	—	—	0.4	V

* Ta = 25°C, V_{DD} = 5.0V

●Terminal Capacitance

(f = 1MHz, Ta = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C_I		—	—	50	pF
Input/output capacitance	$C_{I/O}$		—	—	50	pF

●AC Electrical Characteristics

○Read cycle

($V_{DD}=5V\pm10\%$, $V_{SS}=0V$, Ta=0to70°C)

Parameter	Symbol	Conditions	Min	Max	Unit
Read cycle time	t_{RC}	*1	120	—	ns
Address access time	t_{ACC}		—	120	ns
$\overline{\text{CS1}}$ access time	t_{ACS1}		—	120	ns
CS2 access time	t_{ACS2}		—	120	ns
$\overline{\text{OE}}$ access time	t_{OE}		—	65	ns
$\overline{\text{CS1}}$ output set time	t_{CLZ1}		10	—	ns
$\overline{\text{CS1}}$ output floating time	t_{CHZ1}	*2	—	65	ns
CS2 output set time	t_{CLZ2}	*1	10	—	ns
CS2 output floating time	t_{CHZ2}	*2	—	65	ns
$\overline{\text{OE}}$ output set time	t_{OLZ}	*1	5	—	ns
$\overline{\text{OE}}$ output floating time	t_{OHZ}	*2	—	65	ns
Output hold time	t_{OH}	*1	10	—	ns

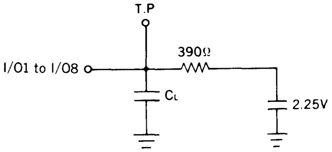
○Write cycle

($V_{DD}=5V\pm10\%$, $V_{SS}=0V$, Ta=0to70°C)

Parameter	Symbol	Conditions	Min	Max	Unit
Write cycle time	t_{WC}	*1	120	—	ns
Chip select time ($\overline{\text{CS1}}$)	t_{CW1}		100	—	ns
Chip select time (CS2)	t_{CW2}		100	—	ns
Address valid time	t_{AW}		100	—	ns
Address setup time	t_{AS}		10	—	ns
Write pulse width	t_{WP}		90	—	ns
Address hold time	t_{WR}		10	—	ns
Input data setup time	t_{DW}		60	—	ns
Input data hold time	t_{DH}		10	—	ns
$\overline{\text{WE}}$ output floating time	t_{WHZ}	*2	—	65	ns
$\overline{\text{WE}}$ output setup time	t_{OW}	*1	10	—	ns

*1 Test Conditions

1. Input pulse level: 0.4V to 3.85V······$\overline{\text{CS1}}$, CS2, A15, A16
   0.6V to 2.4V ······Other except $\overline{\text{CS1}}$, CS2, A15, A16
2. $t_r=t_f=10ns$
3. Input and output timing reference levels: 1.5V
4. Output load: $C_L=100pF$
5. Output load: $C_L=100pF$ (Include scope & jig capacitance)
6. Circuit



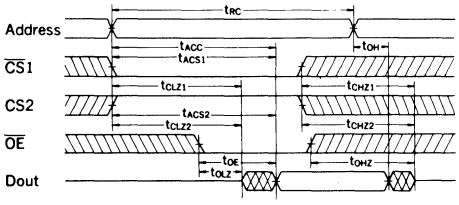
$C_L=100pF$ (Include jig capacitance)

*2 t_{CHZ}, t_{OHZ}, t_{WHZ} Test Conditions

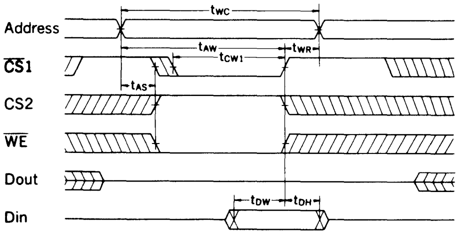
1. Input pulse level: 0.4V to 3.85V······$\overline{\text{CS1}}$, CS2, A15, A16
   0.6V to 2.4V ······Other except $\overline{\text{CS1}}$, CS2, A15, A16
2. $t_r=t_f=10ns$
3. Input and output timing reference levels: 1.5V
4. Output timing reference levels: ± 200mV (the level displaced from stable output voltage level)

● Timing Chart

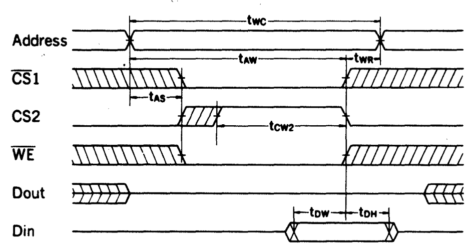
○ Read Cycle*1



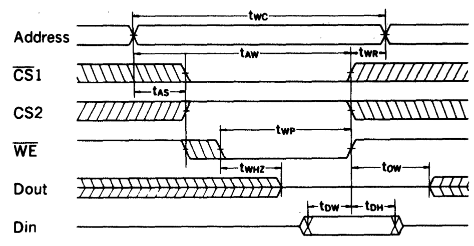
○ Write Cycle 1 ($\overline{\text{CS1}}$ Control)*2



o Write Cycle 2 (CS2 Control)*3



o Write Cycle 3 ($\overline{WE}$ Control)*4



*1 During read cycle time, $\overline{WE}$ should be high.
*2 During write cycle that is controlled by $\overline{CS1}$, the output buffer changes to high impedance.
*3 During write cycle that is controlled by CS2, the output buffer changes to high impedance.
*4 During write cycle that is controlled by $\overline{WE}$, the output buffer changes to high impedance. ($\overline{OE}$="H")

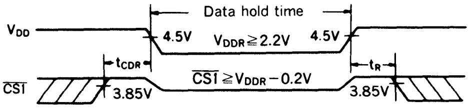
■DATA RETENTION CHARACTERISTICS WITH LOW VOLTAGE POWER SUPPLY

($V_{SS}=0V$, Ta=0 to 70°C)

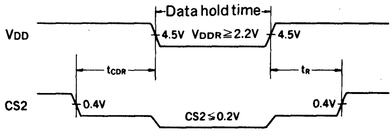
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDR}	$\overline{CS1} \geq V_{DDR}-0.2V$ or $CS2 \leq 0.2V$	2.2	—	5.5	V
Data retention current	I_{DDR}	$V_{DDR}=3V$, $\overline{CS1} \geq V_{DDR}-0.2V$, or $CS2 \leq 0.2V$, $V_I=V_{DDR}-0.2V$ or 0.2V	—	—	240	μA
Chip select data hold time	t_{CDR}		30	—	—	ns
Operating recovery time	t_R		t_{RC}*	—	—	ns

*t_{RC}=Read cycle time

Data retention timing ($\overline{CS1}$ Control)



Data retention timing 2 (CS2 Control)



NOTE : When retaining data in stand-by mode the supply voltage can be lowered within a certain range. The read or write cycle are disabled when the supply voltage is low.

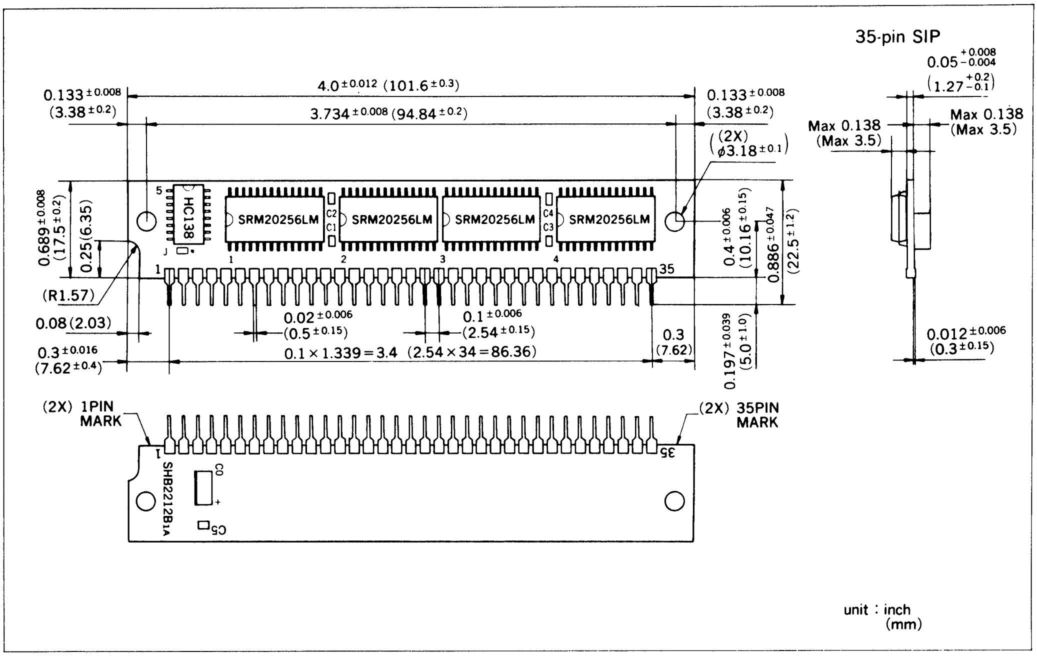
■FUNCTION

●Truth Table

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	A0 to A16	DATA I/O	MODE	I_{DD}
H	×	×	×	×	Hi-Z	Not selected	I_{DDS}, I_{DDS1}, I_{DDR}
×	L	×	×	×	Hi-Z	Not selected	I_{DDS}, I_{DDS1}, I_{DDR}
L	H	×	L	Stable	Data in	Write	I_{DDA}
L	H	L	H	Stable	Data out	Read	I_{DDA}
L	H	H	H	Stable	Hi-Z	Output disable	I_{DDA}

× : "H" or "L"

■PACKAGE DIMENSIONS



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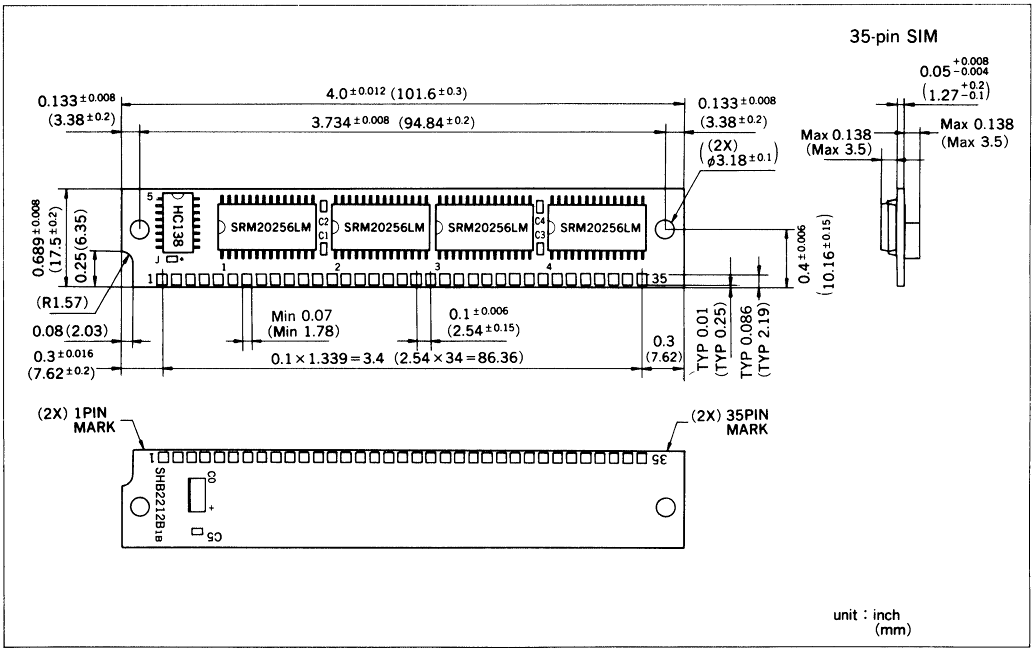


SHB2212B1B

■CHARACTERISTICS CURVES

Under measurement

SHB2125B$_{0A/0B}$

CMOS 2M-BIT HYBRID STATIC RAM

- **●Low Supply Current**
- **●Access Time 120ns**
- **●262,144 Word×8 Bits Asynchronous**

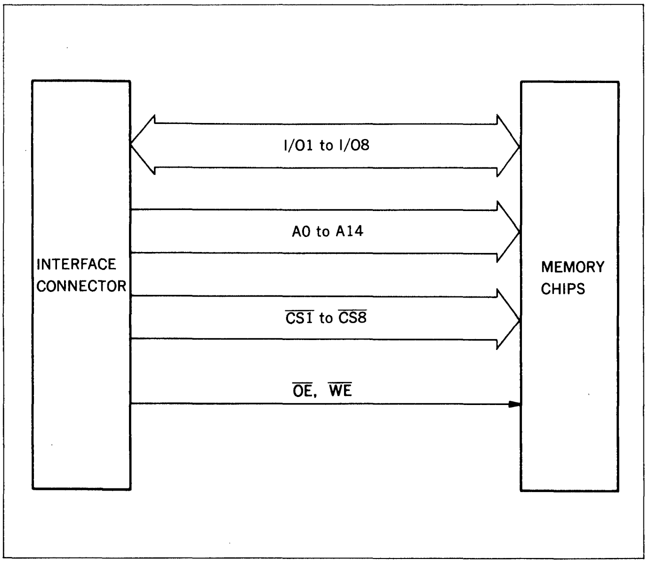
■DESCRIPTION

The SHB2125B$_{0A/0B}$ is a 262,144-word ×8-bit hybrid LSI module with eight 256K SRAM (SRM20256LM). With low power consumption, the module can be used with applications which require a battery back-up. Since it is a static device, it does not requires a clock or refresh circuitry. The I/O control provides 3-state output, for data bus connection. These features provide solutions for a wide variety of applications, including microcomputers and other peripheral equipments.

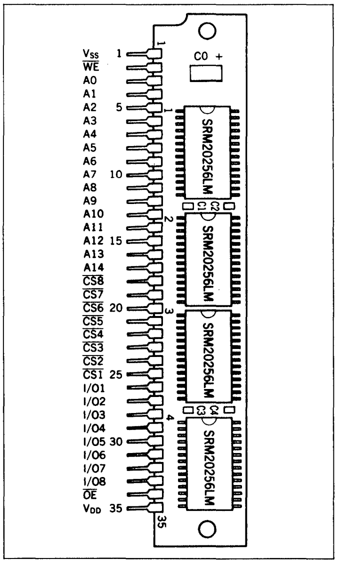
■FEATURES

- ●Hybrid CMOS LSI
- ●262,144-word×8-bit memory density
- ●Mounting 8 pcs. of 256K static RAM (SRM20256LM$_{12}$)
- ●Access time 120ns (Max)
- ●3-State output, with wired-or capability
- ●Single power supply-5volt
- ●Printed-circuit-board (PCB) size 17.5mm×101.6mm×8.27mm (except pins)
- ●PCB··················SHB2125B$_{0A}$ 35 pin SIP (Single inline package)
  SHB2125B$_{0B}$ 35 pin SIM (Single inline module)

■BLOCK DIAGRAM



■PIN CONFIGURATION



■PIN DESCRIPTION

Pin name	Pin No.	Functions
V_{SS}	1	Grounding pin. This GND is common in signal.
$\overline{WE}$	2	⟨Write Enable⟩ Data write signal line (negative logic). Data is written to the memory module at the positive edge of $\overline{WE}$. When $\overline{WE}$ is "H", this module is read operation.
A0 to A14	3 to 17	⟨Address Input⟩ 15-bit address input pin. (Positive logic)
$\overline{CS1}$ $\overline{CS2}$ ⋮ $\overline{CS8}$	25 24 ⋮ 18	⟨Chip Select⟩ These signal line (negative active) are module select line. These line should be selected each one at read and write operation. Each $\overline{CS}$ is available for each 32kB RAM. That is to say, 256kB is divide by 8 $\overline{CS}$ signal. EX. Data will be valid to read and write when $\overline{CS1}$ is "L" and $\overline{CS2}$ to $\overline{CS8}$ are "H". If $\overline{CS1}$ to $\overline{CS8}$ are "H", this module is non-selected mode (I_{DD} is stand-by mode)
I/O1 to I/O8	26 to 33	⟨Data I/O⟩ Inputs or outputs 8-bit of data. This pin provides an input with $\overline{WE}$ low and an output with $\overline{WE}$ high. Also, it has low impedance with $\overline{OE}$ low and high impedance with $\overline{OE}$ high.
$\overline{OE}$	34	⟨Output Enable⟩ Data read signal line (negative logic) from equipment to the memory module. As Data I/O terminals are hi-impedance when $\overline{OE}$ = "H", the contention of data memory output bus can be avoided.
V_{DD}	35	Positive power supply pin. (5V±10%) Normally, 5V is supplied.

■ABSOLUTE MAXIMUM RATINGS

($V_{SS}=0V$)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.5 to 7.0	V
Input voltage	V_I	−0.5* to 7.0	V
I/O voltage	$V_{I/O}$	−0.5* to $V_{DD}+0.3$	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−40 to 100	°C
Soldering temperature and time	T_{sol}	260°C, 10s (Lead only)	—

* V_I, $V_{I/O}$ (Min.) = −1.0V at pulse width less than 50ns

■DC RECOMMENDED OPERATING CONDITIONS

($V_{SS}=0V$, Ta=0 to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
	V_{SS}		0	0	0	V
Input voltage	V_{IH}		2.4	—	$V_{DD}+0.3$	V
	V_{IL}		−0.3*	0	0.8	V

* V_{IL} (Min.) = −1.0V at pulse width less than 50ns

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

($V_{DD}=5V\pm10\%$, $V_{SS}=0V$, Ta=0 to 70°C)

Parameter	Symbol	Conditions	Min	Typ*	Max	Unit
Input leakage current	I_{LI}	$V_I=0$ to V_{DD}	−2	—	2	μA
Stand-by supply current	I_{DDS}	$\overline{CS1}$ to $\overline{CS8}=V_{IH}$, Non-selected	—	12	24	mA
	I_{DDS1}	$\overline{CS1}$ to $\overline{CS8}\geq V_{DD}-0.2V$, $V_I=V_{DD}-0.2V$ or $0.2V$	—	—	800	μA
Average operating current	I_{DDA}	$V_I=V_{IL}$, V_{IH} $I_{I/O}=0mA$ $t_{cyc}=Min$	—	55	70	mA
Output leakage current	I_{LO}	$\overline{CS1}$ to $\overline{CS8}=V_{IH}$ or $\overline{WE}=V_{IL}$ or $\overline{OE}=V_{IH}$, $V_{I/O}=0$ to V_{DD}	−2	—	2	μA
High level output voltage	V_{OH}	$I_{OH}=-1.0mA$	2.4	—	—	V
Low level output voltage	V_{OL}	$I_{OL}=2.1mA$	—	—	0.4	V

* Ta=25°C, $V_{DD}=5.0V$

●Terminal Capacitance

(f=1MHz, Ta=25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C_I		—	—	80	pF
Input/output capacitance	$C_{I/O}$		—	—	80	pF

●AC Electrical Characteristics

○Read cycle

(V_{DD}=5V±10%, V_{SS}=0V, Ta=0 to 70°C)

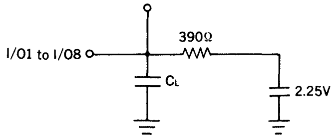
Parameter	Symbol	Conditions	Min	Max	Unit
Read cycle time	t_{RC}	*1	120	—	ns
Address access time	t_{ACC}		—	120	ns
$\overline{CS}$ access time	t_{ACS} *3		—	120	ns
$\overline{OE}$ access time	t_{OE}		—	60	ns
$\overline{CS}$ output set time	t_{CLZ} *3		10	—	ns
$\overline{CS}$ output floating time	t_{CHZ} *3	*2	—	45	ns
$\overline{OE}$ output set time	t_{OLZ}	*1	5	—	ns
$\overline{OE}$ output floating time	t_{OHZ}	*2	—	45	ns
Output hold time	t_{OH}	*1	10	—	ns

○Write cycle

(V_{DD}=5V±10%, V_{SS}=0V, Ta=0 to 70°C)

Parameter	Symbol	Conditions	Min	Max	Unit
Write cycle time	t_{WC}	*1	120	—	ns
Chip select time	t_{CW} *3		105	—	ns
Address valid time	t_{AW}		105	—	ns
Address setup time	t_{AS}		0	—	ns
Write pulse width	t_{WP}		80	—	ns
Address hold time	t_{WR}		0	—	ns
Input data setup time	t_{DW}		50	—	ns
Input data hold time	t_{DH}		0	—	ns
$\overline{WE}$ output floating time	t_{WHZ}	*2	—	45	ns
$\overline{WE}$ output setup time	t_{OW}	*1	10	—	ns

*1 Test Conditions
1. Input pulse level: 0.6V to 2.4V
2. $t_r = t_f$=10ns
3. Input and output timing reference levels: 1.5V
4. Output load: C_L=100pF
5. Output load: C_L=100pF (Include scope & jig capacitance)
6. Circuit



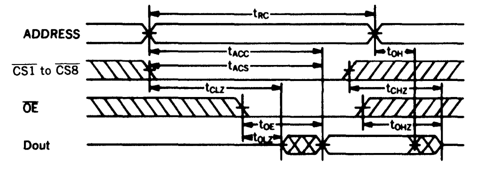
C_L = (Include jig capacitance)

*2 t_{CHZ}, t_{OHZ}, t_{WHZ} Test Conditions
1. Input pulse level: 0.6V to 2.4V
2. $t_r = t_f$=10ns
3. Input timing reference levels: 1.5V
4. Output timing reference levels: ±200V (the level displaced from stable output voltage level)

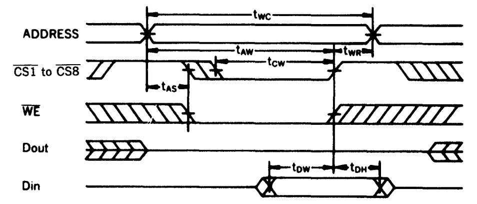
*3 $\overline{CS1}$ to $\overline{CS8}$

● Timing Chart

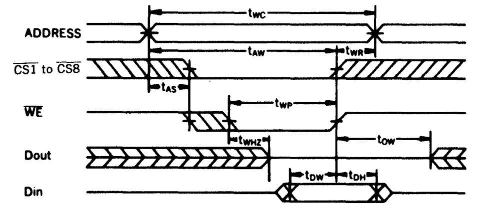
○ Read Cycle*1



○ Write Cycle 1 ($\overline{CS1}$ to $\overline{CS8}$ Control)*2



○ Write Cycle ($\overline{WE}$ Control)*3



*1 During read cycle time, $\overline{WE}$ should be high.

*2 During write cycle that is controlled by $\overline{CS1}$ to $\overline{CS8}$, the output buffer changes to high impedance.
$\overline{CS1}$ to $\overline{CS8}$ should be selected each one at read and write operation.

*3 During write cycle that is controlled by $\overline{WE}$, the output buffer changes to high impedance. ($\overline{OE}$= "H")

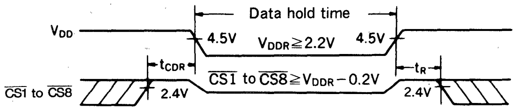
■DATA RETENTION CHARACTERISTICS WITH LOW VOLTAGE POWER SUPPLY

($V_{SS}=0V$, $Ta=0$ to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDR}	$\overline{CS1}$ to $\overline{CS8} \geqq V_{DDR}-0.2V$	2.2	—	5.5	V
Data retention current	I_{DDR}	$V_{DDR}=3V$, $\overline{CS1}$ to $\overline{CS8} \geqq V_{DDR}-0.2V$ $V_I=V_{DDR}-0.2V$ or $0.2V$	—	—	400	μA
Chip select data hold time	t_{CDR}		0	—	—	ns
Operating recovery time	t_R		t_{RC}*	—	—	ns

*t_{RC}=Read cycle time

Data Retention timing 1 ($\overline{CS1}$ to $\overline{CS8}$ control)



NOTE: When retaining data in stand-by mode supply voltage can be lowered within a certain range.
The read or write cycle are disabled when the supply voltage is low.

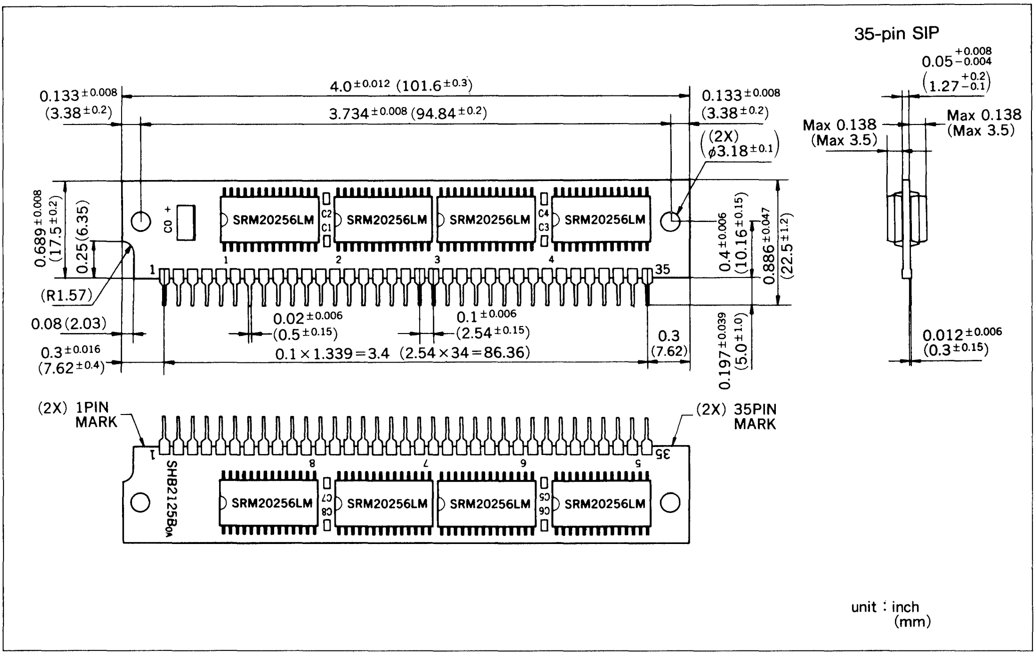
■FUNCTION

●Truth Table

$\overline{CS1}$ to $\overline{CS8}$ *	$\overline{OE}$	$\overline{WE}$	A0 to A14	DATA I/O	MODE	I_{DD}
H	×	×	×	Hi-Z	Not selected	I_{DDS} I_{DDS1} I_{DDR}
Stable *	×	L	Stable	Data in	Write	I_{DDA}
Stable *	L	H	Stable	Data out	Read	I_{DDA}
Stable *	H	H	Stable	Hi-Z	Output disable	I_{DDA}

×: "H" or "L"
*: These lines should be selected each one at read and write operation.

■PACKAGE DIMENSIONS



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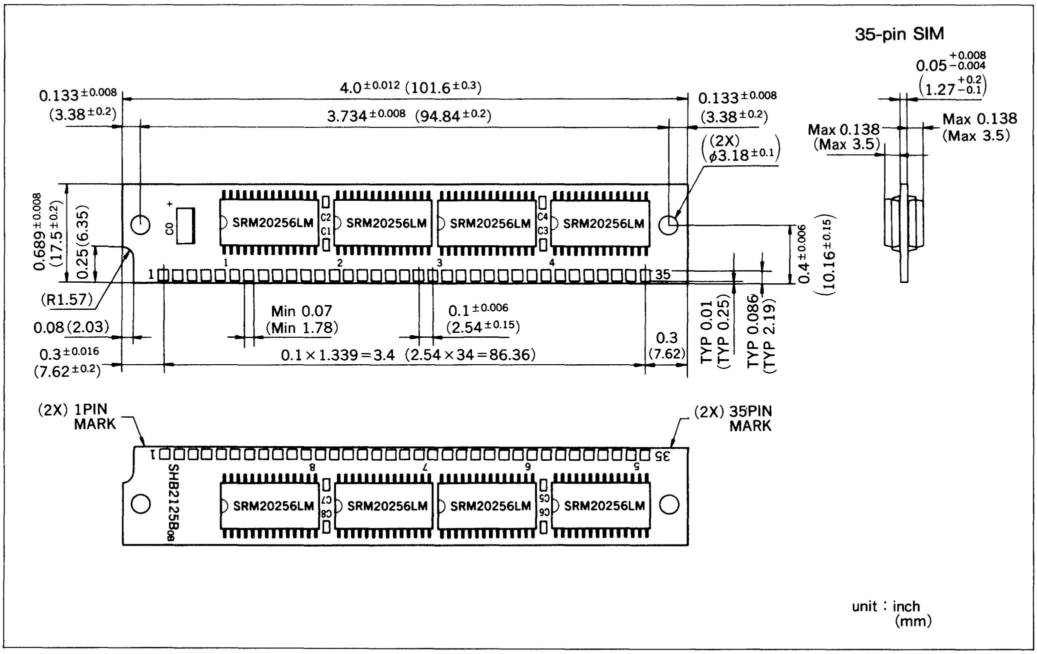

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■CHARACTERISTICS CURVES

Under measurement

PF373-01

SHB2225B0A/0B

CMOS 2M-BIT HYBRID STATIC RAM

- **Low Supply Current**
- **Access Time 150ns**
- **262,144 Words×8 Bits Asynchronous**
- **Included Decoder**

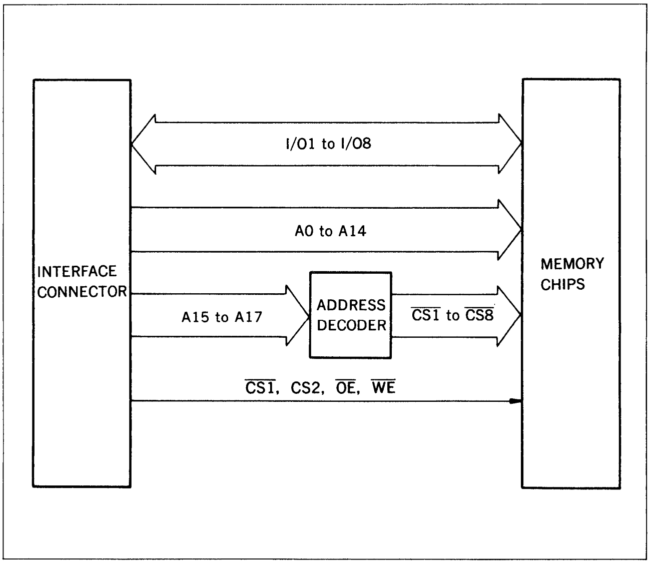
■DESCRIPTION

The SHB2225B0A/0B is a 262, 144-word×8-bit hybrid LSI module with eight 256K SRAM (SRM20256LM) and a 3-8Line decoder. With low power consumption, the module can be used with applications which require a battery back-up. Since it is a static device, it does not requires a clock or refresh circuitry. The I/O control provides 3-state output, for data bus connection. These features provide solutions for a wide variety of applications, including microcomputers and other peripheral equipments.

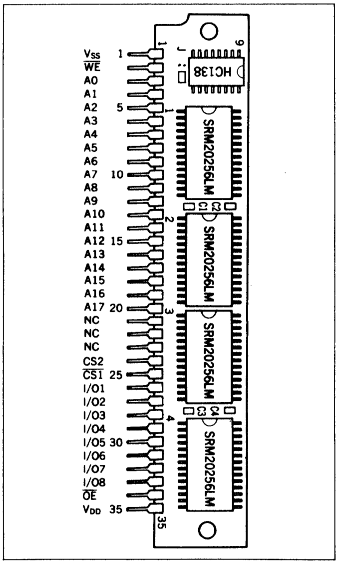
■FEATURES

- Hybrid CMOS LSI
- 262,144-word×8-bit memory density
- Mounting 8 pcs. of 256K static RAM (SRM20256LM12)
- 3-8 line decoder
- Access time 150ns
- Single power supply-5volt
- 3-State output, with wired-or capability
- Printed-circuit-board (PCB) size 17.5mm×101.6mm×8.27mm (except pins)
- PCB··················SHB2225B0A 35 pin SIP (Single inline package)
  SHB2225B0B 35 pin SIM (Single inline module)

■BLOCK DIAGRAM



■PIN CONFIGURATION



■PIN DESCRIPTION

Pin name	Pin No.	Functions
V_{SS}	1	Grounding pin. This GND is common in signal.
$\overline{\text{WE}}$	2	<Write Enable> Data write signal line (negative logic). Data is written to the memory module at the positive edge of $\overline{\text{WE}}$. When $\overline{\text{WE}}$ is "H", this module is read operation.
A0~A17	3 to 20	<Address Input> 18-bit address input pin. (Positive logic)
NC	21 to 23	<No Connection>
$\overline{\text{CS1}}$ CS2	25 24	<Chip Select> Memory module select signal line. Data is valid for read and write when $\overline{\text{CS1}}$ is "L" (negative logic) and CS2 is "H" (positive logic). When $\overline{\text{CS1}}$ is "H" or CS2 is "L" level, the module is in the non-selected mode. (I_{DD} is stand-by mode.)
I/O1 to I/O8	26 to 33	<Data I/O> 8-bit bi-directional data signal bus. (Positive logic) This bus carries data for transfer between the equipment and the memory module.
$\overline{\text{OE}}$	34	<Output Enable> Data read signal line (negative logic) from the equipment to the memory module. As Data I/O terminals are hi-impedance when $\overline{\text{CS1}}$ = "L", CS2 = "H", $\overline{\text{OE}}$ = "H", the contention of data memory output bus can be avoided.
V_{DD}	35	Positive power supply pin. (5V ± 10%) Normally, 5V is supplied.

■ABSOLUTE MAXIMUM RATINGS

($V_{SS}=0V$)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.5 to 7.0	V
Input voltage	V_I	−0.5* to 7.0	V
I/O voltage	$V_{I/O}$	−0.5* to V_{DD}+0.3	V
Operating temperature	T_{opr}	0 to 70	℃
Storage temperature	T_{stg}	−40 to 100	℃
Soldering temperature and time	T_{sol}	260℃, 10s (Lead only)	—

* V_{IL} (Min.) = −1.0V at pulse width less than 50ns

■DC RECOMMENDED OPERATING CONDITIONS

($V_{SS}=0V$, $Ta=0$ to 70℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
	V_{SS}		0	0	0	V
Input voltage	V_{IH}		3.85*2 2.4*3	—	V_{DD}+0.3	V
	V_{IL}		−0.3*1	0	0.8	V

*1 V_{IL} (Min.) = −1.0V at pulse width less than 50ns *2 A15, A16, A17, $\overline{\text{CS1}}$, CS2 *3 Others except A15, A16, A17, $\overline{\text{CS1}}$, CS2

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

($V_{DD}=5V \pm 10\%$, $V_{SS}=0V$, $Ta=0$ to 70℃)

Parameter	Symbol	Conditions	Min	Typ*	Max	Unit
Input leakage current	I_{LI}	$V_I=0$ to V_{DD}	−2	—	2	μA
Stand-by supply current	I_{DDS}	$\overline{\text{CS1}}=V_{IH}$, $CS2=V_{IL}$ Non-Selected	—	—	10	mA
	I_{DDS1}	$\overline{\text{CS1}} \geqq V_{DD}-0.2V$, $CS2 \leqq 0.2V$, $V_I=V_{DD}-0.2V$ or 0.2V	—	—	800	μA
Average operating current	I_{DDA}	$V_I=V_{IL}, V_{IH}$ $I_{I/O}=0mA$ $t_{cyc}=Min$	—	60	75	mA
Output leakage current	I_{LO}	$\overline{\text{CS1}}=V_{IH}$ or $CS2=V_{IL}$ or $\overline{\text{WE}}=V_{IL}$ or $\overline{\text{OE}}=V_{IH}$ $V_{I/O}=0$ to V_{DD}	−2	—	2	μA
High level output voltage	V_{OH}	$I_{OH}=-1.0mA$	2.4	—	—	V
Low level output voltage	V_{OL}	$I_{OL}=2.1mA$	—	—	0.4	V

* $Ta=25℃$, $V_{DD}=5.0V$

●Terminal Capacitance

($f=1MHz$, $Ta=25℃$)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C_I		—	—	80	pF
Input/output capacitance	$C_{I/O}$		—	—	80	pF

●AC Electrical Characteristics

○Read cycle

(V_{DD}=5V±10%, V_{SS}=0V, Ta=0to70°C)

Parameter	Symbol	Conditions	Min	Max	Unit
Read cycle time	t_{RC}	*1	150	—	ns
Address access time	t_{ACC}		—	150	ns
$\overline{\text{CS1}}$ access time	t_{ACS1}		—	150	ns
CS2 access time	t_{ACS2}		—	150	ns
$\overline{\text{OE}}$ access time	t_{OE}		—	70	ns
$\overline{\text{CS1}}$ output set time	t_{CLZ1}		10	—	ns
$\overline{\text{CS1}}$ output floating time	t_{CHZ1}	*2	—	70	ns
CS2 output set time	t_{CLZ2}	*1	10	—	ns
CS2 output floating time	t_{CHZ2}	*2	—	70	ns
$\overline{\text{OE}}$ output set time	t_{OLZ}	*1	5	—	ns
$\overline{\text{OE}}$ output floating time	t_{OHZ}	*2	—	70	ns
Output hold time	t_{OH}	*1	10	—	ns

○Write cycle

(V_{DD}=5V±10%, V_{SS}=0V, Ta=0to70°C)

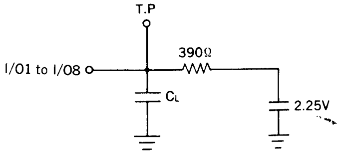
Parameter	Symbol	Conditions	Min	Max	Unit
Write cycle time	t_{WC}	*1	150	—	ns
Chip select time ($\overline{\text{CS1}}$)	t_{CW1}		130	—	ns
Chip select time (CS2)	t_{CW2}		130	—	ns
Address valid time	t_{AW}		130	—	ns
Address setup time	t_{AS}		10	—	ns
Write pulse width	t_{WP}		100	—	ns
Address hold time	t_{WR}		10	—	ns
Input data setup time	t_{DW}		70	—	ns
Input data hold time	t_{DH}		10	—	ns
$\overline{\text{WE}}$ output floating time	t_{WHZ}	*2	—	70	ns
$\overline{\text{WE}}$ output setup time	t_{OW}	*1	10	—	ns

*1 Test Conditions

1. Input pulse level: 0.4V to 3.85V······$\overline{\text{CS1}}$, CS2, A15, A16, A17
   0.6V to 2.4V ······Other except $\overline{\text{CS1}}$, CS2, A15, A16, A17
2. $t_r=t_f$=10ns
3. Input and output timing reference levels: 1.5V
4. Output load: C_L=100pF

*2 t_{CHZ}, t_{OHZ}, t_{WHZ} Test Conditions

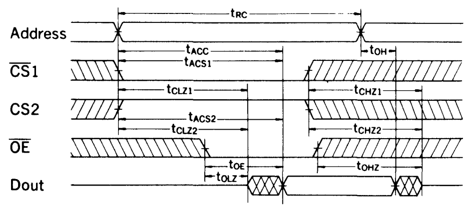
1. Input pulse level: 0.4V to 3.85V······$\overline{\text{CS1}}$, CS2, A15, A16, A17
   0.6V to 2.4V ······Other except $\overline{\text{CS1}}$, CS2, A15, A16, A17
2. $t_r=t_f$=10ns
3. Input and output timing reference levels: 1.5V
4. Output timing reference levels: ±200mV (the level displaced from stable output voltage level)
5. Output load: C_L=100pF (Include scope & jig capacitance)
6. Circuit



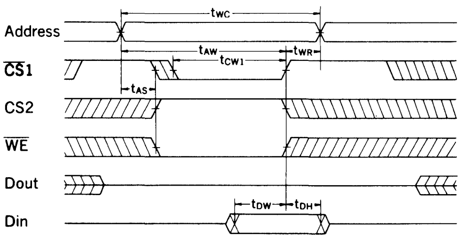
C_L=100pF (Include jig capacitance)

● Timing Chart

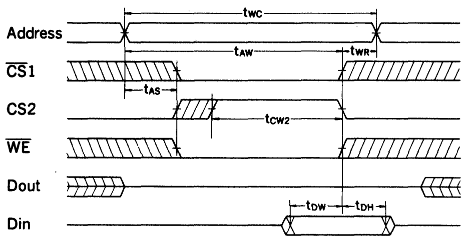
○ Read Cycle*1



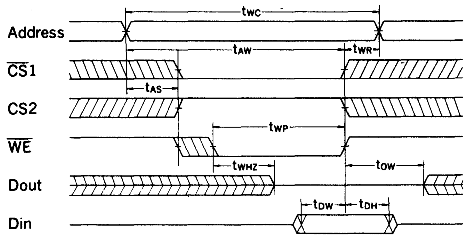
○ Write Cycle 1 ($\overline{\text{CS1}}$ Control)*2



o Write Cycle 2 (CS2 Control)*3



o Write Cycle 3 ($\overline{\text{WE}}$ Control)*4



*1 During read cycle time, $\overline{\text{WE}}$ should be high.
*2 During write cycle that is controlled by $\overline{\text{CS1}}$, the output buffer changes to high impedance.
*3 During write cycle that is controlled by CS2, the output buffer changes to high impedance.
*4 During write cycle that is controlled by $\overline{\text{WE}}$, the output buffer changes to high impedance. ($\overline{\text{OE}}$="H")

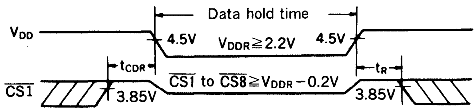
■DATA RETENTION CHARACTERISTICS WITH LOW VOLTAGE POWER SUPPLY

(V_{SS}=0V, Ta=0 to 70°C)

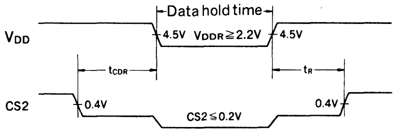
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDR}	$\overline{\text{CS1}} \geqq V_{DDR}-0.2V$ or $CS2 \leqq 0.2V$	2.2	—	5.5	V
Data retention current	I_{DDR}	$V_{DDR}=3V$, $\overline{\text{CS1}} \geqq V_{DDR}-0.2V$, or $CS2 \leqq 0.2V$, $V_I=V_{DDR}-0.2V$ or $0.2V$	—	—	440	μA
Chip select data hold time	t_{CDR}		30	—	—	ns
Operating recovery time	t_R		t_{RC}*	—	—	ns

*t_{RC}=Read cycle time

Data retention timing 1 ($\overline{\text{CS1}}$ Control)



Data retention timing 2 (CS2 Control)



NOTE : When retaining data in stand-by mode the supply voltage can be lowered within a certain range. The read or write cycle are disabled when the supply voltage is low.

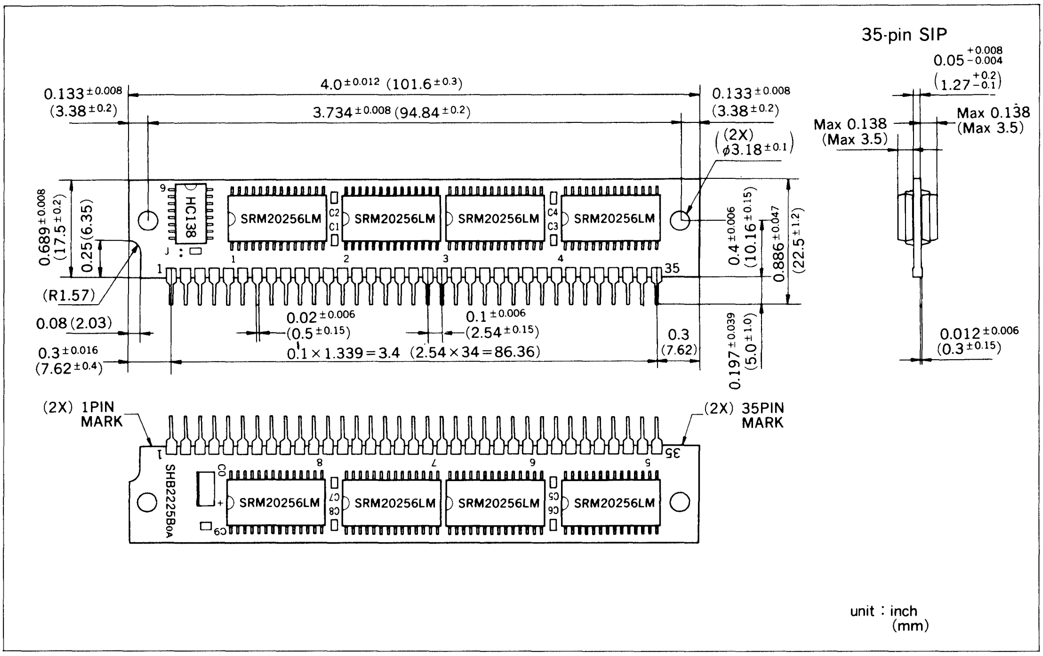
■FUNCTION

●Truth Table

$\overline{\text{CS1}}$	CS2	$\overline{\text{OE}}$	$\overline{\text{WE}}$	A0 to A17	DATA I/O	MODE	I_{DD}
H	×	×	×	×	Hi-Z	Not selected	I_{DDS} I_{DDS1} I_{DDR}
×	L	×	×	×	Hi-Z	Not selected	I_{DDS} I_{DDS1} I_{DDR}
L	H	×	L	Stable	Data in	Write	I_{DDA}
L	H	L	H	Stable	Data out	Read	I_{DDA}
L	H	H	H	Stable	Hi-Z	Output disable	I_{DDA}

× : "H" or "L"

PACKAGE DIMENSIONS



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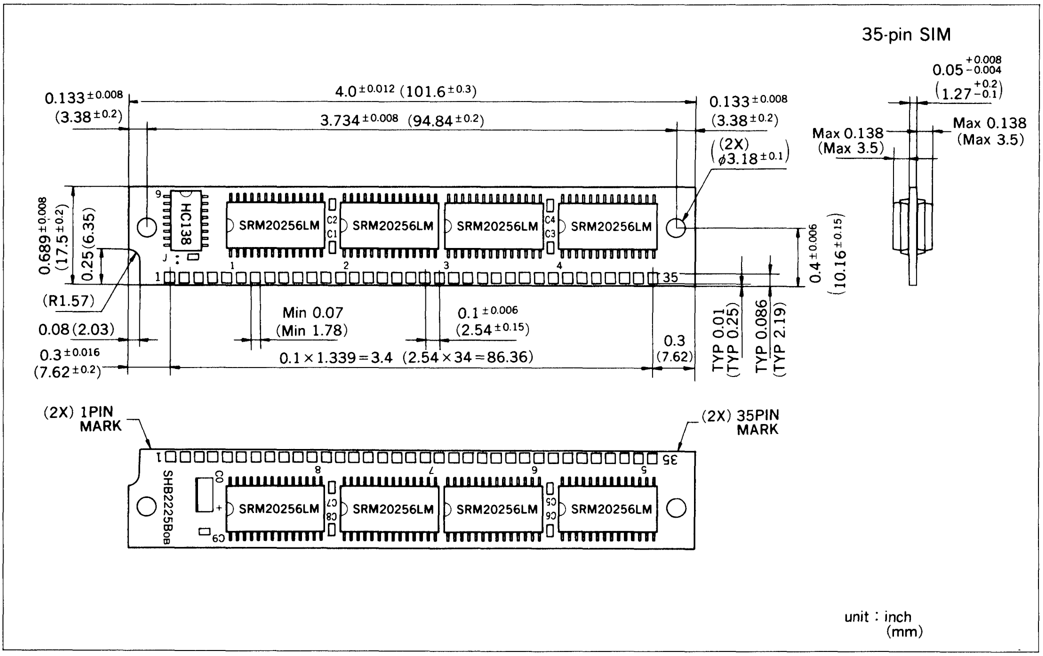


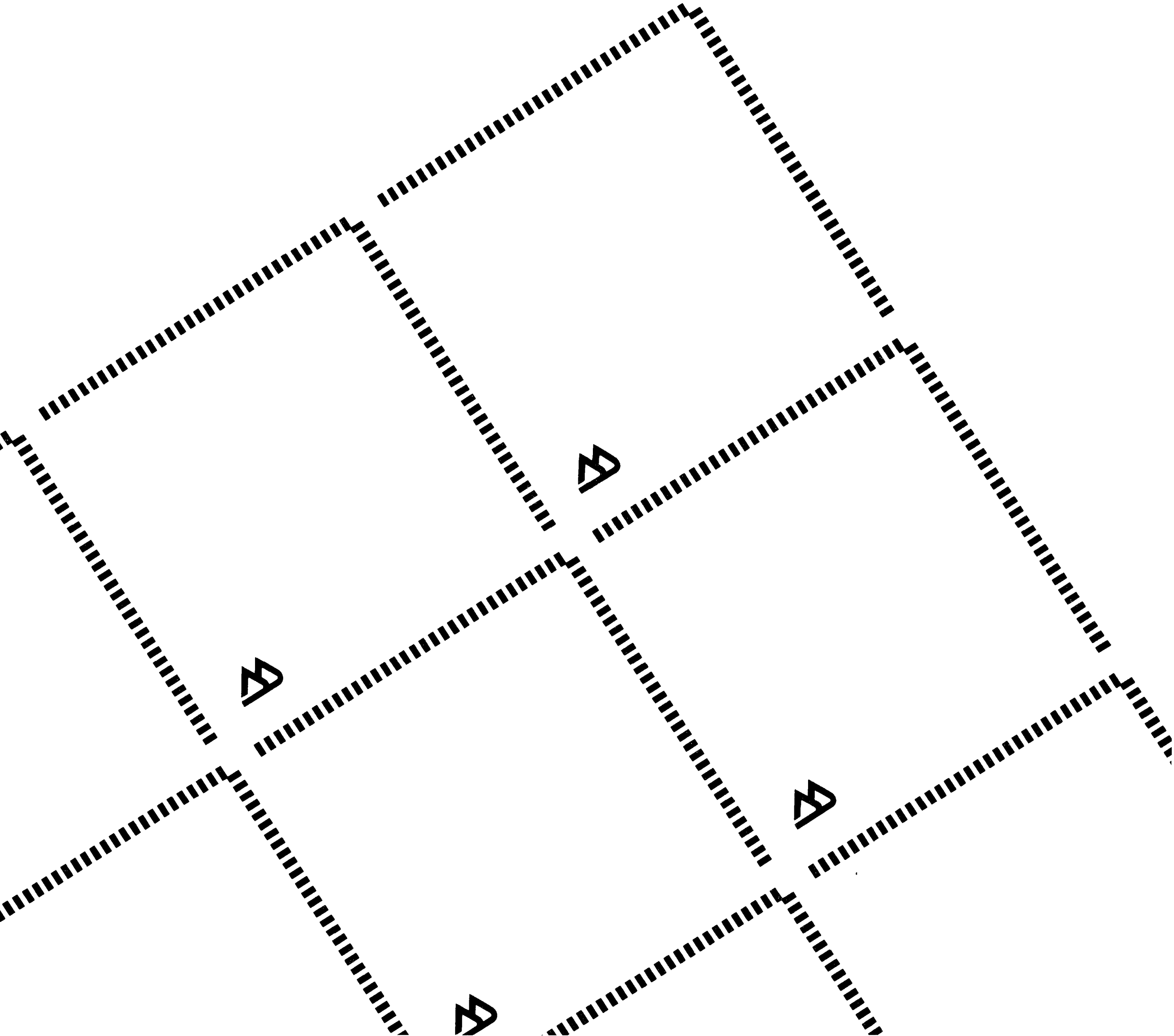
SHB2225B0B

■CHARACTERISTICS CURVES

Under measurement

1988/1989 CMOS DATA BOOK

I. OTHER PRODUCTS



SED9420C$_{AC}$

CMOS DATA SEPARATOR FOR FDD

- Built-in Terminals for Switching between 5$\frac{1}{4}$-inch and 8-inch Floppy Disks and between Double Density and Single Density
- For Filter Switching System Only

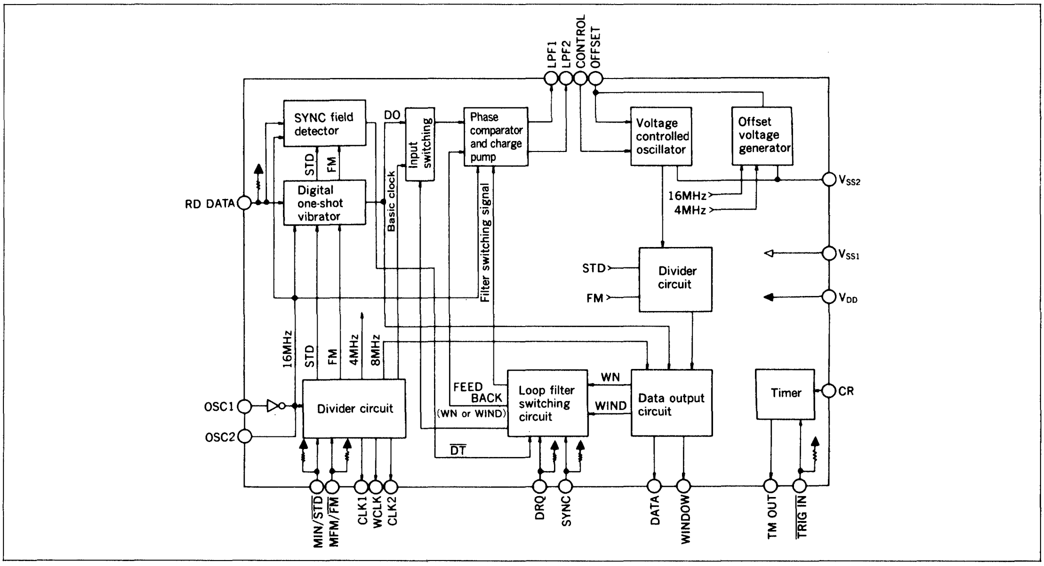
■DESCRIPTION

The SED9420C$_{AC}$ is a CMOS VFO data separator LSI for use in floppy disk interfaces. Equipped with its own SYNC field detection, loop filter switching, and timer functions, the IC allows construction of a one-chip VFO circuit with just a few external components. Floppy disk controllers which can be used with this IC are the μPD765, μPD765A, FD1791-02, FD1793-02, MB8876A, MB8877A.

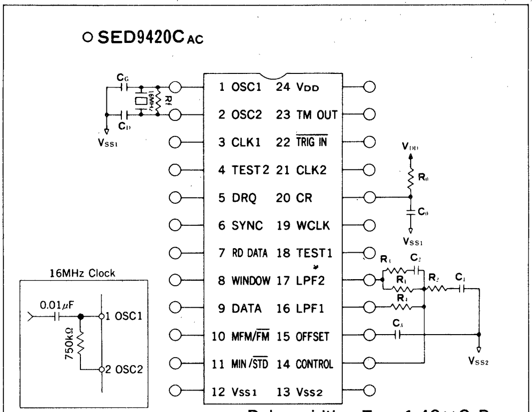
■FEATURES

- Data separation function using the VFO system (a phase locked loop)
- Switchable between 8-inch and 5$\frac{1}{4}$-inch floppy disk drives (FDDs)
- Recording can be switched between double density and single density
- Requires no adjustment and few external circuits
- Compatible with the IBM Format
- Clock output for floppy disk controllers ······to be connected with μPD765series, MB8877series or FD179Xseries
- Single 5V power supply
- TTL-compatible I/O pins (excluding OSC1 and OSC2)
- Built-in timer circuit (with external C-R)
- Package··24-pin DIP(plastic)

■BLOCK DIAGRAM



PIN CONFIGURATION AND AN EXAMPLE OF EXTERNAL CIRCUITS



Pulse width $T_w = 1.42 \times C_0 R_0$
$R_0 > 5k\Omega$

[Reference value of external circuits]

FDD	5¼-inch/8-inch
R_1	33kΩ
R_2	2.4kΩ
R_3	7.5kΩ
R_4	100Ω
C_1	0.01μF
C_2	3,300pF
C_3	0.01 to 0.1μF
C_D	10pF
C_G	10pF
R_f	1 MΩ
f_0	16MHz±0.5%

Accuracy of resistor ±5%, Accuracy of capacitor ±10%

PIN DESCRIPTION

Pin Name	Pin No.	Function
OSC1	1	(1) Gate input terminal for the inverted amplifier of the crystal oscillator circuit. (2) Clock input terminal when using an external 16MHz clock.
OSC2	2	Drain output terminal for the crystal oscillator circuit's inverted amplifier.
CLK1	3	FDC clock output terminal (for the μPD765) • f=8MHz for 8-inch floppy disk • f=4MHz for 5¼-inch floppy disk
TEST2*	4	Test terminal for testing functions (with pull-up resistor)
DRQ*	5	Input signal for FDC data transfer signal (with pull-up resistor)
SYNC*	6	FDC control signal input terminal for GAP area and SYNC area detection (with pull-up resistor).
RD DATA*	7	Input terminal for the read data signal from the floppy disk drive (FDD) (with pull-up resistor).
WINDOW	8	Output terminal for the data window signal used to separate data pulses in the DATA signal from clock pulses.
DATA	9	Output terminal for the read data signal produced from the RD DATA signal. Sent to the FDC together with the WINDOW signal, and is then separated into clock and data pulses.
MFM/$\overline{\text{FM}}$*	10	Terminal for switching between double density and single density (with pull-up resistor) HIGH selects double density (MFM), LOW selects single density (FM).
MIN/$\overline{\text{STD}}$*	11	Terminal for switching between 5¼-inch and 8-inch floppy disks (with pull-up resistor). HIGH selects 5¼-inch floppies LOW selects 8-inch floppies.
V_{SS1}	12	Ground terminal for the digital system.
V_{SS2}	13	Ground terminal for the analog system. (VCO ground)
CONTROL	14	Input terminal for the VCO (voltage controlled oscillator) control voltage.
OFFSET	15	Input terminal for offset voltage for VCO center frequency correction. An external capacitor tied to this pin generates offset voltage.
LPF1	16	Terminal for connecting the PLL system's loop filter. Selected when sync field is detected for frequency lock-in.
LPF2	17	Terminal for connecting the PLL system's loop filter. Selected when ID and DATA fields are detected after frequency lock-in.
TEST1	18	Test terminal for testing functions (ordinarily not connected).
WCLK	19	Write clock for the μPD765 FDC. • 8-inch MFM: Interval T=1 μs • 8-inch FM: Interval T=2 μs • 5¼-inch MFM: Interval T=2 μs • 5¼-inch FM: Interval T=4 μs
CR	20	CR connection terminal for the timer circuit.
CLK2	21	FDC clock output terminal (for the MB8877 and FD1791). • f=2MHz for 8-inch floppy disk • f=1MHz for 5¼-inch floppy disk
$\overline{\text{TRIG IN}}$*	22	Trigger input terminal for the timer circuit (with pull-up resistor).
TM OUT	23	Retriggerable oneshot timer output terminal (Timer for head-load timing or motor-on signal, etc.)
V_{DD}	24	+5V power supply terminal

NOTE: *Input terminals with pull-up resistors are pulled up through a standard resistance of 100K ohms. Since susceptibility to noise is increased by leaving terminals open, it is recommended that terminals which are to be kept HIGH be connected directly to V_{DD}.

■ABSOLUTE MAXIMUM RATINGS

($V_{SS}=0V$)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	-0.5 to 7.0	V
Input voltage	V_I	-0.5 to $V_{DD}+0.3$	V
Output voltage	V_O		
Operating temperature	T_{opr}	-10 to 60	℃
Storage temperature	T_{stg}	-65 to 150	℃
Soldering temperature and time	T_{sol}	260℃, 10s (at lead)	–

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

($V_{SS}=0V$)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating supply voltage	V_{DD}	—	4.75	5.0	5.25	V
High level input voltage	V_{IH}	—	2.0	—	$V_{DD}+0.3$	V
Low level input voltage	V_{IL}	—	-0.3	—	0.8	V
High level output voltage	V_{OH}	$I_{OH}=-200\mu A$	2.4	—	V_{DD}	V
Low level output voltage	V_{OL}	$I_{OL}=2.0mA$	0	—	0.4	V
High level input current*1	I_{IH1}	$V_{IH}=V_{DD}$	—	—	2.0	μA
Low level input current*2	I_{IL1}	$V_{IL}=V_{SS}$ $V_{DD}=5V$	-100	-50	-10	μA
High level output current*3	I_{OH1}	$V_{OH}=2.4V$	—	—	-200	μA
Low level output current*4	I_{OL1}	$V_{OL}=0.4V$	2.0	—	—	mA
Current consumption	I_{DD}	Output open, $V_{DD}=5V$, 16MHz oscillation	—	—	10	mA

*1 HIGH input current for pins with pull-up resistors
*2 LOW input current for pins with pull-up resistors
*3 HIGH output current for driver output terminals
*4 LOW output current for driver output terminals

●AC Electrical Characteristics

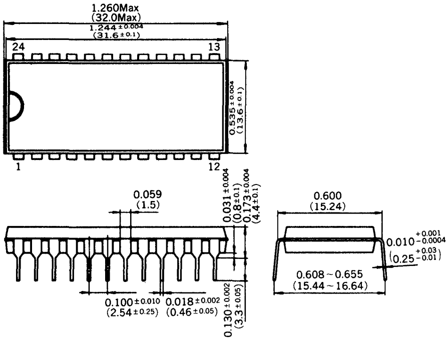
(Standard frequency ; $f_0=16MHz$)

Parameter	Symbol	Pin Name	Conditions	Min	Typ	Max	Unit
Frequency	f_{CLK1}	CLK1	$MIN/\overline{STD}=Low$	—	8.0	—	MHz
			$MIN/\overline{STD}=High$	—	4.0	—	MHz
	f_{CLK2}	CLK2	$MIN/\overline{STD}=Low$	—	2.0	—	MHz
			$MIN/\overline{STD}=High$	—	1.0	—	MHz
Cycle time and Window width	t_{CYWCL} and t_{WHWIND}	WCLK and WINDOW	$MIN/\overline{STD}=Low$ $MFM/\overline{FM}=Low$	—	2	—	μs
			$MIN/\overline{STD}=High$ $MFM/\overline{FM}=Low$	—	4	—	μs
			$MIN/\overline{STD}=Low$ $MFM/\overline{FM}=High$	—	1	—	μs
			$MIN/\overline{STD}=High$ $MFM/\overline{FM}=High$	—	2	—	μs
High level width	t_{WHDT}	DATA	$C_L=15pF$	110	125	140	ns
High level width	t_{WHRD}	RD DATA	—	150	—	—	ns
VCO Oscillation frequency	f_{VCO}	—	CONTROL terminal$=V_{DD}/2$ External capacitance ($0.1\mu F$) connected to OFFSET terminal	3.8	4.0	4.3	MHz
VCO control voltage coefficient	K_V	—	$\lvert V_{DD}/2\text{-CONTROL voltage}\rvert \leqq 0.5V$	1.0	1.2	1.4	MHz/V
Supply voltage rise time	V_R	—	Time for voltage to rise from 10% level to 90%	5	—	—	ms

PACKAGE DIMENSIONS

C24

24-pin DIP



unit : inch
(mm)

NOTE : The SED9420C_{AC} cannot execute the Read Truck Command of MB8877 and FD179X.

NOTE : It is impossible to read 8-inch Media with SED9420C_{AC} when the GAP DATA of 8-inch Media is written in (00)H.

KF055
PF276-01

SCI7700Y Series/SCI7701Y Series

CMOS VOLTAGE DETECTOR

- **●Voltage Detector**
- **●Many Types**
- **●Low Operating Supply Current**

■DESCRIPTION

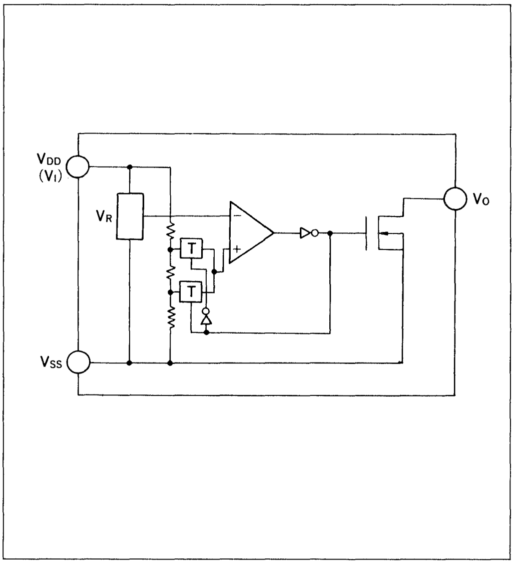
The SCI7700YSeries/SCI7701YSeries are a series of low-power precision voltage detectors, which do not require external adjustments. The SCI7700YSeries/SCI7701YSeries have such applications as battery-life detecion, power supply fault monitoring, over/under-voltage protecion and battery back-up swiching. The SCI7700YSeries is a n open-drain Nch output type and the SCI7701YSeries is a CMOS output type. Both are available in SOT 89 (plastic) packages.

■FEATURES

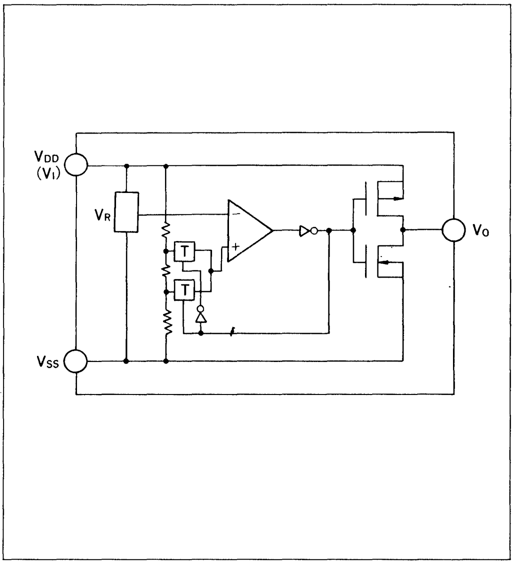
●Many types	See the next page.
●Low operating supply current	Typ 1.8μA (SCI7700Y$_{NA}$, $V_{DD}=3.0V$)
●Low range of operating voltage	Typ 1.2V (SCI7700Y$_{NA}$)
●Temperature coefficient of detection voltage	Typ (detection voltage/reference voltage) × 0.1 (mV/°C)
●Hysterisis difference	Typ detection voltage × 0.05V
●Package	SOT 89 (plastic)

■BLOCK DIAGRAM

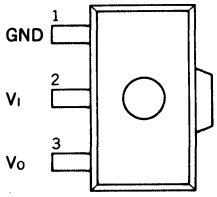
●SCI7700Y series



●SCI7701Y series



■PIN CONFIGURATION



■SCI7700Y Series/SCI7701Y Series

(Ta=25°C)

Type No.	Output mode	Detection voltage (V)			Operating voltage (V)	Operating supply current (μA)
		Min	Typ	Max		
SCI7700Y$_{VA}$	Open drain Nch	0.90	0.95	1.00	0.8 to 5.0	Typ 1.4 (V_{DD}=1.5V)
SCI7700Y$_{AA}$	Open drain Nch	1.00	1.05	1.10	0.9 to 5.0	Typ 1.4 (V_{DD}=1.5V)
SCI7700Y$_{BA}$	Open drain Nch	1.10	1.15	1.20	0.9 to 5.0	Typ 1.4 (V_{DD}=1.5V)
SCI7700Y$_{NA}$	Open drain Nch	1.85	1.90	1.95	1.2 to 10.0	Typ 1.8 (V_{DD}=3.0V)
SCI7700Y$_{TA}$	Open drain Nch	3.80	4.00	4.20	1.5 to 10.0	Typ 2.6 (V_{DD}=6.0V)
SCI7701Y$_{CA}$	CMOS	2.10	2.15	2.20	1.5 to 10.0	Typ 1.8 (V_{DD}=3.0V)
SCI7701Y$_{PA}$	CMOS	2.20	2.25	2.30	1.5 to 10.0	Typ 1.8 (V_{DD}=3.0V)
SCI7701Y$_{SA}$	CMOS	2.30	2.35	2.40	1.5 to 10.0	Typ 1.8 (V_{DD}=3.0V)
SCI7701Y$_{EA}$	CMOS	2.50	2.55	2.60	1.5 to 10.0	Typ 1.8 (V_{DD}=3.0V)
SCI7701Y$_{FA}$	CMOS	2.60	2.70	2.80	1.5 to 10.0	Typ 1.8 (V_{DD}=3.0V)
SCI7701Y$_{RA}$	CMOS	2.70	2.80	2.90	1.5 to 10.0	Typ 1.8 (V_{DD}=3.0V)
SCI7701Y$_{GA}$	CMOS	2.90	3.00	3.10	1.5 to 10.0	Typ 2.2 (V_{DD}=4.5V)
SCI7701Y$_{HA}$	CMOS	3.10	3.20	3.30	1.5 to 10.0	Typ 2.2 (V_{DD}=4.5V)
SCI7701Y$_{TA}$	CMOS	3.80	4.00	4.20	1.5 to 10.0	Typ 2.6 (V_{DD}=6.0V)
SCI7701Y$_{MA}$	CMOS	4.00	4.15	4.30	1.5 to 10.0	Typ 2.6 (V_{DD}=6.0V)
SCI7701Y$_{JA}$	CMOS	4.30	4.45	4.60	1.5 to 10.0	Typ 2.6 (V_{DD}=6.0V)
SCI7701Y$_{KA}$	CMOS	4.60	4.75	4.90	1.5 to 10.0	Typ 2.6 (V_{DD}=6.0V)
SCI7701Y$_{LA}$	CMOS	4.90	5.10	5.30	1.5 to 10.0	Typ 2.6 (V_{DD}=6.0V)

■ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Input voltage (supply voltage)	$V_{DD}(V_I)-V_{SS}$	12	V
Output voltage	V_O	$V_{DD}+0.3$ to $V_{SS}-0.3$	V
Output current	I_O	50	mA
Power dissipation (Ta≦25°C)	P_D	400	mW
Operating temperature	T_{opr}	−20 to 70	°C
Storage temperature	T_{stg}	−65 to 150	°C
Soldering temperature and time	T_{sol}	260°C, 10s (at lead)	—

NOTE) Although this IC has electrostatic protection circuit, damage may still occur if very high electrostatic potentials are applied.

■ELECTRICAL CHARACTERISTICS

●SCI7700Y Series/SCI7701Y Series

Parameter	Symbol	Ratings	Min	Typ	Max	Unit
Detection voltage	V_{DET}	$Ta=25°C$	See the left page			V
Operating supply current	I_{DDO}	$V_{DD}=1.5V, Ta=25°C$	—	1.4	3.0	μA
		$V_{DD}=3.0V, Ta=25°C$	—	1.8	4.0	
		$V_{DD}=4.5V, Ta=25°C$	—	2.2	5.0	
		$V_{DD}=6.0V, Ta=25°C$	—	2.6	6.0	
Supply (Operating) voltage	V_{DD} (V_I)	$Ta=-20\sim70°C$	See the left page			V
Hysteresis difference	$\varDelta V_{DET}$	$Ta=-20\sim70°C$	—	$V_{DET}\times0.05$*	—	V
Temperature coefficient of V_{DET}	$\frac{V_{DET}(Ta=70°C)-V_{DET}(Ta=-20°C)}{90}$	$Ta=-20\sim70°C$	Typ $(V_{DET}/V_R)\times0.1$			mV/°C

*$V_{DET}\times0.04$ (Typ) about SCI7700Y$_{TA}$/SCI7701Y$_{TA}$/SCI7701Y$_{MA}$/SCI7701Y$_{JA}$/SCI7701Y$_{KA}$/SCI7701Y$_{LA}$

●SCI7700Y$_{VA}$/SCI7700Y$_{AA}$/SCI7700Y$_{BA}$

Parameter	Symbol	Ratings	Min	Typ	Max	Unit
Output current	I_O (Nch)	$V_{DD}=0.85V, V_{DS}=0.5V, Ta=25°C$	0.05	0.40	1.00	mA
		$V_{DD}=0.95V, V_{DS}=0.5V, Ta=25°C$	0.15	0.70	1.50	
		$V_{DD}=1.05V, V_{DS}=0.5V, Ta=25°C$	0.30	1.00	2.00	
Reference voltage supply	V_R	$Ta=25°C$	0.70	0.80	0.90	V

V_{DS}: Voltage between drain and source

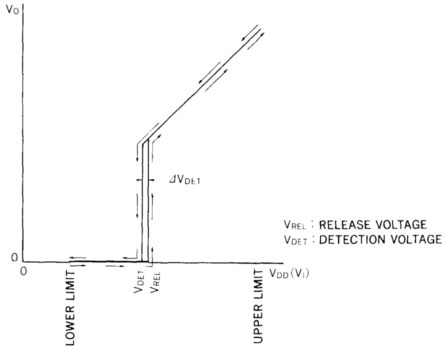
●SCI7700Y$_{NA}$/SCI7700Y$_{TA}$/SCI7701Y$_{CA}$/SCI7701Y$_{PA}$/SCI7701Y$_{SA}$/SCI7701Y$_{EA}$/SCI7701Y$_{FA}$/SCI7701Y$_{RA}$/SCI7701Y$_{GA}$/SCI7701Y$_{HA}$/SCI7701Y$_{TA}$/SCI7701Y$_{MA}$/SCI7701Y$_{JA}$/SCI7701Y$_{KA}$/SCI7701Y$_{LA}$

Parameter	Symbol	Ratings	Min	Typ	Max	Unit
Output current	I_O (Nch)	$V_{DD}=0.95V, V_{DS}=0.5V, Ta=25°C$	0.03	0.15	0.50	mA
		$V_{DD}=1.00V, V_{DS}=0.5V, Ta=25°C$	0.05	0.22	0.60	
		$V_{DD}=1.20V, V_{DS}=0.5V, Ta=25°C$	0.30	0.70	1.50	
		$V_{DD}=2.40V, V_{DS}=0.5V, Ta=25°C$	1.40	2.00	2.30*1	
		$V_{DD}=3.60V, V_{DS}=0.5V, Ta=25°C$	1.50	2.30	2.60*2	
	I_O (Pch)	$V_{DD}=4.50V, V_{DS}=2.1V, Ta=25°C$	1.7	2.0	2.3	
		$V_{DD}=8.00V, V_{DS}=2.1V, Ta=25°C$	2.8	3.1	3.8	
Reference voltage supply	V_R	$Ta=25°C$	0.90	1.00	1.10	V

*1 : 3.30 mA about SCI7700Y$_{TA}$, *2 : 4.00mA about SCI7700$_{TA}$

V_{DS}: Voltage between drain and source

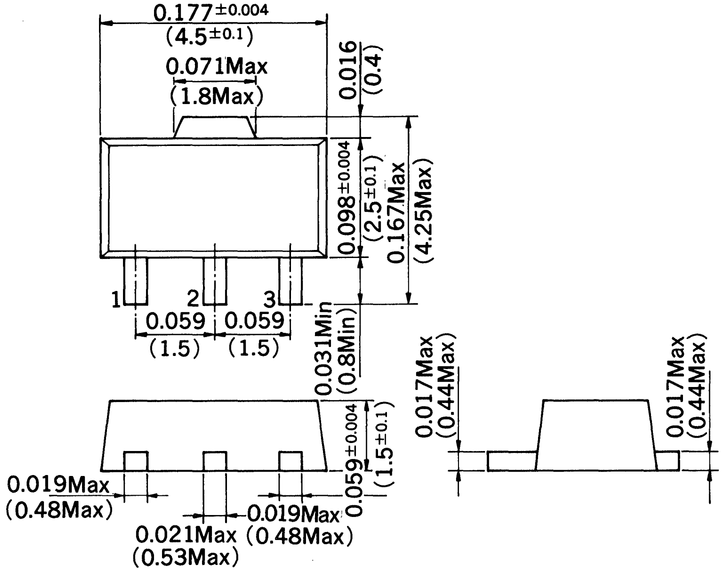
●Performance Curves



■PACKAGE DIMENSIONS

Y3

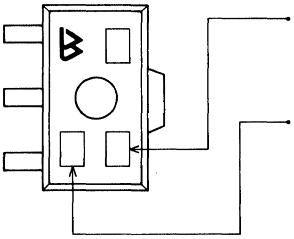
3-pin SOT89



unit : inch
(mm)

■MARKING

An abbreviation code is printed on SCI7700Y Series/SCI7701Y Series below, because its package size is very small.



Detection voltage code

The first code of SUB CODE (Ex. B with SCI7700YBA)

Series code

C : CMOS output (SCI7701Y Series)

D : Open drain Nch output (SCI7700Y Series)

SCI7710Y Series/SCI7711Y Series

CMOS VOLTAGE REGULATOR

- ●Voltage Regulator (Positive Output/Negative Output)
- ●Low Operating Supply Current

■DESCRIPTION

SCI7710YSeries/SCI7711YSeries are fixed voltage regulators of a CMOS silicon gate process. The SCI7710YSeries/SCI7711YSeries are constructed of a reference voltage source, a differential amplifier and a resistor for setting voltage levels. The SCI7710YSeries are positive voltage regulators and the SCI7711YSeries are negative regulators. Both are available in SOT 89 (plastic) packages.

■FEATURES

- ●Low operating supply current……………………………Typ 1.0μA (SCI7711Y$_{DA}$)
- ●Small temperature coefficient of output voltage………Typ 1.8mV/°C (SCI7711Y$_{DA}$)
- ●Wide range of operating voltage…………………………Max 15V
- ●Line regulation……………………………………………Typ 0.1%/V (SCI7711Y$_{DA}$)
- ●Package……………………………………………………SOT 89 (plastic)

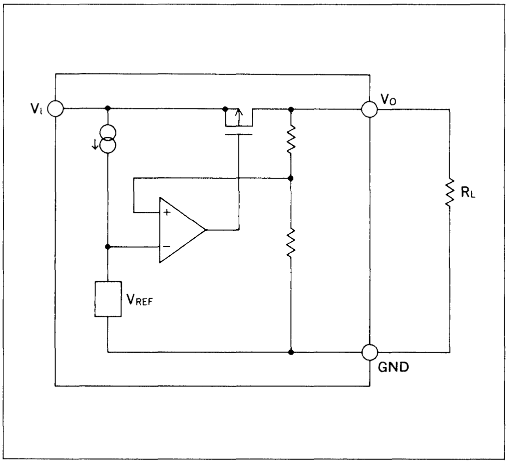
■SCI7710YSeries/SCI7711YSeries

Type No.	Output voltage	Output current	Operating current	Input voltage	Absolute maximum input voltage
SCI7710Y$_{BA}$	5V	Typ 50mA $V_I=7V$	Typ 2.4μA	15V	21V
SCI7710Y$_{DA}$	3V	Typ 30mA $V_I=5V$	Typ 2.0μA	15V	21V
SCI7711Y$_{BA}$	−5V	Typ 50mA $V_I=-7V$	Typ 1.4μA	−15V	−21V
SCI7711Y$_{DA}$	−3V	Typ 30mA $V_I=-5V$	Typ 1.0μA	−15V	−21V

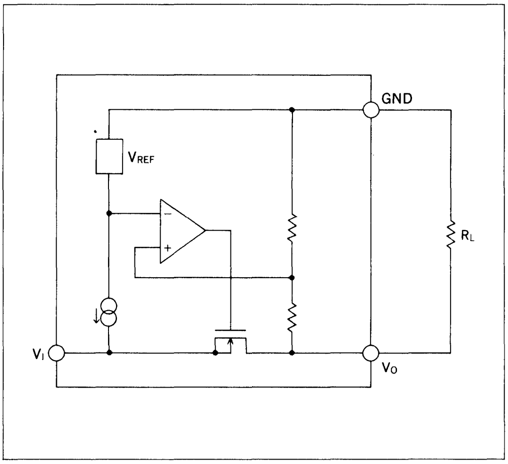
∗1.5V, 1.8V and 2.2V (output voltage) are under development.

■BLOCK DIAGRAM

●SCI7710Y Series

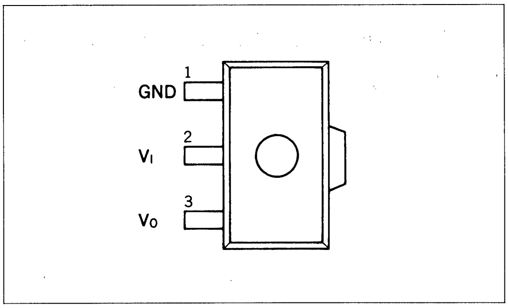


●SCI7711Y Series

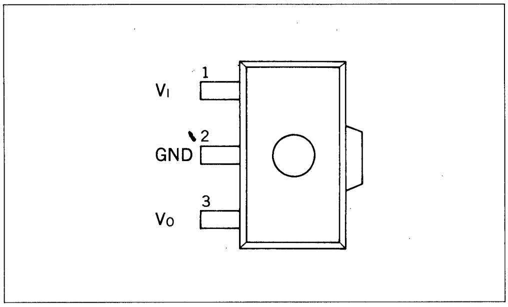


■PIN CONFIGURATION

●SCI7710Y Series



●SCI7711Y Series



■ABSOLUTE MAXIMUM RATINGS

●SCI7710Y Series

Parameter	Symbol	Ratings	Unit
Input voltage	V_I	21	V
Output current	I_O	100	mA
Output voltage	V_O	V_I+0.3 to GND−0.3	V
Power dissipation (Ta≦25°C)	P_D	400	mW
Operating temperature	T_{opr}	−20 to 70	°C
Storage temperature	T_{stg}	−65 to 150	
Soldering temperature and time	T_{sol}	260°C, 10s (at lead)	—

●SCI7711Y Series

Parameter	Symbol	Ratings	Unit
Input voltage	V_I	−21	V
Output current	I_O	100	mA
Output voltage	V_O	GND+0.3 to V_I−0.3	V
Power dissipation (Ta≦25°C)	P_D	400	mW
Operating temperature	T_{opr}	−20 to 70	°C
Storage temperature	T_{stg}	−65 to 150	
Soldering temperature and time	T_{sol}	260°C, 10s (at lead)	—

■ELECTRICAL CHARACTERISTICS

●SCI7710Y$_{BA}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input voltage	V_I	Ta=−20 to 70°C	—	—	15	V
Output voltage	V_O	V_I=7.0V, I_O=10mA, Ta=25°C	4.75	5.00	5.25	V
		V_I=6.0V to15V, I_O=10mA, Ta=−20to70°C	4.50	—	5.50	
		V_I=7.2V to15V, I_O=50mA, Ta=−20to70°C	4.50	—	5.50	
Voltage tolerance	$\|V_I - V_O\|$	V_I=5.0V, I_O=10mA, Ta=−20to70°C	—	0.25	0.35	V
		V_I=5.0V, I_O=50mA, Ta=−20to70°C	—	1.35	1.70	
Line regulation	$\frac{\|\Delta V_O\|}{\|\Delta V_I \cdot V_O\|}$	Ta=−20°C to 70°C (constant condition) V_I=6.0V to15V, I_O=1mA to10mA	—	0.18	—	%/V
Operating supply current	I_{DDO}	V_I=5.0V to15V, Ta=25°C	—	2.4	4.8	μA
Temperature coefficient of output voltage	K_t		—	−3.0	—	mV/°C
Load regulation	ΔV_O	V_I=7V, 1mA≦I_O≦50mA	—	50	—	mV

●SCI7710Y$_{\text{DA}}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input voltage	V_I	Ta = −20 to 70°C	—	—	15	V
Output voltage	V_O	V_I=5.0V, I_O=10mA, Ta=25°C	2.85	3.00	3.15	V
		V_I=4.0Vto15V, I_O=10mA, Ta=−20to70°C	2.70	—	3.30	
		V_I=5.0Vto15V, I_O=30mA, Ta=−20to70°C	2.70	—	3.30	
Voltage tolerance	$\|V_I - V_O\|$	V_I=3.0V, I_O=10mA, Ta=−20to70°C	—	0.35	0.50	V
		V_I=3.0V, I_O=30mA, Ta=−20to70°C	—	1.20	1.70	
Line regulation	$\frac{\|\Delta V_O\|}{\|\Delta V_I \cdot V_O\|}$	Ta=−20 to 70°C (constant condition) V_I=4.0Vto15V, I_O=1mA to10mA	—	0.15	—	%/V
Operating supply current	I_{DDO}	V_I=3.0Vto15V, Ta=25°C	—	2.0	4.5	μA
Temperature coefficient of output voltage	K_t		—	−1.8	—	mV/°C
Load regulation	ΔV_O	V_I=5V, 1mA≦I_O≦30mA	—	30	—	mV

●SCI7711Y$_{\text{BA}}$

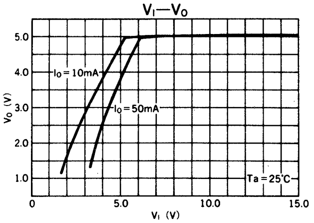
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input voltage	V_I	Ta = −20 to 70°C	−15	—	—	V
Output voltage	V_O	V_I=−7.0V, I_O=10mA, Ta=25°C	−5.25	−5.00	−4.75	V
		V_I=−5.7Vto−15V, I_O=10mA, Ta=−20to70°C	−5.50	—	−4.50	
		V_I=−6.5Vto−15V, I_O=50mA, Ta=−20to70°C	−5.50	—	−4.50	
Voltage tolerance	$\|V_I - V_O\|$	V_I=−5.0V, I_O=10mA, Ta=−20to70°C	—	0.16	0.20	V
		V_I=−5.0V, I_O=50mA, Ta=−20to70°C	—	0.80	1.00	
Line regulation	$\frac{\|\Delta V_O\|}{\|\Delta V_I \cdot V_O\|}$	Ta=−20 to 70°C (constant condition) V_I=−6.0Vto−15V, I_O=1mAto10mA	—	0.1	—	%/V
Operating supply current	I_{DDO}	V_I=−5.0Vto−15V, Ta=25°C	—	1.4	2.0	μA
Temperature coefficient of output voltage	K_t		—	3.0	—	mV/°C
Load regulation	ΔV_O	V_I=−7V, 1mA≦I_O≦50mA	—	50	—	mV

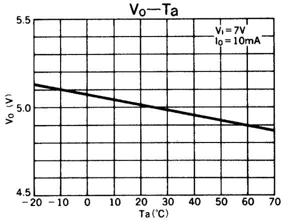
●SCI7711Y$_{\text{DA}}$

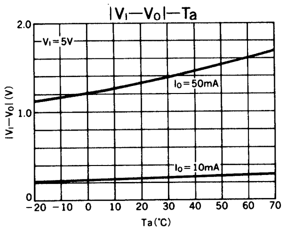
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input voltage	V_I	Ta = −20 to 70°C	−15	—	—	V
Output voltage	V_O	V_I=−5.0V, I_O=10mA, Ta=25°C	−3.15	−3.00	−2.85	V
		V_I=−3.7Vto−15V, I_O=10mA, Ta=−20to70°C	−3.30	—	−2.70	
		V_I=−4.5Vto−15V, I_O=30mA, Ta=−20to70°C	−3.30	—	−2.70	
Voltage tolerance	$\|V_I - V_O\|$	V_I=−3.0V, I_O=10mA, Ta=−20to70°C	—	0.22	0.30	V
		V_I=−3.0V, I_O=30mA, Ta=−20to70°C	—	0.70	1.00	
Line regulation	$\frac{\|\Delta V_O\|}{\|\Delta V_I \cdot V_O\|}$	Ta=−20 to 70°C (constant condition) V_I=−4.0Vto−15V, I_O=1mAto10mA	—	0.1	—	%/V
Operating supply current	I_{DDO}	V_I=−3.0Vto−15V, Ta=25°C	—	1.0	1.5	μA
Temperature coefficient of output voltage	K_t		—	1.8	—	mV/°C
Load regulation	ΔV_O	V_I=−5V, 1mA≦I_O≦30mA	—	30	—	mV

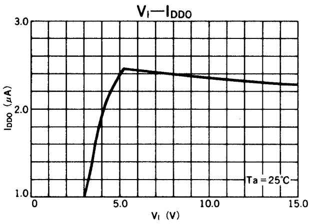
■CHARACTERISTICS CURVES

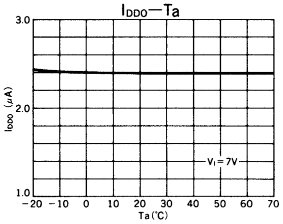
●SCI7710Y$_{BA}$

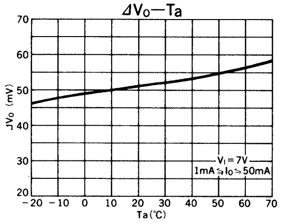




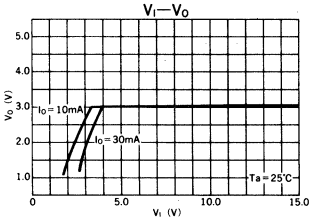


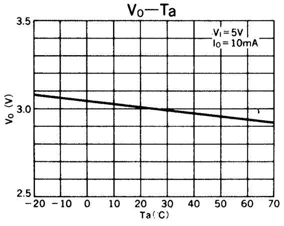


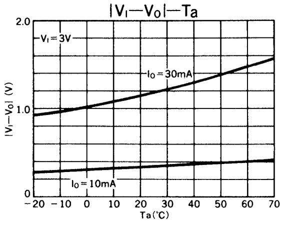


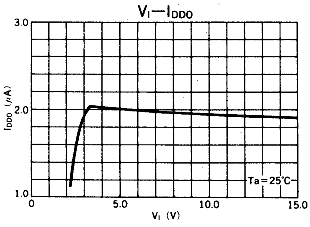


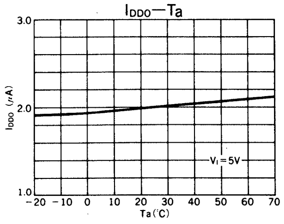
●SCI7710Y$_{DA}$

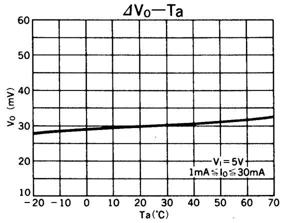




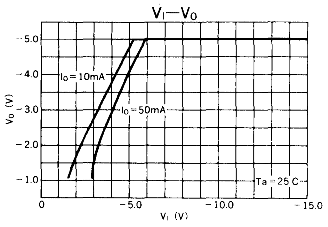


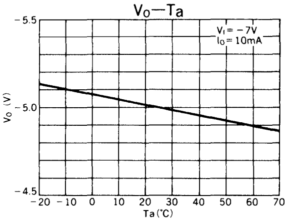


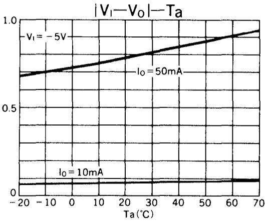


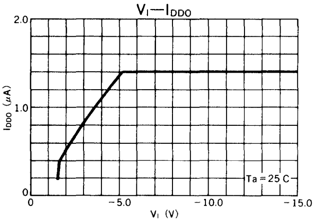


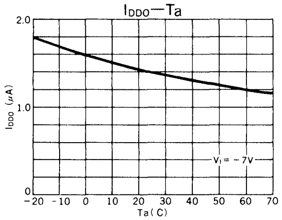
●SCI7711Y$_{BA}$

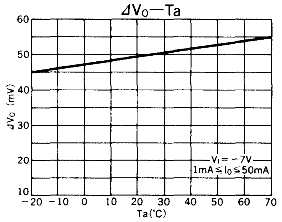




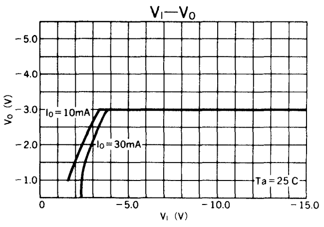


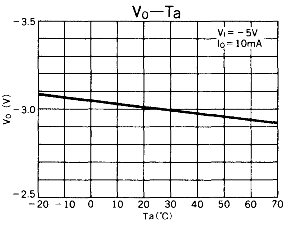


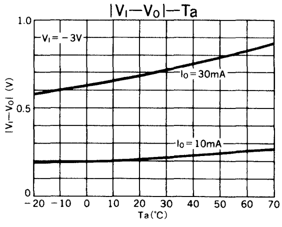


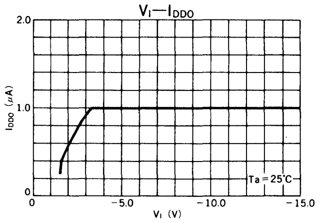


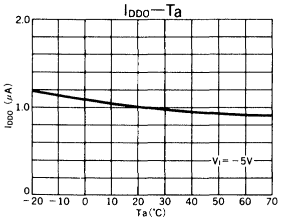
●SCI7711Y$_{DA}$

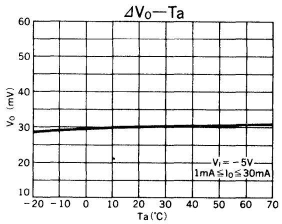




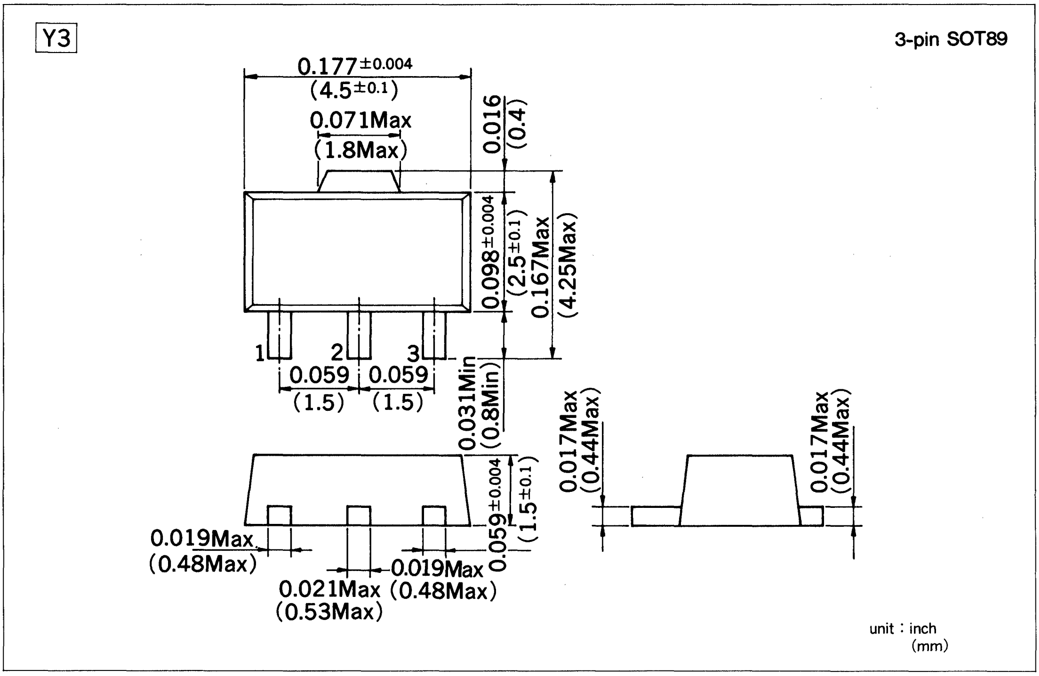






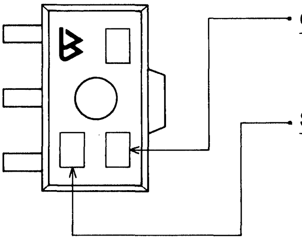


■PACKAGE DIMENSIONS



■MARKING

An abbreviation code is printed on SCI7710Yseries/SCI7711Yseries below, because its package size is very small.



Output voltage code

B : 5V/−5V, D : 3V/−3V

Series code

P : Positive voltage regulator, N : Negative voltage regulator

SCI7660C

CMOS DC/DC CONVERTER

- **95% Typical Power Efficiency**
- **Doubled Output Voltage**
- **Voltage Conversion (Positive↔Negative)**

■DESCRIPTION

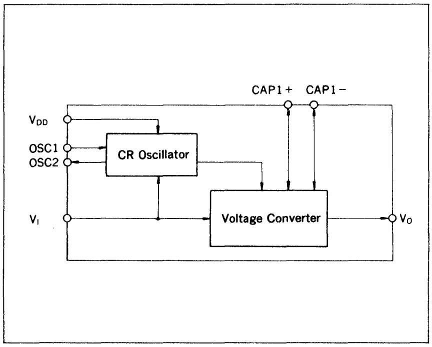
The SCI7660C CMOS DC/DC Converter features high operational performance with low power dissipation. The booster generates a doubled output voltage from the input.

It is possible to drive the LSI that need another power supply than main power supply. (LCD drivers•Analog LSI etc.) Its very low power requirement makes it ideal to supply handy equipments with power.

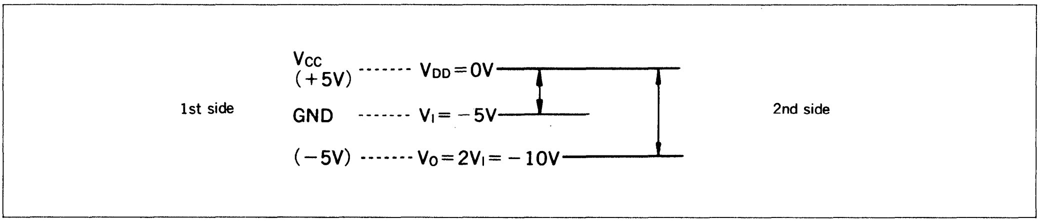
■FEATURES

- High performance with low power dissipation
- Simple conversion of V_{DD}(+5V) to $-V_I$(−5V), $+2V_I$ (+10V)
- Output current ······················30mA Max (V_{DD}=5V)
- Power conversion efficiency······95% Typ
- Cascade connection (two device connected V_{DD}=5V, V_O=−10V)
- Low power·····························Ideal for dry cell battery
- On-chip CR oscillator
- Package·······························8 pin DIP (plastic)

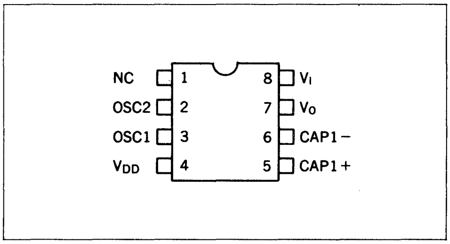
■BLOCK DIAGRAM



■VOLTAGE RELATIONS



■PIN CONFIGURATION



■PIN DESCRIPTION

Pin Name	Pin No.	Functions
OSC1	3	Oscillation resistor connection terminal
OSC2	2	
V_{DD}	4	Power supply terminal (positive, system supply Vcc)
CAP1+	5	Terminal for connection of capacitor for booster (positive)
CAP1−	6	Terminal for connection of capacitor for booster (negative)
V_O	7	Output terminal at doubling
V_I	8	Power supply terminal (negative, system supply GND)

■ABSOLUTE MAXIMUM RATINGS

($V_{DD}=0V$, $Ta=25°C$)

Parameter	Symbol	Ratings	Unit
Input voltage	V_I	−10.0 to 0.5	V
Output voltage	V_O	−20.0 to V_I	V
Power dissipation	P_D	300	mW
Operating temperature	T_{opr}	−30 to 85	°C
Storage temperature	T_{stg}	−65 to 150	°C
Soldering temperature and time	T_{sol}	260°C, 10s (at lead)	—

■ELECTRICAL CHARACTERISTICS

($V_{DD}=0V$, $Ta=-30$ to 85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input voltage	V_I		−8.0	—	−1.2	V
Output voltage	V_O		−16.0	—	—	V
Booster current consumption	I_{opr}	$R_L=\infty$, $R_{OSC}=1M\Omega$, $V_I=-5V$	—	40	70	μA
Stationary current	I_Q	$R_L=\infty$, $V_I=-8V$	—	—	2.0	μA
Output impedance	R_O	$I_O=10mA$, $V_I=-5V$	—	80	120	Ω
Booster power conversion efficiency	P_{eff}	$I_O=5mA$, $V_I=-5V$	90	95	—	%
Input leakage current	I_{LI}	OSC1 terminal, $V_I=-8V$	—	—	2.0	μA
Oscillation frequency	f_{OSC}	$R_{OSC}=1M\Omega$, $V_I=-5V$	16	20	24	kHz

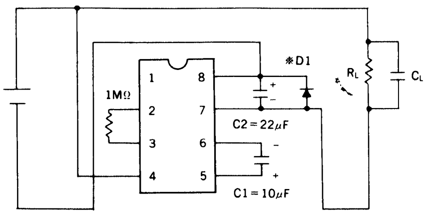
■RECOMMENDED OPERATING CONDITIONS

($V_{DD}=0V$, $Ta=-30$ to 85°C)

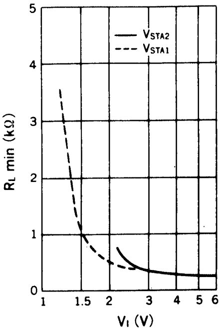
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Booster start voltage	V_{STA1}	$R_{OSC}=1M\Omega$, $C_L/C_2\leqq 1/20$ *1 $C_2\geqq 10\mu F$ $Ta=-20$ to 85°C	—	—	−1.2	V
	V_{STA2}	$R_{OSC}=1M\Omega$	—	—	−2.2	V
Booster stop voltage	V_{STP}	$R_{OSC}=1M\Omega$	−1.2	—	—	V
Output load resistance	R_L		R_L min *2	—	—	Ω
Output current	I_O		—	—	30	mA
Oscillation frequency	f_{OSC}		10	—	30	kHz
External resistance for oscillation	R_{OSC}		680	—	2000	kΩ
Capacitor for booster	C_1, C_2, C_3		3.3	—	—	μF

*1 Recommended circuity in low voltage operation is shown below.
*2 R_L min depends on input voltage as shown below.

Recommended circuit in low voltage operation



※D1 (VF(IF=1mA)≦0.6V)



■TYPICAL PERFORMANCE CHARACTERISTICS

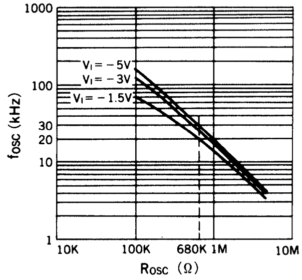


Fig. 1 Oscillation Frequency (fosc) vs. External-Resistance (Rosc)

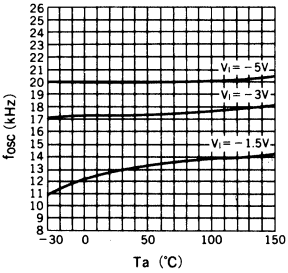


Fig. 2 Oscillation Frequency (fosc) vs. Temperature (Ta)

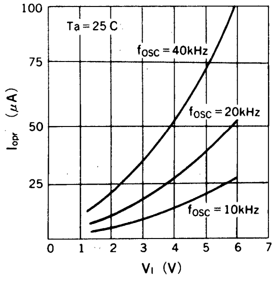


Fig. 3 Booster Current Consumption (I_{opr}) vs. Input Voltage (V_I)

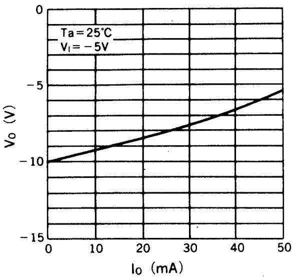


Fig. 4 Output Voltage (Vo) vs. Output Current (Io)

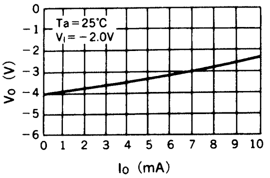


Fig. 5 Output Voltage (Vo) vs. Output Current (Io)

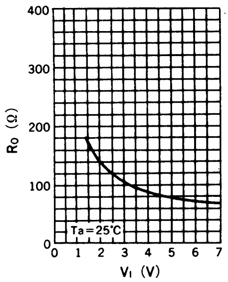


Fig. 6 Output Impedance (Ro) vs. Input Voltage (V_I)

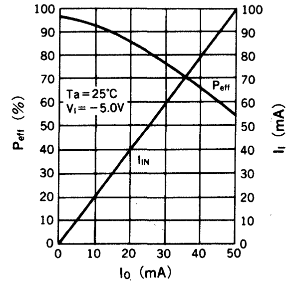


Fig. 7 Power Conversion Efficiency (Peff)/Input Current (Ii) vs. Output Current (Io)

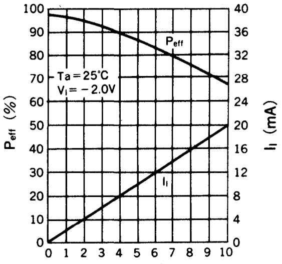


Fig. 8 Power Conversion Efficiency (Peff)/Input Current (Ii) vs. Output Current (Io)

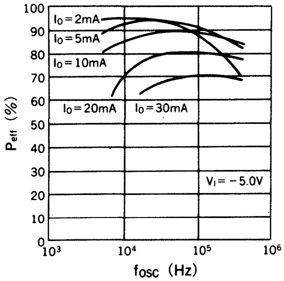


Fig. 9 Power Conversion Efficiency (Peff) vs. Oscillation Frequency (fosc)

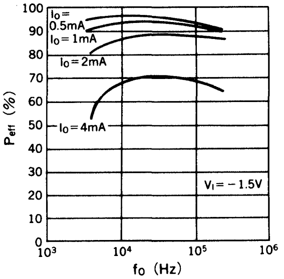
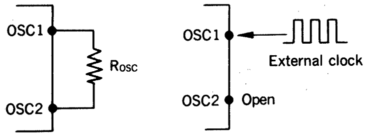


Fig. 10 Power Conversion Efficiency (Peff) vs. Oscillation Frequency (fosc)

■CIRCUIT DESCRIPTION

●C-R Oscillator

The SCI7660C contains a C-R oscillator for internal oscillation. It consists of an external resistor Rosc connected between the OSC1 pin and OSC2 pin.

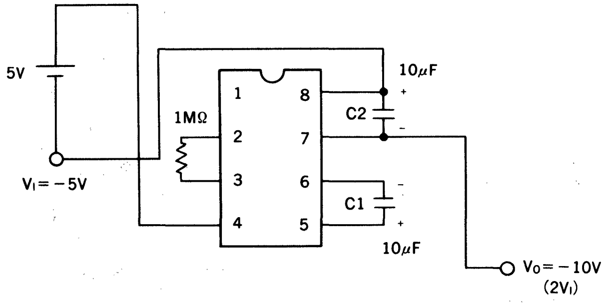


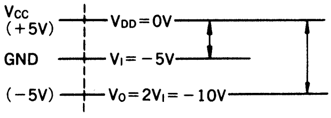
C-R Oscillation

External Clock Operation

●Voltage Converters

The voltage converters double the input supply voltage (Vi) using clocks generated by the C-R oscillator. A doubled voltage can be obtained with a booster capacitor between CAP+ and CAP−, and with a external smoothing capacitor between Vi and Vo.

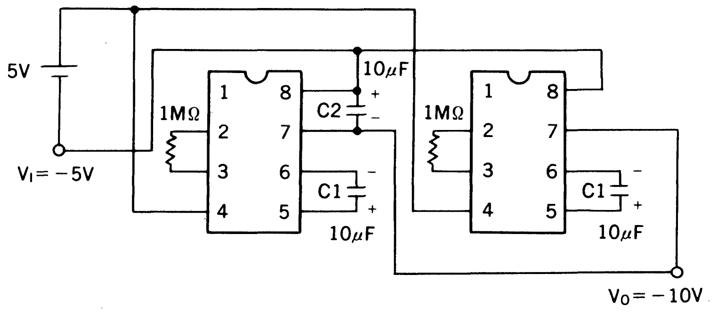




Typical doubled voltage relations

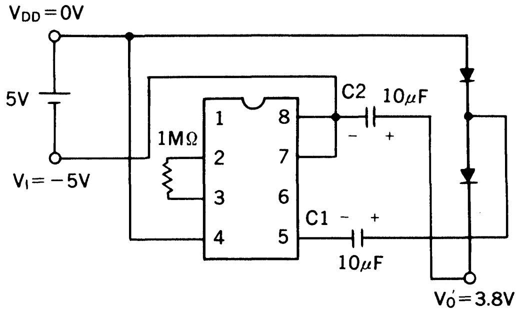
■EXAMPLE OF APPLICATIONS

- **Parallel Connection** (Output impedance can be reduced by parallel connections.)



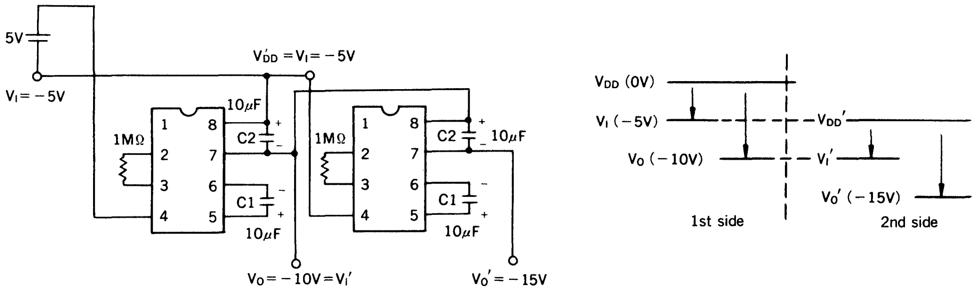
Parallel Connection

- **Positive Voltage Conversion** (Input voltage can be doubled toward the positive side with diode.)



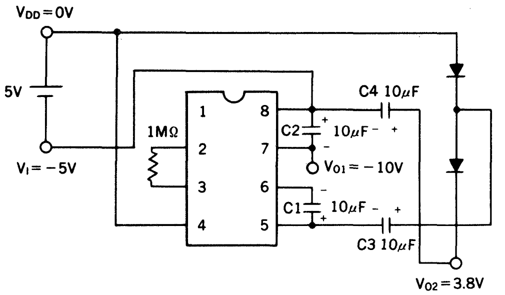
Positive Voltage Conversion

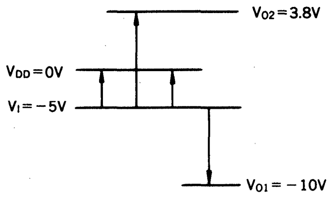
- **Cascade Connection** (Cascade connection of SCI7660 further increase the output voltage. Note, however, that the cascade connection increase the output impedance.)



Cascade Connection

- **Negative Voltage Conversion+Positive Voltage Conversion** (This circuit produces outputs of −10V and +3.8V from the −5V input by combination of voltage doubler circuit and positive voltage conversion circuit.)



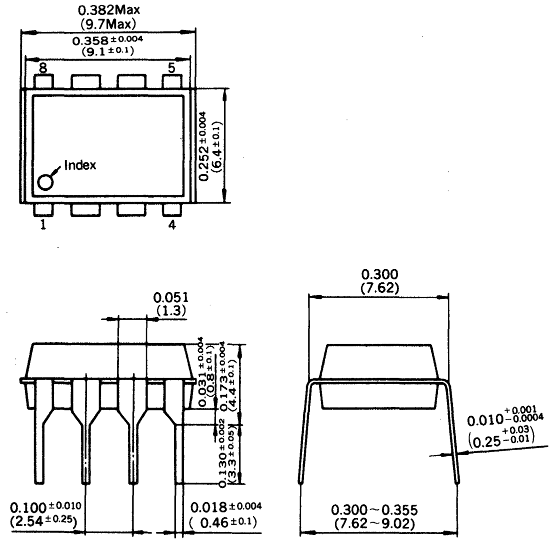


Negative Voltage Conversion+
Positive Voltage Conversion

■PACKAGE DIMENSIONS

C8

8-pin DIP



unit : inch
(mm)

SCI7661C/M

CMOS DC/DC CONVERTER

- **95% Typical Power Efficiency**
- **Doubled/Tripled Output Voltage**
- **Internal Voltage Regulator**

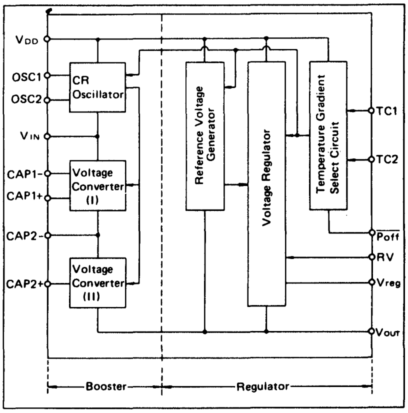
■DESCRIPTION

The SCI7661C CMOS DC/DC Converter features high operational performance with low power dissipation. It consists of two major parts: the booster circuitry and the regulator circuitry. The booster generates a doubled output voltage (-2.4V to -12V) or tripled output voltage (-3.6V to -18V) from the input (-1.2 to -6V). The regulator is capable of setting the output to any desired voltage. The regulated voltage can be given one of the three threshold temperature gradients.

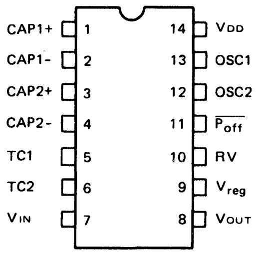
■FEATURES

- High performance with low power dissipation
- Simple conversion of V_{IN} (-5V) to $|V_{IN}|$ (+5V), $2|V_{IN}|$ (+10V), $2V_{IN}$ (-10V) or $3V_{IN}$ (-15V)
- On-chip output voltage regulator
- Power conversion efficiency – Typ95%
- Temperature gradient for LCD power supply – 0.1%/°C, 0.4%/°C or 0.6%/°C
- Power off by external signals – Stationary current at power off – Max 2μA
- Cascade connection – two device connected: V_{IN} =-5V, V_{OUT} =-20V
- On-chip C-R oscillator
- Package................SCI7661C·····14-pin DIP (plastic)
  SCI7661M·····14-pin SOP (plastic)

■BLOCK DIAGRAM



■PIN CONFIGURATION



The same pin configuration in DIP and SOP

■PIN DESCRIPTION

Terminal	No.	Functions
CAP1+, CAP1-	1, 2	Terminal for connection of capacitor for doubler
CAP2+, CAP2-	3, 4	Terminal for connection of capacitor for tripler
TC1, TC2	5, 6	Temperature gradient selection terminal
V_{IN}	7	Power supply terminal (negative, system supply GND)
V_{OUT}	8	Output terminal at tripling
V_{reg}	9	Regulated voltage output terminal
$\overline{RV}$	10	Regulated voltage control terminal
$\overline{P_{off}}$	11	V_{reg} output ON/OFF control terminal
OSC2, OSC1	12, 13	Oscillation resistor connection terminal
V_{DD}	14	Power supply terminal (positive system supply V_{CC})

■ABSOLUTE MAXIMUM RATINGS

(V_{DD} =0V)

Parameter	Symbol	Ratings		Unit	Remarks
		Min	Max		
Input supply voltage	V_I	-20/N	0.5	V	N = 2: Doubler N = 3: Tripler
Input terminal voltage	V_I	V_{IN}-0.5	0.5	V	OSC1, $\overline{\text{Poff}}$
		V_{OUT}-0.5	0.5	V	TC1, TC2, RV
Output voltage	V_O	-20.0		V	
Allowable loss	P_d		300	mW	
Operating temperature	T_{opr}	-30	85	°C	Plastic package
Storage temperature	T_{stg}	-55	150	°C	

■ELECTRICAL CHARACTERISTICS

(V_{DD} =0V, V_{IN} =-5V, Ta=-30to85°C)

Parameter	Symbol	Ratings			Unit	Conditions
		Min	Typ	Max		
Input supply voltage	V_I	-6.0		-1.2	V	
Output voltage	V_O	-18.0			V	
	Vreg	-18		-2.6	V	$R_L = \infty$, R_{RV} = 1MΩ, V_O = -18V
Regulator operating voltage	V_{OUT}	-18.0		-3.2	V	
Booster current consumption	I_{opr1}		60	100	μA	$R_L = \infty$, Rosc = 1MΩ
Regulator current consumption	I_{opr2}		5.0	12.0	μA	$R_L = \infty$, R_{RV} = 1MΩ V_{OUT} = -15V
Stationary current	I_Q			2.0	μA	TC2 = TC1 = V_{OUT}, $R_L = \infty$
Oscillation frequency	fosc	16	20	24	kHz	Rosc = 1MΩ
Output impedance	R_{OUT}		150	200	Ω	I_{OUT} = 10mA
Booster power conversion efficiency	Peff	90	95		%	I_{OUT} = 5mA
Regulated output voltage fluctuation	$\frac{\Delta Vreg}{\Delta V_{OUT} \cdot Vreg}$		0.2		%/V	$-18V < V_{OUT} < -8V$, Vreg = -8V, $R_L = \infty$, Ta = 25°C
Regulated output load fluctuation	$\frac{\Delta Vreg}{\Delta I_{OUT}}$		5		Ω	V_{OUT} = -15V, Vreg = -8V, Ta = 25°C $0 < I_{OUT} < 10mA$, TC1=V_{DD} TC2 = V_{OUT}
Regulated output saturation resistance	R_{SAT}		8		Ω	$R_{SAT} = \Delta(Vreg - V_{OUT})/\Delta I_{OUT}$ $0 < I_{OUT} < 10mA$, RV = V_{DD}, Ta = 25°C
Reference voltage	V_{RV0}	−2.3	-1.5	−1.0	V	TC2 = V_{OUT}, TC1 = V_{DD}, Ta = 25°C
	V_{RV1}	−1.7	-1.3	−1.1	V	TC2 = TC1 = V_{OUT}, Ta = 25°C
	V_{RV2}	−1.1	-0.9	−0.8	V	TC2 = V_{DD}, TC1 = V_{OUT}, Ta = 25°C
Temperature Gradient	CT0	-0.25	-0.1	-0.06	%/°C	$CT = \frac{\lvert Vreg(50°C)\rvert - \lvert Vreg(0°C)\rvert}{50°C - 0°C} \times \frac{1}{\lvert Vreg(25°C)\rvert} \times 100$
	CT1	-0.5	-0.4	-0.3	%/°C	
	CT2	-0.7	-0.6	-0.5	%/°C	
Input leakage current	I_L			2.0	μA	$\overline{\text{Poff}}$, TC1, TC2, OSC1, RV pins

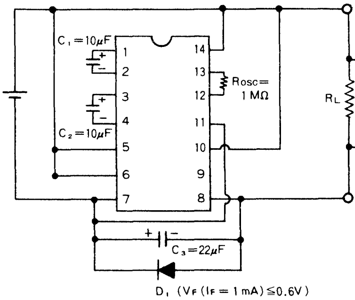
■RECOMMENDED OPERATING CONDITIONS

(Ta = -30 ~ 85°C)

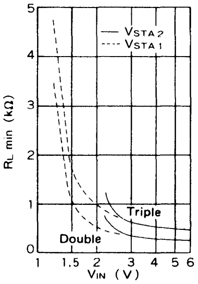
Parameter	Symbol	Ratings		Unit	Remarks
		Min	Max		
Booster start voltage	V_{STA1}		-1.2	V	R_{OSC} = 1MΩ, $C_3 \geqq 10\mu F$ *2 $C_L/C_3 \leqq 1/20$, Ta = -20to85°C
	V_{STA2}		-2.2	V	R_{OSC} = 1 MΩ
Booster stop voltage	V_{STP}	-1.2		V	R_{OSC} = 1 MΩ
Output load resistance	R_L	R_L min *3		Ω	
Output load current	I_{OUT}		20	mA	
Oscillation frequency	f_{OSC}	10	30	kHz	
Extarnal resistance for oscillation	R_{OSC}	680	2000	kΩ	
Capasitor for booster	C_1, C_2, C_3	3.3		μF	
Regulated output adjustable resistance	R_{RV}	100	1000	kΩ	

*1 V_{DD} =0V

*2 Recommended circuity in low voltage operation is shown below (VIN =-1.2V~-2.2V)



*3 R_L min depends on input voltage as shown below.



■PERFORMANCE CURVES

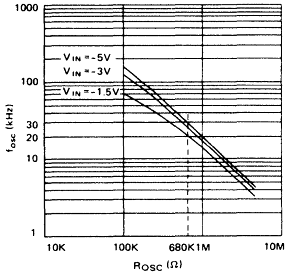


Fig. 1 Oscillation Frequency (fosc) vs. External - Resistance (Rosc)

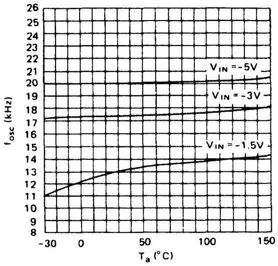


Fig. 2 Oscillation Frequency (fosc) vs. Temperature (Ta)

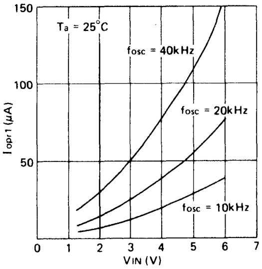


Fig. 3 Input Voltage (VIN) vs. Booster Current Consumption (Iopr1)

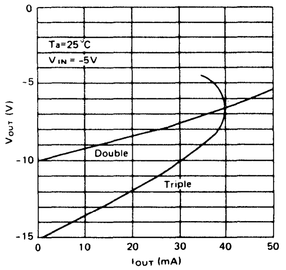


Fig. 4 Output Voltage (VOUT) vs. Output Current (IOUT)

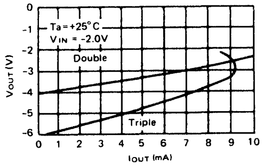


Fig. 5 Output Voltage (VOUT) vs. Output Current (IOUT)

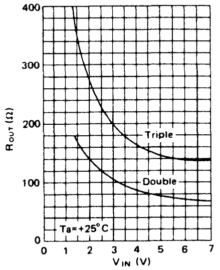


Fig. 6 Output Impedance (ROUT) vs. Input Voltage (VIN)

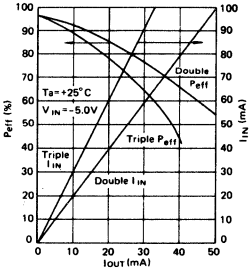


Fig. 7 Power Conversion Efficiency (Peff)/Input Current (IIN) vs. Output Current (IOUT)

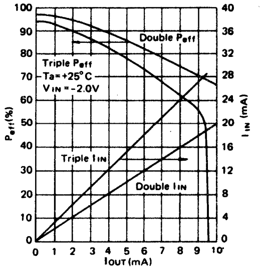


Fig. 8 Power Conversion Efficiency (Peff)/Input Current (IIN) vs. Output Current (IOUT)

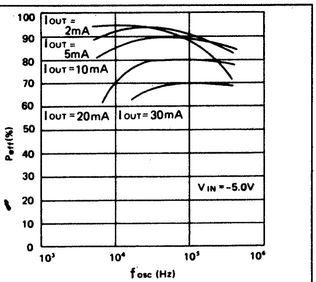


Fig. 9 Power Conversion Efficiency (Peff) vs. Oscillation Frequency (fosc)

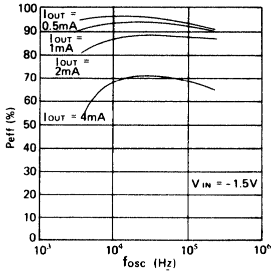


Fig. 10 Power Conversion Efficiency (Peff) vs. Oscillation Frequency (fosc)

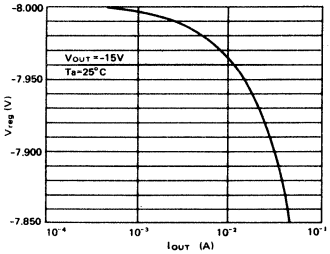


Fig. 11 Output Voltage (Vreg) vs. Output Current (IOUT)

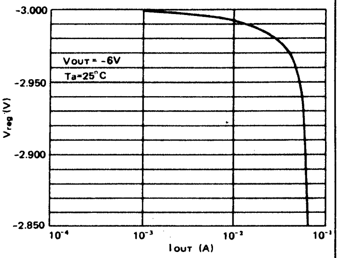


Fig. 12 Output Voltage (Vreg) vs. Output Current (IOUT)

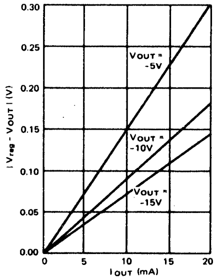


Fig. 13 Regulated Output Saturation Resistance (RSAT) |Vreg - VOUT| — IOUT

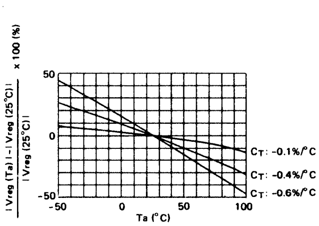
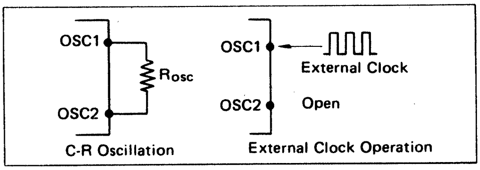


Fig. 14 Output Voltage (Vreg) vs. Temperature (Ta)

■CIRCUIT DESCRIPTION

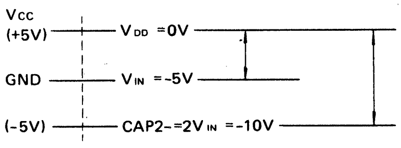
● C-R Oscillator

The SCI7661C contains a C-R oscillator for internal oscillation. It consists of an external resistor Rosc connected between the OSC1 pin and OSC2 pin.

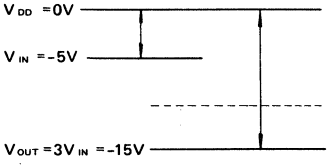


● Voltage Converters

The voltage converters double/triple the input supply voltage (VIN) using clocks generated by the C-R oscillator.

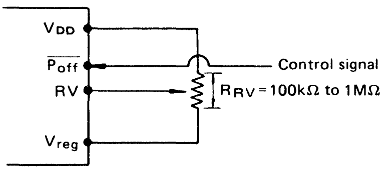


Typical Doubled Voltage Relations



Typical Tripled Voltage Relations

- **Reference Voltage Generator and Voltage Regulator**
  The reference voltage generator produces reference voltage needed for operation of regulator circuit. The voltage regulator is used to regulate a boosted output voltage and its circuit contains a power-off function which uses signals from the system for on-off control of the V_{reg} output.



Voltage Regulator

- **Temperature Gradient Selector Circuit**
  The SCI7661C provides the V_{reg} output with a temperature gradient suitable for LCD driving.

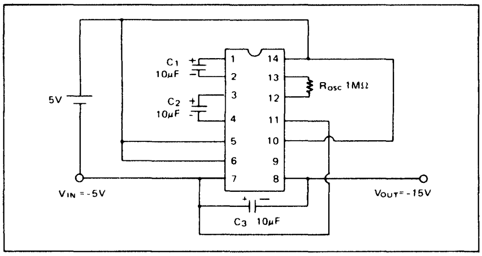
- **Temperature Gradient Assignment**

$\overline{P_{off}}$	TC2	TC1	Temp. Gradient	V_{reg} Output	CR oscillation	Remarks
1 (V_{DD})	L (V_{OUT})	L (V_{OUT})	-0.4%/°C	ON	ON	
1	L	H (V_{DD})	-0.1%/°C	ON	ON	
1	H (V_{DD})	L	-0.6%/°C	ON	ON	
1	H	H	-0.6%/°C	ON	OFF	Cascade connection
0 (V_{IN})	L	L	–	OFF (Hi-Z)	OFF	
0	L	H	–	OFF (Hi-Z)	OFF	
0	H	L	–	OFF (Hi-Z)	OFF	
0	H	H	–	OFF (Hi-Z)	ON	Without regulation

NOTE: The potential at Low level is different between the $\overline{P_{off}}$ pin and the TC1/TC2 pin.

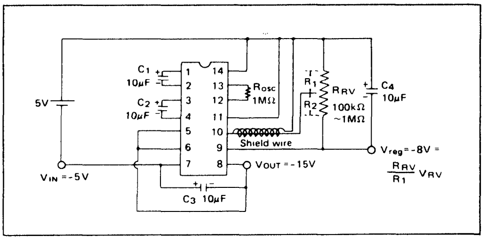
■EXAMPLE OF APPLICATIONS

- **Voltage Doubler and Tripler**
  A doubled voltage can be obtained at V_{OUT} (CAP2-) by disconnecting capacitor C_2 from the tripler configuration and shorting CAP2– (pin 4) and V_{OUT} (pin 8).



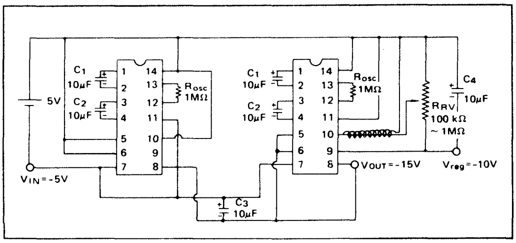
Voltage Tripler

- **Voltage Tripler + Regulator**
  V_{reg} output is given a temperature gradient, after boosted output V_{OUT} regulated. In this connection, both V_{OUT} and V_{reg} can be taken out at the same time.



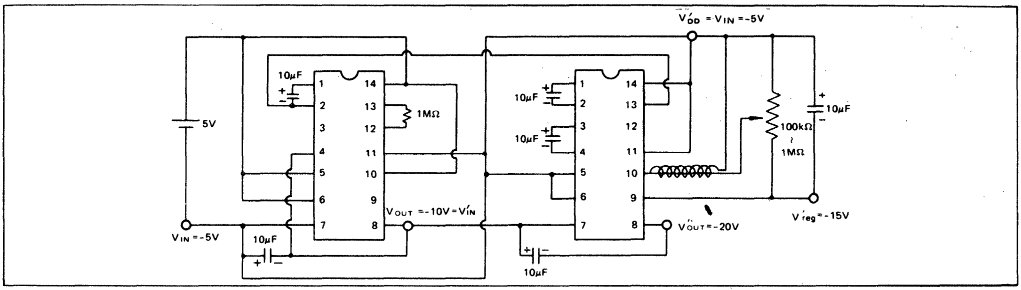
Tripler + Regulator
(-0.4%/°C selected as temperature gradient)

- **Parallel Connection**
  Parallel connection of n circuits can reduce R_{out} to about 1/n, that output impedance R_{out} can be reduced by connecting serial configuration. A single smoothing capacitor C_3 can be used commonly for all parallely connected circuit.
  In parallely connection, a regulated output can be obtained by applying the regulation circuit to only one of the n parallely connected circuit.



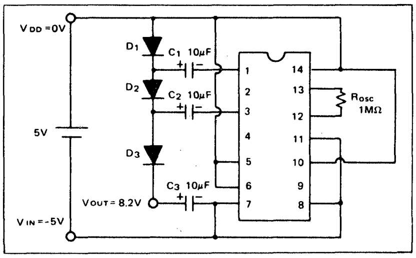
Parallel Connection

- **Cascade Connection**
  Cascade connection of SCI7661C (by connecting V_{IN} and V_{OUT} of one stage to V_{DD} and V_{IN} respectively of the next stage) further increase the output voltage. Note, however, that the serial connection increases the output impedance.



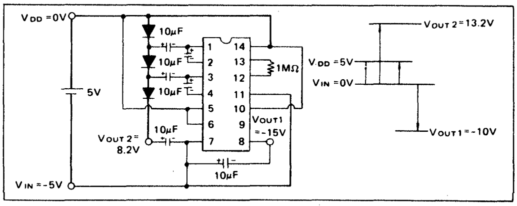
Serial Connection

- **Positive Voltage Conversion**
  The input voltage can be doubled or tripled toward the positive side. (In the doubler configuration, capacitor C2 and diode D3 are disconnected and the diode D3 shorted at the both ends.) In this case, however, the output voltage decrease by V_F (forward voltage).
  For example V_{DD} =0V, V_{IN} =-5V and V_F=0.6V, then V_{OUT} =10V -3 x 0.6V=8.2V (if doubled, 5V-2 x 0.6V= 3.8V)



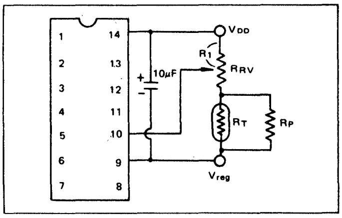
Positive Voltage Conversion D1, D2, D3: Shottky diodes with small V_F are recommended.

- **Negative Voltage Conversion + Positive Voltage Conversion**
  This circuit produces outputs of -15V and +8.2V from the -5V input. Note that this configuration causes higher output impedance than in a single function (negative or positive voltage converter).



Negative Voltage Convertion + Positive Voltage Conversion

- **Changing the Temperature Gradient through Use of External Temperature Sensor (Thermistor)**
  The SCI7661C has a temperature gradient selector circuit in its regulator. It selects any one of the three gradients: -0.1%/°C, -0.4%/°C and -0.6%/°C. It is necessary that the temperature gradient can be changed to any other value by connecting a thermistor in series to the output voltage control resistor R_{RV}.

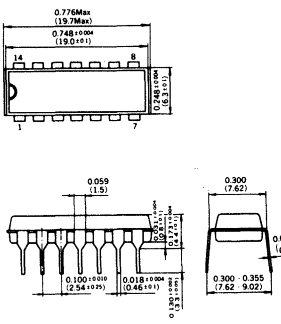


Example of Change of Temperature Gradient

■PACKAGE DIMENSIONS

C14

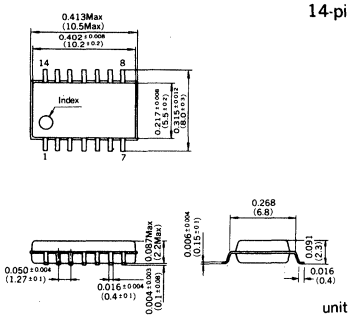
14-pinDIP



unit : inch
(mm)

M14

14-pin SOP



unit : inch
(mm)

SED3064F

CMOS 8×8 ANALOG SWITCH ARRAY

- **Low ON state resistance**
- **Built-in address decoder and control memory for switches**

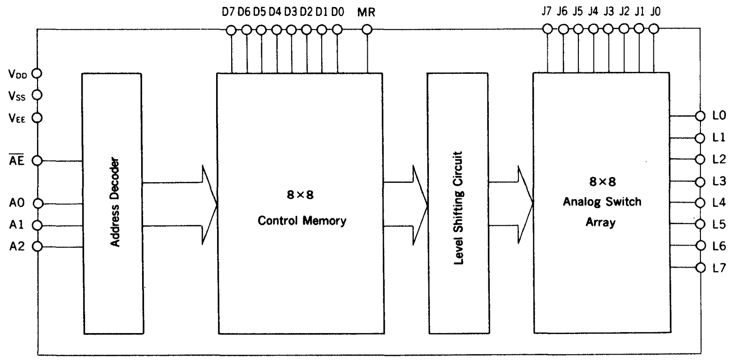
■DESCRIPTION

The SED3064F is a CMOS LSI 8×8 analog switch array incorporating a built-in address decoder and memory control for switches, moreover, with data reset mechanism for each switch. This circuit consists of 64 cross point switches in 8×8 array. Any one of the cross points can be selected, and can be turned on or off. Either analog or digital power supply is applied to the circuit depends on the DC voltage level of signals. Since the difference of "ON" resistance values between each switch on circuit is very small, change in (voltage) level for signals can be minimized.

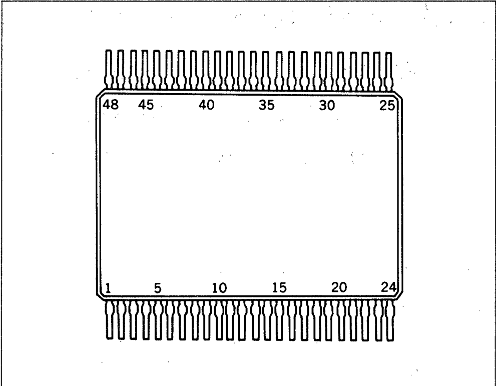
■FEATURES

- 8×8 analog switch array
- Low "ON" state resistance……………………125Ω Max at $V_{DD}-V_{EE}=10V$
- Maximum rating voltage……………………$V_{DD}-V_{SS}=7V$ (on any logic pin)
  $V_{DD}-V_{EE}=13V$
  (On any junctor or line)
- Built-in address decoder and control memory
- Separated power supply for switch array and logic circuit.
- "ON" resistance allowance……………………25Ω (Max)
- Package……………………………………48-pin QFP (plastic)

■BLOCK DIAGRAM



■PIN CONFIGURATION



Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
1	MR	13	D3	25	L3	37	NC
2	NC	14	D2	26	L2	38	NC
3	$\overline{AE}$	15	D1	27	L1	39	J4
4	V_{EE}	16	D0	28	L0	40	J5
5	NC	17	NC	29	NC	41	J6
6	NC	18	NC	30	NC	42	J7
7	D7	19	NC	31	NC	43	NC
8	D6	20	NC	32	NC	44	V_{DD}
9	D5	21	L7	33	J0	45	A0
10	D4	22	L6	34	J1	46	A1
11	NC	23	L5	35	J2	47	A2
12	NC	24	L4	36	J3	48	V_{SS}

■PIN DESCRIPTION

A0 to A2	Control memory address input
$\overline{AE}$	Control memory address enable input
MR	Master reset input
D0 toD7	Control memory data input
J0 to J7	Analog switch array input/output (junctor)
L0 to L7	Analog switch array input/output (line)
V_{DD}	Positive analog/digital power supply
V_{SS}	Negative digital power supply
V_{EE}	Negative analog power supply
NC	No connection

■ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Supply voltage	$V_{DD}-V_{SS}$	−0.3 to 7	V
	$V_{DD}-V_{EE}$	−0.3 to 16	V
	$V_{SS}-V_{EE}$	−0.3 to 16	V
Input voltage	V_I	$V_{SS}-0.3$ to $V_{DD}+0.3$ $V_{EE}-0.3$ to $V_{DD}+0.3$	V
Power dissipation	P_D	250	mW
Operating temperature	T_{opr}	−40 to 85	℃
Storage temperature	T_{stg}	−65 to 150	℃
Soldering temperature and time	T_{sol}	260℃, 10s (at lead)	—

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

($V_{DD}=5V$, $V_{SS}=0V$, $V_{EE}=-5V$, Ta=25℃ Unless Specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage						
Digital	$V_{DD}-V_{SS}$		4.5	5	7	V
Analog	$V_{DD}-V_{EE}$		4.5	10	13	V
On state resistance	R_{ON}	$V_{Jn}-V_{Ln}=0.6V$ ($n=0, \cdots, 7$)	—	90	125	Ω
Difference in on state (resistance between any switches)	$\triangle R_{ON}$		—	—	25	Ω
Input/Output off state leakage current	I_{OFF}		—	±0.02	±100	nA
Input voltage	V_{IL}		—	—	1.5	V
	V_{IH}		3.5	—	—	V
Quiescent device current	I_Q		—	0.1	10	μA

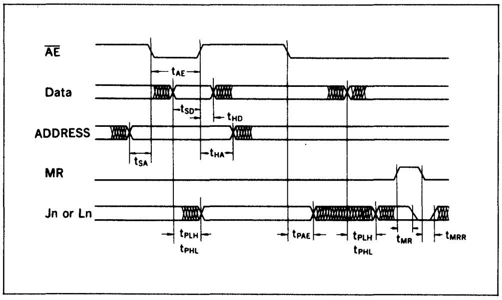
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Maximum current through cross point switch	I_{Max}		—	±8.0	—	mA
Switch input capacitance	C_{IL}	$V_{in}=0V$	—	100	—	pF
Switch output capacitance	C_{OJ}	$V_{in}=0V$	—	110	—	pF
Feedthrough capacitance	C_{IOS}	$V_{in}=0V$	—	0.2	—	pF
Digital input capacitance	C_{IN}	$V_{in}=0V$	—	5	—	pF

●AC Electrical Characteristics

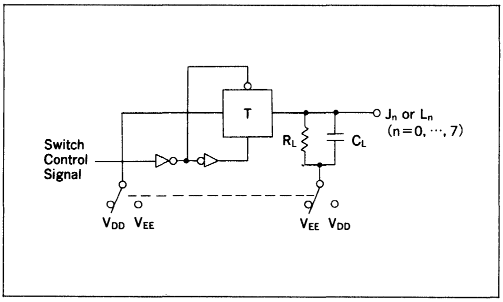
($V_{DD}=5V$, $V_{SS}=0V$, $V_{EE}=-5V$, Ta=25°C Unless Specified)

Parameter		Symbol	Conditions		Min	Typ	Max	Unit
Sine wave response (Distortion)			$V_{is}=5V(P-P)$ $R_L=10k\Omega$ $f_{in}=1kHz$	$V_{DD}-V_{SS}=5V$ $V_{DD}-V_{EE}=13V$	—	0.1	—	%
				$V_{DD}-V_{SS}=5V$ $V_{DD}-V_{EE}=10V$	—	0.2	—	
				$V_{DD}-V_{SS}=5V$ $V_{DD}-V_{EE}=5V$	—	1.0	—	
Maximum frequency responce (Channel "ON") (Sine wave input)		f_{Max} (I-O)	$V_{is}=5V\ (P-P)$ $R_L=1k\Omega$ $(V_O/V_I)\ dB=-3dB$		—	40	—	MHz
Feedthrough (Channel "OFF")			$V_{is}=5V\ (P-P)$ $f_{in}=1MHz$ $R_L=1k\Omega$		—	−40	—	dB
Crosstalk between any two channels			$f_{in}=1MHz$		—	−40	—	dB
			$f_{in}=3.4kHz$ $R_L=1k\Omega$		—	−90	—	
Propagation delay time signal input to signal output (Jn−Ln)		t_{PS}	Switch "ON" $C_L=50pF$ $R_L=10k\Omega$ $t_r=t_f=20ns$ (input signal)		–	10	–	ns
Turn "ON" propagation delay data input to signal output (Dn−Jn or Ln)		t_{PLH} t_{PHL}	$C_L=50pF$ $R_L=10k\Omega$ $t_r=t_f=20ns$ (input signal)		—	120	400	ns
Address enable to signal output ($\overline{AE}$−Jn or Ln)		t_{PAE}	$C_L=50pF$ $R_L=10k\Omega$ $t_r=t_f=20ns$ (input signal)		—	150	600	ns
Minimum address enable pulse width		t_{AE}			—	30	80	ns
Minimum set up time	Address to $\overline{AE}$	t_{SA}			0	50	80	ns
	Data in to $\overline{AE}$	t_{SD}			0	50	80	ns
Minimum hold time	Address to $\overline{AE}$	t_{hA}			0	50	80	ns
	Data in to $\overline{AE}$	t_{hD}			0	50	80	ns
Memory reset time		t_{MR}	$C_L=50pF$ $R_L=1k\Omega$		—	100	380	ns
Memory reset recovery time		t_{MRR}	$C_L=50pF$ $R_L=1k\Omega$		—	200	380	ns

●Timing Chart



●AC Electrical Measurement Circuit



■DESCRIPTION FOR MECHANISM

●Address Decoder

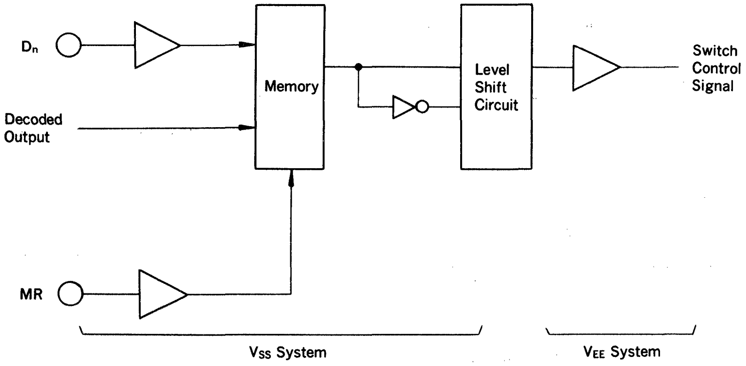
8 address lines are decoded by the combination of three ADDRESS (A0, A1, A2) inputs when the ADDRESS ENABLE ($\overline{AE}$) is Low. The control memory is selected with the decoded output. All switches have corresponding control memory provided with data reset for each. A "1" written into a memory cell turns the corresponding crosspoint switch"ON" while a "0" causes the cross point to turn"OFF". Since the ADDRESS LINE (Ln, n=0 to 7) is corresponding to Analog Switch Array output. J0−L0 is turned on by selecting L0 (A0="L", A1="L", A2="L") for ADDRESS LINE, and also inputting "1" to D0 for INPUT DATA.

MR	$\overline{AE}$	ADDRESS			ADDRESS LINE	INPUT DATA								MEMORY CONTENT							
		A2	A1	A0		D7	D6	D5	D4	D3	D2	D1	D0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
H	X	X	X	X	all	X	X	X	X	X	X	X	X	L	L	L	L	L	L	L	L
L	H	X	X	X	none	X	X	X	X	X	X	X	X	NO CHANGE OF STATE							
L	L	L	L	L	L0	d7	d6	d5	d4	d3	d2	d1	d0	d7	d6	d5	d4	d3	d2	d1	d0
L	L	L	L	H	L1				↑								↑				
L	L	L	H	L	L2																
L	L	L	H	H	L3																
L	L	H	L	L	L4																
L	L	H	L	H	L5																
L	L	H	H	L	L6																
L	L	H	H	H	L7																

X: Don't care condition
di (i=0 to 7): Data (either "1" or "0")

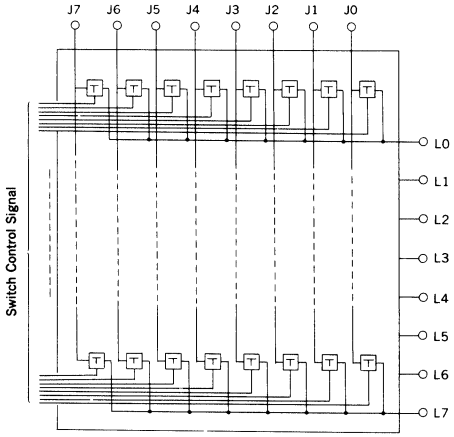
●Control Memory

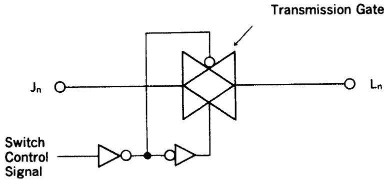
When the previous decoded output is fixed to high level, Dn (n=0 to 7) the INPUT DATA is read in.
"1" written into INPUT DATA turns the corresponding crosspoint switch "ON" while "0" causes the crosspoint to turn "OFF".
Since Control Memory provided with DATA RESET is corresponding to each switch one-to-one, it is possible to fix every switch to either "ON" or "OFF".



●Switch

On chip 8×8 Analog Switch Array is controlled by the output of the previous control memory.

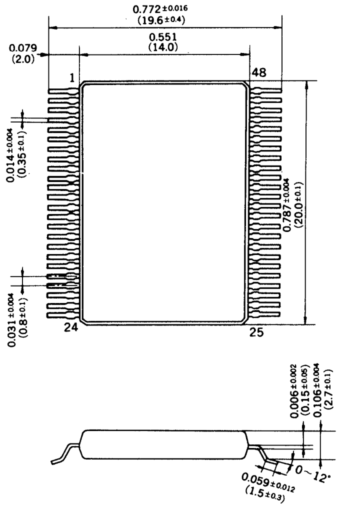




■PACKAGE DIMENSIONS

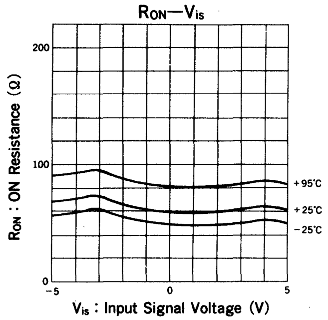
F48-5

48-pin QFP

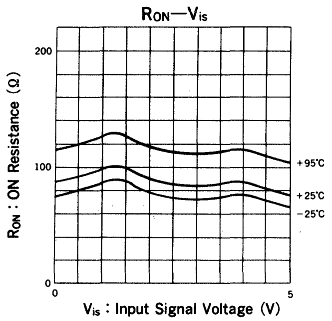


unit : inch
(mm)

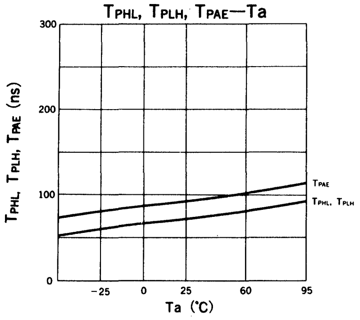
■PERFORMANCE CURVES



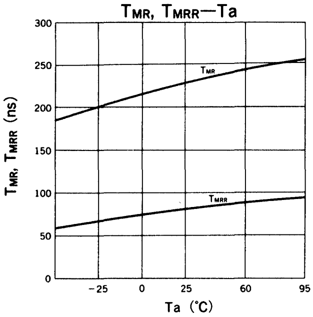
R_{ON} ($V_{DD}=5V$, $V_{SS}=0V$, $V_{EE}=-5V$)



R_{ON} ($V_{DD}=5V$, $V_{SS}=V_{EE}=0V$)



$T_{PLH,PHL}$, T_{PAE} Temperature Characteristic
($V_{DD}=5V$, $V_{SS}=0V$, $V_{EE}=-5V$)



T_{MR}, T_{MRR} Temperature Characteristic
($V_{DD}=5V$, $V_{SS}=0V$, $V_{EE}=-5V$)

SEA7000H

MOS AREA IMAGE SENSOR

- **2/3-inch Size Solid State Imaging Device**
- **244 (Horizontal) × 244 (Vertical) Photo Sensor Incorporated**

■DESCRIPTION

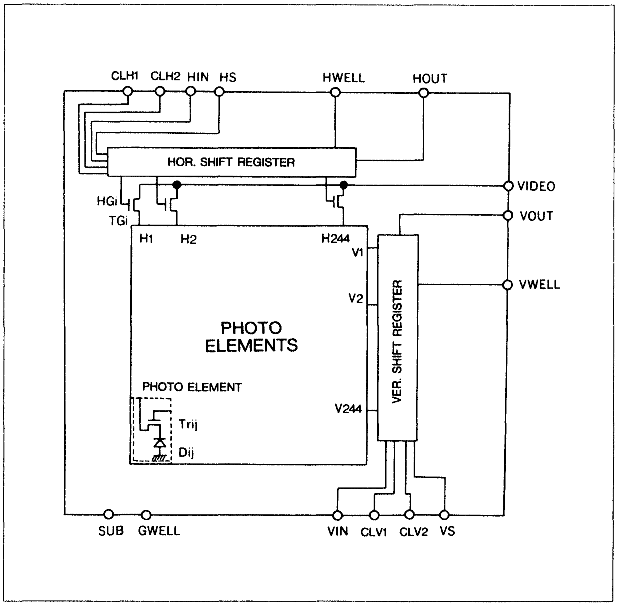
The SEA7000H is a MOS area image sensor designed for use with black-and-white video cameras. Implemented in unique technology, the sensor features suppressed blooming and low noise.

Because of the 2/3-inch size, the SEA7000H can be used with low-cost standard lenses. Combining it with a dedicated synchronization control LSI enables the user to easily build a compact video camera with high packaging density.

■FEATURES

- ●Photo elements······244 (horizontal) × 244 (vertical)
- ●Resolution ······················180 TV lines (horizontal) × 180 TV lines (vertical)
- ●Low voltage operation (7V) and low power consumption (70mW)
- ●Blooming suppressed by special technology
- ●Light-receiving area·················8.8 mm × 6.6 mm
- ●Peripheral circuits supported by dedicated synchronization control LSI
- ●Highly resistant to vibration and shock (operable under vibration)
- ●Package ···················20-pin DIP (ceramic) with optical glass

■BLOCK DIAGRAM



■CIRCUIT CONFIGURATION

The SEA7000H consists of three blocks : photo element (photo diode cell) block, horizontal shift register block, and vertical shift register block.

●Photo element block

244 selection lines V1 through V244 run horizontally and 244 signal lines H1 through H244 run vertically. A photo element consisting of a MOS transistor Trij and a photo diode Dij is located at each crossing point.

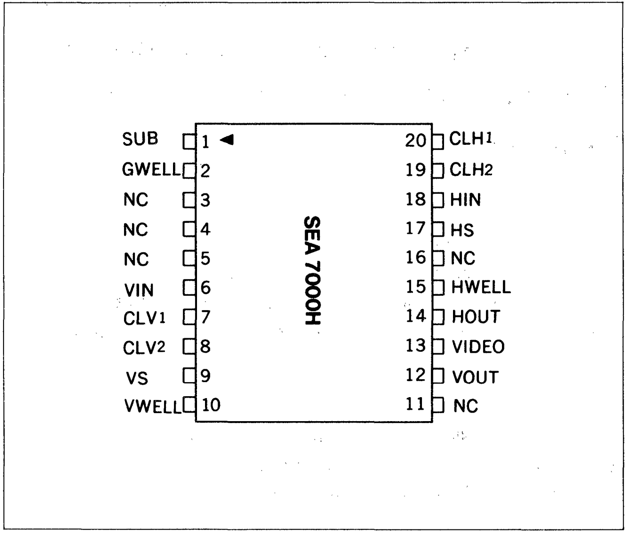
●Horizontal shift register block

This block consists of 488 bit shift registers and MOS transistors TGi that are controlled with the output HGi of each bit as the gate signal.

●Vertical shift register block

The vertical shift register block consists of 244 bit shift registers. The output of each bit becomes the scanning line Vj.

■PIN CONFIGURATION



■PIN DESCRIPTION

Pin No.	Terminal	Function
1	SUB	Board voltage
2	GWELL	Well voltage
6	VIN	Vertical S. R. input
7	CLV1	Vertical S. R. clock 1
8	CLV2	Vertical S. R. clock 2
9	VS	Vertical S. R. source
10	VWELL	Ground voltage (V)
12	VOUT	Shift register output
13	VIDEO	Video output
14	HOUT	Horizontal S. R. output
15	HWELL	Ground voltage (H)
17	HS	Horizontal S.R. source
18	HIN	Horizontal S.R. input
19	CLH2	Horizontal S.R. clock 2
20	CLH1	Horizontal S.R. clock 1
3, 4, 5, 11, 16	NC	No connection

■ABSOLUTE MAXIMUM RATINGS

(VWELL = HWELL = 0V, Ta = 25℃)

Parameter	Symbol	Ratings	Unit
Terminal voltage (Horizontal S. R. input) *1	V_H	−0.3 to 10	V
Terminal voltage (Vertical S. R. input) *2	V_V	−0.3 to 10	V
Terminal voltage (Video bias)	V_{VIDEO}	−0.3 to 10	V
Operating temperature	T_{opr}	− 10 to 60	℃
Storage temperature	T_{stg}	− 20 to 80	℃
Soldering temperature/time	T_{sol}	260℃, 10s (lead only)	—

*1 : H_{IN}, CLH1, CLH2 *2 : V_{IN}, CLV1, CLV2

■ELECTRICAL CHARACTERISTICS

●Recommended Operating Conditions

(VWELL = HWELL = 0V, Ta = 25℃)

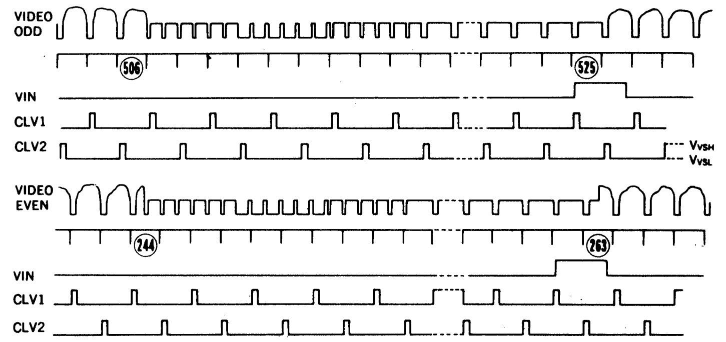
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Horizontal clock frequency	f_{CLH}	$V_{HSH} = 7V$	—	4.625	—	MHz
Vertical clock frequency	f_{CLV}	$V_{VSH} = 7V$	—	7.8	—	kHz
High level input voltage	V_{HSH}, V_{VSH}		—	7	—	V
Low level input voltage	V_{HSL}, V_{VSL}		—	0	—	V
GWELL voltage	V_{GWELL}		—	0.8	—	V
SUB voltage	V_{SUB}		—	7	—	V

●Opto-electrical Characteristics

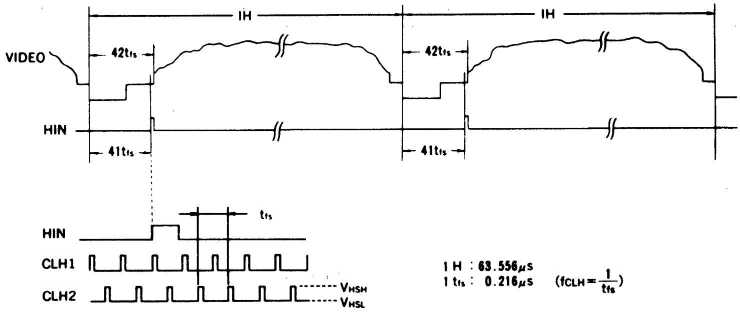
(VWELL = HWELL = 0V, Ta = 25℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Saturated light quantity	L_{sat}	$V_{VIDEO} = 3.0V$	—	0.33	—	lx·sec
Sensitivity	S	$V_{VIDEO} = 3.0V$	—	0.15	—	μA/lx
Horizontal resolution	R_H		—	180	—	TVline
Vertical resolution	R_V		—	180	—	TVline
Power consumption	P	$F_{CLH} = 4.625MHz$, $V_{HSH} = V_{VSH} = 7V$	—	70	—	mW

●Timing Chart



Vertical drive pulse

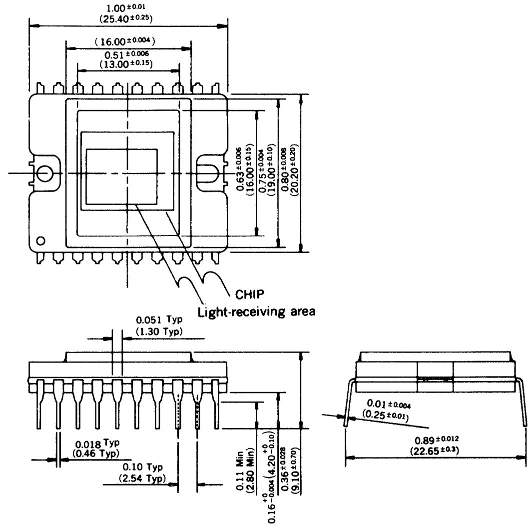


1 H : 63.556μs
1 tfs : 0.216μs $(f_{CLH} = \frac{1}{t_{fs}})$

Horizontal drive pulse

■PACKAGE DIMENSIONS

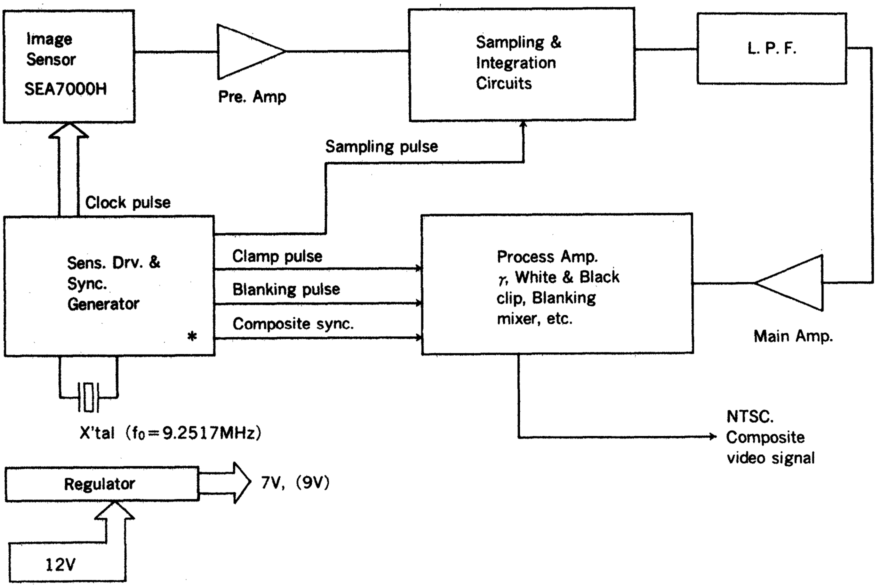
H20



20-pin DIP (ceramic)

unit : inch
(mm)

■EXAMPLE OF APPLICATION (Peripheral Circuit Configuration)



Video Camera Block Diagram

*:Sync. control LSI (flat plastic package) is available as a system support IC. (SED3081F$_{2T}$)

[Precaution to handle]

1. The image sensor SEA7000H is a MOS LSI, so protect it against electrostatic breakdown. Never touch the sensor without grounding your body and the tools. Connect a resistance of about 1MΩ between the body and GND in series to ensure safety.
2. Do not touch the glass surface of the device. Wipe the surface, if soiled, with a clean applicator.
3. Take care not to drop the device, which has a glass cap.

SEA7010H

MOS AREA IMAGE SENSOR

- 8 mm Size Solid State Imaging Device
- 244 (Horizontal) × 244 (Vertical) Photo Sensor Incorporated

■DESCRIPTION

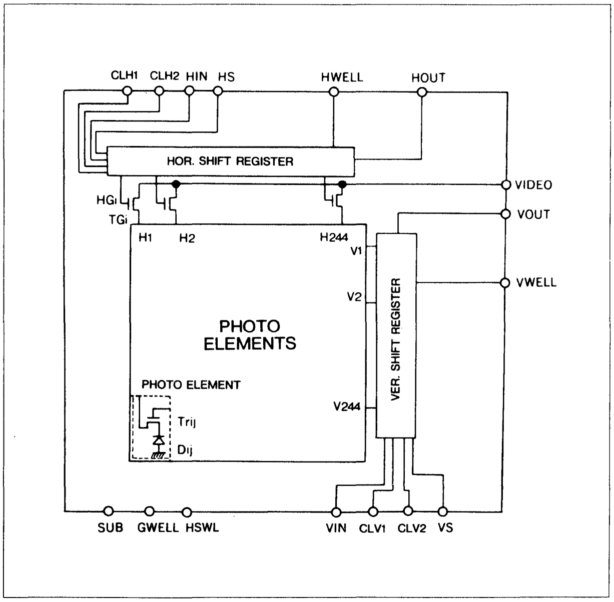
The SEA7010H is a MOS area image sensor designed for use with black-and-white video cameras. Implemented in unique technology, the sensor features suppressed blooming and low noise.

Because of its 8mm size, the SEA7010H can be used with low-cost standard lenses. Combining it with a dedicated synchronization control LSI enables the user to easily build a compact video camera with high packaging density.

■FEATURES

- Photo elements······244 (horizontal) × 244 (vertical)
- Resolution······················180 TV lines (horizontal) × 180 TV lines (vertical)
- Low voltage operation (7V) and low power consumption (50mW)
- Blooming suppressed by special technology
- Light-receiving area··8 mm Size (5.3 mm × 4.0 mm)
- Peripheral circuits supported by dedicated synchronization control LSI
- Highly resistant to vibration and shock (operable under vibration)
- Package·········20-pin Shrink DIP (ceramic) with optical glass

■BLOCK DIAGRAM

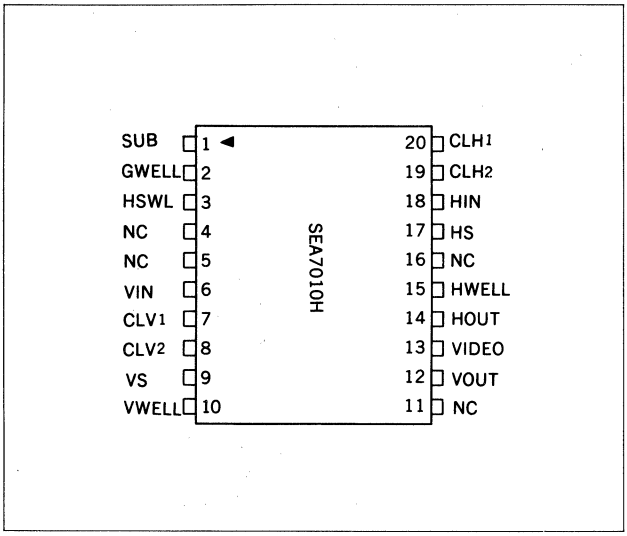


■CIRCUIT CONFIGURATION

The SEA7010H consists of three blocks : photo element (photo diode cell) block, horizontal shift register block, and vertical shift register block.

- **Photo element block**
  244 selection lines V1 through V244 run horizontally and 244 signal lines H1 through H244 run vertically. A photo element consisting of a MOS transistor Trij and a photo diode Dij is located at each crossing point.
- **Horizontal shift register block**
  This block consists of 488 bit shift registers and MOS transistors TGi that are controlled with the output HGi of each bit as the gate signal.
- **Vertical shift register block**
  The vertical shift register block consists of 244 bit shift registers. The output of each bit becomes the scanning line Vj.

■PIN CONFIGURATION



■PIN DESCRIPTION

Pin No.	Terminal	Function
1	SUB	Board voltage
2	GWELL	Well voltage
3	HSWL	Reset pulse voltage
6	VIN	Vertical S.R. input
7	CLV1	Vertical S.R. clock 1
8	CLV2	Vertical S.R. clock 2
9	VS	Vertical S.R. source
10	VWELL	Ground voltage (V)
12	VOUT	Shift register output
13	VIDEO	Video output
14	HOUT	Horizontal S.R. output
15	HWELL	Reset pulse voltage
17	HS	Horizontal S.R. source
18	HIN	Horizontal S.R. input
19	CLH2	Horizontal S.R. clock 2
20	CLH1	Horizontal S.R. clock 1
4, 5 11, 16	NC	No connection

■ABSOLUTE MAXIMUM RATINGS

(VWELL = HWELL = 0V, Ta = 25°C)

Parameter	Symbol	Ratings	Unit
Terminal voltage (Horizontal S. R. input) *1	V_H	−0.3 to 10	V
Terminal voltage (Vertical S. R. input) *2	V_V	−0.3 to 10	V
Terminal voltage (Video bias)	V_{VIDEO}	−0.3 to 10	V
Operating temperature	T_{opr}	− 10 to 60	℃
Storage temperature	T_{stg}	− 20 to 80	℃
Soldering temperature/time	T_{sol}	260℃, 10s (lead only)	—

*1 : H_{IN}, CLH1, CLH2 *2 : V_{IN}, CLV1, CLV2

■ELECTRICAL CHARACTERISTICS

●Recommended Operating Conditions

(VWELL = HWELL = 0V, Ta = 25°C)

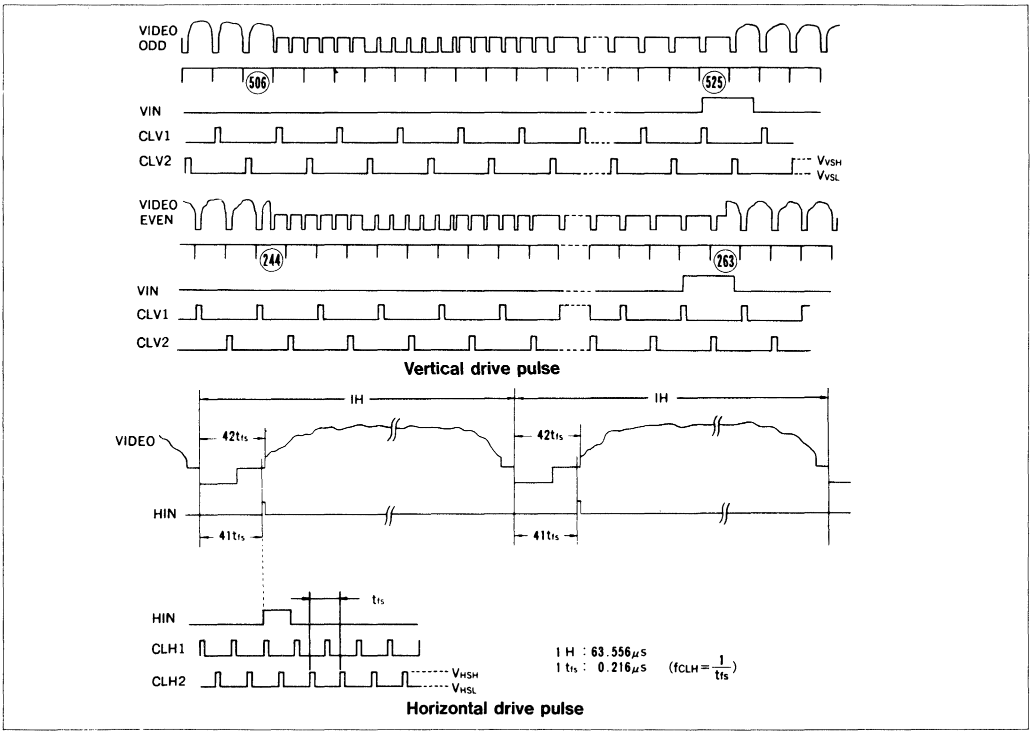
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Horizontal clock frequency	f_{CLH}	$V_{HSH} = 7V$	—	4.625	—	MHz
Vertical clock frequency	f_{CLV}	$V_{VSH} = 7V$	—	7.8	—	kHz
High level input voltage	V_{HSH}, V_{VSH}		6.5	7	7.5	V
Low level input voltage	V_{HSL}, V_{VSL}		0	0	0.1	V
GWELL voltage	V_{GWELL}		0.6	0.8	1.0	V
SUB voltage	V_{SUB}	$V_{SUB} \geqq V_{HSH}$, V_{VSH}	6.5	7	7.5	V
Reset high level input voltage	V_{HWL}		0.65	—	0.75	V
Reset low level input voltage	V_{LWL}		0	—	0.05	V

●Opto-electrical Characteristics

(VWELL = HWELL = 0V, Ta = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Saturated light quantity	L_{sat}	$V_{VIDEO} = 3.0V$	—	0.9	—	lx•sec
Sensitivity	S	$V_{VIDEO} = 3.0V$	—	40	—	nA/lx
Horizontal resolution	R_H		—	180	—	TVline
Vertical resolution	R_V		—	180	—	TVline
Power consumption	P	$F_{CLH} = 4.625MHz$, $V_{HSH} = V_{VSH} = 7V$	—	—	50	mW

●Timing Chart



Vertical drive pulse

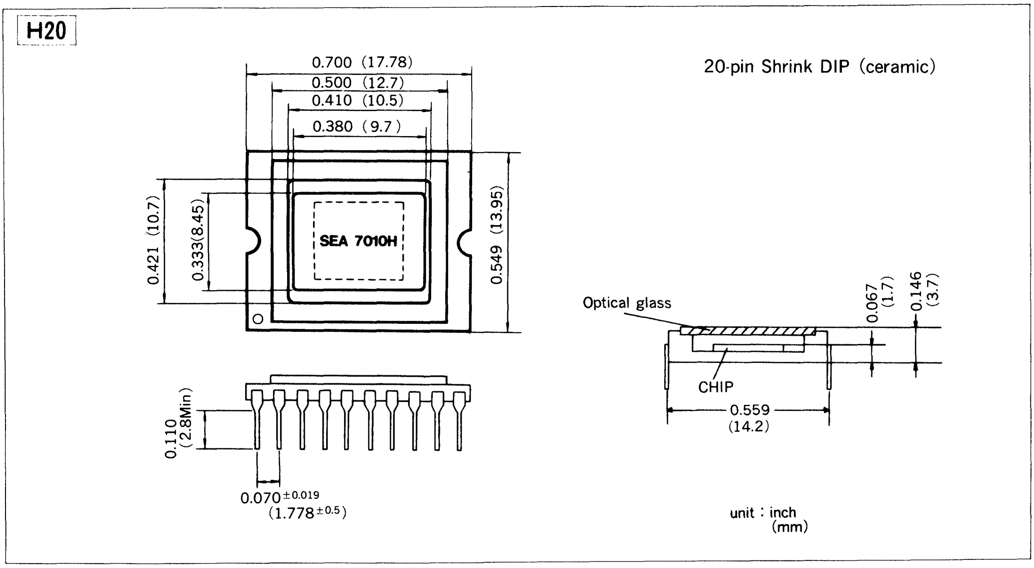
1 H : 63.556μs
1 tfs : 0.216μs (fCLH = $\frac{1}{tfs}$)

Horizontal drive pulse

■PACKAGE DIMENSIONS

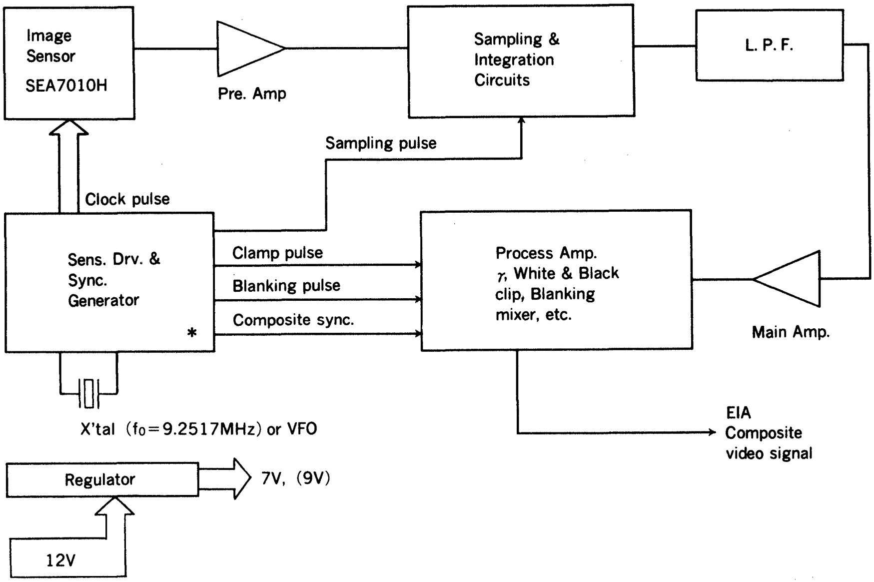
H20

20-pin Shrink DIP (ceramic)



unit : inch (mm)

■EXAMPLE OF APPLICATION (Peripheral Circuit Configuration)



Video Camera Block Diagram

* Sync. control LSI (flat plastic package) is available as a system support IC. (SED3081F$_{2T}$)

[Precaution to handle]

1. The image sensor SEA7010H is a MOS LSI, so protect it against electrostatic breakdown. Never touch the sensor without grounding your body and the tools. Connect a resistance of about 1MΩ between the body and GND in series to ensure safety.
2. Do not touch the glass surface of the device. Wipe the surface, if soiled, with a clean applicator.
3. Take care not to drop the device, which has a glass cap.

SEA7100H

MOS AREA IMAGE SENSOR

- ●High Resolution
- ●384 (Horizontal)×485 (Vertical) Photo Sensors Incorporated
- ●2/3-inch Size Solid State Imaging Device

■DESCRIPTION

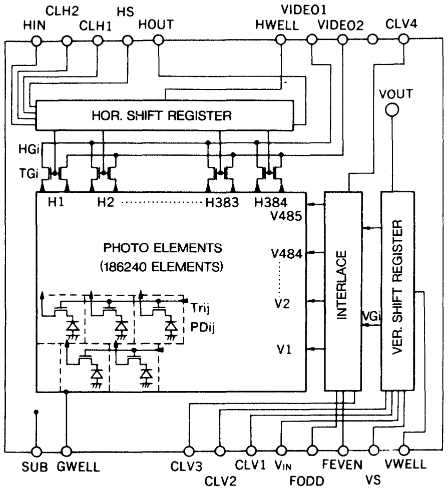
The SEA7100H is a high-density MOS area image sensor designed for use with black-and-white video cameras. Implemented in unique technology, the sensor features suppressed blooming and low noise.

Because of the 2/3-inch size, the SEA7100H can be used with low-cost standard lenses. Combining it with a dedicated synchronization control LSI enables the user to easily build a compact video camera with high packaging density.

■FEATURES

- ●Photo elements······················384(horizontal)×485(vertical)
- ●Resolution··············450TV lines(horizontal)×350 TV(vertical)
- ●Photo elements arranged in a checkered pattern, and two-line simultaneous reading which permits photo element interpolation
- ●Low voltage operation (7V) and low power consumption (70mW)
- ●Blooming suppressed by special technology
- ●Light-receiving area································8.8mm×6.6mm
- ●Peripheral circuits supported by dedicated synchronization control LSI
- ●Highly resistant to vibration and shock (operable under vibration)
- ●Package····················20-pin DIP(ceramic) with optical glass

■BLOCK DIAGRAM



■CIRCUIT CONFIGURATION

The SEA 7100H consists of three blocks : photo element (photo diode cell) block, horizontal shift register block, and vertical shift register block (including the interlace).

●Photo element block

Photo elements are arranged in a checkered pattern : [384 elements horizontal] × [485 elements vertical] = [186240 elements]. 485 selection lines VI through V485 run horizontally and 384 × 2signal lines H1 through H384 (pair lines) run vertically. A photo element consisting of a MOS transistor Trij and a photo diode Dij is located at each crossing point.

●Horizontal shift register block

This block consists of 768 bit shift registers and MOS transistors TGi that are controlled with the output HGi of each bit as the gate signal.

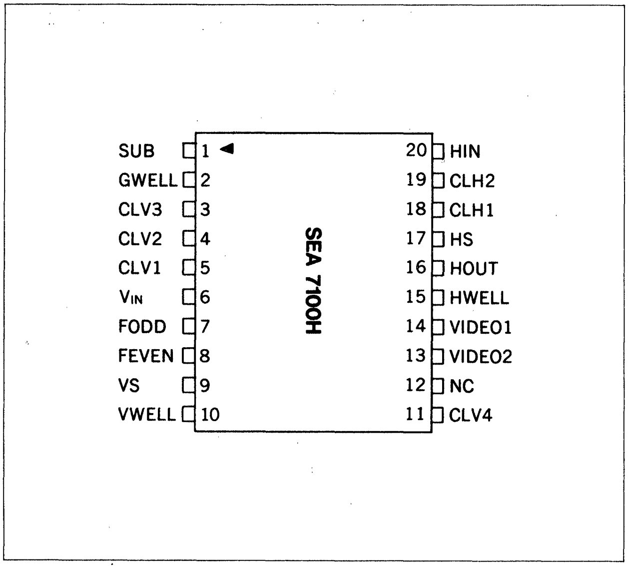
●Vertical shift registers

485 shift registers are provided. Output VGj of each bit is supplied to the interlace part.

●Interlace

This part receives vertical shift register output VGj, and converts it for interlacing. This output is scanning line Vj.

■PIN CONFIGURATION



■PIN DESCRIPTION

Pin NO.	Pin name	Function
1	SUB	Board voltage
2	GWELL	Well voltage
3	CLV3	I.L. CLOCK 3
4	CLV2	Vertical S.R. clock 2
5	CLV1	Vertical S.R. clock 1
6	V_{IN}	Vertical S.R. input
7	FODD	I.L. clock (odd field signal)
8	FEVEN	I.L. clock (even field signal)
9	VS	Vertical S.R. source
10	VWELL	Ground voltage (V)
11	CLV4	I.L. clock 4
12	NC	No connection
13	VIDEO2	Video output 2
14	VIDEO1	Video output 1
15	HWELL	Ground voltage (H)
16	HOUT	Horizontal S.R. output
17	HS	Horizontal S.R. source
18	CLH1	Horizontal S.R. clock 1
19	CLH2	Horizontal S.R. clock 2
20	HIN	Horizontal S.R. input

■ABSOLUTE MAXIMUM RATINGS

(VWELL=HWELL=0V, Ta=25℃)

Parameter	Symbol	Ratings	Unit
Terminal voltage (Horizontal shift register)*1	V_H	−0.3 to 10	V
Terminal voltage (Vertical shift register)*2	V_V	−0.3 to 10	V
Terminal voltage (Video bias)	V_{VIDEO}	−0.3 to 10	V
Operating temperature	T_{opr}	− 10 to 60	℃
Storage temperature	T_{stg}	− 20 to 80	℃
Soldering temperature/time	T_{sol}	260℃, 10s (lead only)	—

*1 : H_{IN}, CLH1, CLH2 *2 : V_{IN}, CLV1, CLV2

■ELECTRICAL CHARACTERISTICS

●Recommended Operating Conditions

(VWELL=HWELL=0V, Ta=25℃)

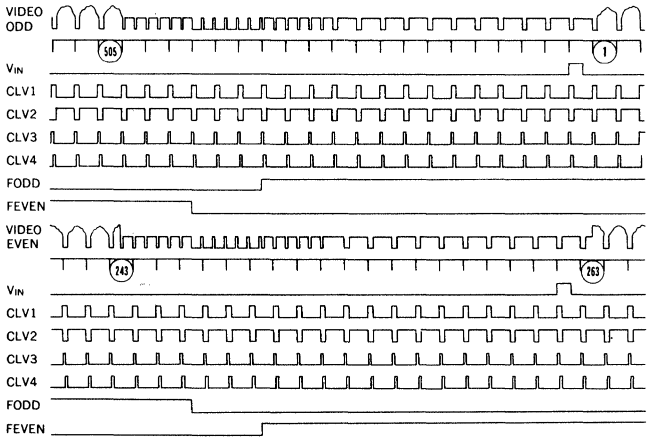
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Horizontal clock frequency	f_{CLH}	$V_{HSH}=7V$	—	7.16	—	MHz
Vertical clock frequency	f_{CLV}	$V_{VSH}=7V$	—	15.74	—	kHz
High level input voltage	V_{HSH},V_{VSH}		—	7	—	V
Low level input voltage	V_{HSL},V_{VSL}		—	0	—	V
GWELL voltage	V_{GWELL}		—	0.8	—	V
SUB voltage	V_{SUB}		—	7	—	V

●Opto-electrical Characteristics

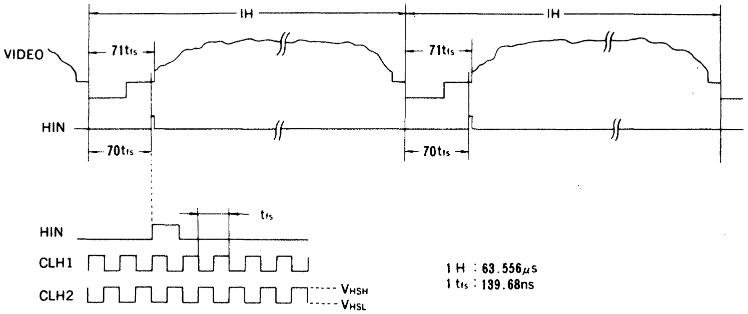
(VWELL=HWELL=0V, Ta=25℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Saturated light quantity	L_{sat}	$V_{VIDEO}=3.0V$	—	1.3	—	lx•sec
Sensitivity	S	$V_{VIDEO}=3.0V$	—	15	—	nA/lx
Horizontal resolution	R_H		—	450	—	TVline
Vertical resolution	R_V		—	350	—	TVline
Power consumption	P	$F_{CLH}=4.625MHz$, $V_{HSH}=V_{VSH}=7V$	—	70	—	mW

●Timing Chart



Vertical drive pulse

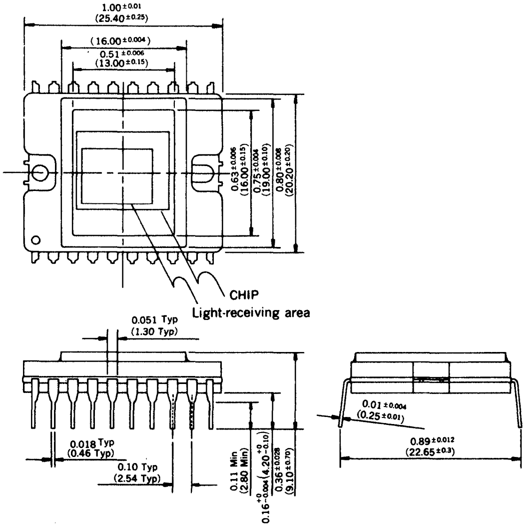


1 H : 63.556μs
1 tfs : 139.68ns

Horizontal drive pulse

■PACKAGE DIMENSIONS

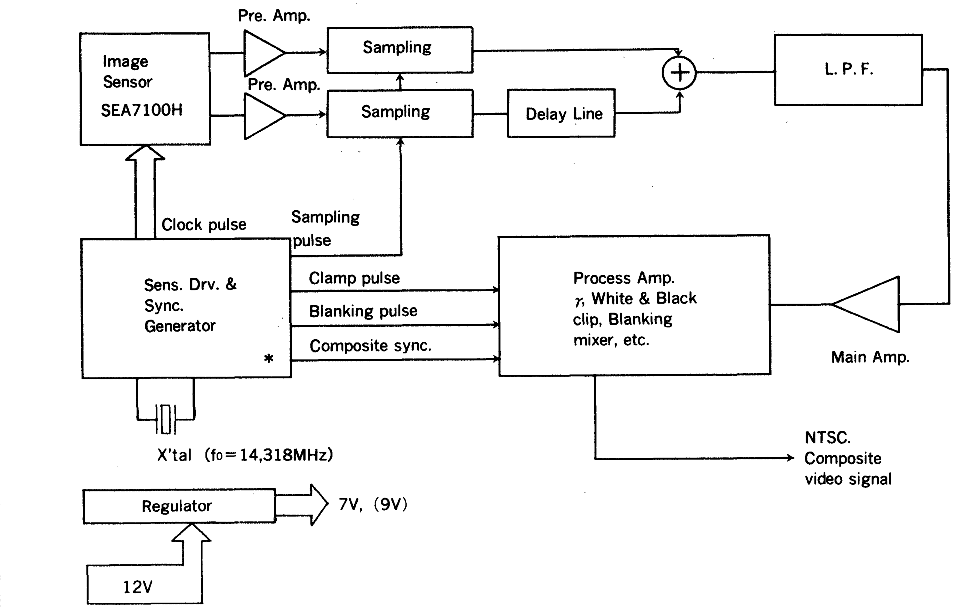
H20



20-pin DIP (ceramic)

unit : inch
(mm)

■EXAMPLE OF APPLICATION (Peripheral Circuit Configuration)



Video Camera Block Diagram

* Sync. control LSI (flat plastic package) is available as a system support IC. (SED3181F3A)

[Precaution to handle]

1. The image sensor SEA7100H is a MOS LSI, so protect it against electrostatic breakdown. Never touch the sensor without grounding your body and the tools. Connect a resistance of about 1MΩ between the body and GND in series to ensure safety.
2. Do not touch the glass surface of the device. Wipe the surface, if soiled, with a clean applicator.
3. Take care not to drop the device, which has a glass cap.

SEA7521H

CCD LINE SENSOR

●2,048 Bits Photo-element

●14μm Pitch

■DESCRIPTION

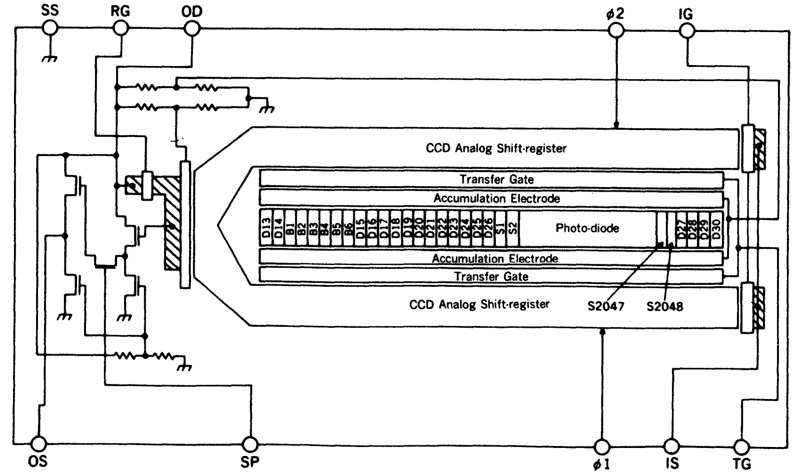
The SEA7521H is a 2,048 bits CCD line sensor which has a CCD analog shift register for reading image signals. It is possible to read a manuscript of B4 size (36.4cm × 25.8cm) by 8 line/mm.

The SEA7521H is appropriate for facsimile, image scanner and industrial measurement/control system applications.

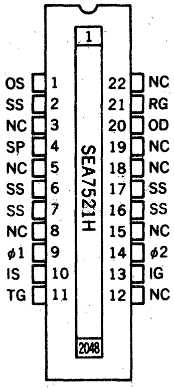
■FEATURES

- ●Photo element ··········· 2,048 bits
- ●Element pitch ··········· 14μm
- ●Data transmit frequency ··········· 1 MHz (Typ)
- ●Saturation voltage ··········· 1.0 V (Typ)
- ●Saturated exposure value ··········· 1.0 lx·sec (Typ)
- ●Photo response ··········· 1.0 V/lx·sec (Typ)
- ●Improvement of blue response by using P/N photo diodes
- ●Elements exclusive to black level are incorporated
- ●Sample-hold circuits are incorporated for output signal
- ●2 phases clock for CCD analog shift register
- ●Single power supply ··········· 12V
- ●Package ··········· 22-pin DIP (CERDIP) with optical glass

■BLOCK DIAGRAM



■PIN CONFIGURATION



■PIN DESCRIPTION

Pin No.	Pin Name	Function
1	OS	Source of output transistor
2	SS	Substrate (GND)
3	NC	non-connection
4	SP	Sample-hold
5	NC	non-connection
6	SS	Substrate (GND)
7	SS	Substrate (GND)
8	NC	non-connection
9	$\phi 1$	Clock (first phase)
10	IS	Input source (for testing)
11	TG	Transfer gate
12	NC	non-connection
13	IG	Input gate (for testing)
14	$\phi 2$	Clock (second phase)
15	NC	non-connection
16	SS	Substrate (GND)
17	SS	Substrate (GND)
18	NC	non-connection
19	NC	non-connection
20	OD	Drain of output transistor
21	RG	Reset gate
22	NC	non-connection

(The NC should be connected to the SS)

■ABSOLUTE MAXIMUM RATINGS

($V_{SS}=0V$)

Parameter		Symbol	Ratings	Unit
Terminal voltage	$\phi 1$, $\phi 2$	V_{ϕ}	−0.3 to 15	V
	TG	V_{TG}		
	RG	V_{RG}		
	SP	V_{SP}		
	OD	V_{OD}		
	IG	V_{IG}		
	IS	V_{IS}		
Operation temperature		T_{opr}	−25 to 60	℃
Storage temperature		T_{stg}	−40 to 100	℃
Soldering temperature/time		T_{sol}	260℃, 10s (at lead)	—

■ELECTRICAL CHARACTERISTICS

●Recommended Operating Conditions

($V_{SS}=0V$, $Ta=25℃$)

Parameter		Symbol	Conditions	Min	Typ	Max	Unit
Transfer clock voltage	High level	$V_{\phi H}$		11	12	13	V
	Low level	$V_{\phi L}$		0	0.5	0.8	V
Transfer gate voltage	High level	V_{TGH}		11	12	13	V
	Low level	V_{TGL}		0	0.5	0.8	V
Reset gate voltage	High level	V_{RGH}		11	12	13	V
	Low level	V_{RGL}		0	0.5	0.8	V
Sample-hold gate voltage	High level	V_{SPH}		11	12	13	V
	Low level	V_{SPL}		0	0.5	0.8	V
Output Tr. drain voltage		V_{OD}		11.5	12	13	V
Input gate voltage		V_{IG}		0	0	1	V
Input source voltage		V_{IS}		11	12	13	V

Note; The SP should be connected to the OD when the sample-hold function is not used.

●Clock Characteristics

(Ta = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Transfer clock frequency	f_ϕ		—	0.5	—	MHz
Reset gate clock frequency	f_{RG}		—	1	—	MHz
Input capacity of $\phi1/\phi2$	C_ϕ		—	950	—	pF
Input capacity of TG	C_{TG}		—	150	—	pF
Input capacity of RG	C_{RG}		—	10	—	pF
Input capacity of SP	C_{SP}		—	10	—	pF

●Opto-electrical Characteristics

($V_\phi = V_{TG} = V_{RG} = V_{SP} = V_{OD} = V_{IS} = 12V$, $V_{IG} = 0V$, $f_\phi = 0.5MHz$, Optical accumulation time = 10ms,
A light source of 2,856K colour temperature, Ta = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Photo response	R	—	0.8	1.0	1.3	V/lx·sec
Unequalness of photo response	PRNU*1	50% of SE	—	—	±10	%
Unequalness of adjacent-photo response	PRNUN*2	—	—	—	±4	%
Saturated output voltage	V_{SAT}	—	0.8	1.0	—	V
Saturated exposure value	SE	—	—	1.0	—	lx·sec
Dark output voltage	V_{DRK}	—	—	1.1	5.0	mV
DC power consumption	PD	$V_{OD} = 13V$	—	20	40	mW
Total transfer efficiency	TTE	—	0.92	0.95	—	—
Output impedance	Z_O	—	—	0.9	1.5	kΩ
Dynamic range	DR	V_{SAT}/V_{DRK}	—	600	—	—

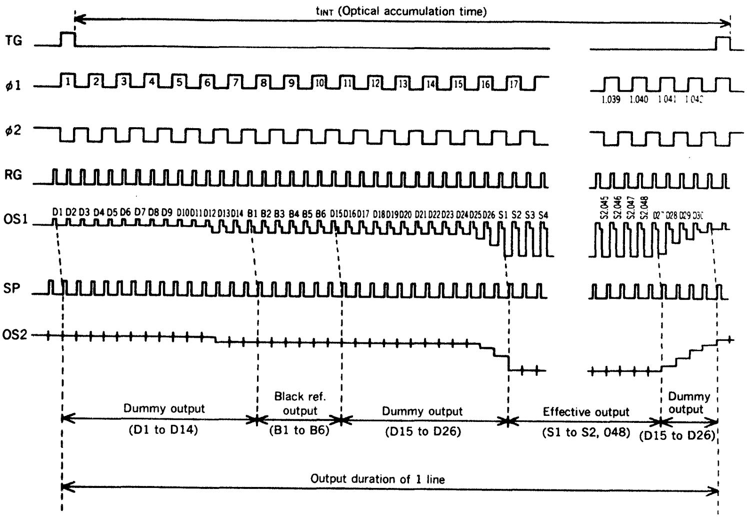
*1 $\mathrm{PRNU} = \frac{V - \bar{V}}{\bar{V}} \times 100$ [%]

$\bar{V}$: Average output voltage of all photo-elements
V: Output voltage of each photo-element

*2 $\mathrm{PRNUN} = \frac{V - \bar{V}}{\bar{V}} \times 100$ [%]

$\bar{V}$: Average output voltage of adjacent 32 photo-elements
V: Output voltage of each adjacent 32 photo elements

■TIMING CHART

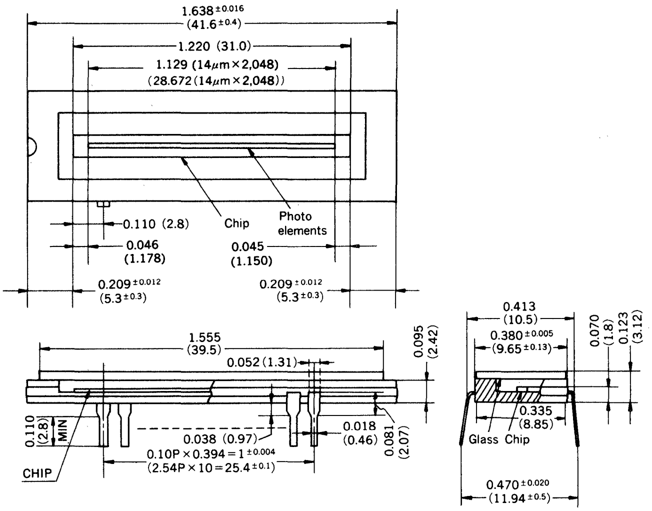


OS1: Output signal if the sample-hold function is not used.
OS2: Output signal if the sample-hold function is used.

The transfer clock ($\phi1/\phi2$) should be given 1,042 times and more.

■PACKAGE DIMENSIONS

22-pin DIP (CERDIP)



unit : inch
(mm)

[Precaution to handle]

1. Handle the CCD line sensor carefully against electro-statics. Though SEA7521H is of such design as to be protected from electro-statics, some careless handling may cause the damage.
2. Wipe off the smear on the front glass with alcohol or the like. Otherwise, it will appear as a dark spot.
3. Use a visible radiation as the light incident to the device. Otherwise, the performance may not sometimes satisfy the specified characteristics.
4. Don't apply strong shocks to the device, which may cause the damage on the glass or other parts.

SEA7551H

CCD LINE SENSOR

- **5,000 Bits Photo-element**
- **7μm Pitch**

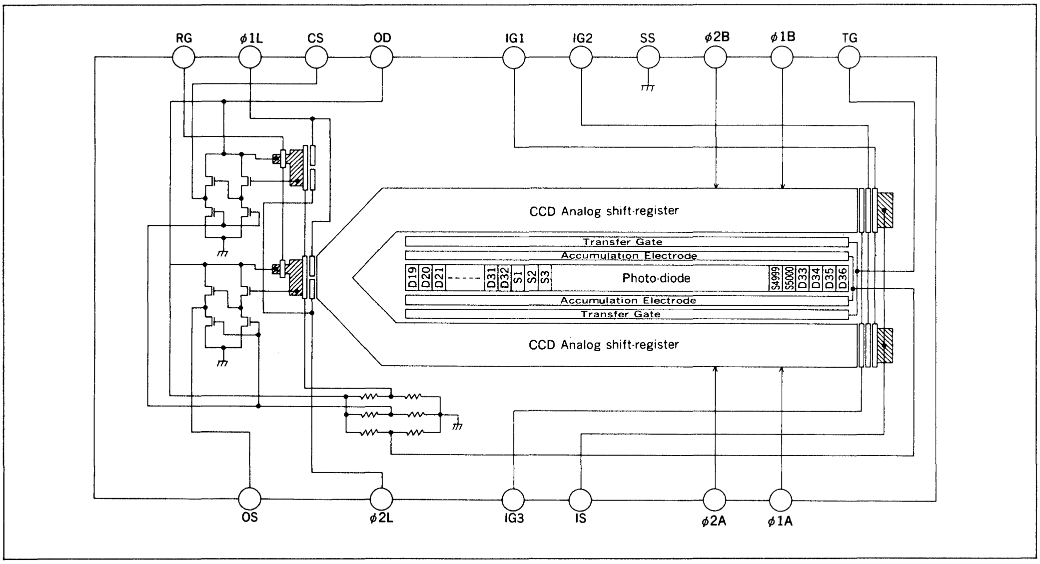
■DESCRIPTION

The SEA7551H is a 5,000 bits CCD line sensor which has a CCD analog shift register for reading image signals. It is possible to read a manuscript of A3 size (29.6cm × 42cm) by 16 line/mm.
The SEA7551H is appropriate for image scanners, degital copy, and industrial measurement/control systems applications.

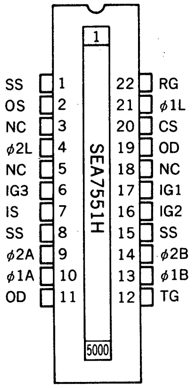
■FEATURES

- Photo element ……………… 5,000 bits
- Element pitch ……………… 7μm
- Data transmit frequency ……………… 0.5MHz (Typ)
- Saturation voltage ……………… 0.6V (Typ)
- Saturated exposure value ……………… 2.0 lx・sec (Typ)
- Photo response ……………… 0.3V/lx・sec (Typ)
- Improvement of blue response by using P/N photo diodes
- The signal output circuit has 2 step amplifiers, and it is enough output drive capability.
- The compensational output circuit is builded in, and it is easy to eliminate reset noise.
- 2 phases clock for CCD analog shift register
- Single power supply ……………… 12V
- Package ……………… 22-pin DIP (Ceramic) with optical glass

■BLOCK DIAGRAM



■PIN CONFIGURATION



■PIN DESCRIPTION

Pin No.	Pin Name	Function
1	SS	Substrate (GND)
2	OS	Source of output transistor
3	NC	No Connection
4	φ2L	Last gate clock (second phase)
5	NC	No Connection
6	IG3	Input gate 3 (for testing)
7	IS	Input source (for testing)
8	SS	Substrate (GND)
9	φ2A	Clock (second phase)
10	φ1A	Clock (first phase)
11	OD	Drain of output transistor
12	TG	Transfer gate
13	φ1B	Clock (first phase)
14	φ2B	Clock (second phase)
15	SS	Substrate (GND)
16	IG2	Input gate 2 (for testing)
17	IG1	Input gate 1 (for testing)
18	NC	No Connection
19	OD	Drain of output transistor
20	CS	Source of compensational output transistor
21	φ1L	Last gate clock (first phase)
22	RG	Reset Gate

(The NC should be connected to the SS)

■ABSOLUTE MAXIMUM RATINGS

($V_{SS}=0V$)

Parameter	Symbol	Ratings	Unit
Transfer clock voltage	$V_{\phi 1A}$, $V_{\phi 1B}$, $V_{\phi 1L}$, $V_{\phi 2A}$, $V_{\phi 2B}$, $V_{\phi 2L}$	−0.3 to 15	V
Transfer gate voltage	V_{TG}		
Reset gate voltage	V_{RG}		
Output tr. drain voltage	V_{OD}		
Input gate voltage	V_{IG1}, V_{IG2}, V_{IG3}		
Input source voltage	V_{IS}		
Operation temperature	T_{opr}	−25 to 60	℃
Storage temperature	T_{stg}	−40 to 100	℃
Soldering temperature/time	T_{sol}	260℃, 10s (at lead)	—

■ELECTRICAL CHARACTERISTICS

●Recommended Operating Conditions

($V_{SS}=0V$, $Ta=25℃$)

Parameter		Symbol	Conditions	Min	Typ	Max	Unit
Transfer clock voltage	High level	$V_{\phi 1A}$, $V_{\phi 1B}$, $V_{\phi 1L}$, $V_{\phi 2A}$, $V_{\phi 2B}$, $V_{\phi 2L}$		11	12	13	V
	Low level	$V_{\phi 1A}$, $V_{\phi 1B}$, $V_{\phi 1L}$, $V_{\phi 2A}$, $V_{\phi 2B}$, $V_{\phi 2L}$		0	0.5	0.8	V
Transfer gate voltage	High level	V_{TGH}		11	12	13	V
	Low level	V_{TGL}		0	0.5	0.8	V
Reset gate voltage	High level	V_{RGH}		11	12	13	V
	Low level	V_{RGL}		0	0.5	0.8	V
Output Tr. drain voltage		V_{OD}		11.5	12	13	V
Input gate voltage		V_{IG1}, V_{IG2}, V_{IG3}		0	0	1	V
Input source voltage		V_{IS}		11	12	13	V

●Clock Characteristics

(Ta = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Transfer clock frequency	f_ϕ		—	0.5	—	MHz
Reset gate clock frequency	f_{RG}		—	1	—	MHz
Input capacity of ϕ_{1A}, ϕ_{2A}, ϕ_{1B}, ϕ_{2B}	$C_{\phi A,B}$		—	600	—	pF
Input capacity of ϕ_{1L}, ϕ_{2L}	$C_{\phi L}$		—	20	—	pF
Input capacity of TG	C_{TG}		—	150	—	pF
Input capacity of RG	C_{RG}		—	20	—	pF

●Opto-electrical Characteristics

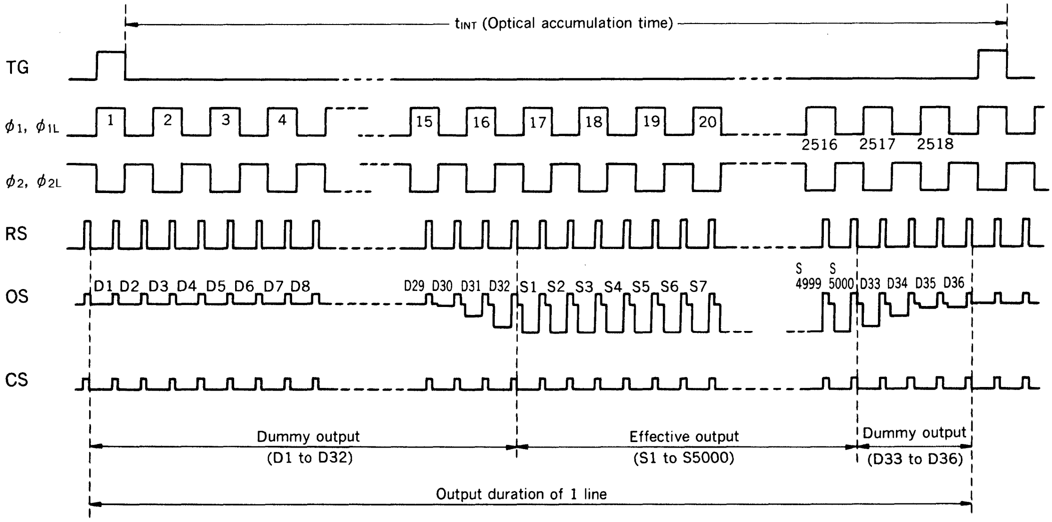
($V_\phi = V_{TG} = V_{RG} = 12V$ pulse drive, $V_{OD} = V_{IS} = 12V$, $V_{IG} = 0V$, $f_\phi = 0.5MHz$, Optical accumulation time = 10ms, A light source of 2,856K colour temperature, Ta = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Photo response	R	—	0.27	0.3	—	V/lx·sec
Unequalness of photo response	PRNU*1	50% of SE	—	—	±10	%
Saturated output voltage	V_{SAT}	—	0.55	0.6	—	V
Saturated exposure value	SE	—	1.5	2.0	—	lx·sec
Dark output voltage	V_{DRK}	—	—	1.2	8	mV
DC power consumption	PD	$V_{OD} = 13V$	—	30	40	mW
Total transfer efficiency	TTE	—	0.90	0.95	—	—
Output impedance	Z_O	—	—	1	2	kΩ
Dynamic range	DR	V_{SAT}/V_{DRK}	—	500	—	—
Output voltage-Compensational output voltage	$\lvert V_{OS} - V_{CS} \rvert$	—	—	—	300	mV

*1 $\mathrm{PRNU} = \frac{V - \bar{V}}{\bar{V}} \times 100$ [%]

$\bar{V}$: Average output voltage of all photo-elements
V: Output voltage of each photo-element

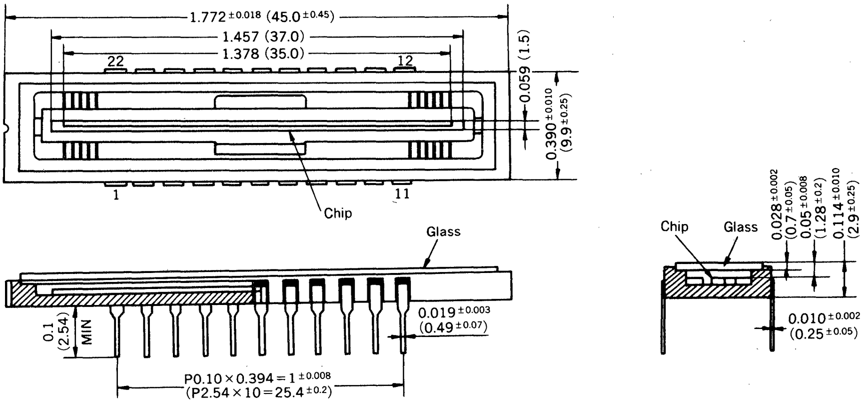
■TIMING CHART



The transfer clock (ϕ_1, ϕ_2) should be given 2,518 times and more.

■PACKAGE DIMENSIONS

22-pin DIP (Ceramic)



unit : inch
(mm)

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3. Use a visible radiation as the light incident to the device. Otherwise, the performance may not sometimes satisfy the specified characteristics.
4. Don't apply strong shocks to the device, which may cause the damage on the glass or other parts.

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