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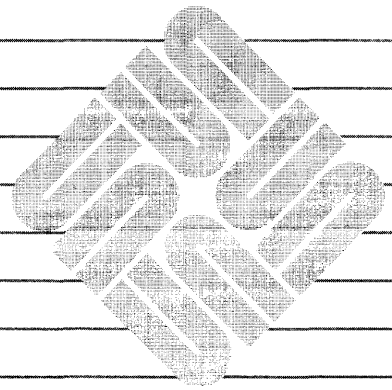
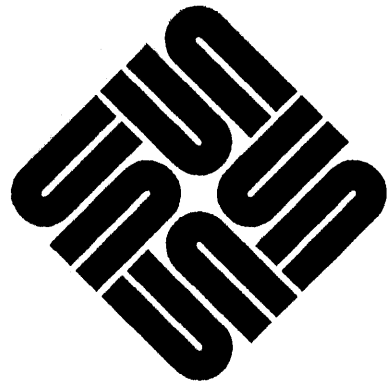
Sun™ VME-Multibus Adapter Board User's Manual



Part Number 800-1193-05
Revision: A of 25 September 1986

Introduction



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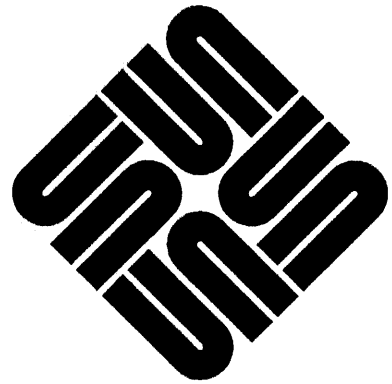

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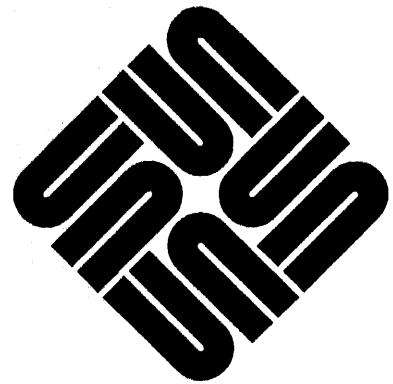

Part Number 800-1193-05
Revision: A of 25 September 1985
Class:3

Users' Manual

for the

Sun VME-Multibus Adapter Board

Sun Microsystems, Inc.,
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This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

Contents

Contents

Tables

Figures

Preface

Welcome to the Sun VME-to-Multibus Adapter board. This manual presents a functional and engineering description of the VME-Multibus board, tells you how to set the switches and jumpers, and also contains tutorials to assist you in setting the configuration of the board for your particular application.

Summary of Contents

This manual contains three chapters and two appendices:

Chapter 1

Functional Description — presents a basic functional description (tells you what the board does), including a description of the interrupt, DMA, and clock circuits.

Chapter 2

Switches on the VME-to-Multibus Adapter Board — describes the purpose and function of the DIP switches on the VME-to-Multibus board.

Chapter 3

Theory of Operations — explains in some detail the electrical operation (how the board works) of the VME-to-Multibus board.

Appendix A

Switch Settings Worksheet — this appendix gives you space to work out the switch settings for your own Multibus board. Includes examples.

Appendix B

Example Configurations — gives the switch settings for Sun-provided boards.

Glossary

A few terms are used throughout this document which, without explanation, may seem confusing.

- Positive Logic — positive logic means that the asserted level (see below) of a signal is the *higher* of the two voltage levels.
- Negative Logic — negative logic means that the asserted level (see below) of a signal is the *lower* of the two voltage levels.
- Asserted — when we say that a signal is "asserted," we mean that it is in its active, or true, state. In positive logic this means that a signal like READ, when asserted, is equal to its most positive state. When a signal like WRITE*, WRITE-, or WRITE\ (the three are synonymous) is asserted it is equal to its most negative state.

- Logic 1 — in positive logic, a logic 1 stands for the more positive of the two voltage levels. In negative logic, a logic 1 stands for the more negative of the two voltage levels.
- Logic 0 — in positive logic, a logic 0 stands for the more negative of the two voltage levels. A logic 0 in negative logic stands for the more positive of the two voltage levels.
- Set — means the same as logical 1.
- Clear — means the same as a logical 0.
- ON — when it refers to a switch (or switch section) setting, is synonymous with CLOSED. This means that the signal at the input of the switch (or switch section) is shorted to its output.
- OFF — when it refers to a switch (or switch section) setting, is synonymous with OPEN. This means that the signal at the input of the switch (switch section) is NOT SHORTED (signal is not passed) to its output.
- CLOSED — when it refers to a switch (or switch section) setting, is synonymous with ON. This means that the signal at the input of the switch (switch section) is shorted to its output.
- OPEN — when it refers to a switch (or switch section) setting, is synonymous with OFF. This means that the signal at the input of the switch (switch section) is NOT SHORTED (signal is not passed) to its output.
- DIP — stands for Dual In-line Package, and refers to the physical geometry of the chip (rectangular, with pins on the two longer sides).
- DIP Switch — a multi-sectioned switch which has DIP geometry.
- Switch — a device for making or breaking an electrical circuit. A switch may have one or more sections, each of which may control a circuit.
- 0x — hexadecimal prefix; the number following this prefix is in hexadecimal.

Finally, thanks to Doug Ward for all his help.

Revision History

Revision	Date	Comments
A-01	1 June 1985	First release of this Users' Manual.
A-05	25 September 1986	Corrected textual inaccuracies dealing with DIP switch 11 and described board modifications.

1

Functional Description

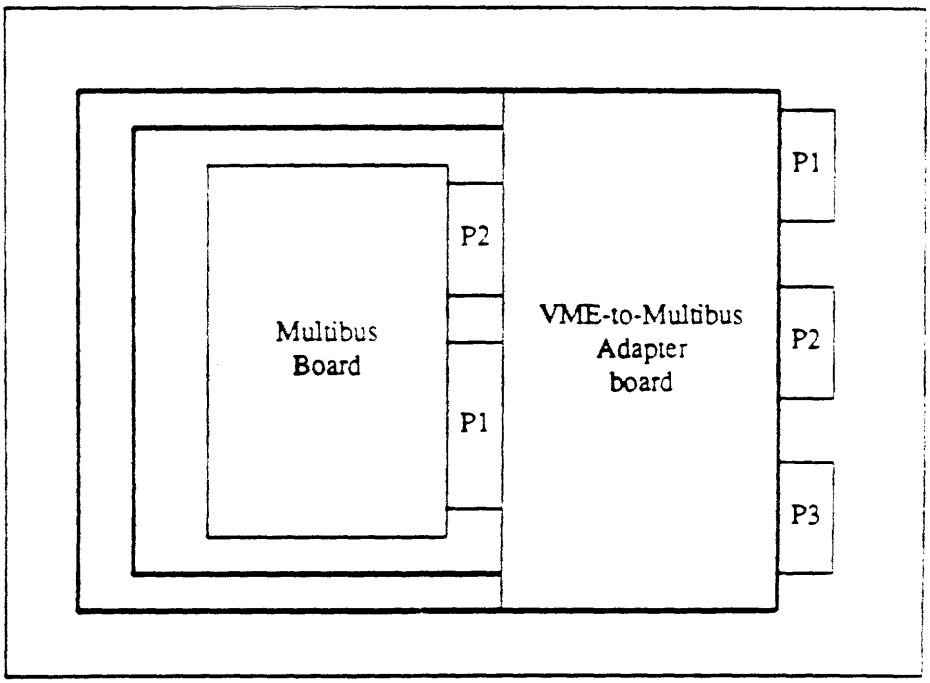
1

Functional Description

1.1. Overview

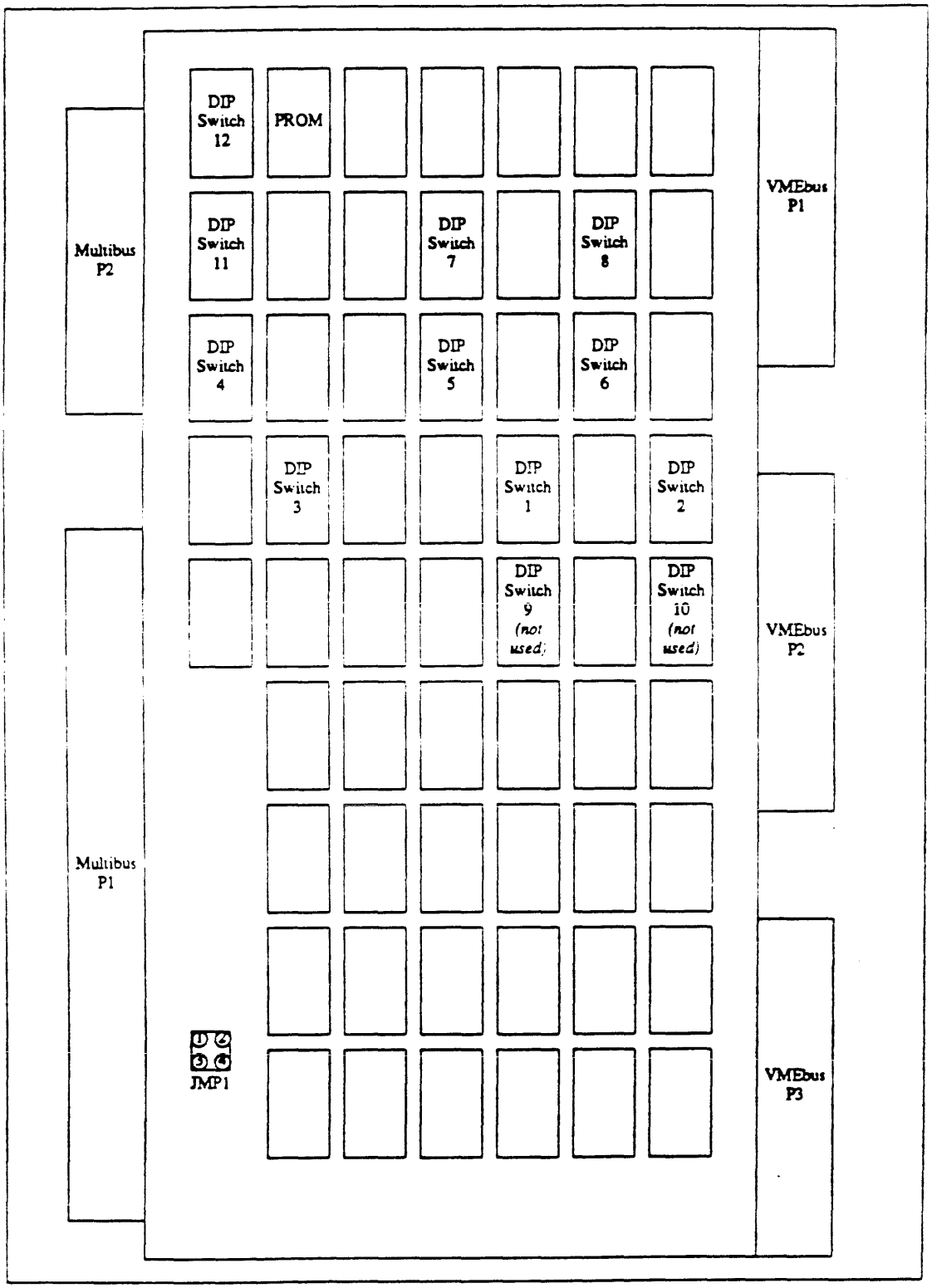
This manual describes the VME-to-Multibus™ adapter board for use in the Sun VME products. This adapter board allows you to plug your own Multibus boards into Sun's VME backplane, and this manual tells you how to set the switches appropriately.†

Figure 1-1 *VME-to-Multibus Adapter Board*



†If you already know how the switches work and just want to set the switches for your own Multibus board, please see the switch settings worksheet in the appropriate appendix.

Figure 1-2 *Adapter Board Layout*



For location of the VME-to-Multibus adapter board in a Sun backplane, please see the *Cardcage Slot Assignment and Backplane Configuration Guide*, part number 813-2004, available through Sun Sales or Service.

1.2. What the Switches Do

Switches on the adapter board allow you to

- generate a Multibus memory read or write command from the VMEbus using the Multibus board as either a 20-bit or 24-bit slave device;
- generate a Multibus I/O read or write command from the VMEbus;
- generate a DMA cycle from the Multibus board using the Multibus board as either a 20-bit or 24-bit bus master;
- generate single-level or multi-level vectored interrupts.

Switches are set to define

- the base address of the Multibus memory and I/O spaces, and
- the block size of the Multibus memory and I/O spaces.

2

Switches on the VME-to-Multibus Adapter Board

2

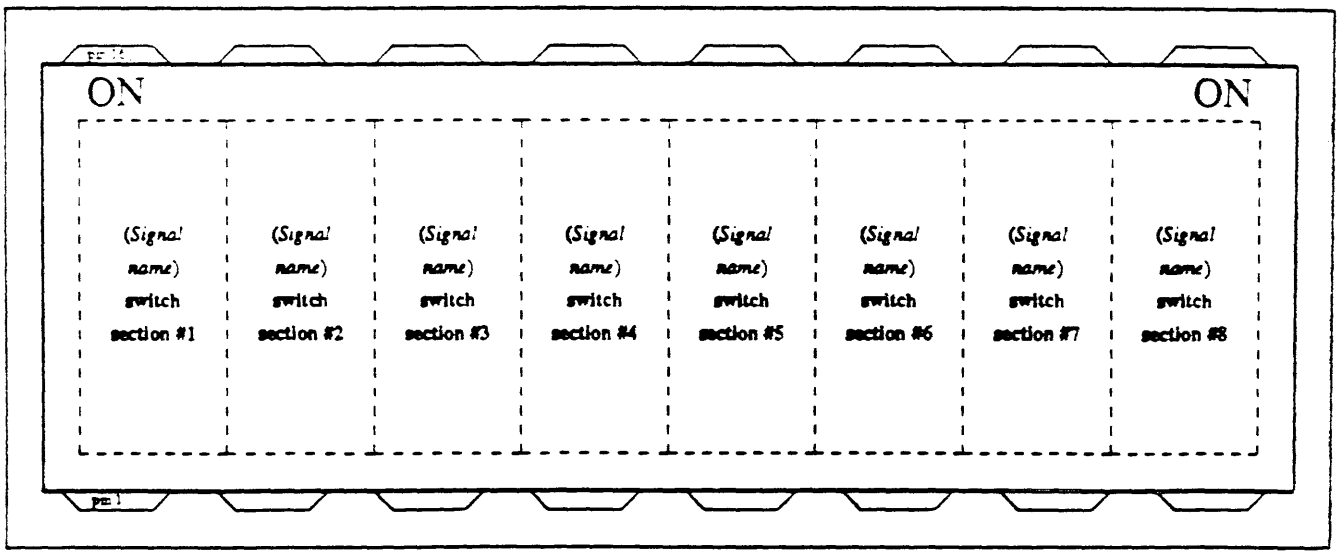
Switches on the VME-to-Multibus Adapter Board

This section describes the DIP switches on the VME-to-Multibus Adapter boards. Appendix A contains a worksheet for use by those who already understand the function of the switches; Appendix B contains this same information along with a step-by-step explanation as help should you need to set the DIP switches yourself.

2.1. Multibus Memory Addressing—DIP Switches 5, 6, 7, and 8

NOTE *For an explanation of some of the terms used in this (and other) sections, please see the glossary included in the Preface of this manual. Briefly, a DIP switch is composed of switch sections, each section of which will short (when the switch section is set to ON) or open (when the switch section is set to OFF) its circuit.*

Figure 2-1 *Example of a Typical 8-Section DIP Switch*



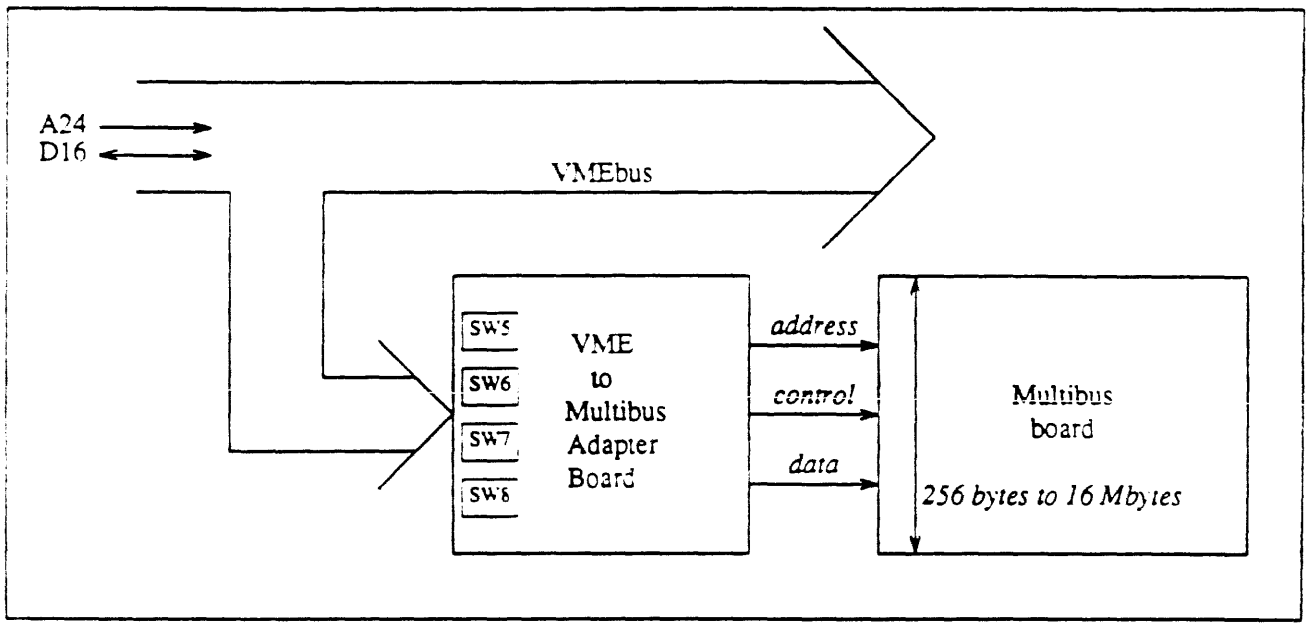
The adapter board can respond to a block of addresses in the 24-bit VME address space. When the adapter board sees an address within the selected block, it

passes all the address bits through to the Multibus board and generates a Multibus Memory read or write command.

The size of the block of addresses can be any power of 2 between 2 to the 8th power and 2 to the 24th power (256 bytes to 16 Mbytes). The starting address of the block can be any address which is a multiple of the size of the block.

Another way of saying this is that any VME address bit between A8 and A23 can either be ignored or compared against a switch section. The switches which control Multibus memory addressing are SW5, SW6, SW7, and SW8.

Figure 2-2 *Multibus Memory Address Decoding*



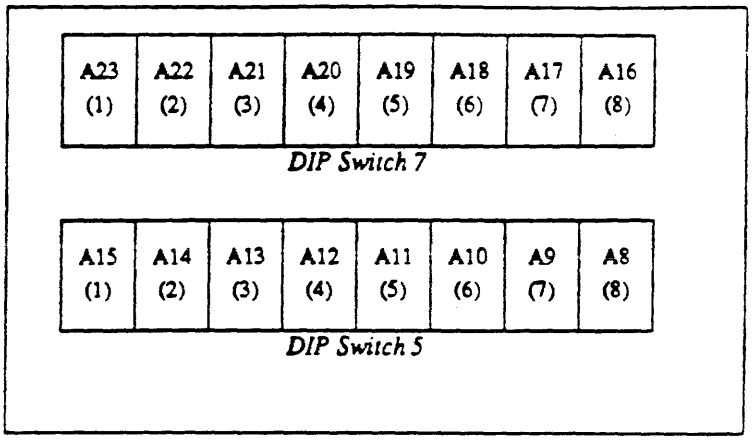
Multibus Memory Space Switch Settings

- **DIP 7, DIP 5**—Select the 24-bit VME space base address for accesses to the Multibus Memory space.

```
DIP 7 sections 1-8  =>   A23-A16  respectively.

DIP 5 sections 1-8  =>   A15-A08  respectively.
```

Figure 2-3 *Address Switches for the 24-Bit Multibus Memory Space*



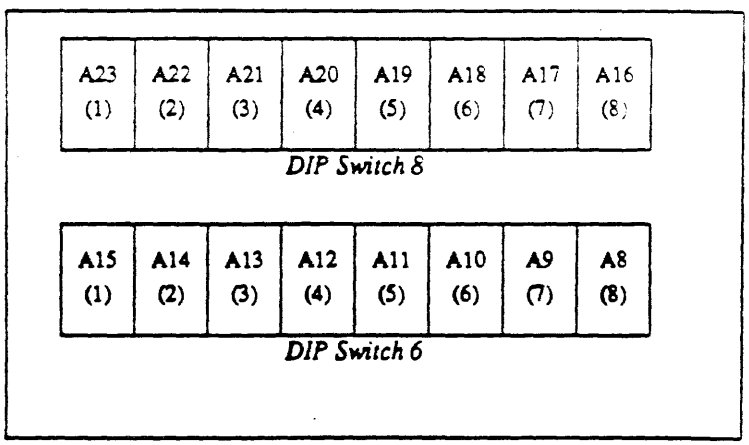
A switch section ON causes a match when the corresponding VME address bit is 0.

- **DIP 8, DIP 6**—Sets the size of the block in 24-bit VME address space that the board responds to.

```
DIP 8  sections 1-8  =>  A23-A16  respectively.

DIP 6  sections 1-8  =>  A15-A08  respectively.
```

Figure 2-4 *Block-Size Switches for 24-Bit Multibus Memory Space*



There is a separate switch section for each address bit from A8 to A23.

- If the switch section is ON, that address bit is compared against the corresponding base address switch section. If the address bit matches the

switch section setting, the adapter board responds.

- If the switch section is OFF, that bit is ignored by the adapter board, and is simply passed through to the Multibus board.

To set the size of the block, all address bits whose binary weighting is *larger* than the size of the block should have their switch sections ON, because these bits will be decoded by the adapter board. Address bits with binary weighting *smaller* than the size of the block should have both their "size" switch section and their "base address" switch section OFF, because the address bits within the block size are of interest only to the Multibus board.

Thus, if you have a block size of 1024 bytes, you would set the switch sections for address bits A8 and A9 to OFF, because the adapter board DOESN'T CARE about (won't compare) these address bits. The rest of the address bits, A10-A23, would set ON, because the adapter board DOES CARE about these bits, and will use them for comparison.

The following example explains this further.

Let's say you want to configure your adapter board for an imaginary Multibus board which has a block size of 16 Kbytes starting at address 0x280000.

First, you want to set a block size of 16 Kbytes into the block size switches, DIPs 8 and 6. Remember that when you define block size you are telling the adapter board which address lines *are to be ignored*; in other words, don't compare them. Since a block size of 16 Kbytes is decoded by address lines A13-A0, address bits A13-A8 (A7-A0 are *always* passed through) will be passed *to the Multibus board only*; the adapter board doesn't care what value is on them.

Thus the switch sections for address lines A13-A8 will be set OFF.

However, the adapter board *does care* what is on address lines A23-A14, because it will be decoding them; therefore these switch sections will be set to ON.

Here's how to set the switch sections on the block size switches: first convert the hex value to binary:

```
                                          |
16K =  0x004000 = 0000  0000  0100  0000  | 0000  0000
                     <- A23-A08 ->        |<- always passed ->
                                          |     (A7-A0)
           (single one-bit ON is address bit A14)
```

Next, set the switch sections for address lines A13-A8 to OFF; all the others ON. Then make this binary address correspond to the memory space block size switches, DIP 8 (upper byte) and DIP 6 (lower byte). Remember, a 0 means the switch section is ON; a 1 means the switch section is OFF.

Switch section	1	2	3	4	5	6	7	8
(upper byte binary value) =	0	0	0	0	0	0	0	0
DIP 8 Address =	A23	A22	A21	A20	A19	A18	A17	A16
(lower byte binary value) =	0	0	1	1	1	1	1	1
DIP 6 Address =	A15	A14	A13	A12	A11	A10	A09	A08

Here's what the block size switches look like when correctly set:

Figure 2-5 *Memory Space Block Size Switches for a 16 Kbyte Block*

A23 (SW1)	A22 (SW2)	A21 (SW3)	A20 (SW4)	A19 (SW5)	A18 (SW6)	A17 (SW7)	A16 (SW8)
ON	ON	ON	ON	ON	ON	ON	ON

DIP Switch 8

A15 (SW1)	A14 (SW2)	A13 (SW3)	A12 (SW4)	A11 (SW5)	A10 (SW6)	A9 (SW7)	A8 (SW8)
ON	ON	OFF	OFF	OFF	OFF	OFF	OFF

DIP Switch 6

Here's the switch section settings for the various block sizes available in the Multibus memory space.

Table 2-1 *Setting 256 to 64K Block Sizes In Multibus Memory*

Switch	*DIP 8*	*DIP 6*							
Section	*All*	*1*	*2*	*3*	*4*	*5*	*6*	*7*	*8*
Address	*A23-A16*	*A15*	*A14*	*A13*	*A12*	*A11*	*A10*	*A9*	*A8*
Size									
256	ON	ON	ON	ON	ON	ON	ON	ON	ON
512	ON	ON	ON	ON	ON	ON	ON	ON	OFF
1024	ON	ON	ON	ON	ON	ON	ON	OFF	OFF
2048	ON	ON	ON	ON	ON	ON	OFF	OFF	OFF
4096	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF
8192	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF
16K	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF
32K	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
64K	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

Table 2-2 *Setting 128K to 16M Block Sizes In Multibus Memory*

Switch	*DIP 8*								*DIP 6*
Section	*1*	*2*	*3*	*4*	*5*	*6*	*7*	*8*	*All*
Address	*A23*	*A22*	*A21*	*A20*	*A19*	*A18*	*A17*	*A16*	*A15-A8*
Size									
128K	ON	ON	ON	ON	ON	ON	ON	OFF	OFF
256K	ON	ON	ON	ON	ON	ON	OFF	OFF	OFF
512K	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF
1M	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF
2M	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF
4M	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
8M	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
16M	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

To set the base address of 0x280000, first convert the hex address to binary:

```
                                          |
0x280000 = 0010  1000  0000  0000 |  0000  0000
                                          |<- not connected ->
                    <- A23-A08 ->         |  (A7-A0)
```

Since the block size is 16 Kbytes and the adapter board doesn't compare address bits from within this 16 Kbyte block size, you must set address bits A13-A8 to OFF.

```
A13-A8 OFF = 0010  1000  0011  1111 | 0000  0000
                                    |<- not connected ->
                  <- A23-A08 ->     | (A7-A0)
```

Make this hexadecimal address correspond to the memory space base address switches, DIP 7 (upper byte) and DIP 5 (lower byte).

Switch section	1	2	3	4	5	6	7	8
(upper byte binary value) =	0	0	1	0	1	0	0	0
DIP 7 Address =	A23	A22	A21	A20	A19	A18	A17	A16
(lower byte binary value) =	0	0	1	1	1	1	1	1
DIP 5 Address =	A15	A14	A13	A12	A11	A10	A09	A08

Here's what the base address switches look like when correctly set:

Figure 2-6 *Memory Space Base Address Switches*

A23 (SW1)	A22 (SW2)	A21 (SW3)	A20 (SW4)	A19 (SW5)	A18 (SW6)	A17 (SW7)	A16 (SW8)
ON	ON	OFF	ON	OFF	ON	ON	ON

DIP Switch 7

A15 (SW1)	A14 (SW2)	A13 (SW3)	A12 (SW4)	A11 (SW5)	A10 (SW6)	A9 (SW7)	A8 (SW8)
ON	ON	OFF	OFF	OFF	OFF	OFF	OFF

DIP Switch 5

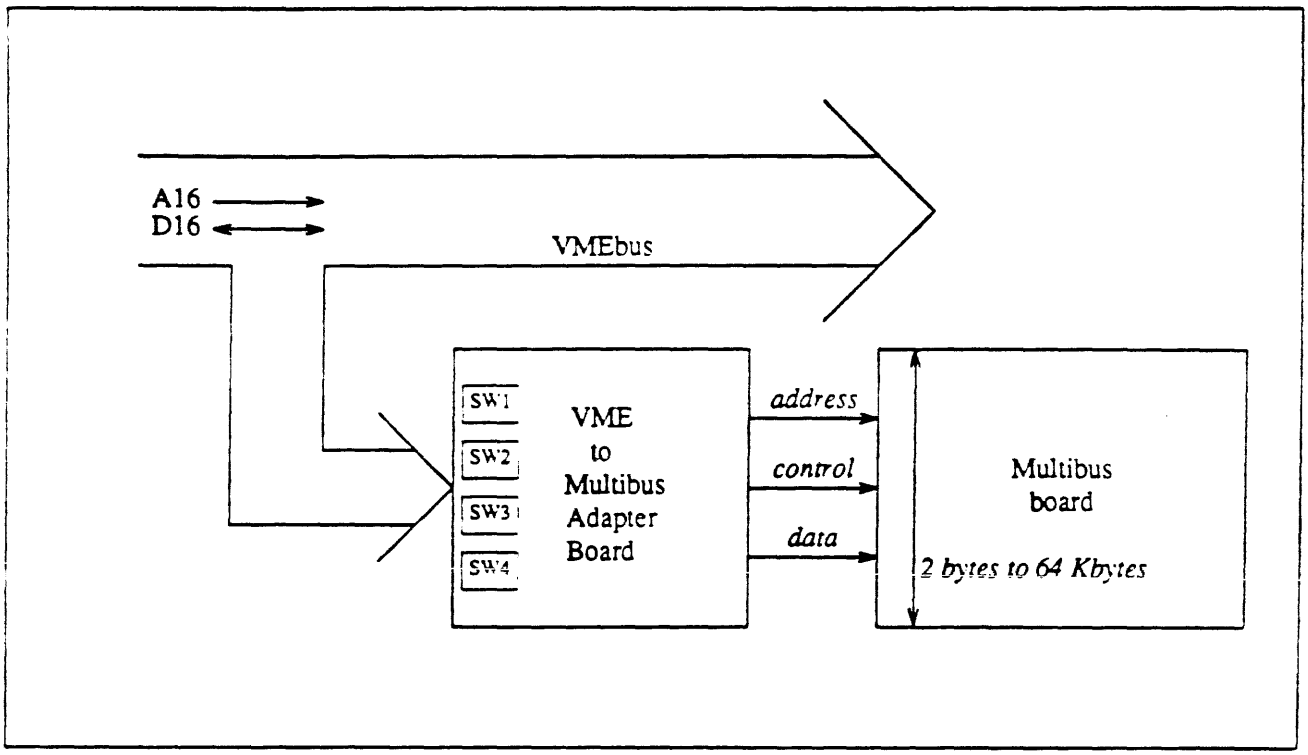
If you don't want the Multibus board to respond to the Multibus memory space at all, disable the VME 24-bit space decoding by setting

- all sections of DIP 8 and DIP 6 to OFF, and
- all sections of DIP 7 and DIP 5 to ON.

2.2. Multibus I/O Addressing—DIP Switches 1, 2, 3, and 4

The adapter board can respond to a block of addresses in the 16-bit VME address space. When the adapter board sees an address within the selected block, it passes all the address bits through to the Multibus board and generates a Multibus I/O read or write command.

Figure 2-7 *Multibus I/O Address Decoding*



The size of the block of addresses can be any power of 2 between 2 to the 1st power and 2 to the 16th power (2 bytes to 64 Kbytes). The starting address of the block can be any address which is a multiple of the size of the block. Another way of saying this is that any VME address bit between A1 and A15 can either be ignored or compared against a switch section.

This function is controlled by DIP switches 1, 2, 3, and 4.

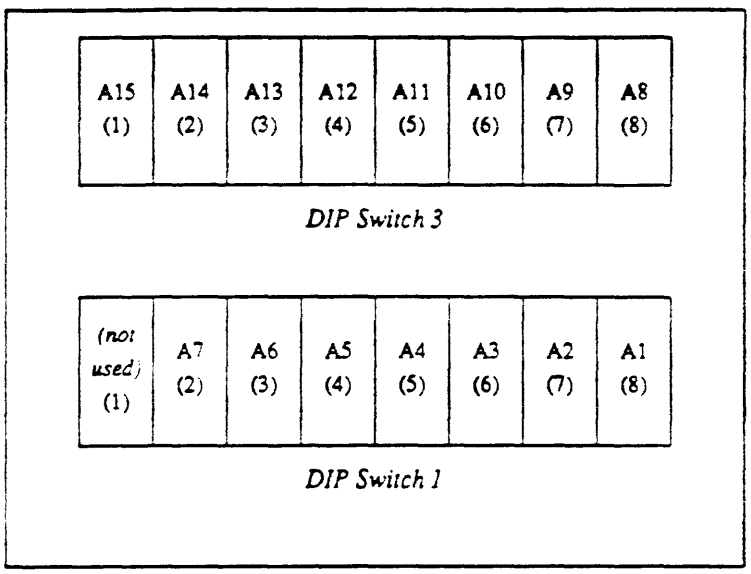
Multibus I/O Space

- **DIP 1, DIP 3**—Select the 16-bit VME space base address for accesses to the Multibus I/O space.

```
DIP 3 sections 1-8  =>   A15-A08  respectively.

DIP 1 sections 2-8  =>   A07-A01  respectively.
```
(DIP 1 section 1 unused.)

Figure 2-8 *Address Switches for the Multibus I/O Space*



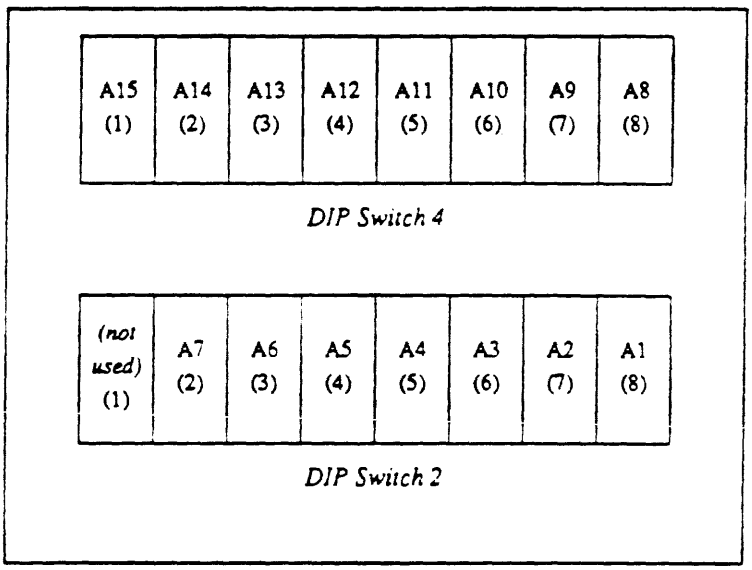
A switch section ON causes a match when the corresponding VME address bit is 0.

- **DIP 4, DIP 2**—Sets the size of the block in 16-bit VME address space that the board responds to.

```
DIP 4 sections 1-8  =>   A15-A08  respectively.

DIP 2 sections 2-8  =>   A07-A01  respectively.
     (DIP 2 section 1 is unused.)
```

Figure 2-9 *Block-Size Switches for the Multibus I/O Space*



There is a separate switch section for each address bit from A1 to A15. If the switch section is ON, that address bit is compared against the corresponding base address switch section. If the address bit matches the switch section setting, the adapter board responds. If the switch section is OFF, that bit is ignored by the adapter board, and is simply passed through to the Multibus board.

To set the size of the block, all address bits whose binary weighting is larger than the size of the block should have their switch sections ON, because these bits will be decoded by the adapter board. Address bits with binary weighting smaller than the size of the block should have both their "size" switch section and their "base address" switch section OFF, because the address bits within the block size are of interest only to the Multibus board. Thus, if you have a block size of 8 bytes, you would set the switch sections for address bits A1 and A2 to OFF, because the adapter board DOESN'T CARE what these bits are. A0 is always passed through.

The tables below give the switch setings for various block sizes in I/O space.

Table 2-3 *Setting 2 to 256 Byte Block Sizes In Multibus I/O Space*

Switch	*DIP 4*	*DIP 2*						
Section	*All*	*2*	*3*	*4*	*5*	*6*	*7*	*8*
Address	*A15-A8*	*A7*	*A6*	*A5*	*A4*	*A3*	*A2*	*A1*
Size								
2	ON	ON	ON	ON	ON	ON	ON	ON
4	ON	ON	ON	ON	ON	ON	ON	OFF
8	ON	ON	ON	ON	ON	ON	OFF	OFF
16	ON	ON	ON	ON	ON	OFF	OFF	OFF
32	ON	ON	ON	ON	OFF	OFF	OFF	OFF
64	ON	ON	ON	OFF	OFF	OFF	OFF	OFF
128	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF
256	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF

Table 2-4 *Setting 512 Byte to 64 Kbyte Block Sizes In Multibus I/O Space*

Switch	*DIP 4*								*DIP 2*
Section	*1*	*2*	*3*	*4*	*5*	*6*	*7*	*8*	*All*
Address	*A15*	*A14*	*A13*	*A12*	*A11*	*A10*	*A9*	*A8*	*A7-A1*
Size									
512	ON	ON	ON	ON	ON	ON	ON	OFF	OFF
1024	ON	ON	ON	ON	ON	ON	OFF	OFF	OFF
2048	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF
4096	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF
8192	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF
16K	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
32K	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
64K	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

If you don't want the Multibus board to respond to the Multibus I/O space at all, disable the VME 16-bit space decoding by setting

- all sections of DIP 4 and DIP 2 to OFF, and
- all sections of DIP 3 and DIP 1 to ON.

2.3. Multibus Memory Address Space Size and DMA Transfer Address—DIP Switch 11

DIP switch 11 handles two related functions:

1. it chooses between 20-bit and 24-bit addressing for the Multibus board (using switch sections 5-8);
2. if the board does 20-bit addressing and is a DMA controller, DIP switch 11 will provide a set of default high order address bits to fill the DMA address out to 24 bits (using switch sections 1-4).

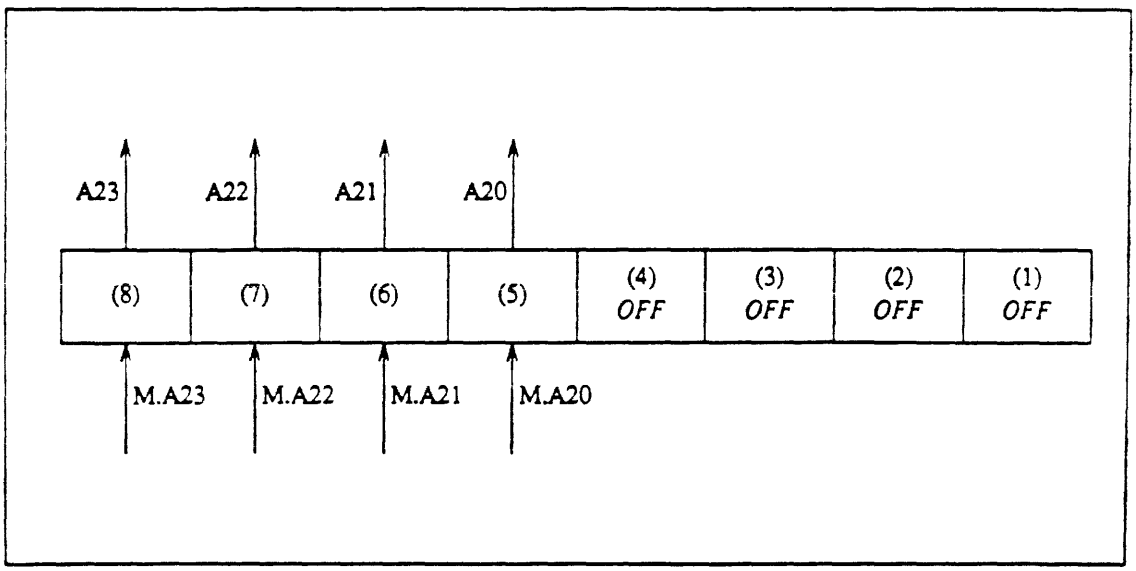
Multibus Memory Address Space Size—DIP Switch 11, Sections 5-8

The Multibus specification has several different variations for addressing. The address space sizes supported by the adapter board are 20- and 24-bit addressing for memory space boards, and 16-bit addressing for I/O space boards. The address lines for the first 20 bits are located on the Multibus P1 connector, while the remaining four high-order bits, A23-A20, reside on the Multibus P2 connector. However, Multibus boards which do 20-bit addressing often use the lines on the Multibus P2 connector *for some other purpose*; to avoid contention the adapter board provides a DIP switch to connect or disconnect lines on the P2 connector to or from the translation circuitry on the adapter board.

Sections 5-8 of DIP switch 11 connect Multibus address lines A20-A23 (respectively) from the Multibus P2 connector on the board's edge, through the adapter board's translation circuitry, to the adapter board's internal Multibus address bus. If sections 5-8 of DIP switch 11 are closed (ON)†, address bits A20-A23 will be passed to and from the Multibus board.

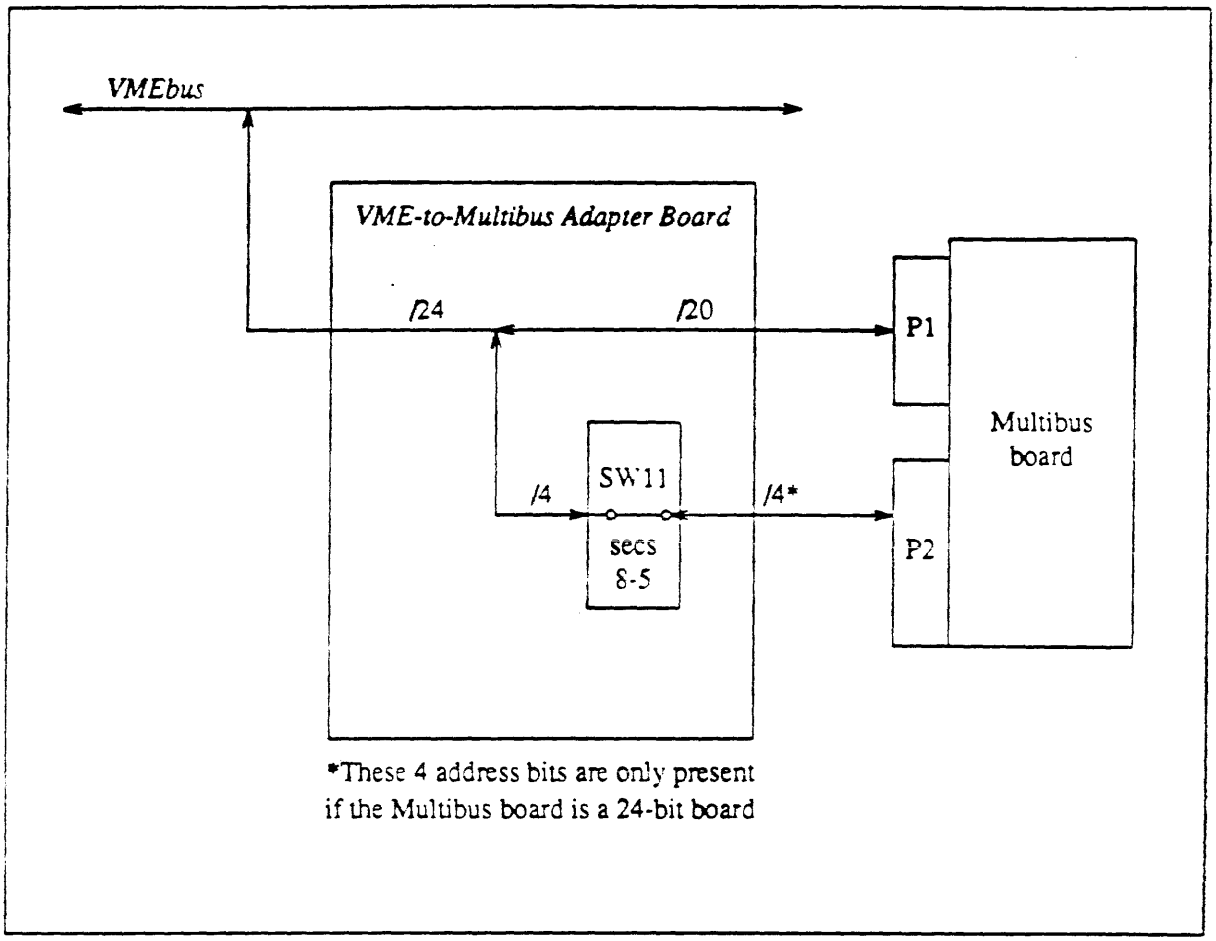
- For those boards which expect 24-bit addresses, or which generate 24-bit DMA addresses, sections 5-8 of DIP switch 11 should be ON†.
- For those boards which expect 20-bit addresses or which generate 20-bit DMA addresses, sections 5-8 should be OFF†.

Figure 2-10 *DIP Switch 11, Sections 5-8*



†Since the Multibus address lines use negative logic, a switch section must be set ON to provide a logic 1 to the VMEbus and OFF to provide a logic 0.

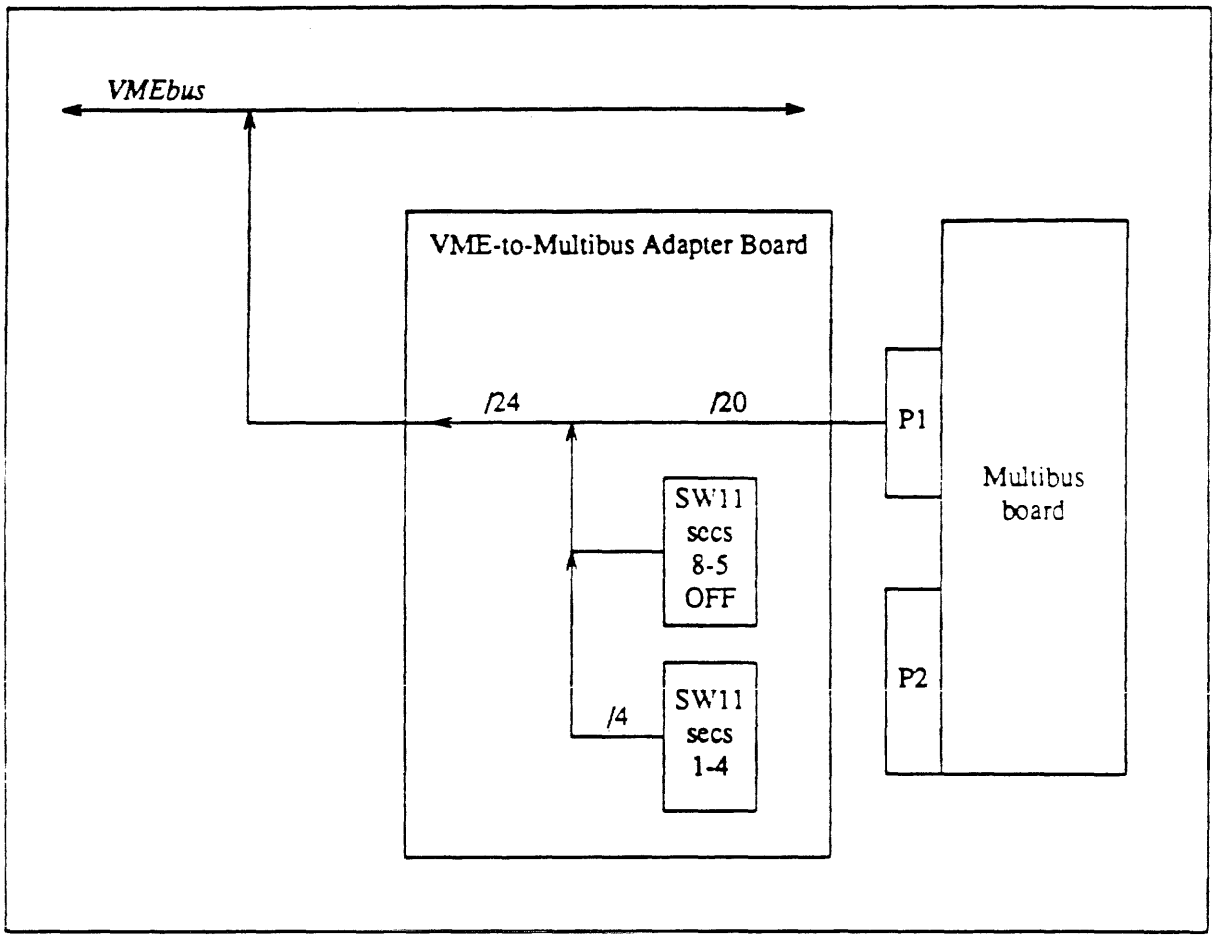
Figure 2-11 *20-Bit versus 24-Bit Addressing*



DMA Transfer Address—DIP Switch 11, Sections 1-4

A Multibus board which only supplies 20 bits of address may be a DMA controller. However the VMEbus requires a 24-bit address, so the adapter board is designed to supply the remaining four high-order address bits, A23-A20, by setting DIP switch sections 1-4 (respectively).

Figure 2-12 *20-bit Multibus DMA Cycle*



In this case, sections 5-8 of DIP switch 11 must be set OFF, to isolate the Multibus P2 connector, and the necessary four high-order address bits must be set into sections 1-4 of DIP switch 11.

Normally devices will be doing DMA into Sun main memory. Since the DVMA port on the Sun CPU board answers to addresses between 0x000000 and 0x100000, this means that the high-order address bits supplied by sections 1-4 of DIP switch 11 should all be zero (set to OFF).

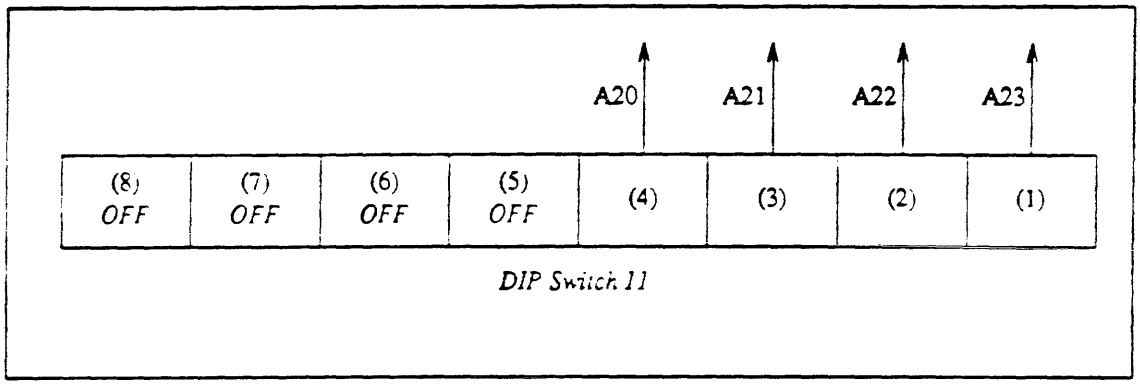
Since a 20-bit master can only generate 1 Mbyte of addresses, the only time that these switches (sections 1-4) should be set to provide a different address is in the case where the board is doing DMA to some other device and NEVER to the Sun. These situations are VERY RARE!

For example, in order to direct all DMA references by a 20-bit Multibus board to an area between 3 Mbytes (0x300000) and 4 Mbytes (0x400000), sections 1-4 of DIP switch 11 must be set to 0x3:

Switch Section:	1	2	3	4
(setting)	OFF	OFF	ON	ON
(address bit)	A23	A22	A21	A20

Remember, when using switch sections 1-4, switch sections 5-8 must all be set OFF, to prevent contention.

Figure 2-13 *DIP Switch 11, Sections 1-4*



2.4. Interrupt Vector—DIP Switch 12

The adapter board will respond to non-bus-vectored Multibus interrupts and translate them to vectored VME interrupts.

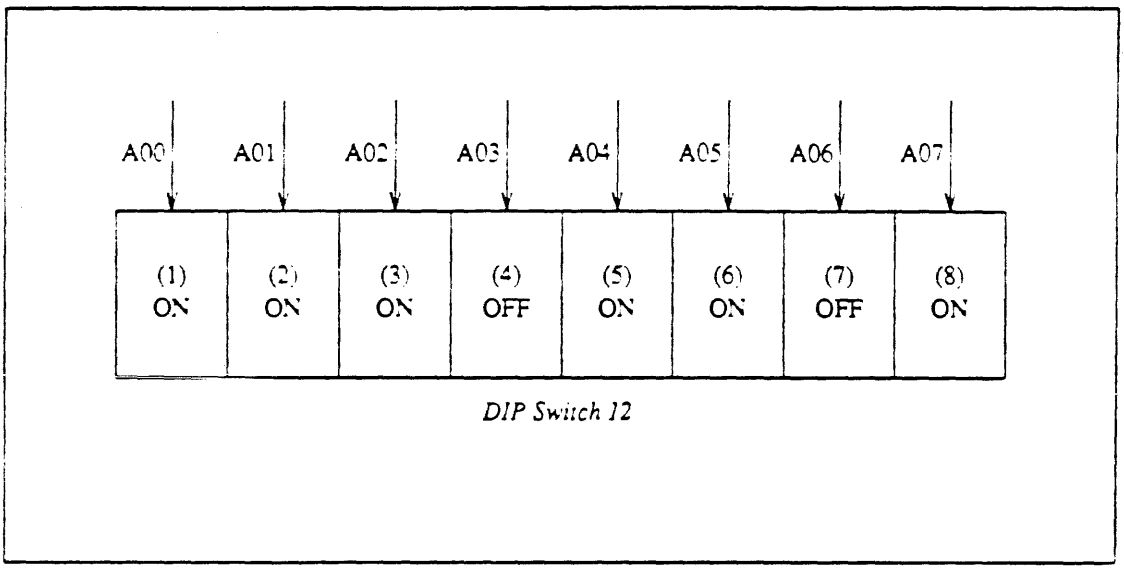
The VME interrupt vector number is provided on the adapter board by either switch sections or a PROM. The switch sections may be used if the Multibus board interrupts on only one level, or if multiple levels vector to the same location. The PROM must be used if the Multibus board interrupts on more than one level and a separate vector is desired for each level. The switch sections are in DIP switch 12. The PROM, if used, is installed at U402.

NOTE *Please refer to* Writing Device Drivers for the Sun Workstation, *part number 800-1304, when selecting an interrupt vector. (The section you want is titled "Interrupt Vector Assignments," in the Device Driver manual.) It is very important that you do not select an interrupt vector already in use.*

DIP 12—Selects the VME Interrupt Vector to use if the Multibus board interrupts. Switch sections 1-8 correspond to VME vector bits 0-7 respectively. A switch section ON sets the corresponding bit to 0. For example, if the desired VME interrupt vector number is 0x48, the correct switch setting is (notice that the bit-ordering goes from right to left):

Section:	1	2	3	4	5	6	7	8
	ON	ON	ON	OFF	ON	ON	OFF	ON
	D0	D1	D2	D3	D4	D5	D6	D7
(binary)	0	0	0	1	0	0	1	0
(hex)		8				4		

Figure 2-14 *Switch Setting for an Interrupt Vector Number of 0x48*



NOTE *The VME interrupt vector number is the 68000 vector address divided by 4. Thus VME vector 0x48 causes the 68000 to fetch its interrupt vector from memory location 0x48 * 4 = 0x120.*

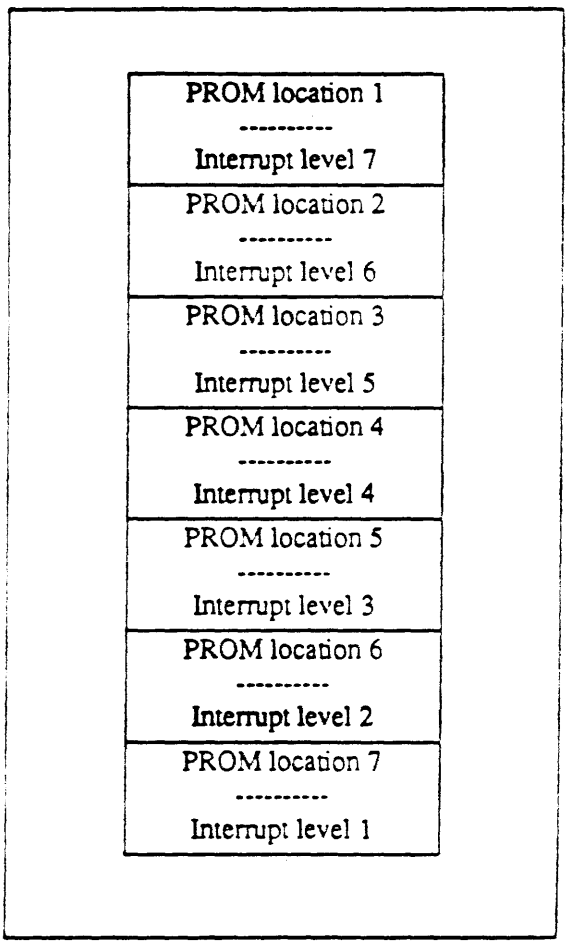
If the switch is used to set the interrupt vector, the Interrupt Vector PROM must NOT be installed in its socket. If the PROM is used to set the interrupt vector, all the switch sections in DIP 12 must be set to OFF.

Interrupt Vector PROM

If the Multibus board interrupts on different levels, it is possible to configure the adapter board to provide a separate VME Interrupt Vector for each Multibus interrupt level. This is done by programming a 32-by-8 bipolar PROM with the desired interrupt vectors. Locations 0 through 6 in the PROM are used for the interrupt vectors for Multibus interrupt levels 7 through 1 respectively. Other locations in the PROM are not used. Note that Multibus interrupt level 0 cannot be used in any case, since the VMEbus has no level 0 interrupt.

PROM Data Bit	0	1	2	3	4	5	6	7
PROM Pin #	1	2	3	4	5	6	7	8
VME Data Line	D0	D1	D2	D3	D4	D5	D6	D7

Figure 2-15 *Interrupt Vector PROM*



If the switch is used to set the interrupt vector, the Interrupt Vector PROM must NOT be installed in its socket. If the PROM is used to set the interrupt vector, all the switch sections in DIP 12 must be set to OFF.

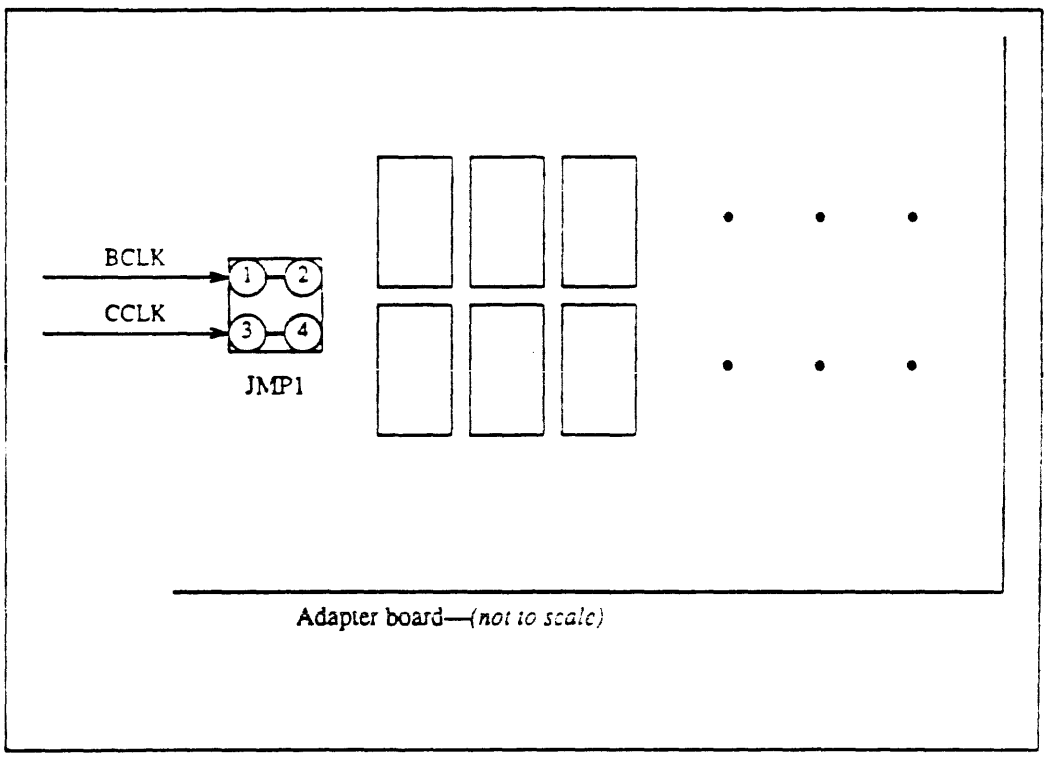
2.5. BCLK (Bus Clock) and CCLK (Constant Clock)—JMP1

For Multibus boards which require external BCLK and CCLK (most boards!), the adapter can provide these clocks. Jumper block JMP1 controls this feature. Section 1 is for BCLK, section 2 is for CCLK. The jumpers should be installed to provide the clocks.

JMP1:

- Section 1 BCLK: INSTALL to provide BCLK to the Multibus board
- Section 2 CCLK: INSTALL to provide CCLK to the Multibus board

Figure 2-16 *BCLK and CCLK Jumper, JMP1*



3

Theory of Operations

3

Theory of Operations

3.1. Overview

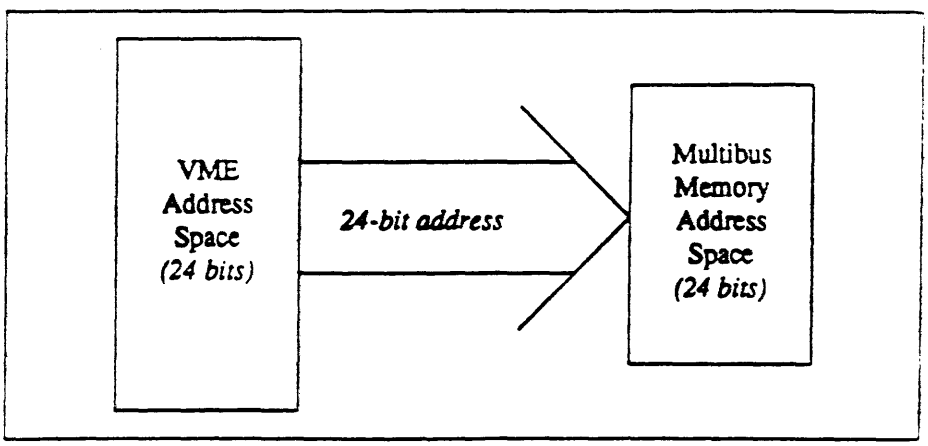
The VME-to-Multibus board is an adapter which allows the use of Multibus cards on the VMEbus of the Sun-2 and Sun-3 product line. (For an enumeration of which products and exact backplane-location within these products, please see the Cardcage Slot Assignment and Backplane Configuration Guide, part number 813-2004, available from Sun Sales or Service.)

The VME-to-Multibus card scheme is transparent to the system—there are no registers on the adapter board that software can modify. This section describes how VME signals are routed through the adapter board so that Multibus cards can be read, written, and interrupted (using programmed cycles). Functional block diagrams are included to illustrate how the adapter board works.

3.2. How the Adapter Board Works

There are a number of switch settings which must first be described in order to understand the functional capabilities of the VME-to-Multibus adapter board. The adapter board can respond to a block of addresses in the 24-bit VME address space. When the adapter board sees an address within the selected block, it passes the address bits to the Multibus board and generates a read or write command to Multibus memory space.

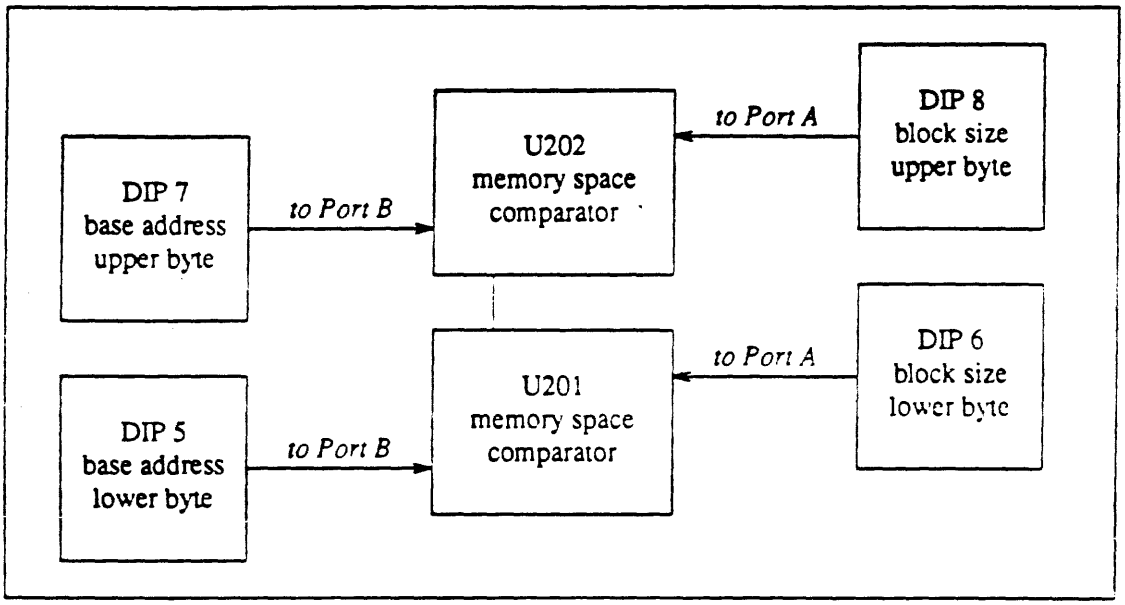
Figure 3-1 *VME and Multibus Memory Address Space*



This addressing function is controlled by the DIP switches (DIPs 5, 6, 7, 8) which set up in two 8-bit equal-to-comparators (U201, U202). If the comparators

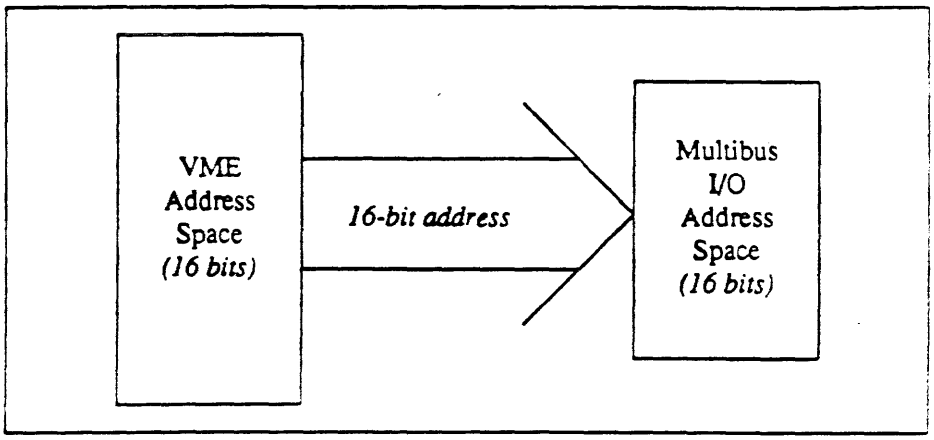
match the addresses a select signal is asserted toward control PAL U307 on the adapter board. At this point, the PAL would assert a "memory enable" strobe to the "transfer enable" PAL (U301) on the adapter board which selects the bidirectional transceivers for a data transfer. A "data out" (DATOUT-) signal from the same PAL controls the direction of the transfer at the transceivers.

Figure 3-2 *Memory Space Switches and Comparators*



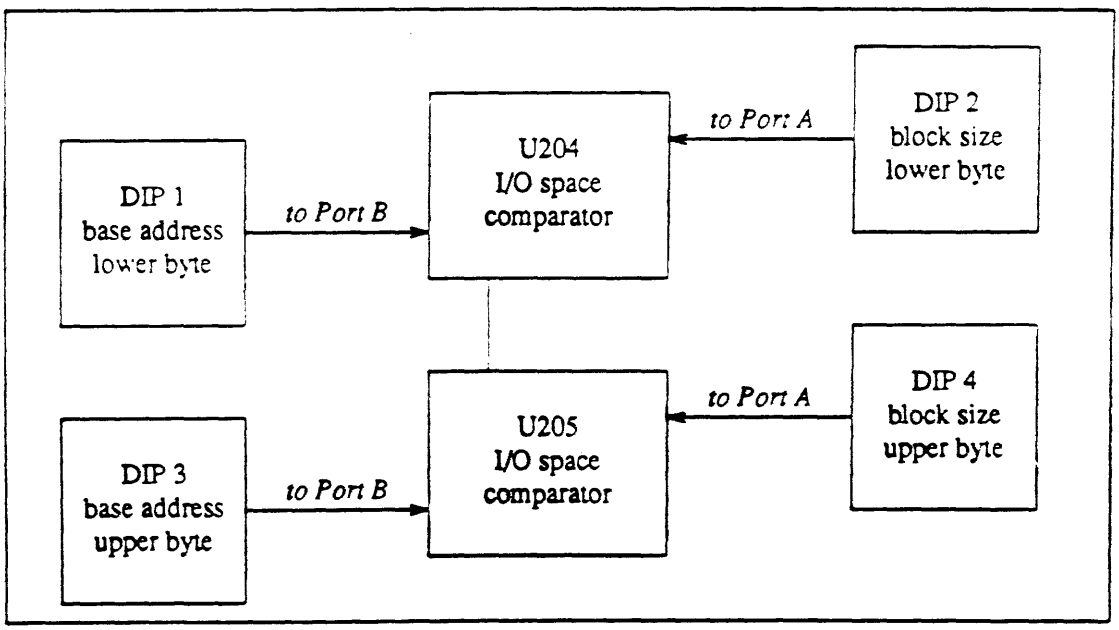
The adapter board can also respond to a block of addresses in the 16-bit VME address space. Here, when the adapter board sees an address within the selected block, it passes the address bits to the Multibus board and generates a Multibus I/O read or write. This function is controlled by DIP switches on the adapter board (DIPs 1, 2, 3, 4).

Figure 3-3 *VME and Multibus I/O Address Space*



The 16-bit address will be set-up in two 8-bit equal-to-comparators (U204, U205), and assert select signals toward the control PAL at U307. This PAL then asserts I/O enable to the transfer PAL (U303).

Figure 3-4 *I/O Space Switches and Comparators*



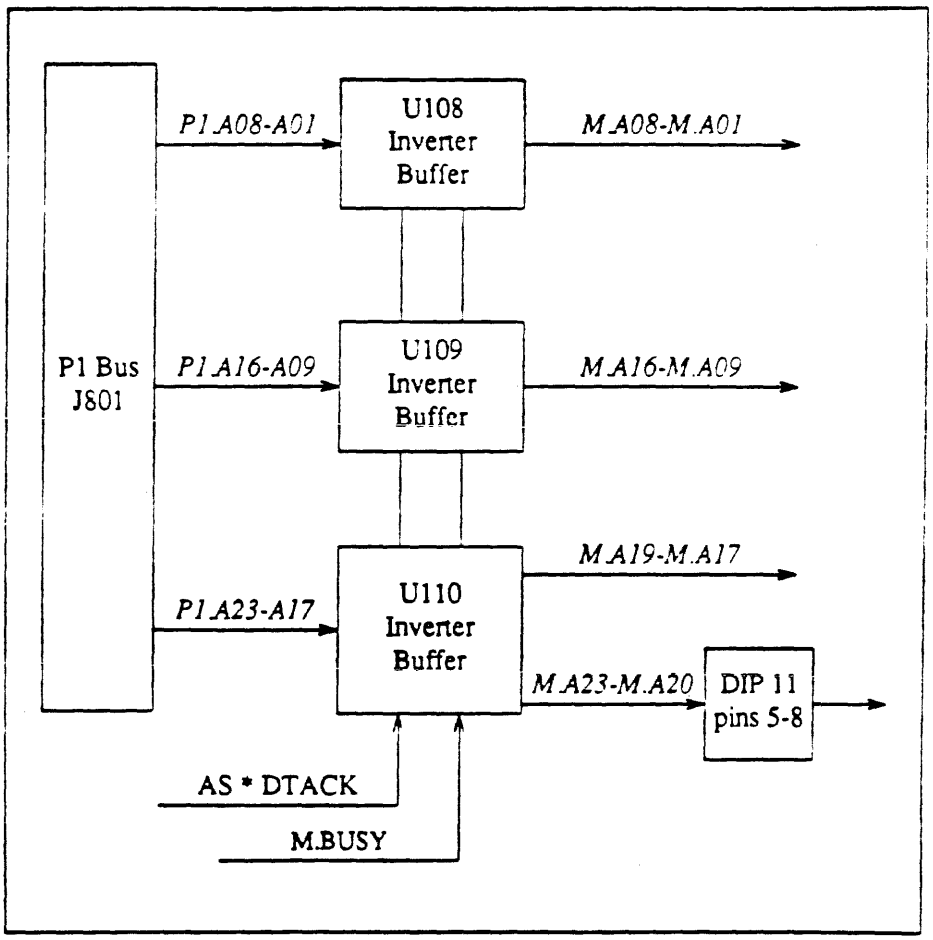
3.3. VMEbus to Multibus Addressing

During a VME read cycle to a Multibus card, P1 address lines A01-A23 are transferred to the Multibus adapter card in conjunction with P1 address strobe (AS) and P1 data strobes (DS0, DS1). If the Multibus board is a 24-bit address master, the four high-order address bits (A23-A20) are passed through by setting switch sections 5-8 of DIP switch 11 ON. Address lines which pass on to

Multibus cards are latched onto the adapter board by transparent latches (U108, U109, U110) with address strobe. After setting up, the inverted address lines are passed onto the Multibus. The latches are enabled by the AND of address strobe (AS-) and data transfer acknowledge (B.DTACK-); their outputs are enabled by the assertion of the busy signal, M.BUSY.

Note that VME address lines are active high, and Multibus address lines are active low, which is why the signals are inverted.

Figure 3-5 *Address Signal Flow: VMEbus to Multibus Board*



3.4. Multibus to VMEbus Addressing

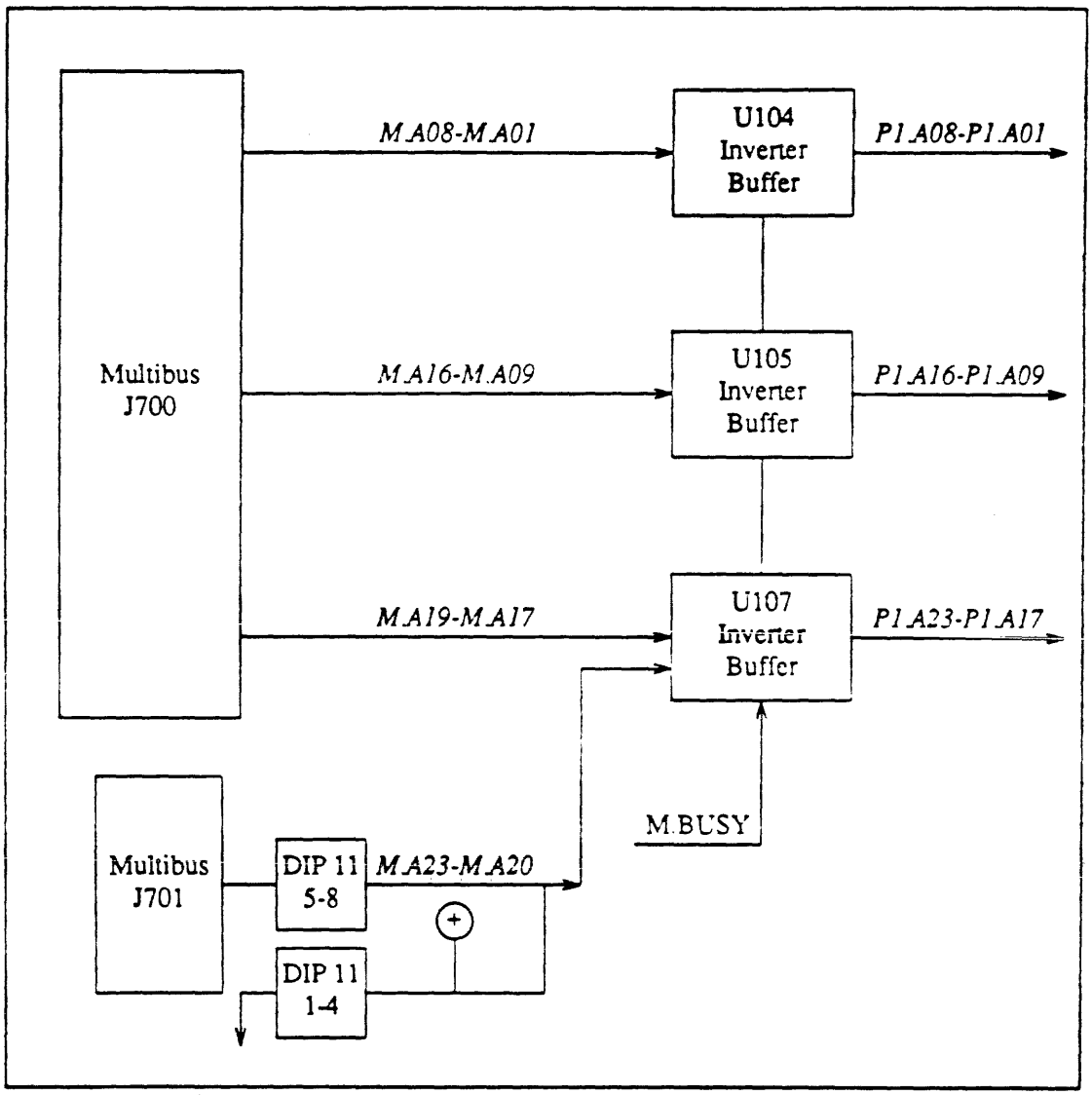
In the process of a read cycle from the Multibus to the VMEbus, Multibus address lines M.A01-A19 are enabled onto the adapter board via buffers (U104, U105, U107), which invert the lines and enable (pass) them on to the VMEbus (P1), via connector J801. For 20-bit Multibus boards, default values for address bits A23-A20 can be provided by setting DIP switch 11, sections 1-4 (respectively). Sections 1-4 are connected to ground at their input sides and their outputs connected to a pullup before passing through inverting buffer U107. Therefore, closing any of these four switch sections will assert a logical 1 on the corresponding VME address line.

If the Multibus board provides a 24-bit address, the four high order address bits (M.A23-M.A20) are passed to the adapter board through DIP switch 11, sections 5-8, to inverting buffer U107 to complete the 24-bit address to the VMEbus.

NOTE *To prevent conflicting signals, switch sections 1-4 MUST BE SET TO OFF when switch sections 5-8 are being used, and vice versa. This is because the output of switch 1 is electrically connected to the output of switch 8, switch 2 to switch 7, switch 3 to switch 6 and switch 4 to switch 5.*

At the end of the cycle, a P1 "data transfer acknowledge" (P1.DTACK) is sent from the VMEbus to the adapter board via a buffer (U106) which asserts "bus data transfer acknowledge" (B.DTACK-) to the transfer acknowledge PAL (U302). Refer to the block diagram below for an illustration of this function.

Figure 3-6 *Address Signal Flow: Multibus Board to VMEbus*



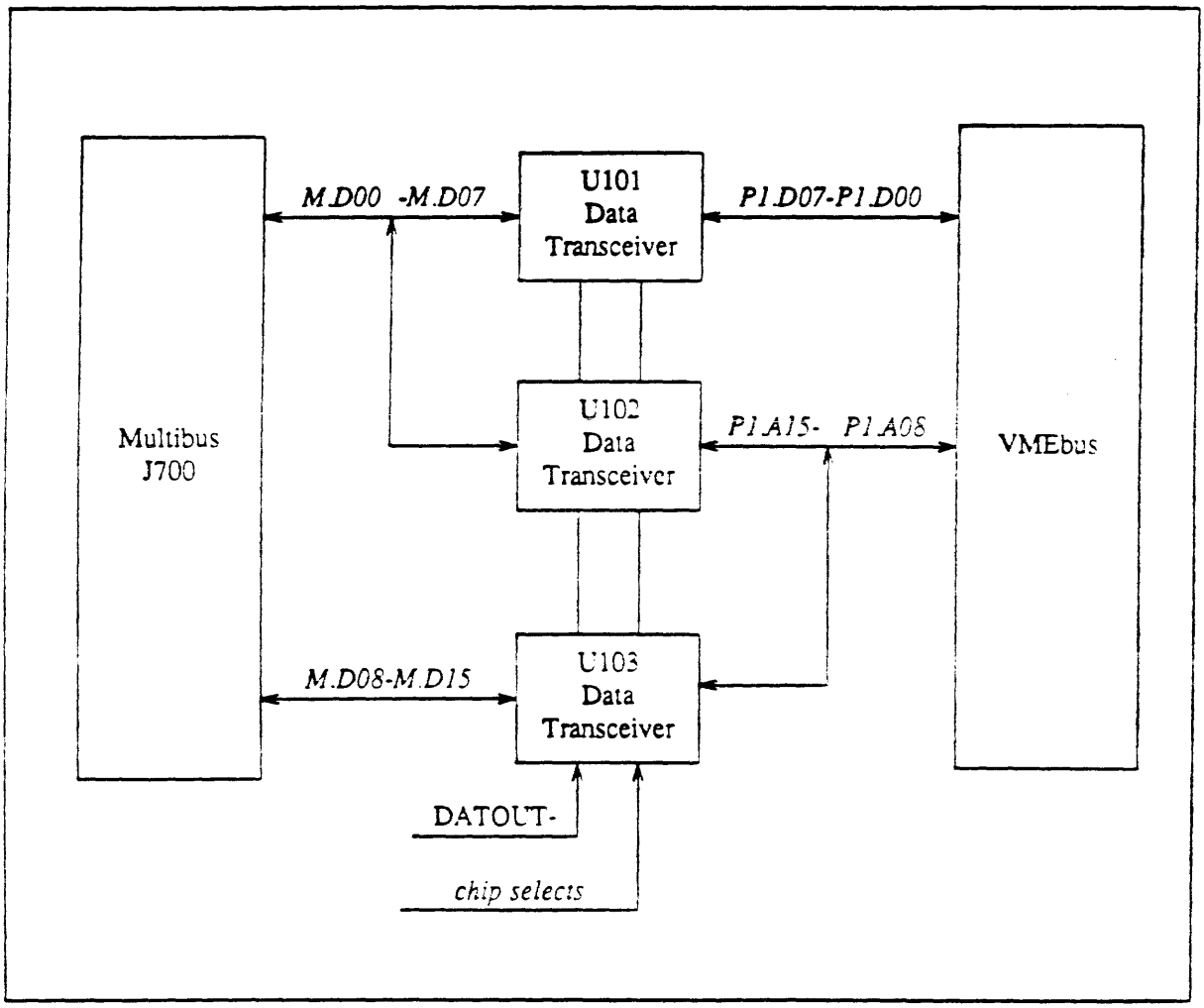
3.5. Data Transfers To and From the Adapter Board

During a transfer cycle, data is transferred from the Multibus to the VMEbus (and vice versa) via bidirectional transceivers (U101, U102, U103). Two of the transceivers (U101, U103) are used when the data transferred is a 16-bit word. For byte transfers, U101 is used when the data is a byte at an odd address, and U102 is used when data is a byte at an even address.

The three transceivers are selected by "low word/byte" (WBL-), "high byte" (BH-), and "high word" (WH-) signals which are driven by a data transfer enable PAL (U301). The PAL is set-up by "data strobes" (DS0, DS1) and bus write conditions originating from the VMEbus (P1) during a write cycle to the Multibus. For data transfers to the VMEbus (from the Multibus), a "data out"

(DATOUT-) signal is asserted to the transceivers for direction control toward the P1 data bus. DATOUT- is also set-up by the data transfer enable PAL (U301). Refer to the following block diagram for an illustration of this function.

Figure 3-7 *Data Signal Flow: Multibus Board to VMEbus*



3.6. Bus Request/Bus Grant Logic

For bus requests from the Multibus to the VMEbus, the requesting board will assert a "bus request" (BRQ1-) and "bus-priority-in level" (BPRN) to a handshanking PAL (U501) on the adapter board. This PAL then asserts a P1 bus request level (P1.BR3-) to the VMEbus (P1). If the bus is not busy, a P1 "bus grant" level (P1.BG3IN-) will be sent to the handshaking PAL which then asserts the bus grant as a "Multibus- priority-out" (P1.BG3OUT-) to the requesting Multibus board.

3.7. Interrupt Logic

Vectored interrupts are not supported on the Multibus, however, they are supported on the VMEbus and therefore must be translated by the adapter board. A VME interrupt vector is generated on the adapter board by a switch (DIP 12), or by a PROM (U402).

The switch is used if the Multibus board interrupts on one level only, or if a multi-level interrupt vectors to the same place. If a Multibus board interrupts on more than one level and a seperate vector is required for each level, the PROM must be used.

When one of the Multibus interrupt lines (INT1-INT7) goes active, it passes through octal transceivers (U405) to the VMEbus (P1.IRQ7-P1.IRQ1). When the processor sees the interrupt, it goes into an interrupt acknowledge cycle by putting the interrupt level on the lower-order address bits (P1.A3-P1.A1), while driving P1 "interrupt acknowledge" (P1.IACKIN-) and asserting P1 "address strobe." Note that P1 interrupt acknowledge is bused to every board on the backplane. A version of P1 "interrupt acknowledge-in/interrupt acknowledge-out" is daisy-chained from board to board.

When the adapter board sees this version of interrupt, it will check to see if the interrupt level specified by the address lines (P1.A3-P1.A1) is on the same level as the one on which it was trying to interrupt. If so, the adapter board will enable the interrupt vector (ENVEC-) through U406 NAND gates onto the VMEbus. If the interrupt level is not the one specified by the address lines, the adapter will pass the interrupt on to the next board with P1 "interrupt acknowledge-out."

3.8. VME DMA Cycle

The adapter board can generate a VME DMA cycle (when the adapter is the VMEbus master) in response to a DMA cycle by the Multibus board. The Multibus board can be a 20-bit address master, or a 24-bit address master (the adapter board is always 24-bits—slave or master). If the Multibus board is a 24-bit master, the four high order bits are passed through sections 8, 7, 6, and 5 (A23-A20, respectively) in DIP 11 on the adapter board. If the Multibus board is a 20-bit master, the four high order bits are supplied by sections 1-4 (respectively) of DIP switch 11.

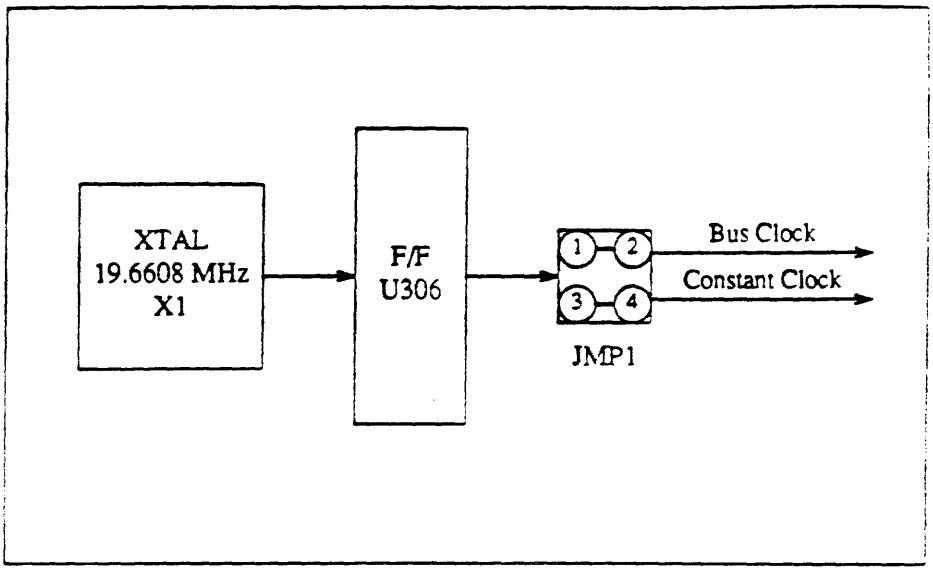
NOTE *If you are using switch sections 1-4 to supply the address bits, sections 5-8 must be set OFF, to avoid contention. If you are using switch sections 5-8 to pass the address bits, sections 1-4 must be set OFF.*

3.9. Clock Logic

The adapter board provides an external bus clock and constant clock for those Multibus boards (most boards) which require these clocks. The clocks originate at a 19.6608 MHz crystal (X1) and is divided down by a flip-flop (U306) to provide a 9.8304MHz clock. A jumper block on the adapter board (J1) allows the enabling/disabling of both the bus clock and the constant clock. Pins 1 to 2 should be jumpered for the bus clock, and pins 3 to 4 should be jumpered for the constant clock. Note that the jumpers should be installed to provide the clocks.

Refer to the diagram below for an illustration of these settings.

Figure 3-8 *BCLK and CCLK Circuitry*



A

Switch Settings Worksheet

A

Switch Settings Worksheet

NOTE *This appendix (Appendix A) is for those who already understand the theory behind the switch settings on the adapter board, and just need a workspace to figure the settings out. For a detailed explanation of how to set the switches, see the appendix following this.*

A.1. Setting Multibus Memory Space Switches

This section tells you how to set the base address and block size switches for the Multibus memory space. Included are both a

- sample switch setting (labelled "Example") and
- space for you to work out the switch settings for your own particular board.

Block Size Switches—Example

This page gives an example of sample block size switch settings for Multibus memory space.

EXAMPLE

```
Block size: 0x 0 0 2 0 0 0
```

⇒ *Discard the low-order byte, address bits A0-A7*

```
Block size: 0x 0 0 2 0
```

⇒ *Convert to binary:*

```
0000 0000 0010 0000
```

CAUTION There should be only a single one-bit in your number. (If there is more than one, then your block size is not a power of two. Pick the next larger size.)

⇒ *Turn the one-bit to a zero-bit, and turn all the zero-bits below it to one-bits.*

```
0 0 0 0   0 0 0 0   0 0 0 1   1 1 1 1
```

⇒ *Set DIP 8 and DIP 6 to this value: 0 = ON and 1 = OFF.*

```
0  0  0  0    0  0  0  0    0  0  0  1    1  1  1  1
-- -- -- -- | -- -- -- -- | -- -- -- -- | -- -- -- --
1  2  3  4    5  6  7  8  | 1  2  3  4    5  6  7  8
                          (section #)
<--------DIP 8----------> | <--------DIP 6--------->
```

Setting the Block Size Switches on Your Board

Fill in this page with your particular block size information for Multibus memory space.

YOUR DATA

```
YOUR BLOCK SIZE: 0x __ __ __ __ __ __
```

⇒ *Discard the low-order byte, address bits A0-A7*

```
YOUR BLOCK SIZE: 0x __ __ __ __
```

⇒ *Convert to binary:*

```
                  |                 |                 |
-- -- -- -- | -- -- -- -- | -- -- -- -- | -- -- -- --
<--------DIP 8----------> | <--------DIP 6--------->
```

CAUTION There should be only a single one-bit in your number. (If there is more than one, then your block size is not a power of two. Pick the next larger size.)

⇒ *Turn the one-bit to a zero-bit, and turn all the zero-bits below it to one-bits.*

YOUR REVISED BLOCK SIZE IN BINARY:

```
                  |                 |                 |
-- -- -- -- | -- -- -- -- | -- -- -- -- | -- -- -- --
<--------DIP 8----------> | <--------DIP 6--------->
```

⇒ *Enter your block size here.*

```
DIP 8:  ___   ___   ___   ___     ___   ___   ___   ___
        A23   A22   A21   A20     A19   A18   A17   A16

DIP 6:  ___   ___   ___   ___     ___   ___   ___   ___
        A15   A14   A13   A12     A11   A10   A09   A08
```

⇒ *Set DIP 8 and DIP 6 to this value: 0 = ON and 1 = OFF.*

```
                  |                 |                 |
-- -- -- -- | -- -- -- -- | -- -- -- -- | -- -- -- --
1  2  3  4    5  6  7  8  | 1  2  3  4    5  6  7  8
                           (section #)
<--------DIP 8----------> | <--------DIP 6--------->
```

Base Address Switches—Example

This page gives an example of sample base address switch settings for Multibus memory space.

EXAMPLE

⇒ *Find your base address.*

Base address: 0x 2 8 0 0 0 0

⇒ *Discard the low-order byte, address bits A0-A7*

Base address: 0x 2 8 0 0

⇒ *Convert to binary:*

0010 1000 0000 0000

⇒ *Remember the bits you turned from zero to one in the block size? Turn those same bits to ones here.*

change 0010 1000 0000 0000 *to* 0010 1000 0001 1111

⇒ *Enter your base address here.*

DIP 7:	0	0	1	0	1	0	0	0
	$\overline{A23}$	$\overline{A22}$	$\overline{A21}$	$\overline{A20}$	$\overline{A19}$	$\overline{A18}$	$\overline{A17}$	$\overline{A16}$
DIP 5:	0	0	0	1	1	1	1	1
	$\overline{A15}$	$\overline{A14}$	$\overline{A13}$	$\overline{A12}$	$\overline{A11}$	$\overline{A10}$	$\overline{A09}$	$\overline{A08}$

⇒ *Set DIP 7 and DIP 5 to this value: 0 = ON and 1 = OFF.*

```
 0  0  1  0 |  1  0  0  0 |  0  0  0  1 |  1  1  1  1
-- -- -- -- | -- -- -- -- | -- -- -- -- | -- -- -- --
1  2  3  4    5  6  7  8  | 1  2  3  4    5  6  7  8
                          (section #)
<--------DIP 7----------> | <--------DIP 5--------->
```

Setting the Base Address Switches on Your Board

Fill in this page with your particular memory space base address information.

⇒ *Find your base address.*

YOUR DATA

YOUR BASE ADDRESS: 0x __ __ __ __ __ __

⇒ *Discard the low-order byte, address bits A0-A7*

YOUR BASE ADDRESS: 0x __ __ __ __

⇒ *Convert to binary:*

```
                |               |               |
-- -- -- -- | -- -- -- -- | -- -- -- -- | -- -- -- --
<--------DIP 7----------> | <--------DIP 5--------->
```

⇒ *Remember the bits you turned from zero to one in the block size? Turn those same bits to ones here.*

```
                |               |               |
-- -- -- -- | -- -- -- -- | -- -- -- -- | -- -- -- --
<--------DIP 7----------> | <--------DIP 5--------->
```

⇒ *Enter the base address here.*

```
DIP 7:
        A23   A22   A21   A20     A19   A18   A17   A16

DIP 5:
        A15   A14   A13   A12     A11   A10   A09   A08
```

⇒ *Set DIP 7 and DIP 5 to this value: 0 = ON and 1 = OFF.*

```
                |               |               |
-- -- -- -- | -- -- -- -- | -- -- -- -- | -- -- -- --
1  2  3  4    5  6  7  8  | 1  2  3  4    5  6  7  8
                          (section #)
<--------DIP 7----------> | <--------DIP 5--------->
```

A.2. Setting Multibus I/O Space

This section tells you how to set the base address and block size switches for the Multibus I/O space. Included are both a

- sample switch setting (labelled "Example") and
- space for you to work out the switch settings for your own particular board.

Block Size Switches—Example

This page gives an example of sample block size switch settings for Multibus I/O space.

EXAMPLE

```
Block size: 0x 0 0 0 8
```

⇒ *Ignore the low-order address bit, A0.*

⇒ *Convert to binary:*

```
0000 0000 0000 1000
```

CAUTION **There should be only a single one-bit in your number. (If there is more than one, then your block size is not a power of two. Pick the next larger size.)**

⇒ *Turn the one-bit to a zero-bit, and turn all the zero-bits below it to one-bits.*

Change `0000 0000 0000 1000` *to* `0000 0000 0000 0111`

⇒ *Set DIP 4 and DIP 2 to this value: 0 = ON and 1 = OFF.*

```
0  0  0  0    0  0  0  0    X† 1  0  1     0  0  1  1
-- -- -- -- | -- -- -- -- | -- -- -- -- | -- -- -- --
1  2  3  4    5  6  7  8  | 1  2  3  4     5  6  7  8
                          (section #)
<--------DIP 4----------> | <--------DIP 2--------->
```

†Remember, address bit A0 is not set into this DIP switch.

Setting the Block Size Switches on Your Board

Fill in this page with your particular Multibus I/O space block size information.

YOUR DATA

YOUR BLOCK SIZE: 0x ___ ___ ___ ___

⇒ *Convert to binary:*

```
                                        X†
-- -- -- -- | -- -- -- -- | -- -- -- -- | -- -- -- --
<--------DIP 4----------> | <--------DIP 2--------->
```

CAUTION **There should be only a single one-bit in your number. (If there is more than one, then your block size is not a power of two. Pick the next larger size.)**

⇒ *Turn the one-bit to a zero-bit, and turn all the zero-bits below it to one-bits.*

YOUR REVISED BLOCK SIZE IN BINARY:

```
                                        X†
-- -- -- -- | -- -- -- -- | -- -- -- -- | -- -- -- --
<--------DIP 4----------> | <--------DIP 2--------->
```

⇒ *Enter your block size here.*

```
DIP 4:   A15  A14  A13  A12    A11  A10  A09  A08

DIP 2:  XXX
       (not   A07  A06  A05    A04  A03  A02  A01
       used)
```

⇒ *Set DIP 4 and DIP 2 to this value: 0 = ON and 1 = OFF.*

```
                                        X†
-- -- -- -- | -- -- -- -- | -- -- -- -- | -- -- -- --
1  2  3  4    5  6  7  8  | 1  2  3  4    5  6  7  8
                            (section #)
<--------DIP 4----------> | <--------DIP 2--------->
```

†Remember, address bit A0 is not set into this DIP switch.

Base Address Switches—Example

This page gives an example of sample base address switch settings for Multibus I/O space.

EXAMPLE

⇒ *Find your base address.*

Base address: 0x 0 0 A 0

⇒ *Ignore the low-order address bit, A0.*

⇒ *Convert to binary:*

0000 0000 1010 0000

⇒ *Remember the bits you turned from zero to one in the block size? Turn those same bits to ones here.*

Change 0000 0000 1010 0000 *to* 0000 0000 1010 0111

⇒ *Enter the base address here.*

DIP 3:	0	0	0	0	0	0	0	0
	$\overline{A15}$	$\overline{A14}$	$\overline{A13}$	$\overline{A12}$	$\overline{A11}$	$\overline{A10}$	$\overline{A09}$	$\overline{A08}$
DIP 1:	XXX	1	0	1	0	0	1	1
	(not used)	$\overline{A07}$	$\overline{A06}$	$\overline{A05}$	$\overline{A04}$	$\overline{A03}$	$\overline{A02}$	$\overline{A01}$

⇒ *Set DIP 3 and DIP 1 to this value: 0 = ON and 1 = OFF.*

```
 0  0  0  0    0  0  0  0    X† 1  0  1    0  0  1  1
-- -- -- -- | -- -- -- -- | -- -- -- -- | -- -- -- --
1  2  3  4    5  6  7  8  | 1  2  3  4    5  6  7  8
                           (section #)
<--------DIP 3----------> | <--------DIP 1--------->
```

†Remember, address bit A0 is not set into this DIP switch.

Setting the Base Address Switches on Your Board

Fill in this page with your particular Multibus I/O space base address information.

YOUR DATA

⇒ *Find your base address.*

YOUR BASE ADDRESS: 0x _ _ _ _

NOTE *Remember to ignore the low-order address bit, A0.*

⇒ *Convert to binary:*

```
_ _ _ _ | _ _ _ _ | XX† _ _ _ | _ _ _ _
<--------DIP 3----------> | <--------DIP 1--------->
```

⇒ *Remember the bits you turned from zero to one in the block size? Turn those same bits to ones here.*

```
_ _ _ _ | _ _ _ _ | XX† _ _ _ | _ _ _ _
<--------DIP 3----------> | <--------DIP 1--------->
```

⇒ *Enter the base address here.*

DIP 3:

$\overline{A15}$	$\overline{A14}$	$\overline{A13}$	$\overline{A12}$	$\overline{A11}$	$\overline{A10}$	$\overline{A09}$	$\overline{A08}$

DIP 1: XXX

(not used)	$\overline{A07}$	$\overline{A06}$	$\overline{A05}$	$\overline{A04}$	$\overline{A03}$	$\overline{A02}$	$\overline{A01}$

⇒ *Set DIP 3 and DIP 1 to this value: 0 = ON and 1 = OFF.*

```
                                    X†
-- -- -- -- | -- -- -- -- | -- -- -- -- | -- -- -- --
1  2  3  4    5  6  7  8  | 1  2  3  4    5  6  7  8
                           (section #)
<--------DIP 3----------> | <--------DIP 1--------->
```

†Remember, address bit A0 is not set into this DIP switch.

A.3. DIP Switch 11

This section tells you how to set the switch sections for DIP switch 11. There are both

- sample settings (labelled "Example,") and
- space for you to figure out the settings for your own board (labelled "Your Board").

DIP switch 11 is divided into two functional parts:

1. sections 1-4 control DMA transfer address
2. sections 5-8 control Multibus memory address space size.

When using one functional part (either switch sections 1-4 or sections 5-8) the other functional part must be set OFF to avoid contention.

DIP Switch 11, Sections 5-8—Multibus Memory Address Space Size

For 24-bit addressing, set sections 5-8 of DIP switch 11 ON (allowing address bits A23-A20 to pass through).

For 20-bit addressing, set sections 5-8 of DIP switch 11 OFF (isolating the Multibus P2 connector from the adapter board's address logic).

NOTE *For 24-bit address boards, sections 1-4 of DIP switch 11 should be OFF, even if your board does not do DMA transfers. (See the following section, "DIP Switch 11, Sections 1-4—DMA Transfer Address.")*

SETTING MEMORY ADDRESS SPACE SIZE:

EXAMPLE BOARD

For a 24-bit Multibus board:

⇒ *Set sections 5-8 of DIP 11 ON (allowing A23-A20 to pass through).*

(switch)	Sec. 5	Sec. 6	Sec. 7	Sec. 8	
DIP 11:	ON	ON	ON	ON	
	$\overline{A20}$	$\overline{A21}$	$\overline{A22}$	$\overline{A23}$	*(pass these bits through the board)*

SETTING MEMORY ADDRESS SPACE SIZE: YOUR BOARD

⇒ *For a 24-bit Multibus board: set sections 5-8 ON.*

⇒ *For a 20-bit Multibus board: set sections 5-8 OFF.*

	Sec. 5	Sec. 6	Sec. 7	Sec. 8
DIP 11:	___	___	___	___

DIP Switch 11, Sections 1-4— DMA Transfer Address

If your Multibus board handles 24-bit addressing, then set sections 1-4 of DIP 11 to OFF.

If your Multibus board does DMA transfers, but only provides 20 address bits, sections 1-4 of DIP switch 11 can be used to provide the 4 high-order bits of the 24-bit address which the VMEbus requires. In order to access Sun main memory via DVMA transfers, *these bits must be set to zero*! The only time these switch sections (sections 1-4) should be set to provide any other value than zero is in the case where the board will be doing DMA to some other device and **NEVER** to the Sun memory. These situations are very rare!

24-BIT MULTIBUS BOARD: EXAMPLE

For a 24-bit Multibus board:

⇒ *Set sections 1-4 of DIP 11 OFF.*

(switch)	Sec. 1	Sec. 2	Sec. 3	Sec. 4
DIP 11:	OFF	OFF	OFF	OFF

20-BIT MASTER DOING DVMA TO SUN MEMORY: EXAMPLE

The DVMA port on the Sun CPU board responds to addresses in the 0-1 Mbyte range. Since 20 bits address a 1 Mbyte range, the high order address bits (A23-A20) must be set to a binary zero (0000) in order for a 20-bit Multibus board to do DVMA to Sun memory.

For a 20-bit Multibus board:

⇒ *Set the binary value 0000 into sections 1-4 of DIP 11. Remember: 0 = OFF and 1 = ON.*†

(switch)	Sec. 1	Sec. 2	Sec. 3	Sec. 4
DIP 11:	0	0	0	0
	OFF	OFF	OFF	OFF

20-BIT MASTER DOING DMA ONLY TO ANOTHER PERIPHERAL: EXAMPLE

In a 20-bit master, the remaining (top) four address bits, A23-A20, must be supplied by DIP switch 11, sections 1-4.

The *only* time that these switches should be set to any other value than zero is in the case where the board is doing DMA *only to some other device and NEVER to Sun memory*. These situations are VERY RARE!

⇒ *Determine the value to be set into switches 1-4 (let's choose an arbitrary value of 0xC). 0xC = (binary) 1 1 0 0.*

⇒ *Set this binary value (1100) into sections 1-4 of DIP 11. Remember, 0 = OFF and 1 = ON.*†

(switch)	Sec. 1	Sec. 2	Sec. 3	Sec. 4
DIP 11:	1	1	0	0
	ON	ON	OFF	OFF

†The Multibus is active low, so these settings are the reverse of other switches.

DIP SWITCH 11, SECTIONS 1-4:

YOUR BOARD

- ▫ **If your board handles 24-bit addressing: set sections 1-4 OFF**
- ▫ If your board handles 20-bit addressing but does not do DMA: set sections 1-4 OFF.
- ▫ If your board handles 20-bit addressing and will be doing DMA to SUN memory: set sections 1-4 to OFF.

(switch)	Sec. 1	Sec. 2	Sec. 3	Sec. 4
DIP 11:	OFF	OFF	OFF	OFF

- ▫ If your board handles 20-bit addressing and will be doing DMA *only to some other device and never to Sun memory* then:

⇒ *Determine the value you want to be set into switches 1-4.*

Your value is 0x_____

which is equal to binary ____ ____ ____ ____

⇒ *Set these four bits into sections 1-4 of DIP 11. Remember: 0 = OFF and 1 = ON.*†

(switch)	Sec. 1	Sec. 2	Sec. 3	Sec. 4
DIP 11:	___	___	___	___
	A23	A22	A21	A20

†The Multibus is active low, so these settings are the reverse of other switches.

A.4. Interrupt Vector Switch DIP 12

This section tells you how to set the switches for the the interrupt vector. There are both

- sample settings (labelled "Example,") and
- space for you to figure out the settings for your own board.

Interrupt Vector—Example

⇒ *Convert the hex value of the vector to binary:*

EXAMPLE

```
0xA6 = 1010 0110
```

⇒ *Set this value into DIP 12: 0 = ON and 1 = OFF.*

```
                (switch section #)          S1  S2  S3  S4  S5  S6  S7  S8
0xA6 = 1  0  1  0     0  1  1  0 =  0   1   1   0   0   1   0   1
       -- -- -- --    -- -- -- --   --- --- --- --- --- --- --- ---
(bit#) 7  6  5  4     3  2  1  0    0   1   2   3   4   5   6   7
```

Interrupt Vector—Your Board

⇒ *Convert the hex value of the vector to binary:*

YOUR BOARD

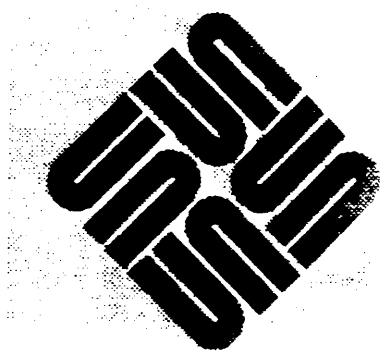
```
0x _____ _____ = _ _ _ _   _ _ _ _
```

⇒ *Set this value into DIP 12: 0 = ON and 1 = OFF.*

```
                                          S1  S2  S3  S4  S5  S6  S7  S8
0x__ =                          =
       -- -- -- --    -- -- -- --   --- --- --- --- --- --- --- ---
(bit#) 7  6  5  4     3  2  1  0    0   1   2   3   4   5   6   7
```

B

Example Configurations



B

Example Configurations

B.1. Xylogics 450 Disk Controller

```
Multibus Memory Space:  Not Used
Multibus I/O Space: 8 bytes starting at 0xEE40
DMA address size:   24 bits
Interrupt Vector:   0x48
BCLK, CCLK:     Needs external clocks
```

NOTE *Configure the Xylogics board for 24-bit operation.*

Switch Settings:

- For No Multibus Memory Space Response:

```
DIP 8-All OFF
DIP 6-All OFF
DIP 7-All  ON
DIP 5-All  ON
```

- For I/O space size 8:

DIP 2 Section	1	2	3	4	5	6	7	8
	X	ON	ON	ON	ON	ON	OFF	OFF

DIP 4 All ON

- For I/O base address 0xEE40:

DIP 1 Section	1	2	3	4	5	6	7	8
	X	ON	OFF	ON	ON	ON	OFF	OFF

DIP 3 Section	1	2	3	4	5	6	7	8
	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON

- For 24-bit Multibus DMA addressing:

```
DIP 11  Sections 1-4  All OFF    Sections 5-8   All ON
```

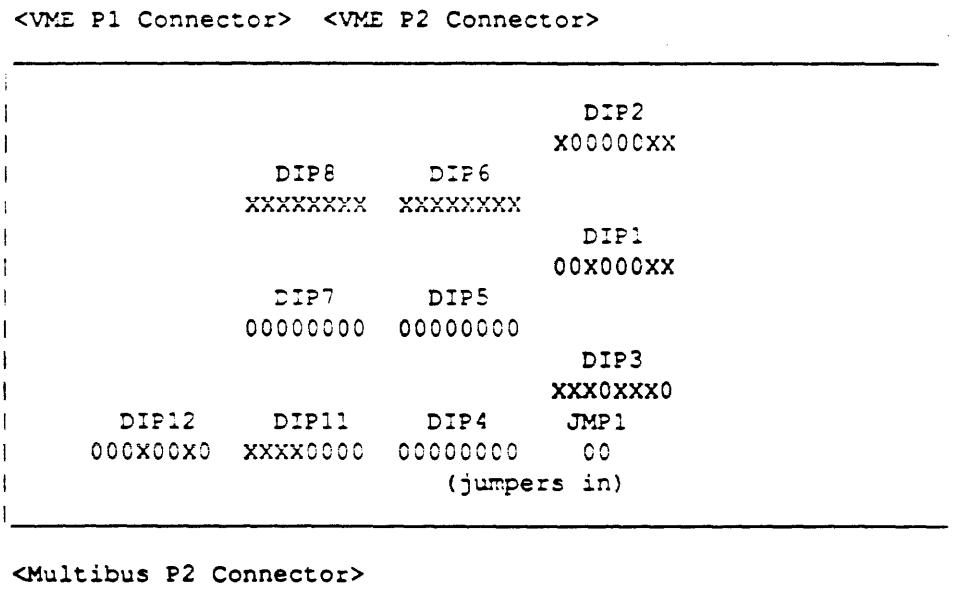
- For Interrupt Vector 0x48:

```
DIP 12  Section:   1   2   3   4   5   6   7   8
                  ON  ON  ON OFF  ON  ON OFF  ON
```

- For BCLK and CCLK:

```
JMP1   Section 1   INSTALLED     Section 2 INSTALLED
```

Following is a diagram of the switch settings (0 is ON, X is OFF).



B.2. Tapemaster 1/2 Inch Tape Controller

```
Multibus Memory Space:  Not Used
Multibus I/O Space: 2 bytes starting at 0x00A0
DMA address size:   20 bits
Interrupt Vector:   0x60
BCLK, CCLK:     Needs external clocks
```

Switch Settings:

- For No Multibus Memory Space Response:

```
DIP 8—All OFF
DIP 6—All OFF
DIP 7—All  ON
DIP 5—All  ON
```

- For I/O space size 2:

DIP 2 Section	1	2	3	4	5	6	7	8
	X	ON	ON	ON	ON	ON	ON	ON

DIP 4 All ON

- For I/O base address 0x00A0:

DIP 1 Section	1	2	3	4	5	6	7	8
	X	OFF	ON	OFF	ON	ON	ON	ON

DIP 3 Section	1	2	3	4	5	6	7	8
	ON	ON	ON	ON	ON	ON	ON	ON

- For 24-bit Multibus DMA addressing:

DIP 11 Sections 1-4 All OFF Sections 5-8 All ON

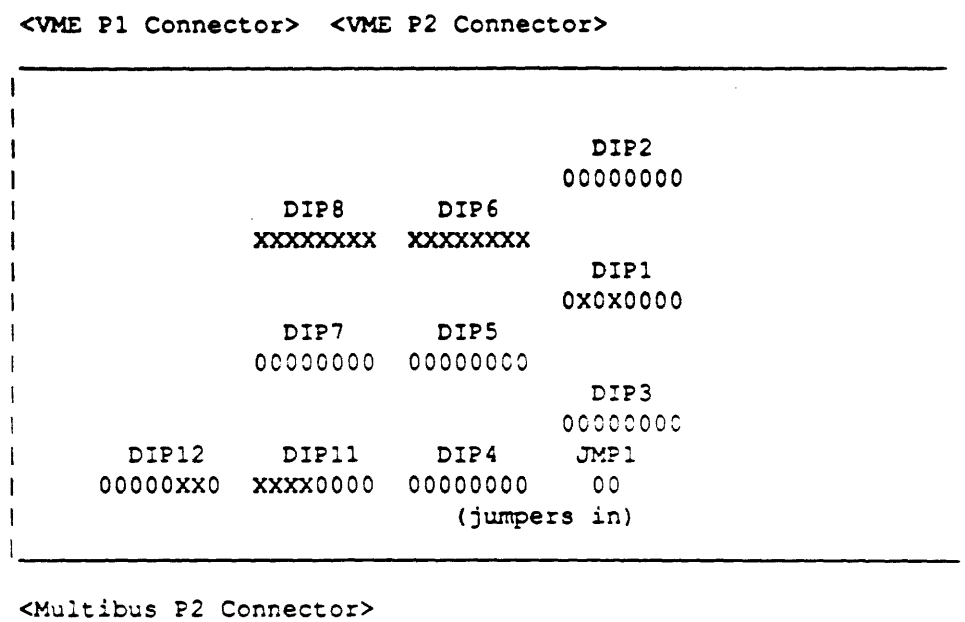
- For Interrupt Vector 0x60:

DIP 12 Section	1	2	3	4	5	6	7	8
	ON	ON	ON	ON	ON	OFF	OFF	ON

- For BCLK and CCLK:

JMP1 Section 1 INSTALLED Section 2 INSTALLED

Following is a diagram of the switch settings (0 is ON, X is OFF).



B.3. DMA Tester Board

```
Multibus Memory Space:  16K bytes starting at 0x280000
Multibus I/O Space: Not Used
DMA address size:   20 bits
Interrupt Vector:   0x48
BCLK, CCLK:     Needs external clocks
```

Switch Settings:

- For No Multibus I/O Space Response:

```
DIP 2-All OFF
DIP 4-All OFF
DIP 1-All  ON
DIP 3-All  ON
```

- For Memory space size 16K:

```
DIP 6  Section     1    2    3    4    5    6    7    8
                  ON   ON   OFF  OFF  OFF  OFF  OFF  OFF

DIP 8 All ON
```

- For Memory base address 0x280000:

```
DIP 5  Section     1    2    3    4    5    6    7    8
                  ON   ON   OFF  OFF  OFF  OFF  OFF  OFF

DIP 7  Section     1    2    3    4    5    6    7    8
                  ON   ON   OFF  ON   OFF  ON   ON   ON
```

- For 20-bit Multibus DMA addressing, using zeroes as the high-order 4 bits:

```
DIP 11  Sections 1-4  All OFF   Sections 5-8   All OFF
```

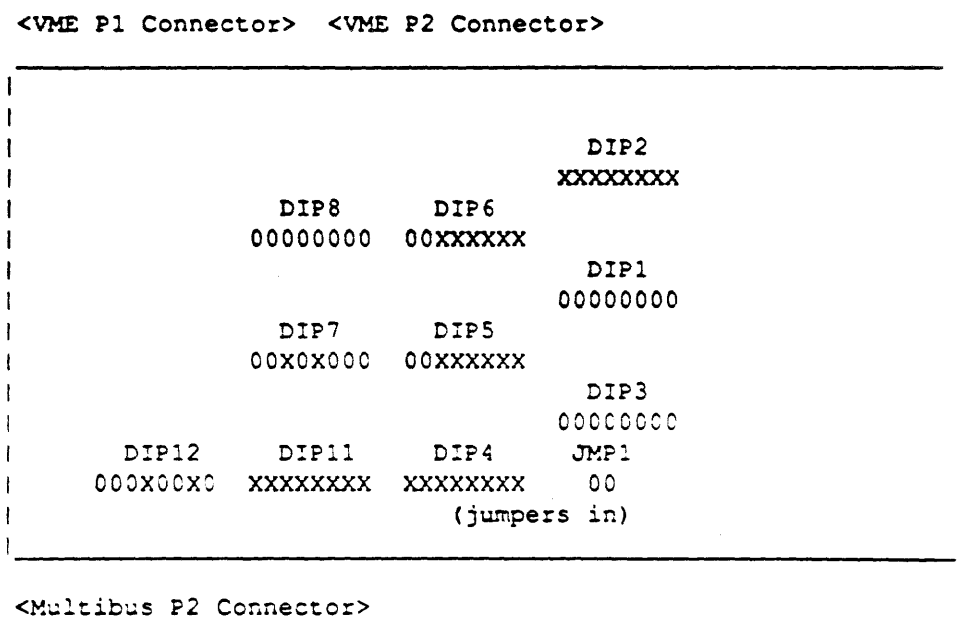
- For Interrupt Vector 0x48:

```
DIP 12  Section    1    2    3    4    5    6    7    8
                  ON   ON   ON   OFF  ON   ON   OFF  ON
```

- For BCLK and CCLK:

```
JMP1   Section 1   INSTALLED     Section 2 INSTALLED
```

Following is a diagram of the switch settings (0 is ON, X is OFF).



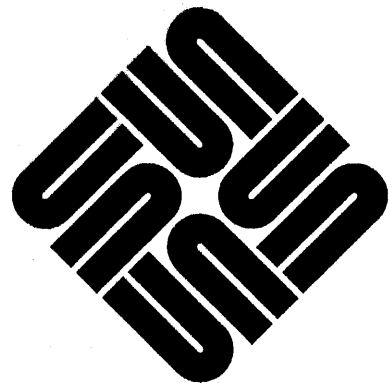
Index

Engineering & Technical Documentation

Not Available

At This Time

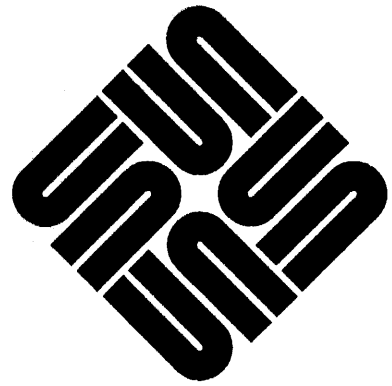
Depot Test Procedure



Not Available

At This Time

Miscellaneous Technical Documentation

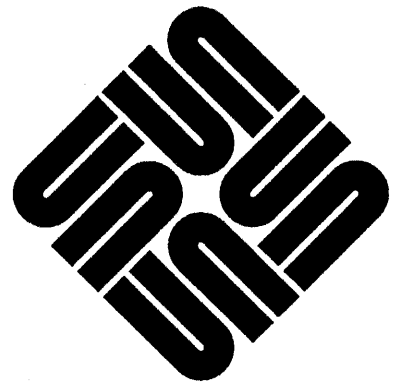


Not Available

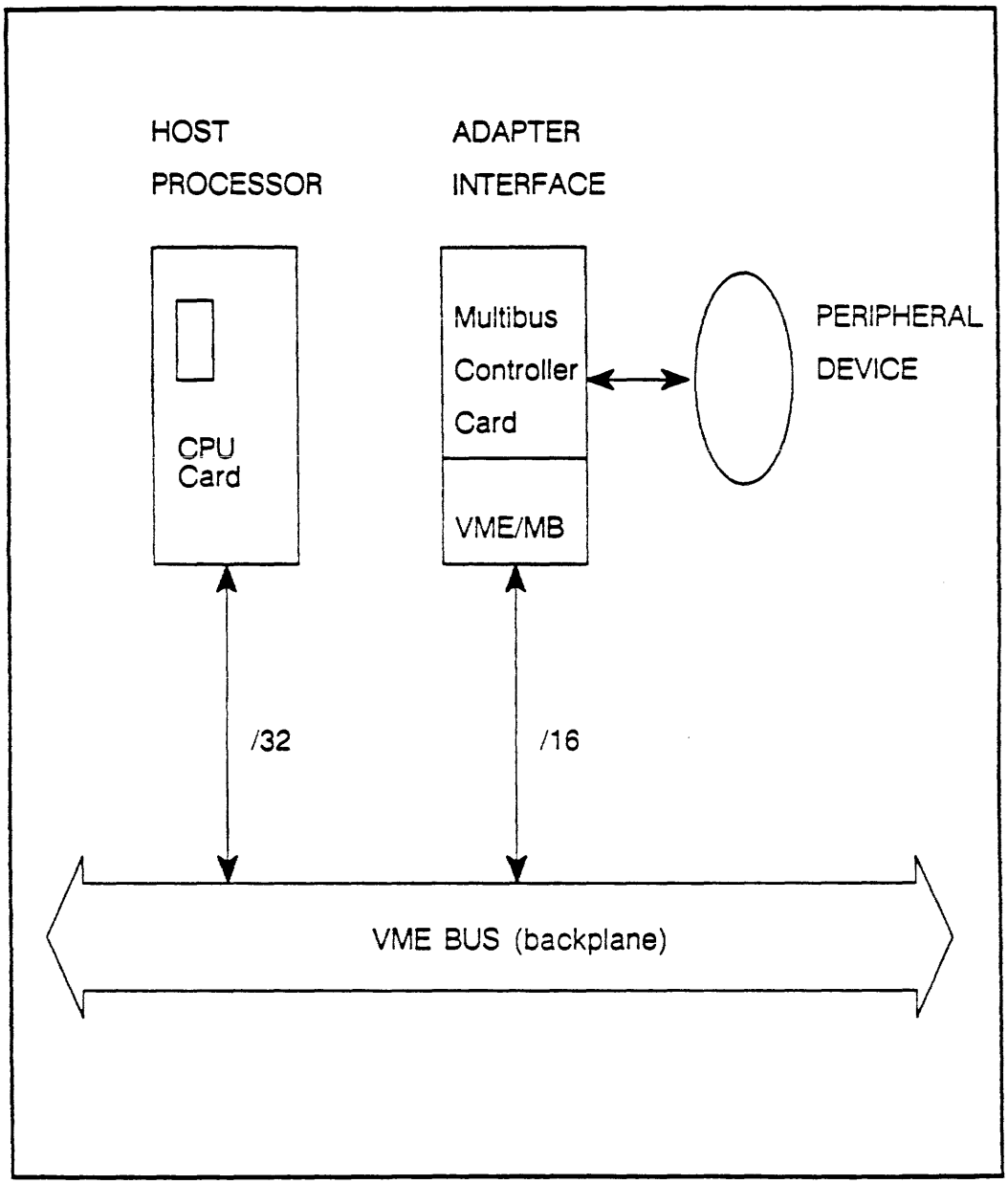
At This Time

Training Documentation

Section 1



VME to Multibus Adapter Card

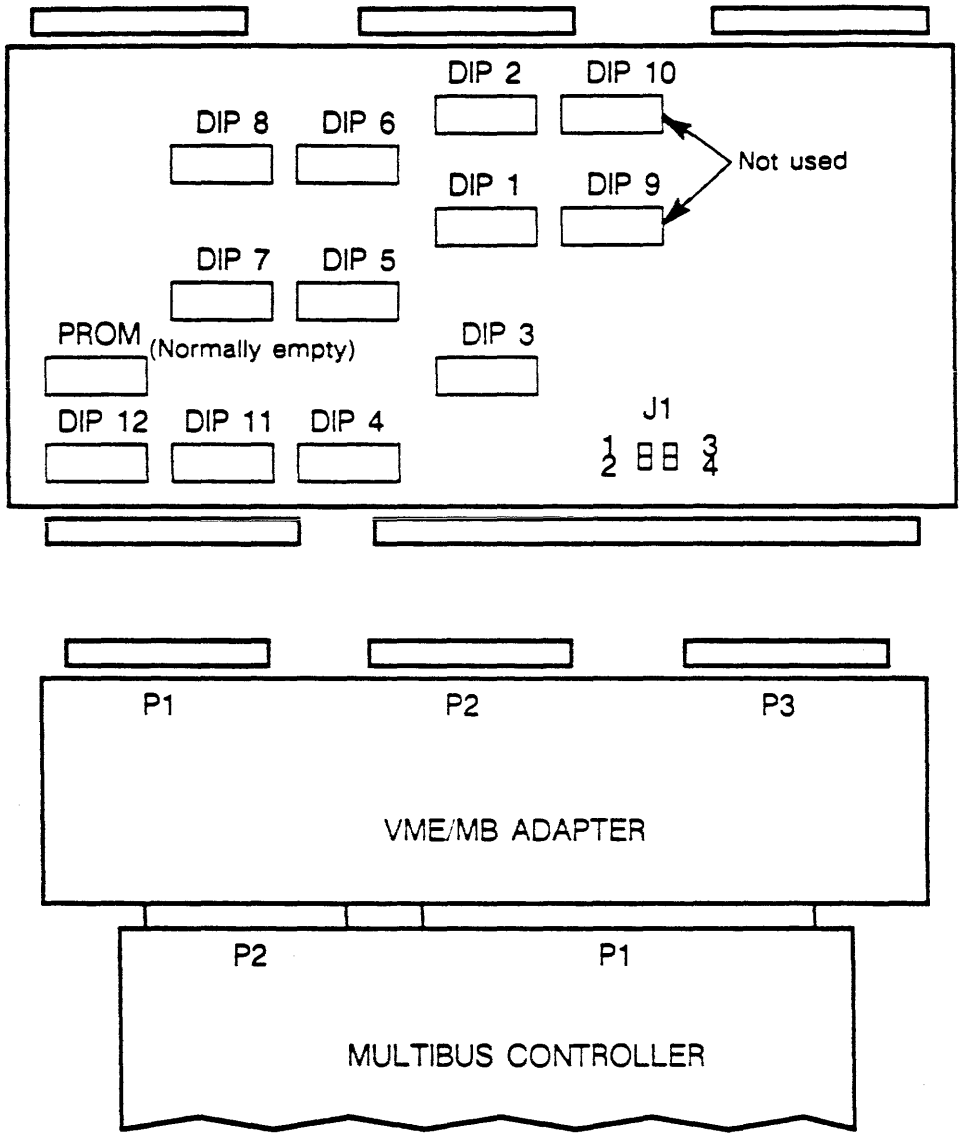


VME to Multibus Adapter Card

This card allows Multibus protocol 2-high cards to work with Sun VMEbus protocol 3-high systems.

The 2-high controller card (example: Xylogics 451 SMD disk) is plugged into the adapter and the entire assembly is plugged into the proper slot as if it were all one card.

VME to Multibus Adapter Layout



VME/MB MOUNTING

VME to Multibus Adapter Layout

- Each DIP has 8 switches 1-8.
- On is up, off is down.
- Do not use lead pencil to change switches.
- The prom socket, usually unstuffed, is for special order Sun Proms which would provide the customer with multiple interrupt vectors.

VME/MB Switch Settings for Xylogics 450/451 Controller Boards

SWITCH	1	2	3	4	5	6	7	8	DESCRIPTION
1	ON	ON	OFF	ON	ON	ON	OFF	OFF	ADDR 0x40 I/O
2	OFF	ON	ON	ON	ON	ON	OFF	OFF	I/O space=8
3	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	ADDR 0xEE
4	ON	ON	ON	ON	ON	ON	ON	ON	I/O space=8
5	ON	ON	ON	ON	ON	ON	ON	ON	24-bit addr space
6	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24-bit bolck size
7	ON	ON	ON	ON	ON	ON	ON	ON	24-bin addr space
8	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24-bit block size
11	OFF	OFF	OFF	OFF	ON	ON	ON	ON	Set addr A23-A20
12	ON	ON	ON	OFF	ON	ON	OFF	ON	Int Vec at 0x48
J1	Install pins 1-2 for BCLK					Install pins 3-4 for CCLK			

FIRST SMD (DISK) CONTROLLER

SWITCH	1	2	3	4	5	6	7	8	DESCRIPTION
1	ON	ON	OFF	ON	ON	OFF	OFF	OFF	ADDR 0x48 I/O
2	OFF	ON	ON	ON	ON	ON	OFF	OFF	I/Ospace=8
3	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	ADDR 0xEE
4	ON	ON	ON	ON	ON	ON	ON	ON	VME addr space
5	ON	ON	ON	ON	ON	ON	ON	ON	24-bit addr space
6	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24-bit block size
7	ON	ON	ON	ON	ON	ON	ON	ON	24-bit addr space
8	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24-bit block size
11	OFF	OFF	OFF	OFF	ON	ON	ON	ON	Sets addr A23-A20
12	OFF	ON	ON	OFF	ON	ON	OFF	ON	Int Vec 0x49
J1	Install pins 1-2 for BCLK					Install pins 3-4 for CCLK			

SECOND SMD (DISK) CONTROLLER

VME/MB Switch Settings for Xylogics 450/451 Controller Boards

Note: Switch 11, positions 5, 6, 7 and 8 are on for *all* cards except:

- Xylogics 472's.
- Gateway's.

VME/MB Settings For Gateway and Sunlink Controllers

SWITCH	1	2	3	4	5	6	7	8	DESCRIPTION
1	ON	ON	ON	ON	ON	ON	ON	ON	ADDR 0x00
2	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	No response to I/O space
3	ON	ON	ON	ON	ON	ON	ON	ON	ADDR 0x00
4	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	No response to I/O space
5	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24-bit addr space
6	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24-bit block size
7	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	24-bit addr space
8	ON	ON	ON	ON	OFF	OFF	OFF	OFF	24-bit block size
11	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	Sets addr A23-A20
12	OFF	ON	OFF	ON	OFF	OFF	OFF	ON	Int Vec 0x75
J1	Install pins 1-2 for BCLK					Install pins 3-4 for CCLK			

SECOND ETHERNET

SWITCH	1	2	3	4	5	6	7	8	DESCRIPTION
1	ON	ON	ON	ON	ON	OFF	OFF	OFF	ADDR 0x800
2	ON	ON	ON	ON	ON	OFF	OFF	OFF	I/O space = 16
3	ON	ON	ON	ON	OFF	ON	ON	ON	ADDR 0x0800
4	ON	ON	ON	ON	ON	ON	ON	ON	VME addr space
5	ON	ON	ON	ON	ON	ON	ON	ON	24-bit addr space
6	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24-bit block
7	ON	ON	ON	ON	ON	ON	ON	ON	24-bit addr space
8	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24-bit block
11	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	Sets addr A23-A20
12	ON	ON	OFF	OFF	ON	ON	ON	OFF	Int Vec 0x8C
J1	Install pins 1-2 for BCLK					Install pins 3-4 for CCLK			

FIRST SUNLINK CONTROLLER

VME/MB Settings for Xylogics 472 Tape and Systech ALM 1 Controllers

SWITCH	1	2	3	4	5	6	7	8	DESCRIPTION
Dip 1	ON	ON	OFF	OFF	ON	***	OFF	OFF	Addr 0x60 I/O
Dip 2	OFF	ON	ON	ON	ON	ON	OFF	OFF	I/O space = 8 bytes
Dip 3	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	Addr 0xEE for I/O
DIP 4	ON	ON	ON	ON	ON	ON	ON	ON	I/O space = 8
Dip 5	ON	ON	ON	ON	ON	ON	ON	ON	24-bit addr space
Dip 6	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24-bit block size
Dip 7	ON	ON	ON	ON	ON	ON	ON	ON	
Dip 8	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
Dip 9	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
Dip 10	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
Dip 11	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	Set A23 to A20
Dip 12	***	ON	OFF	ON	ON	OFF	OFF	ON	Int vector set to 0x64
JUMPERS	Install pins 1-2 for BCLK				Install pins 3-4 for CCLK				
*** set ON for xtc0 , set OFF for xtc1									

GCR (6250) 1/2-INCH TAPE CONTROLLER

SWITCH	1	2	3	4	5	6	7	8	DESCRIPTION
Dip 1	OFF	ON	ON	OFF	ON	ON	OFF	OFF	Addr 0x20 for I/O
Dip 2	OFF	ON	ON	ON	ON	ON	OFF	OFF	I/O space = 8
Dip 3	ON	ON	ON	ON	ON	OFF	OFF	ON	Addr 0x06 for I/O
Dip 4	ON	ON	ON	ON	ON	ON	ON	ON	I/O space = 8
Dip 5	ON	ON	ON	ON	ON	ON	ON	ON	VME 24-bit addr space
Dip 6	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24-bit block size
Dip 7	ON	ON	ON	ON	ON	ON	ON	ON	24-bit addr space
Dip 8	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24-bit block size
Dip 9	---	---	---	---	---	---	---	---	Not Used
Dip 10	---	---	---	---	---	---	---	---	Not Used
Dip 11	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	Sets addr A23-A20
Dip 12	ON	ON	ON	OFF	ON	ON	ON	OFF	Int Vec at 0x88
JUMPERS	Install pins 1-2 for BCLK				Install pins 3-4 for CCLK				

SYSTECH ALM 1 (MTI) INTERFACE CONTROLLER

Section 2

CHAPTER SEVEN SECTION 7C:

VME-MULTIBUS ADAPTER

OVERVIEW

The VME to Multibus board is an adapter which allows the use of Multibus cards on the VME bus for Sun 3 pedestal products. The VME to Multibus card scheme is transparent to the system in that there are no registers on the adapter board that software can modify. The following text defines how VME signals are routed through the adapter so that Multibus cards can be read and written, as well as interrupted using programmed cycles. Functional block diagrams have been included to illustrate how the adapter operates. The following block illustrates the VME interface to the adapter:

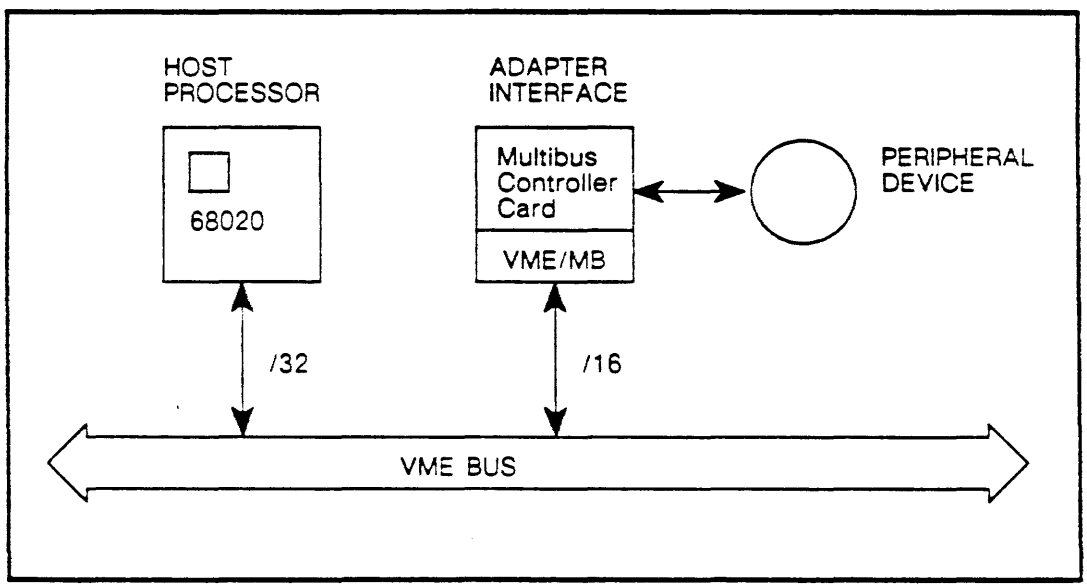


FIGURE 7C-1: VME INTERFACE

7C.1 ADAPTER CONFIGURATION CONSIDERATIONS

There are a number of switch settings which must first be described in order to better understand the functional capabilities of the VME to Multibus board. The adapter board can respond to a block of addresses in the 24-bit VME address space. When the adapter board sees an address within the selected block, it throughputs the address bits to the Multibus board and generates a Multibus

read or write command. The addressing can range from 256K to 16M bytes for Multibus memory address decoding.

This addressing function is controlled by the dip switches (DIP's 5,6,7,8,) which set up in three 8-bit equal-to-comparators. If the comparators match the addresses a select signal is asserted toward a control PAL on the adapter board. At this point, the PAL would assert a 'memory enable' strobe to the 'transfer enable' PAL on the adapter board which selects the bidirectional transceivers for a data transfer. A 'dataout' signal from the same PAL controls the direction of the transfer at the transceivers. Dips 5 and 7 (see Figure 7C-2) select the 24-bit VME space base address for access to the Multibus memory space.

The adapter board can also respond to a block of addresses in the 16-bit VME address space that the board responds to.. Here, when the adapter board sees an address within the selected block, it throughputs the address bits to the multibus board and generates a Multibus read or write. This function is controlled by dip switches on the adapter board (DIP's 8 and 6).

For Multibus I/O addressing, the adapter board can respond to a block of addresses in the 16-bit VME address space. When the adapter sees an address within the block set up by the switches, it passes the address bits to the Multibus board and asserts a Multibus I/O read or write. The address range of these blocks is from 2 Bytes to 64K bytes. This function is set-up in dip switches 1 through four.

The 16-bit address will be set-up in two 8-bit equal-to-comparators, and assert select signals toward the control PAL. This PAL then asserts I/O enable to the transfer PAL. Figure 7C-2 illustrates the configuration selects for the adapter board.

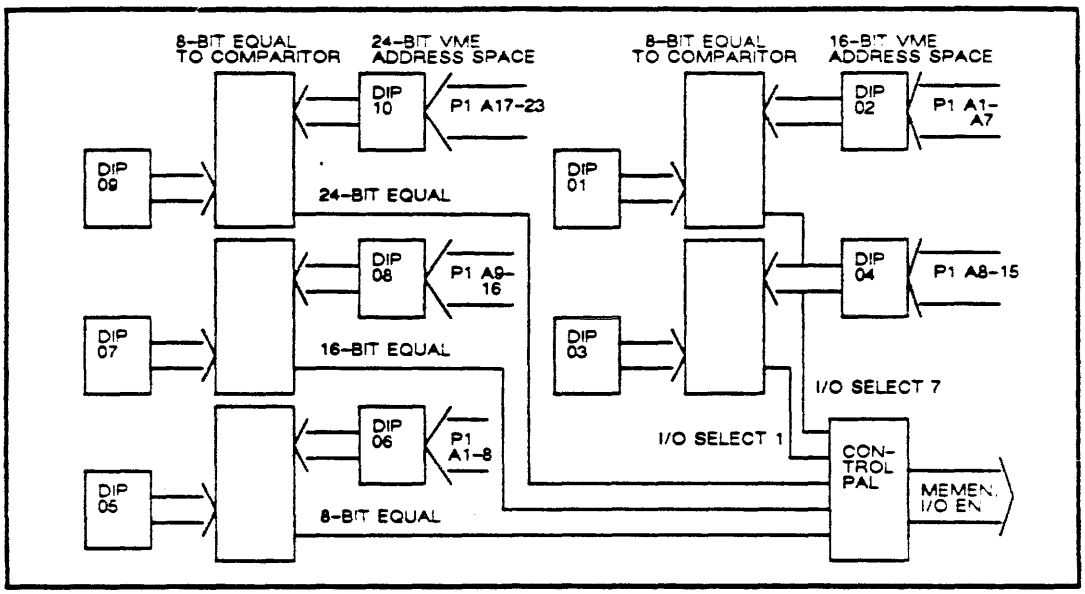


FIGURE 7C-2: CONFIGURATION SELECTS

7C-2 VME BUS TO MULTIBUS ADDRESSING

During a VME read cycle to a Multibus card, P1 address lines A01-A23 are transferred to to the multibus adapter card in conjunction with P1 address strobe (AS) and P1 data strobes (DS0,DS1). Address lines which pass on to Multibus cards are latched onto the adapter by transparent latches with address strobe. After setting up, the inverted address lines are passed onto the Multibus with the assertion of Multibus 'read'.

Note that VME address lines are active high, and Multibus address lines are active low. Address lines are inverted by the latches on the adapter card.

A transfer PAL is used to set up the Multibus read command using address and data strobes. While active, the read signal allows the addresses to pass to the Multibus at connector J700. At the end of the read cycle, the Multibus board will respond by asserting a 'transfer acknowledge' to the adapter, which asserts P1 'data transfer acknowledge', thus, completing the cycle. The following block diagram illustrates this function:

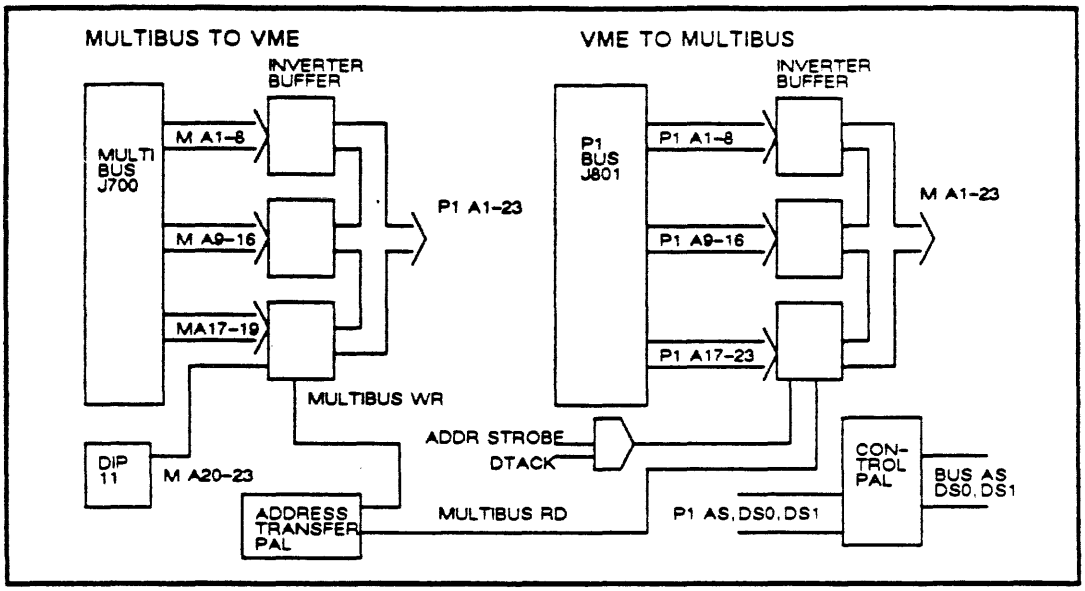


FIGURE 7C-3: VME/MULTIBUS ADDRESSING

7C.3 MULTIBUS TO VME BUS ADDRESSING

In the process of a read cycle from the Multibus to the VME bus, multibus address lines M.A01-A19 are enabled onto the adapter via buffers, which invert the lines and enable (pass) them on to the VME (P1) bus, via connector J801. A dip switch at DIP 11, furnishes the high order address bits (M. A20-A23) to the inverting buffer to complete the 24 bit address to the VME bus.

At the end of the cycle, a P1 'data transfer acknowledge' is sent from the VME bus to the adapter board via a buffer which asserts 'bus data transfer acknowledge' to the transfer acknowledge PAL. Refer to the block diagram above for an illustration of this function.

7C.4 DATA TRANSFERS TO AND FROM THE ADAPTER

During a transfer cycle, data is transferred from the Multibus to the VME bus (and vice versa) via bidirectional transceivers. Two of the transceivers are used when the data transferred is a 16-bit word. For byte transfers the transceivers are used when the data is a byte at an odd address, or when data is a byte at an even address. In a write cycle to the Multibus, 'multibus write' will be active. When the direction is toward the VME bus, 'multibus read' will be active on the adapter. Both signals are asserted via the transfer PAL.

The three transceivers are enabled by 'write enable' signals which are driven by a data transfer enable PAL. The PAL is set-up by 'data strobes' (DS0,DS1)

and bus write conditions originating from the VME (P1) bus during a write cycle to the multibus. For data transfers to the VME bus (from the Multibus), a 'dataout' signal is asserted to the transceivers for direction control toward the P1 data bus. Dataout is also set-up by the data transfer enable PAL. Refer to the following block diagram for an illustration of this function:

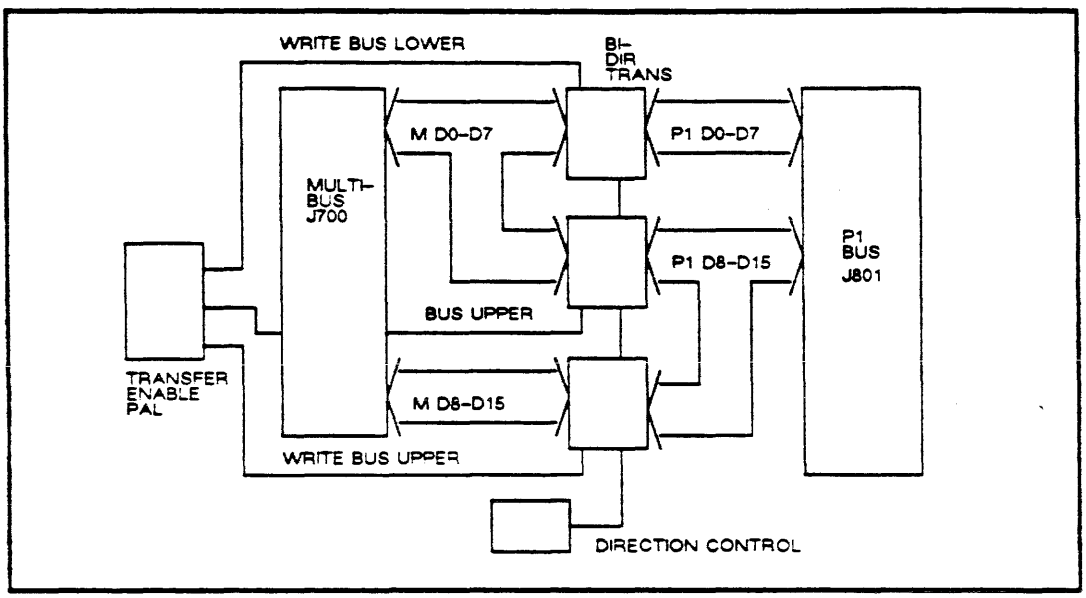


FIGURE 7C-4: VME/MULTIBUS DATA TRANSFERS

7C.5 BUS REQUEST/BUS GRANT LOGIC

For bus requests from the Multibus to the VME bus, the requesting board will assert a 'bus request' and 'bus-priority-in level' to a handshanking PAL on the adapter board. This PAL then asserts a P1 bus request level to the VME (P1) bus. If the bus is not busy, a P1 'bus grant' level will be sent to the handshaking PAL which then asserts the bus grant as a 'multibus- priority-out' to the requesting Multibus board.

7C.6 INTERRUPT LOGIC

Vectored interrupts are not supported on the Multibus, however, they are supported on the VME bus and therefore must be translated by the adapter board. A VME interrupt vector is generated on the adapter board by switches (DIP 12), or by an interrupt PROM(supplied by Sun).

The switches are used if the Multibus board interrupts on one level only. Where a Multibus board interrupts on more than one level, and a separate vector is required for each level, the PROM is used.

When one of the Multibus interrupt lines (INT1-INT7) goes active, it through puts to the VME bus via an open collector buffer (U405). When the processor sees the interrupt, it goes into an interrupt acknowledge cycle by putting the interrupt level on the lower-order address bits (P1 A1-A3), while driving P1 'interrupt acknowledge' and asserting P1 'address strobe'. Note that P1 interrupt acknowledge is bussed to every board on the backplane. A version of P1 'interrupt acknowledge-in/interrupt acknowledge-out' is daisy-chained from board to board.

When the adapter board sees this version of interrupt, it will check to see if the interrupt level specified by the address lines (P1 A1-A3) is in the same level as the one its trying to interrupt on. If so, the adapter will enable the interrupt vector onto the VME bus via the buffer. If the interrupt level is not the one specified by the address lines, the adapter will pass the interrupt on to the next board with P1 'interrupt acknowledge-out'. The following block diagram illustrates this function:

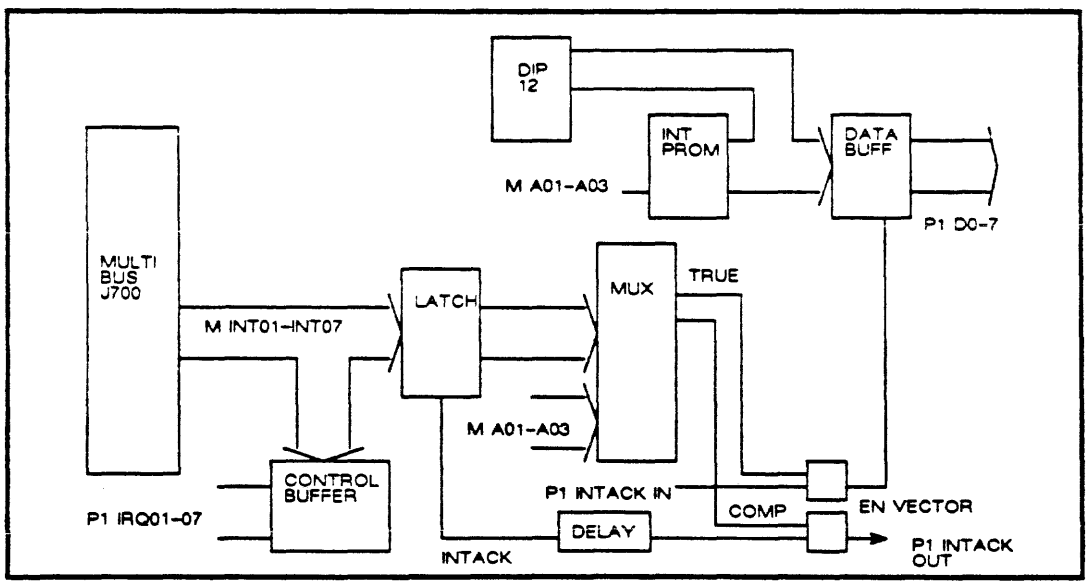


FIGURE 7C-5: INTERRUPT LOGIC

7C.7 VME DMA CYCLE

The adapter board can generate a VME DMA cycle (when the adapter is the VME bus master) in response to a DMA cycle by the Multibus board. The

Multibus board can be a 20-bit address master, or a 24-bit address master (the adapter board is a 24-bit master). If the Multibus board becomes a 24-bit master, the 4-high order bits are generated by the switches on the adapter board which are in DIP 11. DIP 11 generates addresses A20-A23 toward the VME bus via the inverter address buffers.

7C.8 CLOCK LOGIC

For multibus boards which require an external bus clock and constant clock (that is most boards), the adapter provides for those clocks. The clocks originate at a 19.6608 MHz crystal (X1) and is divided down by a flip-flop to provide a 9.8344 MHz clock. A jumper block on the adapter board (J1) allows the enabling/disabling of the bus clock and the constant clock. Pins 1 to 2 should be jumpered for the bus clock, and pins 3 to 4 should be jumpered for the constant clock. Note that the jumpers should be installed to provide the clocks. Refer to the block diagram in Figure 7C-6 for an illustration of these settings.

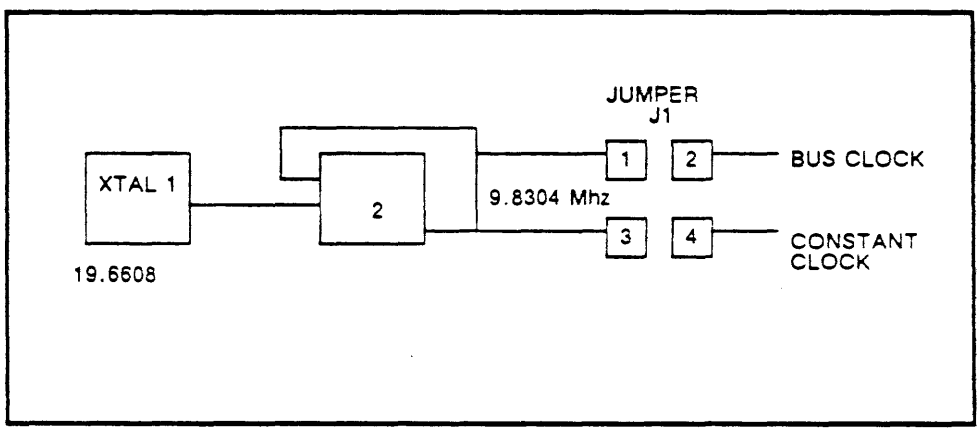


FIGURE 7C-6: CLOCK LOGIC

The next two blocks illustrate the layout of the VME/MB adapter:

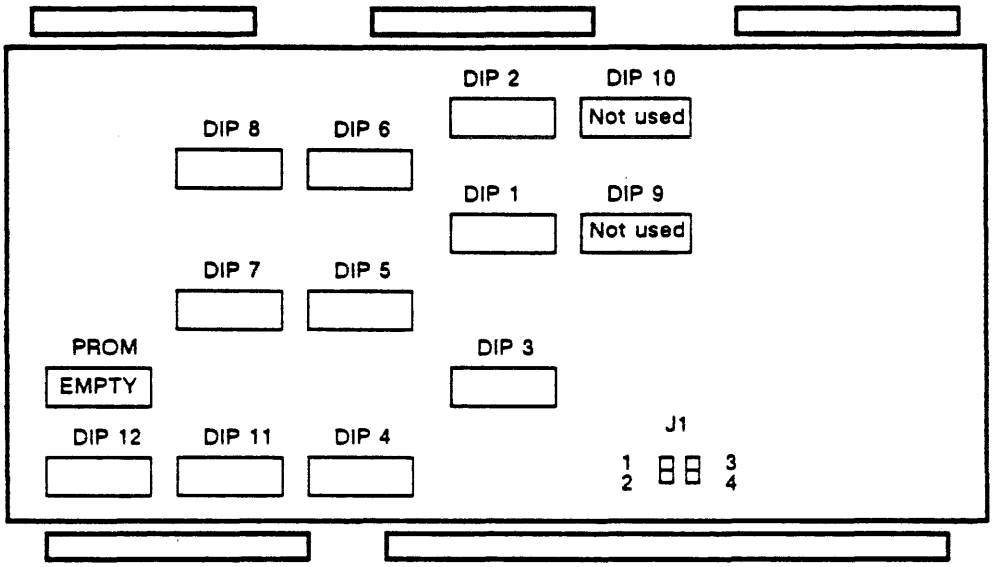


FIGURE 7C-15: VME/MB CARD LAYOUT

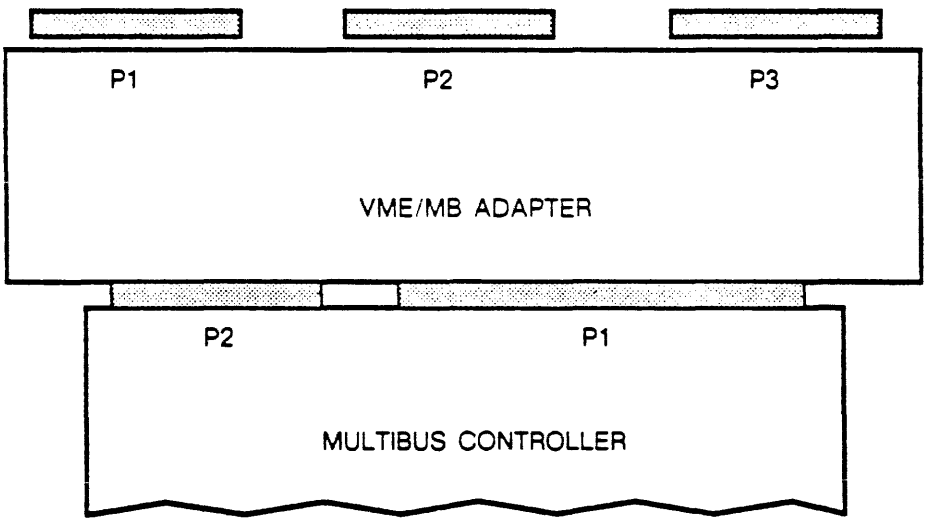


FIGURE 7C-16: VME/MB MOUNTING

7C.9 SUN 3 VME/MB ADAPTER SETTINGS

The following Tables list the default settings for Sun supported controller boards:

SWITCH	1	2	3	4	5	6	7	8	DESCRIPTION
1	ON	ON	OFF	ON	ON	ON	OFF	OFF	ADDR 0x40 I/O
2	OFF	ON	ON	ON	ON	ON	OFF	OFF	I/O space=8
3	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	ADDR 0xEE
4	ON	ON	ON	ON	ON	ON	ON	ON	I/O space=8
5	ON	ON	ON	ON	ON	ON	ON	ON	24-bit addr space
6	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24-bit bolck size
7	ON	ON	ON	ON	ON	ON	ON	ON	24-bin addr space
8	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24-bit block size
11	OFF	OFF	OFF	OFF	ON	ON	ON	ON	Set addr A23-A20
12	ON	ON	ON	OFF	ON	ON	OFF	ON	Int Vec at 0x48
J1	Install pins 1-2 for BCLK					Install pins 3-4 for CCLK			

FIGURE 7C-7: FIRST SMD CONTROLLER

SWITCH	1	2	3	4	5	6	7	8	DESCRIPTION
1	ON	ON	OFF	ON	ON	OFF	OFF	OFF	ADDR 0x48 I/0
2	OFF	ON	ON	ON	ON	ON	OFF	OFF	I/Ospace=8
3	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	ADDR 0xEE
4	ON	ON	ON	ON	ON	ON	ON	ON	VME addr space
5	ON	ON	ON	ON	ON	ON	ON	ON	24-bit addr space
6	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24-bit block size
7	ON	ON	ON	ON	ON	ON	ON	ON	24-bit addr space
8	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24-bit block size
11	OFF	OFF	OFF	OFF	ON	ON	ON	ON	Sets addr A23-A20
12	OFF	ON	ON	OFF	ON	ON	OFF	ON	Int Vec 0x49
J1	Install pins 1-2 for BCLK					Install pins 3-4 for CCLK			

FIGURE 7C-8: SECOND SMD CONTROLLER

SWITCH	1	2	3	4	5	6	7	8	DESCRIPTION
1	ON	ON	ON	ON	ON	ON	ON	ON	ADDR 0x00
2	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	No response to I/O spac
3	ON	ON	ON	ON	ON	ON	ON	ON	ADDR 0x00
4	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	No response to I/O spac
5	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24-bit addr space
6	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24-bit block size
7	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	24-bit addr space
8	ON	ON	ON	ON	OFF	OFF	OFF	OFF	24-bit block size
11	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	Sets addr A23-A20
12	OFF	on	off	on	OFF	off	off	ON	Int Vec 0x75
J1	Install pins 1-2 for BCLK					Install pins 3-4 for CCLK			

FIGURE 7C-9: SECOND ETHERNET BOARD

SWITCH	1	2	3	4	5	6	7	8	DESCRIPTION
1	ON	ON	ON	ON	ON	OFF	OFF	OFF	ADDR 0x800
2	ON	ON	ON	ON	ON	OFF	OFF	OFF	I/O space = 16
3	ON	ON	ON	ON	OFF	ON	ON	ON	ADDR 0x0800
4	ON	ON	ON	ON	ON	ON	ON	ON	VME addr space
5	ON	ON	ON	ON	ON	ON	ON	ON	24-bit addr space
6	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24-bit block
7	ON	ON	ON	ON	ON	ON	ON	ON	24-bit addr space
8	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24-bit block
11	OFF	OFF	OFF	OFF	ON	ON	ON	ON	Sets addr A23-A20
12	ON	ON	OFF	OFF	ON	ON	ON	OFF	Int Vec 0x8C
J1	Install pins 1-2 for BCLK					Install pins 3-4 for CCLK			

FIGURE 7C-10: SUNLINK CONTROLLER

SWITCH	1	2	3	4	5	6	7	8	DESCRIPTION
Dip 1	ON	ON	OFF	OFF	ON	***	OFF	OFF	Addr 0x60 I/O
Dip 2	OFF	ON	ON	ON	ON	ON	OFF	OFF	I/O space = 8 bytes
Dip 3	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	Addr 0xEE for I/O
DIP 4	ON	ON	ON	ON	ON	ON	ON	ON	I/O space = 8
Dip 5	ON	ON	ON	ON	ON	ON	ON	ON	24-bit addr space
Dip 6	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24-bit block size
Dip 7	ON	ON	ON	ON	ON	ON	ON	ON	
Dip 8	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
Dip 9	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	Not used
Dip 10	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	Not used
Dip 11	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	Set A23 to A20
Dip 12	***	ON	OFF	ON	ON	OFF	OFF	ON	Int vector set to 0x64
JUMPERS	Install pins 1-2 for BCLK					Install pins 3-4 for CCLK			
*** set ON for xtc0 , set OFF for xtc1									

FIGURE 7C-11: GCR 1/2-INCH TAPE CONTROLLER

SWITCH	1	2	3	4	5	6	7	8	DESCRIPTION
Dip 1	OFF	ON	ON	OFF	ON	ON	OFF	OFF	Addr 0x20 for I/O
Dip 2	OFF	ON	ON	ON	ON	ON	OFF	OFF	I/O space = 8
Dip 3	ON	ON	ON	ON	ON	OFF	OFF	ON	Addr 0x06 for I/O
Dip 4	ON	ON	ON	ON	ON	ON	ON	ON	I/O space = 8
Dip 5	ON	ON	ON	ON	ON	ON	ON	ON	VME 24-bit addr space
Dip 6	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24-bit block size
Dip 7	ON	ON	ON	ON	ON	ON	ON	ON	24-bit addr space
Dip 8	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	24-bit block size
Dip 9	---	---	---	---	---	---	---	---	Not Used
Dip 10	---	---	---	---	---	---	---	---	Not Used
Dip 11	OFF	OFF	OFF	OFF	ON	ON	ON	ON	Sets addr A23-A20
Dip 12	ON	ON	ON	OFF	ON	ON	ON	OFF	Int Vec at 0x88
JUMPERS	Install pins 1-2 for BCLK					Install pins 3-4 for CCLK			

FIGURE 7C-12: ALM INTERFACE CONTROLLER

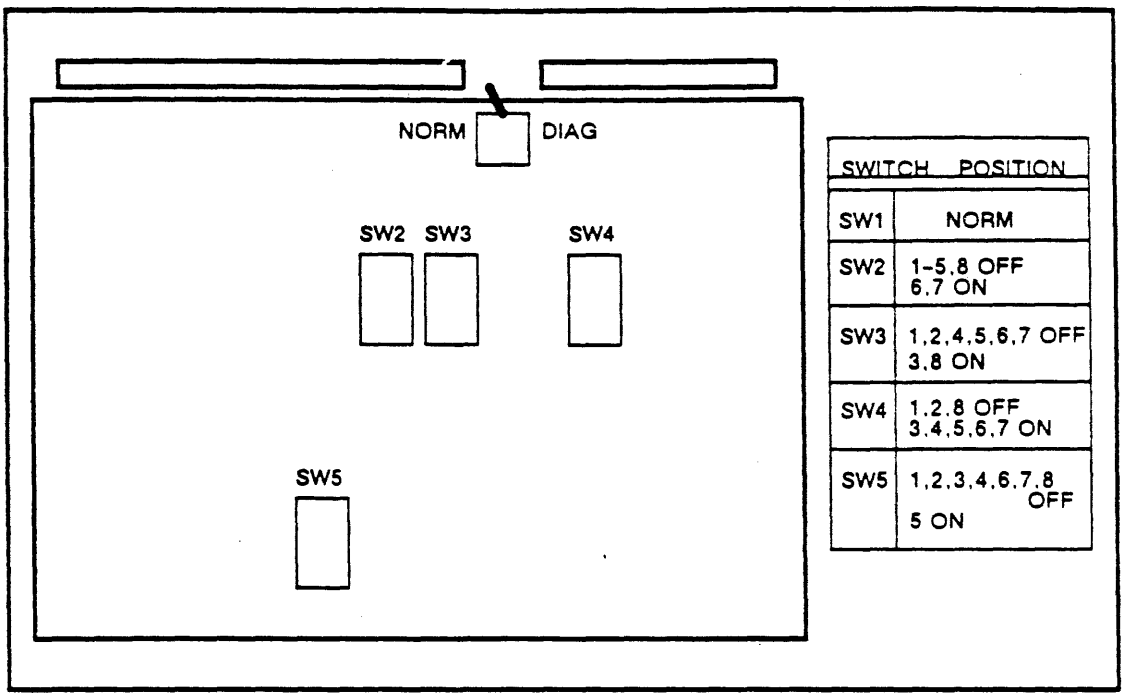


FIGURE 7C-13: ALM BOARD DIP SWITCH SETTINGS

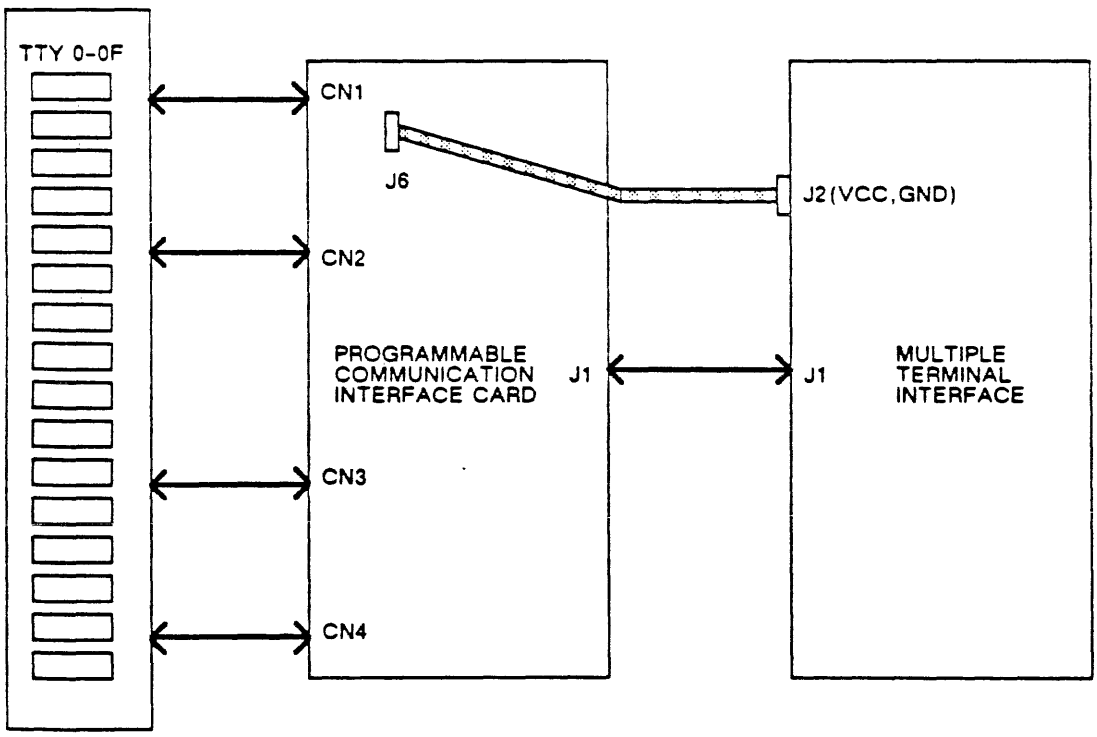
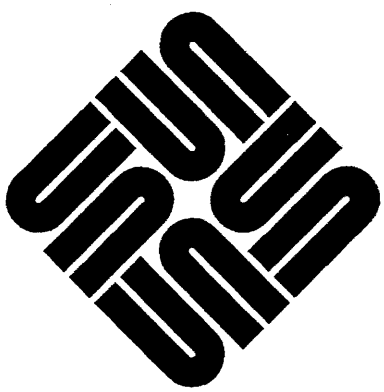


FIGURE 7C-14: PROGRAMMABLE COMMUNICATION INTERFACE (SECOND ALM BOARD)

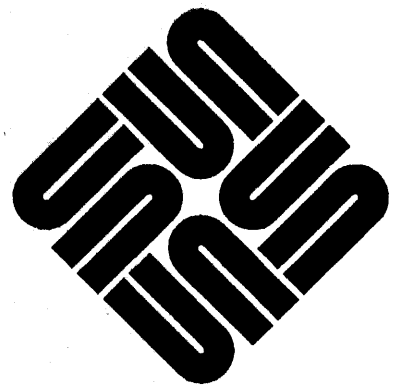
Programmable Parts

Not Available

At This Time

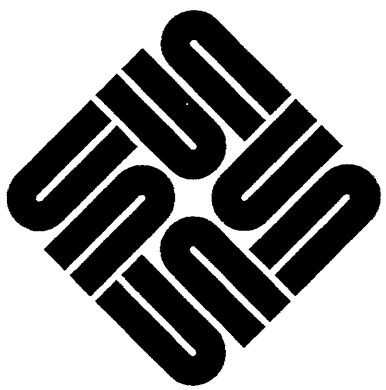


Spares Information



Not Available

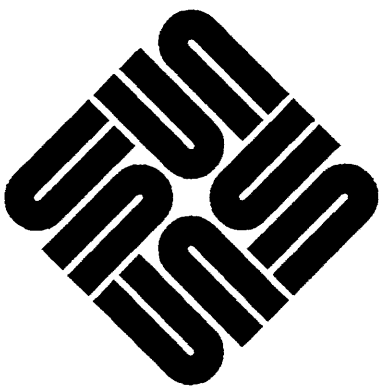
At This Time



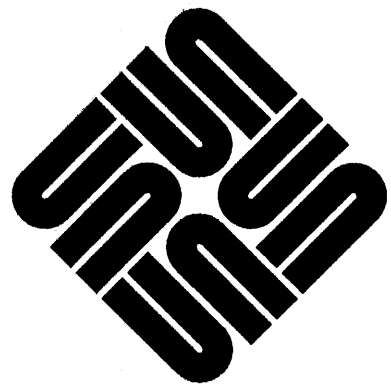
Bill Of Material (BOM)

Not Available

At This Time



Field Alerts



Not Available

At This Time

Engineering Change Orders

Not Available

At This Time

ECO Summary Sheets

SUMMARY SHEET

VME MULTIBUSS ADAPTER

501-1054 Rev. - 01/29/88

UPDATED PER ECO 3282 / DOCUMENTATION

NOTE: * REQUIRES DEPOT REWORK

ECO #	REV. OUT	EFFECTIVE DATE	CORRECTIVE ACTION
1463	03/50	03/20/85	DOCUMENTATION
1607	03/51	05/17/85	ENGINEERING RELEASE / DOCUMENTATION
*1609	03/51	05/17/85	ON FAB 270-1054-03 REWORK DIP SWITHES 1,2 &11. CUT PINS 1&2 FLUSH TO SWITCH BODY AND MOUNT PIN 2 OF SWITCH TO PIN 1 OF BOARD LOC. ON SOLDER SIDE JUMPER DIP12 PIN 8 TO DIP11 PINS 1,2,3,& 4.
1746	03/52	08/20/85	DOCUMENTATION
*1850	04/50	09/09/85	REMOVE P2 CONNECTOR
1725	04/A	09/30/85	PRODUCTION RELEASE
1993	04/B	11/05/85	ADDS BAR CODE LABELS
2080	04/C	12/10/85	DOCUMENTATION
2309	04/D	03/18/86	CHANGE IN BOM
2525	04/E	06/26/86	USE KEPTON TAPE (P/N 150-1180-01) ON BOARD SUPPORTS WHERE OPTION BOARDS REST.
*2189	N/A	06/19/86	SPRING FINGERS Problem: Add spring fingers to pass FCC Part 15.
*2748	05/A	11/06/86	ADD THICKER INSULATION (FR4) P/N 330-1099-01. ADD DOUBLE SIDED TAPE (P/N 150-1192-01) Problem: Make the spring finger insulator thicker to prevent the spring finger from shorting to the printed circuit board.
3018	05/B	03/10/87	DOCUMENTATION
3080	05/C	08/03/87	Add Bar Code tabs to BOM.

3267	05/D	06/30/87	U locations on the printed circuit board need to be standardized.
3014	05/E	10/12/87	Documentation
3282	05/F	10/08/87	Documentation

Purge Notice

P.N. # 649	06/02/87	PURGE DALE 10K SIP WITH DATE CODE 8649 (P/N 120-1419-01).

ECO Rework Sheets

ECO 1609

DATE APPROVED: 05/17/85

EFFECTIVE DATE: 05/17/85

PART NO. AFFECTED: 501-1054

ECO BOARD REV: FROM 03/50 TO 03/51

AVERAGE REWORK TIME: 15 min.

PARTS NEEDED:	DESCRIPTION	SUN PART NO.	QTY.
	8 Pin Dip Switch	150-1006-01	1

ADDITIONAL MATERIALS / TOOLS: 30 guage Kynar wire

REWORK INSTRUCTION FOR 1609:

1) Dip switched Dip1 and Dip2 cut off pins 1 and 16 flush with the Dip switch body.

2) Install the two Dip switched in to the positions marked on the printed circuit board maked Dip1 and Dip2 so that pin 2 of the switch goes into pin 1 on the board.

3) On the solder side of the board, jumper Dip11 pins 1,2,3, and 4 to pin 8 of Dip12.

4) Change the Printed Circuit Board revision level to a -03/51.

Comments: None

ECO 1850

DATE APPROVED: 09/09/85

EFFECTIVE DATE: 09/09/85

PART NO. AFFECTED: 501-1054

ECO BOARD REV: FROM 03/52 TO 04/50

AVERAGE REWORK TIME: 15 min.

PARTS NEEDED: None

ADDITIONAL MATERIALS / TOOLS: None

REWORK INSTRUCTIONS FOR ECO 1850:

1) Remove the P2 VME connector from the VME to Multibus adapter.

2) Change the Printed Circuit Board revision level to a -04/50.

Comments: None

ECO 2189

DATE APPROVED: 6/19/86

EFFECTIVE DATE: 6/19/86

PART NO. AFFECTED: 501-1054

ECO BOARD REV: FROM 01/C TO 02/A

AVERAGE REWORK TIME: 15 min.

PARTS NEEDED:	DESCRIPTION	SUN PART NO.	QTY.
	Spring finger	340-1228-03	1
	FR4 10 mil	330-1099-01	1
	Foam tape	150-1192-01	2
	Rivets 1/8 in.	240-1320-01	1

ADDITIONAL MATERIALS / TOOLS: Electric Hand Drill with a 1/8 inch bit
3/16 inch socket or nutdriver
Bostik POPRIVETOOL 1/8"-5/32"-3/16"
pop rivet tool or equivalent
Small screwdriver

REWORK INSTRUCTION FOR 2189:

1. Remove one of the pop rivets from the board stiffener with the electric hand drill.

2. Remove the screws and nuts that hold the connectors to the board stiffener with the screwdriver and 3/16" socket or nut driver.

3. Pull the board stiffener away from the printed circuit board and install the spring finger.

4. Place the insulator at the edge of the printed circuit board, near the board stiffener.

5. Place the board stiffener with the spring finger onto the printed circuit board and install the nuts and screws onto the connectors.
   * The springfinger should be resting on the FR4 insulator and not touching the printed circuit board.

6. Mark the revision level of the board with a -02/A.

COMMENTS: ECO 2748 requires the use of the FR4 10 mil insulator that has been installed with this rework instruction.

ECO 2748

DATE APPROVED: 11/06/86

EFFECTIVE DATE: 11/06/86

PART NO. AFFECTED: 501-1054

ECO BOARD REV: FROM 04/E to 05/A

AVERAGE REWORK TIME: 15 Min.

PARTS NEEDED:	DESCRIPTION	SUN PART NO.	QTY.
	FR4 10 mil	330-1099-01	1
	Foam tape	150-1192-01	2

ADDITIONAL MATERIALS / TOOLS: None

REWORK INSTRUCTION FOR ECO 2748:

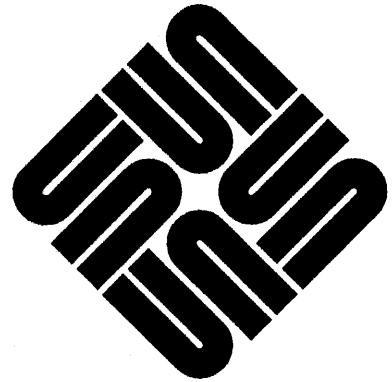
1. Remove any insulator under the springfinger except the FR4 10 mil insulator.

2. Install a FR4 10 mil insulator under the springfinger held in place by the 2 pieces of foam tape at each end of the insulator.

3. Mark the revision level of the board to a -05/A.

COMMENTS: None

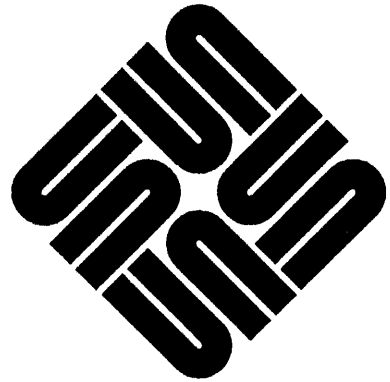
Tech Tips



Not Available

At This Time

Miscellaneous



Not Available

At This Time

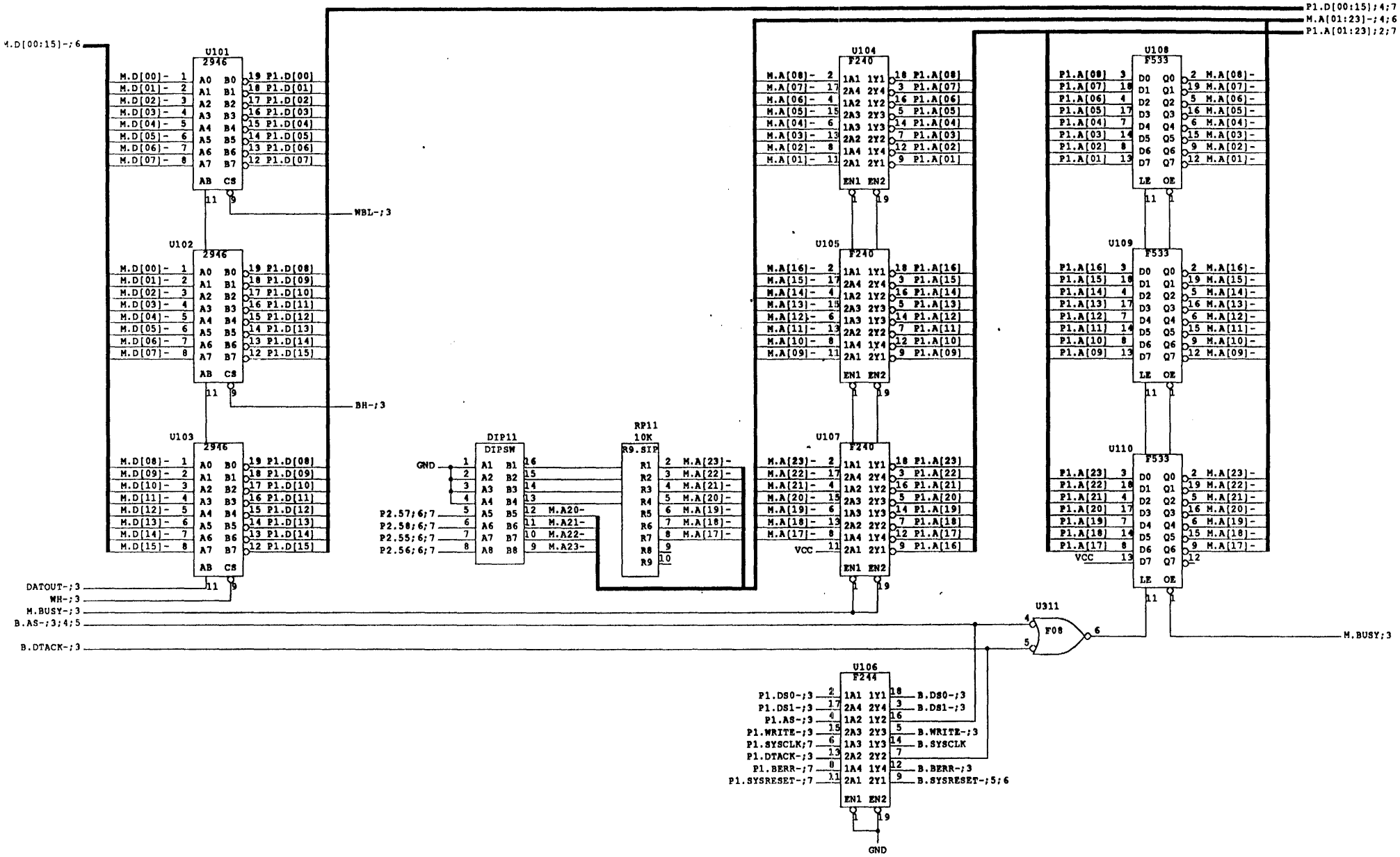
Schematics

VME TO MULTIBUS ADPT.

501-1054-05

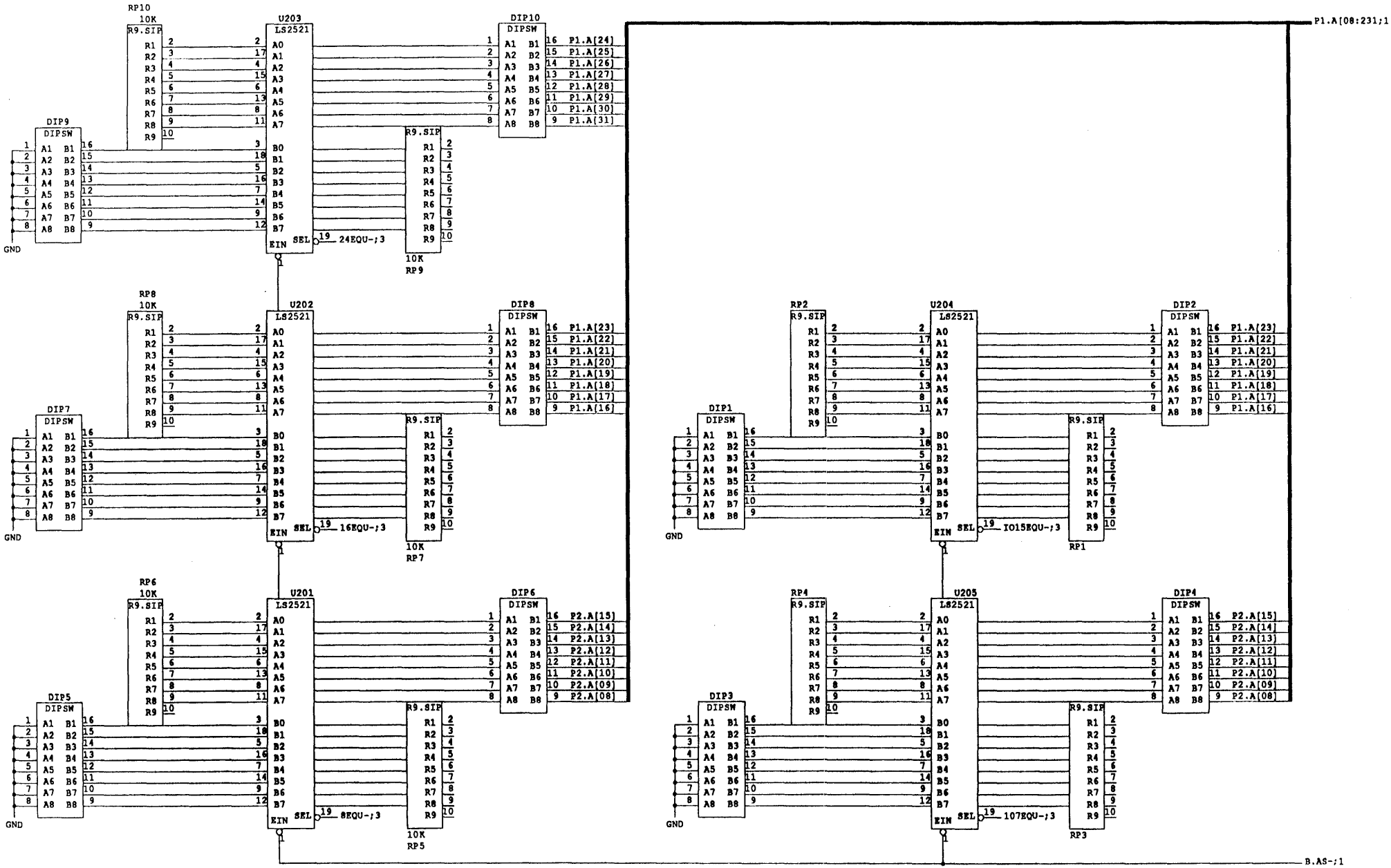
Rev B

ECO	Description	Date	Approvals
XXXX		6/19/87	



Title:	VME MULTIBUS ADAPTER MOD 160	Drawing:	501-1054-05 Rev: B
Sheet:	1	File:	sh1.d
Engineer:		Date:	Thu Oct 13 11:26:33 1988

ECO	Description	Date	Approvals



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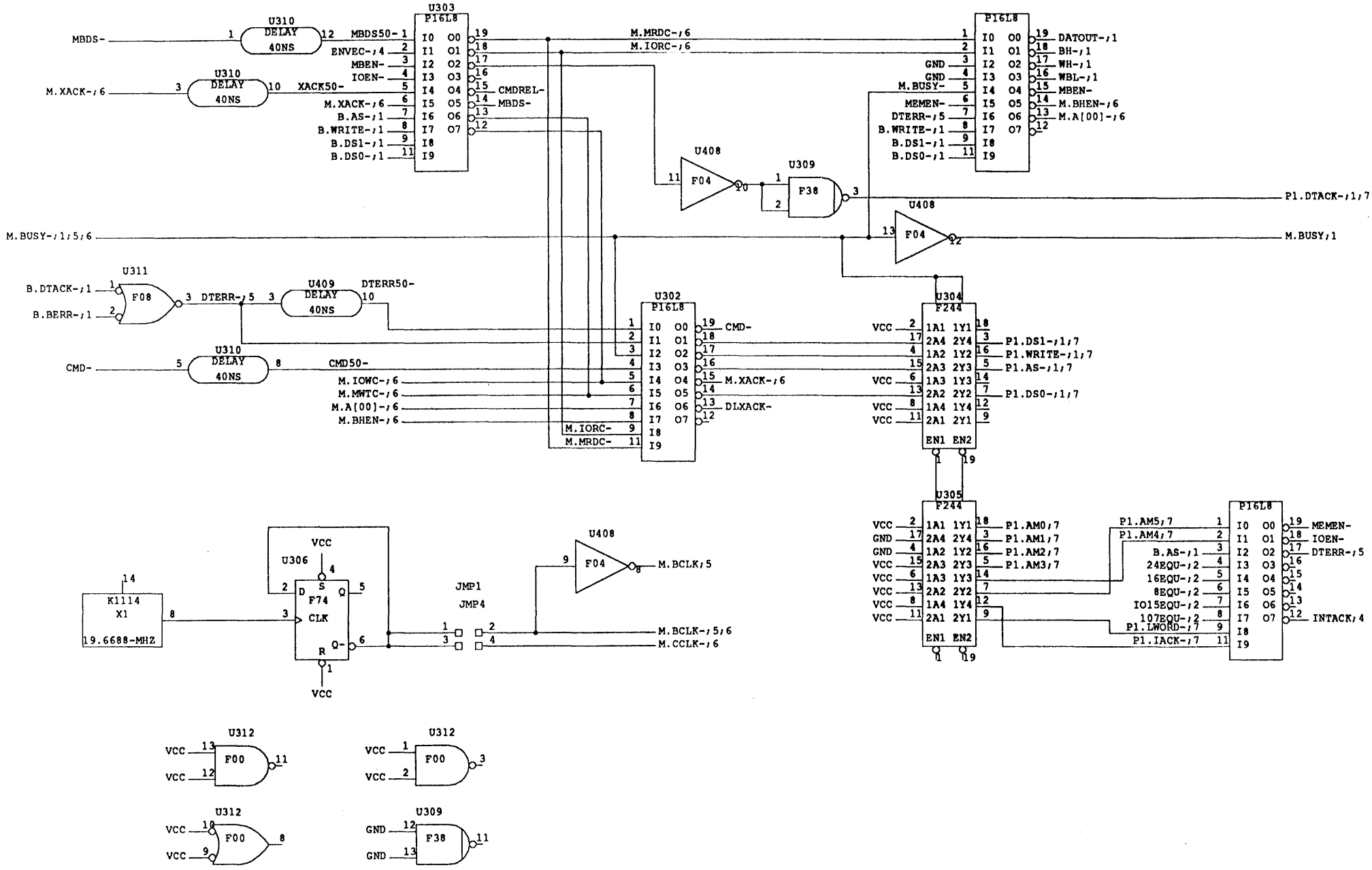
Sheet:	2	File:	sh2.d
Engineer:		Date:	Thu Oct 13 11:27:00 1988

ECO	Description	Date	Approvals



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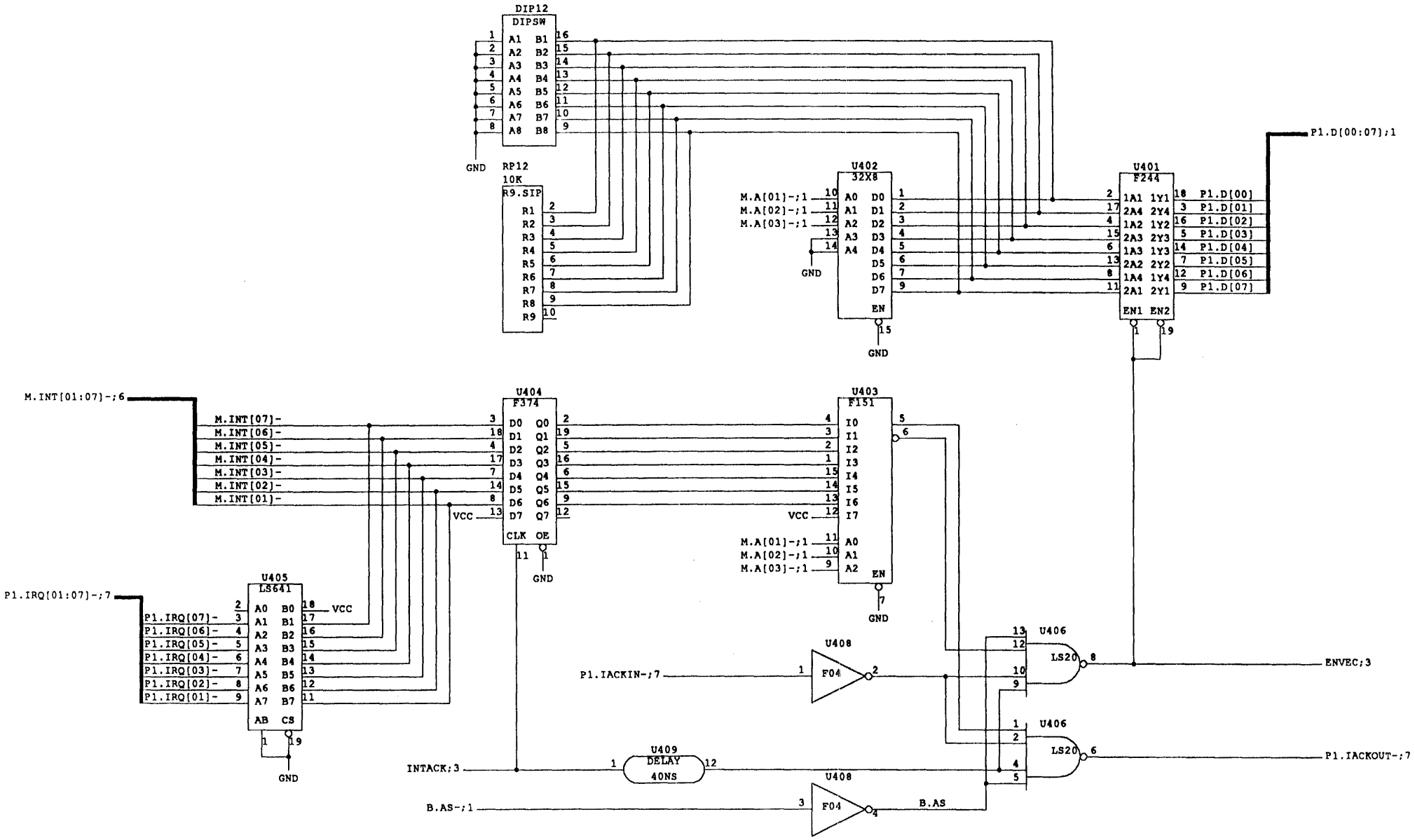
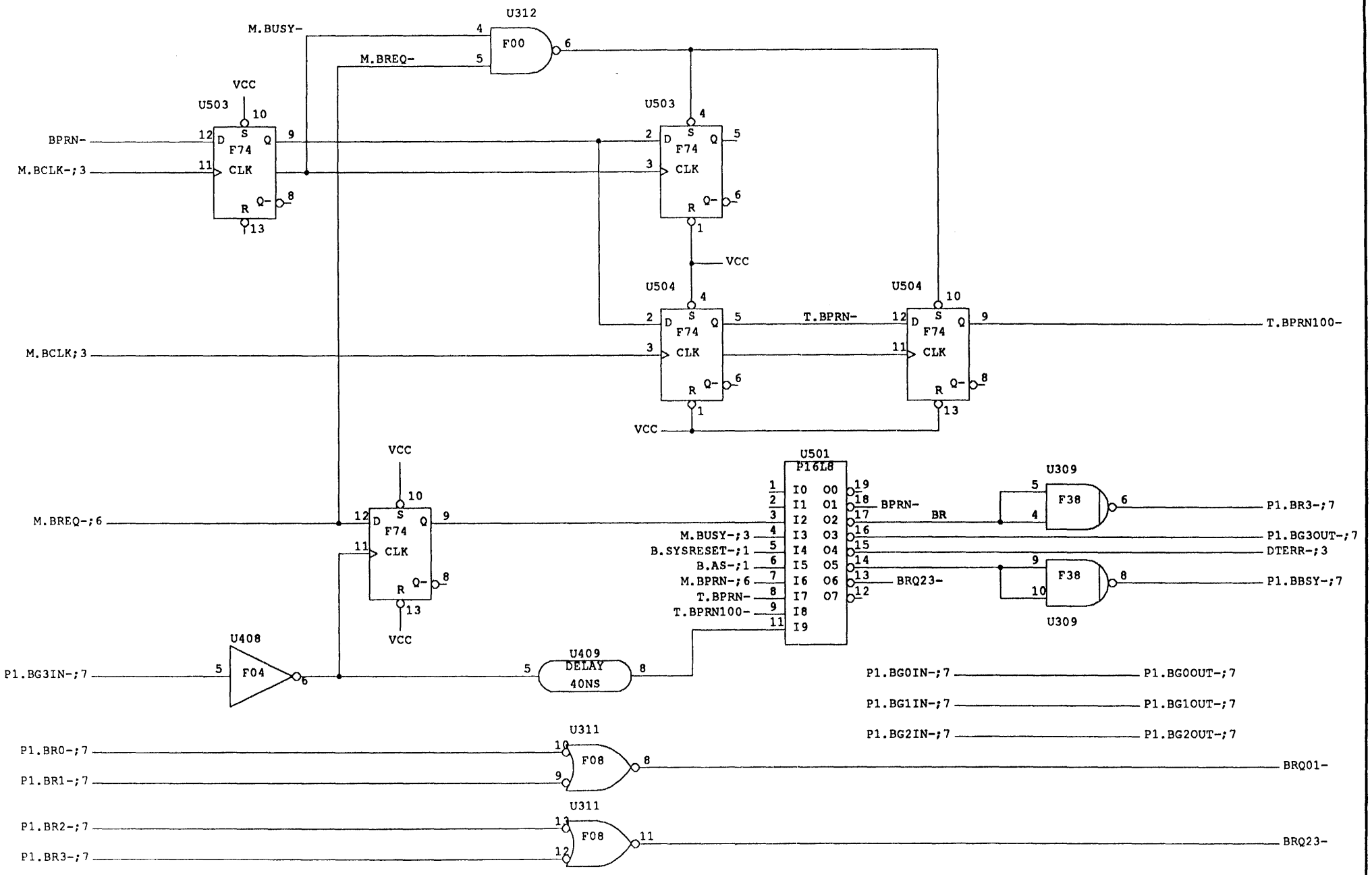
Sheet:	3	File:	sh3.d
Engineer:		Date:	Thu Oct 13 11:27:24 1988

ECO	Description	Date	Approvals



Title:	VME MULTIBUS ADAPTER MOD 160	Drawing:	501-1054-05 Rev: B
Sheet:	4	File:	sh4.d
Engineer:		Date:	Thu Oct 13 11:27:48 1988

ECO	Description	Date	Approvals



Title:	VME MULTIBUS ADAPTER MOD 160	Drawing: 501-1054-05	Rev: B
Sheet:	5	File:	sh5.d
Engineer:		Date:	Thu Oct 13 11:28:09 1988

ECO	Description	Date	Approvals

RP13
1K
R9.SIP

R1	2	M.INH2-
R2	3	M.INH1-
R3	4	M.IOWC-;3
R4	5	M.MWTC-;3
R5	6	M.BREQ-;5
R6	7	
R7	8	B.SYSRESET-;1
R8	9	
R9	10	

RP14
1K
M.INT[00:07]-;4
R9.SIP

R1	2	M.INTA-
R2	3	M.INT[07]-
R3	4	M.INT[06]-
R4	5	M.INT[05]-
R5	6	M.INT[04]-
R6	7	M.INT[03]-
R7	8	M.INT[02]-
R8	9	M.INT[01]-
R9	10	M.INT[00]-

RP15
1K
R9.SIP

R1	2	
R2	3	M.CBRQ-
R3	4	M.LOCK
R4	5	M.XACK-;3
R5	6	M.IORC-;3
R6	7	M.MRDC-;3
R7	8	M.BUSY-;3
R8	9	
R9	10	

RP16
2.2K
R9.SIP

R1	2	M.D[01]-;1
R2	3	M.D[03]-;1
R3	4	M.D[05]-;1
R4	5	M.D[07]-;1
R5	6	M.D[09]-;1
R6	7	M.D[11]-;1
R7	8	M.D[13]-;1
R8	9	M.D[15]-;1
R9	10	

RP17
2.2K
R9.SIP

R1	2	M.D[00]-;1
R2	3	M.D[02]-;1
R3	4	M.D[04]-;1
R4	5	M.D[06]-;1
R5	6	M.D[08]-;1
R6	7	M.D[10]-;1
R7	8	M.D[12]-;1
R8	9	M.D[14]-;1
R9	10	

RP18
2.2K
R9.SIP

R1	2	M.A[00]-;1
R2	3	M.A[02]-;1
R3	4	M.A[04]-;1
R4	5	M.A[06]-;1
R5	6	M.A[08]-;1
R6	7	M.A[10]-;1
R7	8	M.A[12]-;1
R8	9	M.A[14]-;1
R9	10	

RP19
2.2K
R9.SIP

R1	2	M.A[01]-;1
R2	3	M.A[03]-;1
R3	4	M.A[05]-;1
R4	5	M.A[07]-;1
R5	6	M.A[09]-;1
R6	7	M.A[11]-;1
R7	8	M.A[13]-;1
R8	9	M.A[15]-;1
R9	10	

RP20
2.2K
R9.SIP

R1	2	M.A[16]-;1
R2	3	M.A[17]-;1
R3	4	M.A[18]-;1
R4	5	M.A[19]-;1
R5	6	M.A[20]-;1
R6	7	M.A[21]-;1
R7	8	M.A[22]-;1
R8	9	M.A[23]-;1
R9	10	M.BHEN-;3

RP21
1K
R9.SIP

R1	2	P2.17;7
R2	3	P2.18;7
R3	4	P2.19;7
R4	5	P2.20;7
R5	6	P2.13;7
R6	7	
R7	8	
R8	9	
R9	10	

J700
D86

GND	1	2	GND
VCC	3	4	VCC
VCC	5	6	VCC
+12V	7	8	+12V
-5V	9	10	-5V
GND	11	12	GND
M.BCLK-;3	13	14	B.SYSRESET-;1
M.BPRN-;5	15	16	M.BPRO-
M.BUSY-;3	17	18	M.BREQ-;5
M.MRDC-;3	19	20	M.MWTC-;3
M.IORC-;3	21	22	M.IOWC-;3
M.XACK-;3	23	24	M.INH1-
M.LOCK-	25	26	M.INH2-
M.BHEN-;3	27	28	M.A16-;1
M.CBRQ-	29	30	M.A17-;1
M.CCLK-;3	31	32	M.A18-;1
M.INTA-	33	34	M.A19-;1
M.INT06-;4	35	36	M.INT07-;4
M.INT04-;4	37	38	M.INT05-;4
M.INT02-;4	39	40	M.INT03-;4
M.INT00-;4	41	42	M.INT01-;4
M.A[14]-;1	43	44	M.A[15]-;1
M.A[12]-;1	45	46	M.A[13]-;1
M.A[10]-;1	47	48	M.A[11]-;1
M.A[08]-;1	49	50	M.A[09]-;1
M.A[06]-;1	51	52	M.A[07]-;1
M.A[04]-;1	53	54	M.A[05]-;1
M.A[02]-;1	55	56	M.A[03]-;1
M.A[00]-;1	57	58	M.A[01]-;1
M.D[14]-;1	59	60	M.D[15]-;1
M.D[12]-;1	61	62	M.D[13]-;1
M.D[10]-;1	63	64	M.D[11]-;1
M.D[08]-;1	65	66	M.D[09]-;1
M.D[06]-;1	67	68	M.D[07]-;1
M.D[04]-;1	69	70	M.D[05]-;1
M.D[02]-;1	71	72	M.D[03]-;1
M.D[00]-;1	73	74	M.D[01]-;1
GND	75	76	GND
	77	78	
-12V	79	80	-12V
VCC	81	82	VCC
VCC	83	84	VCC
GND	85	86	GND

J701
D60

P2.1;7	1	2	P2.2;7
P2.3;7	3	4	P2.4;7
P2.5;7	5	6	P2.6;7
P2.7;7	7	8	P2.8;7
P2.9;7	9	10	P2.10;7
P2.11;7	11	12	P2.12;7
P2.13;7	13	14	P2.14;7
P2.15;7	15	16	P2.16;7
P2.17;7	17	18	P2.18;7
P2.19;7	19	20	P2.20;7
P2.21;7	21	22	P2.22;7
P2.23;7	23	24	P2.24;7
P2.25;7	25	26	P2.26;7
P2.27;7	27	28	P2.28;7
P2.29;7	29	30	P2.30;7
P2.31;7	31	32	P2.32;7
P2.33;7	33	34	P2.34;7
P2.35;7	35	36	P2.36;7
P2.37;7	37	38	P2.38;7
P2.39;7	39	40	P2.40;7
P2.41;7	41	42	P2.42;7
P2.43;7	43	44	P2.44;7
P2.45;7	45	46	P2.46;7
P2.47;7	47	48	P2.48;7
P2.49;7	49	50	P2.50;7
P2.51;7	51	52	P2.52;7
P2.53;7	53	54	P2.54;7
P2.55;7	55	56	P2.56;7
P2.57;7	57	58	P2.58;7
P2.59;7	59	60	P2.60;7

Title:	VME MULTIBUS ADAPTER MOD 160	Drawing:	501-1054-05 Rev: B
Sheet:	6	File:	sh6.d
Engineer:		Date:	Thu Oct 13 11:28:32 1988

ECO	Description	Date	Approvals

J800

DIN CONNECTOR

1	P2.2;6	33	VCC	65	P2.1;6
2	P2.4;6	34	GND	66	P2.3;6
3	P2.6;6	35		67	P2.5;6
4	P2.8;6	36	P1.A[24];2	68	P2.7;6
5	P2.10;6	37	P1.A[25];2	69	P2.9;6
6	P2.12;6	38	P1.A[26];2	70	P2.11;6
7	P2.14;6	39	P1.A[27];2	71	P2.13;6
8	P2.16;6	40	P1.A[28];2	72	P2.15;6
9	P2.18;6	41	P1.A[29];2	73	P2.17;6
10	P2.20;6	42	P1.A[30];2	74	P2.19;6
11	P2.22;6	43	P1.A[31];2	75	P2.21;6
12	P2.24;6	44	GND	76	P2.23;6
13	P2.26;6	45	VCC	77	P2.25;6
14	P2.28;6	46	P1.D[16];1	78	P2.27;6
15	P2.30;6	47	P1.D[17];1	79	P2.29;6
16	P2.32;6	48	P1.D[18];1	80	P2.31;6
17	P2.34;6	49	P1.D[19];1	81	P2.33;6
18	P2.36;6	50	P1.D[20];1	82	P2.35;6
19	P2.38;6	51	P1.D[21];1	83	P2.37;6
20	P2.40;6	52	P1.D[22];1	84	P2.39;6
21	P2.42;6	53	P1.D[23];1	85	P2.43;6
22	P2.44;6	54	GND	86	P2.45;6
23	P2.46;6	55	P1.D[24];1	87	P2.47;6
24	P2.48;6	56	P1.D[25];1	88	P2.49;6
25	P2.50;6	57	P1.D[26];1	89	P2.51;6
26	P2.52;6	58	P1.D[27];1	90	P2.53;6
27	P2.54;6	59	P1.D[28];1	91	P2.55;1;6
28	P2.56;1;6	60	P1.D[29];1	92	P2.57;1;6
29	P2.58;1;6	61	P1.D[30];1	93	P2.59;6
30	P2.60;6	62	P1.D[31];1	94	
31		63	GND	95	
32		64	VCC	96	

J801

DIN CONNECTOR

1	P1.D[00];1	33	P1.BBSY-;5	65	P1.D[08];1
2	P1.D[01];1	34	P1.BCLR-	66	P1.D[09];1
3	P1.D[02];1	35	P1.ACFAIL-	67	P1.D[10];1
4	P1.D[03];1	36	P1.BG0IN-;5	68	P1.D[11];1
5	P1.D[04];1	37	P1.BG0OUT-;5	69	P1.D[12];1
6	P1.D[05];1	38	P1.BG1IN-;5	70	P1.D[13];1
7	P1.D[06];1	39	P1.BG1OUT-;5	71	P1.D[14];1
8	P1.D[07];1	40	P1.BG2IN-;5	72	P1.D[15];1
9	GND	41	P1.BG2OUT-;5	73	GND
10	P1.SYSCLK;1	42	P1.BG3IN-;5	74	P1.SYSFAIL-
11	GND	43	P1.BG3OUT-;5	75	P1.BERR-;1
12	P1.DS1-;3	44	P1.BR0-;5	76	P1.SYSRESET-;1
13	P1.DS0-;3	45	P1.BR1-;5	77	P1.LWORD-;3
14	P1.WRITE-;3	46	P1.BR2-;5	78	P1.AM5;3
15	GND	47	P1.BR3-;5	79	P1.A[23];2
16	P1.DTACK-;3	48	P1.AM0;3	80	P1.A[22];2
17	GND	49	P1.AM1;3	81	P1.A[21];2
18	P1.AS-;3	50	P1.AM2;3	82	P1.A[20];2
19	GND	51	P1.AM3;3	83	P1.A[19];2
20	P1.IACK-;3	52	GND	84	P1.A[18];2
21	P1.IACKIN-;4	53	P1.SERCLK;1	85	P1.A[17];2
22	P1.IACKOUT-;4	54	P1.SERDAT	86	P1.A[16];2
23	P1.AM4;3	55	GND	87	P1.A[15];2
24	P1.A[07];2	56	P1.IRQ[07]-;4	88	P1.A[14];2
25	P1.A[06];2	57	P1.IRQ[06]-;4	89	P1.A[13];2
26	P1.A[05];2	58	P1.IRQ[05]-;4	90	P1.A[12];2
27	P1.A[04];2	59	P1.IRQ[04]-;4	91	P1.A[11];2
28	P1.A[03];2	60	P1.IRQ[03]-;4	92	P1.A[10];2
29	P1.A[02];2	61	P1.IRQ[02]-;4	93	P1.A[09];2
30	P1.A[01];2	62	P1.IRQ[01]-;4	94	P1.A[08];2
31	-12V	63	+5VSTDBY	95	+12V
32	VCC	64	VCC	96	VCC

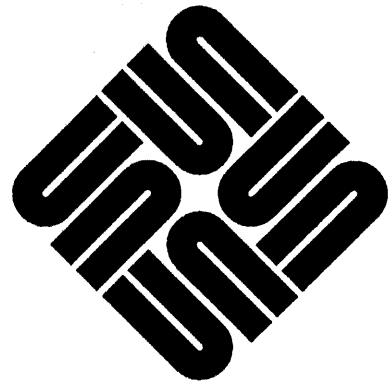
J802

DIN CONNECTOR

1	VCC	33		65	GND
2	VCC	34		66	GND
3	VCC	35		67	GND
4	VCC	36		68	GND
5	VCC	37		69	GND
6	VCC	38		70	GND
7	VCC	39		71	GND
8	VCC	40		72	GND
9	VCC	41		73	GND
10	VCC	42		74	GND
11	VCC	43		75	GND
12	VCC	44		76	GND
13	VCC	45		77	GND
14	VCC	46		78	GND
15	VCC	47		79	GND
16	VCC	48		80	GND
17	VCC	49		81	GND
18	VCC	50		82	GND
19	VCC	51		83	GND
20	VCC	52		84	GND
21	VCC	53		85	GND
22	VCC	54		86	GND
23	VCC	55		87	GND
24	VCC	56		88	GND
25	VCC	57		89	GND
26	+12V	58		90	+12V
27	+12V	59		91	+12V
28	-12V	60		92	-12V
29	-12V	61		93	-12V
30	-5V	62		94	-5V
31	-5V	63		95	-5V
32	-5V	64		96	-5V

Title:	VME MULTIBUS ADAPTER MOD 160	Drawing: 501-1054-05	Rev: B
Sheet:	7	File: sh7.d	
Engineer:		Date: Thu Oct 13 11:28:52 1988	

Mechanical & Assembly Drawings



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