TeleVideo® TS 1605/1605H Technical Reference

TeleVideo®
TS 1605/TS 1605H
Technical Reference

TeleVideo Systems, Inc., • 1170 Morse Avenue • P.O. Box 3568 • Sunnyvale, CA 94088 • (408) 745-7760

TeleVideo® Tele-PC and Tele-XT
Models TS 1605 and TS 1605H Technical Reference Manual

TeleVideo Part Number 123181-01 Rev. A
15 June 1984

Copyright

Disclaimer

TeleVideo Systems, Inc. reserves the right to make improvements to products without incurring any obligations to incorporate such improvements in products previously sold. Specifications and information contained in this manual are subject to change without notice.

Material describing applications of components supplied by independent vendors such as Intel, Synertek, and Western Digital have been based in large part upon handbooks, technical manuals, and similar information distributed by such vendors. For a complete description of those parts and the ways in which they may be used, reference should be had to vendors' texts, which will be more complete.

TeleVideo Systems, Inc., 1170 Morse Avenue, P.O. Box 3568, Sunnyvale, CA 94088

COMPUTER SYSTEMS DIVISION BUYER'S LIMITED WARRANTY

TeleVideo Systems, Inc. ("TeleVideo") warrants to Buyer that its products, except software, will be free from defects in materials and workmanship for 90 calendar days after date of sale. TeleVideo's obligations under this warranty will be limited to repairing or replacing, at TeleVideo's option, the part or parts of the products which prove defective in material or workmanship, provided that Buyer gives TeleVideo prompt notice of any defect and satisfactory proof thereof.

If service is required under this warranty, Customer must return the product to an Authorized TeleVideo Dealer or the original Dealer from which the unit was purchased. With respect to any product or part thereof not manufactured by TeleVideo, only the warranty, if any, given by the manufacturer thereof will apply.

EXCLUSIONS

All statements, technical information, and recommendations in this document and in any manuals or related documents are believed to be reliable, but the accuracy or completeness thereof is not guaranteed.

This limited warranty does not cover losses or damage which occurs in shipment to or from Buyer, or is due to (1) improper installation or maintenance, misuse, neglect, or any cause other than ordinary commercial or industrial application or (2) adjustment, repair, or modifications by other than TeleVideo authorized personnel or (3) improper environment, excessive or inadequate heating or air conditioning, and electrical power failures, surges, or other irregularities or (4) any statements made about TeleVideo's products by salesmen, dealers, distributors, or agents unless confirmed in writing by a TeleVideo officer.

The foregoing TeleVideo limited warranty is in lieu of all other warranties, whether oral, written, express, implied, or statutory. Implied warranties or merchantability and fitness for a particular purpose will not apply. TeleVideo's warranty obligations and buyer's remedies hereunder are solely and exculsively as stated herein. TeleVideo makes no warranty whatsoever concerning any software products, which are sold "as is" and "with all faults."

TeleVideo's liability, whether based on contract, tort, warranty, strict liability, or any other theory, shall not exceed the price of the individual unit whose defect or damage is the basis of the claim. In no event shall TeleVideo be liable for any loss of profits, loss of use of facilities or equipment, or other indirect, incidental, or consequential damages.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. INTRODUCTION

The TeleVideo TS 1605 and TS 1605H computer systems are based on the Intel 8088 microprocessor, using the same circuit board in different configurations. The 8088 microprocessor is an 8-bit external, 16-bit internal device with a 20-bit address bus.

The TS 1605 is an integrated stand-alone system with two slim line floppy disk drives. The vertically-mounted floppy disk drives are 48 TPI drives with a formatted storage of 360 kilobytes per drive.

The system board contains an RS-232 serial I/O port, configured for asynchronous communication. An IBM-compatible parallel I/O port is configured for a parallel printer or other general communications device. Keyboard I/O is handled by a programmable peripheral interface device. An IBM-type I/O channel can interface with any I/O devices not on the system board.

The TS 1605H is similar to the TS 1605, except that it features a 3 1/2-inch 10 megabyte Winchester hard disk drive and a single floppy disk drive. The controller for the Winchester drive is contained on a separate board.

Standard main memory for the TS 1605 is 128 kilobytes, expandable to 256 kilobytes with an expansion board or added memory chips. Standard main memory for the TS 1605H is 256 kilobytes. An 8-kilobyte system ROM device is used for system power-on self-test, disk drive bootstrap loader, and input/output drivers.

The color/graphics monitor interface, capable of operating in black and white or color, is designed around the Synertek 6845R CRT controller. Graphics memory uses 16 kilobytes of static RAM. Resolution is 640 pixels horizontal by 200 pixels vertical for the monochrome graphics display and 320 pixels by 200 pixels for the color graphics display. The alphanumeric display is 25 lines by 80 columns of characters, featuring hidden attributes for the monochrome display, and eight background colors and sixteen foreground colors for the color display.

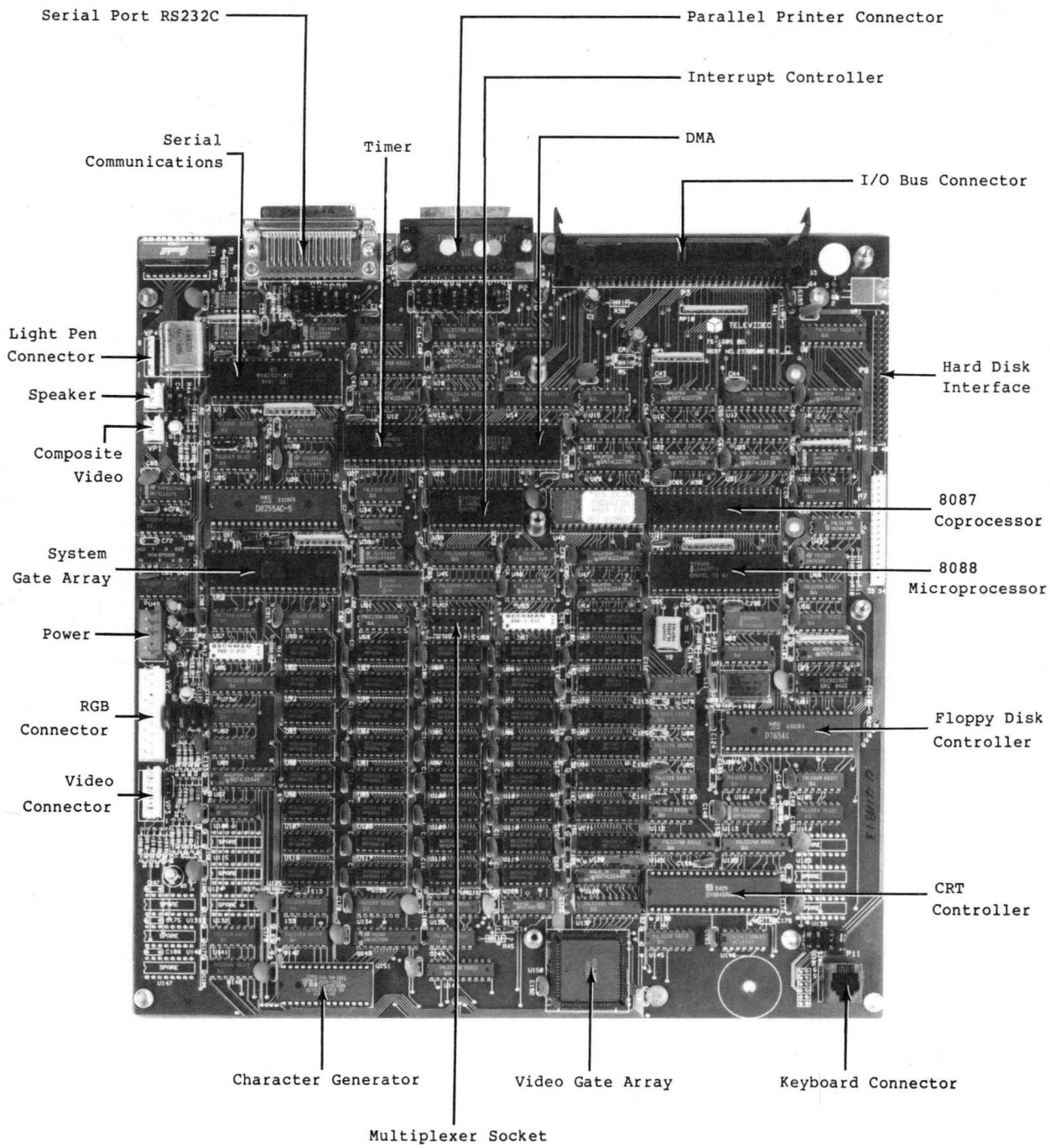
The TS 1605 and TS 1605H use an IBM-style keyboard and standard TeleVideo video driver circuits.

See Appendix A for a list of suggested technical references that include more information about the TS 1605 and the TS 1605H.

2. FUNCTIONAL DESCRIPTION

The TS 1605 and TS 1605H are single-board systems (see Figure 2-1). The TS 1605H has interface circuitry for a Winchester hard disk controller board.

Figure 2-1
TS 1605 System Board



SYSTEM BOARD

The system board contains circuits for control and video processing functions. An Intel 8088 8-bit HMOS microprocessor device performs logical and computational functions of the running software, handles graphics processing, and updates video memory.

Arithmetic and comparison operations can be handled with the addition of an optional Intel 8087 Numeric Data Processor. The CPU and numeric data processor operate at a frequency of 4.77 MHz, which is divided down from a 14.31818-MHz crystal through an Intel 8284A Clock Generator.

An Intel 8237A-5 DMA controller device allows external devices to transfer information directly to or from system memory. The DMA provides four channels of 16-bit address space. Twenty bits of address space can be obtained by programming a hardware latch for the highest four bits of address. One DMA channel is used to refresh dynamic memory. The three remaining DMA channels are used for data transfers of the floppy disk, hard disk, and I/O channel.

All necessary signals for dynamic memory reads and writes are generated by the TeleVideo Memory Control Gate Array. The memory control gate array works together with an Intel 8288 Bus Controller to control timing when the DMA uses the buses.

An Intel 8259A Interrupt Controller provides eight prioritized levels of interrupt for the system.

Main memory is configured in 64K x 1 dynamic RAM chips with a minimum data access time of 150-200 nanoseconds. Standard main memory capacity is 128 Kbytes of dynamic RAM for the TS 1605 and 256 Kbytes for the TS 1605H. Main memory can be expanded in three ways:

* Up to 256 Kbytes on the TS 1605 by adding 64K x 1 RAM chips into the existing sockets on the system board.

* Up to 512 Kbytes by replacing the 64K x 1 RAM chips with 256K x 1 RAM chips (64K chips cannot be mixed with 256K chips). This requires installing a multiplexer 74LS158 chip into the existing socket on the system board (see the Multiplexer Socket in Figure 2-1).

* Up to 640 Kbytes by connecting an expansion board via a 64-pin ribbon cable to the expansion slot on the system board (see the I/O Bus Connector in Figure 2-1). Before connecting the expansion board, all 64K x 1 RAM chips must be installed on the system board.

Read-only memory is configured in a single 8-Kbyte ROM chip. This memory contains codes for system boot and power-up diagnostics. Graphics memory has 16 kilobytes of static RAM. The I/O ports are decoded with two devices. I/O port decoder #1 enables the programmable interrupt controller, programmable DMA controller, programmable interval timer, and programmable peripheral interface. I/O decoder #2, a read-only device, enables the floppy disk controller, serial I/O port, parallel I/O port, and Winchester disk controller board.

A list of I/O port addresses is contained in Table 2-1 and Appendix B. The I/O port decoders are addressed on lines XA5 through XA8 and A2 through A9. The decoder enables, along with the internal I/O device registers, configure the system and pass data to system peripheral devices.

Table 2-1
I/O Port Addresses

Device			Address
DMA			%000-%00F
	Channel 0	DMA refresh	
	Channel 1	I/O channel	
	Channel 2	FDC data transfer or I/O channel	
	Channel 3	Hard disk transfer or I/O channel	
Programmable Interrupt Controller			%020-%021
Programmable Interval Timer			%040-%043
	Channel 0	Time of day	%040
	Channel 1	Dynamic RAM refresh	%041
	Channel 3	Audio speaker tone	%042
	Command Register		%043
Programmable Peripheral Interface			%060-%063
	PA (Input)	Keyboard scan code	%060
	PB (Output)	PB0 Speaker gate	%061
		PB1 Speaker data	
		PB2 Spare	
		PB3 Read switch high/low bits	
		PB4 Spare	
		PB5 Enable I/O channel check	
		PB6 Force keyboard clock low	
		PB7 Clear keyboard	
	PC (Input)	PC0 SW1	%062
		PC1 SW2	
		PC2 SW3	
		PC3 SW4	
		PC4 Speaker data	
		PC5 Timer channel 2 output	
		PC6 I/O channel check	
		PC7 Always low	
	Command/Mode Register (set to %99)		%063

DMA Page Register	%080-%083
NMI Mask Register	%0A0
To enable NMI, write data %80 into address %0A0	
To disable NMI, write data %00 into address %0A0	
Serial Port (Primary)	%3F8-%3FF
Tx Buffer/Rx Buffer/ Divisor Latch LSB	%3F8
Interrupt Enable/Divisor Latch MSB	%3F9
Interrupt Identification Register	%3FA
Line Control Register	%3FB
Modem Control Register	%3FC
Line Status Register	%3FD
Modem Status Register	%3FE
Floppy Disk Control Port	%3F2
Select drive A	D0 = 0
Select drive B	D0 = 1
Reset 8272A FDC	D2 = 0
Disable interrupt/DMA operation	D3 = 0
Enable interrupt/DMA operation	D3 = 1
Turn on both motors	D4 = 1 or D5 = 1
Floppy Disk Controller	%3F4-%3F5
FDC Main Status Register	%3F4
FDC Data Register	%3F5
Parallel Data Port (Read/write)	%3BC
Parallel Control Port (Read/write)	%3BE
STROBE (-)	D0
AUTO FD XT	D1
INIT (-)	D2
SLCT IN (-)	D3
INTERRUPT ENABLE	D4
Parallel Status Port (Read only)	%3BD
ERROR (-)	D3
SLCT	D4
PE	D5
ACK (-)	D6
BUSY (-)	D7
Winchester Disk Control Register	%0E0
To enable interrupt:	D6 = 1
To disable interrupt:	D6 = 0
To enable DMA operation:	D7 = 1
To disable DMA operation:	D7 = 0

Winchester Disk Controller Board Task File Register		%330-337
Read Data	Write Data	%330
Error flag	Write precomp cylinder	%331
Sector count	Sector count	%332
Sector number	Sector number	%333
Cylinder low	Cylinder low	%334
Cylinder high	Cylinder high	%335
SDH	SDH	%336
Status register	Command register	%337

The serial I/O port is contained in a WD8250 serial I/O device as a general purpose, asynchronous RS-232 port. This device can be programmed for data rates of from 50 baud to 9600 baud. Current-loop operation is also supported in the serial port.

A general-purpose parallel I/O port provides a parallel printer interface. Interrupts are enabled or disabled by program control.

The I/O channel is used to interface to any I/O devices not on the system board. The I/O channel provides data and address lines, control signals, interrupt lines, and DMA control lines. Devices are addressed using I/O mapped address space. The I/O channel provides power to expansion slot J1.

An Intel 8272A Floppy Disk Controller device and FDC9229B Data Separator support double-sided, double-density format for the system floppy disk drives.

An eight-section DIP switch pack can be read by program control through an Intel 8255 Programmable Peripheral Interface device. The DIP switch provides all system information to firmware and software. Settings for this switch pack are given in the system User's Manual.

Scan codes from the keyboard, which are in serial data format, are converted into parallel data format and read by the programmable peripheral interface. The peripheral interface also controls the audio speaker tone and enable/disable I/O channel error check.

VIDEO MONITOR INTERFACE

The video monitor interface is configured around the Synertek 6845R CRT Controller. The interface is capable of operating in either monochrome or color.

WINCHESTER DISK CONTROLLER BOARD

A Western Digital WD1010-05 Controller on a WD1000-05 3 1/2-inch Winchester Disk Controller board is used to interface with the 5 1/4-inch Winchester hard disk drive.

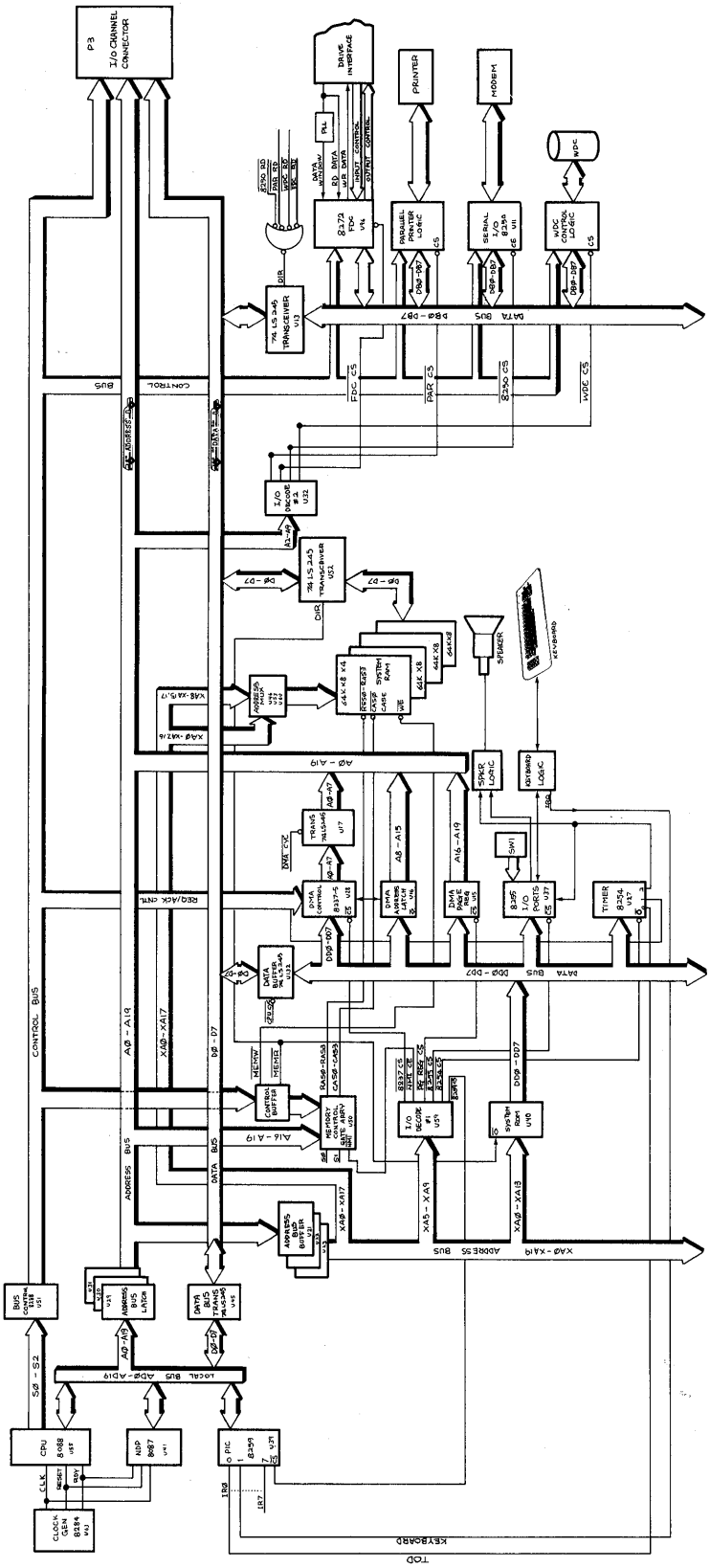
3. CIRCUIT DESCRIPTION

This section contains circuit descriptions of the major functional blocks of the TS 1605 and TS 1605H system board, as well as a description of the WD1000-05 Winchester Disk Controller Board.

The system board contains the CPU, main memory, I/O ports, controllers, and video display circuits for the system.

Figure 3-1 is a block diagram of the main board for the system.

Figure 3-1
Block Diagram of the Main Board



CPU CONTROLLER SECTION

The control section block diagram illustrates the processing of the control, data, and address buses. The 8284 time (U63) sends three signals to the 8088 and 8087 processors. The clock signal is a 4.77 MHz signal with a 33% duty cycle. The RESET signal halts CPU operation. The RDY signal inserts wait states between times T3 and T4 of the system bus cycle.

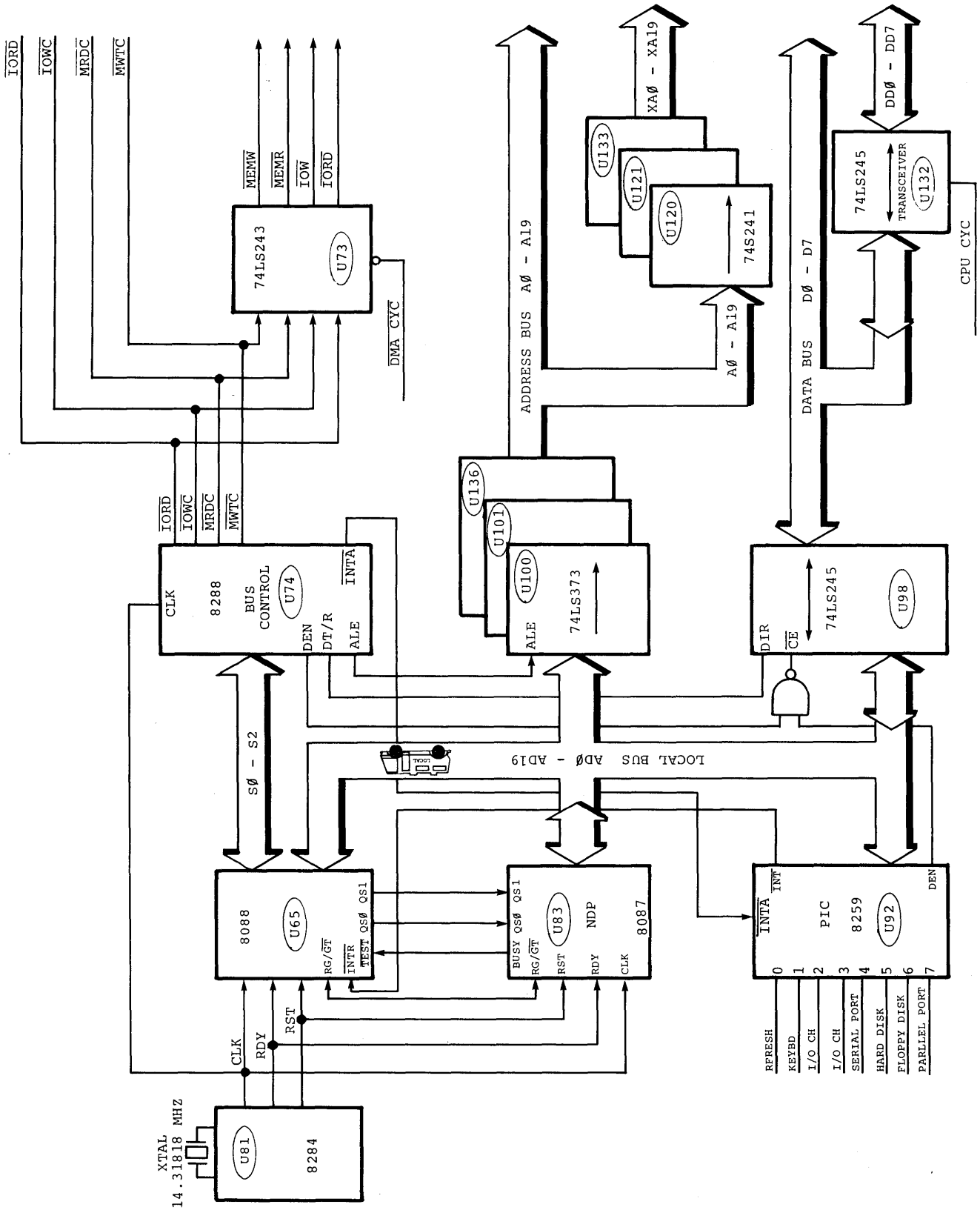
There are four signals that tie the 8088 to the 8087 co-processor. QSO and QSI are input to the 8087 so it can monitor the status of the 8088's internal queue. The RQ/GT1 signal of the 8088 is connected to the RQ/GT0 pin of the 8087. This signal allows the co-processor (8087) to take over the local bus to perform its functions. The TEST signal to the 8088 is examined by a WAIT instruction. If the TEST input is LOW, execution continues. Otherwise, the processor waits in an "idle" state.

Signals S0-S2 leave the 8088 with status information used and decoded by the 8288 bus controller. When decoded by the bus controller, these signals become the control bus signals IORD, IOWC, MRDC, and MWTC. However, during a DMA cycle, bidirectional transceiver U44 is the path for control bus signals which come from the DMA controller.

The 8288 bus controller also issues control signals DEN, DT/R, and ALE. The DEN signal enables bidirectional transceiver U45 which enables data onto the system data bus at T3 of the bus cycle. The DT/R signal controls the direction of the data flow through bidirectional transceiver U45. When active HIGH, the ALE signal latches address lines A0-A19 into latches U29, U30, and U31. These address lines are then buffered by U21, U22, and U23.

The 8259 interrupt controller accepts one of eight designated interrupts and issues an interrupt request (-INT) to the 8088. The 8288 bus controller checks the S0-S2 status lines from the 8088 and issues the interrupt acknowledge signal (-INTA) to the interrupt controller.

Figure 3-2
Control Section



The major components of the CPU Controller section are:

U55	Intel 8088 CPU System Microprocessor
U41	Intel 8087 Numeric Data Processor
U63	Intel 8284A Clock Generator
U29,U30,U31	Address Latches, #1,#2,#3
U45,U14	Transceivers, #1,#2
U21,U22,U23	Address Buffers, #1,#2,#3
U39	Intel 8259A Programmable Interrupt Controller
U28	Intel 8237A-5 Programmable DMA Controller
U40	Intel 2764 System ROM
U27	Intel 8254 Programmable Interval Timer

Table 3-1 lists the devices or lines on the CPU and their description.

Table 3-1
CPU Devices

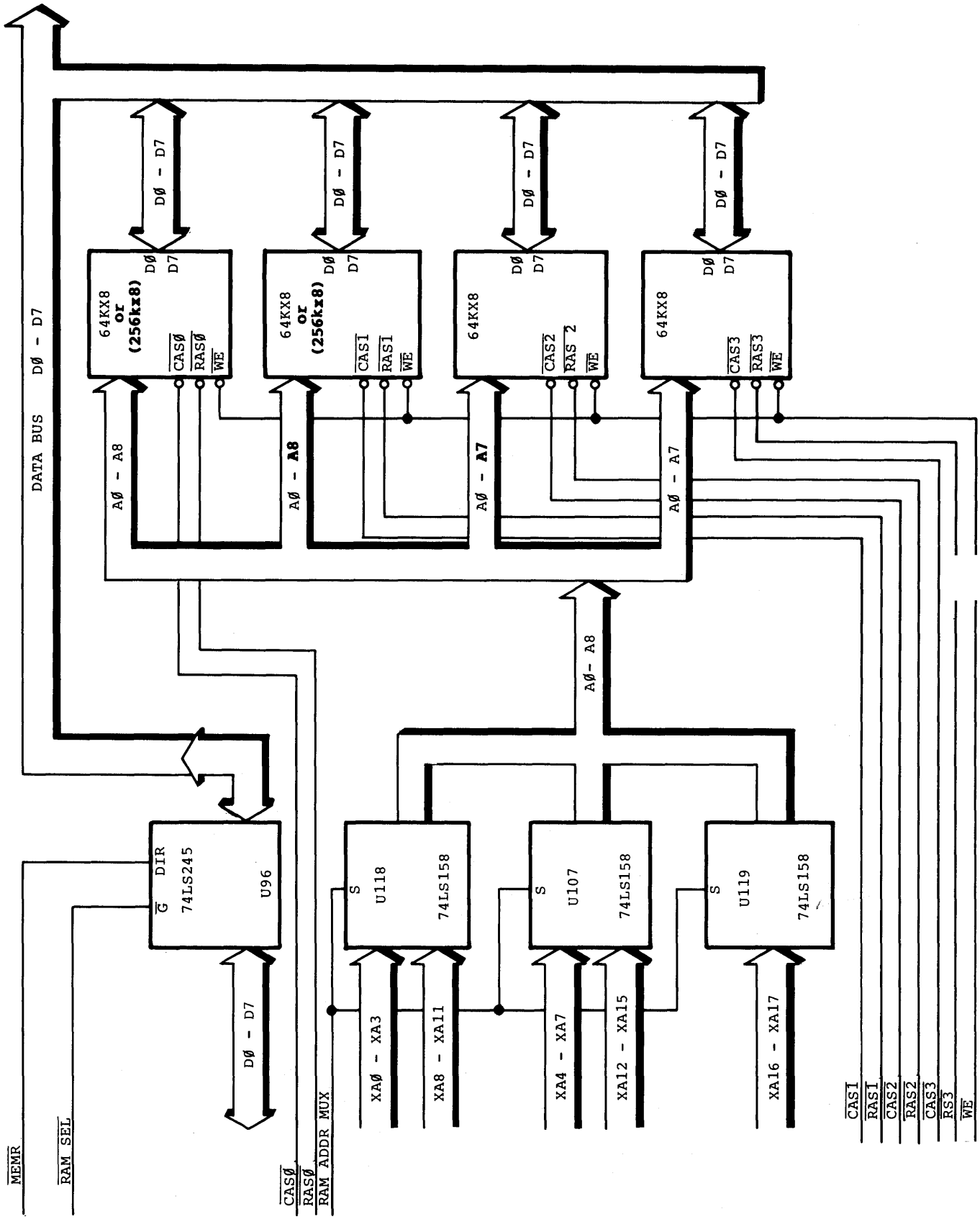
Device or Line	Source/Description
8088 CPU	Operated in the maximum mode, the CPU handles central processing functions, graphics display-related processing, and all writes to video memory. CPU timing conforms to the standards shown in the Intel Component Data Catalog.
-RD	CPU. Read signal indicates that the CPU is performing a memory or I/O read cycle.
RDY	CPU. Ready acknowledges that when not busy, addressed memory or I/O device will complete a data transfer. -S2,S1,S0 CPU. Status signal is active during clock high of T4, T1, and T2 and is returned to the passive state (1,1,1) during T3 or during Tw when RDY is high. Status signals are used by bus controller to generate all memory and I/O access control signals.
-RQ/GT0,-RQ/GT1	Request/Grant signals are used by other local bus masters to force the CPU to release the local bus at the end of the CPU's current bus cycle.
-LOCK	CPU. This signal indicates that other system bus masters are not to gain control of system bus while LOCK is active (low).
QS1,QS0	CPU. Queue status signal allows external tracking of the internal CPU instruction queue.

Numeric Data Processor	Provides instructions anddata types for high-performance numeric applications. Serves as a co-processor to the CPU.
Clock Generator	Generates the system clock for the CPU. Using a 14.31818-MHz crystal, the clock generator divides down a 4.77-MHz frequency source for the CPU and numeric data processor.
Address Latch #1	Address latch #1 converts CPU lines AD0 through AD7 to address lines A0 through A7.
Address Latch #2	Address latch #2 converts CPU lines AA8 through AA15 to address lines A8 through A15.
Address Latch #3	Address latch #3 converts CPU lines AS16 through AS19 to address lines A16 through A19.
Data Transceiver	Converts CPU lines AD0 through AD7 to data #1 lines D0 through D7.
Data Transceiver	Converts data lines D0 through D7 to data #2 lines DD0 through DD7.
Address Buffer	Buffers address lines A0 through A7, which #1 become XA0 through XA7.
Address Buffer	Buffers address lines A8 through A15, which #2 become XA8 through XA15.
Address Buffer	Buffers address lines A16 through A19, which #3 become XA16 through XA19.
Programmable Interrupt Controller	Handles vectored interrupts for the CPU, accepting interrupt requests from peripherals and determining priority.
Programmable DMA Controller	Allows peripheral devices todirectly transfer information from or to system memory.
System ROM	Addressed on lines XA0 through XA7, XA8 through XA13, and data lines DD0 through DD7, system ROM allows CPU to operate without generating wait states to the system.
Programmable Interval Timer	A three-channel,counter-timerdevice. Channel 0 is used for time-of-day implementation, and channel 1 times out dynamic memory refresh. Channel 2 supports tone generation for the speaker.

MAIN MEMORY

The addresses on the TS 1605/1605H RAM are multiplex. The RAM address MUX signal selects either the Row address (RAS) or the column address (CAS) lines. For 64K x 1, U60 is not used. The total address is 16 bit - the upper 8 bits are used for column, and the lower are used for row. READ comes from memory to the CPU. WRITE comes from the CPU to memory. Refer to Figure 3-3 for a block diagram of the RAM main memory.

Figure 3-3
RAM Main Memory



The major components of main memory are:

U50	TeleVideo Memory Control Gate Array
U51	Intel 8288 Bus Controller
U128,U93,U119, U86,U110,U77, U101,U69	Bank 0 Dynamic RAM
U127,U92,U118, U85,U109,U76, U100,U68	Bank 1 Dynamic RAM
U126,U91,U117, U84,U108,U75, U99,U67	Bank 2 Dynamic RAM
U125,U90,U116, U83,U107,U74, U98,U66	Bank 3 Dynamic RAM

Table 3-2 lists the components of the main memory and their description.

Table 3-2
Main Memory Components

Device or Line	Source/Description
Memory Control Gate Array	Generates all necessary signals for reads and writes to dynamic memory.
A16-A19	CPU address latch #3. Address lines to memory control gate array. Provide address for memory data bus exchanges.
S0,S1	CPU. Status lines to memory control gate array. Memory control gate array. Row select -RAS2,-RAS3 signals to main memory. -RAS0 selects row address for bank 0, -RAS1 for bank 1, -RAS2 for bank 2, and -RAS3 for bank 3.
-RAS0, -RAS1 -RAS2, -RAS3	
-CAS0,-CAS1, -CAS2,-CAS3	Memory control gate array. Column select signals to main memory. -CAS0 selects column address for bank 0, -CAS1 for bank 1, -CAS2 for bank 2, and -CAS3 for bank 3.
-RAM SEL	Memory control gate array. Control signal selects one of four banks of main memory.
Bus Controller	Decodes status lines and provides the system with all bus control signals. Together with memory control gate array, provides command and control timing generation and bipolar bus drive capability.

-MEMR	Bus controller. Control signal into memory control gate array to generate memory reads to main memory.
-MEMW	Bus controller. Control signal into memory control gate array to generate memory writes to main memory.

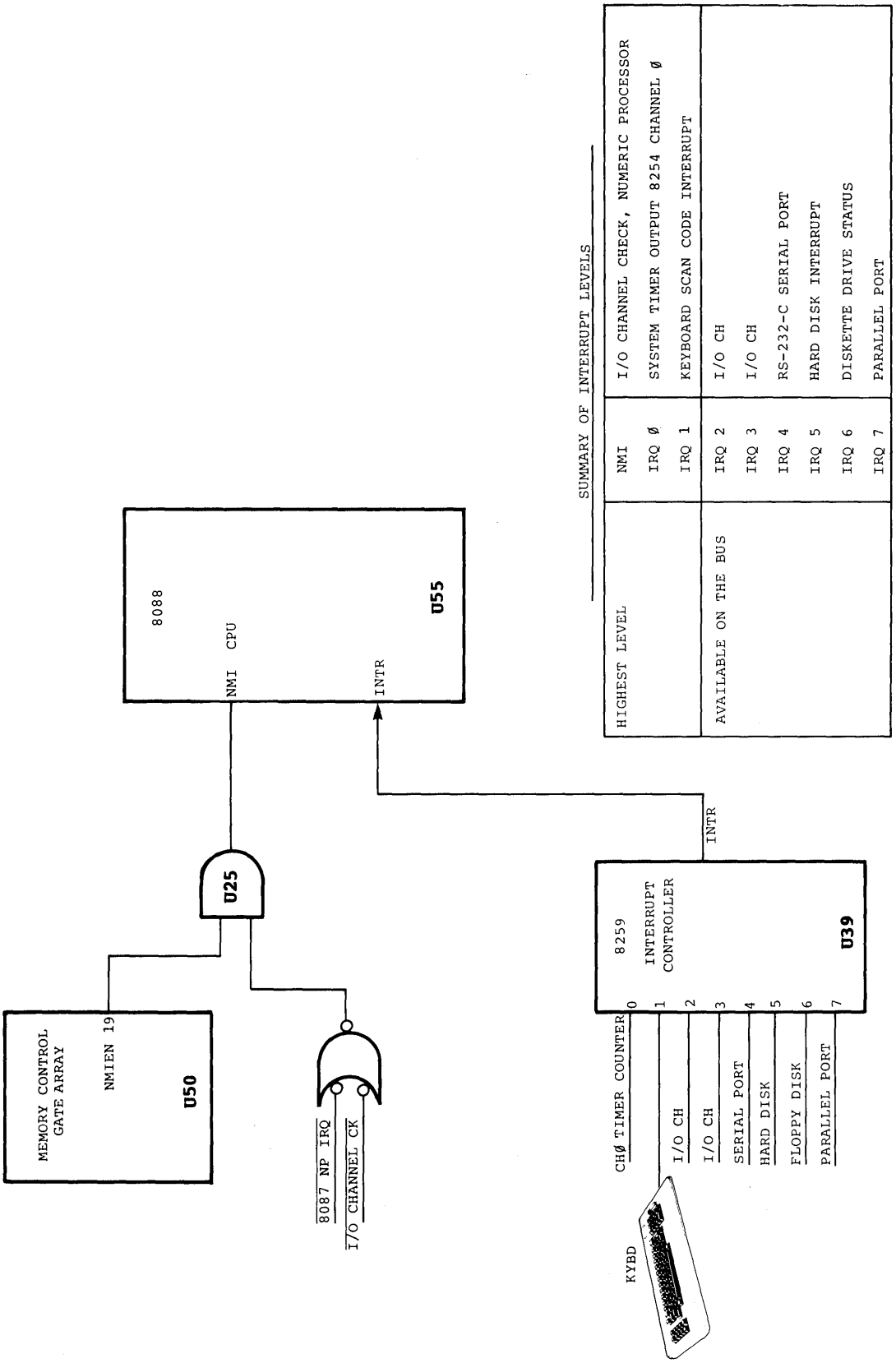
INTERRUPT SYSTEM

The system can generate one of eight designated interrupts to the 8259 interrupt controller. The INT controller then issues an interrupt signal to the CPU. Status lines -S0, -S1, and -S2 go from the CPU to the 8288 bus controller. The signal tells the 8259 to run an interrupt. The 8288 issues an INTA (two signal pulses) to the 8259. The first pulse freezes the interrupt priority in the 8259. The second pulse causes the 8259 to put an 8-bit word on the data bus to the CPU. This is a partial address of the interrupt vector in the lower 1K of system RAM.

The CPU issues a 10-bit address that accesses one of a possible 256 locations in memory. Each of these 256 memory locations consists of 32 bits of memory. These 32 bits are segmented to establish the current address of the interrupt subroutine.

See Figure 3-4 for a diagram of the interrupt system.

Figure 3-4
Interrupt System



DMA

There are four DMA channels, 0, 1, 2, and 3.

0 = refresh
1 = optional I/O channel
2 = floppy disk controller
3 = optional I/O channel

The DMA cycle is initiated by a DMA request from one of the four above channels. For example, if the FDC requests a DMA request, it sends an FDC DRQ signal to the memory control gate array. The gate array issues a signal to the DMA controller. See Figures 3-5 and 3-6 for diagrams of the DMA.

Figure 3-5
DMA Control

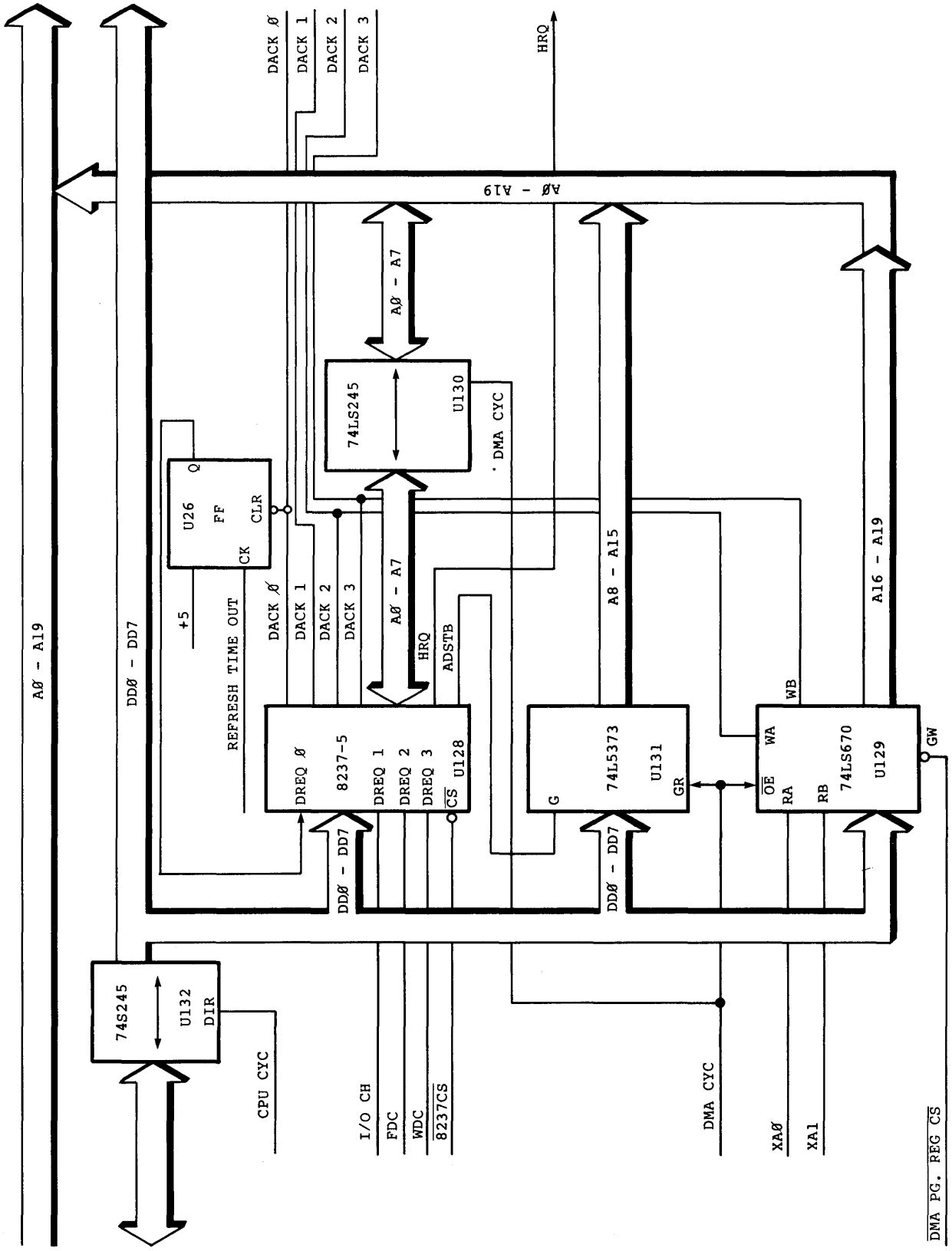
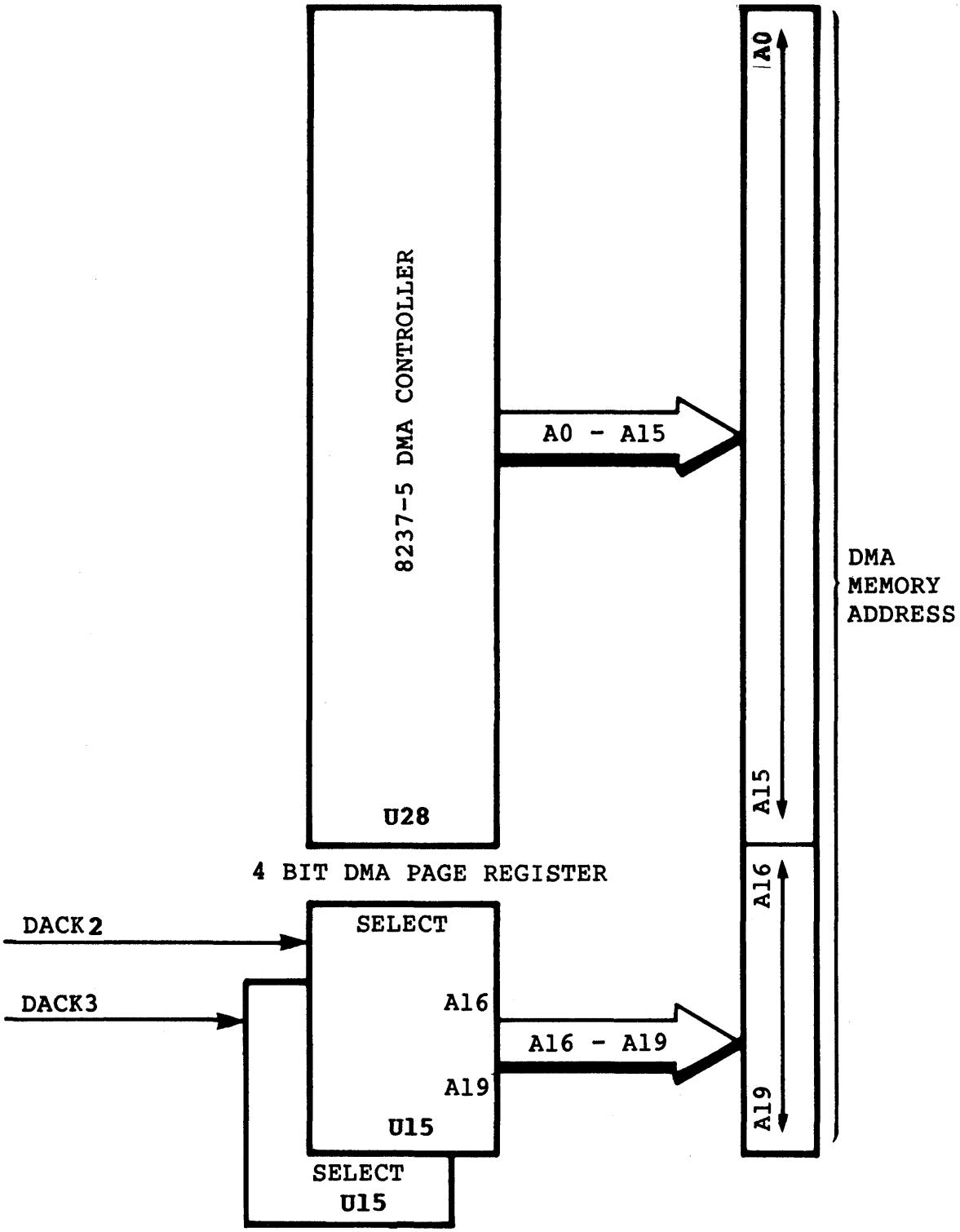


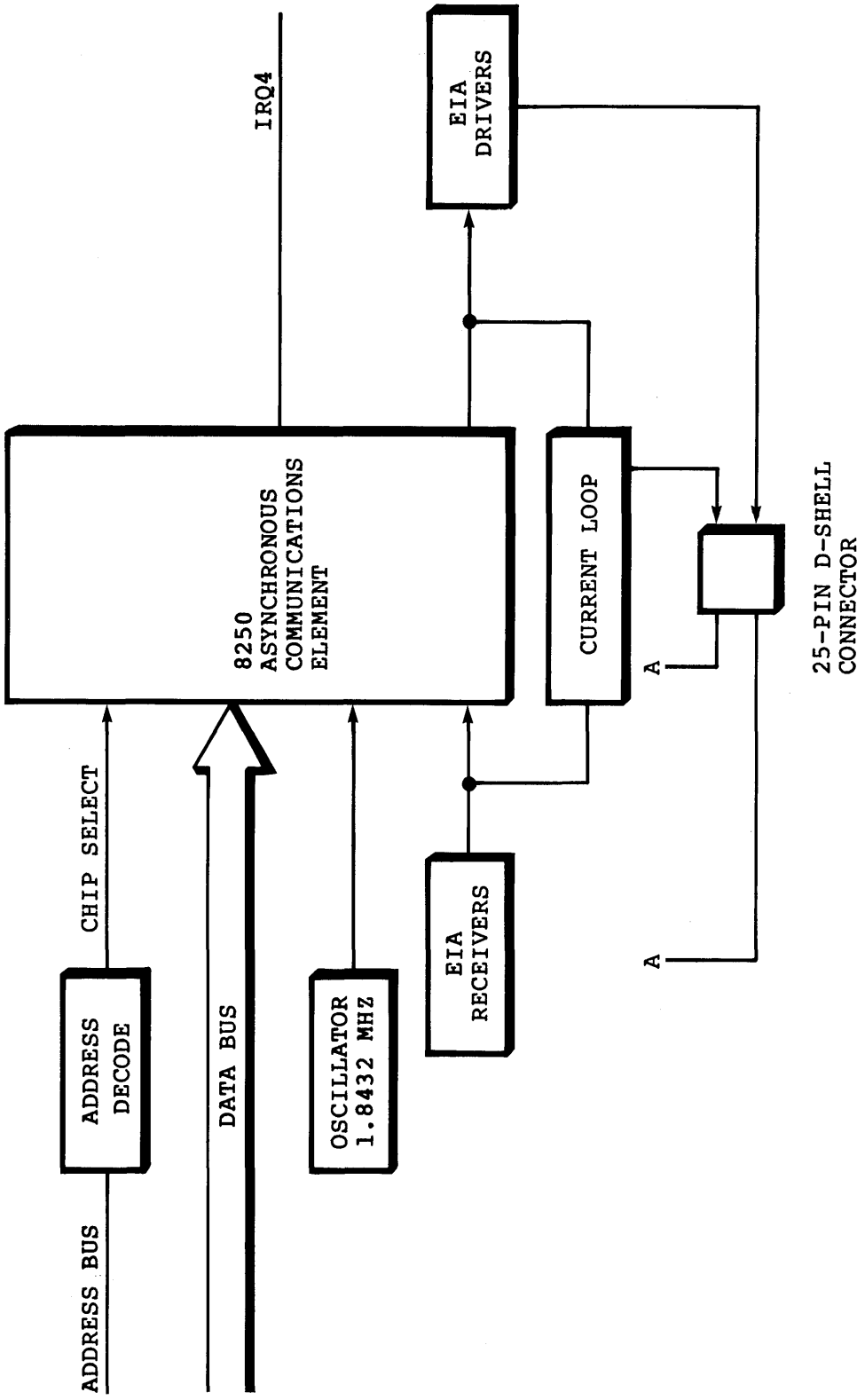
Figure 3-6
DMA Memory Address Generation



SERIAL I/O

The serial communications port interfaces with an RS-232 asynchronous communications-type device at 50 - 9600 baud rate, such as a serial printer or modem. There is a transmit and receive line, and handshaking protocol. Figure 3-7 shows a diagram of the asynchronous communications of the TS 1605/1605H.

Figure 3-7
Asynchronous Communications



The major serial I/O component is:

U11 WD8250 or INS8250BSerial I/O Controller

A block diagram of the serial I/O port is shown in Figure 3-8.

Figure 3-8
I/O Interface Diagram

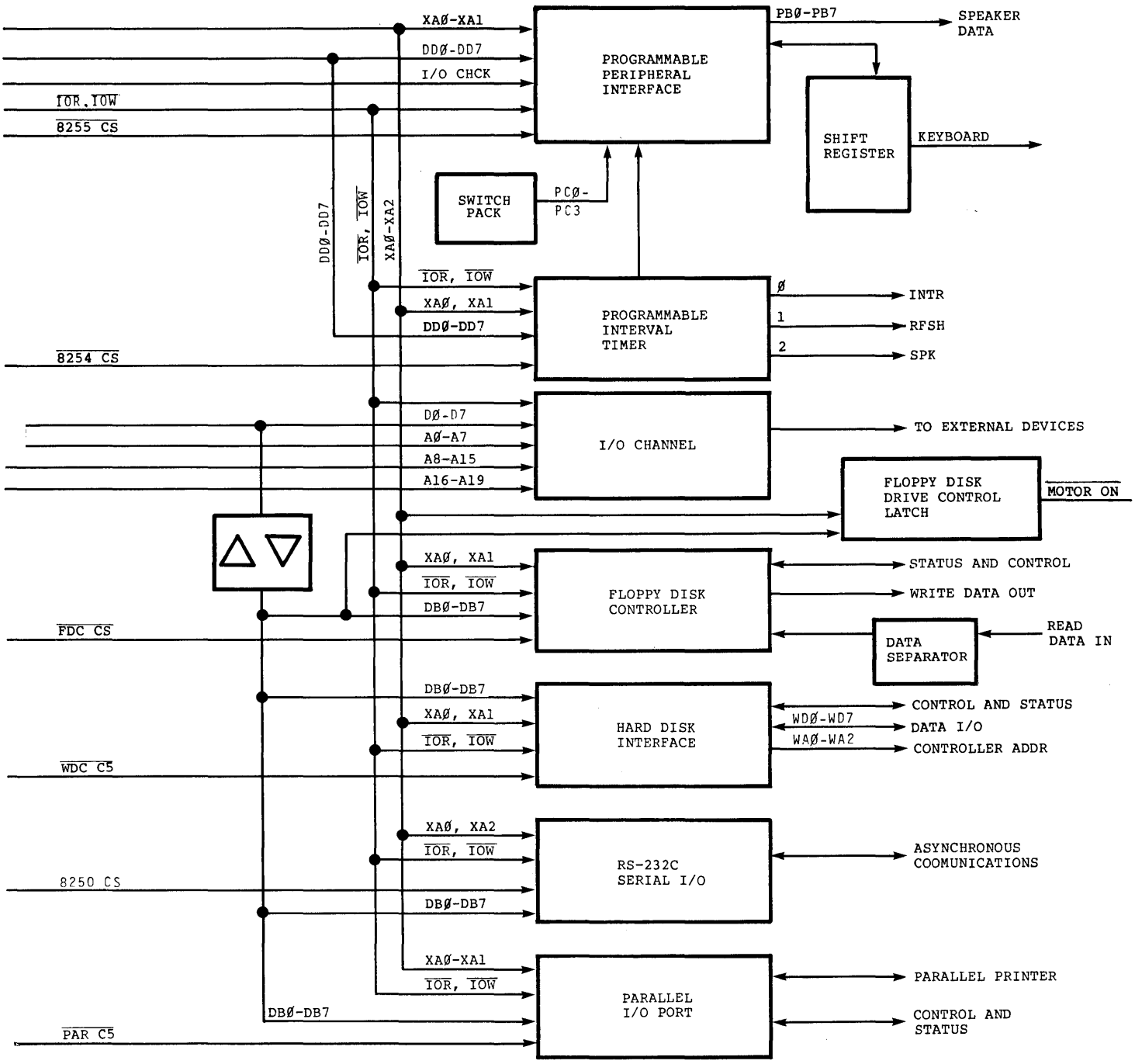


Table 3-3 lists the major component of the serial I/O and its description.

Table 3-3
I/O Component

Device or Line	Source/Description
Serial I/O Controller	An RS-232Cdevice thatis usedfor asynchronous communications only, but is capable of supporting current loop operation. Enabled by CPU lines XA0 through XA2 and DB0 through DB7 and control signals -IOR, -IOW, and -8250 CS. This device can be programmed from 50 baud to 9600 baud.

PARALLEL PRINTER PORT

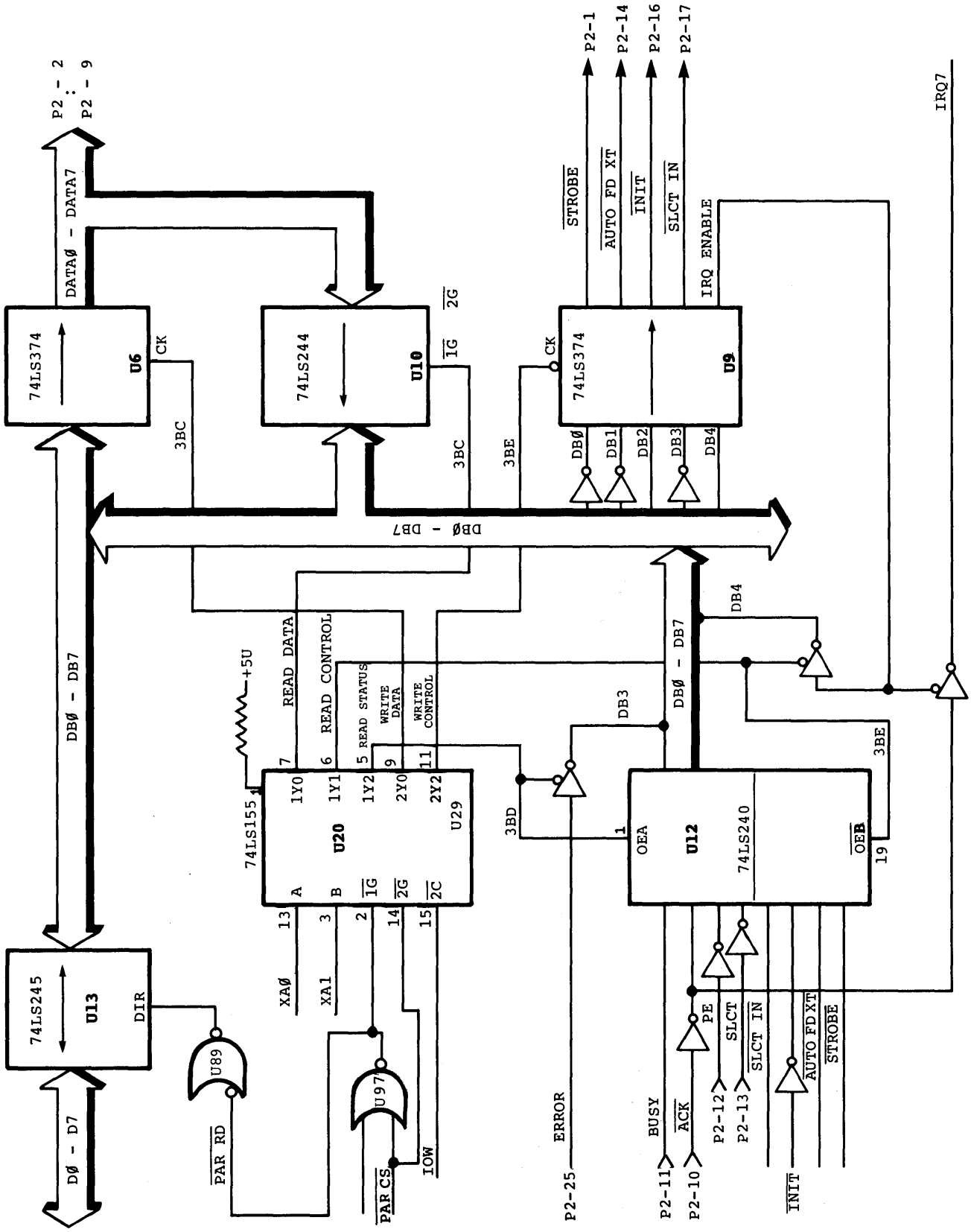
The parallel port is a general purpose I/O port configured on the TS 1605/1605H to interface to a parallel printer. Interrupts can be enabled or disabled under program control. Since a 25-pin, D-type connector is used in this system, a special cable is required for interface to a standard Centronics-type printer. See Figure 3-9 for a diagram of the parallel printer port.

U8 is a bidirectional receiver with the direction controlled by the parallel chip select or an I/O read.

Write data in U6 is read back through U10. Then write control and write information goes into INIT, SLST N, AUTO FD XT, STROBE. Read control is enabled to read those control signals. Once read, the system and hardware are functioning properly. Then status is read from the printer for error, busy, ACK, PE, or select. Then write data is sent to the printer. STROBE then goes to low. This initiates read status to read busy and ACK signals from the printer. When okay, reads information into the CPU via the data bus. Then a write data into U6, then strobe data with write control signal into parallel printer. Then another read status cycle. This process continues until all of the data is transferred.

NOTE! Read control is performed for the data latch only when the system is first booted up.

Figure 3-9
Parallel Printer Logic



The major parallel I/O components are:

U6	Data Latch
U10	Data Buffer
U12	Status Buffer
U9	Control Latch
U20	Multiplexer

The major parallel I/O components are in Table 3-4.

Table 3-4
Major Parallel I/O Components

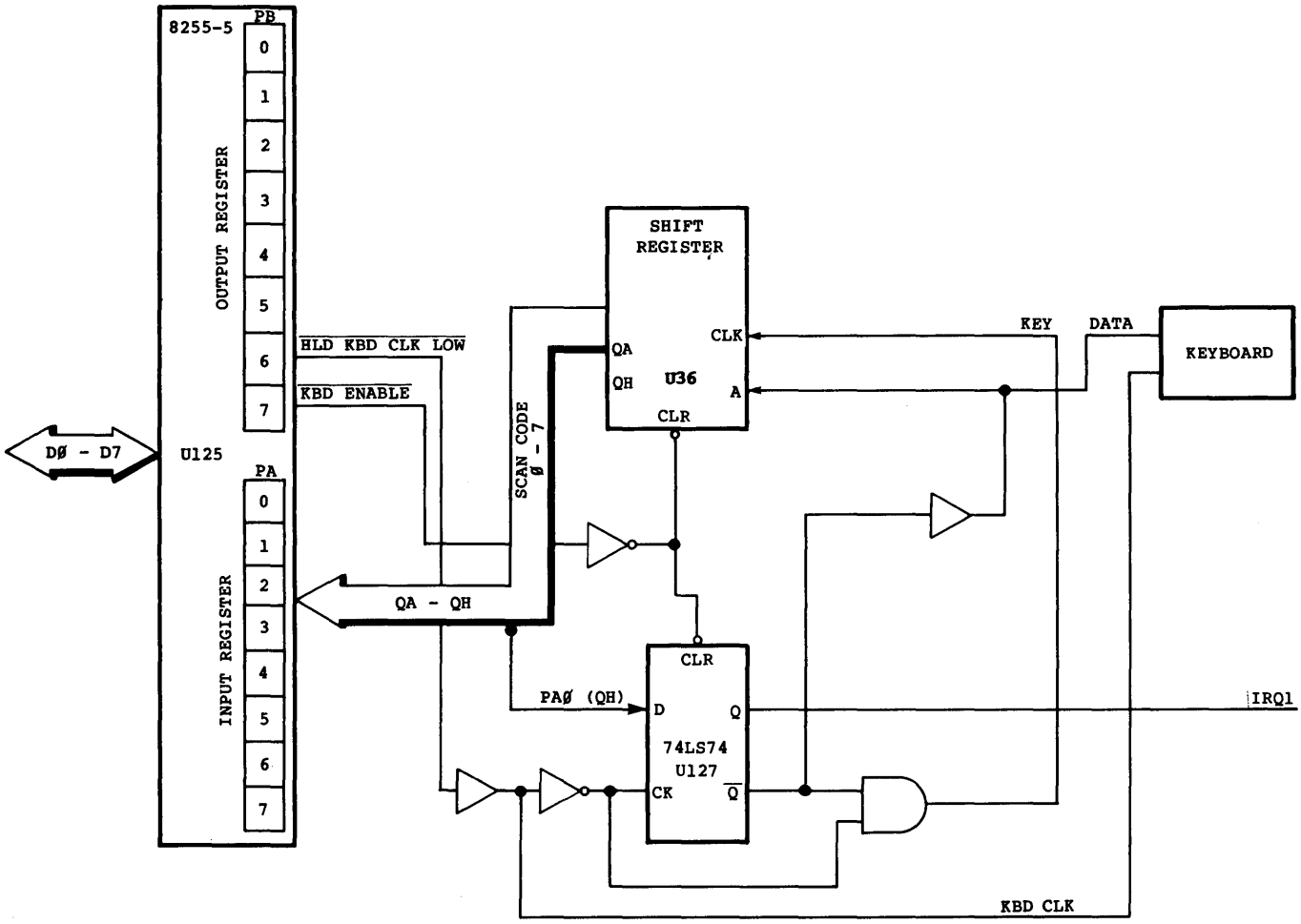
Device or Line	Source/Description
Data Latch	Used as a temporary storage buffer for data transmitted to the parallel printer on output lines DATA0 through DATA7. Data is written into the data latch by the CPU when signals -PAR CS and -IOW are activated. Data lines DB0 through DB7 carry data transfers to this latch.
Data Buffer	Buffers output lines DATA0 through DATA7 into data lines DB0 through DB7.
Status Buffer	Buffers status signals, -ERROR, SLCT, PE, -ACK, and BUSY that go from the parallel printer to the CPU. These signals are read by the CPU when -IOR and -PAR CS are activated.
Control Latch	Control signals -STROBE, -AUTO FEED, -INIT, and -SLCT IN are transmitted to the parallel printer when the CPU enables lines -IOW and -PAR CS.

KEYBOARD INTERFACE

The TeleVideo and IBM keyboards are not plug-compatible. A TeleVideo keyboard must be used with the TeleVideo system. Under normal keyboard conditions, the output register of 8255, PB bits 6 and 7, control the keyboard-enabling circuit - bit 6 is high, bit 7 is low. In this condition, the keyboard circuit can receive data from the keyboard. Whenever the key is pressed, the data goes from the keyboard to input A of the U116 input register (see Figure 3-10). At the same time, the keyboard clock sends information through inverter U19 and through AND gate U25 and then to the clock of the shift register. This clocks the 8-bit code representing the number of the key that was pressed. The start bit is the MSB (QH). When the information is stored in the shift register, QH is fed back to the data input of D flip-flop U127. When the clock goes in, it generates interrupt IRQ1. This sends the microprocessor into the interrupt service routine which processes the key.

When the interrupt is generated at the Q output with a logic high, the Q is a logic 0 which is sent back to the keyboard data input via U7 and that prevents the keyboard from sending more data. It also inhibits U25 to prevent the keyboard clock from shifting more data into the shift register.

Figure 3-10
Keyboard Circuit



The major components of the keyboard interface are:

U37	Intel 8255A-5 Programmable Peripheral Interface (PPI)
U38	Serial Shift Register

The major components of the keyboard interface and their description are listed in Table 3-5.

Table 3-5
Keyboard Interface Components

Device or Line	Source/Description
Programmable Peripheral Device	Programmed by system software, this device reads the eight-position DIP switch and interfaces to keyboard receiving and transmitting scan code. Controls audio speaker tone and enable/disable I/O channel error check. Enabled by address lines XA0 through XA1, data lines DD0 through DD7, and control signals -IOR, -IOW, and -8255 CS.
PA0-PA7, PB0-PB7, PC0-PC7	PPI. Ports A, B, and C. Each port is composed of eight bits, configured by system software. Accepts commands from read/write control logic, receives control words from the internal data bus, and issues the proper commands to the associated ports.
A0-A1	CPU. Port select input signals, in conjunction with -RD and -WR signals, control the selection of one of three ports or the control word registers.
Serial Shift Register	Permits complete control over incoming data lines PA0 through PA7. Data at serial inputs may be changed while clock is high or low, but only information meeting set-up requirements is entered. Clocking occurs in low-to-high transition of clock input.

SPEAKER DRIVE SYSTEM

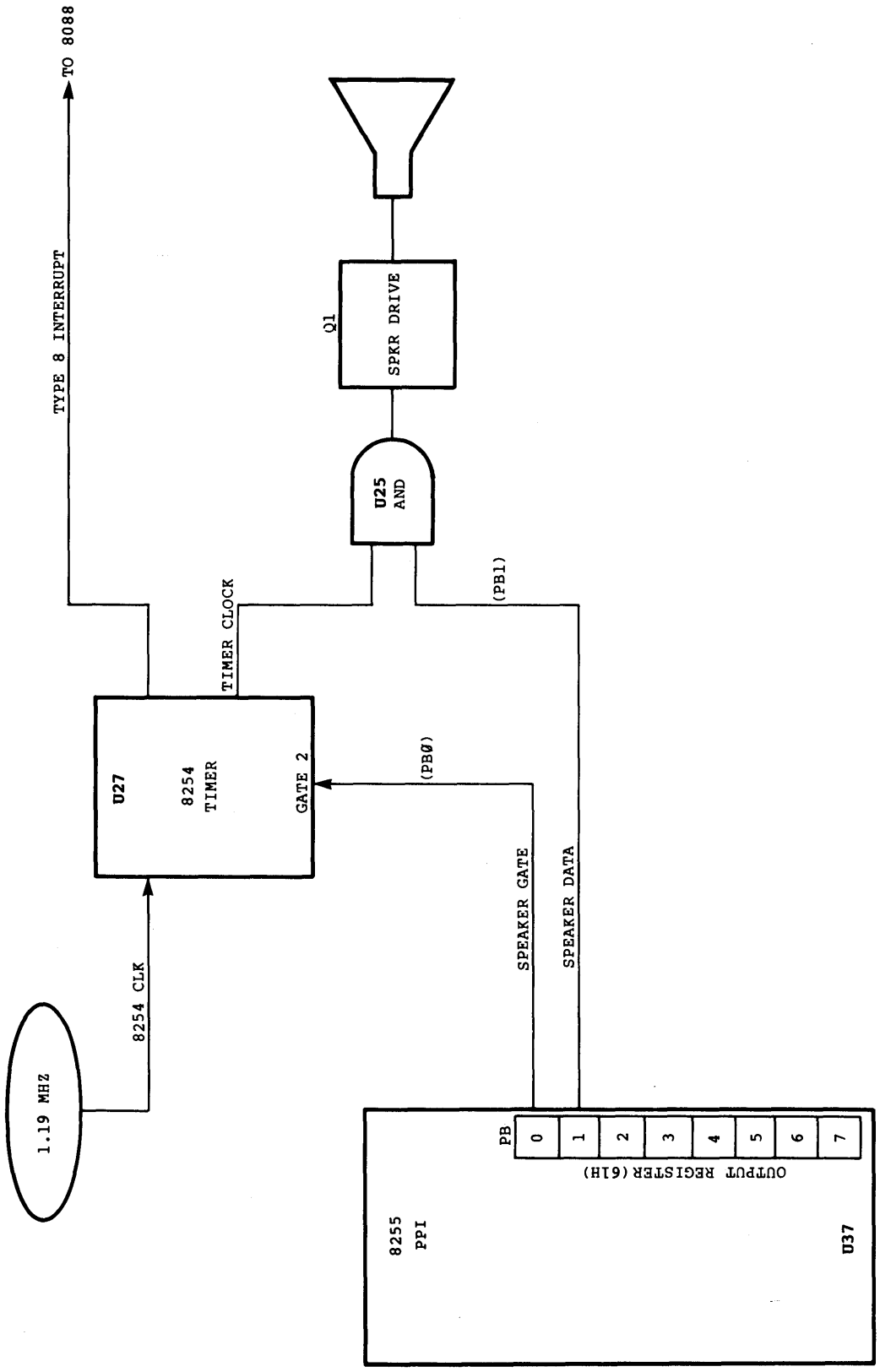
You can control the frequency of the speaker output by programming the different frequencies coming from timer 8254 (see Figure 3-11). The speaker frequency is controlled by the frequency divider in the 8254 timer 2. The frequency can be controlled by programming so you can change it through software. Bit 0 of the output register PB of the 8255 is used to control the speaker gate so you can turn the timer on and off. The timer clock is ANDed with the 8255 output register PB bit 1. The output of U26 provides the information to speaker drive Q25.

The speaker driver is controlled by 8255. 0 enables the speaker interface. Channel 2 timer clock is used to supply the oscillating frequency to control the speaker.

When you want to turn on a speaker, use 8255 PB 1.

PB1 = 1 = turn on speaker
PB1 = 0 = turn off speaker

Figure 3-11
Speaker Drive System



INPUT/OUTPUT CHANNEL

The input/output channel, located on the system board, provides interface to I/O devices external to the system board. This channel consists of a connector with data and address buses, control signals, interrupt lines, DMA control lines, and power and ground lines. The I/O channel pin configuration is listed in Appendix F. A block diagram of the input/output channel is shown in Figure 3-8.

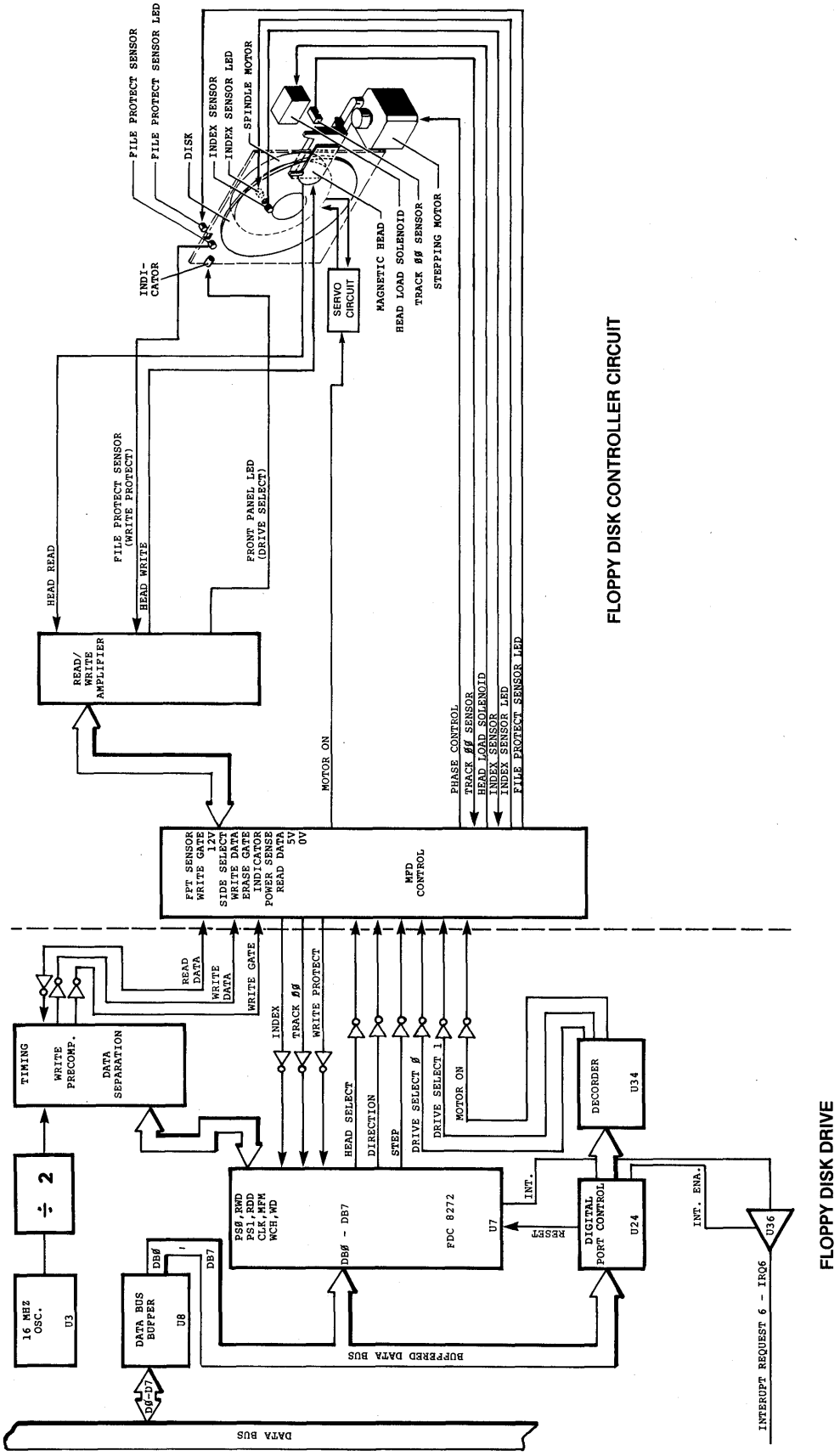
FLOPPY DISK CONTROLLER

The floppy disk control circuitry is based around the 8272A (U96) floppy disk controller chip. The 9229B FDC does all write precompensation functions. The 8272A keeps track of where the floppy heads are currently located and stores more internal memory than previous floppy disk controllers. Also, data being read from the disk is intercepted by a 9229B (U81) Data Separator. The Data and Clock pulses that compose MFM data on the diskette are separated and synchronized with the 8272A internal clock to ensure accurate data exchanges. The 8272A FDC is programmed to operate in the burst transfer mode at system initialization by the EPROM.

The other important support ICs are the bidirectional buffer (U13) and the floppy disk latch (U42). They control the selection of the disk drive and the turning on of the floppy motor. These are taken as control words from the system data bus.

The basic functions of the floppy disk controller circuitry are 1) writing data to the diskette, 2) reading data form the diskette 3) determining where to write on the diskette, and 4) turning the drive off and on and selecting drive A or B. 1, 2, and 3 are all controlled by the 8271A FDC.

Figure 3-12
Floppy Disk Controller



The major components of the floppy disk controller are:

U96	Intel 8272A Floppy Disk Controller Device
U42	Floppy Disk Drive Control Latch
U81	FDC9229B Data Separator

The floppy disk controller components and their description are listed in Table 3-6.

Table 3-6
Floppy Disk Controller Components

Device or Line	Source/Description
Floppy Disk Controller	Provides parallel-to-serial conversion of data from the system to the floppy disk, and serial-to-parallel conversion from the floppy disk to the system, as well as all drive control functions, such as head step, head direction, write protect, and track 0 detection. The controller can be programmed to handle seek track, read sector, write sector, read address, read track, and write track operations. The DB0-DB7 Data Transceiver carries data and programming signals between the FDC and CPU.
-COMP READ DATA	FDD. Carries composite read data to floppy disk drives.
-COMP WR DATA	FDC. Carries composite write data to floppy disk drives.
Floppy Disk Drive Control Latch	Controls floppy disk drive number selection, motor on/off, enable/disable interrupt, enable/disable DMA operation, and FDC reset.
Data Separator	Performs write precompensation and data separation.

WINCHESTER CONTROLLER INTERFACE

The major components of the Winchester controller interface are:

U8	Data/Address Transceiver
U18	Control Signals Buffer

A block diagram of the Winchester controller interface is shown in Figure 3-8.

The Winchester controller interface components and their description are listed in Table 3-7.

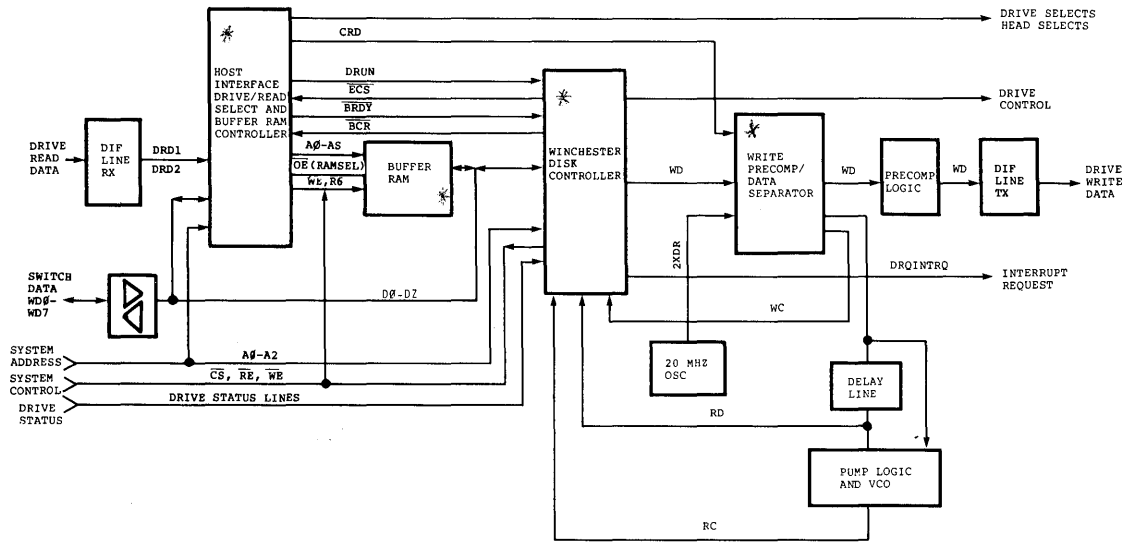
Table 3-7
Winchester Controller Interface Components

Device or Line	Source/Description
Data/Address Transceiver and Control Signals Buffer	The transceiver and buffer pass data, address, and control signals to an external Winchester disk controller board.
WD0-WD7	Data/Address Transceiver. Buffered data lines to the Winchester controller board. WA0-WA2 Control signals buffer. Buffered address lines to the Winchester controller board.
-WCS,-WWE, -WRE,WMR, -WDC RD	Control signals buffer. Buffered control signals to the Winchester controller board.

WINCHESTER DISK CONTROLLER BOARD

The Winchester disk controller board provides all control and data handling functions needed to interface the system with a 3 1/2-inch Winchester disk drive. Figure 3-13 shows a block diagram of the Winchester disk controller board.

Figure 3-13
Winchester Disk Controller Board Block Diagram



The major components of the Winchester disk controller board are:

U24	WD1100-21 Host Interface, Head and Drive Select, and Buffer Ram Controller
U23	WD1010-05 Winchester Disk Controller
U16	WD1100-10 Write Precompensation and Data Separator
U25	Type 6116 Buffer RAM
U26	Board Busy Tristate Buffer
U5	Error Amplifier
U11,U18	Pump Logic
U13	Voltage Controlled Oscillator (VCO)
U27	Host Interface Bus Transceiver
U3	Differential Line Receiver
U17	Precompensation Logic
U4	Differential Line Transmitter

System/Controller Interface

The system programs the Winchester disk controller board by accessing the WD1010-05 controller device task file registers.

The system/controller interface lines are shown in Figure 3-2.

Table 3-8 lists the system/controller interface components and their description.

Table 3-8
System/Controller Interface Components

Active Line	Source/Description
A0 to A2	System. Task file register address.
-WE or -RE	System. -WE to activate task file write, or -RE to activate task file read.
D0 to D7	System. Data or command.

Operations With Buffer RAM

The Winchester disk controller board uses 1 kilobyte of a 2 kilobyte-by-8-bit buffer RAM to interact with the system during disk read and write operations. When writing to disk, the system writes the data to the buffer RAM by sector. After a sector of data is loaded into the buffer RAM, the WD1010-05 reads the data from the buffer RAM to the disk. The lines used in the operations with buffer RAM are shown in Figure 3-2.

Table 3-9
Write From Buffer RAM

Active Line	Source/Description
D0 to D7	System. Sets up Task File Register and Write Sector command in WD1010-05 task file and writes data to buffer RAM.
-BCR	WD1010-05. Strobed to zero counter in WD1100-21.
DRQ	WD1010-05. Active to indicate that the buffer RAM is empty.
-BCS	WD1010-05. Set high to enable host control of buffer RAM. Transceiver direction is ready for write.
-WE	System. Loads buffer and increments counter with -CS.
-BRDY	WD1100-21. Active to indicate buffer full.
-BCS	WD1010-05. Active to disconnect host control of buffer RAM. Board busy tristate buffer on line WD7 is activated by -BCS to prevent system access during next operation.
-RE	WD1010-05. Reads buffer RAM to transfer data to disk (See Writing Disk Data).
-BCS	WD1010-05. Set high to allow next operation by system. Board busy tristate buffer inactive.
INTRQ	WD1010-05. Signals end of command to system.

Reads of buffer RAM occur after a sector of data has been loaded to the RAM from the disk. For a read from buffer RAM, see Table 3-10.

Table 3-10
Read From Buffer RAM

Active Line	Source/Description
D0 to D7	System. Sets up Task File Registers and places Read Sector command in WD1010-05 task file.

-BCS	WD1010-05. Active to disconnect host control of buffer RAM. Board busy tristate buffer on line WD7 is activated by -BCS to prevent system access during next operation.
-BCR	WD1010-05. Strobed to zero counter in WD1100-21.
-WE	WD1010-05. Loads buffer from disk (See Reading Disk Data), and increments counter with -CS.
BRDY	WD1100-21. Active to indicate buffer full.
-BCR	WD1010-0d. Strobed to zero counter in WD1100-21.
-BCS	WD1010-05. Set high to enable system control of buffer RAM. Board busy tristate buffer inactive.
DRQ	WD1010-05. Active to initiate transfer to system.
-RE	System. Reads buffer RAM and increments counter with -CS.
-BRDY	WD1100-21. Active to indicate buffer empty.
-INTRQ	WD1010-05. Set high to stop operation.

Writing Disk Data

The write sector command requires that the Winchester controller locate the place on the disk that is to receive the data, control the write operation to buffer RAM by the system, then read the data from the buffer RAM, condition the data into MFM format, and write the data to disk.

Under MFM, clock bits are recorded only when two successive data bits are missing in the serial data stream. Using MFM reduces the total number of bits required to record a given amount of information on the disk. Because this effectively doubles the amount of disk capacity, it is termed "double density."

Encoding MFM follows three rules: 1) if the current data cell contains a data bit, then no clock is generated, 2) if the previous data cell contained a data bit, then no clock is generated; 3) if the previous data cell and the present data cell are vacant, then a clock is generated in the current clock cell. Data and clock cells are defined by the state of the write clock line, WC. If WC is low, it is a data cell; if WC is high, it is a clock cell. Both clock and data cells are 100 nanoseconds long in ST506-compatible drives.

The active lines for writing disk data are diagrammed in Figure 3-14.

Figure 3-14
Writing Disk Data

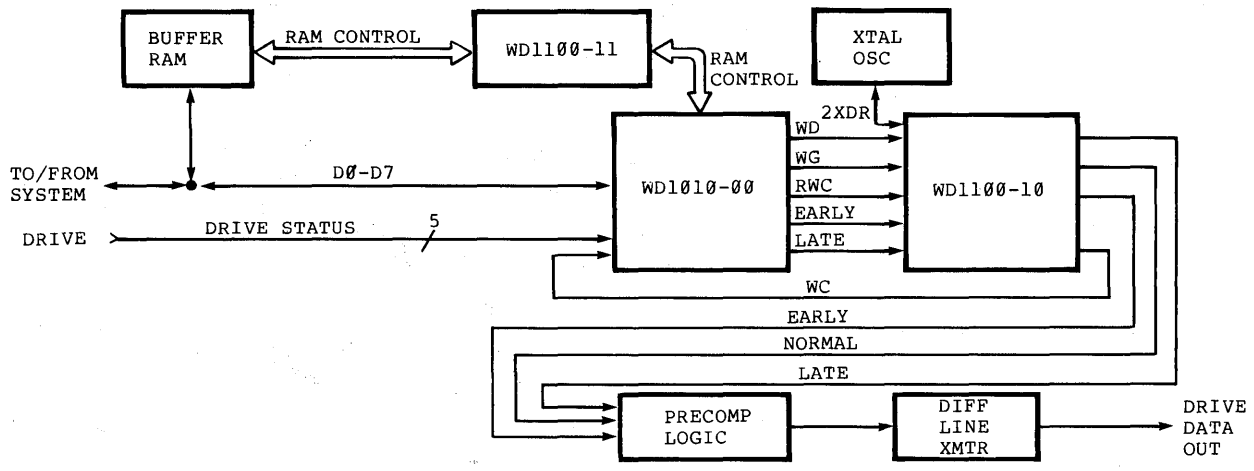


Table 3-11
Writing from Buffer RAM

Active Line	Source/Description
D0 to D7	System. Contains write sector command. When the WD1010-05 receives this command, it checks its cylinder registers against the current cylinder position.
-BCR	WD1010-05. Strobed to begin write to buffer RAM by system.
BRDY	WD1100-21. Buffer RAM full.
-BCS	WD1010-05. Active to disconnect host control of buffer RAM. Board busy tristate buffer on line WD7 is activated by -BCS to prevent system access during next operation.
-STEP,-DIRET	WD1010-05. Moves head to locate cylinder.

SEEK COMPLETE	Drive. Informs WD1010-05 that the head settling time for the current step is expired. If current step is not the required cylinder position, the head is moved again. After seek to desired cylinder, controller checks for desired sector address by reading data from drive.
WG	WD1010-05. Write gate signal to WD1100-10.
WC	WD1100-10. Carries 5 MHz write clock, derived from 2XDR clock signal, to WD1010-05.
-RWC	WD1010-05. Reduced write current signal; turns on precompensation circuits for write to disk.
-WD	WD1010-05. Write data as read from buffer RAM and serialized by WD1010-05.
-EARLY, -LATE	WD1010-05. Precompensation signals to WD1100-10. Precompensation is used to counteract the effects of dynamic bit shift when writing the inside recorded tracks of the disk. Dynamic bit shift results when a bit on the disk influences the position of an adjacent bit. The leading edges of the bits are moved closer together, or further apart, depending upon the polarity of each bit. Because the positions of the bits shift as they are written to the disk, the data is harder to recover without error. Write precompensation is applied to counteract the effects of dynamic bit shift. Precompensation predicts the direction a bit will be shifted, then writes the bit out of position in the opposite direction to the shift. The prediction is done in the WD1010-05 by checking the next two data bits, the last bit written, and the present bit.
EARLY, NORMAL, LATE	WD1100-10. Precompensation signals to precompensation logic. Data is shifted +/-12 nanoseconds from normal position through a delay line.
Data	Differential Line Driver. Carries MFM formatted, precompensated, RS-422 write data to drive head.
-BCS	Set high to allow next operation by system. Board busy tristate buffer inactive.

Reading Disk Data

For disk reads, the Winchester disk controller board locates the sector to be read, identifies the start of the data field, reads the data in from the disk, separates the data and clock signals, writes the data to buffer RAM, and controls the system read of the data out of buffer RAM.

The active lines for reading disk data are diagrammed in Figure 3-15 and are listed with a description in Table 3-12.

Figure 3-15
Reading Disk Data

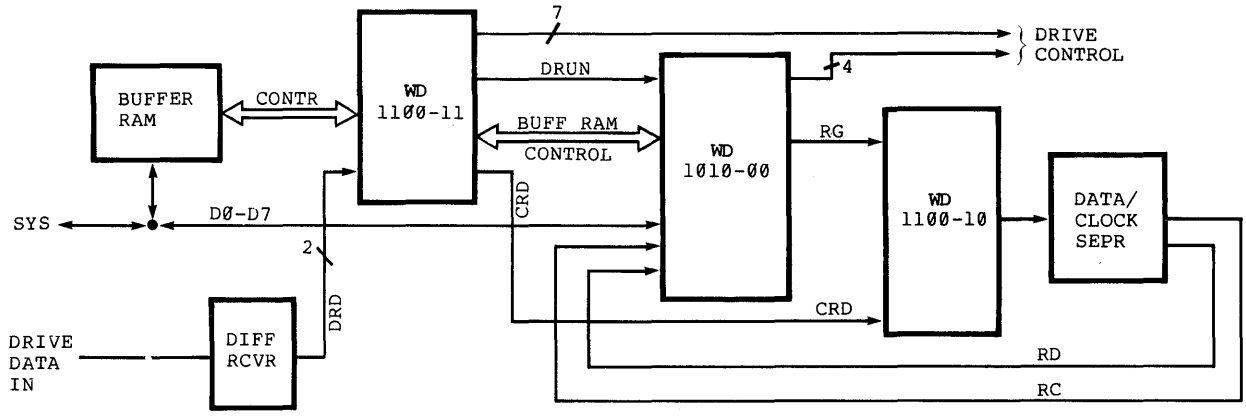


Table 3-12
Disk Data

Active Line	Source/Description
D0 to D7	System. Contains read sector command. When the WD1010-05 receives this command, it checks its cylinder registers against the current cylinder position.
-BCS	WD1010-05. Active to disconnect host control of buffer RAM. Board busy tristate buffer on line WD7 is activated by -BCS to prevent system access during next operation.
-STEP,-DIRET	WD1010-05. Moves head to locate cylinder.
-SEEK COMPLETE	Drive. Informs WD1010-05 that head settling time for ts enter C below and each item

VIDEO SECTION

The major integrated circuits in the video display section include the following:

CRTC	U90
Video gate array	U150
Character generator ROM	U151
Shift register	U143
16K of video display RAM	

The CRTC has several outputs which affect video display operation. Both the vertical and horizontal sync pulses originate at the output of the CRTC. During power up, the CRTC's internal registers are initialized with the proper vertical and horizontal operating frequencies. The vertical sync operates at 60 Hz and the horizontal frequency rate is approximately 16 KHz. Cursor movement is controlled by the cursor output of the CRTC. The CRTC has four output signals RA0-RA3, the scan line count signals, which increment upon completion of each horizontal scan line.

During a display cycle, the CRTC addresses video memory. Latches U112 and U113 are enabled by the DISP CYCLE signal and the addresses are passed to the latch outputs by the CRT LATCH clock. Each character that is displayed occupies two bytes of video memory. One byte represents the character to be displayed while the following memory location stores the attribute of the character. The function of the EVEN/ODD signal is to alternately select either the address of the character or its associated attribute.

The information stored in video memory is passed to both the video gate array and character latch U59. The outputs of the character latch, access the appropriate memory location in the character generator ROM, U151. The TS 1605 employs an 8 x 9 character matrix. Therefore, the scan line count signals to the ROM, reset with the completion of the ninth scan line. Parallel data from the ROM is loaded into the parallel to serial shift register, U143, at the character clock rate of 1.7895 MHz. Data is shifted out of the register by the Dot clock, which is an output of the video gate array. The data is shifted out of U58 serially, at the Dot clock rate of 14.31 MHz. The output of U143 is sent to one of the input lines of the video gate array for processing.

There are many outputs to the video gate array, many of which are not shown in the block diagram. Outputs EG (green voltage), EB (blue voltage), ER (red voltage), and EI (half-intensity video are mixed in a transistor circuit prior to becoming the raw video signal sent to the video module board. Signals I2 (video and color), I3 (horizontal and vertical blanking), and I4 (sync) are mixed in a transistor and sent to a phono jack at the back panel of the TS 1605, as the composite video signal.

During a CPU cycle, video information can either be written into video memory or read from video memory by the CPU. During a CPU cycle it is the CPU that addresses video memory. The signal, CPU CYCLE, enables buffers U110 and U111. The CRTC and CPU cannot address video memory simultaneously.

Video Memory

The CPU performs all writes to video memory, and reads data from video memory to perform graphics formatting. All graphics control firmware is in system ROM and is acted on by the CPU. The CRT controller reads data from video memory to perform screen updates.

The major components of video memory are:

U62,U70,U78, U87,U94,U102, U111,U120	Type 6167 Static RAM devices
U47,U54	CPU Address Buffer

A block diagram of video memory is shown in Figure 3-3.

The video memory components and their description are listed in Table 3-13.

Table 3-13
Video Memory Components

Device or Line	Source/Description
GD0-GD7	CPU. Buffered data lines D0 through D7, carry write data to video memory.
-CPU CYC	CPU. Toggles alpha graphics for the CPU.
XA0-XA7,XA8-XA13	CPU. Buffered address lines to video memory.
DMD0-DMD7	Video memory. Carry read data from video memory.

CRT Controller and Character Generator

The CRT controller retrieves data from the video memory for screen updates. Alphanumeric data from the video memory is passed through a character generator and shifted into a serial bit stream for the video display circuits. Graphics data is sent directly to the shift register. The major components of the CRT controller and character generator are:

U138	Synertek SY6845R CRT Controller
U137	CRT Data Transceiver
U121,U122	CRT Latch
U151	Character Generator ROM
U97	Display Buffer
U150	TeleVideo Video Gate Array
U143	Video Shift Register
Q2,Q3	Video Drivers

A block diagram of the CRT controller and character generator is shown in Figure 3-16.

Figure 3-16
CRT Controller and Video Memory Block Diagram

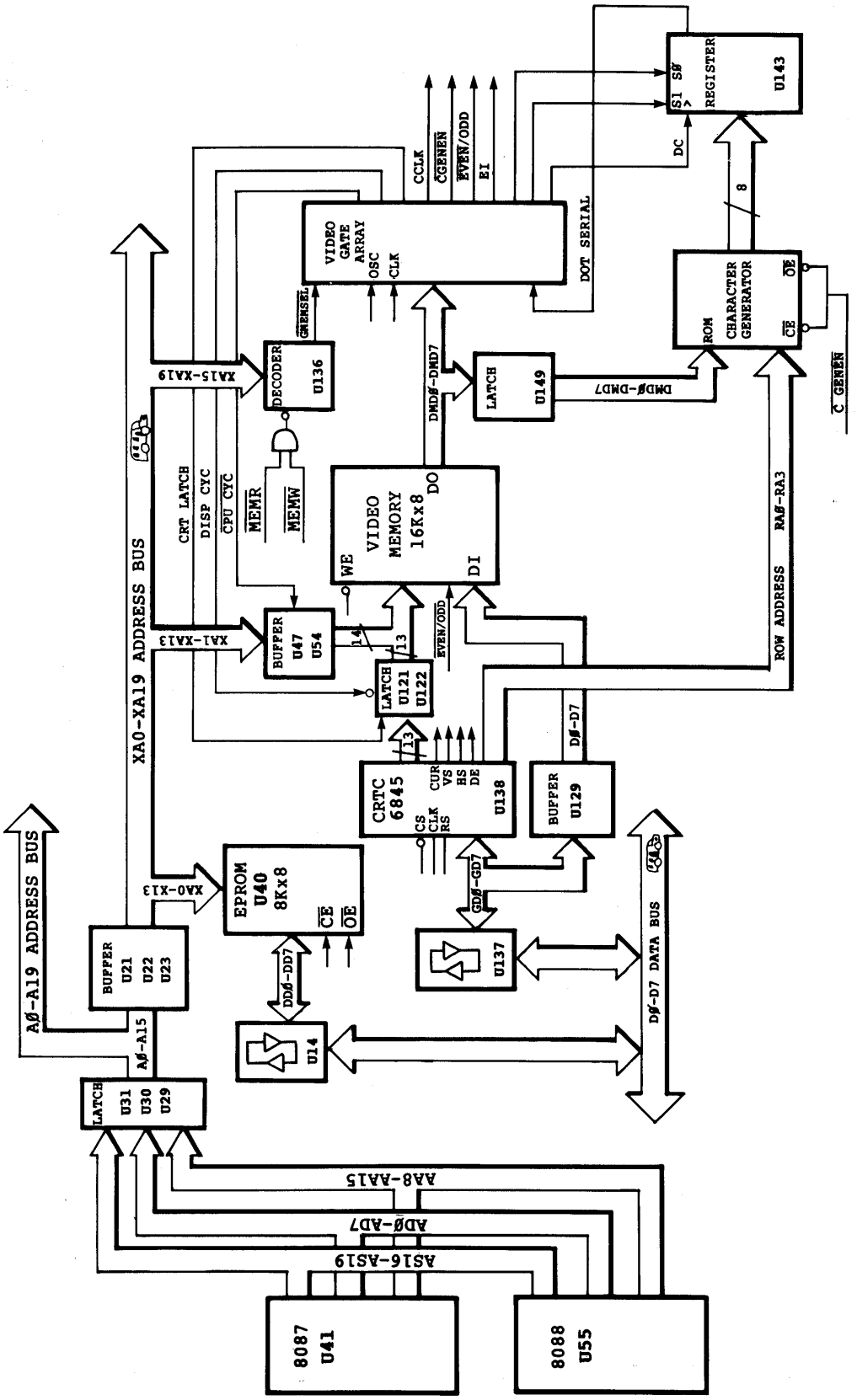


Table 3-14 lists the CRT controller and character generator components and their description.

Table 3-14
CRT Controller and Character Generator Components

Device or Line	Source/Description
CRT Controller	Performs screen updates and generates control signals for video display. Internal registers define and control the raster-scan CRT display.
-DISP CYCLE	CRT controller. Toggles alpha graphics for the CRT.
GD0-GD7	CPU. Buffered data lines D0 through D7, carry write data to the CRT controller.
CRT VS,CRT HS	CRT controller. Vertical and horizontal synchronization signals for video monitor.
CRT CUR	CRT controller. Indicates the position of the graphics cursor.
RA0-RA3	CRT controller. These lines form the address to the character generator.
CRT Latch	Latches address lines MA0 through MA12 of video memory to refresh the screen.
Character Generator ROM	A read-only memory containing two different character fonts. Character size for the high resolution mode is 8 dots x 9 dots. A jumper option, E13, provides a single-dot font or double-dot font in a character size of 8 dots x 9 dots.
Display Buffer	Defines display characters, with each character having a corresponding character attribute. Takes the alpha video bit stream and the character bytes and generates attributes of the screen. The most significant bit of the character determines whether the character is shown blinking or not.
Video Gate Array	Performs all the logic and timing functions of the graphics section. Takes in CPU lines GD0 through GD7 and XA0 through XA2, CPU signals -MEMR, -MEMW, and -GMEMSEL, and lines DMD0 through DMD7 from video memory. Handles screen attributes for the video monitor.

Video Shift Register	Creates the dot serial bit stream from the character generator that is then sent to the video gate array on the DOT SERIAL line. Takes in alpha data and creates a serial bit stream for the video drivers.
Video Drivers	Boost the video signal on the VIDEO line for application to the video monitor. Supports RGB, composite, and monochrome.

VIDEO MODULE

The Video Monitor is made up of two sections: the vertical amplifier and the horizontal amplifier. These amplifiers provide the voltages necessary to drive the CRT yoke, which deflects the electron beam across the CRT.

The electron beam which is generated by the CRT electron gun is swept across and down the screen to create scan lines. The movement of the beam is driven by vertical and horizontal sweep rates. These sweep rates are determined by the display circuitry on the logic board. The horizontal sweep is approximately 16 KHz and the vertical sweep is 60 Hz for domestic and 50 Hz for international applications.

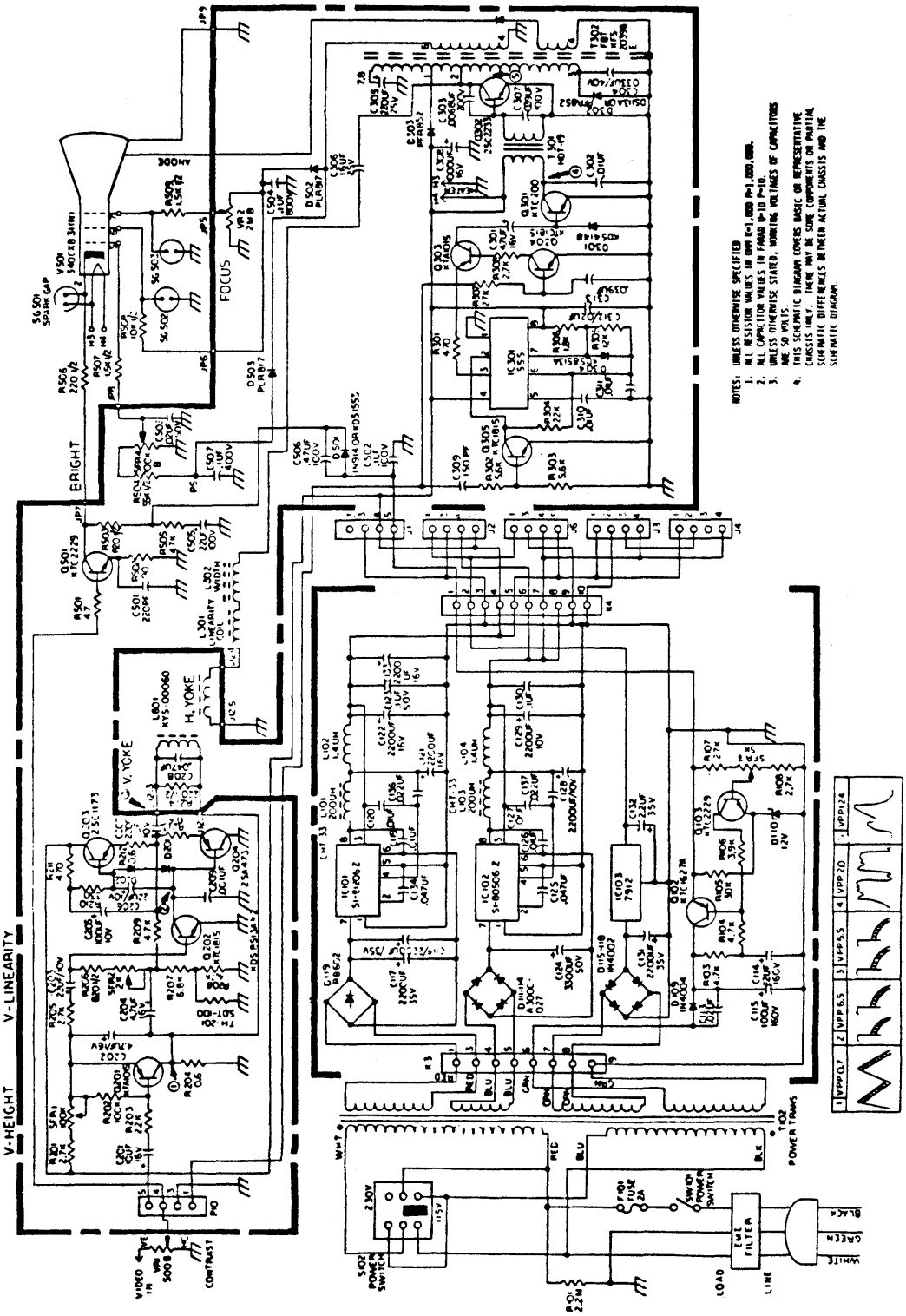
The horizontal sync pulses coming into the Video Monitor are inverted by transistor Q305 and then trigger IC301. In the precision timing mode of operation, the pulse width of IC301 is precisely controlled by R304, R306, and C312. The output of IC301 is then coupled by Q303 and Q301 to drive transformer T301. The output of T301 is amplified by drive transistor Q302. This transistor drives both the horizontal yoke windings and the step-up transformer that produces the anode high voltage and the grid voltage for the CRT grid in the neck of the CRT. A new width coil is used for better raster width control.

The vertical sync pulses come into the Video Monitor and are converted to a sawtooth wave form. The sawtooth pulse goes from a negative leading edge to a positive falling edge and goes through transistor Q202 where it is inverted to its usable form. The pulse now goes from a positive 2 volt leading edge to a negative 2.5 volt falling edge. The timing is critical because within one sawtooth pulse there are 250 horizontal pulses. This is the total number of horizontal scan lines on the CRT. The sawtooth pulse has to be proportional to all of the previous pulses or the timing will be wrong for the vertical sweep and the horizontal sweep.

When the vertical sweep is negative, Q201 conducts and Q202 discharges. During the positive time that C202 is charging, the electron beam is scanning. The vertical sweep scans from top to the bottom. When the scan reaches the bottom of the page, a (blank) occurs, the video beam is turned off, and it is retraced back to the top of the screen, where C202 is now discharging.

After the retrace, the beam is once again turned on and begins its scan routine. Adjusting SFR1 (vertical height) and SFR2 (vertical linearity) changes the rate of charge of C202 thus changing the slope of the sawtooth pulse.

Figure 3-17
Video Monitor



4. HARDWARE PROGRAMMING

This section provides the experienced programmer with the coding tables, command codes, and registers needed to interface with the system hardware.

SYSTEM INTERRUPTS

The programmable interrupt controller provides eight prioritized levels of interrupts with level 0 having the highest priority. The interrupt levels are shown in Table 4-1.

Table 4-1
Hardware Interrupt Listing

Interrupt Level	Input	Type Code	Device
0	IRQ0	%08	Timer channel 0
1	IRQ1	%09	Keyboard
2	IRQ2	%0A	I/O channel
3	IRQ3	%0B	I/O channel
4	IRQ4	%0C	Serial port or I/O channel
5	IRQ5	%0D	Hard disk or I/O channel
6	IRQ6	%0E	Floppy disk or I/O channel
7	IRQ7	%0F	Parallel port or I/O channel

An interrupt source can be disabled by setting the respective bit of the interrupt controller interrupt mask register (%21) to 1.

The other active interrupt controller register is the interrupt-command register at %020. Upon completion of an interrupt service routine, an end of interrupt (EOI) command must be sent to the interrupt control register. The EOI command is represented by the value %20.

PROGRAMMABLE INTERVAL TIMER PROGRAMMING

Each channel of the programmable interval timer contains a 16-bit latch register and a 16-bit counter register. The three access ports (%40-%42) are the least significant bits of the channel latch registers. Each channel also has two input signals (clock and gate) and one output signal (out). The clock inputs of all three channels are tied to a 1.19318-MHz signal and the gate inputs of channels 0 and 1 are tied to a positive high signal (always enabled). The gate for channel 2 is controlled by bit 0 of the programmable peripheral interface device, (PPI) port B at %061.

To place a count value in the count register, the value must be programmed into the latch register and transferred to the count register. The count value is then decremented by one each time a clock pulse is received. When the count register reaches zero, a signal is output on the out line.

The programmable interval timer is programmed by writing a command to the command register (%043) and then reading or writing the appropriate latch register. If both bytes of a latch register need to be accessed, two read or write instructions are needed. The command format is outlined in Table 4-2. The six possible timer modes are described in Table 4-3.

Table 4-2
Timer Command Format

Bits 7	6	5	4	3	2	1	0	
							0	= Decremented in binary format
							1	= Decremented in BCD format
				0	0	0		= Mode 0
				0	0	1		= Mode 1
				0	1	0		= Mode 2
				0	1	1		= Mode 3
				1	0	0		= Mode 4
				1	0	1		= Mode 5
		0	0	= Latch present counter value				
		0	1	= Read/write MSB only				
		1	0	= Read/write LSB only				
		1	1	= Read/write LSB, then MSB				
0	0	= Program channel 0						
0	1	= Program channel 1						
1	1	= Program channel 2						

Table 4-3
Timer Modes

Mode	Description
0	When the latch register is loaded the following occurs: 1. The value is transferred from the latch register to the count register 2. The out signal goes low 3. The counter begins to decrement (if the gate is high) 4. When the count reaches zero, the out signal goes high and remains high 5. The count register continues to decrement below zero
1	When the latch register is loaded the following occurs: 1. The value is transferred from the latch register to the count register 2. The out signal goes low 3. The counter begins to decrement when the gate goes high 4. When the count reaches zero, the out signal goes high and remains high If the gate is dropped low before the count reaches zero, the counting will stop. If the gate is again brought high, the count value is reloaded into the count register (from the latch register) and counting will begin again.
2	When the latch register is loaded the following occurs: 1. The value is transferred from the latch register to the count register 2. The out signal goes high 3. The counter begins to decrement 4. When the counter reaches one, the out signal goes low for one clock period 5. The counter register is reloaded from the latch register and the operation repeats This mode produces a low pulse on the out line for one clock cycle out of every N clock cycles, where N is the value loaded in the latch register.

3 When the latch register is loaded the following occurs:

1. The value is transferred from the latch register to the count register
2. The out signal goes high
3. The counter begins to decrement
4. When the count reaches half of the original count value, the out signal goes low
5. When the count reaches zero, the count value is reloaded into the count register and the operation is repeated

This mode can be used to create a square wave on the out line with the frequency of the clock input signal divided by the value programmed into the latch register.

4 When the latch register is loaded the following occurs:

1. The value is transferred from the latch register to the count register
2. The out signal goes high
3. The counter begins to decrement (if the gate is high)
4. When the count reaches zero, the out signal goes low for one clock cycle and then returns high

5 When the latch register is loaded the following occurs:

1. The value is transferred from the latch register to the count register
2. The out signal goes high
3. The counter begins to decrement when the gate goes high
4. When the count reaches zero, the out signal goes low for one clock cycle and then returns high

If the gate is dropped low before the count reaches zero, the counting stops. If the gate is again brought high, the count value is reloaded into the count register (from the latch register) and counting begins again.

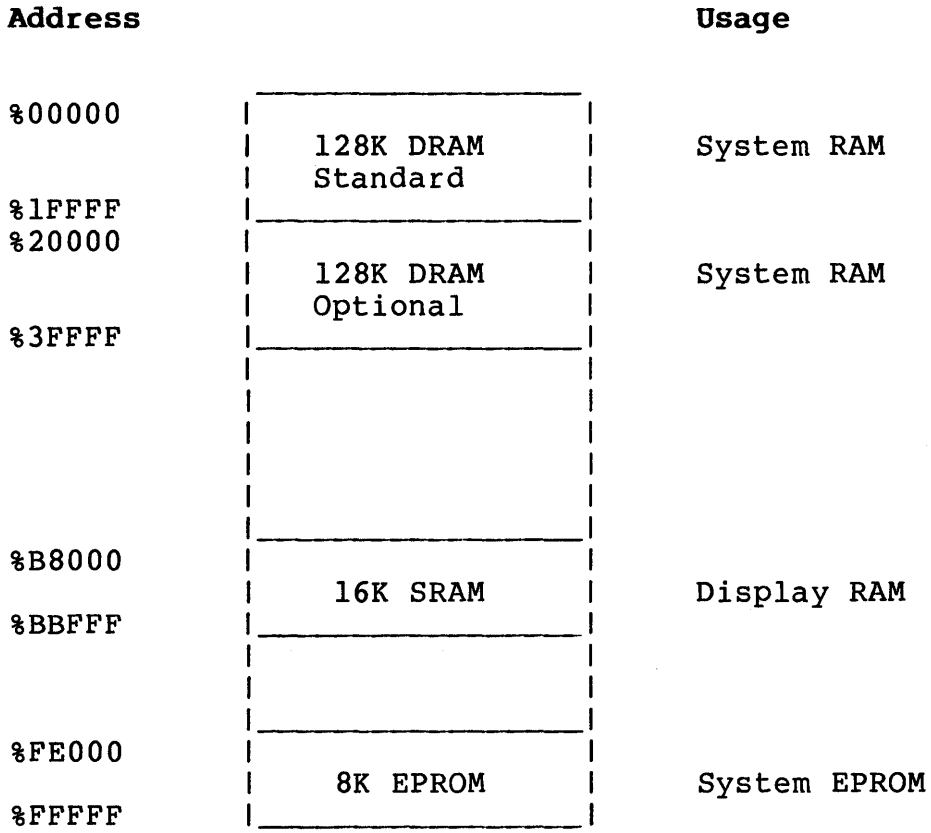
When power is applied to the system, the BIOS initializes channel 0 to operate in mode 3 with a count value of %0000. This results in 65536 counts before zero is reached again. The output is a square wave with a frequency of 18.2 Hz. When the 0 level interrupt is enabled, this output is used by the BIOS for the time-of-day clock.

Timer channel 1 is programmed by the BIOS to operate in mode 2. A count value of 18 is used to send DMA refresh pulses every 15 microseconds.

MEMORY

Both read only memory (ROM) and read/write memory (RAM) are used. An 8-kilobyte EPROM contains the system power-on self-test, the disk drive bootstrap loader, and the I/O drivers. The system read/write memory consists of 128 kilobytes of dynamic memory which can be expanded to 256 kilobytes. The video display uses 16 kilobytes of static read/write memory. Figure 4-1 shows the system memory map.

Figure 4-1
System Memory Map



PROGRAMMABLE PERIPHERAL INTERFACE DEVICE

When power is applied to the system, the BIOS initializes the PPI by sending a value of %99 to the command register at address %063. This configures the PPI so that PA and PC are considered input ports and PB is an output port. Table 4-4 lists the I/O map for the PPI.

Table 4-4
8255A-5 I/O Bit Map

Addr	I/O	Port		Function	
%0060	I	PA	0	+Keyboard Scan Code	0 (PA = Port A)
			1		1
			2		2
			3		3
			4		4
			5		5
			6		6
			7		7
%0061	O	PB	0	+Timer 2 Gate (Speaker)	
			1	+Speaker Data	
			2	Spare	
			3	0 - Read Switches 5-8/1 - Read Switches 1-4	
			4	Spare	
			5	-Enable I/O Channel Check	
			6	-Hold Keyboard Clock Low	
			7	-(Enable Keyboard) or +(Clear Keyboard)	
%0062	I	PC	0	Operation *SW-1	Display Mode SW-5
			1	8087 Installed SW-2 or	Display Mode SW-6
			2	RAM Size SW-3	5 1/4 Drive SW-7
			3	RAM size SW-4	5 1/4 Drive SW-8
			4	Speaker Data	
			5	+Timer Channel 2 Output	
			6	+I/O Channel Check	
			7	Spare (low)	

%0063 Command/Mode Register

Mode Register = %99

* Refer to the system User's Manual for switch settings

NOTE! A plus (+) indicates a bit value of 1 performs the specified function

A minus (-) indicates a bit value of 0 performs the specified function

SPEAKER INTERFACE

The system contains a small speaker, which can be driven from one or both of the following sources:

1. Alternating the value of bit 2 of port B of the PPI.

2. Programming channel 2 of the programmable interval timer.

KEYBOARD

The keyboard is controlled by an Intel 8048 microprocessor. The 8048 performs keyboard scanning, buffering of up to 16-key scan codes, bidirectional communications with the system board, and executes the handshake protocol required by each scan-code transfer.

The keyboard sends scan codes back to the system board as shown in Table 4-5. All keys are typematic and generate a make and break scan code. Break codes are formed by adding %80 to the make code.

Table 4-5
Keyboard Scan Codes

Key	Code Decimal	Code Hex	Key	Code Decimal	Code Hex
Function Keys					
F1	59	%3B	F6	64	%40
F2	60	%3C	F7	65	%41
F3	61	%3D	F8	66	%42
F4	62	%3E	F9	67	%43
F5	63	%3F	F10	68	%44
Alphanumeric Keys					
1	2	%2	A	30	%1E
2	3	%3	S	31	%1F
3	4	%4	D	32	%20
4	5	%5	F	33	%21
5	6	%6	G	34	%22
6	7	%7	H	35	%23
7	8	%8	J	36	%24
8	9	%9	K	37	%25
9	10	%0A	L	38	%26
0	11	%0B	;	39	%27
-	12	%0C	'	40	%28
=	13	%0D	`	41	%29
Q	16	%10	\	43	%2B
W	17	%11	Z	44	%2C
E	18	%12	X	45	%2D
R	19	%13	C	46	%2E
T	20	%14	V	47	%2F
Y	21	%15	B	48	%30
U	22	%16	N	49	%31
I	23	%17	M	50	%32
O	24	%18	,	51	%33
P	25	%19	.	52	%34
[	26	%1A	/	53	%35
]	27	%1B	PrtSc	55	%37
			SPACE BAR	57	%39

Numeric Keypad

7	71	%47	+	78	%4E
8	72	%48	1	79	%4F
9	73	%49	2	80	%50
-	74	%4A	3	81	%51
4	75	%4B	0 (Ins)	82	%52
5	76	%4C	. (Del)	83	%53
6	77	%4D			

Control Characters

Esc	1	%1	Shift (R)	54	%36
Backspace	14	%0E	Alt	56	%38
Tab	15	%0F	Caps Lock	58	%3A
Enter	28	%1C	Num Lock	69	%45
Ctrl	29	%1D	Scroll Lock	70	%46
Shift (L)	42	%2A			

VIDEO SECTION

The video section operates in an alphanumeric mode and a bit-mapped graphics mode.

The alphanumeric mode provides two resolutions. The low-resolution mode is a 40-column by 25-row display using an 8-dots wide by 9-dots high character box and 7 dots x 7 dots with one descender character font. The high-resolution mode is an 80-column by 25-row display with an 8-dots wide by 9-dots high character box and 7 dots x 7 dots with one descender character font. The alphanumeric modes support 256 different character codes (see Appendix D). An 8-kilobyte ROM character generator contains the two different fonts and a jumper option gives a single-dot font or double-dot font in a character size of 8 dots x 9 dots in any alphanumeric mode.

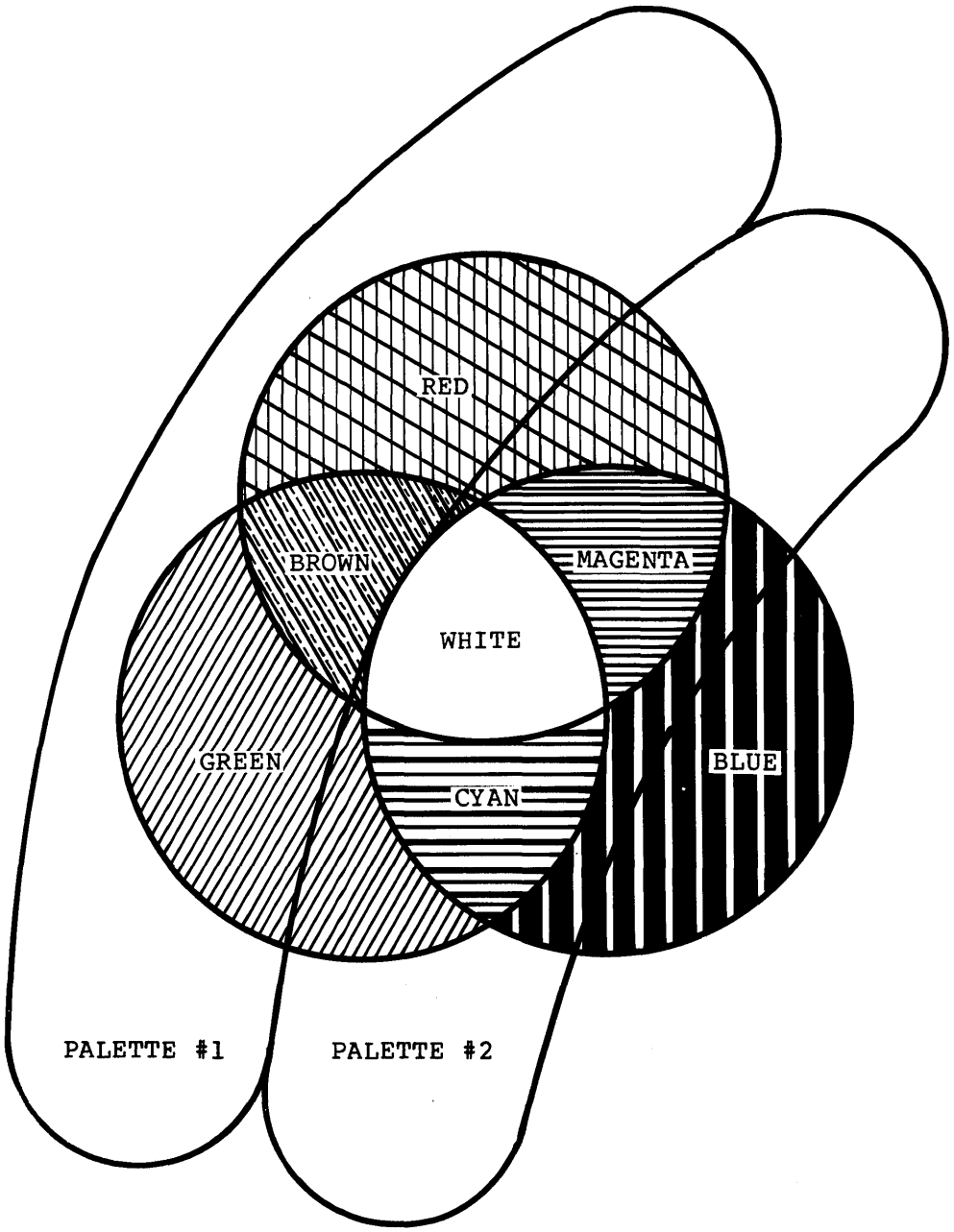
The black-and-white mode provides reverse video, blinking, and highlighting character attributes. The color mode has 16 foreground and eight background colors for each character. Blinking on a per-character basis is also available.

There are 16 kilobytes of static memory used for the display buffer. In the alphanumeric modes, eight screen displays can be stored in the 40 x 25 mode and four screen displays can be stored in the 80 x 25 mode. The start of each display page begins at an even 2- or 4-kilobyte offset and is accessed by changing the offset in the start-address registers.

Two resolutions are provided in the bit-mapped graphics mode; a medium resolution color graphics mode of 320 X 200 pixels and a high resolution black-and-white mode of 640 X 200 pixels.

Each pixel can have one of four colors in the medium-resolution mode. The background color can be one of sixteen colors, with one of two software-selectable palettes providing the three remaining colors. One palette contains red, green, and brown and the other palette contains cyan, magenta, and white, as shown in Figure 4-2. Since both graphics modes require 16 kilobytes of the buffer to define the screen display, the high resolution is available only in black-and-white.

Figure 4-2
Software-Selectable Palettes



Controller Programming

There are nineteen internal registers in the CRT controller that define and control a raster-scan CRT display. The 5-bit, write-only Index register is used as a pointer to the other eighteen registers. This register is loaded from the CPU by executing an OUT instruction to I/O address %3D4.

Any one of the 18 controller registers can be loaded by loading the Index register at %3D4 with the necessary pointer (0-17 decimal) and then loading the Data register with the desired value using an OUT instruction to %3D5. Table 4-6 lists the values that are loaded into the CRT controller registers for controlling the various operational modes.

Table 4-6
CRT Controller Registers

Reg. No.	Register	I/O	40x25 Alpha Hex	80x25 Alpha Hex	Graphics Mode Hex
R0	Horizontal Total	WO	%38	%71	%38
R1	Horizontal Displayed	WO	%28	%50	%28
R2	Horizontal Sync Position	WO	%2D	%59	%2D
R3	Horizontal Sync Width	WO	%0A	%0A	%0A
R4	Vertical Total	WO	%1C	%1C	%7F
R5	Vertical Total Adjust	WO	%01	%01	%06
R6	Vertical Displayed	WO	%19	%19	%64
R7	Vertical Sync Position	WO	%1A	%19	%70
R8	Mode Control	WO	%02	%02	%02
R9	Max. Scan Line Address	WO	%08	%08	%01
R10	Cursor Start	WO	%08	%08	%0
R11	Cursor End	WO	%08	%08	%0
R12	Start Address MSB	WO	%0(Pg 0)	%0(Pg 0)	%0
R13	Start Address LSB	WO	%0(Pg 0)	%0(Pg 0)	%0
R14	Cursor Address MSB	R/W			
R15	Cursor Address LSB	R/W			
R16	Light Pen Address MSB	RO	MA8 - MA13		
R17	Light Pen Address LSB	RO	MA0 - MA7		

NOTE! Addresses in start-address and cursor-address registers are offsets into graphics memory. The CRT controller views these values as offsets into the character positions, ignoring attribute bytes; therefore, the offsets are 1/2 the offset value as viewed by the CPU.

Mode-Select Register

The 6-bit, write-only mode-select register is located at %3D8 and is used to select the video mode. Table 4-7 lists the bit assignments for the mode-select register and Table 4-8 summarizes this register.

Table 4-7
Mode-Select Register

Bit	State	Function
0	0	40 x 25 alphanumeric mode
	1	80 x 25 alphanumeric mode
1	0	Selects alphanumeric mode
	1	Selects 320 x 200 graphics mode
2	0	Selects color mode
	1	Selects black-and-white mode
3	1	Enables the video signal at certain times when modes are being changed (the video signal should be disabled when changing modes)
4	1	Selects 640 x 200 high-resolution black-and-white graphics mode
5	1	Enables blinking attribute in alphanumeric modes

Table 4-8
Mode-Select Register Summary

Bits						
5	**4**	**3**	**2**	**1**	**0**	**Mode Selected**
1	0	1	1	0	0	40 x 25 Alphanumeric Black-and-White
1	0	1	0	0	0	40 x 25 Alphanumeric Color
1	0	1	1	0	1	80 x 25 Alphanumeric Black-and-White
1	0	1	0	0	1	80 x 25 Alphanumeric Color
x	0	1	1	1	0	320 x 200 Black-and-White Graphics
x	0	1	0	1	0	320 x 200 Color Graphics
x	1	1	1	1	0	640 x 200 Black-and-White Graphics

Color-Select Register

The 6-bit, write-only color-select register, located at %3D9 controls the border colors in alpha mode and background colors when in the 320 x 200 graphics mode. Table 4-9 lists the bit assignments for the color-select register.

Table 4-9
Color-Select Register

Bit	Function	MODE 40x25 Alpha	320x200 Graphic	640x200 Graphic
0	Set Blue	Border Color	Background	Foreground
1	Set Green	Border Color	Background	Foreground
2	Set Red	Border Color	Background	Foreground
3	Set Intensity	Border Color	Background	Foreground
4	Set Background Intensity	Background	Intensified Set	
5	Palette Select		0 - red, green, brown 1 - cyan, magenta, white	
6	Not used			
7	Not used			

When bit 5 is set to 0, colors are determined as follows:

C1	C0	Set Selected
0	0	Background, as determined by bits 0-3
0	1	Green
1	0	Red
1	1	Brown

When bit 5 is set to 1, colors are determined as follows:

C1	C0	Set Selected
0	0	Background, as determined by bits 0-3
0	1	Cyan
1	0	Magenta
1	1	White

Status Register

The 4-bit, read-only status register is located at %3DA. Table 4-10 lists the status register bit assignments.

Table 4-10
Status Register

Bit	Function	Description
0	Display Enable	A 1 indicates a display cycle is active.
1	Light Pen	A 1 indicates that a positive going edge of the signal Trigger Set from the light pen has set the light pen's trigger. This trigger is reset upon power-on and may be cleared by performing an I/O OUT command to address %3DB. No specific data setting is required, the action is address-activated.
2	Light Pen	Indicates the status of the light pen switch. A 0 indicates that the switch is on.
3	Vertical Sync	When active, indicates that the raster is in a vertical retrace mode.
4-7	Not used	

Alphanumeric Mode

The alphanumeric mode supports 256 character codes (refer to Appendix D). Each display character is defined by two bytes in the display buffer memory. An even-numbered byte contains the character code and the following odd-numbered byte contains the corresponding character attribute. Table 4-11 lists the bit assignments for the character attribute byte.

Table 4-11
Character Attribute Byte

	Attribute Byte									
	7	6	5	4	3	2	1	0	Background	Foreground
Function	Blk	R	G	B	I	R	G	B	Color	Color
Normal	BL	0	0	0	In	1	1	1	Black	White
Reverse Video	BL	1	1	1	In	0	0	0	White	Black
Blank (Black)	BL	0	0	0	In	0	0	0	Black	Black
Blank (White)	BL	1	1	1	In	1	1	1	White	White

NOTE!
R = Red
G = Green
B = Blue
BL = 1: Blinking, 0: steady
I = Intensity (foreground)
In = 1: Intensity set, 0: normal

Bits 0-3 indicate the foreground color and bits 4-6 indicate the background color. The standard display will produce white characters on a black background with all other foreground/background code combinations. A color monitor will produce the foreground or background colors listed in Table 4-12. The background intensity is set in bit 4 of the color-select register.

Table 4-12
Color Codes

R	G	B	I	Color
0	0	0	0	Black
0	0	1	0	Blue
0	1	0	0	Green
0	1	1	0	Cyan
1	0	0	0	Red
1	0	1	0	Magenta
1	1	0	0	Brown
1	1	1	0	White
0	0	0	1	Gray
0	0	1	1	Light Blue
0	1	0	1	Light Green
0	1	1	1	Light Cyan
1	0	0	1	Light Red
1	0	1	1	Light Magenta
1	1	0	1	Yellow
1	1	1	1	White (High Intensity)

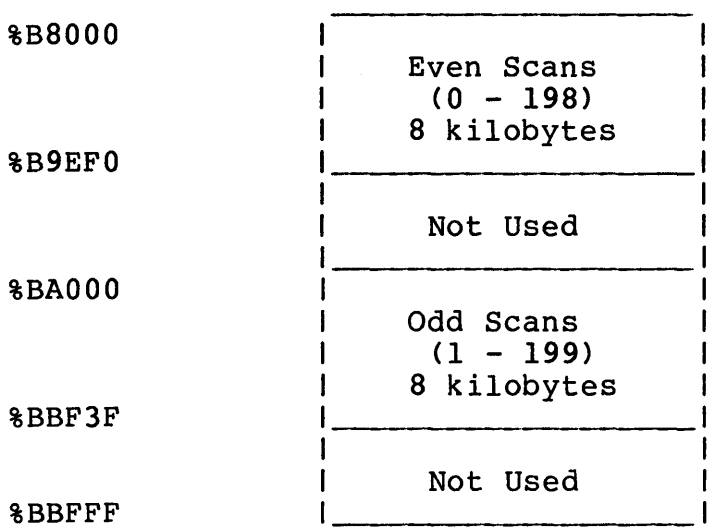
NOTE! Not all RGB monitors recognize the intensity bit.

Graphics Mode

There are two graphics modes: a 320 x 200 pixels medium-resolution color graphics mode and a 640 x 200 pixels high-resolution black-and-white mode. Both modes use memory-mapped graphics and require 16 kilobytes to define the screen.

The graphic information for the screen display is stored in two 8-kilobyte banks as shown in Figure 4-3.

Figure 4-3
Graphic Memory Addresses



In the medium-resolution mode, each byte contains information for four pixels as shown in Table 4-13.

Table 4-13
Medium-Resolution Byte Usage

7 6	5 4	3 2	1 0
C1 C0	C1 C0	C1 C0	C1 C0
First display pixel	Second display pixel	Third display pixel	Fourth display pixel

Each pixel may have one of four colors, while the background color may be one of 16 colors. One of two software-selectable palettes provides the remaining three colors, and are selected by bit 5 of the color-select register. Table 4-14 shows the color selection logic.

Table 4-14
Medium-Resolution Color Selection Logic

C1	C0	Color		
0	0	1 of 16 preselected background colors		
0	1	If palette 1 Green	If palette 2	Cyan
1	0	Red		Magenta
1	1	Brown		White

In the high-resolution black-and-white mode, each bit of a display byte contains the state of one display pixel. Bit 7 corresponds to the first display pixel and bit 0 corresponds to the eighth display pixel.

FLOPPY DISK CONTROLLER

The floppy disk controller (FDC) uses a write only, digital-output register at %3F2 to control drive motors, drive selection, and feature enable. Table 4-15 lists the digital-output register bit assignments.

Table 4-15
Digital-Output Register

```
Bits 7  6  5  4  3  2  1  0
     |  |  |  |  |  |  |  |
     |  |  |  |  |  |  0  0 = Drive A selected
     |  |  |  |  |  |  0  1 = Drive B selected
     |  |  |  |  |  |
     |  |  |  |  |  0 = FDC held reset
     |  |  |  |  |  1 = FDC enabled
     |  |  |  |  |
     |  |  |  |  0 = Interrupt and DMA request I/O driver
     |  |  |  |        disabled
     |  |  |  |  1 = Interrupt and DMA request I/O drive enabled
     |  |  |  |
     |  |  |  0 = Drive A motor off
     |  |  |  1 = Drive A motor on
     |  |  |
     |  |  0 = Drive B motor off
     |  |  1 = Drive B motor on
     |  |
  Not used
```

The FDC has two registers accessible to the CPU: a status register at %3F4 and a data register at %3F5. The status register contains status information on the FDC, as shown in **Table 4-16** and may be accessed at any time. The data register stores data, commands, and parameters and provides floppy disk drive (FDD) status information. Data bytes are read from or written to the data register in order to program or obtain results after a command.

Table 4-16
FDC Status Register
(%3F4)

```
Bit  7  6  5  4  3  2  1  0
     |  |  |  |  |  |  |  |
     |  |  |  |  |  |  |  1 = FDD A is in the seek mode
     |  |  |  |  |  |  |
     |  |  |  |  |  |  1 = FDD B is in the seek mode
     |  |  |  |  |  |
     |  |  |  | not used
     |  |  |  |
     |  |  |  1 = FDC is busy - a read or write command is in
     |  |  |                    progress
     |  |  1 = FDC is in the non-DMA mode
     |  |
     |  0 = Data transfer from CPU to FDC data register
     |  1 = Data transfer from FDC data register to CPU
     |
     1 = Data register is ready to send or receive data
```

The FDC is capable of performing 15 different commands. Commands are initiated by a multi-byte transfer from the CPU. The result after execution of a command may include a multi-byte transfer back to the CPU. Table 4-17 is a summary of the FDC commands. Table 4-18 defines the symbols used in the command table.

Table 4-17
FDC Command Summary

		Data Bus								
Command Phase	**R/W**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Remarks**
					READ DATA					
Command	W	MT	MF	SK	0	0	1	1	0	Command Codes
	W	x	x	x	x	x	HD	US1	US0	
	W				C					Sector ID
	W				H					information
	W				R					prior to
	W				N					command
	W				EOT					execution
	W				GPL					
	W				DTL					

Execution											Data transfer between FDD and system. Status
Result	R					ST0					information
	R					ST1					after command
	R					ST2					execution.
	R					C					Sector ID
	R					H					information
	R					R					after command
	R					N					execution.

READ DELETED DATA

Command	W	MT	MF	SK	0	1	1	0	0		Command Codes
	W	x	x	x	x	x	HD	US1	US0		
	W					C					Sector ID
	W					H					information
	W					R					prior to
	W					N					command
	W					EOT					execution
	W					GPL					
	W					DTL					
Execution											Data transfer between FDD and system. Status
Result	R					ST0					information
	R					ST1					after command
	R					ST2					execution.
	R					C					Sector ID
	R					H					information
	R					R					after command
	R					N					execution.

WRITE DATA

Command	W	MT	MF	0	0	0	1	0	1		Command Codes
	W	x	x	x	x	x	HD	US1	US0		
	W					C					Sector ID
	W					H					information
	W					R					prior to
	W					N					command
	W					EOT					execution
	W					GPL					
	W					DTL					

Execution										Data transfer between FDD and system. Status information
Result	R				ST0					after command execution.
	R				ST1					Sector ID
	R				ST2					information
	R				C					after command
	R				H					execution.
	R				R					
	R				N					

WRITE DELETED DATA

Command	W	MT	MF	0	0	1	0	0	1	Command Codes
	W	x	x	x	x	x	HD	US1	US0	
	W				C					Sector ID
	W				H					information
	W				R					prior to
	W				N					command
	W				EOT					execution
	W				GPL					
	W				DTL					
Execution										Data transfer between FDD and system. Status
Result	R				ST0					ID information
	R				ST1					after command
	R				ST2					execution.
	R				C					Sector ID
	R				H					information
	R				R					after command
	R				N					execution.

READ A TRACK

Command	W	0	MF	SK	0	0	0	1	0	Command Codes
	W	x	x	x	x	x	HD	US1	US0	
	W				C					Sector ID
	W				H					information
	W				R					prior to
	W				N					command
	W				EOT					execution
	W				GPL					
	W				DTL					

Execution			Data transfer between FDD and system. FDC reads all cylinders from index hole to EOT.
Result	R	ST0	Status information after command execution.
	R	ST1	
	R	ST2	
	R	C	Sector ID information after command execution.
	R	H	
	R	R	
	R	N	
Execution			First correct ID information cylinder is stored in data register.
Result	R	ST0	Status information after command execution.
	R	ST1	
	R	ST2	
	R	C	Sector ID information during execution.
	R	H	
	R	R	
	R	N	

FORMAT A TRACK

Command	W	0	MF	0	0	1	1	0	0	Command Codes
	W	x	x	x	x	x	HD	US1	US0	
	W				N					Bytes/Sector
	W				SC					Sector/Track
	W				GPL					Gap 3 filler
	W				D					byte.
Execution										FDC formats an entire cylinder.
Result	R				ST0					Status
	R				ST1					information
	R				ST2					after command
	R				C					execution. In
	R				H					this case, ID
	R				R					information
	R				N					has no meaning.

SCAN EQUAL

Command	W	MT	MF	SK	1	0	0	0	1	Command Codes
	W	x	x	x	x	x	HD	US1	US0	
	W				C					Sector ID
	W				H					information
	W				R					prior to
	W				N					command
	W				EOT					execution
	W				GPL					
	W				DTL					
Execution										Data compared between FDD and system. Status
Result	R				ST0					information
	R				ST1					after command
	R				ST2					execution.
	R				C					Sector ID
	R				H					information
	R				R					after command
	R				N					execution.

SCAN LOW OR EQUAL

Command	W	MT	MF	SK	1	1	0	0	1	Command Codes
	W	x	x	x	x	x	HD	US1	US0	
	W				C					Sector ID
	W				H					information
	W				R					prior to
	W				N					command
	W				EOT					execution
	W				GPL					
	W				DTL					
Execution										Data compared between FDD and system. Status
Result	R				ST0					information
	R				ST1					after command
	R				ST2					execution.
	R				C					Sector ID
	R				H					information
	R				R					after command
	R				N					execution.

SCAN HIGH OR EQUAL

Command	W	MT	MF	SK	1	1	1	0	1	Command Codes
	W	x	x	x	x	x	HD	US1	US0	
	W				C					Sector ID
	W				H					information
	W				R					prior to
	W				N					command
	W				EOT					execution
	W				GPL					
	W				DTL					
Execution										Data compared between FDD and system. Status information
Result	R				ST0					after command
	R				ST1					execution.
	R				ST2					Sector ID
	R				C					information
	R				H					after command
	R				R					execution.
	R				N					

RECALIBRATION

Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	x	x	x	x	x	0	US1	US0	
Execution										Head retracts to track 0.

SENSE INTERRUPT STATUS

Command	W	0	0	0	0	1	0	0	0	Command Codes
Result	R				ST0					Status
	R				PCN					FDC information at end of seek operation

SPECIFY

Command	W	0	0	0	0	0	0	1	1	Command Codes
	W	---SRT--------|-------HUT---								
	W	|------HLT--------------| ND								

SENSE DRIVE STATUS

Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	x	x	x	x	x	HD	US1	US0	
Result	R				ST3					Status FDD information

SEEK

Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	x	x	x	x	x	HD	US1	US0	
	W				NCN					
Execution										Head positioned over proper cylinder on diskette.

INVALID

Command	W	Invalid Codes	Invalid command codes (NoOp-FDC goes into standby state).
Result	R	ST0	ST0 = %80.

Table 4-18
FDC Command Symbols

Symbol	Name	Description
C	Cylinder Number	The current/selected cylinder (track) number.
D	Data	The data pattern that is written into a sector.
D7-D0	Data Bus	8-bit data bus, where D7 stands for the most significant bit and D0 the least significant bit.
DTL	Data Length	When N is defined as 00, DTL stands for data length that users read from or write to the sector.
EOT	End of Track	The final sector number on a cylinder.
GPL	Gap Length	The length of gap 3 (spacing between sectors excluding VCO sync field).
H	Head Address	The head number 0 or 1, as specified in the ID field.
HD	Head	A selected head number 0 or 1. (H=HD in all command words.)
HLT	Head Load Time	The head load time in the FDD (4 to 512 milliseconds in 4-millisecond increments).

HUT	Head Unload Time	The head unload time after a read or write operation has occurred (0 to 480 milliseconds in 32-millisecond increments).
MF	FM or MFM Mode	If MF is low, FM mode is selected. If it is high, MFM mode is selected only if MFM is implemented.
MT	Multi-Track	If MT is high, a multi-track operation is to be performed. (A cylinder under both HD0 and HD1 will be read or written.)
N	Number	The number of data bytes written in a sector.
NCN	New Cylinder	A new cylinder number to define the desired position of the head after the seek operation.
ND	Non-DMA Mode	Operation in the non-DMA mode.
PCN	Present Cylinder	Cylinder number at the completion of sense-interrupt-status command that indicates the position of the head at present time.
R	Record	The sector number to be read or written.
R/W	Read/Write	Either a read or write operation.
SC	Sector	Indicates the number of sectors per cylinder.
SK	Skip	Skip deleted-data address mark.
SRT	Step Rate Time	FDD stepping rate 2 to 32 microseconds (in 2-microsecond increments).
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	One of the four command status registers that store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register. These registers may only be read after a command has been executed and contain information relevant to that particular command.

STP	Scan Test	If STP=1 during a scan operation, the data in contiguous sectors is compared byte-by-byte with data sent from the CPU. If STP=2, then alternate sectors are read and compared.

Command Status Register 0

Bit	Name	Description
US0 US1	Unit Select	Aselecteddrive number encodedthe same as as bits 0 and 1 of the digital-output register.
D0 D1	Unit Select 0 Unit Select 1	Used to indicate a drive unit number at interrupt.
D2	Head Address	Used to indicate the state of the head at interrupt.
D3	Not Ready	This bit is set when the FDD is in the not-ready state and a read or write command is issued.
D4	Equipment Check	This bit is set if a fault is received from the FDD, or if the track 0 signal fails to occur after 77 step pulses (recalibrate command).
D5	Seek End	This bit is set when the FDC completes the seek command.
D6	Interrupt	
D7	Code	

D7	D6	
0	0	Normal termination of command. Command was completed and properly executed.
0	1	Abnormal termination of command. Execution of the command was started, but was not successfully completed.
1	0	Invalid command issue. The command that was issued was never started.
1	1	Abnormal termination because, during execution, the ready signal from the FDD changed states.

Command Status Register 1

Bit	Name	Description

D0	Missing Address	This bit is set if the FDC cannot Mark detect the ID address mark. Note, the missing address mark in the data field of status register 2 is also set.
D1	Not Writeable	This bit is set if the FDC detects a write- protect signal from the FDD during execution of a write data, cylinder command.
D2	No Data	This bit is set if 1) the FDC cannot find the sector specified in the ID register during execution of a read data, write deleted data, or scan command, 2) the FDC cannot read the ID field without an error during execution of the read ID command, or 3) starting sector cannot be found during execution of the read a cylinder command.
D3	Not used	Always set = 0
D4	Over Run	This bit is set if the FDC is not serviced by the main system during data transfers within a certain time interval.
D5	Data Error	This bit is set if the FDC detects a cyclic redundancy check (CRC) error in either the ID field or the data field.
D6	Not used	Always set = 0
D7	End of Cylinder	This bit is set when the FDC tries to access a sector beyond the final sector of a cylinder.

Command Status Register 2

Bit	Name	Description
D0	Missing Address Mark in Data Field	Thisbit is set if the FDC cannot find a data address mark or deleted data address in Data Field when data is read from the medium.
D1	Bad Cylinder	This bit is set when contents of C on the medium are different from that stored in ID register, when contents of C are %FF.

D2	Scan Not Satisfied	This bit is set if FDC cannot find a sector on the cylinder that meets the condition during execution of scan command.
D3	Scan Equal Hit	This bit is set if equal condition is satisfied during execution of scan command.
D4	Wrong Cylinder	This bit is set when the contents of C on the medium are different from that stored in the ID register.
D5	Data Error in Data Field	This bit is set if the FDC detects a CRC error in the data.
D6	Control Mark	This bit is set if the FDC encounters a sector containing a deleted data address mark during execution of read data or scan command.
D7	Not used	Always = 0

Command Status Register 3

Bit	Name	Description
D0	Unit Select 0	The status of the unit-select-0 signal from the FDD.
D1	Unit Select 1	The status of the unit-select-1 signal from the FDD.
D2	Head Address	The status of the side-select signal from the FDD.
D3	Two Side	The status of the two-side signal from the FDD.
D4	Track 0	The status of the track 0 signal from the FDD.
D5	Ready	The status of the ready signal from the FDD.
D6	Write Protect	The status of the write-protected signal from the FDD.
D7	Fault	The status of the fault signal from the FDD.

SERIAL PORT

The WD8250 UART can be programmed to operate from 50 to 9600 baud. Five, six, seven, or eight bit characters with 1, 1-1/2, or 2 stop bits are supported. A fully prioritized interrupt system controls transmit, receive, error, line status, and data set interrupts. Appendix F lists the pin connector assignments for the serial port.

Different modes of operation are selected by initializing the appropriate UART registers. The divisor latch access bit (DLAB), bit 7 of the line-control register, is used to select certain registers. Table 4-19 lists the UART I/O register addresses.

Table 4-19
UART I/O Register Addresses

Address P	Address S	I/O	Register Selected	DLAB State
%3F8	%2F8	O	Transmitting Holding	0 (Write)
%3F8	%2F8	I	Receiver Data Register	0 (Read)
%3F8	%2F8	O	Baud-rate Divisor LSB	1
%3F9	%2F9	O	Baud-rate Divisor MSB	1
%3F9	%2F9	O	Interrupt Enable	0
%3FA	%2FA	I	Interrupt Identification	
%3FB	%2FB	O	Line Control	
%3FC	%2FC	O	Modem Control	
%3FD	%3FD	I	Line Status	
%3FE	%3FE	I	Modem Status	

P = Primary, S = Secondary

The serial port primary adapter uses interrupt line IRQ4. To allow the port to send interrupts to the system, bit 3 of the modem control register must be set high. With bit 3 high, any interrupts allowed by the interrupt enable register will cause an interrupt. A secondary adapter may be utilized with the addition of an optional board.

Line-Control Register

The format of the asynchronous data communication is specified through the line-control register (the contents of this register may be retrieved for inspection). Table 4-20 lists the bit assignment of the line-control register.

Table 4-20
Line-Control Register

Bit	Assignment
0	Character length select bit 0
1	Character length select bit 1
2	Number of stop bits
3	Parity enable
4	Even parity select
5	Stick parity
6	Set break
7	Divisor Latch Access Bit

Bits 0 & 1 These bits set the number of bits in each transmitted transmitted or received serial character. They are encoded as follows:

Bit 1	Bit 0	Character Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2 This bit specifies the number of stop bits as follows:

Bit 2	Character Length	Stop Bits
0	5 - 8	1
1	5	1-1/2
1	6 - 8	2

Bit 3 Parity enable bit. 0 = No parity bit
1 = Parity bit generated

Bit 4 This bit has the following effect:

Bit 4	Bit 3	# of Data bits and parity bit
0	1	Odd number
1	1	Even number

Bit 5 This bit has the following effect:

Bit 5	Bit 4	Bit 3		Parity bit state
1	0	1	=	1
1	1	1	=	0

Bit 6 Set break control bit. When set to 1, the serial output (SOUT) is forced low and remains there regardless of other transmitter activity.

Bit 7 Divisor Latch Access Bit. This bit must be set to 1 to access the divisor latches of the baud rate generator during a read or write operation. This bit must be set to 0 to access the receiver data register, the transmitting holding register, or the interrupt enable register.

Programmable Baud Rate Generator

The UART contains a programmable baud rate generator that is capable of taking the clock input and dividing it by any divisor from 1 to 65,535. The output frequency of the baud rate generator is 16 times the baud rate.

divisor # = input frequency / (baud rate x 16)

Two 8-bit latches store the divisor in a 16-bit format. These divisor latches must be loaded during initialization in order to ensure the desired operation of the baud rate generator. The address bits for the divisor latches are shown in Table 4-21. The divisor baud rates are listed in Table 4-22.

Table 4-21
Divisor Latches

(DLAB=1)	%3F9								%3F8							
Address Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Divisor Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Table 4-22
Divisor Baud Rates

Desired Baud Rate	Divisor Hex	Divisor Decimal
50	%09 00	2304
75	%06 00	1536
110	%04 17	1047
134.5	%03 59	857
150	%03 00	768
300	%01 80	384
600	%00 C0	192
1200	%00 60	96
1800	%00 40	64
2000	%00 3A	58
2400	%00 30	48
3600	%00 20	32
4800	%00 18	24
7200	%00 10	16
9600	%00 0C	12

Line-Status Register

The line-status register provides status information on data transfer. Table 4-23 lists the line-status register bit assignments.

Table 4-23
Line-Status Register
(%3FD or %2FD)

Bit	Assignment
0	Data Ready
1	Overrun error
2	Parity error
3	Framing error
4	Break interrupt
5	Transmitting holding register empty
6	Transmitting shift register empty
7	Set = 0

Bit 0 Data Ready indicator. This bit is set to 1 whenever a complete incoming character has been received and transferred into the receiver buffer register. This bit is reset to 0 either by the CPU reading the data in the receiver buffer register or by writing a logical 0 into it from the CPU.

Bit 1 Overrun error indicator. This bit indicates that data in the receiver buffer register was not read by the CPU before the next character was transferred into the receiver buffer register. This bit is reset whenever the CPU reads the contents of the line status register.

Bit 2 Parity error indicator. This bit indicates that the received data character does not have the correct even or odd parity, as selected by the even parity-select bit. This bit is set to 1 upon detection of a parity error and reset to 0 whenever the CPU reads the contents of the line status register.

Bit 3 Framing error indicator. This bit indicates that the received character did not have a valid stop bit. This bit is set to 1 whenever the stop bit following the last data bit or parity bit is detected as a zero bit.

Bit 4 Break Interrupt indicator. This bit is set to 1 whenever the received data input is held in the 0 state for longer than a full word transmission time.

NOTE! Bits 1-4 are the error conditions that produce a receiver line status interrupt whenever any of the corresponding conditions are detected.

Bit 5 Holding register empty indicator. This bit indicates that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the processor when the transmit holding register empty interrupt enable is set high. Bit 5 is set to 1 when a character is transferred from the transmitter holding register into the transmitter shift register. The bit is reset to 0 when the CPU loads the transmitter holding register.

Bit 6 Transmitter shift register empty. This bit is set to 1 whenever the transmitter shift register is idle. It is reset to 0 upon a data transfer from the transmitter holding register to the transmitter shift register. Bit 6 is a read-only bit.

Bit 7 This bit is set permanently to 0.

Interrupt-Identification Register

The interrupt-identification register is used to indicate that a prioritized interrupt is pending and the type of interrupt. Table 4-24 shows the interrupt-identification register bit assignments and Table 4-25 describes the interrupt control functions.

Table 4-24
Interrupt-Identification Register
(%3FA or %2FA)

Bit	Assignment
0	0 if interrupt pending
1	Interrupt ID bit 0
2	Interrupt ID bit 1
3-7	Set = 0

Bit 0 Indicates whether an interrupt is pending. When set to 1, no interrupt is pending and polling (if used) is continued.

Bit 1 & 2 These two bits identify the highest priority interrupt pending as indicated in **Table 4-25.**

Table 4-25
Interrupt Control Functions

Interrupt ID			Interrupt Set and Reset Functions			
Register Bits			**Priority**	**Interrupt**	**Interrupt**	**Interrupt**
2	**1**	**0**	**Level**	**Type**	**Source**	**Reset Action**
0	0	1		None	None	
1	1	0	First	Received character error (break condition)	Overrun error or Parity error or Framing error or Break interrupt	Read the line-status register
1	0	0	Second	Received data available	Receiver data available	Read the receiver data reg.
0	1	0	Third	Transmitter ready	Transmitter holding reg. empty	Output a character to the transmitter holding register
0	0	0	Fourth	Modem status changed	Clear to send or Data set ready or Ring indicator or Received line	Read the modem status register

Interrupt-Enable Register

The interrupt-enable register is used to enable the four types of interrupts used in the UART. Table 4-26 lists the bit assignments for the interrupt enable register.

Table 4-26
Interrupt-Enable Register
(%3F9 or %2F9 DLAB=0)

Bit	**Assignment**
0	1 = Enable Data Available Interrupt
1	1 = Enable Transmitter Holding Register Empty Interrupt
2	1 = Enable Receive Line Status Interrupt
3	1 = Enable Modem Status Interrupt
4-7	Set = 0

Modem-Control Register

The modem-control register controls the interface with the modem or data set. Table 4-27 lists the bit assignments for the modem control register.

Table 4-27
Modem-Control Register
(%3FC or %2FC)

Bit	Assignment
0	Data Terminal Ready (DTR)
1	Request to Send (RTS)
2	Out 1
3	Out 2
4	Loop
5-7	Set = 0

Bit 0 When this bit is set to 1, the UART -DTR output is forced low (logic 0).

Bit 1 When this bit is set to 1, the UART-RTS output is forced low (logic 0).

Bit 2 When this bit is set to 1, the UART -OUT 1 output is forced low (logic 0). This bit must be set to 1 for the UART to send interrupts to the system bus.

Bit 3 When this bit is set to 1, the UART -OUT 2 output is forced low (logic 0).

Bit 4 This bit provides a loopback feature for diagnostic testing. When set to 1, the following occurs:

1. The transmitter serial output is set low
2. The receiver serial input is disconnected
3. The output of the transmitter shift register is looped back into the receiver shift register input
4. The four modem control inputs are disconnected
5. The four modem control outputs are internally connected to the four modem control inputs

In the diagnostic mode, data that is transmitted is immediately received. This feature allows the CPU to verify the transmit-and receive-data paths of the UART.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The modem-control interrupts are also operational but the interrupt's sources are now the lower four bits of the modem-control register instead of the four modem-control inputs. The interrupts are still controlled by the interrupt-enable register.

Bits 5-7 These bits are permanently set to 0.

Modem-Status Register

The modem-status register provides the current state of the control lines from the modem to the processor. In addition to the current-state information, four bits provide change information. Table 4-28 lists the bit assignments for the modem status register.

Table 4-28
Modem-Status Register
(%3FE or %2FE)

Bit	Assignment
0	Delta Clear to Send
1	Delta Data Set Ready
2	Trailing Edge Ring Indicator
3	Delta Receive Line Signal Detect
4	Clear to Send
5	Data Set Ready
6	Ring Indicator
7	Receive Line Signal Detect

Bit 0 Delta Clear to Send bit. This bit indicates that the UART -CTS input to the device has changed state since the last time it was read by the CPU.

Bit 1 Delta Data Set Ready bit. This bit indicates that the UART -DSR input to the device has changed since the last time it was read by the CPU.

Bit 2 Trailing Edge Ring Indicator bit. This bit indicates that the UART -RI input to the device has changed from an on (logical 1) to an off (logical 0) state.

Bit 3 Delta Receive Line Signal Detect bit. This bit indicates that UART -RLSD input has changed state.

NOTE! Whenever bit 0, 1, 2, or 3 is set to 1, a modem status interrupt is generated.

Bit 4 Clear to Send bit. This bit is the complement of the UART Clear to Send (-CTS) input. If bit 4 (LOOP) of the modem control register is 1, this is equivalent to the Request to Send bit in the modem control register.

Bit 5 Data Set Ready bit. This bit is the complement of the UART Data Set Ready (-DSR) input. If bit 4 (LOOP) of the modem control register is 1, this bit is equivalent to the Data Terminal Ready bit in the modem control register.

Bit 6 Ring Indicator bit. This bit is the complement of the UART Ring Indicator input. If bit 4 (LOOP) of the modem control register is 1, this bit is equivalent to the OUT 1 bit of the modem control register.

Bit 7 Receive Line Signal Detect bit. This bit is the complement of the UART Received Line Signal Detect input. If bit 4 of the modem control register is 1, this bit is equivalent to the OUT 2 bit of the modem control register.

Receiver Data Register

The receiver data register contains the received character as listed in Table 4-29.

Table 4-29
Receiver Data Register
(%3F8 or %2F8 DLAB=0 Read Only)

Bit	Assignment
0	Data bit 0 (least significant bit - first bit received)
1	Data bit 1
2	Data bit 2
3	Data bit 3
4	Data bit 4
5	Data bit 5
6	Data bit 6
7	Data bit 7

Transmitter Holding Register

The transmitter holding register contains the character to be serially transmitted as listed in Table 4-30.

Table 4-30
Transmitter Holding Register
(%3F8 or %2F8 DLAB=0 Write Only)

Bit	Assignment
0	Data bit 0 (least significant bit - first bit transmitted)
1	Data bit 1
2	Data bit 2
3	Data bit 3
4	Data bit 4
5	Data bit 5
6	Data bit 6
7	Data bit 7

PARALLEL PORT

The parallel port uses three ports for data transfer and control. Tables 4-31, 4-32, and 4-33 list the three I/O ports, their addresses, and bit assignments.

Table 4-31
Data Output Port
(%3BC)

Bit	Signal	Pin #
0	Data 0	2
1	Data 1	3
2	Data 2	4
3	Data 3	5
4	Data 4	6
5	Data 5	7
6	Data 6	8
7	Data 7	9

Table 4-32
Output Control Port
(%3BE)

```
Pin                17 16 14 1
Bit  7  6  5  4  3  2  1  0
     |  |  |  |  |  |  |  |
     not used |  |  |  |  0 = Normal setting
              |  |  |  |  1 = Pulse bit to 1 to output data to
              |  |  |  |      printer
              |  |  |  |
              |  |  |  0 = No auto line feed (normal setting)
              |  |  |  1 = Auto line feed after carriage return
              |  |  |
              |  |  0 = Pulse bit must be set low for at least
              |  |      50 microseconds to initialize printer
              |  |  1 = Normal operation
              |  |
              |  1 = To allow printer to read output
              |
              0 = Printer interrupt disabled
              1 = IRQ7 interrupt enabled on printer Acknowledge
                  signal pulse
```

Table 4-33
Control Signal Input Port
(%3BD)

```
Pin  11 10 12 13 15
Bit  7  6  5  4  3  2  1  0
     |  |  |  |  |  |  |  |
     |  |  |  |  |  not used
     |  |  |  |  |
     |  |  |  |  0 = Printer error
     |  |  |  |  1 = Printer normal
     |  |  |  |
     |  |  |  0 = Printer not on line
     |  |  |  1 = Printer on line
     |  |  |
     |  |  0 = Printer has paper
     |  |  1 = Printer out of paper
     |  |
     |  0 = Acknowledge pulse
     |  1 = Normal input
     |
     0 = Printer busy, do not send data
     1 = Printer not busy, send data
```

Once the printer is initialized, data can be output using the following steps:

1. Send a data character to the data output port (%3BC).

2. Check the printer status by reading the control-signal input port (%3BD). Note, bit 7 must be set to 1 before data can be strobed into the printer.

3. When the printer is ready, pulse bit 1 of the output-control port to 1 and then reset it to 0. Note, bit 3 must be set to 1 for the printer to read the data character.

4. When the printer has processed the data character, it sends back an acknowledge signal by pulsing bit 6 of the control-signal input port low. The procedure is then repeated for the next data character.

I/O CHANNEL

The I/O channel provides data bus lines, address bus lines, interrupt lines, DMA control lines, and power and ground lines. These lines and signals are described in Table 4-34.

Table 4-34
I/O Channel Signals

Signal Name	I/O	Description
Address Bits	O	Lines A0 through A19 address system memory and I/O devices, allowing access of up to 1 megabyte of memory. A0 is the least-significant bit and A19 is the most-significant bit. Active high, these lines are addressed by the CPU or DMA.
Address Enable	O	The Address Enable line disables the CPU and other devices from the I/O channel for DMA transfers. The DMA controls address and data lines and read/write command lines when this line is active high.
Address Latch Enable	O	Provided bythe bus controller, Address Latch Enable latches valid CPU addresses. When used with Address Enable, it indicates a valid address to the I/O channel. CPU addresses are latched with falling edge of Address Latch Enable.
Data Acknowledge	O	Active low, these lines acknowledge DMA requests and refresh system dynamic memory.

Data Bits	I/O	Lines D0 through D7 provide data bus bits for the CPU, memory, and I/O devices. Active high, D0 is the least significant bit and D7 is the most significant bit.
Data Request	I	The peripheral devices use these asynchronous channel requests to gain DMA service. Request 1 is prioritized as the highest and request 3 as the lowest. A request is initiated by making a request line active high and holding it high until the corresponding data acknowledge line goes active.
Interrupt Request	I	Whenan I/O device needs attention, Interrupt Request lines signal the CPU. Request 2 is prioritized as the highest and request 7 as the lowest. An interrupt request is initiated by raising the interrupt request line from low to high and holding it high until it is acknowledged by the CPU.
I/O Channel Check	I	The I/O Channel line provides the CPU with parity information on I/O channel devices. A parity error is indicated by an active low signal.
I/O Channel Ready	I	I/O cycles are lengthened by an I/O device pulling the I/O channel line low, which allows slower devices to be easily attached to the I/O channel. When a slow device uses this line, it immediately drives it low as it detects a valid address and a read or write command. This line is held no longer than 10 clock cycles.
I/O Read	O	Input/Output Read command line instructs an I/O device to drive its data onto the data bus. This active low line may be driven by the CPU or DMA.
I/O Reset	O	I/O Reset signal initilizes or resets system logic upon power-up or a low line voltage outage. This active high signal is synchronized to the falling edge of clock.
I/O Write	O	Input/Output Write command signal instructs an I/O device to read data on the data bus. It may be driven by the CPU or the DMA and is active low.
Memory Read	O	Memory Read command signal instructs memory to drive its data onto the data bus. This active low line may be driven by the CPU or the DMA.

Memory Write	O	Memory Write command signal instructs the memory to store the data on the data bus. This active low line may be driven by the CPU or the DMA.
Oscillator	O	The oscillator is a high speed clock with a 70-nanosecond period (14.31818 MHz) and a duty cycle of 50%.
System Clock	O	The system clock is a divide-by-three of the oscillator with a 210-nanosecond period and a duty cycle of 33%.
Terminal Count	O	Active high, this line provides a pulse when the terminal count for a DMA channel is reached.

WINCHESTER DISK CONTROLLER BOARD

The Winchester disk controller board contains a WD1010-05 Winchester disk controller device to perform executive control over disk operations. To command the board, the system addresses a set of task file registers in the WD1010-05 with the I/O port address of each of the individual registers. Table 4-35 is a list of the individual registers, along with their I/O port addresses for the TS 1605H:

Table 4-35
TS 1605 Registers

Address	Read	Write
%0020	System Access	System Access
%0021	Error Flags	Write Precomp Cylinder
%0022	Sector Count	Sector Count
%0023	Sector Number	Sector Number
%0024	Cylinder Low	Cylinder Low
%0025	Cylinder High	Cylinder High
%0026	Sector/Drive/Head	Sector/Drive/Head
%0027	Status Register	Command Register

A detailed description of the WD1010-05 device is given in the referenced Western Digital documentation.

Task File Register Functions

For a typical operation, the task file registers are written to or read for status, and a command is given to the command register. The WD1010-05 then tri-states the address bus and executes the command. At the end of the operation, the task file is again opened to the system.

Error Register. Contains error flags for bad block detect, CRC data field, ID not found, aborted command, TK0000 error, and data address mark error. During read operations, the error register is read after the data is read out of buffer RAM, that is, after the byte count goes to zero. The error register bit assignments are listed in Table 4-36.

Table 4-36
Error Register Bit Assignments

Bit	Description
0	This bit is set during a read sector command if the address mark is not found after the proper sector ID is read.
1	This bit is set only by the restore command. It indicates that the head is not positioned over track 000 after 1024 stepping pulses.
2	This bit is set if a command was issued while the status register shows a drive fault (bit 5), or command disable (bit 6) condition. This bit is also set if an undefined command is issued.
4	This bit is set when the desired cylinder, head, sector, or size parameter cannot be found after 8 revolutions of the disk. This bit is also set if a cyclic redundancy check error has occurred.
6	This bit is set if a data field CRC error has occurred or the data mark address has not been found.
7	This bit is set if an ID field has been encountered that contains a bad block mark (used for bad sector mapping).

Write Precomp. Defines the starting cylinder number at which reduced write current (RWC) begins. This value is in the range 0 to 255, and is internally multiplied by four to obtain the actual cylinder.

Sector Count. Contains the number of sectors that are to be transferred to buffer RAM. Because this is a decrementing function, all zeros are written for a 256-sector transfer and a 1 is written for a one-sector transfer.

Sector Number. Contains the starting sector of a transfer in the range 0 to 255. This register is incremented with every transfer.

Cylinder Number Low. Least significant eight bits of the starting cylinder number in the range 0 through 1023.

Cylinder Number High. Carries the most significant bits of the starting cylinder number as bits 0(8) and 1(9). The other bits of this register are unused.

Sector/Drive/Head Register. Contains the sector size, drive number, and head number parameters for the operation:

```
Bit  7  6  5  4  3  2  1  0
     |  |  |  |  |  |  |  |
     |  |  |  |  |  0  0  0 = Select head 0
     |  |  |  |  |  0  0  1 = Select head 1
     |  |  |  |  |  0  0  1 = Select head 1
     |  |  |  |  |  0  0  1 = Select head 1
     |  |  |  |  |  1  1  1 = Select head 7
     |  |  |  |  |
     |  |  |  0  0 = Select drive 1
     |  |  |  0  1 = Select drive 2
     |  |  |  1  0 = Select drive 3
     |  |  |  1  1 = Select drive 4
     |  |  |
     |  0  0 = Sector size 256
     |  0  1 = Sector size 512
     |  1  0 = Sector size 1024
     |  1  1 = Sector size 128
     |  = Extension bit
```

Bit 7 is an extension bit that extends the data field by seven bytes when ECC codes are used. When set to 1, CRC is not appended to the end of the data field; the data field becomes sector size + 7 bytes long.

The SDH byte written into the ID field is different than the SDH register contents. The recorded SDH byte does not have the drive number written and contains a bad block in bit 7.

Status Register. Contains status bits for device busy, device ready, write fault (same as WF line), seek complete (same as SC line), data request (same as BDRQ line), command in progress, and error register flags set.

Bit Description

0 This bit is set whenever any bits in the error register are set. This bit is reset when a new command is written into the command register.

1 When this bit is set, a command is being executed and a new command should not be loaded.

3 This bit is set when the sector buffer should be loaded or read (depending on the command). It is reset upon completion of the operation.

4 This bit is set during a seek, and reset when the head settling time has expired.

5 This bit indicates a fault condition at the drive when set. An interrupt is generated when this bit is set.

6 This bit must be set for commands to execute.

7 This bit is set whenever the disk is being accessed. Commands should not be loaded into the command register when this bit is set. This bit is reset at the end of all commands except the read sector command. This bit is reset after the sector buffer is filled on the read sector command.

Command Register. This write-only register is used to load the desired command. A command begins to execute immediately upon loading. This register should not be loaded while bits 1 or 7 are set in the status register.

The command set consists of six commands, as shown in Table 4-37. Prior to loading a command, the task file registers must be set with the proper parameters. Except for the command register, the task file registers can be loaded in any order.

RESTORE - Restore heads. The restore command is usually used on a power-up condition. The head is stepped back to track 000. If after 1024 stepping pulses, the head is not over track 000, bit 1 of the error flag is set. The stepping rate used is determined by the head settling time. The rate entered into the rate field of the restore command is stored in an internal register and used in future commands with implied seeks (the default stepping rate is 7.5 ms.)

SEEK - For seek operations between multiple drives. Since all commands feature an implied seek, the seek command is primarily used for overlap seek operations on multiple drives. The rate field step rate is used and then stored in an internal register for future use. The direction and number of step pulses needed

Table 4-37
Command Register Format

Command	7	6	5	4	3	2	1	0
Restore	0	0	0	1	R3	R2	R1	R0
Seek	0	1	1	1	R3	R2	R1	R0
Read sector	0	0	1	0	I	M	0	0
Write sector	0	0	1	1	0	M	0	0
Scan ID	0	1	0	0	0	0	0	0
Write format	0	1	0	1	0	0	0	0

Notes:

1. R0 through R3 is the rate field:

R3	R2	R1	R0	
0	0	0	0	= approx. 35 microseconds
0	0	0	1	= 0.5 milliseconds
0	0	1	0	= 1.0 milliseconds
0	0	1	1	= 1.5 milliseconds
0	1	0	0	= 2.0 milliseconds
0	1	0	1	= 2.5 milliseconds
0	1	1	0	= 3.0 milliseconds
0	1	1	1	= 3.5 milliseconds
1	0	0	0	= 4.0 milliseconds
1	0	0	1	= 4.5 milliseconds
1	0	1	0	= 5.0 milliseconds
1	0	1	1	= 5.5 milliseconds
1	1	0	0	= 6.0 milliseconds
1	1	0	1	= 6.5 milliseconds
1	1	1	0	= 7.0 milliseconds
1	1	1	1	= 7.5 milliseconds

2. M is the multiple sector flag: 0 = transfer 1 sector
   1 = transfer multiple sectors

3. When limited RAM buffer size does not allow multiple sector operations, M must be set to 0.

4. I is the interrupt enable:

   0 = set interrupt when bit 3 of the status register is set (sector buffer is ready to be loaded or read)
   1 = set interrupt upon completion of command

   The value is calculated by comparing the contents of the cylinder high/low registers to the cylinder position number stored internally. After all steps have been issued, the command is terminated.

READ SECTOR - Transfers one or more sectors to disk. The following programming sequence should be used with the read sector command:

a. Check the status of the Busy bit (bit 7) of the status register until a reset condition is found.

b. Write to the task file registers with the transfer parameters:

   Precomp reg = Desired precomp start track/4
   Sector count = 1
   Sector number = Sector number to read
   Cylinder high/low = Desired cylinder number
   SDH = Desired sector size, drive number, and head number

c. Send the read sector command to the command register

d. Delay 1 or 2 NOP instructions

e. Check the status of the Busy bit (bit 7) of the status register until a reset condition is found.

f. Read the data buffer (total number of bytes is equal to the sector size).

g. Read the status register and check the error bit (bit 0).

h. If the error bit is set, read the error register for error information.

WRITE SECTOR - Writes one or more sectors to disk. The following programming sequence should be used with the write command:

a. Check the status of the Busy bit (bit 7) of the status register until a reset condition is found.

b. Write to the task file registers with the transfer parameters:

Precomp reg = Desired precomp start track/4
Sector count = 1
Sector number = Sector number to write
Cylinder high/low = Desired cylinder number
SDH = Desired sector size, drive number, and head number

c. Send the write command to the command register.

d. Write a sector of data to data buffer.

e. Delay 1 or 2 NOP instructions.

f. Check the status of the Busy bit Register (bit 7) of the status register until a reset condition is found.

g. Re-read the status register and check the error bit (bit 0).

h. If the error bit is set, read the error register for error information.

SCAN ID - Updates the head, sector size, sector number, and cylinder registers. The internal cylinder position is also updated. This operation is used for multiple drives for an implied seek.

WRITE FORMAT - Used to format a single track using the task file and sector buffer. The sector buffer is used for additional parameter information instead of sector data. The following programming sequence should be used with the write format command:

a. Check the status of the Busy bit (bit 7) of the status register until a reset condition is found.

b. Write to the task file registers with the transfer parameters:

Precomp reg = Desired precomp start track/4
Sector count = Number of sectors to be formatted.
Sector number = Number of bytes minus three to be used for Gap 1 and Gap 3. Gap 3 is determined as follows:

Gap 3 = 2 * M * S + K + E

where: M = motor speed variation (.03 for +-3%)
S = sector length in bytes
K = 25 for an interleave factor of 1
0 for any other interleave factor
E = 7 if the sector is to be extended

Cylinder high/low = Desired cylinder number
SDH = Desired sector size, drive number, and head number (set extension = 0)

c. Send the write format command to the command register.

d. Fill the interleave table in the sector buffer. Each sector to be formatted requires a two-byte sequence. The first byte indicates whether a bad block mark is to be recorded in the sector's ID field. A 80H indicates a bad block mark for that sector, a 00H is normal. The second byte indicates the logical sector number to be recorded. Using this scheme, sectors may be recorded in any interleave factor desired. The remaining memory in the sector buffer may be filled with any value (but must be filled with one sector size worth of data).

e. Delay 1 or 2 NOP instructions.

f. Check the status of the Busy bit (bit 7) of the status register until a reset condition is found.

g. Re-read the status register and check the error bit (bit 0).

h. If the error bit is set, read the error register for error information.

5. ROM BIOS AND SYSTEM USAGE

This chapter explains how the assembly language programmer can use the basic input/output system (BIOS) to perform block (diskette and disk) or character-level operations.

ROM BIOS

Located in system ROM, BIOS provides device level control for the major I/O devices. BIOS routines are accessed through CPU interrupts. Table 5-1 is a listing of the interrupt vectors.

Table 5-1
Interrupt Vectors

Interrupt Number		Name	Initialized by
%0	8088	Divide by zero	DOS
%1	Interrupt	Single step	DOS
%2	Vectors	Nonmaskable	BIOS
%3		Breakpoint	DOS
%4		Overflow	DOS
%5		Print screen	BIOS
%6		Not used	
%7		Not used	
%8	Interrupt	Time of day	BIOS
%9	Controller	Keyboard	BIOS
%A	Interrupt	Not used	
%B	Vectors	Not used	
%C		Communications	BIOS
%D		Disk	BIOS
%E		Diskette	BIOS
%F		Printer	BIOS
%10	BIOS	Video	BIOS
%11	Entry	Equipment Check	BIOS
%12	Points	Memory	BIOS
%13		Diskette/Disk	BIOS
%14		Communications	BIOS
%15		Reserved	BIOS
%16		Keyboard	BIOS
%17		Printer	BIOS
%18		Reserved	BIOS
%19		Bootstrap	BIOS
%1A		Time of day	BIOS
%1B	User	Keyboard break	DOS
%1C	Supplied	Timer tick	BIOS

%1D	BIOS	Video initialization	BIOS
%1E	Parameters	Diskette parameters	BIOS
%1F		Video graphics characters	BIOS

An interrupt routine is called by using the INT opcode with the interrupt number as the operand. All parameters passed to and from the BIOS routines are transferred through the CPU registers. The BIOS routines normally save all registers except for AH/AL and the flags. Other registers are modified on return only if they are returning a value to the caller. If a BIOS function has several possible operations, the AH register is used at input to indicate the desired operation.

The following sections describe the BIOS entry point interrupt routines.

Video I/O - Interrupt %10

This routine interfaces with the CRT, providing the following functions:

```
AH = 0    AL = 0    40x25 Black-and-white
          AL = 1    40x25 Color
          AL = 2    80x25 Black-and-white
          AL = 3    80x25 Color
          AL = 4    320x200 Color
          AL = 5    320x200 Black-and-white
          AL = 6    640x200 Black-and-white

AH = 1    Set cursor type
          CH =      Start line for cursor in bits 0-4 (0-8 valid)
                    (Erratic blinking or no cursor results when
                    bits 5 or 6 are set.)
          CL =      End line of cursor in bits 0-4 (0-8 valid)

AH = 2    Set cursor position
          DH,DL = Row, column: 0,0 is upper left corner
          BH = Display page number (0 for graphics modes)

AH = 3    Read cursor position
          BH = Display page number (0 for graphics modes)
          On exit, DH,DL = Row, column of current cursor
                   CH,CL = Currently set cursor mode

H = 4     Read light pen position
          On exit, AH = 0      Light pen switch not down/not
                               triggered
                   AH = 1      Valid light pen value in registers
                          DH,DL =    Character light pen
                                     position row, column
                          CH = Raster line, 0 - 199
                          BX = Pixel column, 0 - 319 or 619
```

AH = 5 Select active display page for alphanumeric modes
AL = New page value: 0-7 for modes 0 and 1, 0-3 for modes 2 and 3

AH = 6 Scroll up active page
AL = Number of input lines blanked at window bottom
AL = 0: entire window is blanked
CH,CL = Row, column of upper left scroll corner
DH,DL = Row, column of lower right scroll corner
BH = Blank line attribute

AH = 7 Scroll down active page
AL = Number of input lines blanked at window top
AL = 0: entire window is blanked
CH,CL = Row, column of upper left scroll corner
DH,DL = Row, column of lower right scroll corner
BH = Blank line attribute

Character Handling Routines

AH = 8 Read attribute/character at current cursor position
BH = Display page for alphanumeric modes
On exit, AL = Character read
AH = Character attribute

AH = 9 Write attribute/character at current cursor position
BH = Display page for alphanumeric modes
CX = Count of characters to write
AL = Character to write
BL = Character attribute

AH = 10 Write character only at current cursor position
BH = Display page for alphanumeric modes
CX = Count of characters to write
AL = Character to write

Graphics Interface Routines

AH = 11 Set color palette
BH = Palette color ID being set, 0-127
BL = Color value used with color ID
Color ID = 0 selects background color, 0-15
Color ID = 1 selects palette:

0 = Green: 1 | Red: 2 | Blue: 3
1 = Cyan: 1 | Magenta: 2 | White: 3

Value 0-31 indicates the border color used for palette color 0 in 40x25 or 80x25 alphanumeric modes.

```
AH = 12   Write dot
          DX = Row number
          CX = Column number
          AL = Color value (If bit 7 of AL = 1, the color value
               is exclusive OR'd with the current contents of the
               dot

AH = 13   Read dot
          DX = Row number
          CX = Column number
          AL = Returns dot read
```

Equipment Check - Interrupt %11

This routine determines, when possible, the optional devices to be attached to the system.

```
Input     No registers

Output    AX is set, indicating attached I/O

          Bits 15,14 = Number of attached printers
          Bit 13 is not used
          Bit 12 is not used
          Bits 11,10,9 = Number of RS-232C ports
          Bit 8 is not used
          Bits 7,6 = Number of diskette drives
                     0,0 = 1
                     0,1 = 2
          Bits 5,4 = Initial video mode
                     0,1 = 40 x 25 BW
                     1,0 = 80 x 25 BW
          Bits 3,2 = RAM size
                     Always 1,1
          Bit 1 is not used
          Bit 0 = IPL from diskette,indicating diskette drives
                  are in the system.)
```

Memory - Interrupt %12

Memory quantity in the system is determined by this routine, as represented on the rear panel of the computer by switch SW.

```
Input     No registers

Output    AX = Number of contiguous 1 kilobyte memory blocks
```

Diskette I/O - Interrupt %13

This routine accesses the 5 1/4-inch diskette drives.

```
Input     AH = 0    Reset diskette system
          AH = 1    Read the system status into AL
```

Registers for Read/Write/Verify/Format

DL = Drive number (0-1 allowed, value checked)
DH = Head number (0-1 allowed, not value checked)
CH = Track number (0-39, not value checked)
CL = Sectornumber (1-8, not value checked,not used for format)
AL = Number of sectors (Max = 8, not value checked, not used for format)
ES:BX = Buffer address (not required for verify)

AH = 2 Read the desired sectors into memory

AH = 3 Write the desired sectors from memory

AH = 4 Verify the desired sectors

AH = 5 Format the desired track
The buffer pointer, ES:BX, points to the collection of desired address fields for the track during the format operation. There are 4 bytes in each field (C,H,R,N). C = track number, H = head number, R = sector number, and N = number of bytes per sector (00=128, 01=256, 02= 512, 03=1024). An entry is required for every sector on the track to find the requested sector during read/write access.

Output AH = Operation status
80 = Attachment failed to respond
40 = Seek operation failed
20 = Controller has failed
10 = Bad CRC on diskette read
09 = Attempt to DMA across 64 kilobyte boundary
08 = DMA overrun on operation
04 = Requested sector not found
03 = Write attempted on write-protected disk
02 = Address mark not found
01 = Bad command passed to diskette I/O

CY = 0 Successful operation (AH = 0 on return)
CY = 1 Failed operation (AH has error reason)

For Read/Write/Verify
DS,BX,DX,CH,CL preserved
AL = Number of sectors actually read (may not be correct if time out error occurs)

Fixed Disk I/O - Interrupt %13

This routine accesses the 5 1/4-inch fixed disk through the Winchester disk controller board (TS 1605H).

Input AH = Hex value
- = %00 Reset disk (DL = %80, %81)/diskette
- = %01 Read status of the last disk operation into AL
  DL < %80 - Diskette
  DL > %80 - Disk
- = %02 Read the desired sectors into memory
- = %03 Write the desired sectors from memory
- = %04 Verify the desired sectors
- = %05 Format the desired track
- = %06 Format the desired track and set bad sector flags
- = %07 Format the drive starting at the desired track
- = %08 Return the current drive parameters
- = %09 Initialize drive pair characteristics
  Interrupt %41 points to data block
- = %0A Read long
- = %0B Write long
  Note: Read and write long encompass 512 + 4 bytes ECC
- = %0C Seek
- = %0D Alternate disk reset
- = %0E Read sector buffer
- = %0F Write sector buffer (recommended practice before formatting)
- = %10 Test drive ready
- = %11 Recalibrate
- = %12 Controller RAM diagnostic
- = %13 Drive diagnostic
- = %14 Controller internal diagnostic

Registers used for fixed disk operations

DL = Drive number (%80-%87 for disk, value checked)
DH = Head number (0-7 allowed, not value checked)
CH = Cylinder number (0-1023, not value checked)
CL = Sector number (1-17 decimal, not value checked)

NOTE! High 2 bits of cylinder number are placed in the high 2 bits of the CL register (10 bits total)

AL = number of sectors (maximum possible range 1-%80, for read/write long %01-%79)
ES:BX = Buffer addressfor reads and writes (not required for verify)

Output AH = Status of current operation
- %0FF = Sense operation failed
- %0BB = Undefined error occurred
- %80 = Attachment failed to respond
- %40 = Seek operation failed
- %20 = Controller has failed

%11 = ECC corrected data error
%10 = Bad ECC on disk read
%0B = Bad track flag detected
%09 = Attempt to DMA across 64 kilobyte boundary
%07 = Drive parameter activity failed
%05 = Reset failed
%04 = Requested sector not found
%02 = Address mark not found
%01 = Bad command passed to disk I/O

CY = 0 Successful operation (AH = 0 on return)
= 1 Failed operation (AH has error reason)

DL = Number of consecutive acknowledging drives attached

DH = Maximum usable value for head number

CH = Maximum usable value for cylinder number

CL = Maximum usable value for sector number and cylinder number high bits

RS-232C Communications - Interrupt %14

This routine provides byte stream I/O to the RS-232C serial port.

AH = 0 Initialize the port
AL = Initialization parameters

7 6 5	4 3	2	1 0
baud rate	parity	stopbit	char length
000 = 110	x0 = none	0=1	10 = 7 bits
001 = 150	01 = odd	1=2	11 = 8 bits
010 = 300	11 = even		
011 = 600			
100 = 1200			
101 = 2400			
110 = 4800			
111 = 9600			

AH = 1 Send the character in AL (AL register is preserved).

On exit, if the routine was unable to transmit the data byte over the line, bit 7 of AH is set. When this bit is not set, the remainder of AH is set as in a status request, reflecting the current line status.

AH = 2 Receive an AL character from the line before returning to caller.

On exit, AH has the current status of the line set by the status routine, but the only bits remaining on are the error bits (7,4,3,2,1). These bits are not predictable if AH has bit 7 on (time out). AH is non-zero only when there is an error.

AH = 3 Return the port status in AX

AH contains the line status
- Bit 7 = Time out
- Bit 6 = Transmitter shift register empty
- Bit 5 = Transmitter holding register empty
- Bit 4 = Break detect
- Bit 3 = Framing error
- Bit 2 = Parity error
- Bit 1 = Overrun error
- Bit 0 = Data Ready

AL contains the modem status
- Bit 7 = Received line signal detect
- Bit 6 = Ring indicator
- Bit 5 = Data Set Ready
- Bit 4 = Clear to Send
- Bit 3 = Delta receive line signal detect
- Bit 2 = Trailing edge ring detector
- Bit 1 = Delta Data Set Ready
- Bit 0 = Delta Clear to Send

DX = Parameter indicating which RS-232C (0 and 1 allowed)

Output AX modified according to parameters of call

Keyboard - Interrupt %16

This routine provides support for the keyboard.

Input AH = 0 Read the next ASCII character in the buffer and return the result in AL (scan code in AH). If the buffer is empty, the routine waits for a key to be pressed.

AH = 1 Set the Z flag to indicate if an ASCII character is available to be read
ZF = 0 Code is available
ZF = 1 No code available
If ZF = 0, the next character in the buffer to be read is in AX, and the entry remains in the buffer

```
          AH = 2    Return current shift status in AL register.
                    Bit 7 - 1 = Insert mode is on
                        6 - 1 = Caps lock state is on
                        5 - 1 = Num lock state is on
                        4 - 1 = Scroll lock state is on
                        3 - 1 = Alternate shift key depressed
                        2 - 1 = Control shift key depressed
                        1 - 1 = Left shift key depressed
                        0 - 1 = Right shift key depressed

Output    Only AX and flags changed
```

Printer - Interrupt %17

This routine provides communication with the printer.

```
Input     AH = 0    Print the character in AL

                    On exit, AH = 1 if character could not be
                    printed (time out). Other bits set as on
                    normal status call

          AH = 1    Initialize the printer port

                    On exit,  AH = printer status

          AH = 2    Read the printer status into AH
                    7 - 1 = Not busy
                    6 - 1 = Acknowledge
                    5 - 1 = Out of paper
                    4 - 1 = Selected
                    3 - 1 = I/O error
                    2 - not used
                    1 - not used
                    0 - Time out

          DX = Printer to be used (0,1,2)

Output    AH is modified
```

Bootstrap - Interrupt %19

This routine reads track 0, sector 1 into the boot location (segment 0, offset 7C00), where control is transferred.

Time of Day - Interrupt %1A

This routine allows the clock to be set or read.

```
Input     AH = 0    Read the current clock setting
                    Returns,  CX = High portion of count
                              DX = Low portion of count
                              AL = 0 If timer has not passed 24
                                   hours since last read
                                 <> 0 if on another day
```

AH = 1 Set the current clock
CX = High portion of count
DX = Low portion of count

Note: Counts occur at approx. 18.2/sec

Keyboard Break Address - Interrupt %1B

This vector points to the code called when the Ctrl and Break keys are pressed (keyboard interrupt) and is initialized by power-on routines to point to an IRET instruction. This prevents anything from occurring when the Ctrl and Break keys are pressed. If a different value is set, control should be returned using an IRET instruction.

Timer Tick - Interrupt %1C

This vector points to the code called on every system-clock tick (timer interrupt) and is initialized by power-on routines to point to an IRET instruction. If a different value is set, control should be returned using an IRET instruction.

Video Parameters - Interrupt %1D

This vector points to those parameters necessary for CRT controller initialization, and is initialized by power-on routines to point to parameters in the ROM video routines.

Diskette Parameters - Interrupt %1E

Power-on routines initialize the vector to point to the parameters contained in the ROM diskette routine.

Graphics Character Extensions - Interrupt %1F

The ASCII code point character is developed in the graphics mode by the read/write character interface, using a set of dot patterns. ROM contains the first 128 code points, while the second 128 code points are accessed by pointing the vector to a table of up to 1 kilobyte. Each code point is then represented by eight bytes of graphic information. Power-on routines initialize this vector to 000:0.

Interrupt %40

This vector is used to revector the diskette pointer for the hard disk on the TS 1605H.

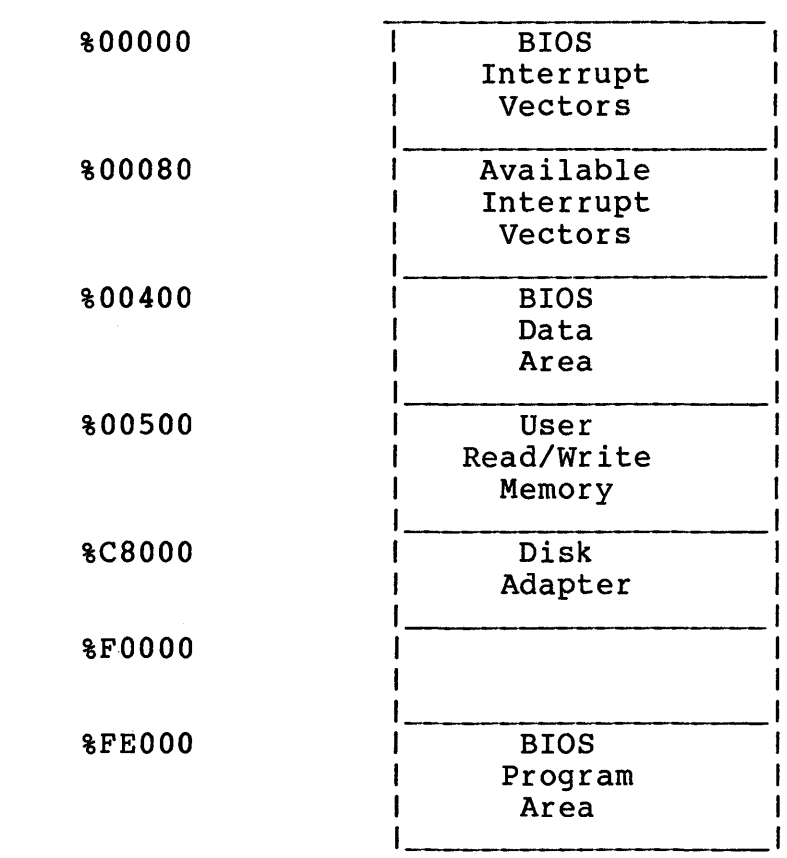
Fixed Disk Parameters - Interrupt %41

This vector points to the parameters necessary for the fixed disk drive, and is initalized by power-on routines to point to the parameters in the ROM disk routine.

BIOS Memory Usage

Beginning at absolute addresses %400 to %4FF, the BIOS routines use 256 bytes of memory. Figure 5-1 shows an overall BIOS memory map.

Figure 5-1
BIOS Memory Map



KEYBOARD ENCODING AND USAGE

Keyboard scan codes are translated into an extended ASCII code by BIOS keyboard routines. Included in the extended ASCII code are one-byte character codes with values from 0-255, extended codes for certain extended keyboard functions, and functions handled within the keyboard routine or through interrupts.

The keyboard routine suppresses the typematic action of the Ctrl, Shift, Alt, Num Lock, Scroll Lock, Caps Lock, and Ins keys. Table 5-2 lists the character codes that are passed through the BIOS routine to the system or program. For key numbers, refer to Table 5-2. For a complete listing of character codes, refer to Appendix D.

Table 5-2
Character Codes

Key #	Base	Shift	Alt	Ctrl
1	Esc	Esc	See note	Esc
2	1	!	Table 5-4	See note
3	2	@	Table 5-4	Nul
4	3	#	Table 5-4	See note
5	4	$	Table 5-4	See note
6	5	%	Table 5-4	See note
7	6	^	Table 5-4	RS(030)
8	7	&	Table 5-4	See note
9	8	*	Table 5-4	See note
10	9	(	Table 5-4	See note
11	0	)	Table 5-4	See note
12	-	_	Table 5-4	US(031)
13	=	+	Table 5-4	See note
14	Backspace (008)	Backspace (008)	See note	Del (127)
15	Tab (009)	Backtab (Note 1)	See note	See note
16	q	Q	Table 5-4	DC1(017)
17	w	W	Table 5-4	ETB(023)
18	e	E	Table 5-4	ENQ(005)
19	r	R	Table 5-4	DC2(018)
20	t	T	Table 5-4	DC4(020)
21	y	Y	Table 5-4	EM(025)
22	u	U	Table 5-4	NAK(021)
23	i	I	Table 5-4	HT(009)
24	o	O	Table 5-4	SI(015)
25	p	P	Table 5-4	DLE(016)
26	[	{	See note	Esc(027)
27	]	}	See note	GS(029)
28	CR	CR	See note	LF(010)
29 Ctrl	See note	See note	See note	See note
30	a	A	Table 5-4	SOH(001)
31	s	S	Table 5-4	DC3(019)
32	d	D	Table 5-4	EOT(004)
33	f	F	Table 5-4	ACK(006)
34	g	G	Table 5-4	BEL(007)
35	h	H	Table 5-4	BS(008)
36	j	J	Table 5-4	LF(010)
37	k	K	Table 5-4	VT(011)
38	l	L	Table 5-4	FF(012)
39	;	:	See note	See note
40	'	"	See note	See note
41	`	~	See note	See note
42 Shift	See note	See note	See note	See note
43	\	|	See note	FS(028)
44	z	Z	Table 5-4	SUB(026)
45	x	X	Table 5-4	CAN(024)
46	c	C	Table 5-4	ETX(003)
47	v	V	Table 5-4	SYN(022)
48	b	B	Table 5-4	STX(002)

49		n	N	Table 5-4	SO(014)
50		m	M	Table 5-4	CR(013)
51		,	<	See note	See note
52		.	>	See note	See note
53		/	?	See note	See note
54	Shift	See note	See note	See note	See note
55		*	Table B-5	See note	Table 5-4
56	Alt	See note	See note	See note	See note
57		Space	Space	Space	Space
58		See note	See note	See note	See note
59		Table 5-4	Table 5-4	Table 5-4	Table 5-4
60		Table 5-4	Table 5-4	Table 5-4	Table 5-4
61		Table 5-4	Table 5-4	Table 5-4	Table 5-4
62		Table 5-4	Table 5-4	Table 5-4	Table 5-4
63		Table 5-4	Table 5-4	Table 5-4	Table 5-4
64		Table 5-4	Table 5-4	Table 5-4	Table 5-4
65		Table 5-4	Table 5-4	Table 5-4	Table 5-4
66		Table 5-4	Table 5-4	Table 5-4	Table 5-4
67		Table 5-4	Table 5-4	Table 5-4	Table 5-4
68		Table 5-4	Table 5-4	Table 5-4	Table 5-4
69		See note	See note	See note	Pause
70		See note	See note	See note	Break

The keys in the numeric keypad only have meaning in the states listed in Table 5-3. The shift key reverses the current Num Lock state.

Table 5-3
Numeric Keypad Keys

Key #	Base	Lock	Num	Alt	Ctrl
71	See Table 5-4	7	See note		Clear screen
72	See Table 5-4	8	See note		See note
73	See Table 5-4	9	See note		Top of Text and Home
74		-	See note		See note
75	See Table 5-4	4	See note		Table 5-4
76	See note	5	See note		See note
77	See Table 5-4	6	See note		Table 5-4
78	+	+	See note		See note
79	See Table 5-4	1	See note		Table 5-4
80	See Table 5-4	2	See note		See note
81	See Table 5-4	3	See note		Table 5-4
82	Ins	0	See note		See note
83	Tables 5-4, 5-5.		Table 5-5		Table 5-5

NOTE! The combination is suppressed in the keyboard routine.

Extended Codes

An extended code is used for certain functions that cannot be represented in the standard ASCII code. If a nul (000) is returned in the AL register, the system or program should check the AH register for a second code, normally the scan code of the primary key that was pressed. Table 5-4 lists the second code and its function.

Table 5-4
Keyboard Extended Codes

Second Code	Function
3	Nul character
15	Backspace
16 - 25	Alt Q, W, E, R, T, Y, U, I, O, P
30 - 38	Alt A, S, D, F, G, H, J, K, L
44 - 50	Alt Z, X, C, V, B, N, M
59 - 68	F1 - F10
71	Home
72	Cursor up
73	Page up and Home cursor
75	Cursor left
77	Cursor right
79	End
80	Cursor down
81	Page down and home cursor
82	Insert
83	Delete
84 - 93	F11 - F20 (Upper-case F1 to F10)
94 - 103	F21 - F30 (Ctrl F1 to F10)
104 - 113	F31 - F40 (Alt F1 to F10)
114	Ctrl PrtSc
115	Ctrl Cursor left (Back one word)
116	Ctrl Cursor right (Advance one word)
117	Ctrl End (Erase to end of line)
118	Ctrl Pgdn (Erase to end of screen)
119	Ctrl Home (Clear screen and home)
120 - 131	Alt 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, -, =
132	Ctrl PgUp (Top 25 lines and Home cursor)

Shift States

The keyboard routine handles most of the shift states so they appear transparent to the system or applications program. The following keys initiate the shifted states:

Shift — The shift keys temporarily shift keys 2-13, 15-27, 30-41, 43-53, 55, and 59-68 to upper-case, or base-case if in the Caps Lock state. The shift keys also temporarily reverse the state of the numeric keypad keys 71, 73, 75, 77, and 79 through 83.

Ctrl The Ctrl key temporarily shifts keys 3, 7, 12, 14, 16-28, 30-38, 43-50, 55, 59-71, 73, 75, 77, 79, and 81 to the Ctrl state.

Alt The Alt key temporarily shifts keys 2-13, 16-25, 30-38, 44-50, and 59-68 to the Alt state.

The Alt key is also used to enter character codes from 0 to 255 into the system. Hold down the Alt key and enter the decimal value of the desired character using the number keys on the numeric keypad. If more than three digits are entered, a modulo-256 is created. The system interprets these three digits as a character code and transmits them through the keyboard routine to the system or applications program.

Caps Lock The Caps Lock key shifts keys 16-25, 30-38, and 44-50 to upper-case. The Caps Lock key works as a toggle between the base-and upper-case state.

In cases where combinations of the Alt, Ctrl, and shift keys are pressed, the Alt key has first priority, followed by the Ctrl key, and then the shift keys.

Special Key Combinations

Table 5-5 lists special key combinations that perform system functions.

Table 5-5
Special Key Combinations

Function	Key Combination	Description
Reset	Ctrl/Alt/Del	When these three keys are pressed simultaneously, a system reset is initiated.
	w W	Table 5-4
18 e	E	Table 5-4 ENQ(005)
19 r	R	Table 5-4 DC2(018)
20 t	T	Table 5-4 DC4(020)
21 y	calling interrupt %1B.	
Pause	Ctrl/Num Lock	This key combination causes the keyboard interrupt routine to loop, waiting for any key except the Num Lock key to be pressed. This provides a method of temporarily suspending and then resuming operation. The resume key code is discarded.

Print Screen	Shift/PrtSc	This key combination results in the keyboard routine calling interrupt %5 (Print Screen). This routine works in both the alpha and graphics modes and prints unrecognizable characters as blanks.

APPENDIX A
REFERENCES

The following publications contain information on the TS 1605 and TS 1605H microcomputer systems:

* TS 1605 Computer System User's Manual, TeleVideo
* Tele-XT Computer System User's Manual, TeleVideo
* TS 1605 TeleDOS User's Manual, TeleVideo
* TS 1605 Field Replaceable Units Manual, TeleVideo
* Intel Component Data Catalog, Intel
* Intel Microprocessor and Peripherals Handbook, Intel
* Synertek SY6845R CRT Controller Data Sheet, Synertek
* How to Get Started with MS-DOS, Dilithium Press
* The 8086/8088 Primer, Hayden Book Company
* The 8086 Book, Osborne/McGraw-Hill
* Western Digital Components Handbook, Western Digital Corporation

APPENDIX B
I/O PORT ADDRESSES

Table B-1
I/O Port Addresses
(Repeated here from Table 2-1 for easy access)

Device			Address
DMA			%000-%00F
Channel 0	DMA refresh		
Channel 1	I/O channel		
Channel 2	FDC data transfer or I/O channel		
Channel 3	Hard disk transfer or I/O channel		
Programmable Interrupt Controller			%020-%021
Programmable Interval Timer			%040-%043
Channel 0	Time of day		%040
Channel 1	Dynamic RAM refresh		%041
Channel 3	Audio speaker tone		%042
Command Register			%043
Programmable Peripheral Interface			%060-%063
PA (Input)	Keyboard scan code		%060
PB (Output)	PB0	Speaker gate	%061
	PB1	Speaker data	
	PB2	Spare	
	PB3	Read switch high/low bits	
	PB4	Spare	
	PB5	Enable I/O channel check	
	PB6	Force keyboard clock low	
	PB7	Clear keyboard	
PC (Input)	PC0	SW1	%062
	PC1	SW2	
	PC2	SW3	
	PC3	SW4	
	PC4	Speaker data	
	PC5	Timer channel 2 output	
	PC6	I/O channel check	
	PC7	Always low	
Command/Mode Register (set to %99)			%063
DMA Page Register			%080-%083
NMI Mask Register			%0A0
To enable NMI, write data %80 into address %0A0			
To disable NMI, write data %00 into address %0A0			

Serial Port (Primary)	%3F8-%3FF
Tx Buffer/Rx Buffer/ Divisor Latch LSB	%3F8
Interrupt Enable/Divisor Latch MSB	%3F9
Interrupt Identification Register	%3FA
Line Control Register	%3FB
Modem Control Register	%3FC
Line Status Register	%3FD
Modem Status Register	%3FE
Floppy Disk Control Port	%3F2
Select drive A	D0 = 0
Select drive B	D0 = 1
Reset 8272A FDC	D2 = 0
Disable interrupt/DMA operation	D3 = 0
Enable interrupt/DMA operation	D3 = 1
Turn on both motors	D4 or D5 = 1
Floppy Disk Controller	%3F4-%3F5
FDC Main Status Register	%3F4
FDC Data Register	%3F5
Parallel Data Port (Read/write)	%3BC
Parallel Control Port (Read/write)	%3BE
STROBE (-)	D0
AUTO FD XT	D1
INIT (-)	D2
SLCT IN (-)	D3
INTERRUPT ENABLE	D4
Parallel Status Port (Read only)	%3BD
ERROR (-)	D3
SLCT	D4
PE	D5
ACK (-)	D6
BUSY (-)	D7
Winchester Disk Control Register	%0E0
To enable interrupt:	D6 = 1
To disable interrupt:	D6 = 0
To enable DMA operation:	D7 = 1
To disable DMA operation:	D7 = 0

Winchester Disk Controller Board Task File Register %330-%337

Read Data	Write Data	%330
Error flag	Write precomp cylinder	%331
Sector count	Sector count	%332
Sector number	Sector number	%333
Cylinder low	Cylinder low	%334
Cylinder high	Cylinder high	%335
SDH	SDH	%336
Status register	Command register	%337

APPENDIX C
POWER-ON SELF TEST

The TS 1605/1605H has a power-on self test that checks the system unit, keyboard, video display, and disk drives. The self test resides in the system's operating ROM and runs automatically when power is applied to the system.

When the test finds a malfuntion, it indicates the source by displaying one of these error messages on the screen:

101	System Board (DMA, Interval Timer)
201	RAM (excluding first 16 kilobytes of memory)
301	Keyboard
601	Diskette Drive
1701	Hard Disk Drive (on TS 1605H only)

If the "301" error message appears on the screen, check the keyboard plug. Ensure the keyboard is plugged in properly and repeat the self test by turning the system off and then on again. If the error message reappears, or if other error messages appear, call your authorized dealer.

Because malfunctions in static RAM, the CRT controller, and the video display cannot be displayed on the screen, the system indicates these errors with one long beep and two short beeps from the system's speakers. Should this occur, call your authorized dealer.

When it completes the self tests, the system sounds one short beep. It then attempts to boot the operating system from drive A (TS 1605) or the hard disk (TS 1605H). If it loads the operating system successfully, a blinking cursor appears on the screen indicating the system is ready for operation. If it fails to load the operating system, an error message appears on the screen.

If the system completes the self test and boots the operating system properly but does not operate, run the special diagnostics (available from your authorized dealer) or return the system to your dealer.

APPENDIX D
ASCII CHARACTER CODE CHART

Figure D-1
ASCII Character Code Chart

Bits 7 6 5					0_0	$0_0{}_1$	$0_1{}_0$	$0_1{}_1$	$1_0{}_0$	$1_0{}_1$	$1_1{}_0$	$1_1{}_1$
4	3	2	1	Column → / ↓ Row	0	1	2	3	4	5	6	7
0	0	0	0	0	NUL	DLE	SP	0	@	P		p
0	0	0	1	1	SOH	DC1	!	1	A	Q	a	q
0	0	1	0	2	STX	DC2	"	2	B	R	b	r
0	0	1	1	3	ETX	DC3	#	3	C	S	c	s
0	1	0	0	4	EOT	DC4	$	4	D	T	d	t
0	1	0	1	5	ENQ	NAK	%	5	E	U	e	u
0	1	1	0	6	ACK	SYN	&	6	F	V	f	v
0	1	1	1	7	BEL	ETB	'	7	G	W	g	w
1	0	0	0	8	BS	CAN	(	8	H	X	h	x
1	0	0	1	9	SKIP HT	EM	)	9	I	Y	i	y
1	0	1	0	10(a)	LF	SUB	*	:	J	Z	j	z
1	0	1	1	11(b)	VT	ESC	+	;	K	[	k	{
1	1	0	0	12(c)	FF	FS	,	<	L	\	l	|
1	1	0	1	13(d)	CR	GS	-	=	M	]	m	}
1	1	1	0	14(e)	SO	HOME RS	.	>	N	^	n	~
1	1	1	1	15(f)	SI	NEW LINE US	/	?	O	_	o	DEL RUB

ASCII Code Table
Abbreviations For Control Characters

NUL	null	FF	form feed	CAN	cancel
SOH	start of heading	CR	carriage return	EM	end of medium
STX	start of text	SO	shift out	SUB	substitute
ETX	end of text	SI	shift in	ESC	escape
EOT	end of transmission	DLE	data link escape	FS	file separator
ENQ	enquiry	DC1	device control 1	GS	group separator
ACK	acknowledge	DC2	device control 2	RS	record separator
BEL	bell	DC3	device control 3	US	unit separator
BS	backspace	DC4	device control 4	SP	space
HT	horizontal tabulation	NAK	negative acknowledge	DEL	delete
LF	linefeed	SYN	synchronous idle		
VT	vertical tabulation	ETB	end of transmission block		

APPENDIX E
GLOSSARY OF ACRONYMS

Table E-1
Glossary of Acronyms

Abbreviation	Description
BIOS	Basic Input/Output System
CRC	Cyclic Redundancy Check
CRT	Cathode Ray Tube
CTS	Clear To Send
DIP	Dual-In-Line Package
DLAB	Divisor Latch Access Bit
DMA	Direct-Memory Access
DSR	Data Set Ready
DTR	Data Terminal Ready
ECC	Error Checking And Correction
EPROM	Erasable Programmable Read-Only Memory
FDC	Floppy Disk Controller
FDD	Floppy Disk Drive
LSB	Least Significant Bit (Byte)
MFM	Modified Frequency Modulation
MSB	Most Significant Bit (or Byte)
PPI	Programmable Peripheral Interface

APPENDIX F
CONNECTOR PIN ASSIGNMENTS

Table F-1
Connector P1 (Serial I/O)

Pin Number	Signal Designator	Signal Description
1	GND	Signal Ground
2	TXD	Transmitted Data
3	RXD	Received Data
4	RTS	Request to Send
5	CTS	Clear to Send
6	DSR	Data Set Ready
7	GND	Signal Ground
8	RLSD	Received Line Signal Detector
9	TXD CL RET	Transmit Current Loop Data Return
11	TXD CL	Transmit Current Loop Data
18	RXD CL	Receive Current Loop Data
20	DTR	Data Terminal Ready
22	RI	Ring Indicator
25	RXD CL RET	Received Current Loop Data Return

Table F-2
Connector P2 (Parallel I/O)

Pin Number	Signal Designator	Signal Description
1	-STROBE	Strobe
2	DATA 0	Data 0
3	DATA 1	Data 1
4	DATA 2	Data 2
5	DATA 3	Data 3
6	DATA 4	Data 4
7	DATA 5	Data 5
8	DATA 6	Data 6
9	DATA 7	Data 7
10	-ACK	Acknowledge
11	BUSY	Busy
12	PE	Paper Empty
13	SLCT	Select
14	-AUTO FD	Auto Feed
15	ERROR	Error
16	-INIT	Initialize Printer
17	-SLCT IN	Select Input

Pins 18 through 25 are signal ground.

Table F-3
Connector P3 (I/O Channel)

Pin Number	Signal Designator	Signal Description
1	GND	GROUND
2	I/O CH CK	I/O Channel Check
3	I/O RESET	I/O Reset
4	D7	Data Line 7
5	+5V	+5 Volts
6	D6	Data Line 6
7	IRQ2	Interrupt Request 2
8	D5	Data Line 5
9	-5V	-5 Volts
10	D4	Data Line 4
11	DERQ2	Data Request 2
12	D3	Data Line 3
13	-12V	-12 Volts
14	D2	Data Line 2
15	+5V	+5 Volts
16	D1	Data Line 1
17	+12V	+12 Volts
18	D0	Data Line 0
19	GND	Ground
20	I/O CH RDY	I/O Channel Ready
21	-MEMW I/O	Memory Write I/O
22	AEN	Address Enable
23	-MEMR I/O	Memory Read I/O
24	A19	Address Line 19
25	-IOW	I/O Write
26	A18	Address Line 18
27	-IOR I/O	I/O Read I/O
28	A17	Address Line 17
29	-DACK3	Data Acknowledge 3
30	A16	Address Line 16
31	DERQ3	Data Request 3
32	A15	Address Line 15
33	-DACK1	Data Acknowledge 1
34	A14	Address Line 14
35	DERQ1	Data Request 1
36	A13	Address Line 13
37	-DACK0	Data Acknowledge 0
38	A12	Address Line 12
39	CLK	Clock
40	A11	Address Line 11
41	IRQ7	Interrupt Request 7
42	A10	Address Line 10
43	IRQ6	Interrupt Request 6
44	A9	Address Line 9
45	IRQ5	Interrupt Request 5
46	A8	Address Line 8
47	IRQ4	Interrupt Request 4
48	A7	Address Line 7

49	IRQ3	Interrupt Request 3
50	A6	Address Line 6
51	-DACK2	Data Acknowledge 2
52	A5	Address Line 5
53	TC	Terminal Count
54	A4	Address Line 4
55	ALE	Address Latch Enable
56	A3	Address Line 3
57	+5V	+5 Volts
58	A2	Address Line 2
59	OSC	Oscillator
60	A1	Address Line 1
61	GND	Ground
62	A0	Address Line 0
63	GND	Ground
64	+5V	+5 Volts

Table F-4
Connector P5 (Power Supply)

Pin Number	Signal Designator	Signal Description
1	-12V	-12 Volts
2	Not Used	Not Used
3	GND	Ground
4	+5V	+5 Volts
5	+12V	+12 Volts

Table F-5
Connector P7 (Floppy Disk Controller)

Pin Number	Signal Designator	Signal Description
6	-DR SEL 4	Select Drive 4
8	-INDEX	Index
10	-DR SEL 1	Select Drive 1
12	-DR SEL 2	Select Drive 2
14	-DR SEL 3	Select Drive 3
18	-DIR SEL	Direction Select
20	-STEP	Step
22	-COMP WE DATA	Composite Write Data
24	-WRITE EN	Write Enable
26	-TRACK 0	Track 0
28	-WR PROTECTED	Write/Read Protected
30	-COMP READ DATA	Composite Read Data
32	SIDE SEL	Side Select

All odd pins are ground.

Table F-6
Connector P9 (Programmable Interval Timer)

Pin Number	Signal Designator	Signal Description
1	SPEAKER OUT	Speaker Out
2	SPEAKER RET	Speaker Return

Table F-7
Connector P8 (Winchester Hard Disk Controller Interface)

Pin Number	Signal Designator	Signal Description
1	WD0	Data Line 0
3	WD1	Data Line 1
5	WD2	Data Line 2
7	WD3	Data Line 3
9	WD4	Data Line 4
11	WD5	Data Line 5
13	WD6	Data Line 6
15	WD7	Data Line 7
17	WA0	Address Line 0
19	WA1	Address Line 1
21	WA2	Address Line 2
23	-WCS	Controller Board Select
25	-WWE	Controller Write Enable
27	-WRE	Controller Read Enable
29	-WMR	Controller Reset
35	WINTRQ	Controller Interrupt Line

All even pins are ground.

Table F-8
Connector P11 (Keyboard Interface)

Pin Number	Signal Designator	Signal Description
1	GND	Ground
2	+12V	+12 Volts
3	GND	Ground
4	KEY DATA	Key Data
5	KEY CLOCK	Key Clock
6	-KEY RESET	Key Reset

Table F-9
Connector VP1 (Composite Color Monitor Port)

Pin Number	Signal Designator	Signal Description
1	-	Peak-to-Peak Amplitude
2	GND	Chassis Ground

Table F-10
Connector VP2 (RGB Color Monitor Port)

Pin Number	Signal Designator	Signal Description
1	GND	Ground
2	GND	Ground
3	R	Red
4	G	Green
5	B	Blue
6	I	Intensity
7	Reserved	Reserved
8	RGB HS	Red, Green, Blue Horizontal Sync
9	RGB VS	Red, Green, Blue Vertical Sync

Table F-11
Connector VP3 (Standard TeleVideo Video Monitor)

Pin Number	Signal Designator	Signal Description
1	HYS	Horizontal Sync
2	Not Used	Not Used
3	GND	Ground
4	VIDEO	Video
5	VSYN	Vertical Sync

APPENDIX G
DISK DRIVE SPECIFICATIONS

DISKETTE DRIVE

TYPE	Slim-line 5 1/4-inch TEAC floppy disk drives
DISKETTES	48 TPI double-sided, double-density 5 1/4-inch floppy diskettes
STORAGE CAPACITY	500 Kbytes per drive unformatted 368.6 Kbytes per drive formatted 737.2 Kbytes total (formatted)
TRANSFER RATE	250 Kbits/second
ACCESS TIME	84 milliseconds average 120 milliseconds maximum

HARD DISK DRIVE

TYPE	Rodine RO252 3 1/2 inch winchester disk drive
DISKS	2
HEADS	4
STORAGE CAPACITY	12.75 Mbytes unformatted 10.0 Mbytes formatted 8192 bytes per track 256 bytes per sector 32 sectors per track 306 cylinders
TRANSFER RATE	5 Mbits per second
SEEK TIMES	(in milliseconds, including settling): 18 track to track 85 average 180 maximum 8.3 average latency

APPENDIX H
JUMPERS

This section describes jumpers on the system board.

COMMUNICATIONS PORT CONFIGURATION

E7, E8, E9 — The default setting for E7, E8, and E9 configures the asynchronous communications port for RS-232.

When you change them all, you reconfigure the asynchronous communications port to a Current Loop.

All three must be changed as a set for each configuration.

DYNAMIC RAM CONFIGURATION

E10, E11, E12 — The default setting for E10, E11, and E12 configures the board for 64K dynamic RAM.

When you change them all, you reconfigure the board for 256K dynamic RAM.

All three must changed as a set for each configuration.

VIDEO CONFIGURATION

E13 Default setting configures the board for double-dot character display.

Remove the jumper for single-dot character display.

E14 Default setting maps the monochrome display memory address B0000 - B7FFF to be the same as the color graphics memory address B8000 - BFFFF. **For those applications that require monochrome only, leave the jumper at default.**

When you change the jumper, you disable the monochrome display memory address map B0000 - B7FFF, thus leaving only the color graphics memory address map enabled. **For those applications that can be dynamically configured to run with color graphics, remove the jumper.**

E15 When the jumper is connected, the board is configured for an internal video controller.

When the jumper is removed, the board is configured for an external video controller.

APPENDIX I
SCHEMATICS

This section contains board assembly schematics and logic diagrams. Parts for TeleVideo systems are available from TeleVideo distributors.

REVISIONS				
REVISION	DESCRIPTION	ECO NO.	DATE	APPROVED
1	PRELIM. REL.			
A	PROD REL.	1252	7/14/82	
B	PROD REL PER ECO	1217	3/30/83	
C	PROD REL PER ECO	1428	5/2/84	

OPTION	DESCRIPTION
-00	FOR SYSTEM 1605 (BASIC SYSTEM)
-01	FOR SYSTEM 1605H ADD IC PART NO. 125016-00 TO DESIGNATIONS: U66,67,74,75,83,84 90,91,98,99,107,108,116,117,125,126
-02	FOR SYSTEM 1600 DELETE IC P/N 123433-00 U81 DELETE IC P/N 123431-00 U96

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE VALUED IN OHMS AND ARE 1/4 WATT, ±5%.
2. ALL CAPACITORS ARE VALUED IN μf AND ARE 16 VDC, ±20%.
3. THE FOLLOWING I.C'S ARE SPARES, U123, 130, 131 132, 139, 140, 147, 148, 124, 115.
4. THE FOLLOWING COMPONENTS ARE NOT USED; C15, 16, 18, 20, 22, 28-30, R12, R13
5. THE FOLLOWING COMPONENTS ARE CUSTOMER OPTION U41, 60

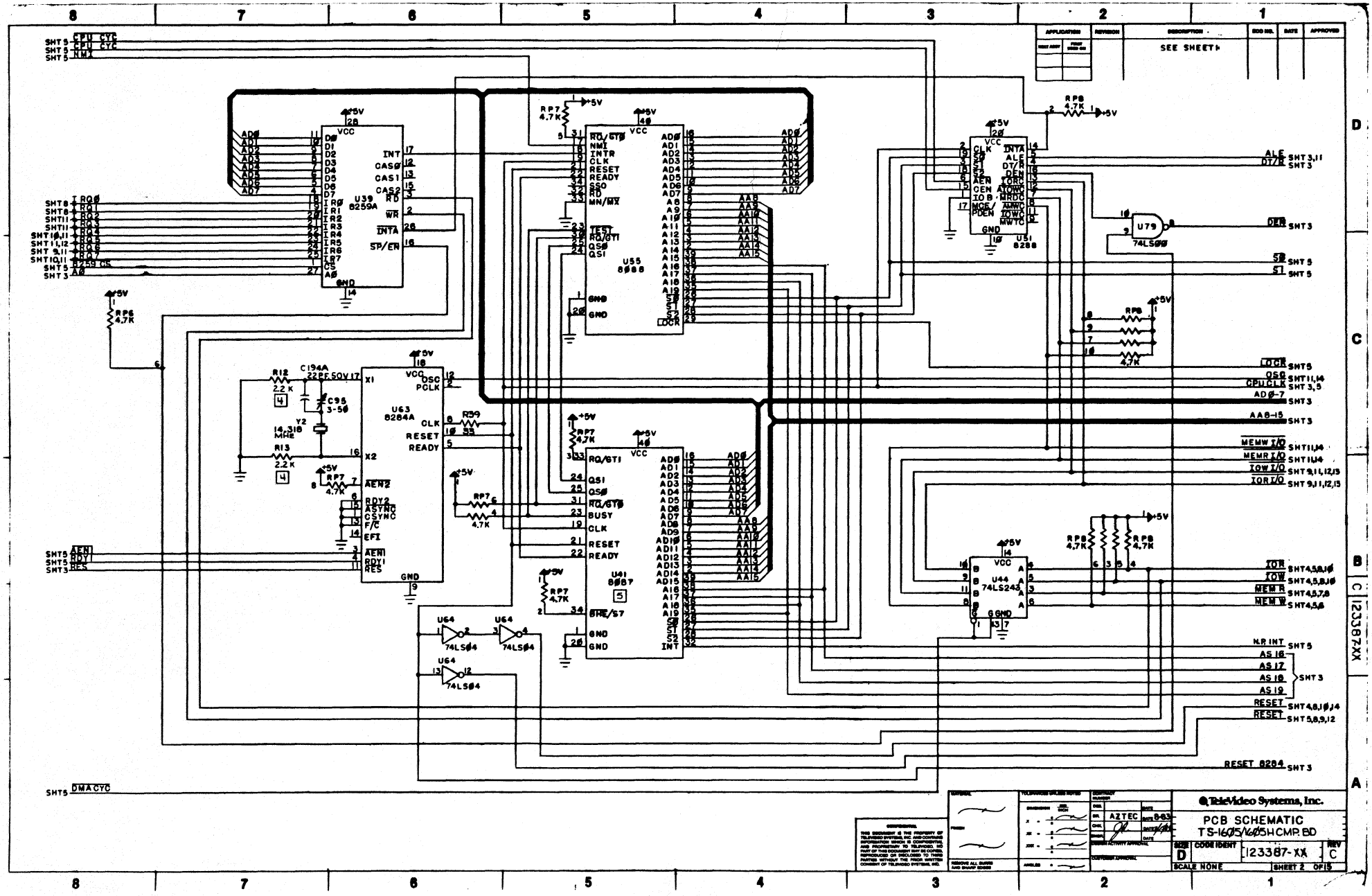
TeleVideo Systems, Inc.

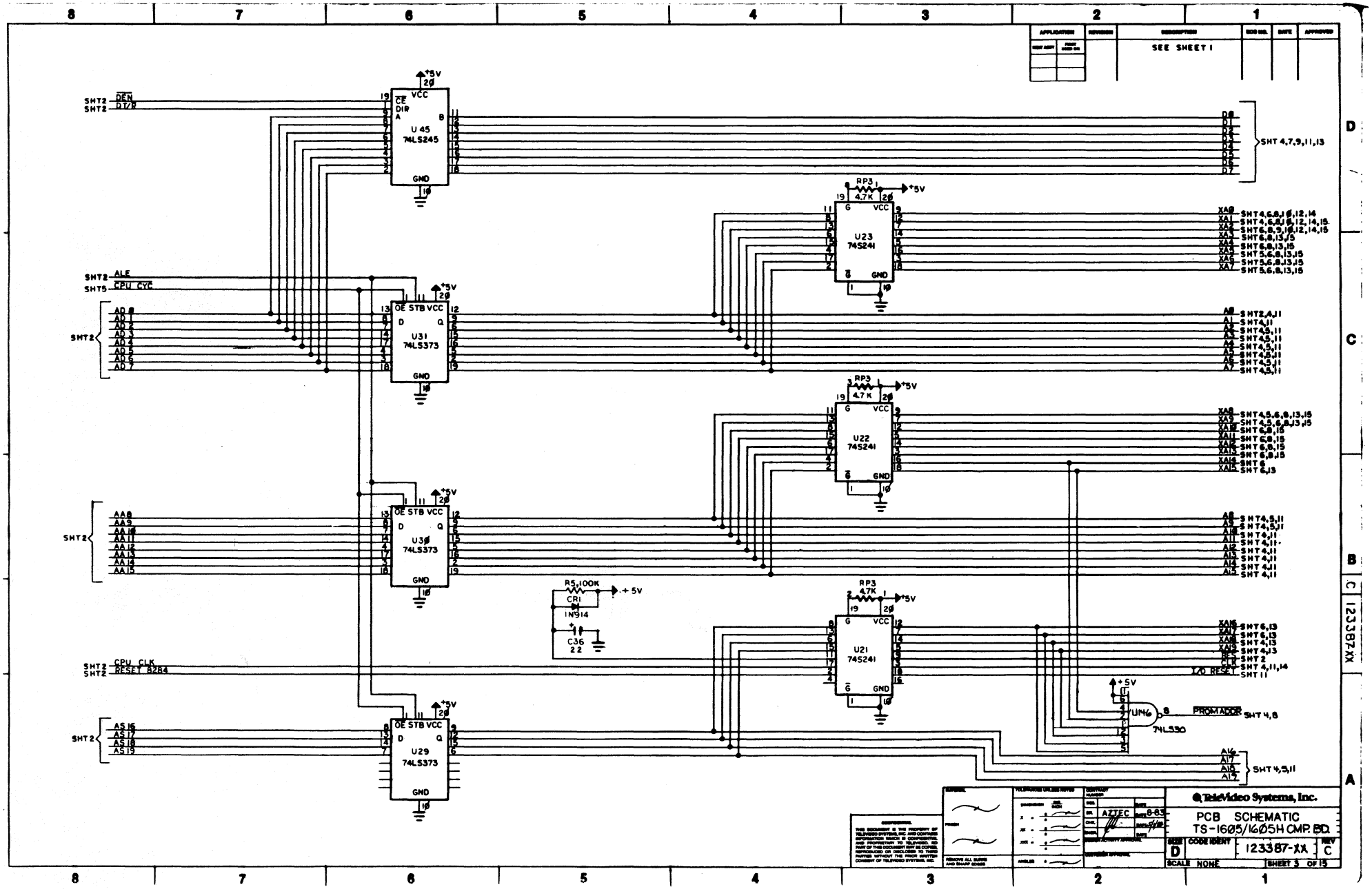
PCB SCHEMATIC
TS-1605/1605H CMP. BD

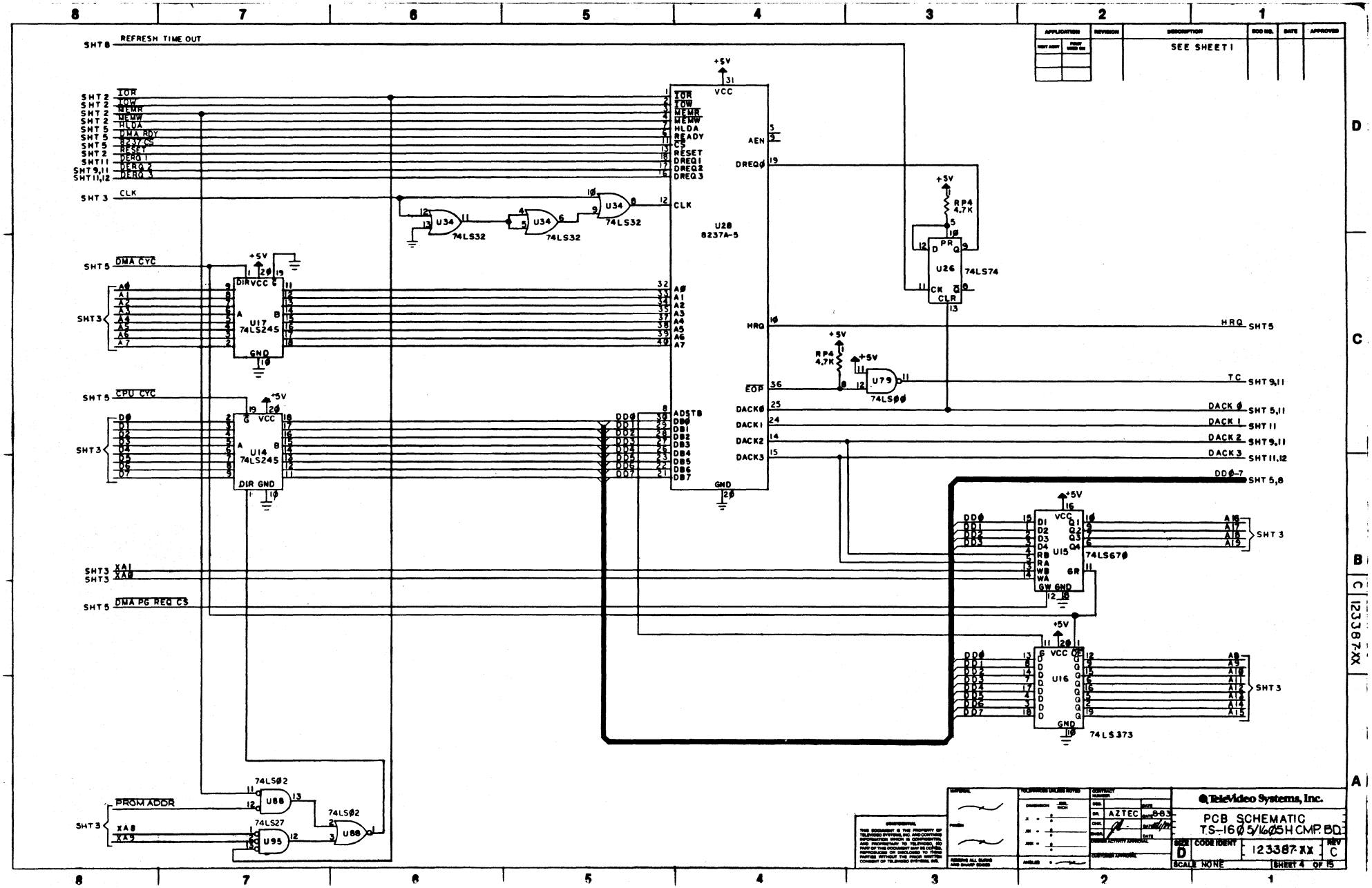
SIZE D | CODE IDENT | 123387-XX | REV C

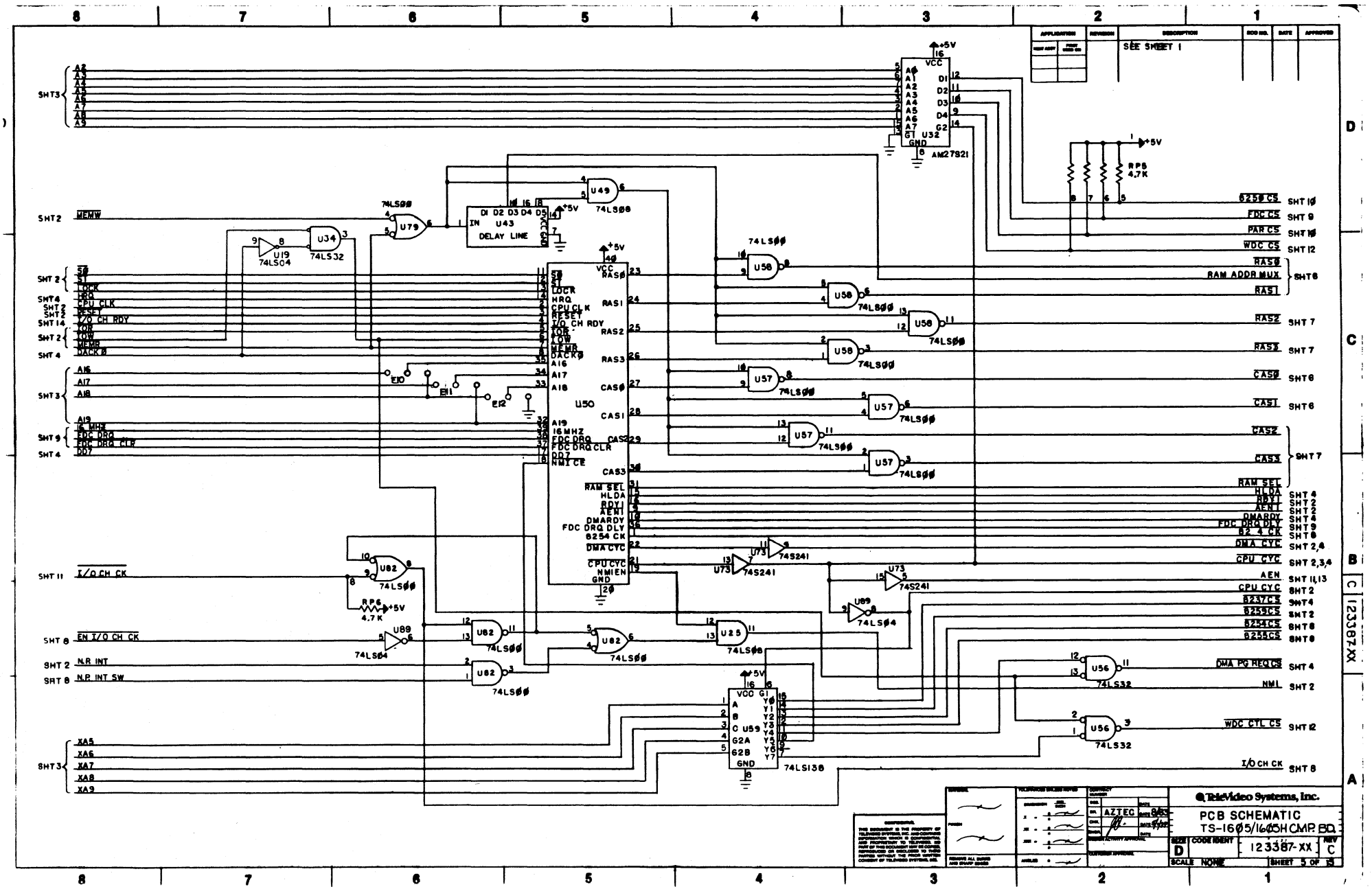
SCALE NONE | SHEET 1 OF 15

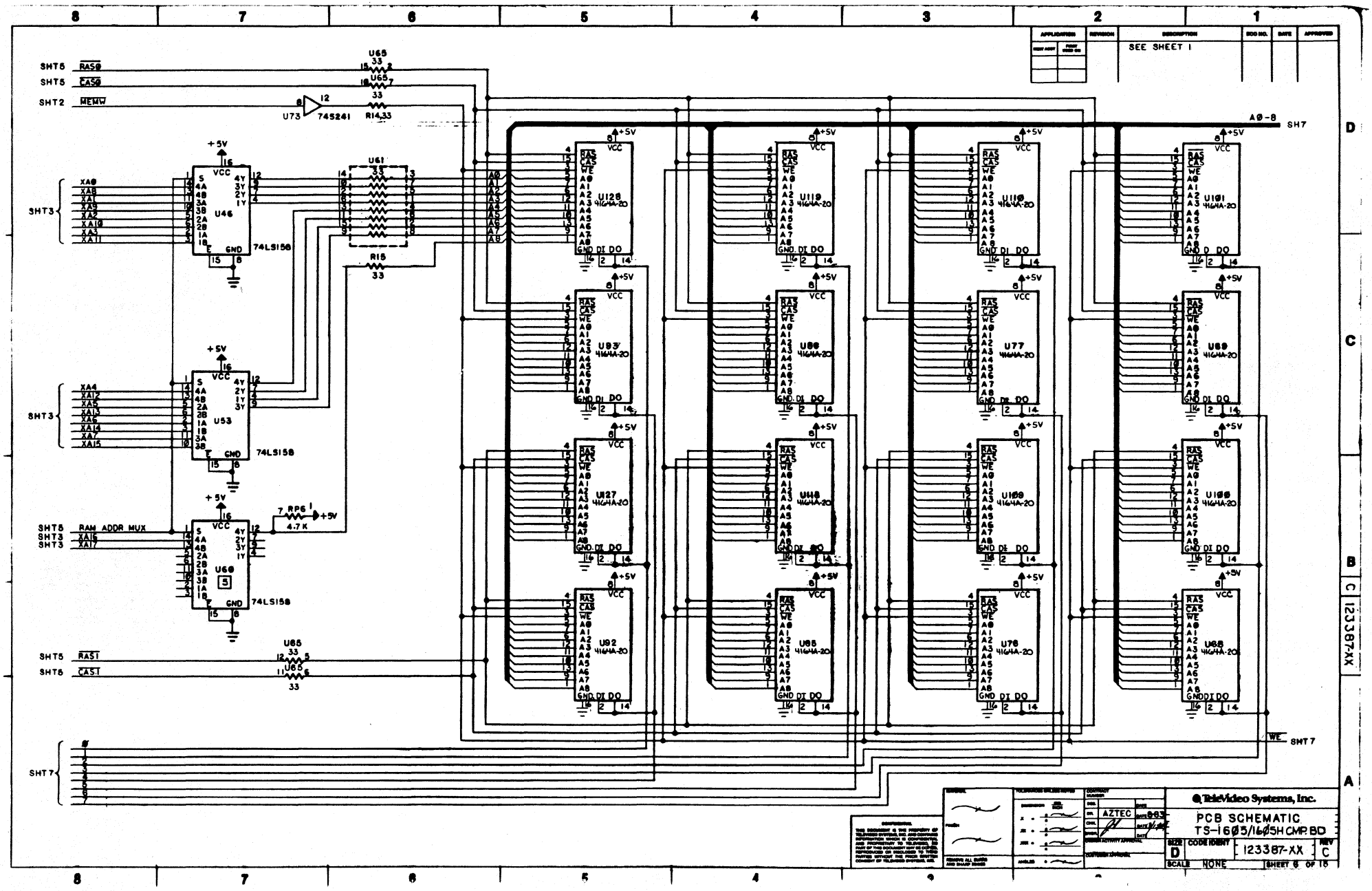
123387-XX

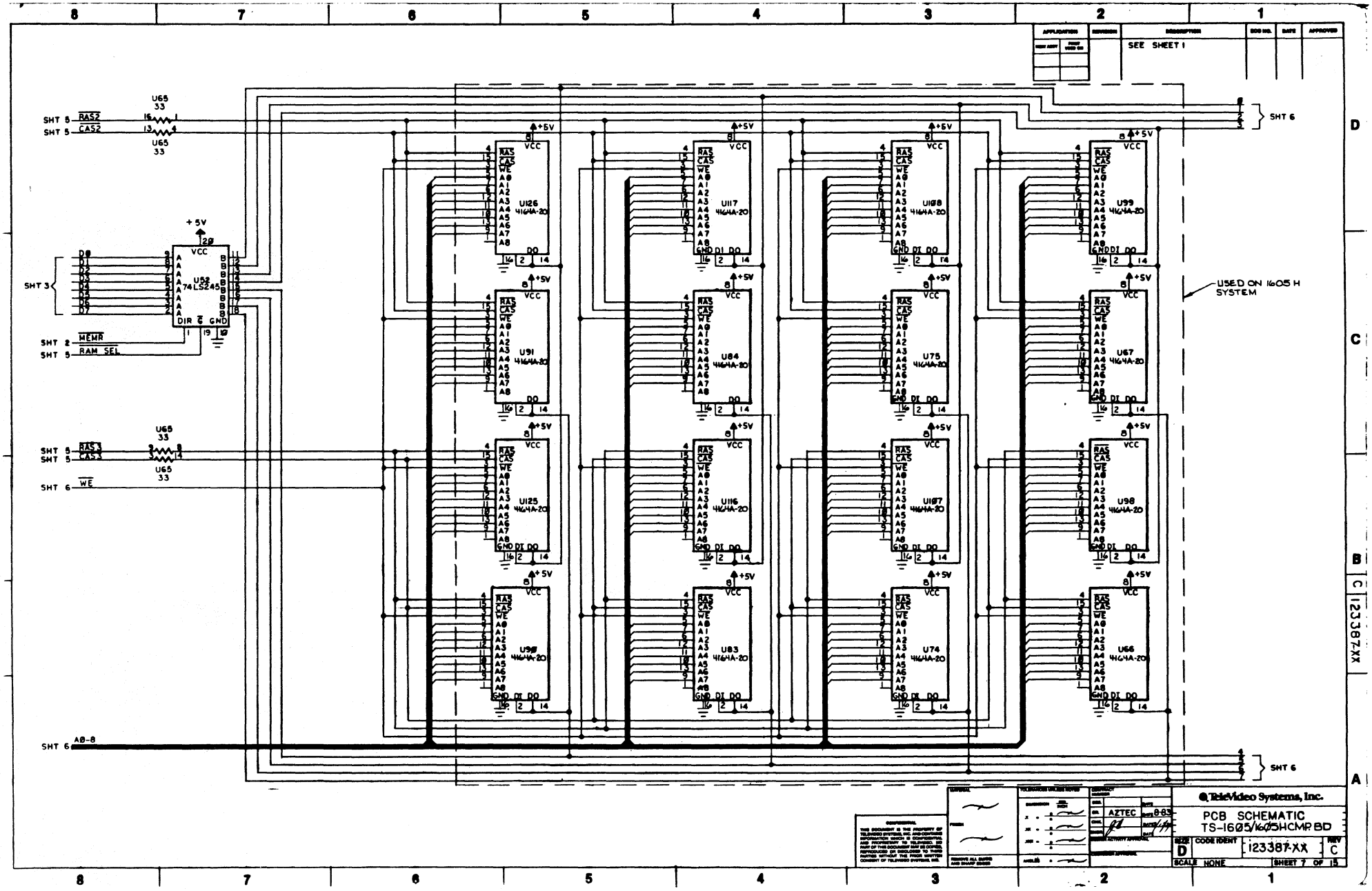

SEE SHEET
U39 8259A
U55 8088
U63 8284A
U41 8087
U44 74LS245
U51 8288
U79 74LS00
U64 74LS04
Y2 14.318 MHz
C95 3-50
C194A 22PF 50V
R12 2.2K
R13 2.2K
R59 33
RP6 4.7K
RP7 4.7K
RP8 4.7K
RP9 4.7K
RP10 4.7K
CPU CYC
NMI
DMA CYC
ALE
DT/R
DEN
IOR
IOW
MEMR
MEMW
RESET
RESET 8284
N.R INT
AS16
AS17
AS18
AS19
AEN
RDY1
RES
AEN2
RDY2
ASYNC
CSYNC
F/C
EFI
BHE/S7
INT
LOCK
QS0
CPU CLK
AD0-7
AA8-15
MEMW I/O
MEMR I/O
IOW I/O
IOR I/O
TeleVideo Systems, Inc.
PCB SCHEMATIC
TS-1605/1605H CMP. BD
AZTEC
8-83
CODE IDENT
123387-XX
REV C
SCALE NONE
SHEET 2 OF 15

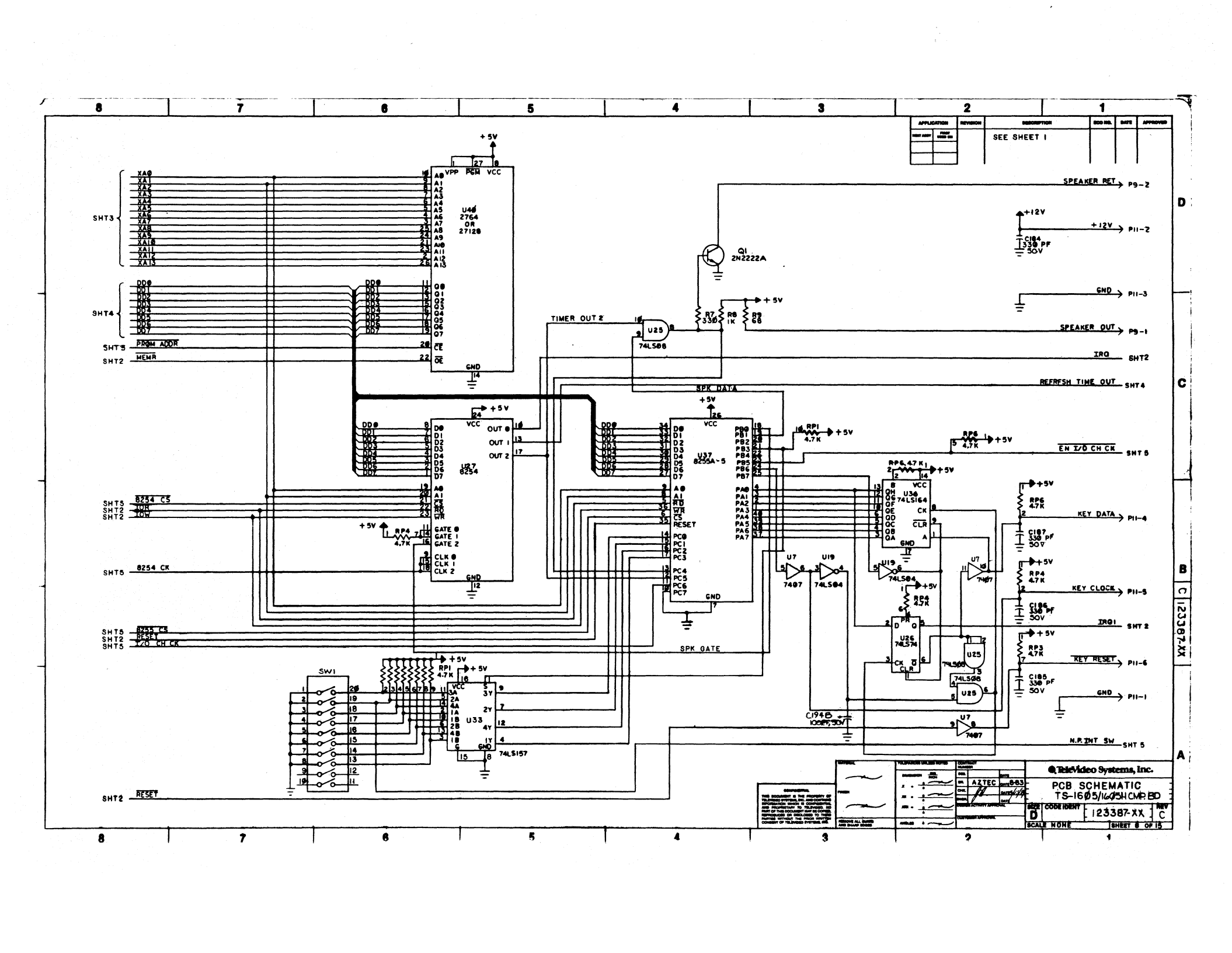

SEE SHEET 1
U 45
74LS245
U31
74LS373
U30
74LS373
U29
74LS373
U23
74S241
U22
74S241
U21
74S241
RP3
4.7K
R5 100K
CR1
IN914
C36
22
U1N6
74LS30
PROM ADDR
SHT 4,8
SHT 4,5,11
SHT 4,7,9,11,13
I/O RESET
TeleVideo Systems, Inc.
PCB SCHEMATIC
TS-1605/1605H CMP. BD.
123387-XX
SCALE NONE
SHEET 3 OF 15

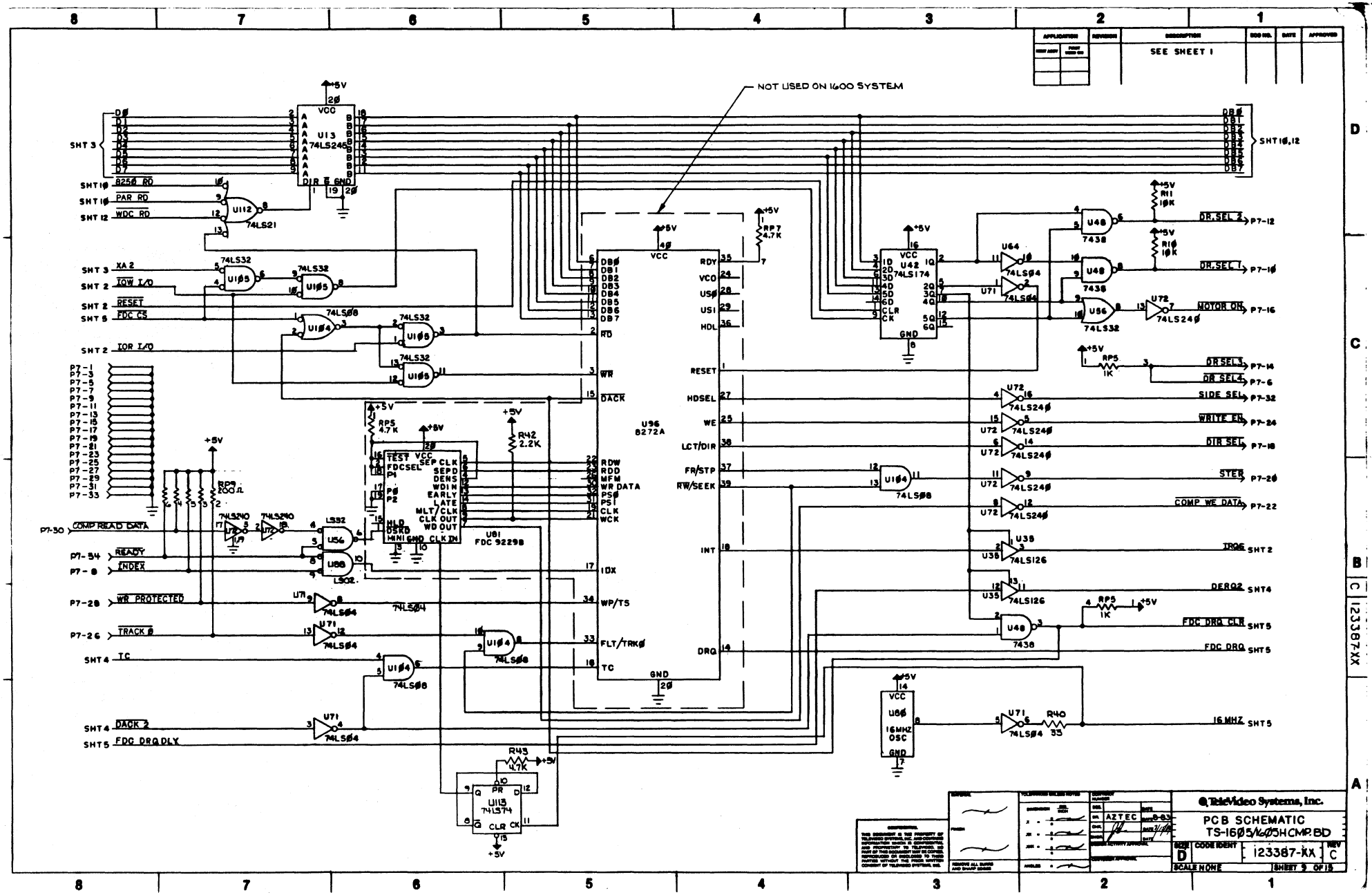

SHT8 REFRESH TIME OUT
SEE SHEET1
+5V
VCC
IOR
IOW
MEMR
MEMW
HLDA
READY
CS
RESET
DREQ1
DREQ2
DREQ3
AEN
DREQØ
CLK
U28
8237A-5
U34
74LS32
RP4
4.7K
U26
74LS74
PR
CK
CLR
HRQ
SHT5
EOP
U79
74LSØØ
TC
SHT9,11
DACKØ
SHT 5,11
DACK1
SHT11
DACK2
SHT9,11
DACK3
SHT11,12
DDØ-7
SHT 5,8
DMA CYC
CPU CYC
SHT3
U17
74LS245
U14
74LS245
DIR
GND
ADSTB
DENØ
DEN1
DT/R
U15
74LS67Ø
U16
74LS373
XA1
XAØ
DMA PG REQ CS
74LSØ2
U88
74LS27
U95
PROM ADDR
XA8
XA9
AZTEC
TeleVideo Systems, Inc.
PCB SCHEMATIC
TS-16Ø5/16Ø5H CMP. BD.
SIZE D
CODE IDENT 123387-XX
REV C
SCALE NONE
SHEET 4 OF 15

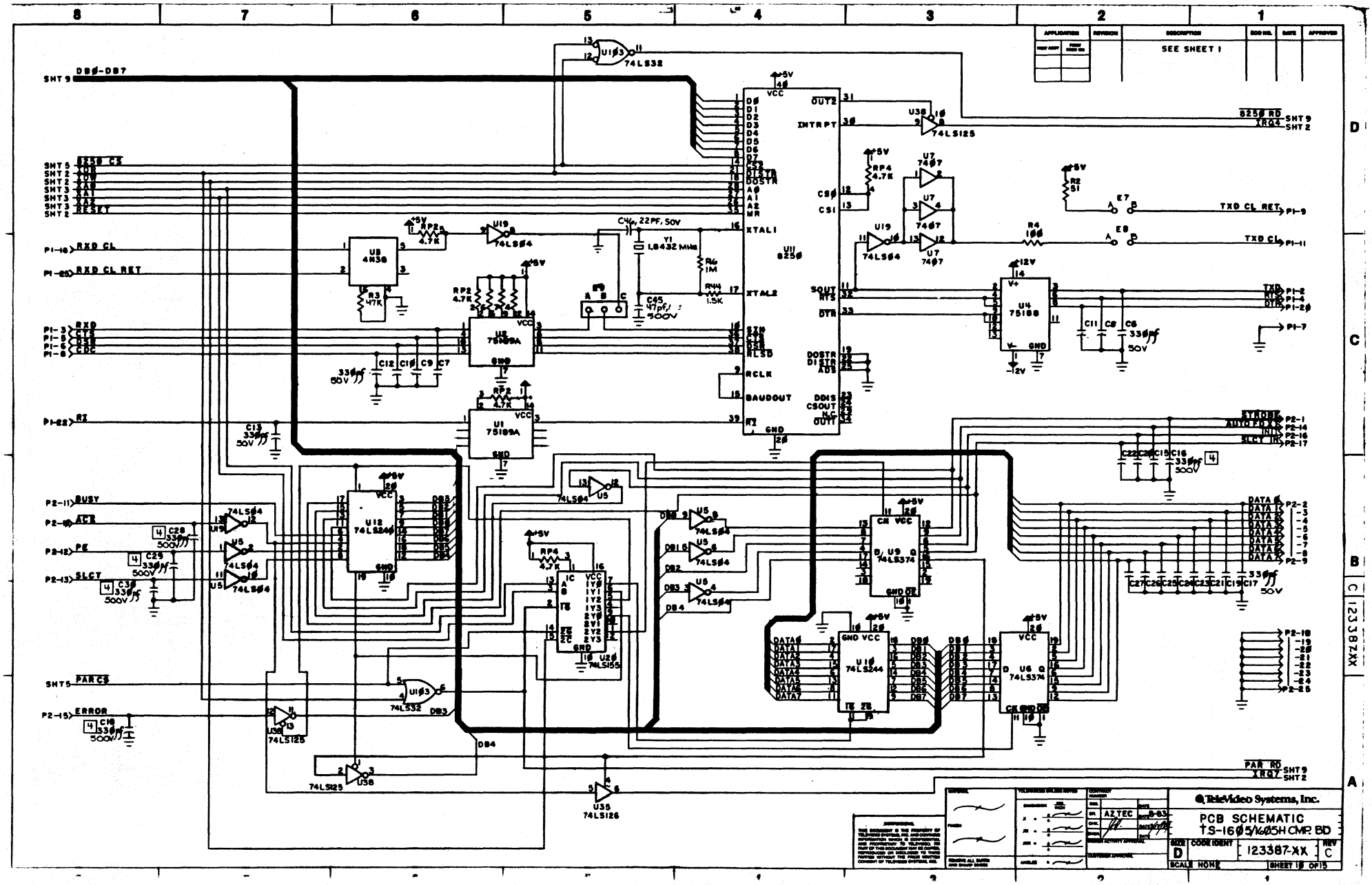

SEE SHEET 1
U32 AM27S21
U49 74LS08
U79 74LS00
U34 74LS32
U19 74LS04
DELAY LINE
U50
U58 74LS00
U57 74LS00
U73 74S241
U89 74LS04
U82 74LS00
U25 74LS08
U56 74LS32
U59 74LS138
RP5 4.7K
RP6 4.7K
6250 CS
FDC CS
PAR CS
WDC CS
RAS0
RAS1
RAS2
RAS3
CAS0
CAS1
CAS2
CAS3
RAM ADDR MUX
RAM SEL
HLDA
RDYI
AENI
DMARDY
FDC DRQ DLY
8254 CK
DMA CYC
CPU CYC
AEN
8237CS
8259CS
8254CS
8255CS
DMA RQ REQ CS
NMI
WDC CTL CS
I/O CH CK
MEMW
I/O CH CK
EN I/O CH CK
N.R INT
N.R INT SW
TeleVideo Systems, Inc.
PCB SCHEMATIC
TS-1605/1605H CMP BD
AZTEC
123387-XX
SCALE NONE
SHEET 5 OF 15

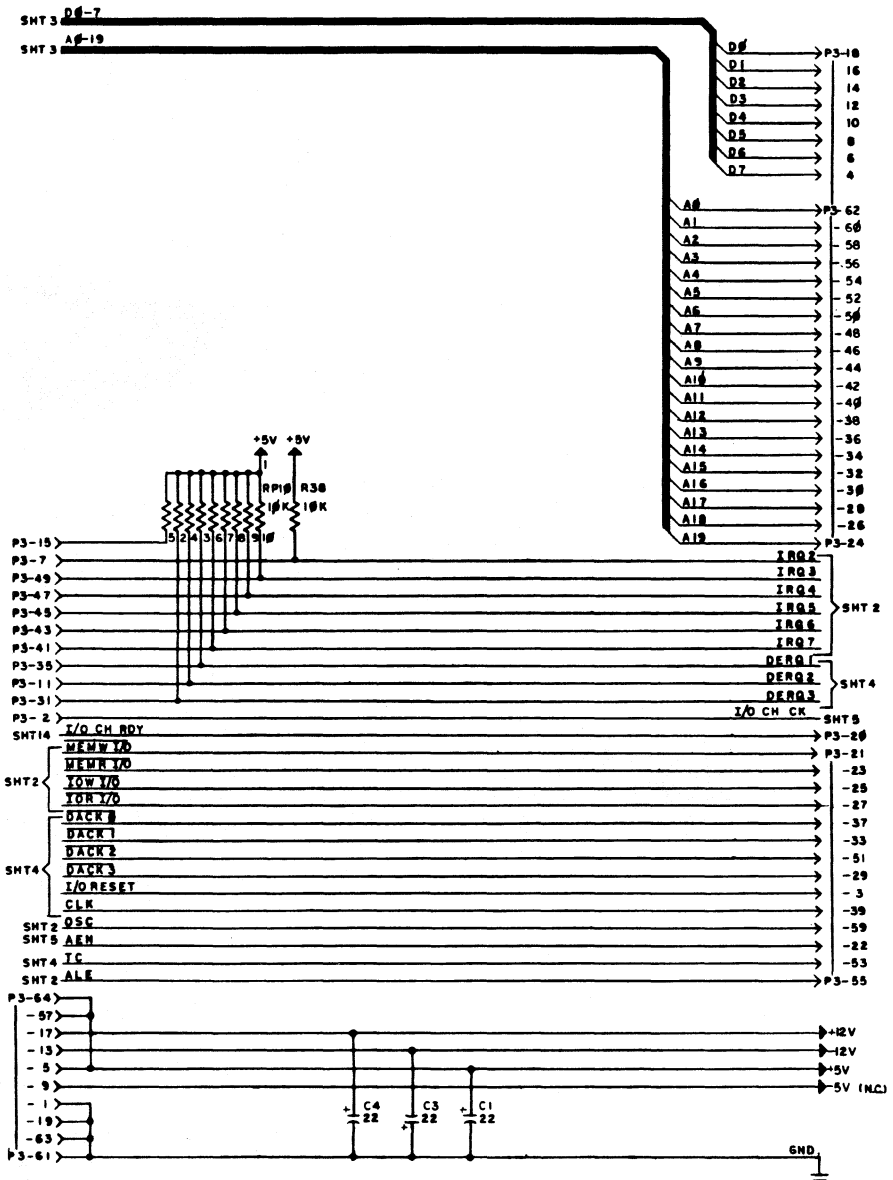

SHT5 RAS0
SHT5 CAS0
SHT2 MEMW
U73 74S241
R14 33
U65
U61
R15 33
A0-8 SHT7
SHT3 XA0 XA8 XA1 XA9 XA2 XA10 XA3 XA11
U46 74LS158
SHT3 XA4 XA12 XA5 XA13 XA6 XA14 XA7 XA15
U53 74LS158
SHT5 RAM ADDR MUX
SHT3 XA16
SHT3 XA17
U60 74LS158
RP6 4.7K +5V
SHT5 RAS1
SHT5 CAS1
SHT7
WE SHT7
U126 U119 U110 U101
U93 U86 U77 U69
U127 U118 U109 U100
U92 U85 U76 U68
SEE SHEET 1
TeleVideo Systems, Inc.
PCB SCHEMATIC
TS-1603/1605H CMP BD
AZTEC
123387-XX
SIZE D
REV C
SCALE NONE
SHEET 6 OF 15


SEE SHEET 1
SHT 5 RAS2
SHT 5 CAS2
U65 33
SHT 6
SHT 3
74LS245
SHT 2 MEMR
SHT 5 RAM SEL
SHT 5 RAS3
SHT 5 CAS3
SHT 6 WE
SHT 6 A0-8
U126
U117
U108
U99
U91
U84
U75
U67
U125
U116
U107
U98
U83
U74
U66
4164A-20
USED ON 1605 H SYSTEM
TeleVideo Systems, Inc.
PCB SCHEMATIC
TS-1605/1605HCMP BD
AZTEC
123387-XX
SCALE NONE
SHEET 7 OF 15


SEE SHEET 1
SPEAKER RET
SPEAKER OUT
TIMER OUT 2
SPK DATA
SPK GATE
REFRESH TIME OUT
EN I/O CH CK
KEY DATA
KEY CLOCK
KEY RESET
IRQ1
N.P. INT SW
U40 2764 OR 27128
U27 8254
U37 8255A-5
U33 74LS157
U36 74LS164
U26 74LS74
Q1 2N2222A
SW1
TeleVideo Systems, Inc.
PCB SCHEMATIC
TS-1605/1605H CMP BD
123387-XX
SHEET 8 OF 15


NOT USED ON 1600 SYSTEM
SEE SHEET 1
U96 8272A
U61 FDC 92298
U42 74LS174
U113 74LS74
U112 74LS21
U113 74LS245
U56 74LS32
U68 LS02
U71 74LS04
U72 74LS240
U72 74LS24Ø
U64 74LS04
U48 7438
U56 74LS32
U68 74LS08
U38 74LS126
U35 74LS126
U80 16MHZ OSC
U71 74LS04
R40 35
RP7 4.7K
RP5 4.7K
RP9 220Ω
R42 2.2K
R43 4.7K
R11 10K
R10 10K
RP5 1K
RP5 1K
+5V
GND
SHT 3
SHT 2
SHT 5
SHT 4
SHT 1Ø,12
B25Ø RD
PAR RD
WDC RD
XA 2
IOW I/O
RESET
FDC CS
IOR I/O
COMP READ DATA
READY
INDEX
WR PROTECTED
TRACK Ø
TC
DACK 2
FDC DRQ DLY
DR SEL 2
DR SEL 1
MOTOR ON
DR SEL 3
DR SEL 4
SIDE SEL
WRITE EN
DIR SEL
STEP
COMP WE DATA
IRQE
DERQ2
FDC DRQ CLR
FDC DRQ
16 MHZ
P7-12
P7-1Ø
P7-16
P7-14
P7-6
P7-32
P7-24
P7-18
P7-2Ø
P7-22
SHT 2
SHT4
SHT5
SHT5
SHT5
RDW
RDD
MFM
WR DATA
PSØ
PS1
CLK
WCK
IDX
WP/TS
FLT/TRKØ
TC
DACK
RDY
VCO
USØ
USI
HDL
RESET
HDSEL
WE
LCT/DIR
FR/STP
RW/SEEK
INT
DRQ
RD
WR
TEST
FDCSEL
P1
P2
SEP CLK
SEPD
DENS
WDIN
EARLY
LATE
MLT/CLK
CLK OUT
WD OUT
HLD
DSKD
MINI
GND
CLK IN
TeleVideo Systems, Inc.
PCB SCHEMATIC
TS-16Ø5/16Ø5HCMP BD
AZTEC
8-83
CODE IDENT
123387-XX
REV C
SIZE D
SCALE NONE
SHEET 9 OF 15
123387-XX


SEE SHEET 1
TeleVideo Systems, Inc.
PCB SCHEMATIC
TS-1605/1605H CMP BD
123387-XX
SCALE NONE
SHEET 1B OF 15



APPLICATION	REVISION	DESCRIPTION	ECO NO.	DATE	APPROVED
		SEE SHEET 1			

CONFIDENTIAL
THIS DOCUMENT IS THE PROPERTY OF TELEVIDEO SYSTEMS, INC. AND CONTAINS INFORMATION WHICH IS CONFIDENTIAL AND PROPRIETARY TO TELEVIDEO, IN PART OF THIS DOCUMENT MAY BE COPIED, REPRODUCED OR DISCLOSED TO THIRD PARTIES WITHOUT THE PRIOR WRITTEN CONSENT OF TELEVIDEO SYSTEMS, INC.

GENERAL
FINISH
REMOVE ALL BURRS AND SHARP EDGES
TOLERANCES UNLESS NOTED
DIMENSION
ANGLES

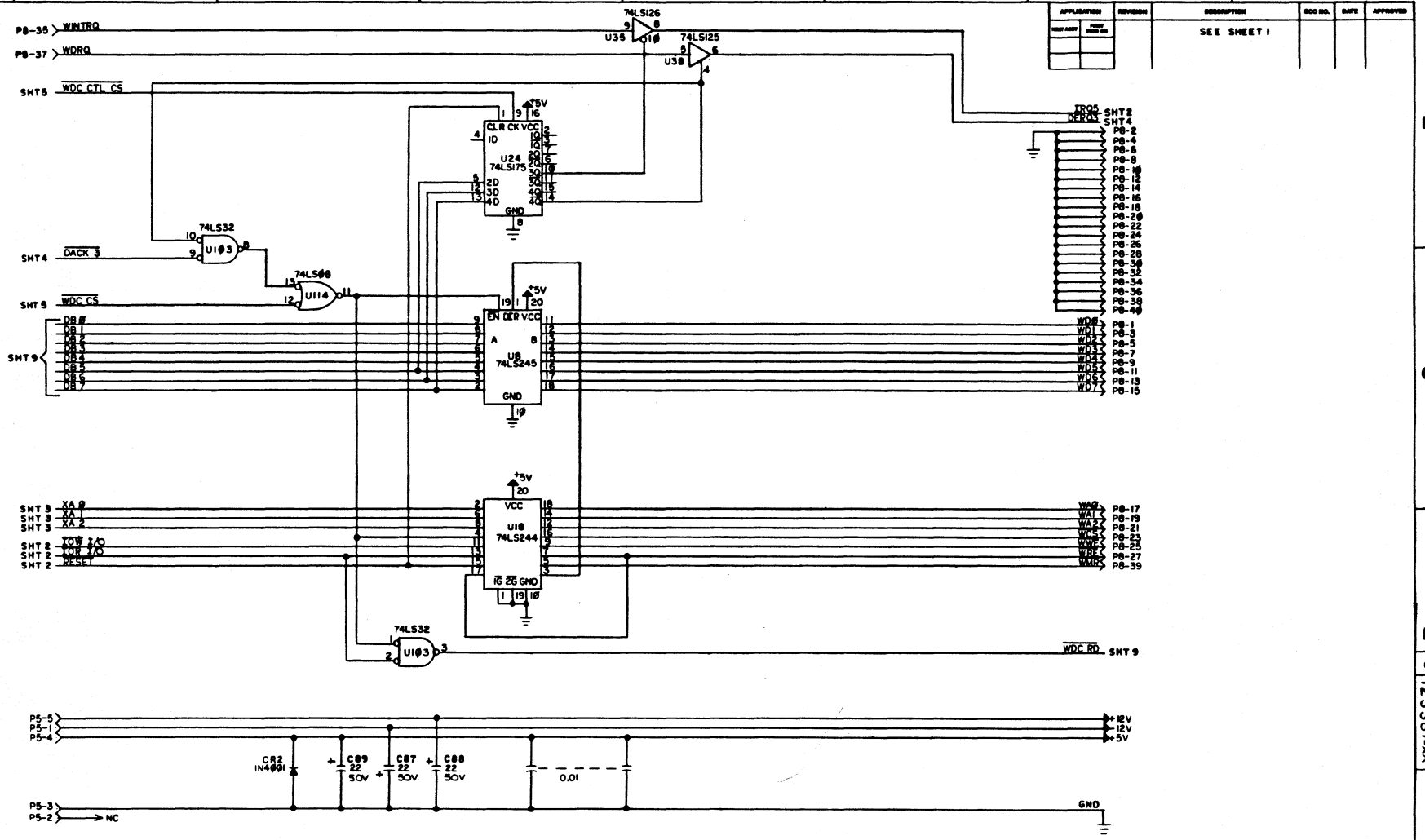
CONTRACT
AZTEC
DRAWN
CHECKED
ENGINEERING APPROVAL
MANUFACTURING APPROVAL
DATE 8/83

TeleVideo Systems, Inc.

PCB SCHEMATIC
TS-1605/1605H CMP.BD

SIZE D | CODE IDENT | 123387-XX | REV C
SCALE NONE | SHEET 11 OF 15

123387-XX



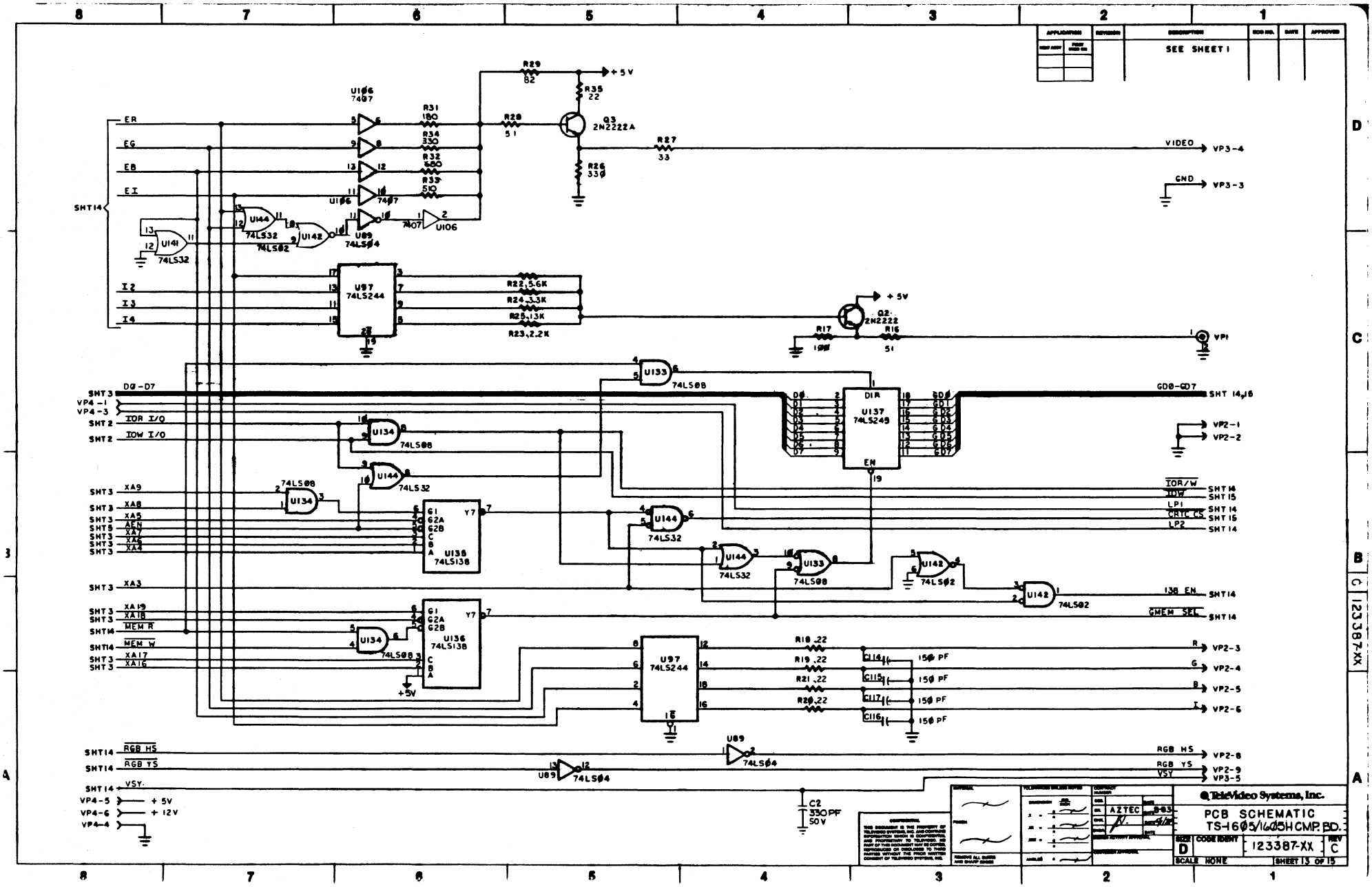
SEE SHEET 1

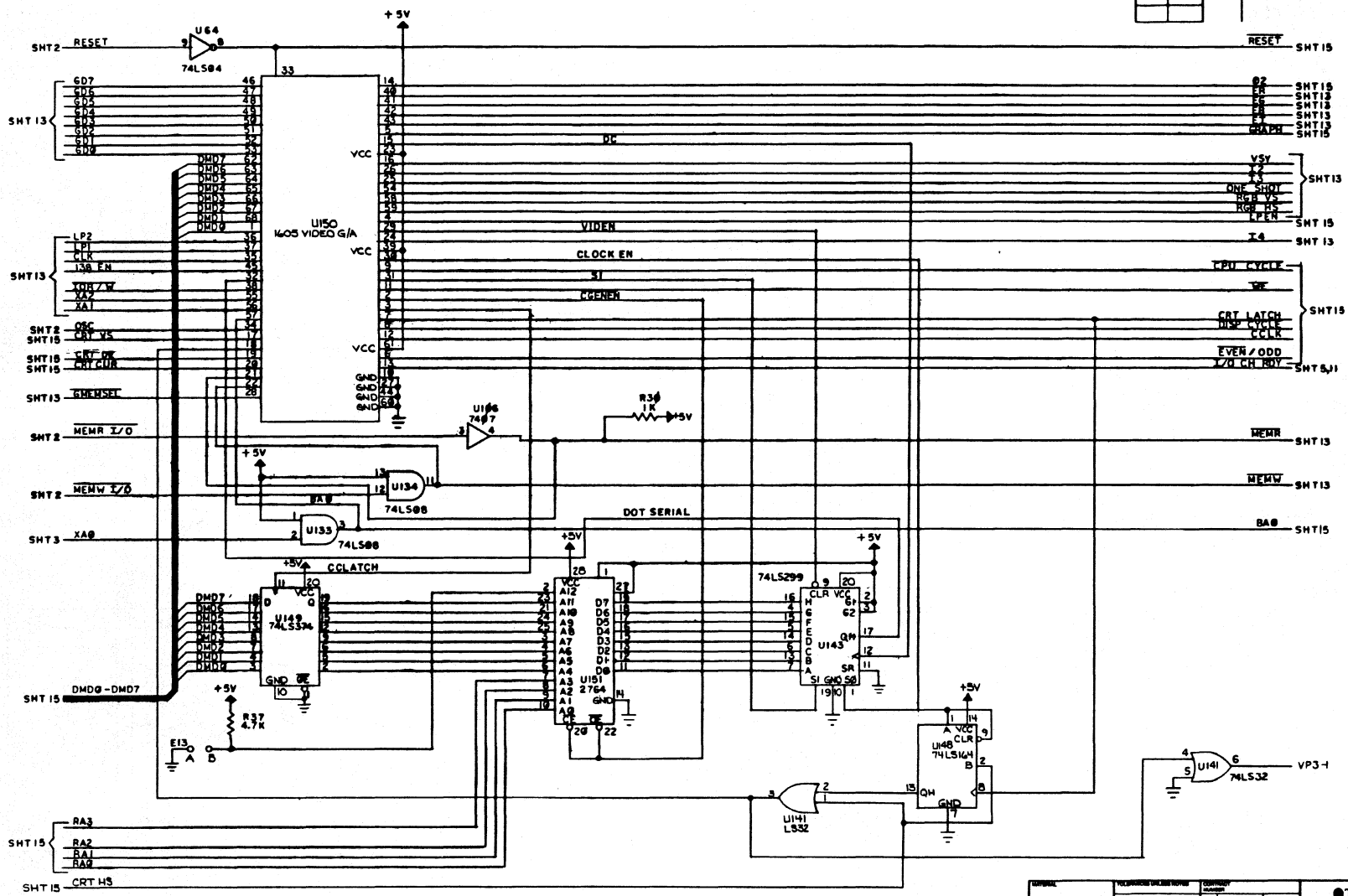
TeleVideo Systems, Inc.

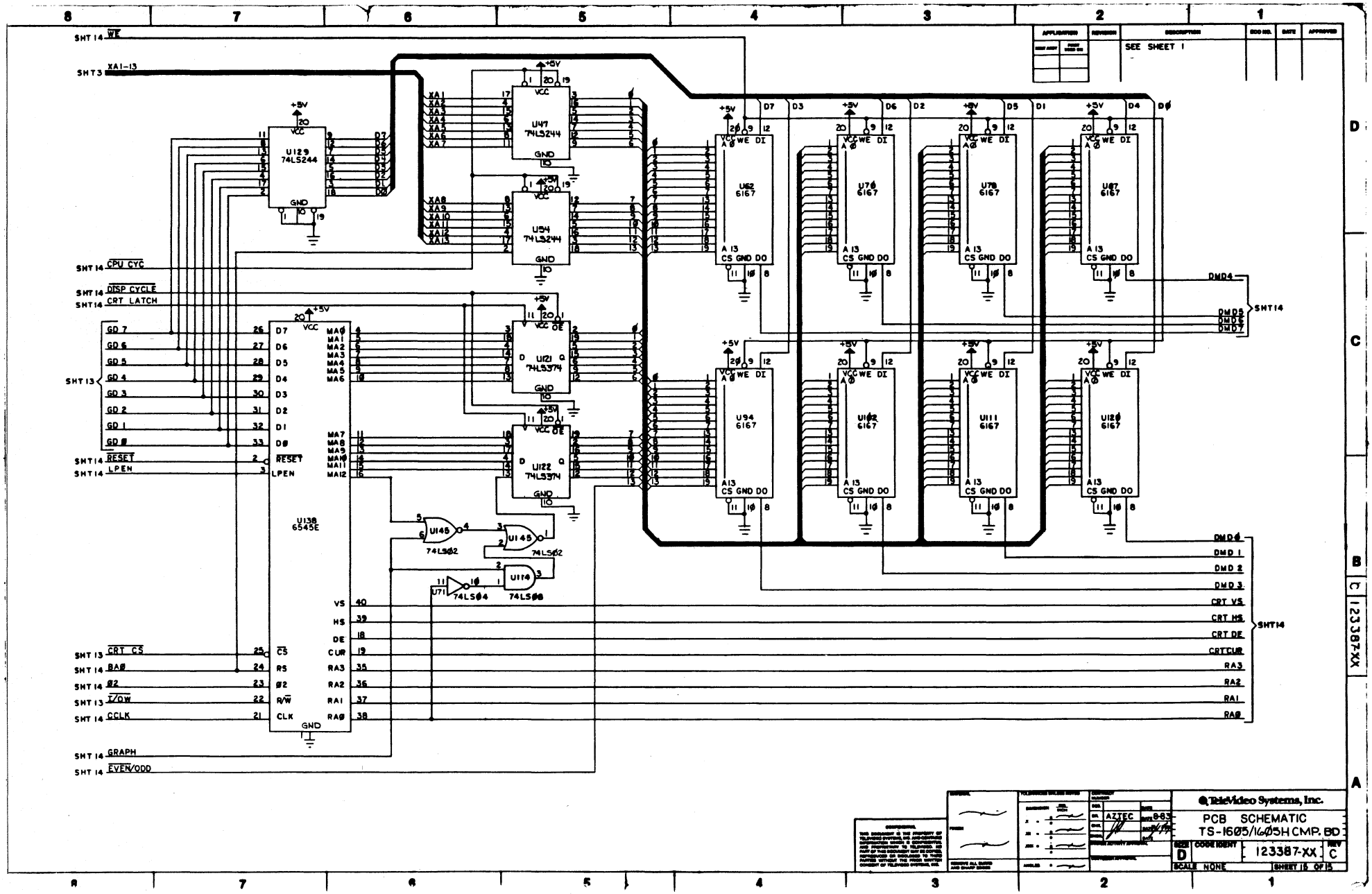
PCB SCHEMATIC
TS-1605/1605H CMP BD

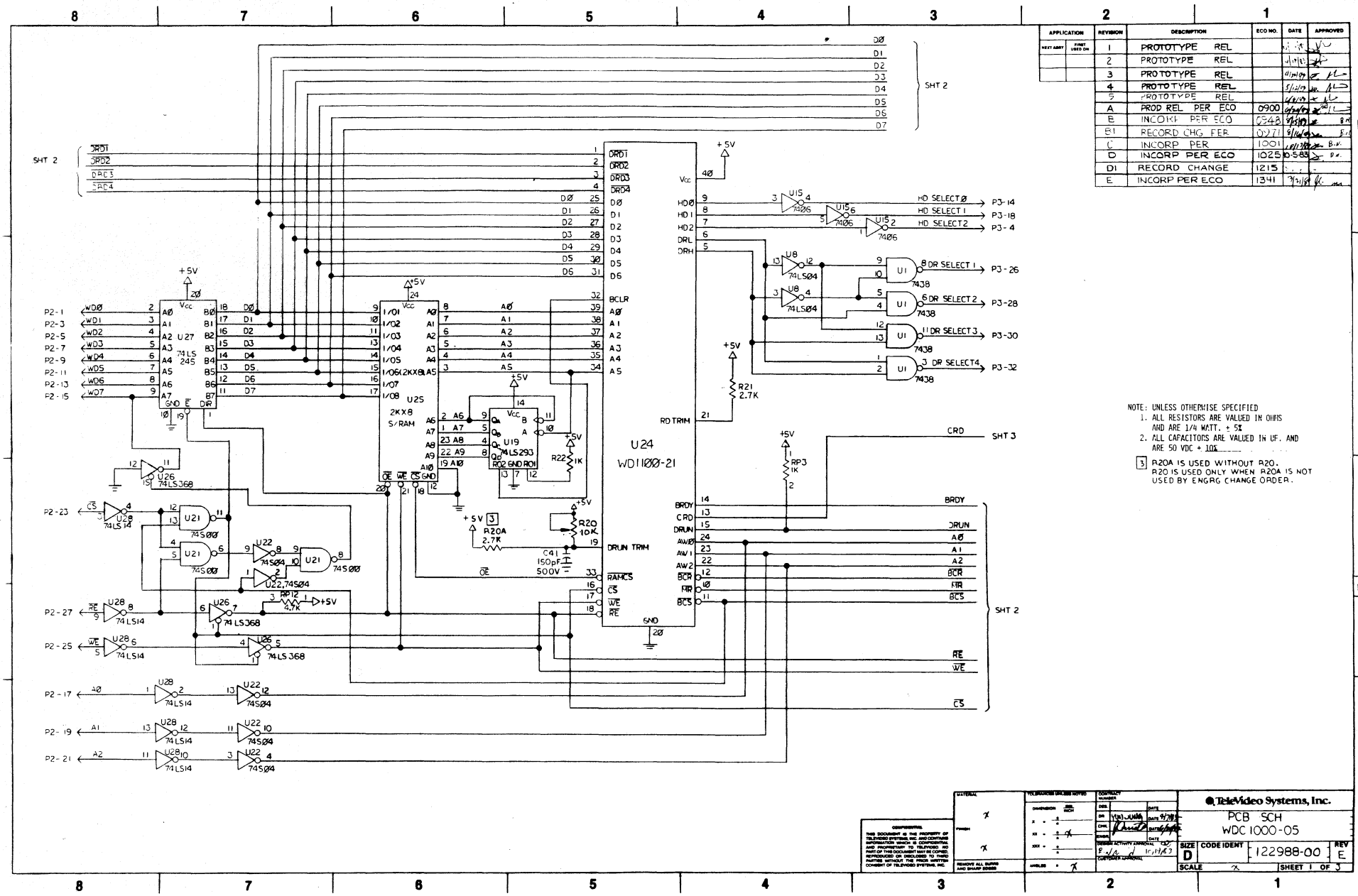
CODE IDENT 123387-XX
REV C
SCALE NONE
SHEET 12 OF 15

123387-XX


SEE SHEET 1
R29 82
+5V
R35 22
Q3 2N2222A
R28 51
R27 33
R26 330
VIDEO
VP3-4
GND
VP3-3
U106 7407
R31 180
R34 330
R32 680
R33 510
ER
EG
EB
EI
SHT14
U144 74LS32
U142 74LS02
U89 74LS04
U141 74LS32
U97 74LS244
I2
I3
I4
R22,5.6K
R24,3.3K
R25,1.3K
R23,2.2K
Q2 2N2222
R17 100
R16 51
VPI
U133 74LS08
DO-D7
SHT 3
VP4-1
VP4-3
SHT 2 IOR I/O
SHT 2 IOW I/O
U137 74LS245
DIR
EN
GD0-GD7
SHT 14,15
VP2-1
VP2-2
U134 74LS08
U138 74LS138
SHT 3 XA9
SHT 3 XA8
SHT 3 XA5
SHT 3 AEN
SHT 3 XA7
SHT 3 XA6
SHT 3 XA4
IOR/W SHT 14
IOW SHT 15
LPI SHT 14
CRTC CS SHT 15
LP2 SHT 14
SHT 3 XA3
SHT 3 XA19
SHT 3 XA18
SHT14 MEM R
SHT14 MEM W
SHT 3 XA17
SHT 3 XA16
U136 74LS138
+5V
138 EN SHT14
GMEM SEL SHT14
R18 ,22
R19 ,22
R21 ,22
R20 ,22
C114 150 PF
C115 150 PF
C117 150 PF
C116 150 PF
R
G
B
I
VP2-3
VP2-4
VP2-5
VP2-6
SHT14 RGB HS
SHT14 RGB YS
SHT14 VSY
RGB HS VP2-8
RGB YS VP2-9
VSY VP3-5
VP4-5 + 5V
VP4-6 + 12V
VP4-4
C2 330PF 50V
TeleVideo Systems, Inc.
PCB SCHEMATIC
TS-1605/1605H CMP. BD.
SIZE D
CODE IDENT 123387-XX
REV C
SCALE NONE
SHEET 13 OF 15
123387-XX


SEE SHEET 1
U64
74LS04
RESET
+5V
U150
1605 VIDEO G/A
VIDEN
CLOCK EN
SI
CGENEN
DC
DOT SERIAL
U134
74LS08
U133
74LS08
U148
74LS374
CCLATCH
U151
2764
74LS299
U143
U148
74LS164
U141
LS32
U141
74LS32
R37
4.7K
R36
1K
DMD0-DMD7
RA3
RA2
RA1
RA0
CRT HS
VP3-1
TeleVideo Systems, Inc.
PCB SCHEMATIC
TS-1605/1605H CMR BD
AZTEC
123387-XX
SCALE NONE
SHEET 4 OF 15


SHT 14 WE
SHT 3 XA1-13
SHT 14 CPU CYC
SHT 14 DISP CYCLE
SHT 14 CRT LATCH
SHT 13 GD 7
GD 6
GD 5
GD 4
GD 3
GD 2
GD 1
GD 0
SHT 14 RESET
SHT 14 LPEN
SHT 13 CRT CS
SHT 14 BA0
SHT 14 Ø2
SHT 13 I/OW
SHT 14 CCLK
SHT 14 GRAPH
SHT 14 EVEN/ODD
U129 74LS244
U47 74LS244
U54 74LS244
U121 74LS374
U122 74LS374
U138 6545E
U145 74LS02
U114 74LS08
U71 74LS04
U62 6167
U94 6167
U76 6167
U102 6167
U78 6167
U111 6167
U87 6167
U120 6167
DMD4
DMD5
DMD6
DMD7
DMD0
DMD1
DMD2
DMD3
CRT VS
CRT HS
CRT DE
CRTCUR
RA3
RA2
RA1
RA0
SHT14
SEE SHEET 1
TeleVideo Systems, Inc.
PCB SCHEMATIC
TS-1605/1605H CMP. BD
123387-XX
REV C
SCALE NONE
SHEET 15 OF 15



APPLICATION		REVISION	DESCRIPTION	ECO NO.	DATE	APPROVED
NEXT ASSY	FIRST USED ON	1	PROTOTYPE REL			
		2	PROTOTYPE REL			
		3	PROTOTYPE REL			
		4	PROTOTYPE REL			
		5	PROTOTYPE REL			
		A	PROD REL PER ECO	0900		
		B	INCORP PER ECO	0548		
		B1	RECORD CHG PER	0571		
		C	INCORP PER	1001		
		D	INCORP PER ECO	1025	10-5-83	
		D1	RECORD CHANGE	1215		
		E	INCORP PER ECO	1341		

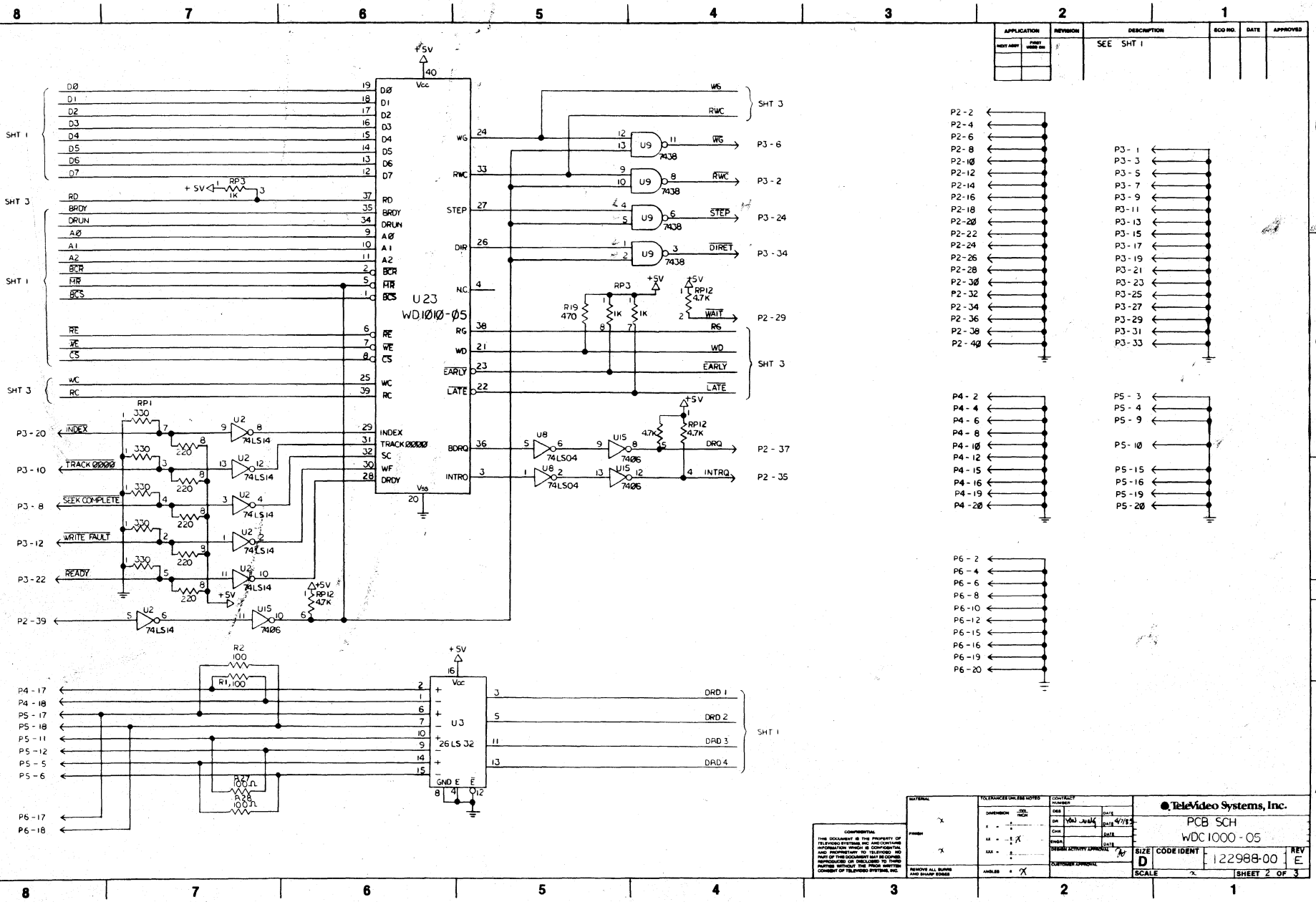
NOTE: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE VALUED IN OHMS AND ARE 1/4 WATT, ± 5%
2. ALL CAPACITORS ARE VALUED IN UF. AND ARE 50 VDC ± 10%
3. R20A IS USED WITHOUT R20. R20 IS USED ONLY WHEN R20A IS NOT USED BY ENGRG CHANGE ORDER.

CONFIDENTIAL
THIS DOCUMENT IS THE PROPERTY OF TELEVIDEO SYSTEMS, INC. AND CONTAINS CONFIDENTIALITY WHICH IS CONFIDENTIAL AND PROPRIETARY TO TELEVIDEO. NO PART OF THIS DOCUMENT MAY BE COPIED, REPRODUCED OR DISCLOSED TO THIRD PARTIES WITHOUT THE PRIOR WRITTEN CONSENT OF TELEVIDEO SYSTEMS, INC.

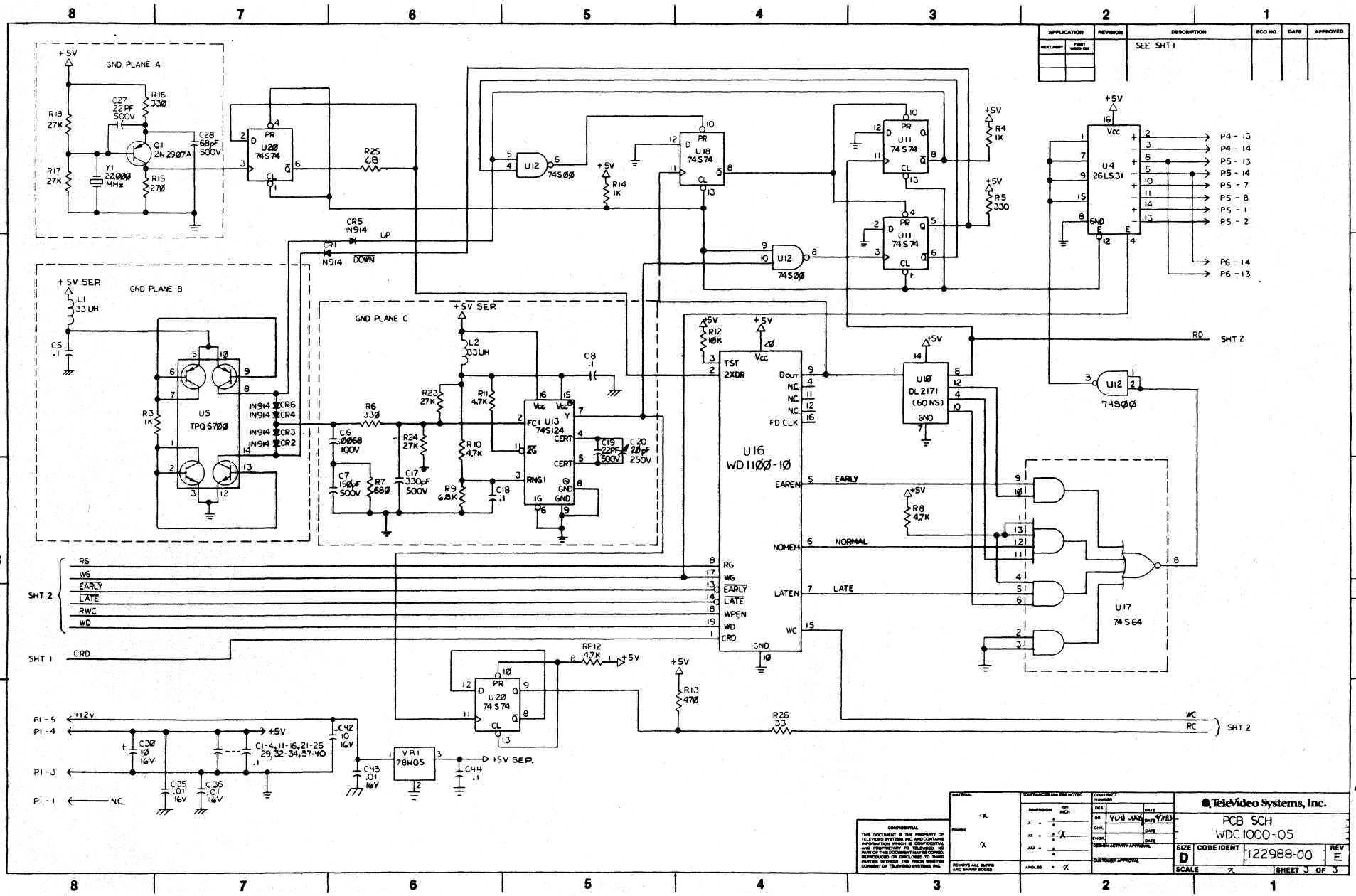
MATERIAL
FINISH
REMOVE ALL BURRS AND SHARP EDGES
TOLERANCES UNLESS NOTED
DIMENSION
ANGLES
CONTRACT NUMBER
DRN
CHK
ENGR
DESIGN ACTIVITY APPROVAL
CUSTOMER APPROVAL
DATE

TeleVideo Systems, Inc.
PCB SCH
WDC 1000-05
SIZE D | CODE IDENT | 122988-00 | REV E
SCALE | SHEET 1 OF 3

122988-00 1 of 3



122988-00 2 of 3


GND PLANE A
GND PLANE B
GND PLANE C
+5V SEP.
SEE SHT 1
WDC1000-05
PCB SCH
TeleVideo Systems, Inc.
SIZE D
CODE IDENT 122988-00
REV E
SHEET 3 OF 3
122988-00 3 of 3
122988-00
E