Model 950 Maintenance Manual

TeleVideo Systems, Inc.

Model 950 Maintenance Manual

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November 1983

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PREFACE

Any comments and suggestions on this manual are welcome. Please address them to:

TeleVideo Systems, Inc.
1170 Morse Ave.
Sunnyvale, CA 94086

LIMITED WARRANTY POLICY AND SERVICE OUT OF WARRANTY

STATEMENT OF LIMITED WARRANTY

TeleVideo Systems, Inc. ("TeleVideo") warrants to its distributors, systems houses, and OEMs ("Buyer"), that products manufactured by TeleVideo are free from defects in materials and workmanship. TeleVideo's obligations under this warranty are limited to repairing or replacing, at TeleVideo's option, the part or parts of the products which prove defective in material or workmanship within 180 days after shipment by TeleVideo. Buyer may pass along to its initial customer or user ("Customer") a maximum of 90 days coverage within this 180-day warranty period, provided that Buyer gives TeleVideo prompt notice of any defect and satisfactory proof thereof.

Products may be returned by Buyer only after a Return Material Authorization number ("RMA") has been obtained from TeleVideo by telephone or in writing. Buyer will prepay all freight charges to return any products to the repair facility designated by TeleVideo and include the RMA number on the shipping container. TeleVideo will, at its option, either repair the defective products or parts or deliver replacements for defective products or parts on an exchange basis to Buyer, freight prepaid to the Buyer or the Customer. Products returned to TeleVideo under this warranty will become the property of TeleVideo. With respect to any product or part thereof not manufactured by TeleVideo, only the warranty, if any, given by the manufacturer thereof, applies.

Exclusions

This limited warranty does not cover losses or damage which occur in shipment to or from Buyer or Customer, or are due to, (1) improper installation or maintenance, misuse, neglect or any cause other than ordinary commercial or industrial application, or (2) adjustment, repair, or modifications by other than TeleVideo-authorized personnel, or (3) improper environment, excessive or inadequate heating or air conditioning and electrical power failures, surges, or other irregularities, or (4) any statements made about TeleVideo's products by salesmen, dealers, distributors or agents, unless confirmed in writing by a TeleVideo officer.

If the firmware or hardware is altered or modified by the Buyer or Customer, this firmware and hardware is not covered within this limited warranty and the Buyer or Customer bears sole responsibility and liability for that firmware and hardware.

THE FOREGOING TELEVIDEO LIMITED WARRANTY IS IN LIEU OF ALL OTHER WARRANTIES, WHETHER ORAL, WRITTEN, EXPRESSED, IMPLIED, OR STATUTORY. IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE DO NOT APPLY. TELEVIDEO'S WARRANTY OBLIGATIONS AND DISTRIBUTER'S REMEDIES HEREUNDER ARE SOLELY AND EXCLUSIVELY AS STATED HEREIN.

TELEVIDEO'S LIABILITY, WHETHER BASED ON CONTRACT, TORT, WARRANTY, STRICT LIABILITY, OR ANY OTHER THEORY, SHALL NOT EXCEED THE PRICE OF THE INDIVIDUAL UNIT WHOSE DEFECT OR DAMAGE IS THE BASIS OF THE CLAIM. IN NO EVENT SHALL TELEVIDEO BE LIABLE FOR ANY LOSS OF PROFITS, LOSS OF USE OF FACILITIES OR EQUIPMENT, OR OTHER INDIRECT, INCIDENTAL OR CONSEQUENTIAL DAMAGES.

SERVICE OUT OF WARRANTY

If your terminal is out of warranty when it needs service, follow the same procedure to receive an RMA. You will be responsible for all shipping costs.

If your company requires a purchase order for out-of-warranty repairs, let us know the purchase order number when you call in. One purchase order may cover several repairs but we will give each unit its own individual RMA number. This allows us to return each unit quickly without holding up the entire purchase order for one unit.

EXTENDED WARRANTY

TeleVideo offers an Extended Warranty Agreement, which extends the terms of the above-stated Limited Warranty for an additional year. To take advantage of this Extended Warranty, you must sign the Extended Warranty Agreement and return it, together with full payment, to TeleVideo before the Limited Warranty expires. Shipping charges are not included in the Extended Warranty. This is normally the only expense you incur. Please contact the Customer Service department or your sales representative for details. To renew the Extended Warranty for another year, follow the same procedure.

ORDERING SPARE PARTS

Order parts directly from the Terminal Division's Spare Parts Order Entry department in Sunnyvale, California. Call (408) 745-7760 or (800) 538-8725 (outsjde California). Please have the purchase order number and TeleVideo part number ready when you call. International customers can telex 910-339-9621, attention Terminal Spares Order Entry.

Contract customers and institutions can order parts on a purchase order and be invoiced. All other customers must order parts on a C.O.D. or cash-in-advance basis.

ALL orders (except manuals) have a $50.00 minimum. Add 6.5% sales tax to orders placed in California. There is also a shipping and handling charge of $10.00 per order. Since we do not make any drop shipments, please include the shipping and billing addresses with your order. Shipments are made Best Way, which is UPS. Although special shipping requests will be accommodated, any extra costs incurred will be added to the invoice.

Regional Sales Offices

Eastern
6900 Jericho Turnpike, Suite 100 LL
Syosset, NY 11791
(516) 496-4777

West
18662 MacArthur Blvd., Suite 107
Irvine, CA 92715
(714) 476-0244

South
5525 High Point Dr., Suite 101
Irving, TX 75062
(214) 258-6776

Southeast
5901-C Peachtree Dunwoody Rd.,
Suite 260
Atlanta, GA 30328
(404) 399-6464

Central Europe
Saturnusstraat 25
2132 HB Hoofddorp
The Netherlands
Phone: (0) 2503-35444
Telex: 74615 TLVDO NL

Northern Europe
Dorna House,
Guildford Rd., West End
Surrey GU249PW
England
Phone: 011-44 (9) 905-6464
Telex: 858922

Northeast
1601 Trapelo Road
Reservoir Place
Waltham, MA 02154
(617) 890-3282

Northwest
1170 Morse Ave.
Sunnyvale, CA 94086
(408) 745-7760

Midwest
125 E. Lake, Suite 203
Bloomingdale, IL 60108
(312) 351-9350

Southern Europe
3 bis rue le Corbusier
Silic 244
94568 Rungis Cedex,
FRANCE
Phone: 011-33 (1) 687-3440
Telex: 205191F

TeleVideo® Systems, Inc.

May 16, 1983
TERMINAL SPARE PART PRICE LIST
REVISED 9-13-83

DESCRIPTION	NEW P/N	LIST PRICE
MANUALS		
INSTAL & USER GUIDE 910	2002500	5.00
INSTAL & USER GUIDE 910PLUS	2004600	5.00
INSTAL & USER GUIDE 912/920	2001800	5.00
INSTAL & USER GUIDE 925	2003500	5.00
INSTAL & USER GUIDE 950	2002000	5.00
INSTAL & USER GUIDE 970	2244600	10.00
INSTAL & USER GUIDE 970/50	3090200	25.00
MAINTENANCE MANUAL 910/910PLUS	2002600	50.00
MAINTENANCE MANUAL 912/920	2001900	50.00
MAINTENANCE MANUAL 925	2003600	50.00
MAINTENANCE MANUAL 950	2002100	50.00
MAINTENANCE MANUAL 970	3002100	50.00
MODULES		
POWER SUPPLY MODULE	2195700	91.00
POWER SUPPLY MODULE 970	2225700	120.00
VIDEO MODULE	2195800	93.00
VIDEO MODULE 970	2226900	110.00
LOGIC BOARD 910 TTL	2014000	395.00
LOGIC BOARD 910 G/A	2014001	395.00
LOGIC BOARD 910PLUS TTL	2014002	395.00
LOGIC BOARD 910PLUS G/A	2246900	395.00
LOGIC BOARD 912/920B TTL	2009000	458.00
LOGIC BOARD 912/920C TTL	2009002	458.00
LOGIC BOARD 925 TTL	2015500	514.00
LOGIC BOARD 925 G/A	2015501	514.00
LOGIC BOARD 950 TTL	2009500	539.00
LOGIC BOARD 950 G/A	2009501	539.00
LOGIC BOARD 970	2021000	750.00
KEYBOARD ASSEMBLY 910/910PLUS	2090001	105.00
KEYBOARD ASSEMBLY 912B	2206500	105.00
KEYBOARD ASSEMBLY 912C	2090000	105.00
KEYBOARD ASSEMBLY 920B	2089900	126.00
KEYBOARD ASSEMBLY 920C	2090100	126.00
KYBD ASSEMBLY W/HOUSING 925/950	2090200	175.00
KYBD ASSEMBLY W/HOUSING 970	2183700	210.00
TUBE B/W P4 12"	2049100	179.00
TUBE GREEN P31 12"	2049300	179.00
TUBE GREEN P31 14"	2218700	192.00
OPTIONS		
PATTERN GENERATOR (912/950 INSTALLED)	2122300	200.00
DEMO PROGRAM EPROM 910	8000094	16.00
DEMO PROGRAM EPROM 910PLUS	8000073	16.00
DEMO PROGRAM EPROM 925	8000072	16.00
DEMO PROGRAM EPROM 950	8000074	16.00
DEMO PROGRAM EPROM 970	8000119	16.00
CONVERSION KIT 910	2169700	25.00

CONVERSION KIT 910PLUS	2169100	25.00
CONVERSION KIT 970/50	3007300	100.00
CONVERSION KIT CP/M WORDSTAR 925	2250900	100.00
CONVERSION KIT CP/M WORDSTAR 950	2187400	100.00
CURRENT LOOP KIT 910/910PLUS	2131000	50.00
CURRENT LOOP KIT 925	2131100	60.00
MEMORY KIT 2ND PAGE 912/920	2001400	35.00
MEMORY KIT 2ND PAGE 925/950	2001500	40.00
MEMORY KIT 3RD 4TH PAGE 950	2001600	80.00
MEMORY KIT 2ND 3RD 4TH PAGE 950	2231700	120.00

KITS

SP PTS LOGIC BOARD 910 TTL	2000600	112.22
SP PTS LOGIC BOARD 910 G/A	2225400	158.12
SP PTS LOGIC BOARD 910PLUS TTL	2000800	124.19
SP PTS LOGIC BOARD 910PLUS G/A	2225500	162.70
SP PTS LOGIC BOARD 912/920 TTL	2000000	150.80
SP PTS LOGIC BOARD 925 TTL	2001000	135.71
SP PTS LOGIC BOARD 925 G/A	2225300	181.61
SP PTS LOGIC BOARD 950 TTL	2000400	183.08
SP PTS LOGIC BOARD 950 G/A	2233000	218.90
SP PTS LOGIC BOARD 970	3208800	299.49
SP PTS MECH 910/910PLUS	2000900	60.23
SP PTS MECH 912/920	2000200	66.03
SP PTS MECH 925/950	2000500	54.05
SP PTS POWER SUPPLY/VIDEO MOD	2000100	134.28
SP PTS POWER SUPPLY/VIDEO MOD 970	3007100	115.99
SP PTS ADDITIONAL PARTS ALL	2000300	202.25
SP PTS MECH 970	3007200	80.73

ELECTRICAL COMPONENTS — CAPACITORS

CAP CERAMIC .02uF 50V	3018600	.72
CAP CERMAIC 150uF 50V 100%	3013800	.72
CAP CERAMIC 1.0uF 1KV SPARK GAP	2030900	2.04
CAP CERAMIC 220uF 50V	2195900	.72
CAP CERAMIC .01uF 50V	3017800	.72
CAP CERAMIC .01uF 16V 20%	2028700	.72
CAP CERAMIC 330PF 50V 20%	2029100	.72
CAP CERAMIC 3300uF 10V	3027600	.72
CAP CERAMIC .1uF 50V 10%	2030100	.72
CAP DIP MICA 10pF	2024100	.72
CAP ELECTROLYTIC (NON-P) 16uF 25V	2280000	4.63
CAP ELECTROLYTIC 22uF 15V	2025700	.72
CAP ELECTROLYTIC 2.2uF 25V 10%	2026500	.72
CAP ELECTROLYTIC 22uF 16V 20%	3018900	.72
CAP ELECTROLYTIC 22uF 50V	2026100	.72
CAP ELECTROLYTIC 4.4uF 35V 10%	2026900	2.08
CAP ELECTROLYTIC 10uF 16V 20%	2027300	.72
CAP ELECTROLYTIC 1uF 16V 10%	2027900	1.08
CAP ELECTROLYTIC 100uF 10V	2196000	.72
CAP ELECTROLYTIC 22uF 100V	2196100	.72
CAP ELECTROLYTIC 2.2KuF 10V	2196200	2.28
CAP ELECTROLYTIC 2.2KuF 16V	3016400	6.60
CAP ELECTROLYTIC 100uF 160V	2196300	6.60
CAP ELECTROLYTIC 22uF 160V	2196400	1.27
CAP ELECTROLYTIC 220uF 16V	2199300	.72
CAP ELECTROLYTIC 220uF 25V	3012700	.72

CAP ELECTROLYTIC 1000uF 16V	3018500	.72
CAP ELECTROLYTIC 3.3KuF 35V	2196500	6.91
CAP ELECTROLYTIC 3300uF 50V	3028100	5.94
CAP ELECTROLYTIC 2200uF 35V	3027500	3.24
CAP ELECTROLYTIC 4.7KuF 16V	2196600	6.56
CAP ELECTROLYTIC 4.7uF 16V	2196700	.72
CAP ELECTROLYTIC 470uF 35V	2198200	1.68
CAP MICA 20pF	2024300	.72
CAP MICA 100pF 50V 5%	2024700	.72
CAP MICA 47pF 50V 5%	2024900	.72
CAP MICA 150pF 500V 1%	2025100	.72
CAP MICA 330pF 500V 5%	2025300	.95
CAP MICA 390pF 500V 5%	2025500	1.07
CAP MONOLYTHIC.01uF 50V 10%	2028900	.72
CAP MONOLYTHIC 330pF 100V 20%	2029300	.72
CAP MONOLYTHIC 47pF 100V 5%	2029500	1.08
CAP MONOLYTHIC 68pF 1KV 20%	2029900	.72
CAP MONOLYTHIC .039uF 50V 10%	2030300	.72
CAP MONOLYTHIC .039uF 50V 5%	2030500	1.08
CAP MYLAR .1pF 100V	3016900	.72
CAP MYLAR .047pF 50V	3016800	.72
CAP MYLAR .0068uF 100V 5%	2028100	.72
CAP MYLAR .0068uF 200V	2196800	.72
CAP MYLAR .001uF 50V	2196900	.72
CAP MYLAR .01uF 50V	2197000	.72
CAP MYLAR .015uF 50V 5%	3013900	.72
CAP MYLAR .033uF 400V	3012600	.72
CAP MYLAR .039uF 50V	3014500	.72
CAP MYLAR .047uF 50V	2197100	.72
CAP MYLAR .47uF 50V	2197200	1.44
CAP MYLAR .47uF 100V	3018800	2.82
CAP MYLAR .1uF 600V	2197300	1.35
CAP MYLAR .1uF 800V 10%	3018400	.96
CAP MYLAR .047uF 400V	2197500	1.86
CAP TANTALUM .22uF 35V	2028500	.72
CAP TANTALUM .68uF 50V	2025900	1.74
CAP TANTALUM 2.2uF 35V	3027400	.72
CAP TANTALUM 3.3uF 50V 10%	2026300	2.40
CAP TANTALUM 10uF 25V 10%	2027100	1.98
CAP TANTALUM 4.7uF 16V 10%	2027500	.96
CAP TANTALUM 4.7uF 25V	3028400	.72
CAP TANTALUM .33uF 35V	2198100	1.20

DIODES - REGULATORS - TRANSISTORS

DIODE ZENER IN759A/RD12EB	2201600	1.82
DIODE ZENER IN747	2207000	.72
DIODE IN914	2047500	.72
DIODE IN920/KDS8513A	2201800	.90
DIODE IN4001	2047700	.91
DIODE IN4004/DS-130TB	2202200	1.00
DIODE IN5391/DS135D	2200600	.72
DIODE DSA17C/MR500	2201500	1.94
DIODE DS18/IDS135D	2201400	.72
DIODE DS113A/MRI-1000	2201700	6.29
DIODE LED MV55A RED	2048100	3.00
DIODE P6KE	2047900	4.20
DIODE PLR 817	3014700	.72
DIODE PFR 852	3025100	.72
DIODE BY251 3A 200V	3009800	.72

DIODE SWITCH IN4148	2048500	.72
REGULATOR LAS1512	2202500	35.00
REGULATOR LAS16CB	2126900	18.60
REGULATOR LAS1605	2126800	23.70
REGULATOR LAS1812	2202400	35.00
REGULATOR 78MO5	2126100	3.96
REGULATOR 79LO5AC	2126200	2.40
REGULATOR 3122P	3001700	6.18
REGULATOR 7912	3001800	3.18
REGULATOR SI-80506Z	2246400	31.86
TRANSISTOR 2N2219A	2045300	3.60
TRANSISTOR 2N2907A	2045900	.97
TRANSISTOR 2N3019	2045700	2.64
TRANSISTOR 2N3906/2SA495	2042200	.91
TRANSISTOR 2N4401/2SC1166	2045500	2.02
TRANSISTOR 2N5551/2SC983	2047100	2.59
TRANSISTOR 2N6121/2SC1173	2199700	4.00
TRANSISTOR 2N6124/2SA473	2202100	4.28
TRANSISTOR 2SC2373/MJE13006	2047300	4.63
TRANSISTOR KTC 1627A/MPSA06	2046700	2.07
TRANSISTOR 2N3904/KTC1815	2046500	4.50
TRANSISTOR B595	3001600	.72
TRANSISTOR KTC 2229Y	3011600	.72
TRANSISTOR KTC 1815Y	3014600	.72
TRANSISTOR KTA 1015Y	3016700	.72
TRANSISTOR KTC 200Y	3011700	.72

FIRMWARE

SYSTEM PROG EPROM 910	8000020	37.50
SYSTEM PROG EPROM 910PLUS	8000040	25.00
SYSTEM PROG ROM 912/920B (A49B1)	2033800	25.80
SYSTEM PROG ROM 912/920C (A49C1)	2034000	25.80
SYSTEM PROG EPROM 925 A	8000033	37.50
SYSTEM PROG EPROM 925 B	8000031	37.50
SYSTEM PROG ROM 950 (-001A)	8000001	18.90
SYSTEM PROG ROM 950 (-007A)	8000007	18.90
SYSTEM PROG EPROM 950 (043X)	8000043	37.50
SYSTEM PROG EPROM 950 (044X)	8000044	37.50
SYSTEM EPROM 970 (A82)	8000100	37.50
SYSTEM EPROM 970 (A87)	8000101	37.50
SYSTEM EPROM 970 (A99)	8000102	37.50
SYSTEM EPROM 970/950 (A82)	8000170	37.50
SYSTEM EPROM 970/950 (A87)	8000171	37.50
SYSTEM EPROM 970/950 (A99)	8000172	37.50
CHAR GEN EPROM 910/910PLUS	8000021	37.50
CHAR GEN ROM 910/910PLUS	8000016	18.90
CHAR GEN ROM 912/920 (A3-2)	2034600	14.94
CHAR GEN EPROM 925	8000021	37.50
CHAR GEN ROM 925	8000016	18.90
CHAR GEN ROM 950 (003A)	8000003	18.90
CHAR GEN ROM 950 (002A)	8000002	18.90
*KYBD EPROM PRO 910/910PLUS	8000019	21.00
**KYBD ENCDR PRO 910/910PLUS	2053200	22.50
KYBD ENCDR 910/910PLUS	2051800	22.50
KYBD CPU 925/950 8048 (U6)	8000009	37.50
KYBD CPU 970 8049 (A6)	8000103	37.50

* Used with KYBD ENCODER 2053200
**Used with KYBD EPROM 8000019

INTERGRATED CIRCUITS

IC 74S00	2024000	2.20
IC 74LS00	2024200	1.72
IC 74LS03	2024400	1.72
IC 74S04	2024600	2.41
IC 74LS04	2024800	1.80
IC 74LS05	2025000	1.80
IC 74LS08	2025200	1.80
IC 74LS10	2025400	1.80
IC 74SL20	2025600	1.72
IC 74LS32	2025800	1.86
IC 74LS42	2026000	2.55
IC 74LS51	2026200	1.80
IC 74S74	2026400	3.58
IC 74H74	3023200	3.00
IC 74LS86	2026800	2.07
IC 74LS109	2027000	2.00
IC 74LS139	2027200	3.18
IC 74LS145	2170000	3.08
IC 74LS157	2027400	2.76
IC 74LS163	2027600	4.56
IC 74LS166	2027800	5.04
IC 74LS173	2028000	4.14
IC 74LS174	2028200	3.18
IC 74LS253	2028400	3.24
IC 74LS367	2028600	2.76
IC 74LS373	2028800	3.48
IC 74LS374	2029000	3.48
IC 75188N/1488	2029200	4.14
IC 75189AN/1489	2029400	4.14
IC TIL117	2029800	4.48
IC NE555	2030200	2.58
IC DP8304	2030400	17.59
IC AMD2111-4A	2030600	13.32
IC 2502HP	2030800	15.52
IC TMS9927/5027	2031000	81.76
IC P8035	2031200	41.05
IC H11G3	2034200	3.45
IC 7406	2034800	2.05
IC 4N38	2035000	4.32
IC 7414	2035400	1.92
IC 2114	2035800	9.75
IC 74LS245/N8T245N	2036200	5.76
IC 74LS191	2036600	2.70
IC 74LS273	2037600	3.48
IC 74S240	2037800	8.82
IC 74LS175	2038000	1.74
IC 74S32/629	2038800	1.80
IC 74LS11	2040000	1.14
IC 93S16PC	2040800	6.60
IC 74LS138	2041000	1.68
IC 74LS02	2041600	1.14
IC 74LS241	2042000	3.54
IC AM26LS31	2042400	7.92
IC AM26LS32	2042600	7.92

IC 74LS240	2044000	3.54
IC 74LS244	2044200	5.52
IC 74S174	2044600	3.96
IC 74LS14	2045800	1.44
IC 74LS164	2048200	3.00
IC 14040B	2245000	1.95
IC 6116	2049200	40.00
IC 6502A	2049600	28.94
IC 6545	2049800	66.24
IC 6551 1MHz	2155700	28.80
IC 6522A	2050200	27.21
IC Z80A SIO/2	2050600	58.00
IC Z80A CTC	2050800	16.80
IC Z80A CPU	2051000	21.18
IC Z80A DMA	2051200	56.76
IC 68B045 2 MHz	2052600	31.50
IC SY6551A-1 2MHz	2053000	24.00
IC SY6545A-1 2MHz	2052800	50.10
IC 910/910 PLUS GATE ARRAY	2057400	42.60
IC 925 GATE ARRAY	2057400	42.60
IC 950 GATE ARRAY A (A34)	2057600	23.88
IC 950 GATE ARRAY B (A37)	2057800	23.88
IC 74LS112	2138500	1.86
IC 74S251	2138600	2.28
IC 2K BY 8 RAM	2138700	28.20
IC 4116 16K DRAM	2139200	7.20
IC 9007 CRTC	2139900	54.00
IC 9006-135 BUFFER	2140000	33.00

RESISTORS & POTENTIOMETERS

RES CF 68 OHM 1/4W 5%	2051100	.72
RES CF 270 OHM 1/4W 5%	2051300	.72
RES CF 330 OHM 1/4W 5%	2051500	.72
RES CF 470 OHM 1/4W 5%	2051700	.72
RES CF 510 OHM 1/4W 5%	2051900	.72
RES CF 1K OHM 1/4W 5%	2052100	.72
RES CF 1.8K OHM 1/4W 5%	2052300	.72
RES CF 3.3K OHM 1/4W 5%	2052700	.72
RES CF 4.7K OHM 1/4W 5%	2053100	.72
RES CF 5.6K OHM 1/4W 5%	3013600	.72
RES CF 12K OHM 1/4W 5%	3013700	.72
RES CF 180 OHM 1/4W 5%	2053300	.72
RES CF 1M OHM 1/4W 5%	2031500	.72
RES CF 750 OHM 1/4W 5%	2031700	.72
RES CF 1.2K OHM 1/4W 5%	2031900	.72
RES CF 100K OHM 1/4W 5%	2032100	.72
RES CF 51K OHM 1/4W 5%	2032300	.72
RES CF 22 OHM 1/4W 5%	2033500	.72
RES CF 47K OHM 1/4W 5%	2033700	.72
RES CF 150 OHM 1/4W 5%	2033900	.72
RES CF 10K OHM 1/4W 5%	2034100	.72
RES CF 200 OHM 1/4W 5%	2034300	.72
RES CF 33 OHM 1/4W 5%	2034500	.72
RES CF 100 OHM 1/4W 1%	2034900	.72
RES CF 51 OHM 1/4W 5%	2036100	.72
RES CF 22K OHM 1/4W 5%	2036300	.72
RES CF 27K OHM 1/4W 5%	2037300	.72
RES CF 47 OHM 1/4W 5%	2037700	.72
RES CF 2.7K OHM 1/4W 5%	2038300	.72

RES CF 90 OHM 1/4W 5%	2177600	.72
RES CF 91 OHM 1/4W 5%	2038500	.72
RES CF 2.2K OHM 1/4W 5%	2038700	.72
RES CF 3.9K OHM 1/4W 5%	2177400	.72
RES CF 6.8K OHM 1.4W 5%	2039100	.72
RES CF 30K OHM 1/4W 5%	2039300	.72
RES CF 56K OHM 1/4W 5%	2039500	.72
RES CF 82 OHM 1/4W 5%	2144000	.72
RES CF 220 OHM 1/4W 5%	2040300	.72
RES CF 680 OHM 1/4W 5%	2037100	.72
RES CF 2K OHM 1/4W 5%	2036900	.72
RES PACK 1K OHM SIP 10%	2040500	1.58
RES PACK 6.2K OHM SIP 10%	2040700	1.73
RES PACK 10K OHM SIP 5%	2041100	2.04
RES PACK 4.7K OHM SIP 10%	2041300	1.20
RES PACK 1K OHM SIP 5%	2042700	3.00
RES PACK 2.2K OHM SIP	2230000	2.64
RES PACK 33 OHM DIP	2041700	2.64
RES CF 56K OHM 1/2W 5%	3016500	.72
RES CF 510 OHM 1/2W 5%	2045100	.72
RES CF 220 OHM 1/2W 5%	2186000	.72
RES CF 390 OHM 1/2W 5%	2176600	.72
RES CF 820 OHM 1/2W 5%	2186200	.72
RES CF 1.5K OHM 1/2W 5%	2186300	.72
RES CF 10K OHM 1/2W 5%	2186400	.72
RES CF 2.2M OHM 1/2W 5%	2186500	.72
RES WW 0.4 OHM 2W 10%	3019500	.72
RES WW 0.6 OHM 2W	2177100	.72
RES WW 0.4 OHM 2W 5%	3019700	.72
POT BRIGHTNESS & VERTICAL HEIGHT	2177700	1.06
POT VERTICAL LINEARITY	2177800	1.06
POT VIDEO B+	2177900	1.06
POT FOCUS	2180100	3.86
POT CONTRAST	2180200	2.77

TRANSFORMERS/COILS

TRANSFORMER FLYBACK KFS-00093	2201300	55.48
TRANSFORMER FLYBACK 970	2269000	58.32
TRANSFORMER HORIZ DR HDT19	2201200	4.08
TRANSFORMER POWER W/CON CRT858	2201100	129.24
TRANSFORMER POWER 970	2225600	127.68
TRANSFORMER BALUN	2186600	7.86
COIL 1.4uH 5%	2268900	2.00
COIL 200uF 5%	2268800	16.08
COIL INDUCTOR 27uH .3PIE	2201000	1.20
COIL LINEARITY ADJUSTABLE	2213600	7.20
COIL LINEARITY NON ADJUSTABLE	2200900	5.24
COIL DEFLECTION YOKE W/CONN	2200800	31.63

MISCELLANEOUS

CRYSTAL 16MHZ OSC	2042800	27.00
CRYSTAL 23.814 MHZ (912/920)	2098600	11.11
CRYSTAL 5.7143 MHZ	2098601	7.85
CRYSTAL 1.8432 MHZ	2098602	8.16
CRYSTAL 8.0000 MHZ	2098603	4.80
CRYSTAL 13.6080 MHZ	2098605	8.70
CRYSTAL 23.814 K1114A (950)	2035200	37.08

CRYSTAL 21.2544 MHz OSC	2138900	20.40
CRYSTAL 13.4784 MHz	2141400	3.24
FUSE 4A 125V	3025300	.72
FUSE 3A 125V	2193100	.72
FUSE 1A 250V	2097000	.72
POWER ADAPTER PATTERN GEN	2176300	41.40
SPEAKER W/CONNECTOR	2152800	7,73
THERMISTER SDT-100	2180300	1.44
TRANSDUCER AUDIO KYBD 970	2215100	5.52
BATTERY 970	2050001	4.20
UPGRADE YOKE 970	3209400	50.00
ANGLE ADJUST(SCREEN TILT MECHANIZEM) 925/950	2108600	2.00

MECHANICAL COMPONENTS CASES

TOP CASE 910/912	2151600	97.80
TOP CASE 920	2153800	97.80
TOP CASE 925/950	2141800	97.80
TOP CASE KEYBOARD 925/950	2204200	25.00
BOTTOM CASE 910/912/920	2151700	70.20
BOTTOM CASE 925/950	2141700	70.20
BOTTOM CASE KEYBOARD 925/950	2199100	35.00
BEZEL TOP CASE 925/950	2141900	20.00
BEZEL KEYBOARD 925/950	2198000	10.00
HOUSING ARM ASSEMBLY 970	2183400	60.72
HOUSING CRT 970	2188600	66.00
HOUSING MAIN ELECTRONIC 970	2188500	71.16
HOUSING KYBD TOP W/PALM REST 970	2188900	17.16
HOUSING KYBD BOTTOM W/PALM REST 970	2189000	35.16
COVER BACK HOUSING CRT 970	2188300	16.32
COVER SIDE HOUSING LOGIC BOARD 970	2188400	39.48
BEZEL CRT 970	2188800	15.48

KEYCAPS*

KEYCAP DG 1X1 BLANK	2065800	.72
KEYCAP DG 1X1 SCULP BLANK 0	2161601	.72
KEYCAP DG 1X1 SCULP BLANK -7	2161900	.72
KEYCAP DG 1X1 SCULP BLANK +7	2161800	.72
KEYCAP DG 1X1 SCULP BLANK +14	2161700	.72
KEYCAP DG 1X1-1/2 BLANK	2072400	1.52
KEYCAP DG 1X1-1/2 SCULP BLANK +7	2161801	2.56
KEYCAP DG 1X2 SCULP BLANK 0	2251400	3.00
KEYCAP DG 1X8	2077400	1.98
KEYCAP DG 1X8 SCULP	2089700	3.00
KEYCAP LG 1X1 BLANK	2073000	.72
KEYCAP LG 1X1 SCULP BLANK 0	2161600	.72
KEYCAP LG 1X1 SCULP BLANK -7	2161901	.90
KEYCAP LG 1X1 LOW PRO BLANK	2076500	.72
KEYCAP LG 1X1 LOW PRO SCULP BLANK	2162101	.90
KEYCAP LG 1X1-1/4 BLANK	2077200	1.52
KEYCAP LG 1X1-1/4 SCULP BLANK +7	2161802	2.44
KEYCAP LG 1X1-1/2 BLANK	2072700	1.52
KEYCAP LG 1X1-1/2 SCULP BLANK -7	2161902	2.56
KEYCAP LG 2X1 SCULP BLANK 0	2251300	3.00
KEYCAP LG "L" RETURN	2077100	1.86
KEYCAP LG "L" BLANK (RETURN)	2077101	3.90

KEYCAP LG "L" SCULP RETURN	2089400	2.76
KEYCAP LG "L" SCULP BLANK (RETURN)	2161602	3.90
KEYCAP BLACK 1X1 BLANK	2053700	.90
KEYCAP BLACK 1X1-1/2 BLANK	2063300	1.80
KEYCAP BLACK 1X8	2077500	2.70
KEYCAP TAN 1X1 BLANK	2063800	.72
KEYCAP TAN 1X1-1/2 BLANK	2063600	1.50
KEYCAP SET 910/910PLUS	3046800	52.44
KEYCAP SET 912B	3046900	52.44
KEYCAP SET 912C	3047000	52.44
KEYCAP SET 920B	3047100	63.24
KEYCAP SET 920C	3047200	56.58
KEYCAP SET 925/950	3047300	79.29
KEYCAP SET 925/950 SCULP	3047400	59.10

*PART NUMBERS FOR PRINTED KEYCAPS CAN BE OBTAINED IN YOUR MAINTENANCE MANUAL OR THROUGH SPARES ORDER ENTRY, TELEVIDEO.

SWITCHES

KEYSWITCH	2199400	3.60
KEYSWITCH - ALPHA LOCK	2199500	6.22
SWITCH TOP ADJ 7 POS DIP	2174200	3.84
SWITCH TOP ADJ 10 POS DIP	2181000	3.90
SWITCH SIDE ADJ 10 POS DIP	2096800	5.70
SWITCH PUSHBUTTON	2096900	17.88
SWITCH POWER ON/OFF SPST	2097300	7.89
SWITCH POWER SELECT DPDT	2097400	6.92

LABEL KITS

KIT LABEL 910	3208100	20.00
KIT LABEL 910+	3208200	20.00
KIT LABEL 912C	3208300	20.00
KIT LABEL 920C	3208400	20.00
KIT LABEL 925	3208500	20.00
KIT LABEL 950	3208600	20.00
KIT LABEL 970	3208700	20.00

SHIPPING CARTONS

CARTON SHIP W/FOAM 910/912/920	2237200	10.00
CARTON SHIP W/FOAM 925/950	2237300	10.00
CARTON SHIP W/FOAM 970	2249700	10.00

MECHANICAL MISCELLANEOUS

BATTERY HOLDER	2050101	4.62
CABLE ASY KEYBOARD 912/920	2005900	25.08
CABLE ASY KEYBOARD 910	2005901	25.08
CABLE ASY KEYBOARD 925/950	2005700	10.92
CABLE ASY KEYBOARD 970	2216100	31.20
CABLE ASY MODEM RJ11	2135900	17.34
CABLE ASSY CURRENT LOOP 925	2005802	10.98
CONNECTOR 2 PIN RT ANGLE	2098703	.72
CONNECTOR 2 PIN STR WAF	2098800	.72
CONNECTOR 5 PIN STR WAF	2098802	.72

CONNECTOR 10 PIN WIRE WRAP	2189300	3.30
CONNECTOR 40 PIN HDR STRAIGHT	2098107	7.50
CONNECTOR KEYBOARD PCB 26PIN	2098701	4.21
CONNECTOR KEYBOARD RJ11 925/950	2097900	2.22
CONNECTOR KEYBOARD RJ12 PCB 970	2141200	3.90
CONNECTOR KEYBOARD RJ12 KYBD 970	2141100	3.90
CONNECTOR RIGHT ANGLE RS232	2097800	10.62
CONNECTOR RIGHT ANGLE METAL RS232	2165300	29.04
CONNECTOR STRAIGHT RS232	2174300	20.00
CONNECTOR BLUE MOLEX MALE	2217301	3.60
CONNECTOR BLUE MOLEX FEMALE	2217300	3.60
CONNECTOR RED MOLEX MALE	2217201	3.60
CONNECTOR RED MOLEX FEMALE	2217200	3.60
CONNECTOR WHITE MOLEX MALE	2217401	3.60
CONNECTOR WHITE MOLEX FEMALE	2217400	3.60
CORD POWER 6' 3 PRONG CONN	2109000	19.87
CORD POWER 3PIN W/PLUG & CONN	2291100	20.00
E-RING MINIMUM 25	2223600	5.70
EQL ASY SPACE BAR DAMPER	2096300	.72
EQL ASY SPACE BAR GUIDE STEM	2096200	.90
EQL ASY SPACE BAR KEY GUIDE	2091200	1.80
EQL ASY SPACE BAR KEYGUIDE ARM	2096400	3.60
FOOT KEYBOARD 925/950	2190600	.72
FOOT KEYBOARD 970	2212700	.72
FUSE HOLDER CLIP	2180400	.72
FUSE HOLDER PANEL MOUNT	2097200	21.00
INSULATION PAD TRANSISTOR	2180800	.72
INSULATOR PAD CRYSTAL	2099700	1.02
KNOB CONTRAST	2153000	.72
KEYSTOPPERS 100ea	2223800	12.00
PIVOTSHAFT MINIMUM 25	2197800	4.68
PLUG JUMPER 910/910PLUS	2098300	1.80
RETAINER BALUN	2164500	.72
SHIELD PLATE LOGIC BOARD 970	3000500	60.00
SHROUD CONN 910/912/920	2100200	10.00
SHROUD CONN MODEM 910/912/920	2100201	20.00
SHROUD CONN 925/950	2100100	10.00
SHROUD CONN MODEM 925/950	2100103	20.00
SPACER NYLON, PCB SNAP MTG	2164400	.90
SOCKET IC 14 PIN	2098403	.78
SOCKET IC 16 PIN	2098405	.72
SOCKET IC 18 PIN	2098400	.83
SOCKET IC 24 PIN	2098401	1.10
SOCKET IC 28 PIN	2098404	1.32
SOCKET IC 40 PIN	2098402	1.80
SOCKET IC 16 PIN LOW PROFILE	2174601	6.00
SPRING CRT GOUNDING	2210500	.72
THUMB WHEEL 970	2218800	1.44

PRICES SUBJECT TO CHANGE WITHOUT NOTICE

PART LIST: KEYCAPS
MODEL: 925 DETACHABLE KEYBOARD
950 DETACHABLE KEYBOARD

PART NUMBER

DATE 11/15/82

DESCRIPTION	STEPPED KEYCAPS PRINTED	STEPPED KEYCAPS BLANK	SCULPTURED/MATTED KEYCAPS PRINTED	SCULPTURED/MATTED KEYCAPS BLANK	COMMENTS/NOTES
1X1 LIGHT GREY BLANK	-------	2073000	-------	2161600	0 DEGREES (1)
1X1 LG NO SCROLL/SETUP	2075500	2073000	2088700	2161600	0 "
1X1 LIGHT GREY F1	2073100	2073000	2085000	2161600	0 "
1X1 LIGHT GREY F2	2073200	2073000	2085100	2161600	0 "
1X1 LIGHT GREY F3	2073300	2073000	2085200	2161600	0 "
1X1 LIGHT GREY F4	2073400	2073000	2085300	2161600	0 "
1X1 LIGHT GREY F5	2073500	2073000	2085400	2161600	0 "
1X1 LIGHT GREY F6	2073600	2073000	2085500	2161600	0 "
1X1 LIGHT GREY F7	2073700	2073000	2085600	2161600	0 "
1X1 LIGHT GREY F8	2073800	2073000	2085700	2161600	0 "
1X1 LIGHT GREY F9	2073900	2073000	2085800	2161600	0 "
1X1 LIGHT GREY F10	2074000	2073000	2085900	2161600	0 "
1X1 LIGHT GREY F11	2074100	2073000	2086000	2161600	0 "
1X1 LG CHAR INSERT	2074200	2073000	2086100	2161600	0 "
1X1 LG CHAR DELETE	2074300	2073000	2086200	2161600	0 "
1X1 LG LINE INSERT	2074400	2073000	2086300	2161600	0 "
1X1 LG LINE DELETE	2074500	2073000	2086400	2161600	0 "
1X1 DARK GREY BLANK	-------	2065800	-------	2161700	+14 DEGREES
1X1 DG ESC/LOC ESC	2072300	2065800	2084200	2161700	+14 "
1X1 DARK GREY 1/!	2065900	2065800	2077800	2161700	+14 " (2)
1X1 DARK GREY 2/@	2066000	2065800	2077900	2161700	+14 "
1X1 DARK GREY 3/#	2066100	2065800	2078000	2161700	+14 "
1X1 DARK GREY 4/$	2066200	2065800	2078100	2161700	+14 "
1X1 DARK GREY 5/%	2066300	2065800	2078200	2161700	+14 "
1X1 DARK GREY 6/^	2066400	2065800	2078300	2161700	+14 "
1X1 DARK GREY 7/&	2066500	2065800	2078400	2161700	+14 "
1X1 DARK GREY 8/*	2066600	2065800	2078500	2161700	+14 "
1X1 DARK GREY 9/(	2066700	2065800	2078600	2161700	+14 "
1X1 DARK GREY 0/)	2066800	2065800	2078700	2161700	+14 "
1X1 DARK GREY -/_	2066900	2065800	2078800	2161700	+14 "
1X1 DARK GREY =/+	2067000	2065800	2078900	2161700	+14 "
1X1 DARK GREY `/~	2067100	2065800	2079000	2161700	+14 "
1X1 DARK GREY \/|	2067200	2065800	2079100	2161700	+14 "
1X1 DG BACK SPACE	2067300	2065800	2079200	2161700	+14 "
1X1-1/2 DARK GREY TAB	2072600	2072400	2084500	2161801	+7 "
1X1 DARK GREY Q	2068700	2065800	2080600	2161800	+7 "
1X1 DARK GREY W	2068800	2065800	2080700	2161800	+7 "
1X1 DARK GREY E	2068900	2065800	2080800	2161800	+7 "
1X1 DARK GREY R	2069000	2065800	2080900	2161800	+7 "

PART LIST: KEYCAPS
MODEL: 925 DETACHABLE KEYBOARD
950 DETACHABLE KEYBOARD

PART NUMBER

DATE 11/15/82

DESCRIPTION	STEPPED KEYCAPS PRINTED	STEPPED KEYCAPS BLANK	SCULPTURED/MATTED KEYCAPS PRINTED	SCULPTURED/MATTED KEYCAPS BLANK	COMMENTS/NOTES
1X1 DARK GREY T	2069100	2065800	2081000	2161800	+7 DEGREES
1X1 DARK GREY Y	2069200	2065800	2081100	2161800	+7 "
1X1 DARK GREY U	2069300	2065800	2081200	2161800	+7 "
1X1 DARK GREY I	2069400	2065800	2081300	2161800	+7 "
1X1 DARK GREY O	2069500	2065800	2081400	2161800	+7 "
1X1 DARK GREY P	2069600	2065800	2081500	2161800	+7 "
1X1 DARK GREY [/]	2069700	2065800	2081600	2161800	+7 "
1X1-1/2 DG LINE FEED	2072500	2072400	2084400	2161801	+7 "
1X1-1/4 LG CLEAR SPACE	2077300	2077200	2089600	2161802	+7 "
1X1 LIGHT GREY CTRL	2075000	2073000	2086900	2161600	0 DEGREES
1X1 DARK GREY ALPHA LOCK	2069900	2065800	2081800	2161601	0 "
1X1 DARK GREY A	2070000	2065800	2081900	2161601	0 "
1X1 DARK GREY S	2070100	2065800	2082000	2161601	0 "
1X1 DARK GREY D	2070200	2065800	2082100	2161601	0 "
1X1 DARK GREY F	2070300	2065800	2082200	2161601	0 "
1X1 DARK GREY G	2070400	2065800	2082300	2161601	0 "
1X1 DARK GREY H	2070500	2065800	2082400	2161601	0 "
1X1 DARK GREY J	2070600	2065800	2082500	2161601	0 "
1X1 DARK GREY K	2070700	2065800	2082600	2161601	0 "
1X1 DARK GREY L	2070800	2065800	2082700	2161601	0 "
1X1 DARK GREY ;/:	2070900	2065800	2082800	2161601	0 "
1X1 DARK GREY '/"	2071000	2065800	2082900	2161601	0 "
LIGHT GREY "L" RETURN	2077100	2077101	2089400	2161602	0 "
1X1 LIGHT GREY BREAK	2075100	2073000	2087000	2161600	0 "
1X1 DARK GREY BACK TAB	2069800	2065800	2081700	2161900	-7 "
1X1-1/2 LG SHIFT	2072800	2072700	2084700	2161902	-7 "
1X1 DARK GREY Z	2071100	2065800	2083000	2161900	-7 "
1X1 DARK GREY X	2071200	2065800	2083100	2161900	-7 "
1X1 DARK GREY C	2071300	2065800	2083200	2161900	-7 "
1X1 DARK GREY V	2071400	2065800	2083300	2161900	-7 "
1X1 DARK GREY B	2071500	2065800	2083400	2161900	-7 "
1X1 DARK GREY N	2071600	2065800	2083500	2161900	-7 "
1X1 DARK GREY M	2071700	2065800	2083600	2161900	-7 "
1X1 DARK GREY ,/<	2071800	2065800	2083700	2161900	-7 "
1X1 DARK GREY ./>	2071900	2065800	2083800	2161900	-7 "
1X1 DARK GREY //?	2072000	2065800	2083900	2161900	-7 "

PART LIST: KEYCAPS
MODEL: 925 DETACHABLE KEYBOARD
950 DETACHABLE KEYBOARD

PART NUMBER

DATE 11/15/82

DESCRIPTION	STEPPED KEYCAPS PRINTED	STEPPED KEYCAPS BLANK	SCULPTURED/MATTED KEYCAPS PRINTED	SCULPTURED/MATTED KEYCAPS BLANK	COMMENTS/NOTES
1X1 DARK GREY {/}	2072100	2065800	2084000	2161900	-7 DEGREES
1X1 LIGHT GREY DEL	2075200	2073000	2087100	2161901	-7 "
1X1 LG PRINT (LP)	2077000	2076500	2089300	2162101	0 " (3)
1X1 LG FUNCT (LP)	2076700	2076500	2089000	2162101	0 " (3)
1X8 DARK GREY SPACE BAR	2077400	-------	2089700	-------	0 "
1X1 LG HOME (LP)	2076800	2076500	2089100	2162101	0 " (3)
1X1 LG CURSER (LP)	2076900	2076500	2140500	2162101	0 " (3)(4)
1X1 LG LINE ERASE	2074600	2073000	2086500	2161600	0 "
1X1 LG PAGE ERASE	2074700	2073000	2086600	2161600	0 "
1X1 LIGHT GREY SEND	2075300	2073000	2088500	2161600	0 "
1X1 DARK GREY 7	2068000	2065800	2079900	2161601	0 "
1X1 DARK GREY 8	2068100	2065800	2080000	2161601	0 "
1X1 DARK GREY 9	2068200	2065800	2080100	2161601	0 "
1X1 DARK GREY 4	2067700	2065800	2079600	2161601	0 "
1X1 DARK GREY 5	2067800	2065800	2079700	2161601	0 "
1X1 DARK GREY 6	2067900	2065800	2079800	2161601	0 "
1X1 DARK GREY 1	2067400	2065800	2079300	2161601	0 "
1X1 DARK GREY 2	2067500	2065800	2079400	2161601	0 "
1X1 DARK GREY 3	2067600	2065800	2079500	2161601	0 "
1X1 DARK GREY ,	2068500	2065800	2080400	2161601	0 "
1X1 DARK GREY 0	2068300	2065800	2080200	2161601	0 "
1X1 DARK GREY .	2068600	2065800	2080500	2161601	0 "
1X1-1/2 LG ENTER	2072900	2072700	2084800	2162103	0 "
1X1 DARK GREY -	2068400	2065800	2080300	2161601	0 "

NOTES:

1) DEGREES REFER TO SCULPTURED/MATTED KEYCAPS ONLY
2) SLASH BETWEEN TWO CHARACTERS (ie: 1/!) IS FOR CLARITY AND IS NOT PRINTED ON KEYCAP
3) LOW PROFILE KEYCAPS
4) SAME KEYCAP CAN BE USED FOR ALL FOUR CURSER POSITIONS

SPARE PART KITS

The following are the terminal spare part kits available through TeleVideo Systems, Inc. Each model terminal has been designated the following spare part kits:

A) Main Logic
B) Power supply/Video module
C) Mechanical components
D) Additional parts

The suggested stocking levels have been identified as follows:

For the first 50 terminals lea of kits A, B, C, & D are suggested.
For the next 50 terminals add lea of kits A, & B
For the next 50 terminals add lea of kits A, B, C, & D
For the next 50 terminals add lea of kits A, & B

The list price of the spare part kits (as shown on the Terminal Spare Parts Price List) reflect a 25% discount, if the items were purchased seperately.

*Attached are the kits currently available through TeleVideo.

SPARE PARTS KIT
MODEL: 950 TTL
LOGIC BOARD
PART NUMBER: 2000400

DATE___02/10/83___

PART #	DESCRIPTION
2029200	IC 75188N/1488
2029400	IC 75189AN/1489
2035200	CRY K1114A 23.814 MHz (950)
2035800	IC 2114 RAM
2049600	IC 6502A CPU
2049800	IC 6545 CRTC
2155700	IC 6551 UART
2050200	IC 6522A VIA
8000043	IC EPROM SYS PROG 950 (A41)
8000044	IC EPROM SYS PROG 950 (A42)
2028700	CAP CERAMIC .01uf/16V 20% (2ea)

SPARE PARTS KIT DATE___02/10/83___
MODEL: 950 GATE ARRAY
LOGIC BOARD
PART NUMBER: 2233000

PART #	DESCRIPTION
2029200	IC 75188N/1488
2029400	IC 75189AN/1489
2035200	CRY K1114A 23.814MHz (950)
2049600	IC 6502A CPU
2049800	IC 6545 CRTC
2155700	IC 6551 UART
2050200	IC 6552A VIA
8000043	IC EPROM SYS PROG 950 (A25)
8000044	IC EPROM SYS PROG 950 A20)
2057600	IC GATE ARRAY 950 A (A34)
2057800	IC GATE ARRAY 950 B (A37)
2049200	IC 6116 RAM 150ns
2028700	CAP CERAMIC .01uf/16V 20% (2ea)

SPARE PART KITS DATE___02/10/83___
MODEL: ALL
ADDITIONAL PARTS
PART NUMBER: 2000300

PART #	DESCRIPTION
2024000	IC 74S00
2024200	74LS00
2024400	74LS03
2024600	74S04
2024800	74LS04
2025000	74LS05
2025200	74LS08
2025400	74LS10
2025600	74LS20
2025800	74LS32
2026000	74LS42
2026200	74LS51
2026600	74LS74
2138500	74LS112
2027400	74LS157
2027600	74LS163
2048200	74LS164
2027800	74LS166
2028000	74LS173
2028200	74LS174
2044200	74LS244
2138600	74LS251
2028400	74LS253
2028600	74LS367
2028800	74LS373
2029000	74LS374
2030200	NE555
2030400	DP 8304
2030600	AMD2111-4A
2044200	74LS244
2030900	CAP CERAMIC 1.0pf 1KV SPARK GAP
2047500	DIODE, IN914
2201700	DIODE DS 113A/MRI-1000
2201800	DIODE, IN920/KDS8513A
2202200	DIODE, IN4004/DS130TB
2180100	POT FOCUS 2M ohm
2177100	RESISTOR 0.6ohm WW 2W
2041300	RESISTOR PAC 4.7K ohm
2040700	RESISTOR PAC 6.2K ohm
2152800	SPEAKER 8ohm W/CONN
2097400	SWITCH, POWER SELECT, DPDT
2180300	THERMISTER, SDT-100
2201100	TRNF, POWER W/CONN (910/920/925/950)
2225600	TRNF, POWER W/CONN (970 ONLY)
2199700	TRANS 2N6121/25C1173
2202100	TRANS 2N6124/25A473

SPARE PARTS KIT
MODEL: 925/950
MECHANICAL
PART NUMBER: 2000500

DATE 02/10/83

PART #	DESCRIPTION
2005700	CABLE ASY KEYBOARD 925/950
2223700	FUSE 3A 125V (25EA)
2223300	FUSE 1A 250V (25EA)
2199400	KEYSWITCH (3EA)
2096800	SWITCH SIDE ADJ 10 POS DIP
2097300	SWITCH POWER ON/OFF SPST
2097800	CONNECTOR RIGHT ANGLE RS232
2097900	CONNECTOR KEYBOARD RJ11
2100100	SHROUD, CONNECTOR 925/950
2180200	POT, CONTRAST

SPARE PARTS KIT: DATE___02/10/83___
MODEL: 910/910PLUS
912/920 925/950
POWER SUPPLY & VIDEO MODULE
PART NUMBER: 2000100

PART #	DESCRIPTION
2197300	CAP MYLAR, .1UF/600V (C504)
2199300	CAP ELECTROLYTIC 220UF (C305)
2200800	DEFLECTION YOKE W/CONN KYS-00060 (L202)
2201000	COIL INDUCTOR 27UH .3PIE (L302)
2213600	COIL LINEARITY ADJUSTABLE (L201)
2200900	COIL LINEARITY 5.4UH NON ADJUSTABLE (L201)
2200600	DIODE IN5391/DS135D (2ea)
2201500	DIODE DSA17C/MR500 (4ea)
2201600	DIODE, ZENER IN759A/RD12EB (D112)
2126800	REGULATOR, LAS1605 2A/5V (IC2)
2126900	REGULATOR, LAS16CB 2A/13.8V (IC1)
2176600	RESISTOR, CF 390 ohm 1/2w 5% (R102)
2201200	TRANSFORMER HORIZ DR HDT19 (T301)
2201300	TNFR FLYBACK KFS-00093 (T302)
2045500	TRANSISTOR 2N4401/2SC1166 (Q301)
2047100	TRANSISTOR 2N5551/2SC983 (Q103/Q105)
2047300	TRANSISTOR 2SC2233/MJE13006 (Q302)
2046700	TRANSISTOR KTC1627A/MPSA06 (Q102)
2280000	CAP NON POLARIZED 16uf/25V (C306)
2177700	POT 100K BRIGHT/VERT HEIGHT (SFR1/SFR4)
2177800	POT 2K VERT LINEARITY (SFR2)
2177900	POT 5K B+ 75VOLT ADJUST (SFR3)

Repairs Price List for Video Display Terminals

October 1, 1983

REPAIR	Price
Terminal Repair Charge (plus individual charges below)	$ 35.00

INDIVIDUAL REPAIR CHARGES	Price
Logic Board (910/910 PLUS)	$ 50.00
Logic Board (912/920)	$ 65.00
Logic Board (914/924/925/950)	$100.00
Logic Board (970)	$120.00
Keyboard (910/912/920)	$ 30.00
Keyboard (914/924/925/950/970)	$ 50.00
Power Supply (all models)	$ 50.00
Video Board (all models)	$ 50.00
Current Loop Board (910/925)	$ 25.00
Integral Modem	$ 60.00

Service

Nationwide Field Service is available from General Electric Co. Instrumentation and Computer Service Centers. In Canada, service is available from Canadian General Electric Service Centers.

Out of Warranty

Customer to return defective module freight prepaid to the factory, 1170 Morse Avenue, Sunnyvale, CA 94086. TeleVideo will send repaired module, billing per above price schedule plus return freight.

Prices subject to change without notice.

TeleVideo Systems, Inc.

1170 Morse Avenue • Sunnyvale, CA 94086

California: Santa Ana (714) 557-6095; Sunnyvale (408) 745-7760 • Georgia: Atlanta (404) 399-6464
Texas: Dallas (214) 980-9978 • Illinois: Bloomingdale (312) 351-9350 • Massachusetts: Boston (617) 668-6891
New York/New Jersey: (201) 267-8805 • London 44-9905-6464 • Paris 33 (1) 687-3440

Terminal Maintenance Training Class

Subjects covered:	*Basic Operation* *Theory of Operation* *Overview of Schematics* *Debug to Component Level* *Interface Considerations* *Installable Options* *Lab* *Structured* *Operations*
Material provided:	*Maintenance Manuals* *Customer Service Notes* *Product Brochures* *Lunch Provided* *Certificate of Completion Awarded*
Price:	*$200.00 per person at TeleVideo Training Center* *$1750.00 (plus travel expenses outside USA) per class on-site, plus $100.00 per person over 10 students.*
Sign Up:	*Classes are scheduled on a demand basis. To enroll, contact Customer Service, TeleVideo, Sunnyvale, (408) 745-7760.*
Fees:	*All fees are due and payable 2 weeks prior to the first class session.*

TeleVideo Systems, Inc.

1170 Morse Avenue • Sunnyvale, CA 94086

California: Santa Ana (714) 557-6095; Sunnyvale (408) 745-7760 • Georgia: Atlanta (404) 399-6464
Texas: Dallas (214) 980-9978 • Illinois: Bloomingdale (312) 351-9350 • Massachusetts: Boston (617) 668-6891
New York/New Jersey: (201) 267-8805 • London 44-9905-6464 • Paris 33 (1) 687-3440

950 THEORY OF OPERATION

TTL

SECTION

MAIN LOGIC BOARD

4.1

Overview

Please refer to figures 1, 2, 3, and 4 of the block diagrams as you read the text that follows.

Figure 1 shows the power-on reset, which is controlled by A17. During power-up, this chip sends the signals necessary to reset the CPU and to perform the initial diagnostic routine. This routine reads the switches in the back of the terminal and configures it for the proper handshaking protocol.

The 950's CPU is a 6502, located at A53.

The Shift clock (OSC1) generates the timing for the 950's logic system. The Stretch clock functions as the main clock for the CPU. Other clock circuits include the Crystal clock to the UARTs, the Shift clock, the DC Carry clock, the C clock, and the QC clock.

The CPU's address bus (6502 bus) addresses the ROM chips (A41 and A42).

The ROMs contain the operating instructions, the power-up diagnostics, and the other intructions necessary to operate the terminal. Most systems only use two ROMs, but the 950 contains an additional, optional ROM (A52).

The decoding gates (A58 and A63) select one of the three ROMs. The other decoder (A62) selects either the DISP.MEM (display memory) or the IOP.SEL (input/output select) signal.

The auxiliary chip in this figure (6522) reads switches (S1 and S2), and generates the control signals for the video attributes and the bell, as well as several auxiliary control signals used to address the display RAM.

In figure 2 of the block diagram, note the continuation of the 6502 and the 6522.

The CRT controller chip (CRTC 6545) generates the signals necessary to control the monitor portion of the terminal. It outputs three primary signals: horizontal synch, vertical synch, and cursor. These signals go to the video module.

The display RAMs are addressed by the 14 address bits coming from the CPU bus, as well as the memory address bits from the CRTC.

The multiplexers in the center of the figure (A43 through A46) alternately select whether the CPU or the CRTC is permitted to address the system and the display RAMs (A25 through A28, A34 through A37).

The Phase clock controls this process. During one phase of the clock the CPU can address RAM. During the other phase, this multiplexer allows the CRTC to address RAM.

When the CPU addresses the system display RAMs, the bidirectional latch at A14 is enabled to either input or output data from the system RAMs. When the CRT controller addresses the RAMs, the latch at A24 holds the display data.

Normally, the outputs of the CRTC would be used for scrolling. However, since the 950 has a smooth scroll option, the output of the counter latches at the bottom of figure 2 (A60 and A61) are used to scroll. The CPU controls these latches through the decoder at A62.

In figure 3 of the block diagrams, the row address signals coming from these counter latches (A60 and A61) and the display data from the latch above it (A24) are used to address the character-generator ROMs (A32 and A33). The character-generator ROMs then output 14 bits to a parallel-to-serial shift register.

The DC.Carry signal loads these 14 bits at the shift register (A22 and A23), and the shift clock shifts the data into the video logic and the drivers as a serial data stream.

The eight bits of display data from latch A24, as well as one bit from the character generator ROMs, address the attribute registers.

The attribute registers' output also addresses the video logic and drivers, as do the video attribute signals sent by 6522. These signals (dark on light, cursor, force blank, blink rate, and maximum intensity) control the video attributes through the video logic and drivers. Note that, in the 950, the maximum intensity signal (MI) is standard. To highlight, the 950 uses half intensity. The output is routed to the video module.

The XTAL1 clock (clock source) controls the three UARTs on figure 4 of the block diagrams.

A49 receives data from the keyboard.
A50 receives and transmits data for the main port (P3).
A51 receives and transmits data for the printer port (P4).

4.2

CPU Timing and Control

A 23.814 MHz. oscillator (OSC 1, sheet 6) generates the timing for the 950's entire internal logic system. Known as the Shift (or dot) clock, it drives the two shift registers (A22 and A23). These registers bring in parallel data and shift it out as serial dot data.

The active low* shift clock is gated with the terminal count output of the C.clock (Character clock) counter. Together they drive a latch (A24, sheet 4) that holds data from character addresses 0 through 7, as well as the flip-flop (A31, sheet 4) that controls the DEL CURSOR signal.

A 4-bit binary counter (A3, sheet 6) divides the shift clock's rate by 14, creating eight 1.701 mHz clocks.

The C.clock, which is the time base for character generation, drives the CRT chip (6545, sheet 2). The active low C.clock has two purposes. It drives the Hex D flip-flops (A64 and A71) that time the CRTC RESET. It also controls the Stretch clock, which generates clock periods twice the normal length (1175ns vs. 588ns) upon command from the CPU.

This circuit (sheet 6) accesses slower memory or peripheral devices. The final output (called "00" or "Phase Zero clock") goes to the 6502 and all the peripheral chips. The Phase Zero clock controls the CPU bus timing, and it triggers all data transfers between the CPU and the other internal processors.

The DC.carry signals function as two clocks. The active high DC.Carry clock drives a flip-flop (A19, sheet 4) that is part of the video attribute circuitry. The active low DC.Carry clock is connected to the LD or Shift/Load enable lines (A22 and A23, pin 15, sheet 4) of two parallel-to-serial shift registers (A22 and A23). These registers are part of the characacter generation circuitry.

The XTAL1 clock drives UARTs A49, A50, and A51, which interface data to and from the terminal.

The QC clock combines with three RAM address lines (A15, sheet 3) to form a 1-of-10 decoder. The decoder's output goes to the chip select lines of each system RAM and each page of memory. The QC clock also deselects the RAM chips while the address lines are settling.

Line lock and smooth scroll are two 950 features not normally attainable with the 6545 CRT controller. To use them, additional circuity is required.

*The active low state is indicated by a bar above the signal name.

To achieve line lock, the top of the 6545's display register must be reloaded at the beginning of each character row. A general description of this circuitry follows.

To achieve smooth scroll, a CPU-loadable count-up counter (A60, sheet 4) must replace the 6545's internal scan line counter.

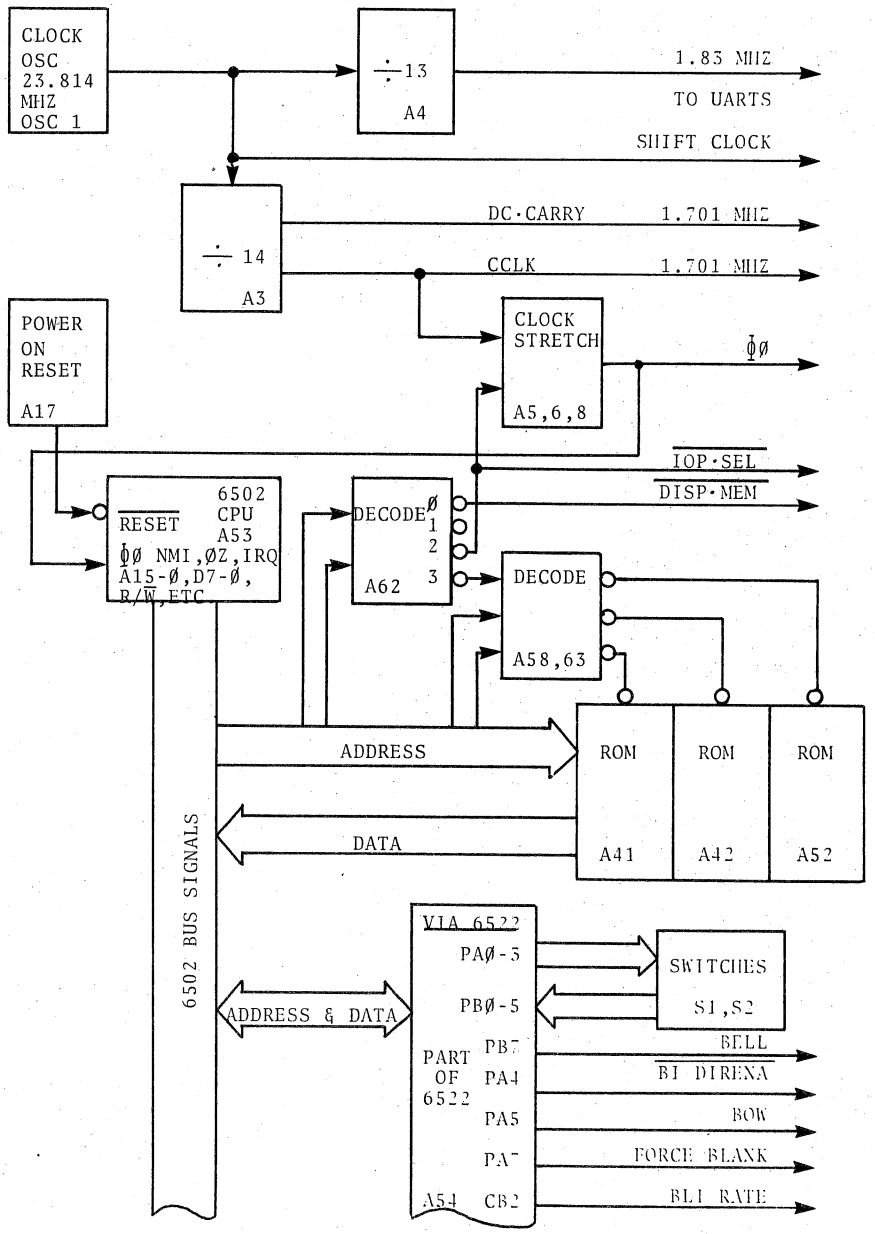


Figure 1 CPU, Timing, and Control

4.3

Display Controller

The 6545 (A55) generates each character's memory address in the display RAMS (A25 through A28) as it is to be displayed. It also generates the horizontal and vertical synchronization (synch) pulses necessary to control the deflection circuits of the monitor (CRT).

Note! In the text that follows, the term "scan line" refers to one of ten scan lines created by the electron beam, which makes up one data row.

The 6522's timer (T2) counts horizontal scan lines. When a specified number of scans have been executed, it interrupts the CPU (6502) with the NMI-interrupt. The CPU then loads the memory address of the next data row into the CRT controller (6545).

At the same time the NMI-interrupt is issued to the CPU, the CRTC reset timer (A64 and A71, sheet 7) is cleared, causing it to reset. The reset is released after seven C.CLK periods, and the CRTC starts timing the next character row. This operation allows the CPU to determine the order of the display lines so that some lines can be locked while others scroll.

To achieve a smooth scrolling effect, the number of scan lines in the character row and the starting scan line of each row must be specified.

The 6522's timer, which counts horizontal synch pulses, specifies the number of scan lines in the present character row. Normally, ten lines are used when smooth scroll is disabled. During a smooth scroll, this number ranges between 1 and 10 on the top and bottom rows.

To do this, the processor loads a 4-bit value into a latch (A61, sheet 4). When the CRTC is reset, this value is transferred to the counter (A60, sheet 4) and becomes the first scan line of the next data line. Each horizontal synch pulse then increases this value until the start of the next data line. At that point, it is preset again to a value determined by the CPU.

The CPU and the display controller share access to the system and display RAM during the alternate phase of the 6502's Phase 2 clock.

During the positive portion of the Phase 2 clock, the CPU address can be gated onto the RAM address bus through multiplexers (A43 through A46, sheet 2). A bidirectional transceiver (A14, sheet 3) passes data between the CPU data bus and the RAM data bus.

During the negative portion of the Phase 2 clock, the 6545 address bus (A55) is gated onto the RAM address bus, allowing the video data to be loaded into a latch (A24, sheet 4). This address becomes the input for the character generators and the attribute generation circuitry.

This alternating ("interleaved") access allows the processor to operate at normal speed without interruption or degradation of the display quality (which could be caused by accidental appropriation of the display bus by the processor as it accesses data).

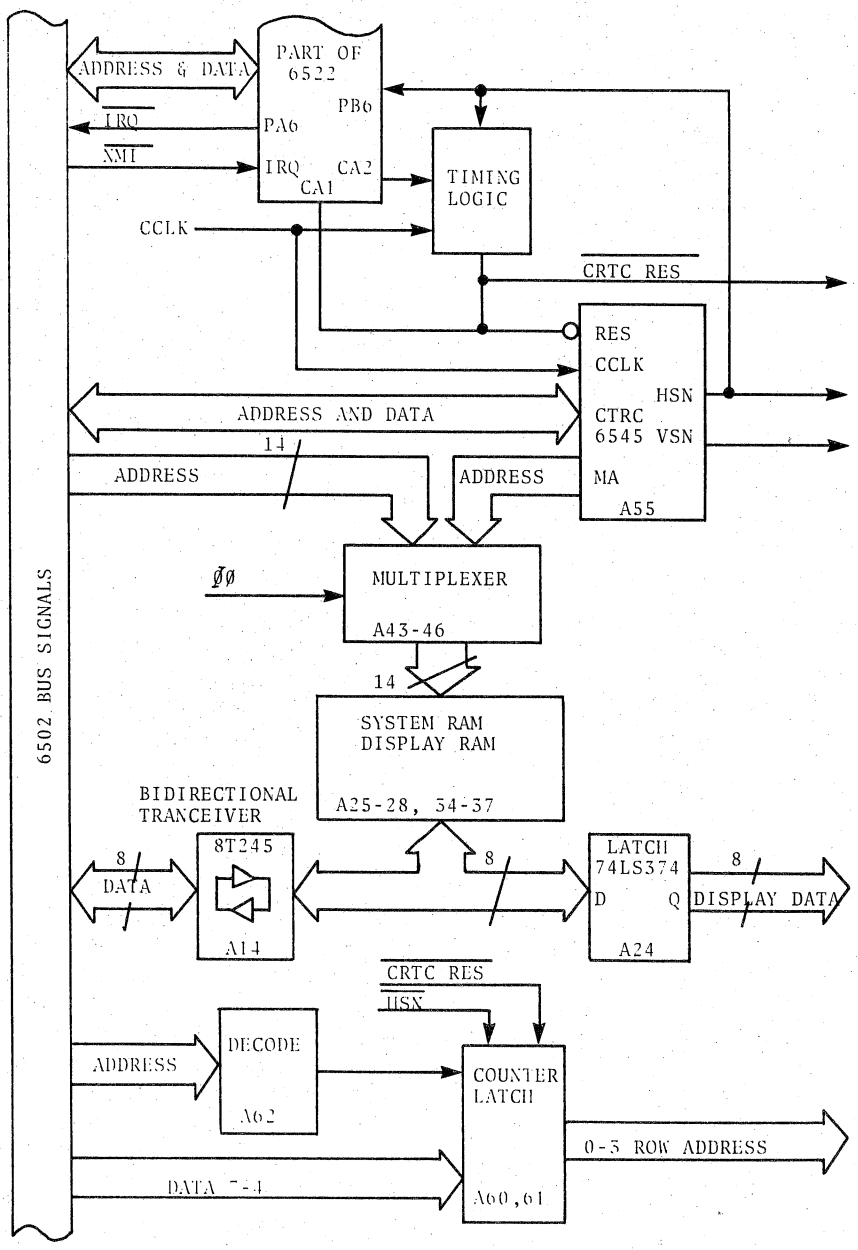


Figure 2 Display Controller

4.4

Video and Character Generation

To create the 950's display, the CRT scans horizontally from left to right, and vertically from top to bottom. Depending on the terminal's Hertz setting, the scan consists of 250 horizontal scan lines, each repeated 50 or 60 times per second. Each scan line displays 80 sections of 14-dot pixels. Each character line contains ten horizontal scan lines. This makes each character cell 14 pixels wide by 10 pixels high.

Characters are formed when the electron beam turns on individual pixels. The CRTC "MA" lines access the display memory once each character time (14 dot clocks). Once each cycle, the data from the display memory is then latched by the character address latch (A24, sheet 4). The output from this latch drives the eight most significant address lines of the character generator ROMs (A32 and A33, sheet 4).

The scan-line counter controls the four least significant address lines of the character generators. The scan-line counter's output changes only at the end of the scan line, when horizontal synch goes high.

The character generator's output is a 14-bit word that represents the pixel pattern to be displayed. The Shift clock loads this word into a 14-bit parallel-in/serial-out shift register (A22 and A23, sheet 4), and shifts it out, one bit at a time.

Thus, as the present pixel pattern of one character is loaded, the character address of the next character is latched. The bits shifted out of the shift register are mixed with display enable and the cursor and attribute data, creating the video output to the monitor. This signal turns the CRT's electron beam on and off as the beam sweeps the raster.

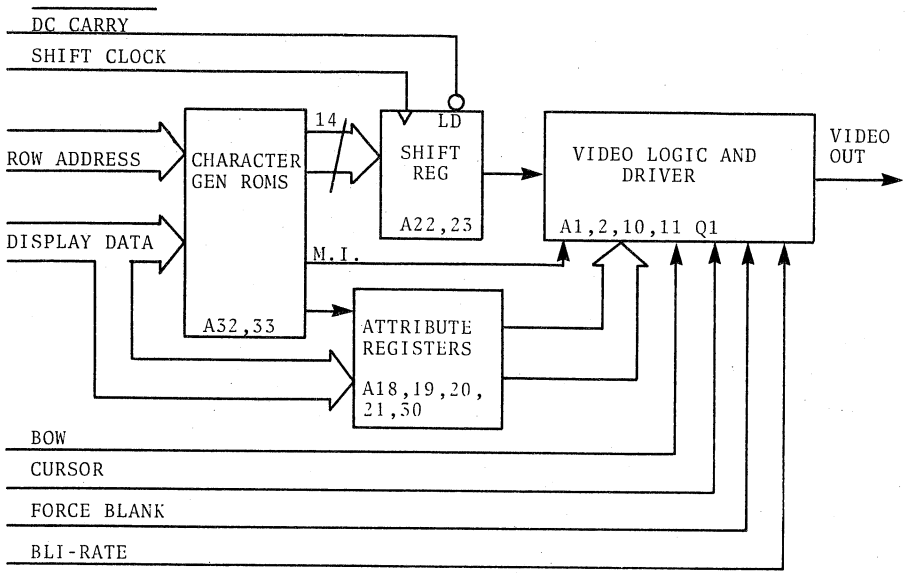


Figure 3 Video and Character Generation

4.5

Visual Attributes

The 950 has five visual attributes: half intensity, blink, blank, underline, and reverse video.

The only attribute created on a character-by-character basis is half intensity. All other attributes are "field" attributes; i.e. they have a specified starting and ending point. All characters between these points are affected by the attribute selected.

In the 950, attributes are stored in the display RAM just like displayed characters. An attribute character occupies a character space on the screen and is displayed as a half intensity space. The attribute becomes active immediately to the right of that space and remains in effect until the end of the screen.

Since an attribute is stored as a character in the display RAM, the character generation logic processes it as though it were a displayed character. However, the byte stored in RAM for an attribute character differs from that for a display character in that bits 4 and 7 are always set, while bits 5 and 6 are always reset.

Bits 0 through 3 define the active attribute. When the low-order character generator ROM (A33, sheet 4) is accessed by these codes (90 through 9F), the resulting data bit (A33, pin 17) is output as a high.

A21's data input comes from the output of a four-channel, two-to-one multiplexer (A20). While nonattribute characters are displayed, the multiplexer is driven by the output of A19. During an attribute character time, the output of Nand gate A11 is low, and it selects the A input to the multiplexer. This input connects with the output of the And gates that compare the previous attributes (output of A21) to the new attributes (output of A24).

If the previous attribute bit and the corresponding bit of the new attribute are both high, the output of the And gate is high. If one or both are low, the ouptut of the And gate is low and the attribute is turned off.

Thus, if an attribute is true for both the previous attribute and the new attribute, it is true while the new attribute is displayed on the screen. Otherwise, it turns off when the new attribute character starts.

The 950's attributes continue from character line to character line. Since any attribute on the previous line must be displayed on the current line until a new attribute is found, the logic must remember the last attribute of the previous line.

To summarize, A21's output is used by the video logic to turn visual attributes on or off. Its input can come from two sources: the output of the AND gates and the output of A19.

The output of the And gates defines the attribute(s) to be displayed during the attribute character, while A19's output determines the attribute(s) to be displayed during a nonattribute character.

A19's output is set to equal the previous character line's attribute until a new attribute is encountered. At that time, the output changes to the new attribute. A18 is used to remember the last attribute of a character in any character line.

Since each character line contains ten scan lines, the attribute data changes ten times. At the end of the displayed portion of each scan line, the Display Enable signal changes from high to low. This signal is then inverted and fed into a two-input Nand gate with the Delayed Display Enable signal, which changes one character time after Display Enable. Both signals are high only during the 81st character time of each scan line, creating a low pulse on the output of the Nand gate (A13 and A11). This pulse enables the output of a tri-state latch (A18).

A18's input comes from A20 and is latched only during the last scan line of the character row (pin 9, clock enable). This "remembers" the last attribute data of any character line. A18's output is latched into A19 at the end of the displayed portion of each scan line. A19's output then defines the attribute to be displayed during the current nonattribute character time.

The signals for Delayed Display Enable, Delayed Cursor, Dot Serial, Bow, Force Blank, and Visual Attribute Data are combined on sheet 6. They are gated together through A1, A9, A10, and A11, and are amplified to proper voltage and current levels by an NPN transistor Q1 (sheet 6). This transistor drives the video signal to the video module and/or external monitor (i.e. composite video).

4.6

Input/Output Circuits

Each of the three peripheral ports is controlled by a seperate 6551 UART.

UART A50 receives and transmits data for the main port (P3)
UART A51 receives and transmits data for the printer port (P4)
UART A49 receives data from the keyboard

The UARTs receive serial data, convert it to parallel data, and tie it directly to the CPU's data bus with input drivers, receivers, and switching circuits (A39, 40, 47, 48, 56, 57, 58, 50, sheet 5).

The use of seperate UARTs for the P3 and P4 ports allows the setting of different baud rates for each port.

The 1489 quadruple input line receivers (A57 and A40) convert RS232C voltage levels to TTL voltage levels. The 1488 quadruple output line drivers (A48 and A39) convert TTL voltage levels to RS232C voltage levels.

The output of A59, a quadruple 2-to-1 multiplexer, selects the output line drivers. A59 can select between two inputs (A or B), and route it to its respective outputs.

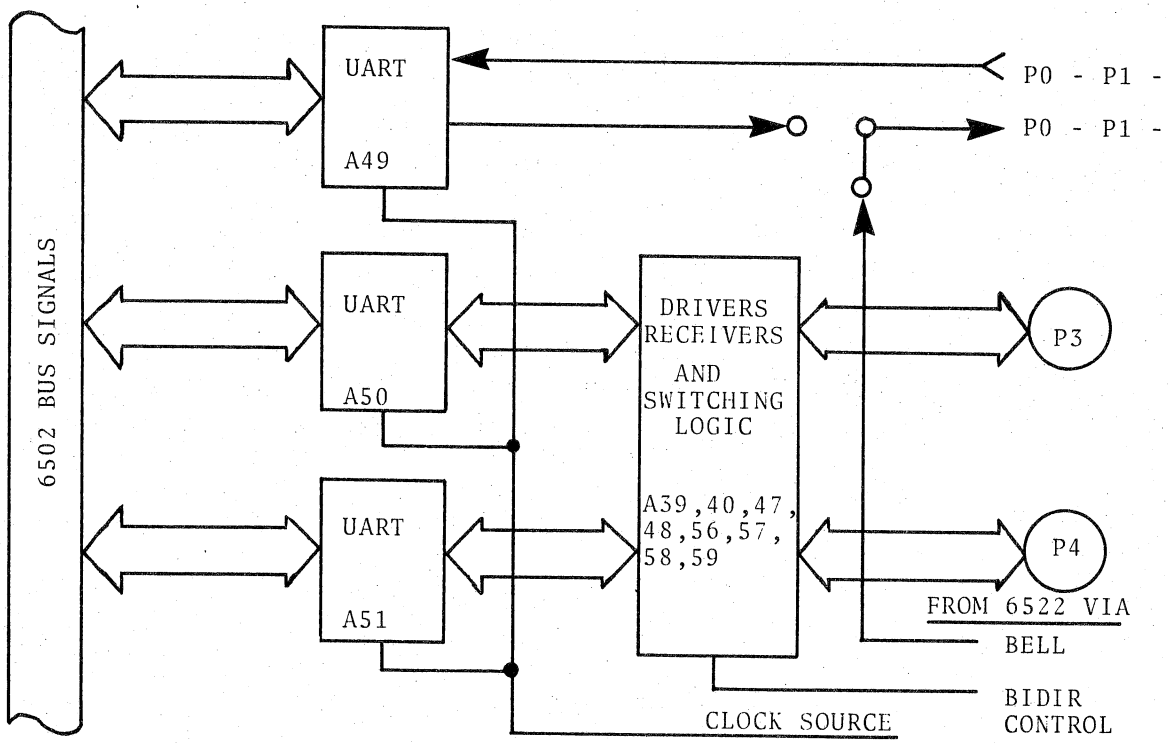


Figure 4 I/O Circuits

KEYBOARD

4.7

Overview

The 950 contains a microprocessor-based keyboard. The firmware monitors keyboard scanning, return-line testing, and communication with the control board.

In addition to the standard keyboard, additional parts let you create a keyboard that allows new key codes to be programmed into the keyboard PROM (2716).

Standard Keyboard (Version 1)

- Requires 5 volts (typical input current = 80 milliamps)
- 8048 microprocessor
- 1k byte ROM capacity (internal to the 8048)
- Asynchronous serial transmit and receive
- Baud rate = 1200 bits/sec.
- Word structure = 1 start bit, 8 data bits, 1 stop bit

Version 2 Keyboard with EPROM

- Requires 5 volts (typical input current = 150 milliamps) .
- 8035 microprocessor
- 2K x 8 byte EPROM 2716 (external to 8035)
- Status display - 8 LED display
- Asynchronous serial transmit and receive
- Baud rate = 1200 bits/sec.
- Word structure = 1 start bit, 8 data bits, 1 stop bit

The Version 2 keyboard with the 2716 EPROM requires a larger memory map and storage capability in the microprocessor. Therefore, you must also change the standard 1K x 8B 8048 microprocessor to a 2K x 8B 8035.

To install it, cut jumpers A through M on the circuit side of the logic board and install the following components in the appropriate locations.

Components

U2,U3	74LS367
U4	75L5373
U5	EPROM (2716)
U7	74LS05
C2,C3	{.01uf cap}
C4,C5	{10% 50V}
R2	1K 5% 1/4 watt

4.8

Keyboard Layout

The keyboard contains 101 keys on a PC board, as shown in Figures 5-A and 5-B.

The key switches are arranged in an X-Y matrix (Figure 6). Only four special keys (CTRL, SHIFT, FUNCT, and ALPHA LOCK) are not included in the X-Y matrix.

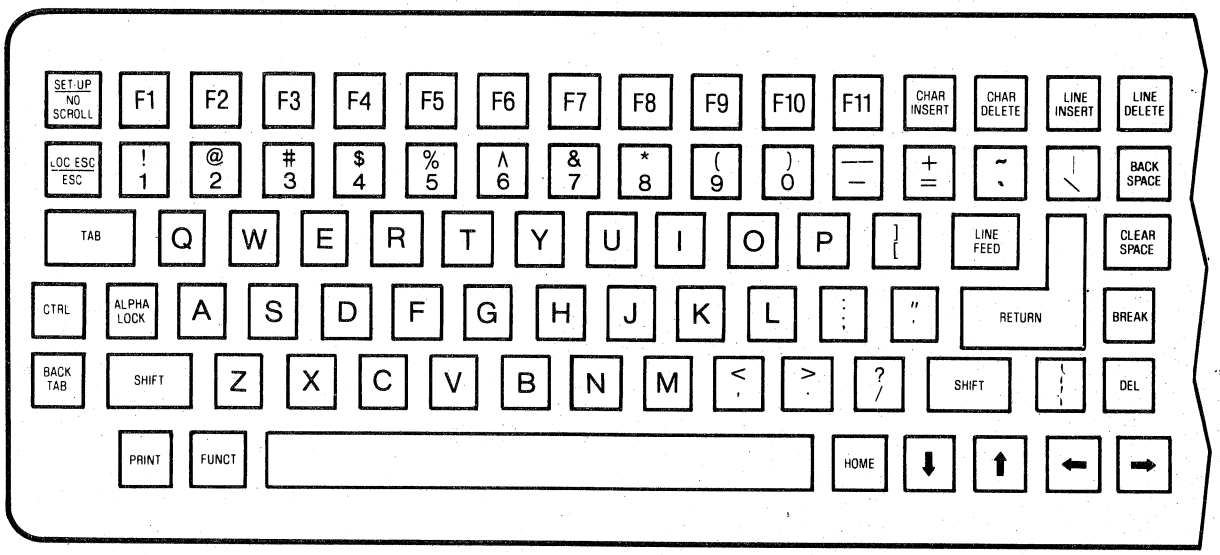


Figure 5-A Keyboard Layout

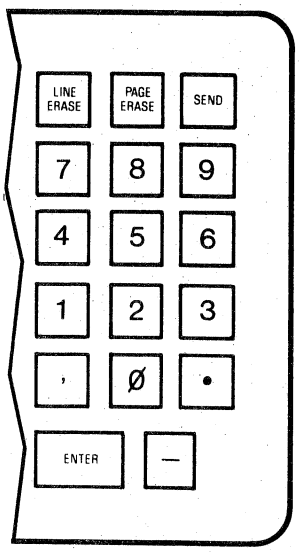


Figure 5-B
Keypad Layout

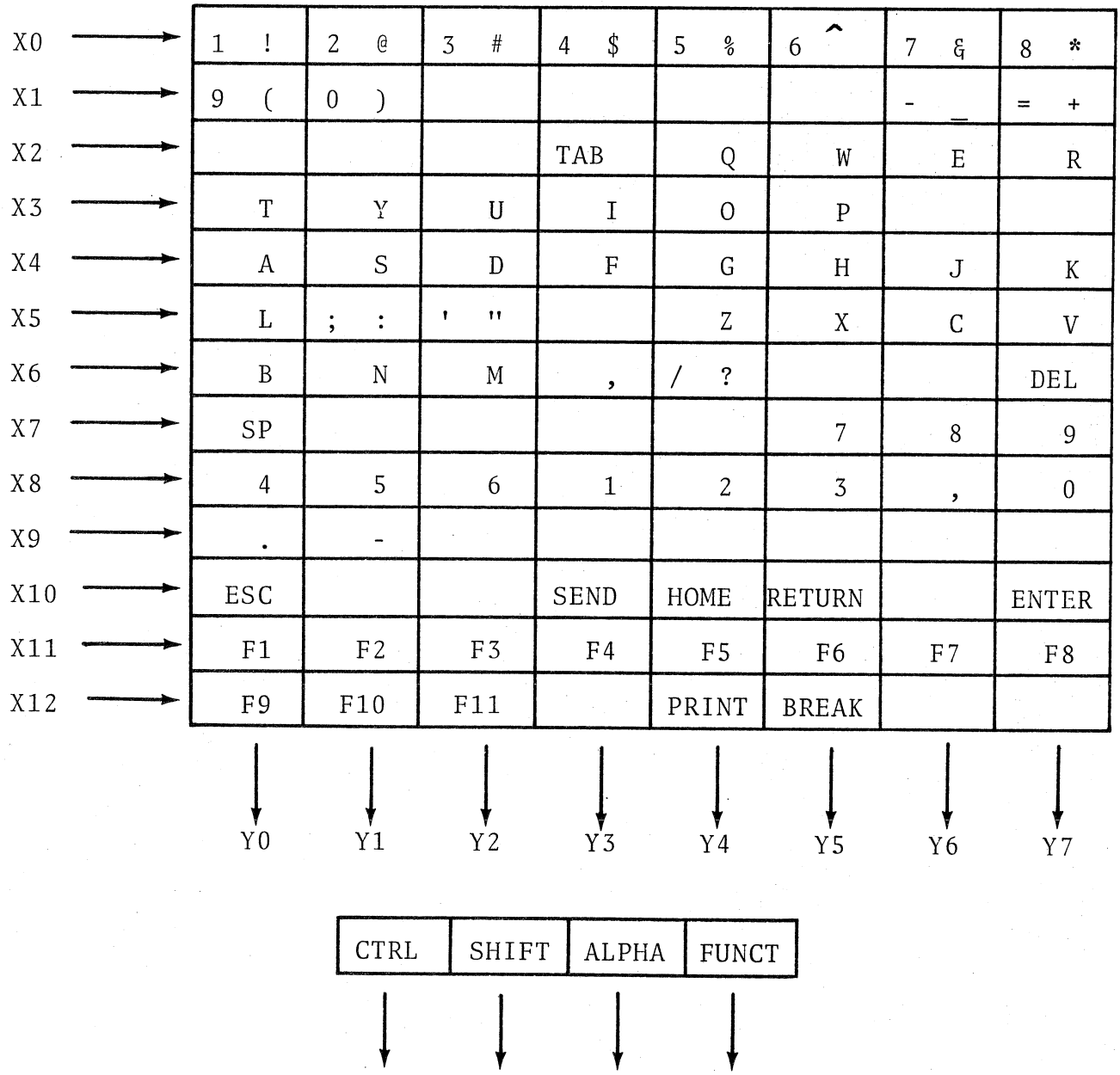


Figure 6 Keyboard X-Y Matrix Arrangement

4.9

Keyboard Interface

Communication between the main control board and the keyboard controller is asynchronous. The standard asynchronous format used by the 950 (Figure 9) consists of one start bit, eight data bits, and one stop bit. The baud rate is set to 1200 bits/sec.

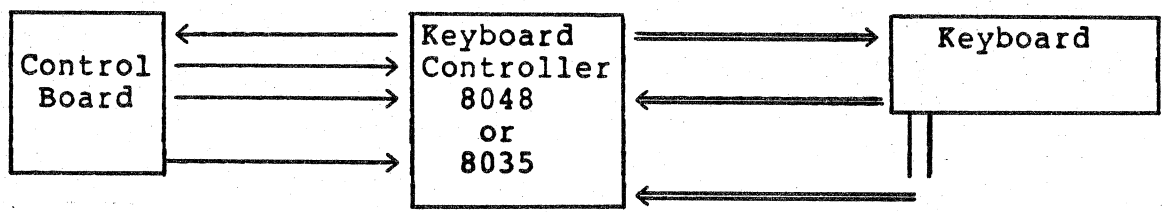


Figure 7 Keyboard Interface

4.10

Keyboard Scanning Method

The keyboard microprocessor (8048 or 8035) drives the scan lines (X lines), one at a time, to a low voltage. The return lines (Y lines) are tested by the microprocessor.

The keyboard matrix output ports (10 through 14, 20 through 27) latch the X0 through X12 lines to the keyboard. The connections are shown in Figure 7.

Whenever a low voltage is detected on a Y input line, it means that a key has been depressed. That key is at the intersection of the driven line (X) and the detected line (Y).

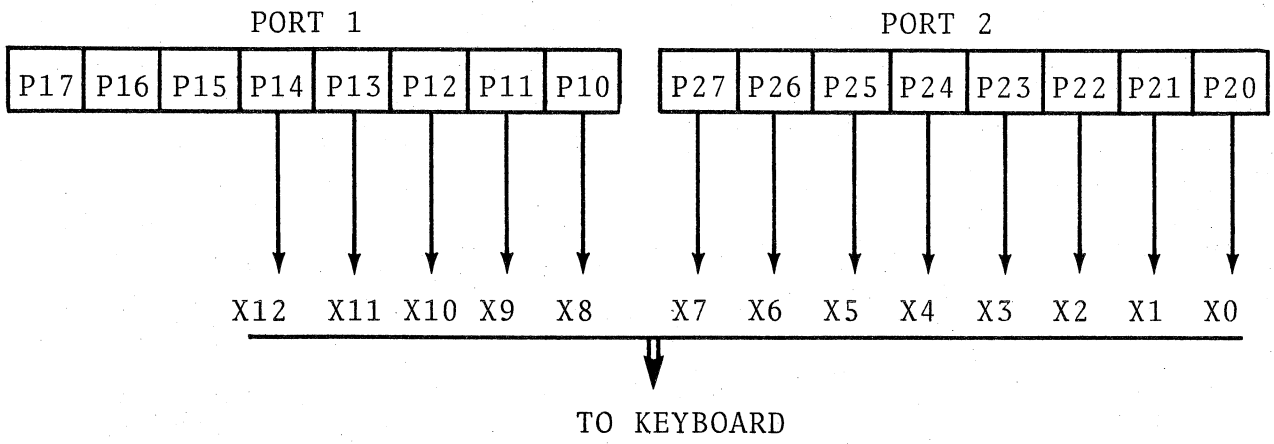


Figure 8 8048 Ports

The return matrix lines (Y lines) from the keyboard are read by the microprocessor's data bus (D0 through D7). The connections are shown in Figure 8.

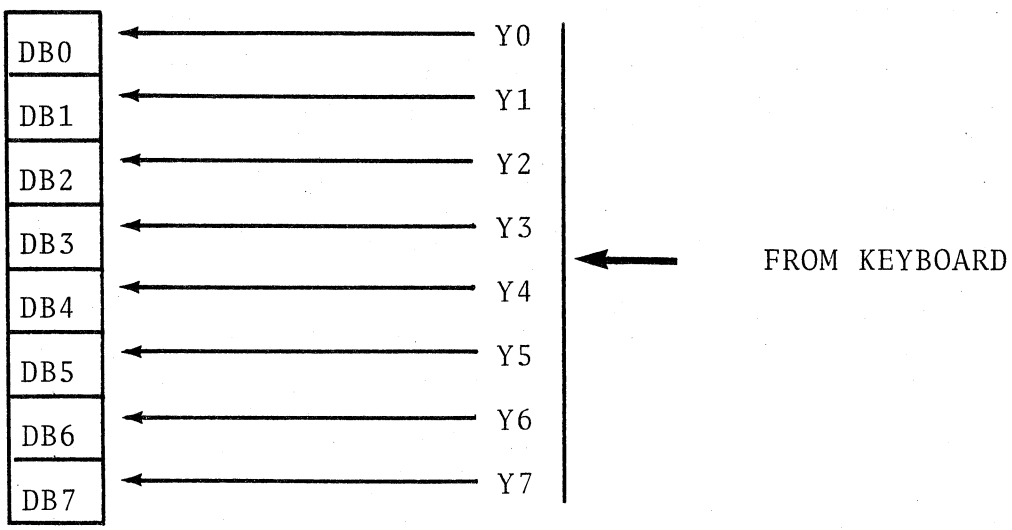


Figure 9 8048 Data Bus

Basic Scan Routine

Starting the scan routine resets the transmit flag and enables the external interrupt for receiving status from the control board.

The keyboard matrix is scanned from the top row to the bottom row. As soon as a key is pressed, the row is tested bit by bit, from left to right. The matrix key codes are immediately encoded and stored in two registers (NEWKY 1 and NEWKY 2).

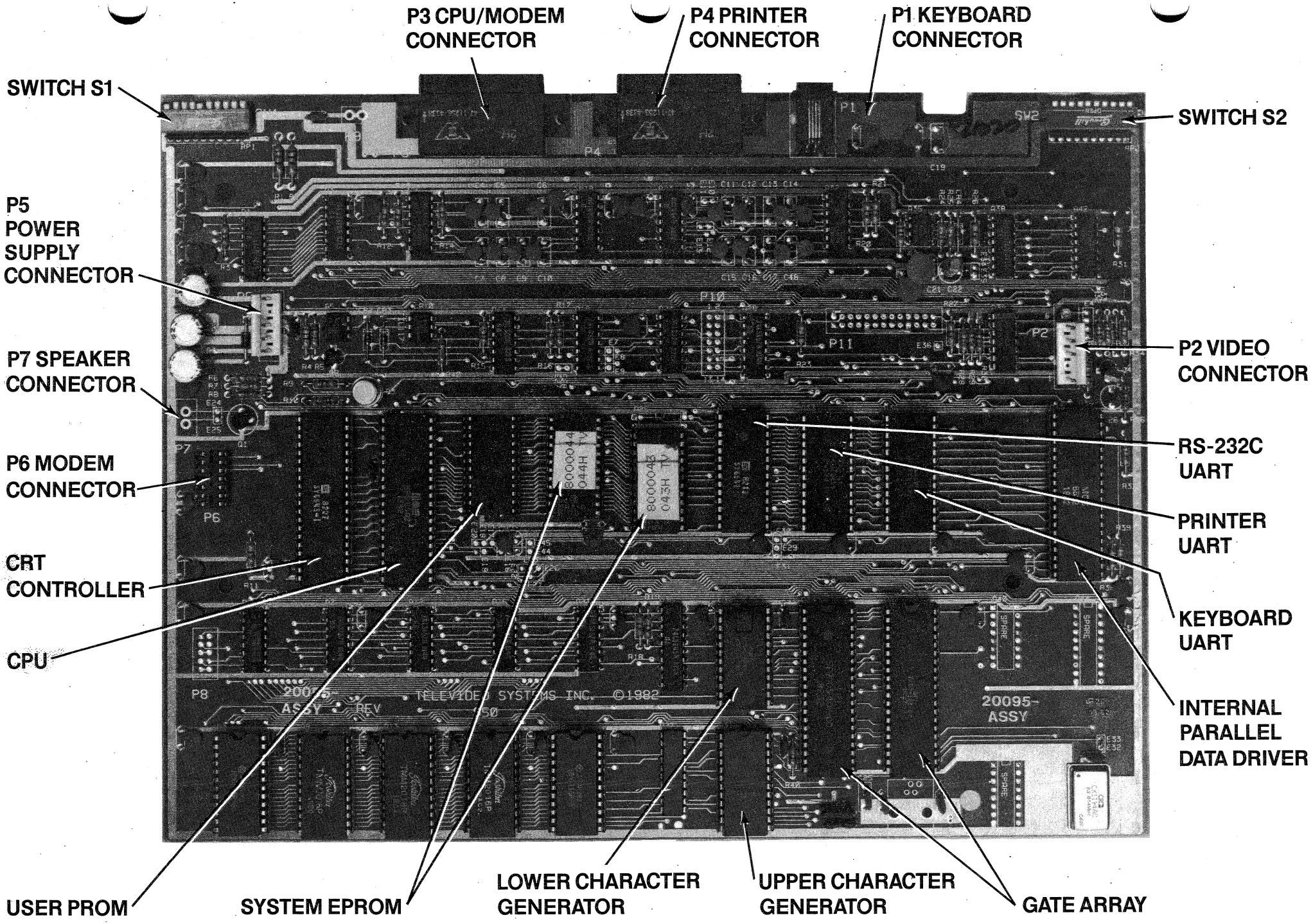
If the results of a matrix scan indicate that more than two keys are depressed, the program enters a delay loop for 11 ms. Meanwhile, the whole matrix is read once again to verify that the key is still depressed. After the key is proven to be valid, the microprocessor sends the proper code to the terminal.

If the depressed key is a repeat key, the last portion of the scan routine controls the length of the repeat delay (0.5 sec.) and the autorepeat rate (16 char/sec.). The program then branches back to the beginning of the scan routine.

950 GATE ARRAY LOGIC BOARD

Newer model 950 terminals have a green gate array logic board instead of the blue TTL logic board found in older versions. The logic and control signals are the same on both boards. However, on the gate array board, the logic gates have been incorporated into one integral semi-custom IC, referred to as the gate array chip. This substantially reduces the number of chips on the logic board and makes it simpler to troubleshoot to the component and signal level.

The corresponding logic schematic in this manual for the 950 gate array board is labeled **950 G/A.**



Gate Array Board

DOCUMENT NO. 29000 D39
REV. 3, FEBRUARY 1979

PART NUMBER
R650X and R651X

Rockwell

R6500 Microcomputer System DATA SHEET

R6500 MICROPROCESSORS (CPU's)

SYSTEM ABSTRACT

The 8-bit R6500 microcomputer system is produced with N-Channel, Silicon Gate technology. Its performance speeds are enhanced by advanced system architecture. This innovative architecture results in smaller chips — the semiconductor threshold to cost-effectivity. System cost-effectivity is further enhanced by providing a family of 10 software-compatible microprocessor (CPU) devices, described in this document. Rockwell also provides memory and microcomputer system . . . as well as low-cost design aids and documentation.

R6500 MICROPROCESSOR (CPU) CONCEPT

Ten CPU devices are available. All are software-compatible. They provide options of addressable memory, interrupt input, on-chip clock oscillators and drivers. All are bus-compatible with earlier generation microprocessors like the M6800 devices.

The family includes six microprocessors with on-board clock oscillators and drivers and four microprocessors driven by external clocks. The on-chip clock versions are aimed at high performance, low cost applications where single phase inputs, crystal or RC inputs provide the time base. The external clock versions are geared for multiprocessor system applications where maximum timing control is mandatory. All R6500 microprocessors are also available in a variety of packaging (ceramic and plastic), operating frequency (1 MHz and 2 MHz) and temperature (commercial, industrial and military) versions.

MEMBERS OF THE R6500 MICROPROCESSOR (CPU) FAMILY

Microprocessors with On-Chip Clock Oscillator

Model	Addressable Memory
R6502	65K Bytes
R6503	4K Bytes
R6504	8K Bytes
R6505	4K Bytes
R6506	4K Bytes
R6507	8K Bytes

Microprocessors with External Two Phase Clock Output

Model	Addressable Memory
R6512	65K Bytes
R6513	4K Bytes
R6514	8K Bytes
R6515	4K Bytes

FEATURES

- Single +5V supply
- N channel, silicon gate, depletion load technology
- Eight bit parallel processing
- 56 Instructions
- Decimal and binary arithmetic
- Thirteen addressing modes
- True indexing capability
- Programmable stack pointer
- Variable length stack
- Interrupt capability
- Non-maskable interrupt
- Use with any type of speed memory
- 8-bit Bidirectional Data Bus
- Addressable memory range of up to 65K bytes
- "Ready" input
- Direct Memory Access capability
- Bus compatible with M6800
- 1 MHz and 2 MHz operation
- Choice of external or on-chip clocks
- On-the-chip clock options
  - External single clock input
  - RC time base input
  - Crystal time base input
- Commercial, industrial and military temperature versions
- Pipeline architecture

Ordering Information

Order Number: R65XX___

- Temperature Range:
  - No suffix = 0°C to +70°C
  - E = -40°C to +85°C (Industrial)
  - MT = -55°C to +125°C (Military)
  - M = MIL-STD-883, Class B
- Package:
  - C = Ceramic
  - P = Plastic (Not Avaible for M or MT suffix)
- Frequency Range:
  - No suffix = 1 MHz
  - A = 2 MHz
- Model Designator:
  - XX = 02, 03, 04, ... 15

NOTE: Contact your local Rockwell Representative concerning availability.

R6500 MICROPROCESSORS (CPU's)

R6500 Signal Description

Clocks (ϕ_1, ϕ_2)

The R651X requires a two phase non-overlapping clock that runs at the V_{CC} voltage level.

The R650X clocks are supplied with an internal clock generator. The frequency of these clocks is externally controlled.

Address Bus (A0-A15)

These outputs are TTL compatible, capable of driving one standard TTL load and 130 pF.

Data Bus (D0-D7)

Eight pins are used for the data bus. This is a bidirectional bus, transferring data to and from the device and peripherals. The outputs are tri-state buffers capable of driving one standard TTL load and 130 pF.

Data Bus Enable (DBE)

This TTL compatible input allows external control of the tri-state data output buffers and will enable the microprocessor bus driver when in the high state. In normal operation DBE would be driven by the phase two (ϕ_2) clock, thus allowing data output from microprocessor only during ϕ_2. During the read cycle, the data bus drivers are internally disabled, becoming essentially an open circuit. To disable data bus drivers externally, DBE should be held low.

Ready (RDY)

This input signal allows the user to halt or single cycle the microprocessor on all cycles except write cycles. A negative transition to the low state during or coincident with phase one (ϕ_1) will halt the microprocessor with the output address lines reflecting the current address being fetched. If Ready is low during a write cycle, it is ignored until the following read operation. This condition will remain through a subsequent phase two (ϕ_2) in which the Ready signal is low. This feature allows microprocessor interfacing with the low speed PROMs as well as fast (max. 2 cycle) Direct Memory Access (DMA).

Interrupt Request ($\overline{IRQ}$)

This TTL level input requests that an interrupt sequence begin within the microprocessor. The microprocessor will complete the current instruction being executed before recognizing the request. At that time, the interrupt mask bit in the Status Code Register will be examined. If the interrupt mask flag is not set, the microprocessor will begin an interrupt sequence. The Program Counter and Processor Status Register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further interrupts may occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, therefore transferring program control to the memory vector located at these addresses. The RDY signal must be in the high state for any interrupt to be recognized. A 3KΩ external resistor should be used for proper wire-OR operation.

Non-Maskable Interrupt ($\overline{NMI}$)

A negative going edge on this input requests that a non-maskable interrupt sequence be generated within the microprocessor.

$\overline{NMI}$ is an unconditional interrupt. Following completion of the current instruction, the sequence of operations defined for $\overline{IRQ}$ will be performed, regardless of the state interrupt mask flag. The vector address loaded into the program counter, low and high, are locations FFFA and FFFB respectively, thereby transferring program control to the memory vector located at these addresses. The instructions loaded at these locations cause the microprocessor to branch to a non-maskable interrupt routine in memory.

$\overline{NMI}$ also requires an external 3K Ω register to V_{CC} for proper wire-OR operations.

Inputs $\overline{IRQ}$ and $\overline{NMI}$ are hardware interrupts lines that are sampled during ϕ_2 (phase 2) and will begin the appropriate interrupt routine on the ϕ_1 (phase 1) following the completion of the current instruction.

Set Overflow Flag (S.O.)

A negative going edge on this input sets the overflow bit in the Status Code Register. This signal is sampled on the trailing edge of ϕ_1 and must be externally synchronized.

SYNC

This output line is provided to identify those cycles in which the microprocessor is doing an OP CODE fetch. The SYNC line goes high during ϕ_1 of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the ϕ_1 clock pulse in which SYNC went high, the processor will stop in its current state and will remain in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.

Reset

This input is used to reset or start the microprocessor from a power down condition. During the time that this line is held low, writing to or from the microprocessor is inhibited. When a positive edge is detected on the input, the microprocessor will immediately begin the reset sequence.

After a system initialization time of six clock cycles, the mask interrupt flag will be set and the microprocessor will load the program counter from the memory vector locations FFFC and FFFD. This is the start location for program control.

After V_{CC} reaches 4.75 volts in a power up routine, reset must be held low for at least two clock cycles. At this time the R/W and (SYNC) signal will become valid.

When the reset signal goes high following these two clock cycles, the microprocessor will proceed with the normal reset procedure detailed above.

ADDRESSING MODES

ACCUMULATOR ADDRESSING — This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

IMMEDIATE ADDRESSING — In immediate addressing, the operand is contained in the second byte of the instruction, with no further memory addressing required.

ABSOLUTE ADDRESSING — In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Thus, the absolute addressing mode allows access to the entire 65K bytes of addressable memory.

ZERO PAGE ADDRESSING — The zero page instructions allow for shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in significant increase in code efficiency.

INDEXED ZERO PAGE ADDRESSING — (X, Y indexing) — This form of addressing is used in conjunction with the index register and is referred to as "Zero Page, X" or "Zero Page, Y". The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally due to the "Zero Page" addressing nature of this mode, no carry is added to the high order 8 bits of memory and crossing of page boundaries does not occur.

INDEXED ABSOLUTE ADDRESSING — (X, Y indexing) — This form of addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X", and "Absolute, Y". The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields resulting in reduced coding and execution time.

IMPLIED ADDRESSING — In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

RELATIVE ADDRESSING — Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is -128 to +127 bytes from the next instruction.

INDEXED INDIRECT ADDRESSING — In indexed indirect addressing (referred to as (Indirect, X)), the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents is the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

INDIRECT INDEXED ADDRESSING — In indirect indexed addressing (referred to as (Indirect), Y), the second byte of the instruction points to a memory location in page zero. The contents of this memory location is added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

ABSOLUTE INDIRECT — The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location is contained in the third byte of the instruction. The contents of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter.

INSTRUCTION SET — ALPHABETIC SEQUENCE

ADC Add Memory to Accumulator with Carry
AND "AND" Memory with Accumulator
ASL Shift left One Bit (Memory or Accumulator)

BCC Branch on Carry Clear
BCS Branch on Carry Set
BEQ Branch on Result Zero
BIT Test Bits in Memory with Accumulator
BMI Branch on Result Minus
BNE Branch on Result not Zero
BPL Branch on Result Plus
BRK Force Break
BVC Branch on Overflow Clear
BVS Branch on Overflow Set

CLC Clear Carry Flag
CLD Clear Decimal Mode
CLI Clear Interrupt Disable Bit
CLV Clear Overflow Flag
CMP Compare Memory and Accumulator
CPX Compare Memory and Index X
CPY Compare Memory and Index Y

DEC Decrement Memory by One
DEX Decrement Index X by One
DEY Decrement Index Y by One

EOR "Exclusive-or" Memory with Accumulator

INC Increment Memory by One
INX Increment Index X by One
INY Increment Index Y by One

JMP Jump to New Location
JSR Jump to New Location Saving Return Address

LDA Load Accumulator with Memory
LDX Load Index X with Memory
LDY Load Index Y with Memory
LSR Shift One Bit Right (Memory or Accumulator)

NOP No Operation

ORA "OR" Memory with Accumulator

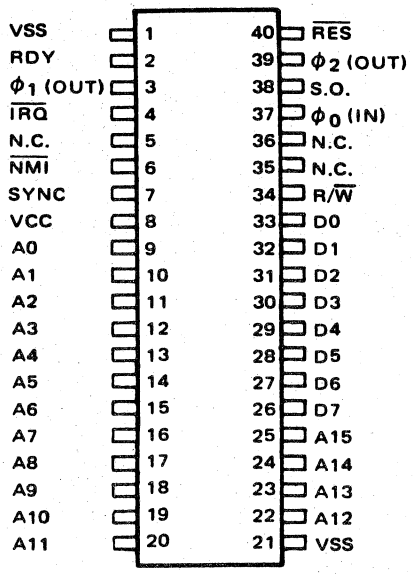
PHA Push Accumulator on Stack
PHP Push Processor Status on Stack
PLA Pull Accumulator from Stack
PLP Pull Processor Status from Stack

ROL Rotate One Bit Left (Memory or Accumulator)
ROR Rotate One Bit Right (Memory or Accumulator)
RTI Return from Interrupt
RTS Return from Subroutine

SBC Subtract Memory from Accumulator with Borrow
SEC Set Carry Flag
SED Set Decimal Mode
SEI Set Interrupt Disable Status
STA Store Accumulator in Memory
STX Store Index X in Memory
STY Store Index Y in Memory

TAX Transfer Accumulator to Index X
TAY Transfer Accumulator to Index Y
TSX Transfer Stack Pointer to Index X
TXA Transfer Index X to Accumulator
TXS Transfer Index X to Stack Register
TYA Transfer Index Y to Accumulator

R6502 – 40 Pin Package



Features of R6502

- 65K Addressable Bytes of Memory (A0-A15)
- $\overline{IRQ}$ Interrupt
- On-the-chip Clock
  - TTL Level Single Phase Input
  - RC Time Base Input
  - Crystal Time Base Input
- SYNC Signal
  (can be used for single instruction execution)
- RDY Signal
  (can be used to halt or single cycle execution)
- Two Phase Output Clock for Timing of Support Chips
- $\overline{NMI}$ Interrupt

INSTRUCTION SET

INSTRUCTIONS		IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM			IMPLIED			(IND. X)			(IND). Y			Z PAGE. X			ABS. X			ABS. Y			RELATIVE			INDIRECT			Z PAGE. Y			PROCESSOR STATUS CODES	
MNEMONIC	OPERATION	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	7 6 5 4 3 2 1 0 N V • B D I Z C	MNEMONIC
ADC	A + M + C → A (4) (1)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3										N V • • • • Z C	ADC
AND	A∧M → A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3										N • • • • • Z •	AND
ASL	C ← [7 0] ← 0				0E	6	3	06	5	2	0A	2	1										16	6	2	1E	7	3													N • • • • • Z C	ASL
BCC	BRANCH ON C = 0 (2)																															90	2	2							• • • • • • • •	BCC
BCS	BRANCH ON C = 1 (2)																															B0	2	2							• • • • • • • •	BCS
BEQ	BRANCH ON Z = 1 (2)																															F0	2	2							• • • • • • • •	BEQ
BIT	A∧M				2C	4	3	24	3	2																															M_7 M_6 • • • Z •	BIT
BMI	BRANCH ON N = 1 (2)																															30	2	2							• • • • • • • •	BMI
BNE	BRANCH ON Z = 0 (2)																															D0	2	2							• • • • • • • •	BNE
BPL	BRANCH ON N = 0 (2)																															10	2	2							• • • • • • • •	BPL
BRK	BREAK													00	7	1																									• • • • 1 • 1 • •	BRK
BVC	BRANCH ON V = 0 (2)																															50	2	2							• • • • • • • •	BVC
BVS	BRANCH ON V = 1 (2)																															70	2	2							• • • • • • • •	BVS
CLC	0 → C													18	2	1																									• • • • • • • 0	CLC
CLD	0 → D													D8	2	1																									• • • • 0 • • •	CLD
CLI	0 → I													58	2	1																									• • • • • 0 • •	CLI
CLV	0 → V													B8	2	1																									• 0 • • • • •	CLV
CMP	A − M	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3										N • • • • • Z C	CMP
CPX	X − M	E0	2	2	EC	4	3	E4	3	2																															N • • • • • Z C	CPX
CPY	Y − M	C0	2	2	CC	4	3	C4	3	2																															N • • • • • Z C	CPY
DEC	M − 1 → M				CE	6	3	C6	5	2													D6	6	2	DE	7	3													N • • • • • Z •	DEC
DEX	X − 1 → X													CA	2	1																									N • • • • • Z •	DEX
DEY	Y − 1 → Y													88	2	1																									N • • • • • Z •	DEY
EOR	A ∨ M → A (1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3										N • • • • • Z •	EOR
INC	M + 1 → M				EE	6	3	E6	5	2													F6	6	2	FE	7	3													N • • • • • Z •	INC
INX	X + 1 → X													E8	2	1																									N • • • • • Z •	INX
INY	Y + 1 → Y													C8	2	1																									N • • • • • Z •	INY
JMP	JUMP TO NEW LOC				4C	3	3																												6C	5	3				• • • • • • • •	JMP
JSR	JUMP SUB				20	6	3																																		• • • • • • • •	JSR
LDA	M → A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3										N • • • • • Z •	LDA
LDX	M → X (1)	A2	2	2	AE	4	3	A6	3	2																			BE	4	3							B6	4	2	N • • • • • Z •	LDX
LDY	M → Y (1)	A0	2	2	AC	4	3	A4	3	2													B4	4	2	BC	4	3													N • • • • • Z •	LDY
LSR	0 → [7 0] → C				4E	6	3	46	5	2	4A	2	1										56	6	2	5E	7	3													0 • • • • • Z C	LSR
NOP	NO OPERATION													EA	2	1																									• • • • • • • •	NOP
ORA	A ∨ M → A	09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3										N • • • • • Z •	ORA
PHA	A → Ms S − 1 → S													48	3	1																									• • • • • • • •	PHA
PHP	P → Ms S − 1 → S													08	3	1																									• • • • • • • •	PHP
PLA	S + 1 → S Ms → A													68	4	1																									N • • • • • Z •	PLA
PLP	S + 1 → S Ms → P													28	4	1																									(RESTORED)	PLP
ROL	[7 0] ← [C]				2E	6	3	26	5	2	2A	2	1										36	6	2	3E	7	3													N • • • • • Z C	ROL
ROR	[C] → [7 0]				6E	6	3	66	5	2	6A	2	1										76	6	2	7E	7	3													N • • • • • Z C	ROR
RTI	RTRN INT													40	6	1																									(RESTORED)	RTI
RTS	RTRN SUB													60	6	1																									• • • • • • • •	RTS
SBC	A − M − $\overline{C}$ → A (1)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3										N V • • • • Z (3)	SBC
SEC	1 → C													38	2	1																									• • • • • • • 1	SEC
SED	1 → D													F8	2	1																									• • • • 1 • • •	SED
SEI	1 → I													78	2	1																									• • • • • 1 • •	SEI
STA	A → M				8D	4	3	85	3	2							81	6	2	91	6	2	95	4	2	9D	5	3	99	5	3										• • • • • • • •	STA
STX	X → M				8E	4	3	86	3	2																													96	4	2	• • • • • • • •	STX
STY	Y → M				8C	4	3	84	3	2													94	4	2																• • • • • • • •	STY
TAX	A → X													AA	2	1																									N • • • • • Z •	TAX
TAY	A → Y													A8	2	1																									N • • • • • Z •	TAY
TSX	S → X													BA	2	1																									N • • • • • Z •	TSX
TXA	X → A													8A	2	1																									N • • • • • Z •	TXA
TXS	X → S													9A	2	1																									• • • • • • • •	TXS
TYA	Y → A													98	2	1																									N • • • • • Z •	TYA

(1) ADD 1 to N IF PAGE BOUNDARY IS CROSSED

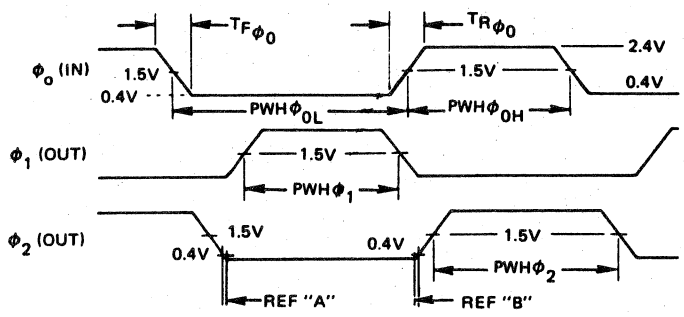
(2) ADD 1 TO N IF BRANCH OCCURS TO SAME PAGE
ADD 2 TO N IF BRANCH OCCURS TO DIFFERENT PAGE

(3) CARRY NOT = BORROW

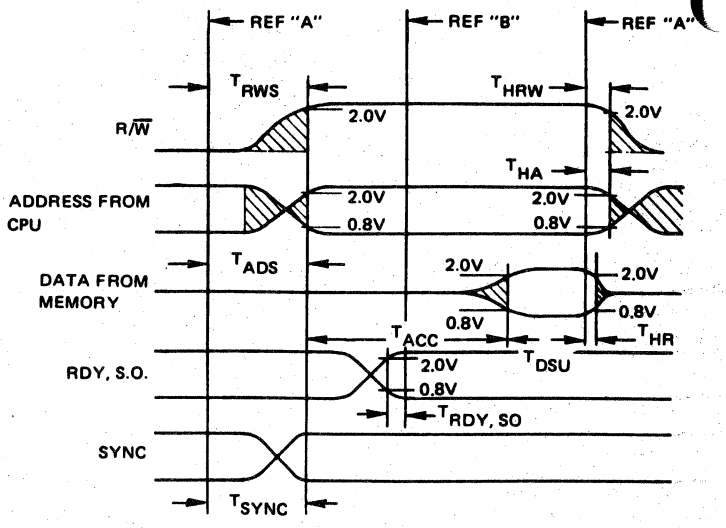
(4) IF IN DECIMAL MODE Z FLAG IS INVALID
ACCUMULATOR MUST BE CHECKED FOR ZERO RESULT

X	INDEX X	+	ADD
Y	INDEX Y	−	SUBTRACT
A	ACCUMULATOR	∧	AND
M	MEMORY PER EFFECTIVE ADDRESS	∨	OR
Ms	MEMORY PER STACK POINTER	∀	EXCLUSIVE OR
M_7	MEMORY BIT 7		
M_6	MEMORY BIT 6		
n	NO. CYCLES		
#	NO. BYTES		

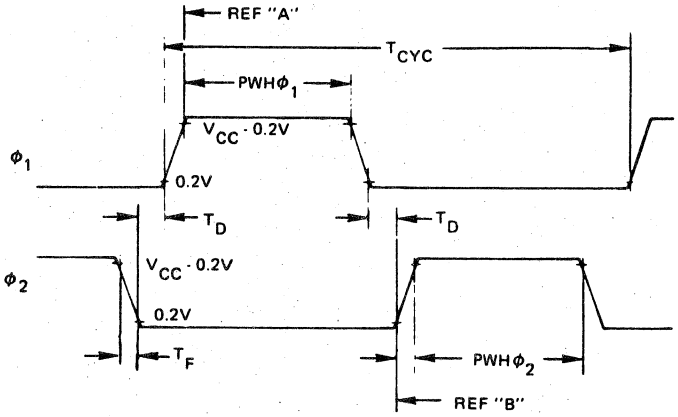
Clock Timing – R6502, 03, 04, 05, 06, 07



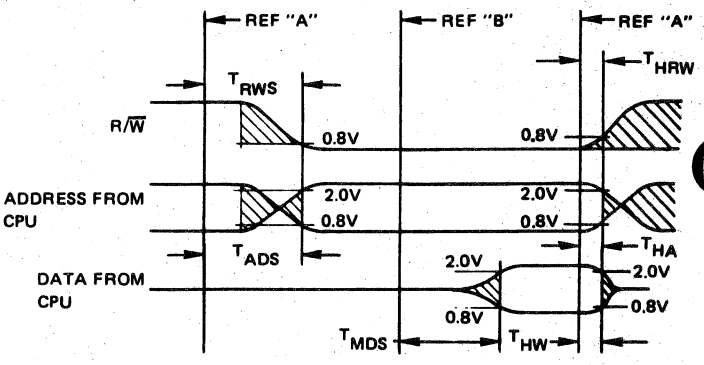
Timing for Reading Data from Memory or Peripherals



Clock Timing – R6512, 13, 14, 15

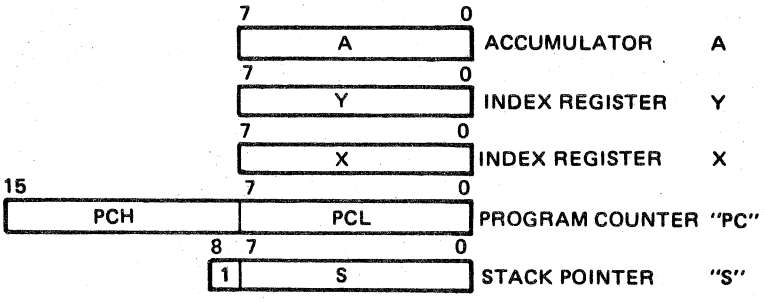


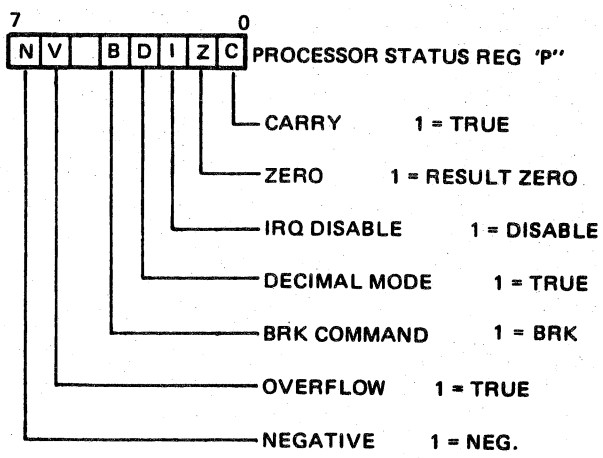
Timing for Writing Data to Memory or Peripherals

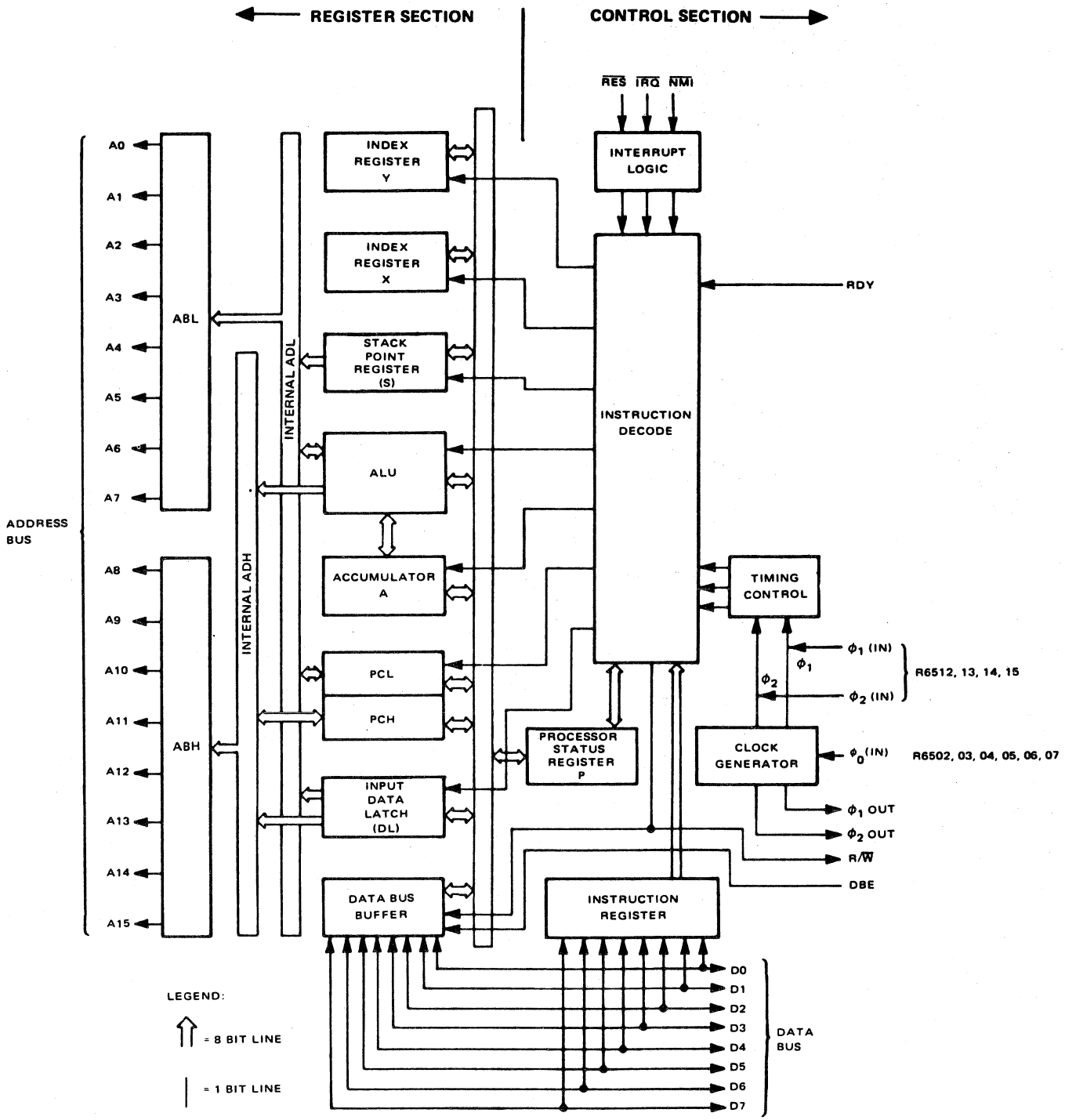


Note: "REF." means Reference Points on clocks.

PROGRAMMING MODEL







Note: 1. Clock Generator is not included on R6512, 13, 14, 15
2. Addressing Capability and control options vary with each of the R6500 Products.

R6500 Internal Architecture

DOCUMENT NO. 29000 D47
REVISION 1, OCT. 1978

PART NUMBER
R6522

Rockwell

R6500 Microcomputer System DATA SHEET

VERSATILE INTERFACE ADAPTER (VIA)

SYSTEM ABSTRACT

The 8-bit R6500 microcomputer system is produced with N-channel, silicon-gate, depletion-load technology. Its performance speeds are enhanced by advanced system architecture. Its innovative architecture results in smaller chips – the semiconductor threshold to cost-effectivity. System cost-effectivity is further enhanced by providing a family of 10 software-compatible microprocessor (CPU) devices, memory and I/O devices . . . as well as low-cost design aids and documentation.

DESCRIPTION

The R6522 VIA adds two powerful, flexible Interval Timers, a serial-to-parallel/parallel-to-serial shift register and input latching on the peripheral ports to the capabilities of the R6520 Peripheral Interface Adapter (PIA) device. Handshaking capability is expanded to allow control of bidirectional data transfers between VIAs in multiple processor systems and between peripherals.

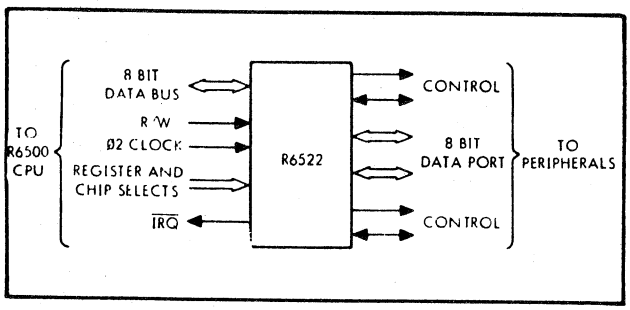
Control of peripherals is primarily through two 8-bit bidirectional ports. Each of these ports can be programmed to act as an input or an output. Peripheral I/O lines can be selectively controlled by the Interval Timers to generate programmable-frequency square waves and/or to count externally generated pulses. Positive control of VIA functions is gained through its internal register organization: Interrupt Flag Register, Interrupt Enable Register, and two Function Control Registers.

FEATURES

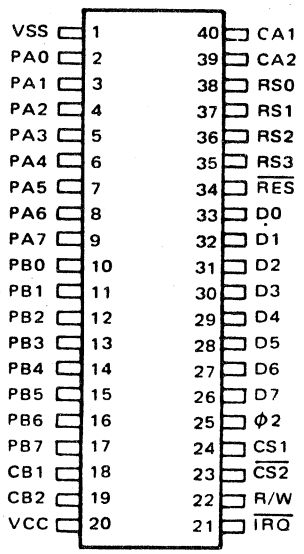
- Organized for simplified software control of many functions
- Compatible with the R650X and R651X family of microprocessors (CPUs)
- Bi-directional, 8-bit data bus for communication with microprocessor
- Two Bi-directional, 8-bit input/output ports for interface with peripheral devices
- CMOS and TTL compatible input/output peripheral ports
- Data Direction Registers allow each peripheral pin to act as either an input or an output
- Interrupt Flag Register allows the microprocessor to readily determine the source of an interrupt and provides convenient control of the interrupts within the chip
- Handshake control logic for input/output peripheral data transfer operations
- Data latching on peripheral input/output ports
- Two fully-programmable interval timers/counters
- Eight-bit Shift Register for serial interface
- Forty-pin plastic or ceramic DIP package.

Ordering Information

Order Number	Package Type	Frequency	Temperature Range
R6522P	Plastic	1 MHz	0°C to +70°C
R6522AP	Plastic	2 MHz	0°C to +70°C
R6522C	Ceramic	1 MHz	0°C to +70°C
R6522AC	Ceramic	2 MHz	0°C to +70°C
R6522PE	Plastic	1 MHz	-40°C to +85°C
R6522APE	Plastic	2 MHz	-40°C to +85°C
R6522CE	Ceramic	1 MHz	-40°C to +85°C
R6522ACE	Ceramic	2 MHz	-40°C to +85°C
R6522CMT	Ceramic	1 MHz	-55°C to +125°C



Basic R6522 Interface Diagram



Pin Configuration

R6522 VERSATILE INTERFACE ADAPTER (VIA)

Specifications subject to change without notice

OPERATION SUMMARY

Register Select Lines (RS0, RS1, RS2, RS3)

The four Register select lines are normally connected to the processor address bus lines to allow the processor to select the internal R6522 register which is to be accessed. The sixteen possible combinations access the registers as follows:

RS3	RS2	RS1	RS0	Register	Remarks	RS3	RS2	RS1	RS0	Register	Remarks
L	L	L	L	ORB		H	L	L	L	T2L-L T2C-L	Write Latch Read Counter
L	L	L	H	ORA	Controls Handshake						
L	L	H	L	DDRB		H	L	L	H	T2C-H	Triggers T2L-L/T2C-L Transfer
L	L	H	H	DDRA							
						H	L	H		SR	
L	H	L	L	T1L-L T1C-L	Write Latch Read Counter	H	L	H	H	ACR	
						H	H	L	L	PCR	
L	H	L	H	T1C-H	Trigger T1L-L/T1C-L Transfer	H	H	L	H	IFR	
						H	H	H	L	IER	
L	H	H	L	T1L-L		H	H	H	H	ORA	No Effect on Handshake
L	H	H	H	T1L-H							

Note: L = 0.4V DC, H = 2.4V DC.

Timer 2 Control

RS3	RS2	RS1	RS0	R/W = L	R/W = H
H	L	L	L	Write T2L-L	Read T2C-L Clear Interrupt flag
H	L	L	H	Write T2C-H Transfer T2L-L to T2C-L Clear Interrupt flag	Read T2C-H

Writing the Timer 1 Register

The operations which take place when writing to each of the four T1 addresses are as follows:

RS3	RS2	RS1	RS0	Operation (R/W = L)
L	H	L	L	Write into low order latch
L	H	L	H	Write into high order latch Write into high order counter Transfer low order latch into low order counter Reset T1 interrupt flag
L	H	H	L	Write low order latch
X	H	H	H	Write high order latch Reset T1 interrupt flag

Reading the Timer 1 Registers

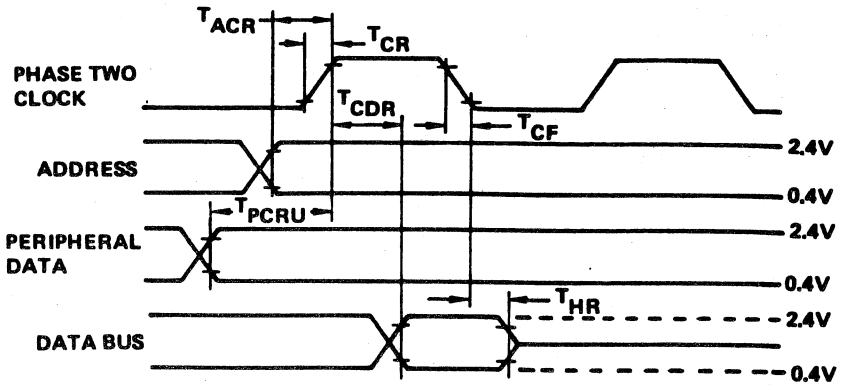
For reading the Timer 1 registers, the four addresses relate directly to the four registers as follows:

RS3	RS2	RS1	RS0	Operation (R/W = H)
L	H	L	L	Read T1 low order counter Reset T1 interrupt flag
L	H	L	H	Read T1 high order counter
L	H	H	L	Read T1 low order latch
L	H	H	H	Read T1 high order latch

TIMING CHARACTERISTICS

Read Timing Characteristics (loading 130 pF and one TTL load)

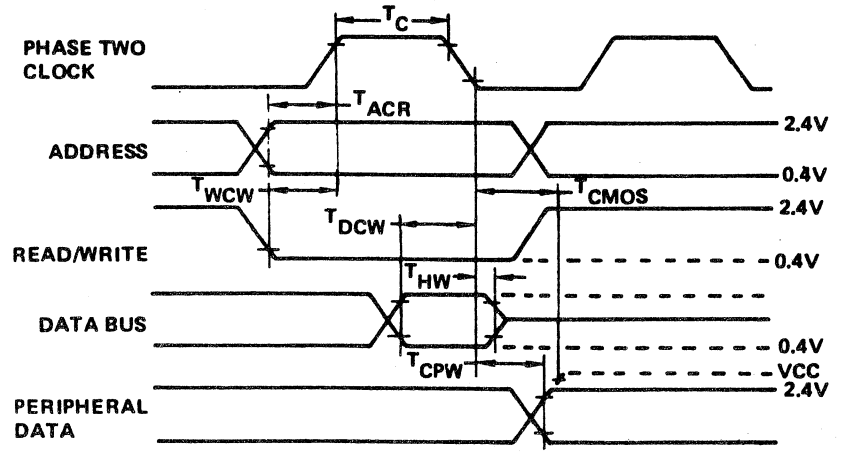
Parameter	Symbol	Min	Typ	Max	Unit
Delay time, address valid to clock positive transition	T_{ACR}	180	–	–	nS
Delay time, clock positive transition to data valid on bus	T_{CDR}	–	–	395	nS
Peripheral data setup time	T_{PCR}	300	–	–	nS
Data bus hold time	T_{HR}	10	–	–	nS
Rise and fall time for clock input	T_{RC} T_{RF}	–	–	25	nS



Read Timing Characteristics

Write Timing Characteristics

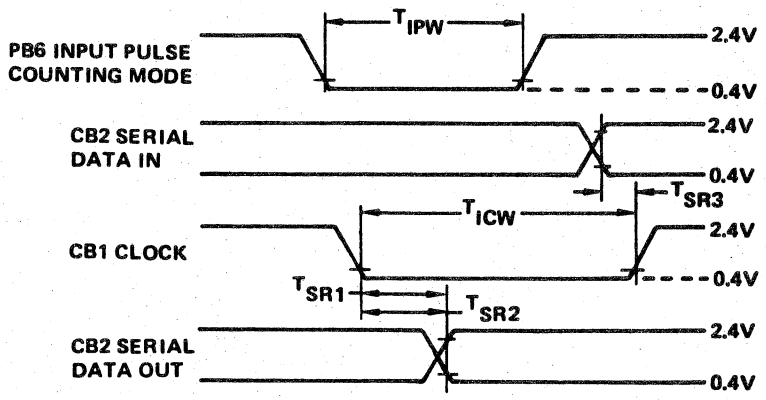
Parameter	Symbol	Min	Typ	Max	Unit
Enable pulse width	T_C	0.47	–	25	μS
Delay time, address valid to clock positive transition	T_{ACW}	180	–	–	nS
Delay time, data valid to clock negative transition	T_{DCW}	300	–	–	nS
Delay time, read/write negative transition to clock positive transition	T_{WCW}	180	–	–	nS
Data bus hold time	T_{HW}	10	–	–	nS
Delay time, Enable negative transition to peripheral data valid	T_{CPW}	–	–	1.0	μS
Delay time, clock negative transition to peripheral data valid CMOS (VCC - 30%)	T_{CMOS}	–	–	2.0	μS



Write Timing Characteristics

I/O Timing Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
Rise and fall time for CA1, CB1, CA2 and CB2 input signals	T_{RF}	–	–	1.0	μs
Delay time, clock negative transition to CA2 negative transition (read handshake or pulse mode)	T_{CA2}	–	–	1.0	μs
Delay time, clock negative transition to CA2 positive transition (pulse mode)	T_{RS1}	–	–	1.0	μs
Delay time, CA1 active transition to CA2 positive transition (handshake mode)	T_{RS2}	–	–	2.0	μs
Delay time, clock positive transition to CA2 or CB2 negative transition (write handshake)	T_{WHS}	–	–	1.0	μs
Delay time, peripheral data valid to CB2 negative transition	T_{DC}	0	–	1.5	μs
Delay time, clock positive transition to CA2 or CB2 positive transition (pulse mode)	T_{RS3}	–	–	1.0	μs
Delay time, CB1 active transition to CA2 or CB2 positive transition (handshake mode)	T_{RS4}	–	–	2.0	μs
Delay time, peripheral data valid to CA1 or CB1 active transition (input latching)	T_{IL}	300	–	–	ns
Delay time CB1 negative transition to CB2 data valid (internal SR clock, shift out)	T_{SR1}	–	–	300	ns
Delay time, negative transition of CB1 input clock to CB2 data valid (external clock, shift out)	T_{SR2}	–	–	300	ns
Delay time, CB2 data valid to positive transition of CB1 clock (shift in, internal or external clock)	T_{SR3}	–	–	300	ns
Pulse Width – PB6 Input Pulse	T_{IPW}	2	–	–	μs
Pulse Width – CB1 Input Clock	T_{ICW}	2	–	–	μs
Pulse Spacing – PB6 Input Pulse	I_{IPS}	2	–	–	μs
Pulse Spacing – CB1 Input Pulse	I_{ICS}	2	–	–	μs



I/O Timing Characteristics

Timer 1 Operating Modes

Two bits are provided in the Auxiliary Control Register to allow selection of the T1 operating modes. These bits and the four possible modes are as follows:

ACR7 Output Enable	ACR6 "Free-Run" Enable	Mode
0	0	Generate a single time-out interrupt each time T1 is loaded
0	1	Generate continuous interrupts
1	0	Generate a single interrupt and an output pulse on PB7 for each T1 load operation
1	1	Generate continuous interrupts and a square wave output on PB7

FUNCTION CONTROL

Control of the various functions and operating modes within the R6522 is accomplished primarily through two registers, the Peripheral Control Register (PCR), and the Auxiliary Control Register (ACR). The PCR is used primarily to select the operating mode for the four peripheral control pins. The Auxiliary Control Register selects the operating mode for the Interval Timers (T1, T2), and the Serial Port (SR).

Peripheral Control Register

The Peripheral Control Register is organized as follows:

Bit #	7	6	5	4	3	2	1	0
Function	CB2 Control			CB1 Control	CA2 Control			CA1 Control

Typical functions are shown below:

PCR3	PCR2	PCR1	Mode
0	0	0	Input mode – Set CA2 interrupt flag (IFR0) on a negative transition of the input signal. Clear IFR0 on a read or write of the Peripheral A Output Register.
0	0	1	Independent interrupt input mode – Set IFR0 on a negative transition of the CA2 input signal. Reading or writing ORA does not clear the CA2 interrupt flag.
0	1	0	Input mode – Set CA2 interrupt flag on a positive transition of the CA2 input signal. Clear IFR0 with a read or write of the Peripheral A Output Register.
0	1	1	Independent interrupt input mode – Set IFR0 on a positive transition of the CA2 input signal. Reading or writing ORA does not clear the CA2 interrupt flag.
1	0	0	Handshake output mode – Set CA2 output low on a read or write of the Peripheral A Output Register. Reset CA2 high with an active transition on CA1.
1	0	1	Pulse output mode – CA2 goes low for one cycle following a read or write of the Peripheral A Output Register.
1	1	0	Manual output mode – The CA2 output is held low in this mode.
1	1	1	Manual output mode – The CA2 output is held high in this mode.

Auxiliary Control Register

Many of the functions in the Auxiliary Control Register have been discussed previously. However, a summary of this register is presented here as a convenient reference for the R6522 user. The Auxiliary Control Register is organized as follows:

Bit #	7	6	5	4	3	2	1	0
Function	T1 Control		T2 Control	Shift Register Control			PB Latch Enable	PA Latch Enable

Shift Register Control

The Shift Register operating mode is selected as follows:

ACR4	ACR3	ACR2	Mode
0	0	0	Shift Register Disabled.
0	0	1	Shift in under control of Timer 2.
0	1	0	Shift in under control of system clock.
0	1	1	Shift in under control of external clock pulses.
1	0	0	Free-running output at rate determined by Timer 2.
1	0	1	Shift out under control of Timer 2.
1	1	0	Shift out under control of the system clock.
1	1	1	Shift out under control of external clock pulses.

T2 Control

Timer 2 operates in two modes. If ACR5 = 0, T2 acts as an interval timer in the one-shot mode. If ACR5 = 1, Timer 2 acts to count a predetermined number of pulses on pin PB6.

Rockwell

R6500 Microcomputer System
DATA SHEET

CRT CONTROLLER (CRTC)

DESCRIPTION

The R6545-1 CRT Controller (CRTC) is designed to interface an 8-bit microprocessor to CRT raster scan video displays, and adds an advanced CRT controller to the established and expanding line of R6500 products.

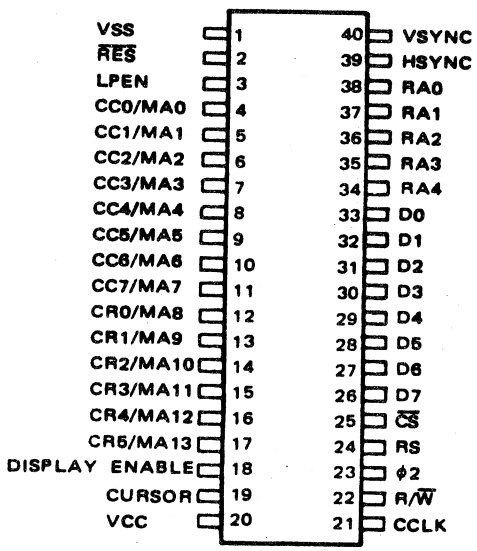
The R6545-1 provides refresh memory addresses and character generator row addresses which allow up to 16K characters with 32 scan lines per character to be addressed. A major advantage of the R6545-1 is that the refresh memory may be addressed in either straight binary or by row/column.

Other functions in the R6545-1 include an internal cursor register which generates a cursor output when its contents are equal to the current refresh address. Programmable cursor start and end registers allow a cursor of up to the full character scan in height to be placed on any scan lines of the character. Variable cursor display blink rates are provided. A light pen strobe input allows capture of the current refresh address in an internal light pen register. The refresh address lines are configured to provide direct dynamic memory refresh.

All timing for the video refresh memory signals is derived from the character clock input. Shift register, latch, and multiplex control signals (when needed) are provided by external high-speed timing. The mode control register allows non-interlaced video display modes at 50 or 60 Hz refresh rate. The internal status register may be used to monitor the R6545-1 operation. The $\overline{RES}$ input allows the CRTC-generated field rate to be dynamically-synchronized with line frequency jitter.

FEATURES

- Compatible with 8-bit microprocessors
- Up to 2.5 MHz character clock operation
- Refresh RAM may be configured in row/column or straight binary addressing
- Alphanumeric and limited graphics capability
- Up and down scrolling by page, line, or character
- Programmable Vertical Sync Width
- Fully programmable display (rows, columns, character matrix)
- Non-interlaced scan
- 50/60 Hz operation
- Fully programmable cursor
- Light pen register
- Addresses refresh RAM to 16K characters
- No external DMA required
- Internal status register
- 40-Pin ceramic or plastic DIP
- Pin-compatible with MC6845
- Single +5 ±5% Volt Power Supply



R6545-1 Pin Configuration

ORDERING INFORMATION

Part Number	Package Type	Frequency	Temperature Range
R6545-1P	Plastic	1 MHz	0°C to +70°C
R6545-1AP	Plastic	2 MHz	0°C to +70°C
R6545-1C	Ceramic	1 MHz	0°C to +70°C
R6545-1AC	Ceramic	2 MHz	0°C to +70°C

Specifications subject to change without notice
Document No. 29000 D67
December 1980

INTERFACE SIGNAL DESCRIPTION

CPU INTERFACE

ϕ2 (Phase 2 Clock)

The input clock is the system Phase 2 (ϕ2) clock and is used to trigger all data transfers between the system processor (CPU) and the R6545-1. Since there is no maximum limit to the allowable ϕ2 clock time, it is not necessary for it to be a continuous clock. This capability permits the R6545-1 to be easily interfaced to non-6500 compatible microprocessors.

R/$\overline{W}$ (Read/Write)

The R/$\overline{W}$ input signal generated by the processor is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the R6545-1, a low on the R/$\overline{W}$ pin allows data on data lines D0-D7 to be written into the R6545-1.

$\overline{CS}$ (Chip Select)

The Chip Select input is normally connected to the processor address bus either directly or through a decoder. The R6545-1 is selected when $\overline{CS}$ is low.

RS (Register Select)

The Register Select input is used to access internal registers. A low on this pin permits writes (R/$\overline{W}$ = low) into the Address Register and reads (R/$\overline{W}$ = high) from the Status Register. The contents of the Address Register is the identity of the register accessed when RS is high.

D0-D7 (Data Bus)

D0-D7 are the eight data lines used to transfer data between the processor and the R6545-1. These lines are bidirectional and are normally high-impedance except during read cycles when the chip is selected ($\overline{CS}$ = low).

VIDEO INTERFACE

HSYNC (Horizontal Sync)

The HSYNC signal is an active-high output used to determine the horizontal position of displayed text. It may drive a CRT monitor directly or may be used for composite video generation. HSYNC time position and width are fully programmable.

VSYNC (Vertical Sync)

The VSYNC signal is an active high output used to determine the vertical position of displayed text. Like HSYNC, VSYNC may be used to drive a CRT monitor or composite video generation circuits. VSYNC time position and width are both programmable.

DISPLAY ENABLE (Display Enable)

The DISPLAY ENABLE signal is an active-high output used to indicate when the R6545-1 is generating active display information. The number of horizontal display characters per row and the number of vertical display rows are both fully programmable and together are used to generate the DISPLAY ENABLE signal. DISPLAY ENABLE can be delayed one character time by setting bit 4 of R8 equal to 1.

CURSOR (Cursor Coincidence)

The CURSOR signal is an active-high output used to indicate when the scan coincides with the programmed cursor position. The cursor position may be programmed to be any character in the address field. Furthermore, within the character, the cursor may be programmed to be any block of scan lines, since the start scan line and the end scan line are both programmable. The cursor position may be delayed by one character time by setting Bit 5 of R8 to A "1".

LPEN (Light Pen Strobe)

The LPEN signal is an edge-sensitive input used to load the internal Light Pen Register with the contents of the Refresh Scan Counter at the time the active edge occurs. The active edge of LPEN is the low-to-high transition.

CCLK (Clock)

The CCLK signal is the character timing clock input and is used as the time base for all internal count/control functions.

$\overline{RES}$

The $\overline{RES}$ signal is an active-low input used to initialize all internal scan counter circuits. When $\overline{RES}$ is low, all internal counters are stopped and cleared, all scan and video outputs are low, and control registers are unaffected. $\overline{RES}$ must stay low for at least one CCLK period. All scan timing is initiated when $\overline{RES}$ goes high. In this way, $\overline{RES}$ can be used to synchronize display frame timing with line frequency. $\overline{RES}$ may also be used to synchronize multiple CRTC's in horizontal and/or vertical split screen operation.

REFRESH RAM AND CHARACTER ROM INTERFACE

MA0-MA13 (Refresh RAM Address Lines)

These 14 signals are active-high outputs used to address the Refresh RAM for character storage and display operations. The starting scan address is fully programmable and the ending scan address is determined by the total number of characters displayed, which is also programmable, in terms of characters/line and lines/frame.

There are two selectable address modes for MA0-MA13:

In the straight binary mode (R8, Mode Control, bit 2 = "0"), characters are stored in successive memory locations. Thus, the software must be designed such that row and column character coordinates are translated into sequentially-numbered addresses. In the row/column mode (R8, Mode Control, bit 2 = "1"), MA0-MA7 become column addresses CC0-CC7 and MA8-MA13 become row addresses CR0-CR5. In this case, the software can manipulate characters in terms of row and column locations, but additional address compression circuits are needed to convert the CC0-CC7 and CR0-CR5 addresses into a memory-efficient binary address scheme.

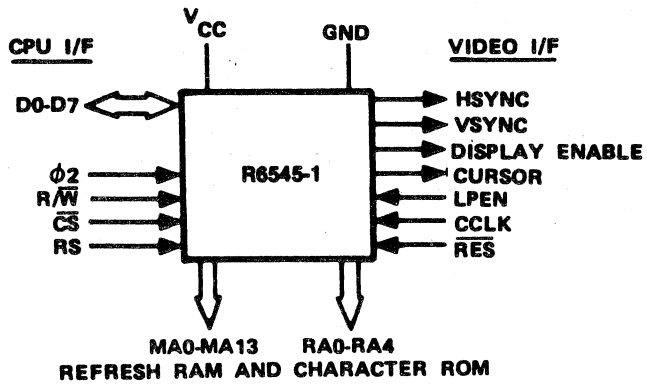
RA0-RA4 (Raster Address Lines)

These 5 signals are active-high outputs used to select each raster scan within an individual character row. The number of raster scan lines is programmable and determines the character height, including spaces between character rows.

INTERNAL REGISTER ORGANIZATION

$\overline{CS}$	RS	Address Register 4	3	2	1	0	Reg. No.	Register Name	Register Units	Read ($R/\overline{W}$ = High)	Write ($R/\overline{W}$ = Low)	Register Bit 7	6	5	4	3	2	1	0
1	X	X	X	X	X	X	X												
0	0	X	X	X	X	X	X	Address Register	Register No.		✓				4	3	2	1	0
0	0	X	X	X	X	X	X	Status Register	–	✓			6	5					
0	1	0	0	0	0	0	R0	Horizontal Total Char	No. of Characters/Row		✓	7	6	5	4	3	2	1	0
0	1	0	0	0	0	1	R1	Horizontal Displayed Char	No. of Characters/Row		✓	7	6	5	4	3	2	1	0
0	1	0	0	0	1	0	R2	Horizontal Sync Position	Character Position		✓	7	6	5	4	3	2	1	0
0	1	0	0	0	1	1	R3	YSYNC, HSYNC Widths	No. of Scan Lines, Characters		✓	7	6	5	4	3	2	1	0
0	1	0	0	1	0	0	R4	Vertical Total Rows	No. of Character Rows		✓		6	5	4	3	2	1	0
0	1	0	0	1	0	1	R5	Vertical Total Adjust Lines	No. of Scan Lines		✓				4	3	2	1	0
0	1	0	0	1	1	0	R6	Vertical Displayed Rows	No. of Character Rows		✓		6	5	4	3	2	1	0
0	1	0	0	1	1	1	R7	Vertical Sync Position	No. of Character Rows		✓		6	5	4	3	2	1	0
0	1	0	1	0	0	0	R8	Mode Control	–		✓	7	6	5	4	3	2	1	0
0	1	0	1	0	0	1	R9	Scan Line	No. of Scan Lines		✓				4	3	2	1	0
0	1	0	1	0	1	0	R10	Cursor Start Line	Scan Line No.		✓		6	5	4	3	2	1	0
0	1	0	1	0	1	1	R11	Cursor End Line	Scan Line No.		✓				4	3	2	1	0
0	1	0	1	1	0	0	R12	Display Start Address (H)	–		✓			5	4	3	2	1	0
0	1	0	1	1	0	1	R13	Display Start Address (L)	–		✓	7	6	5	4	3	2	1	0
0	1	0	1	1	1	0	R14	Cursor Position Address (H)	–	✓	✓			5	4	3	2	1	0
0	1	0	1	1	1	1	R15	Cursor Position Address (L)	–	✓	✓	7	6	5	4	3	2	1	0
0	1	1	0	0	0	0	R16	Light Pen Register (H)	–	✓				5	4	3	2	1	0
0	1	1	0	0	0	1	R17	Light Pen Register (L)	–	✓		7	6	5	4	3	2	1	0

Table 1. Overall Register Structure and Addressing



R6545-1 Interface Diagram

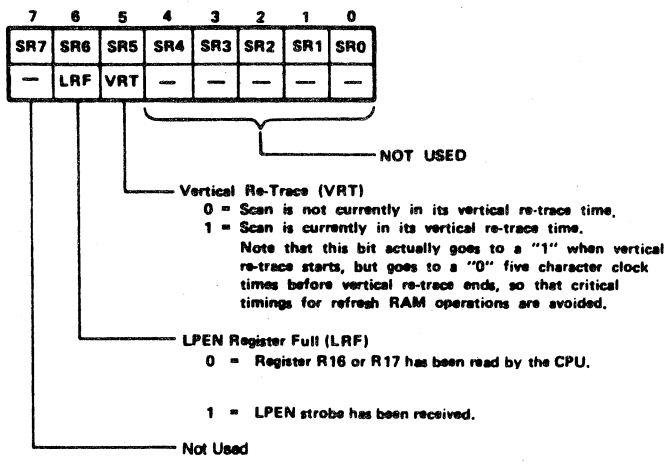
INTERNAL REGISTER DESCRIPTION

ADDRESS REGISTER

This 5-bit write-only register is used as a "pointer" to direct CRTC/CPU data transfers within the CRTC. Its contents is the number of the desired register (0-17). When $\overline{CS}$ and RS are low, then this register may be loaded; when $\overline{CS}$ is low and RS is high, then the register selected is the one whose identity is stored in this address register.

STATUS REGISTER (SR)

This 8-bit register contains the status of the CRTC. Only two bits are assigned, as follows:



NOTE: The Status Register takes the State, | – | 0 | 1 | – | – | – | – | – | immediately after power (V_{CC}) turn-on.

R0—HORIZONTAL TOTAL CHARACTERS

This 8-bit write-only register contains the total of displayed and non-displayed characters, minus one, per horizontal line. The frequency of HSYNC is thus determined by this register.

R1—HORIZONTAL DISPLAYED CHARACTERS

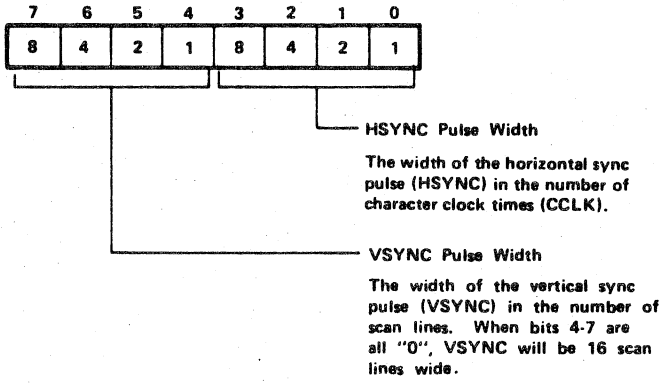
This 8-bit write-only register contains the number of displayed characters per horizontal line.

R2—HORIZONTAL SYNC POSITION

This 8-bit write-only register contains the position of the horizontal SYNC on the horizontal line, in terms of the character location number on the line. The position of the HSYNC determines the left to right location of the displayed text on the video screen. In this way, the side margins are adjusted.

R3—HORIZONTAL AND VERTICAL SYNC WIDTHS

This 8-bit write-only register contains the widths of both HSYNC and VSYNC, as follows:



Control of these parameters allows the R6545-1 to be interfaced to a variety of CRT monitors, since the HSYNC and VSYNC timing signals may be accommodated without the use of external one shot timing.

R4—VERTICAL TOTAL ROWS

The Vertical Total Register is a 7-bit register containing the total number of character rows in a frame, minus one. This register, along with R5, determines the overall frame rate, which should be close to the line frequency to ensure flicker-free appearance. If the frame time is adjusted to be longer than the period of the line frequency, then $\overline{RES}$ may be used to provide absolute synchronism.

R5—VERTICAL TOTAL LINE ADJUST

The Vertical Total Line Adjust Register (R5) is a 5-bit write-only register containing the number of additional scan lines needed to complete an entire frame scan and is intended as a fine adjustment for the video frame time.

R6—VERTICAL DISPLAYED ROWS

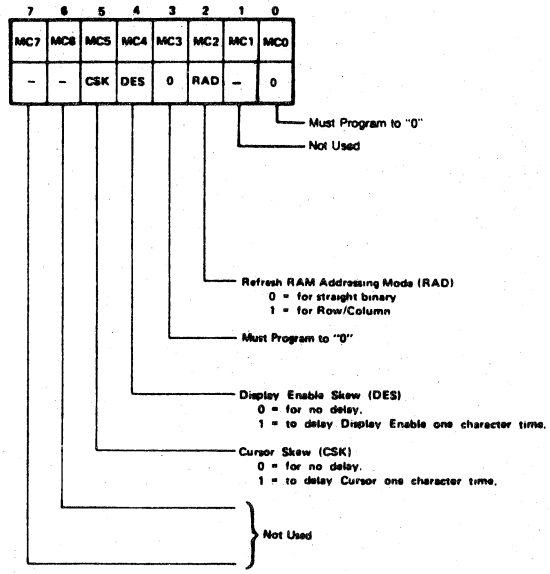
This 7-bit write-only register contains the number of displayed character rows in each frame.

R7—VERTICAL SYNC POSITION

This 7-bit write-only register is used to select the character row time at which the vertical SYNC pulse is desired to occur and, thus, is used to position the displayed text in the vertical direction.

R8—MODE CONTROL (MC)

This 8-bit write-only register selects the operating modes of the R6545-1, as follows:



R9—ROW SCAN LINES

This 5-bit write-only register contains the number of scan lines, minus one, per character row, including spacing.

R10—CURSOR START LINE
R11—CURSOR END LINE

These 5-bit write-only registers select the starting and ending scan lines for the cursor. In addition, bits 5 and 6 of R10 are used to select the cursor blink mode, as follows:

Bit 6	Bit 5	Cursor Blink Mode
0	0	Display Cursor Continuously
0	1	Blank Cursor Continuously
1	0	Blink Cursor at 1/16 Field Rate
1	1	Blink Cursor at 1/32 Field Rate

R12—DISPLAY START ADDRESS HIGH
R13—DISPLAY START ADDRESS LOW

These registers form a 14-bit register whose contents is the memory address of the first character of the displayed scan (the character on the top left of the video display, as in Figure 1). Subsequent memory addresses are generated by the R6545-1 as a result of CCLK input pulses. Scrolling of the display is accomplished by changing R12 and R13 to the memory address associated with the first character of the desired line of text to be displayed first. Entire pages of text may be scrolled or changed as well via R12 and R13.

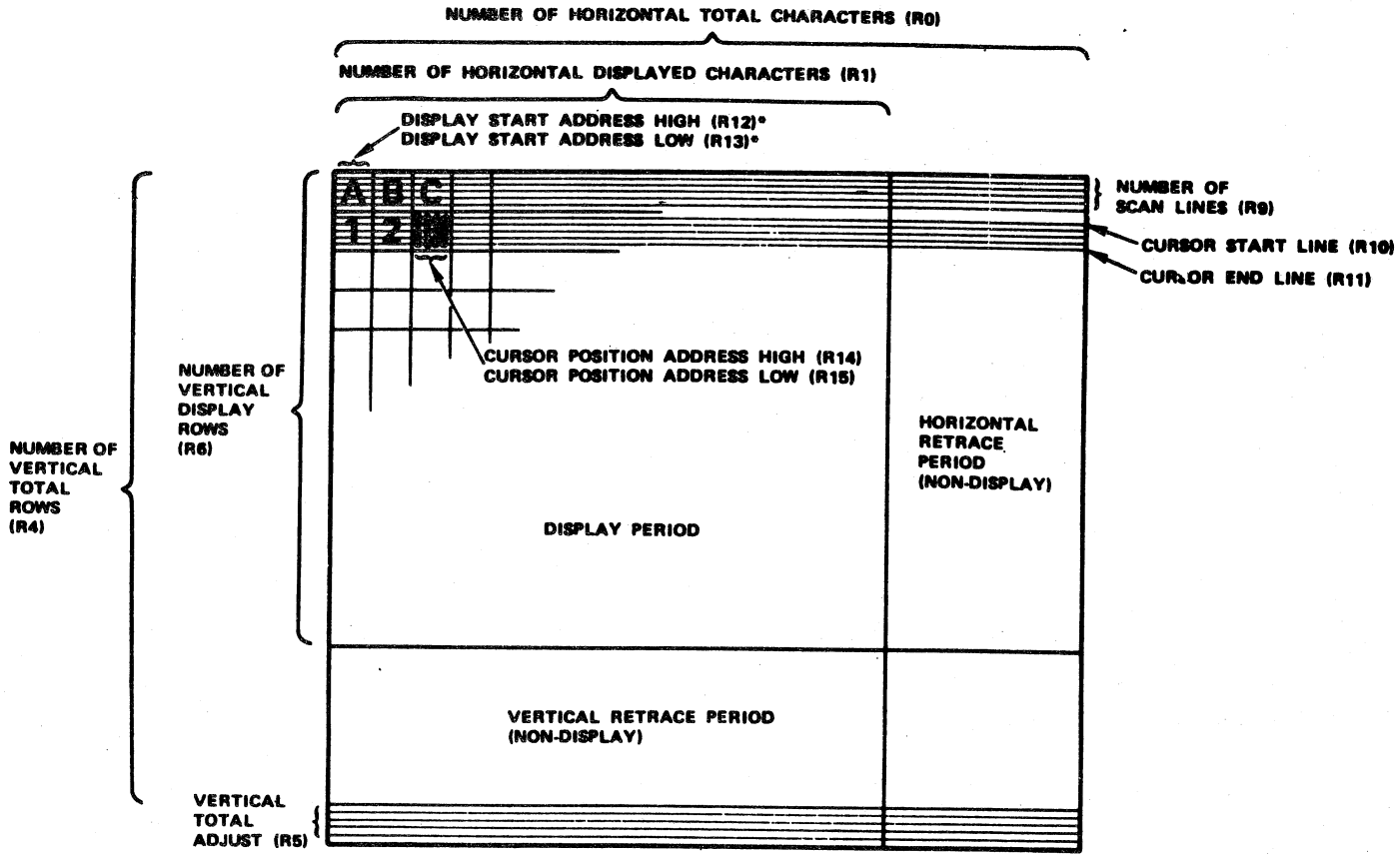


Figure 1. Video Display Format

R14—CURSOR POSITION HIGH
R15—CURSOR POSITION LOW

These registers form a 14-bit register whose contents is the memory address of the current cursor position. When the video display scan counter (MA lines) matches the contents of this register, and when the scan line counter (RA lines) falls within the bounds set by R10 and R11, then the CURSOR output becomes active. Bit 5 of the Mode Control Register (R8) may be used to delay the CURSOR output by a full CCLK time to accommodate slow access memories.

R16—LIGHT PEN HIGH
R17—LIGHT PEN LOW

These registers form a 14-bit register whose contents is the light pen strobe position, in terms of the video display address at which the strobe occurred. When the LPEN input changes from low to high, then, on the next negative-going edge of CCLK, the contents of the internal scan counter is stored in registers R16 and R17.

REGISTER FORMATS

Register pairs R12/R13, R14/R15, and R16/R17 are formatted in one of two ways:

(1) Straight binary, if register R8, bit 2 = "0".

(2) Row/Column, if register R8, bit 2 = "1". In this case the low byte is the Character Column and the high byte is the Character Row.

DESCRIPTION OF OPERATION

VIDEO DISPLAY

Figure 1 indicates the relationship of the various program registers in the R6545-1 and the resultant video display.

Non-displayed areas of the Video Display are used for horizontal and vertical retrace functions of the CRT monitor. The horizontal and vertical sync signals, HSYNC and VSYNC, are programmed to occur during these intervals and are used to trigger the retrace in the CRT monitor. The pulse widths are constrained by the monitor requirements. The time position of the pulses may be adjusted to vary the display margins (left, right, top, and bottom).

REFRESH RAM ADDRESSING

Shared Memory Mode (R8, bit 3 = "0")

In this mode, the Refresh RAM address lines (MA0-MA13) directly reflect the contents of the internal refresh scan character counter. Multiplex control, to permit addressing and selection of the RAM by both the CPU and the CRTC, must be provided external to the CRTC. In the Row/Column address mode, lines MA0-MA7 become character column addresses (CC0-CC7) and MA8-MA13 become character row addresses (CR0-CR5).

ADDRESSING MODES

Row/Column

In this mode, the CRTC address lines (MA0-MA13) are generated as 8 column (MA0-MA7) and 6 row (MA8-MA13) addresses. Extra hardware is needed to compress this addressing into a straight binary sequence in order to conserve memory in the refresh RAM.

Binary

In this mode, the CRTC address lines are straight binary and no compression circuits are needed. However, software complexity is increased since the CRT characters cannot be stored in terms of their row and column locations, but must be sequential.

USE OF DYNAMIC RAM FOR REFRESH MEMORY

The R6545-1 permits the use of dynamic RAMS as storage devices for the Refresh RAM by continuing to increment memory addresses in the non-display intervals of the scan. This is a viable technique, since the Display Enable signal controls the actual video display blanking. Figure 2 illustrates Refresh RAM addressing for the case of binary addressing for 80 columns and 24 rows with 10 non-displayed columns and 10 non-displayed rows.

TOTAL = 90

DISPLAY = 80

TOTAL = 34

DISPLAY = 24

0	1	2	3		76	77	78	79	80	81		89
80	81	82	83		156	157	158	159	160	161		169
160	161	162				237	238	239	240			249
240	241	242				317	318	319	320			329
1680	1681	1682				1757	1758	1759	1760			1769
1760	1761	1762				1837	1838	1839	1840			1849
1840	1841	1842				1917	1918	1919	1920			1929
1920	1921	1922				1997	1998	1999	2000			2009
2000	2001	2002				2077	2078	2079	2080			2089
2640	2641	2642				2717	2718	2720				2729

Figure 2. Memory Addressing Example (80 x 24)

CURSOR OPERATION

A one character wide cursor can be controlled by storing values into the Cursor Start Line (R10) and Cursor End Line (R11) registers and into the Cursor Position Address High (R14) and Cursor Position Low (R15) registers.

Bits 5 and 6 in the Cursor Start Line High Register (R10) control the cursor display and blink rate as follows:

Bit 6	Bit 5	Cursor Operating Mode
0	0	Display Cursor Continuously
0	1	Blank Cursor Continuously
1	0	Blink Cursor at 1/16 Field Rate
1	1	Blink Cursor at 1/32 Field Rate

The cursor of up to 32 characters in height can be displayed on and between the scan lines as loaded into the Cursor Start Line (R10) and Cursor End Line (R11) Registers.

The cursor is positioned on the screen by loading the Cursor Position Address High (R14) and Cursor Position Address Low (R15) registers with the desired refresh RAM address. The cursor can be positioned in any of the 16K character positions. Hardware paging and data scrolling is thus allowed without loss of cursor position. Figure 3 is an example of the display cursor scan line.

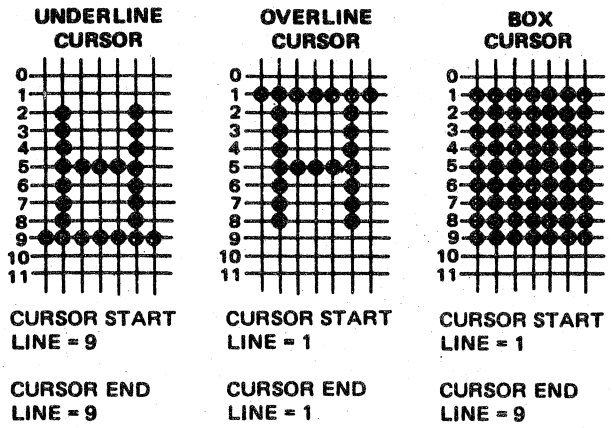


Figure 3. Cursor Display Scan Line Control Examples

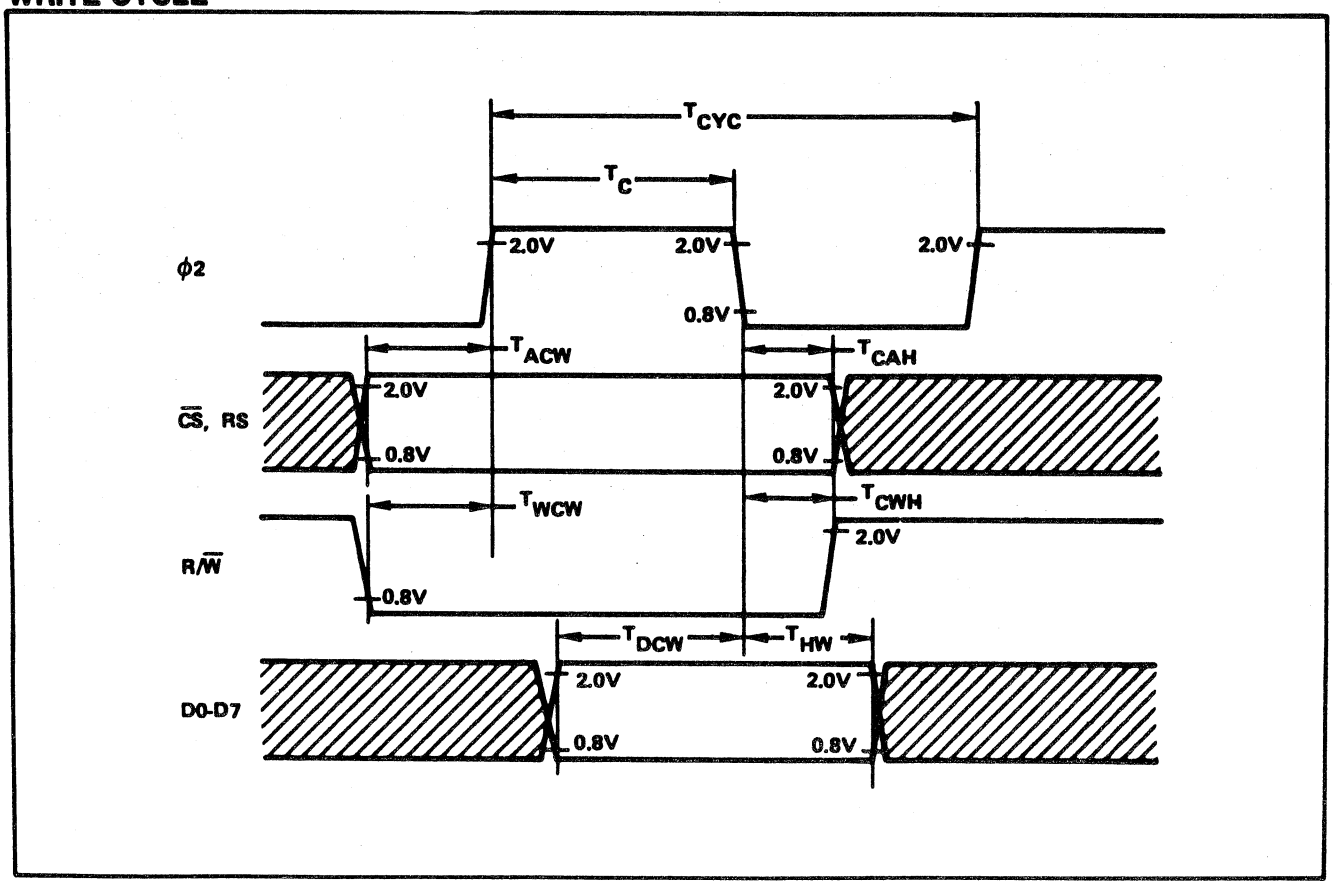
MPU WRITE TIMING CHARACTERISTICS

(V_{CC} = 5.0V ±5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristic	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Cycle Time	T_{CYC}	1.0	–	0.5	–	μs
Ø2 Pulse Width	T_C	440	–	200	–	ns
Address Set-Up Time	T_{ACW}	180	–	90	–	ns
Address Hold Time	T_{CAH}	0	–	0	–	ns
R/$\overline{W}$ Set-Up Time	T_{WCW}	180	–	90	–	ns
R/$\overline{W}$ Hold Time	T_{CWH}	0	–	0	–	ns
Data Bus Set-Up Time	T_{DCW}	265	–	100	–	ns
Data Bus Hold Time	T_{HW}	10	–	10	–	ns

(t_r and t_f = 10 to 30 ns)

WRITE CYCLE



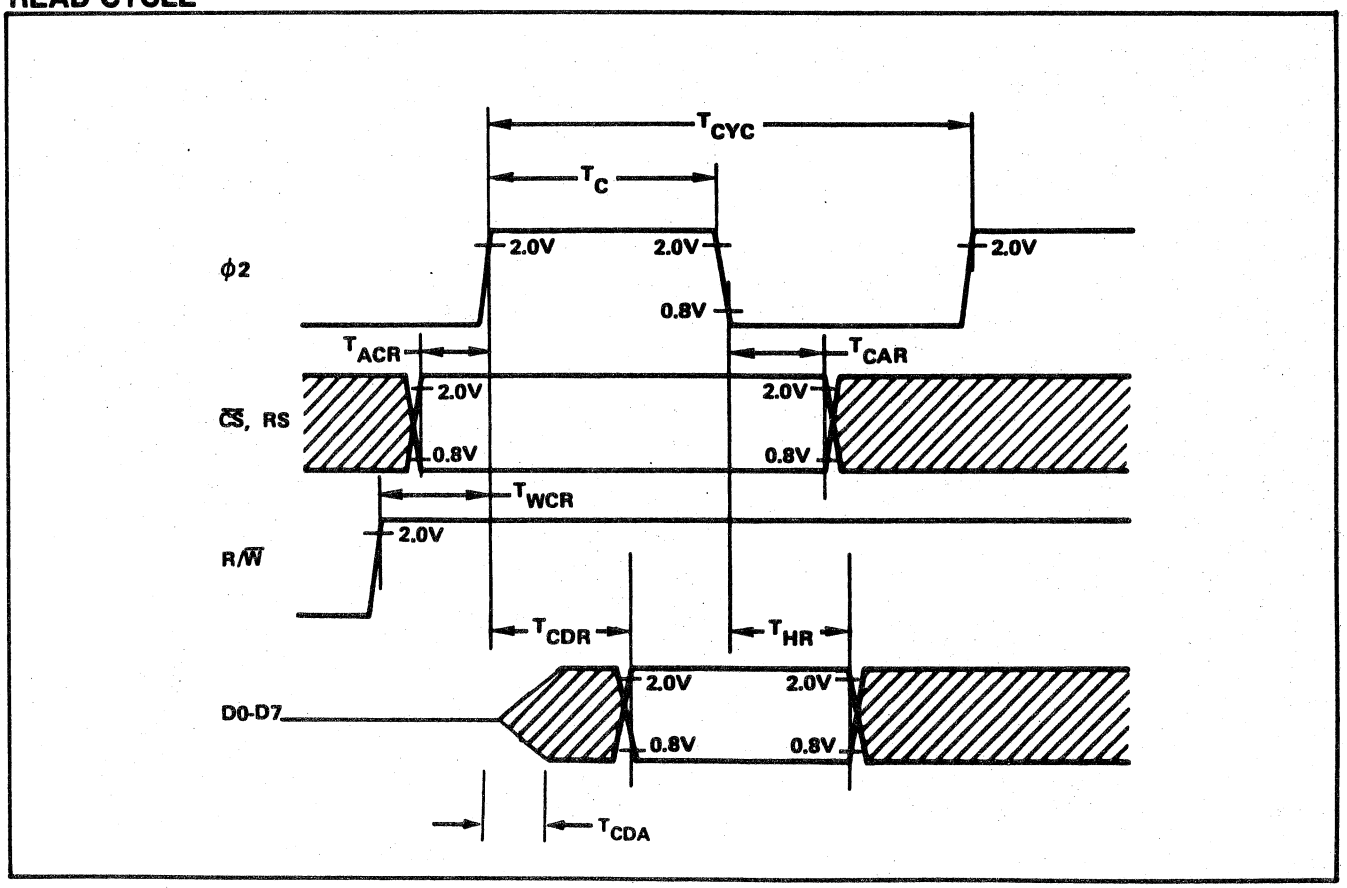
MPU READ TIMING CHARACTERISTICS

(V_{CC} = 5.0V ±5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristic	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Cycle Time	T_{CYC}	1.0	–	0.5	–	μs
Ø2 Pulse Width	T_C	440	–	200	–	ns
Address Set-Up Time	T_{ACR}	180	–	90	–	ns
Address Hold Time	T_{CAR}	0	–	0	–	ns
R/$\overline{W}$ Set-Up Time	T_{WCR}	180	–	90	–	ns
Read Access Time	T_{CDR}	–	340	–	150	ns
Read Hold Time	T_{HR}	10	–	10	–	ns
Data Bus Active Time (Invalid Data)	T_{CDA}	40	–	40	–	ns

(t_r and t_f = 10 to 30 ns)

READ CYCLE



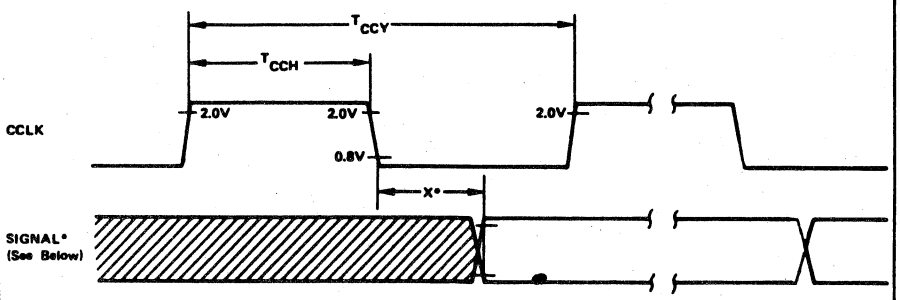
MEMORY AND VIDEO INTERFACE CHARACTERISTICS

(V_{CC} = 5.0V ±5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristics	Symbol	1 MHz		2 MHz		Units
		Min	Max	Min	Max	
Char. Clock Cycle Time	T_{CCY}	0.4	40	0.4	40	µs
Char. Clock Pulse Width	T_{CCH}	200	–	200	–	ns
MA0-MA13 Propagation Delay	T_{MAD}	–	300	–	300	ns
RA0-RA4 Propagation Delay	T_{RAD}	–	300	–	300	ns
DISPLAY ENABLE Prop. Delay	T_{DTD}	–	450	–	450	ns
HYSNC Propagation Delay	T_{HSD}	–	450	–	450	ns
VSYNC Propagation	T_{VSD}	–	450	–	450	ns
Cursor Propagation Delay	T_{CDD}	–	450	–	450	ns
LPEN Strobe Width	T_{LPH}	150	–	150	–	ns
LPEN to CCLK Delay	T_{LP1}	20	–	20	–	ns
CCLK to LPEN Delay	T_{LP2}	0	–	0	–	ns

t_r, t_f = 20 ns (max)

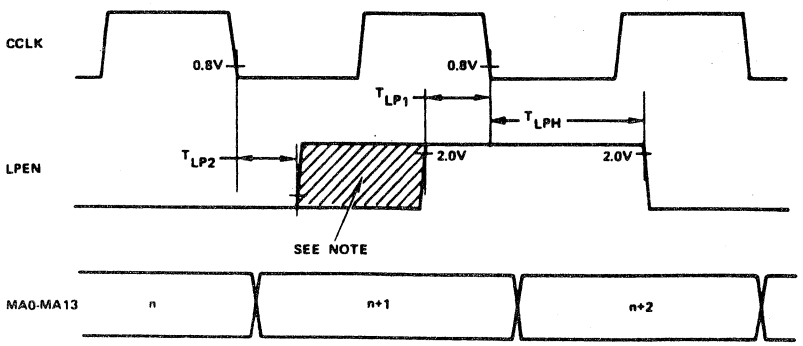
SYSTEM TIMING DEFINITIONS



*

SIGNAL	SIGNAL SYMBOL (X)
MA0-MA13	T_{MAD}
RA0-RA4	T_{RAD}
DISPLAY ENABLE	T_{DTD}
HSYNC	T_{HSD}
VSYNC	T_{VSD}
CURSOR	T_{CDD}

LIGHT PEN STROBE TIMING DEFINITIONS



NOTE:

SLASH AREA DEFINES THE "WINDOW" IN WHICH AN LPEN POSITIVE EDGE WILL CAUSE ADDRESS N+2 TO LOAD INTO LIGHT PEN REGISTER. TRANSITIONS ON EITHER SIDE OF THIS "WINDOW" WILL RESULT IN UNPREDICTABLE VALUES BEING LOADED INTO THE LIGHT PEN REGISTER.

SPECIFICATIONS

Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{IN}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_{OP}	0 to +70	°C
Storage Temperature	T_{STG}	-55 to 150	°C

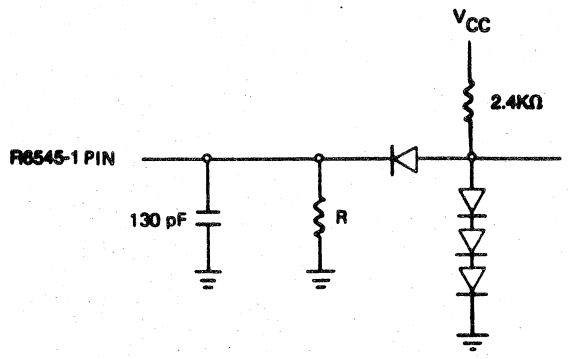
All inputs contain protection circuitry to prevent damage due to high static discharges. Care should be taken to prevent unnecessary application of voltages in excess of the allowable limits.

Electrical Characteristics

(V_{CC} = 5.0V ±5%, T_A = 0-70°C, unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	2.0	V_{CC}	Vdc
Input Low Voltage	V_{IL}	0.3	0.8	Vdc
Input Leakage (Ø2, R/$\overline{W}$, $\overline{RES}$, $\overline{CS}$, RS, LPEN, CCLK)	I_{IN}	–	2.5	µAdc
Three-State Input Leakage (D0-D7) (V_{IN} = 0.4 to 2.4V)	I_{TSI}	–	10.0	µAdc
Output High Voltage I_{LOAD} = 205 µAdc (D0-D7) I_{LOAD} = 100 µAdc (all others)	V_{OH}	2.4	–	Vdc
Output Low Voltage I_{LOAD} = 1.6 mAdc	V_{OL}	–	0.4	Vdc
Power Dissipation	P_D	–	1000	mW
Input Capacitance				
Ø2, R/$\overline{W}$, $\overline{RES}$, $\overline{CS}$, RS, LPEN, CCLK	C_{IN}	–	10.0	pF
D0-D7		–	12.5	pF
Output Capacitance	C_{OUT}	–	10.0	pF

TEST LOAD



R=11KΩ FOR D0-D7
=24KΩ FOR ALL OTHER OUTPUTS

PART NUMBER
R6551

Rockwell

R6500 Microcomputer System DATA SHEET

Asynchronous Communication Interface Adapter (ACIA)

The R6551 Asynchronous Communication Interface Adapter (ACIA) provides a program-controlled interface between 8-bit microprocessor-based systems and serial communication data sets and modems.

With its on-chip baud rate generator, the R6551 is capable of transmitting at 15 different program-selectable rates between 50 baud and 19,200 baud, and receiving at either the transmit rate or at 16 times an external clock rate. The R6551 has programmable word lengths of 5, 6, 7, or 8 bits; even, odd or no parity; 1, 1-1/2 or 2 stop bits.

With the R6551, a crystal is the only required external support component – eliminating the multiple-component support that is typically needed.

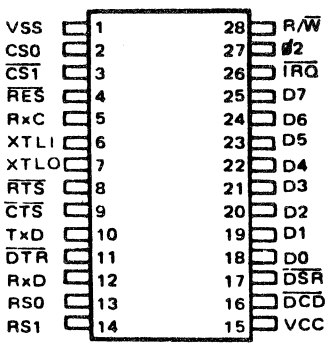
In addition, the R6551 is designed for maximum programmed control from the CPU, to simplify hardware implementation. A control register and a separate command register permit the CPU to easily select the R6551's operating modes and check data, parameters and status.

FEATURES

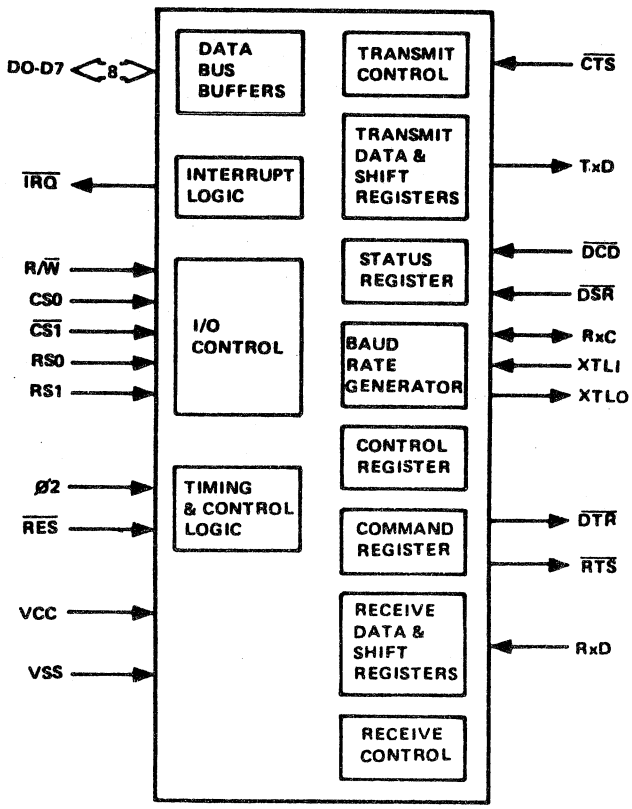
- Compatible with 8-bit microprocessors
- Full duplex or half duplex operation with buffered receiver and transmitter
- 15 programmable Baud Rates (50 to 19,200)
- Receiver data rate may be identical to baud rate or may be 16 times the external clock input
- Data set/modem control functions
- Programmable word lengths, number of stop bits, and parity bit generation and detection
- Programmable interrupt control
- Software reset
- Program-selectable serial echo mode
- Two chip selects
- 2 MHz or 1 MHz clock rate
- Single +5V ±5% power supply
- 28-pin plastic or ceramic DIP
- Full TTL compatibility

Ordering Information

Order Number	Package Type	Frequency	Temperature Range
R6551P	Plastic	1 MHz	0°C to +70°C
R6551AP	Plastic	2 MHz	0°C to +70°C
R6551C	Ceramic	1 MHz	0°C to +70°C
R6551AC	Ceramic	2 MHz	0°C to +70°C



R6551 Pin Configuration

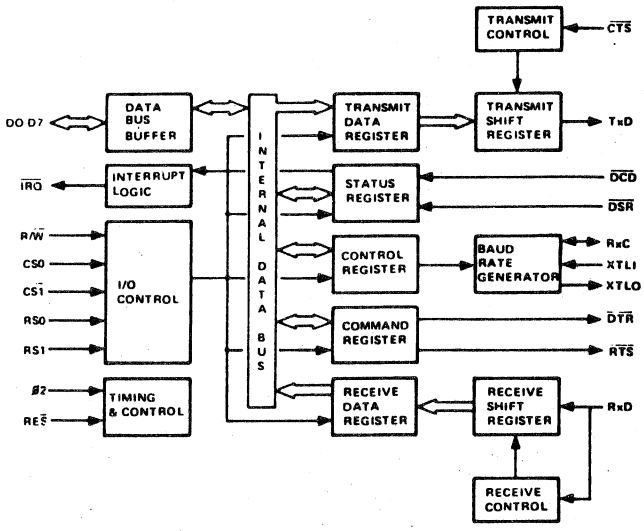


R6551 Interface Diagram

Asynchronous Communication Interface Adapter (ACIA)

Specifications subject to change without notice
Document No. 29000 D53
Rev. 1, January 1981

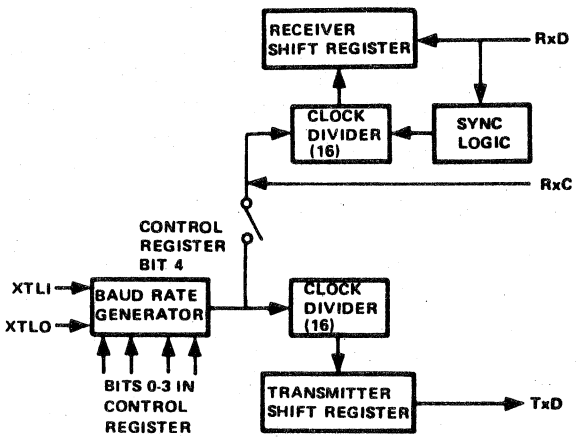
INTERNAL ORGANIZATION



R6551 Block Diagram

Transmitter/Receiver

Bits 0-3 of the Control Register select the divisor used to generate the baud rate for the Transmitter. If the Receiver clock is to use the same baud rate as the Transmitter, then RxC becomes an output pin and can be used to slave other circuits to the R6551.



Transmitter/Receiver Clock Circuits

Transmit and Receive Data Registers

These registers are used as temporary data storage for the 6551 Transmit and Receive circuits. The Transmit Data Register is characterized as follows:

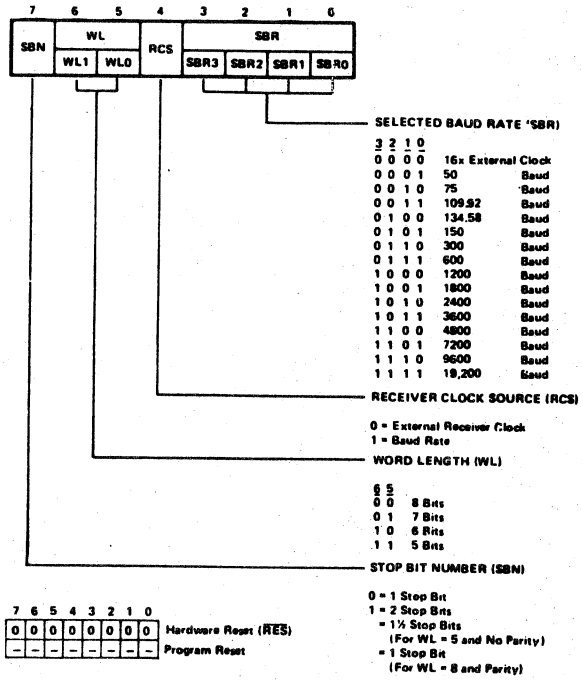
- Bit 0 is the leading bit to be transmitted.
- Unused data bits are the high-order bits and are "don't care" for transmission.

The Receive Data Register is characterized in a similar fashion:

- Bit 0 is the leading bit received.
- Unused data bits are the high-order bits and are "0" for the receiver.
- Parity bits are not contained in the Receive Data Register, but are stripped-off after being used for external parity checking. Parity and all unused high-order bits are "0".

Control Register

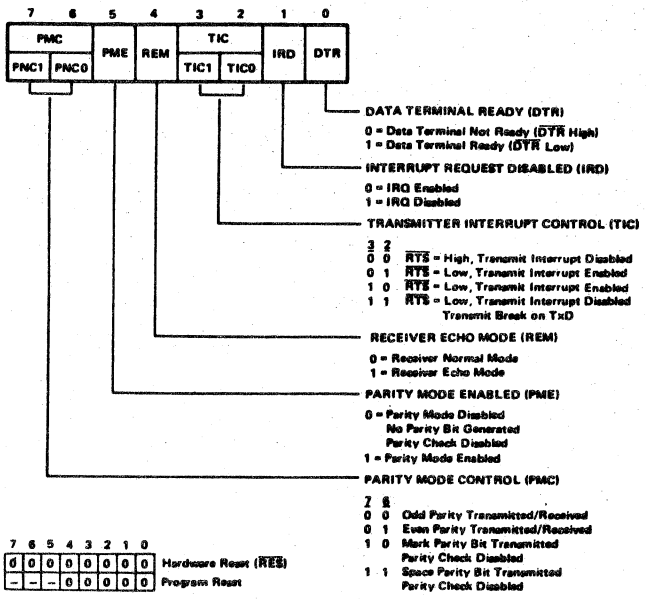
The Control Register selects the desired baud rate, frequency source, word length, and the number of stop bits.



R6551 Control Register

Command Register

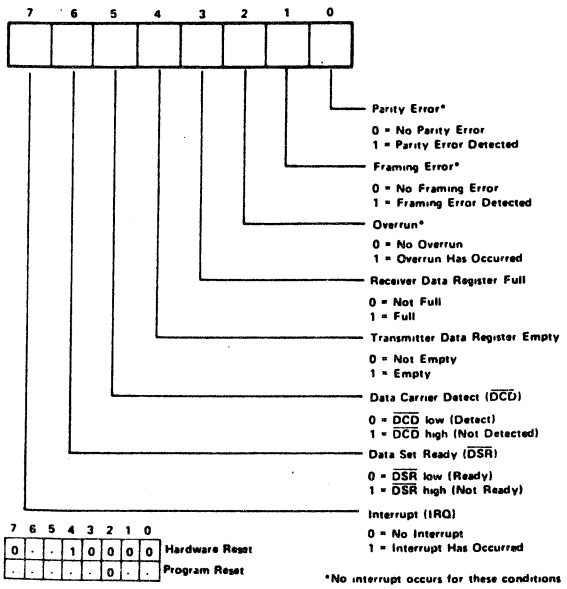
The Command Register controls specific modes and functions.



R6551 Command Register

Status Register

The Status Register reports the status of various R6551 functions



R6551 Status Register

INTERFACE SIGNAL DESCRIPTION

$\overline{RES}$ (Reset)

During system initialization a low on the $\overline{RES}$ input will cause internal registers to be cleared.

Ø2 (Input Clock)

The input clock is the system Ø2 clock and is used to synchronize all data transfers between the system microprocessor and the R6551.

R/$\overline{W}$ (Read/Write)

The R/$\overline{W}$ is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the R6551. A low on the R/$\overline{W}$ pin allows a write to the R6551.

$\overline{IRQ}$ (Interrupt Request)

The $\overline{IRQ}$ pin is an interrupt output from the interrupt control logic. It is an open drain output, permitting several devices to be connected to the common $\overline{IRQ}$ microprocessor input. Normally a high level, $\overline{IRQ}$ goes low when an interrupt occurs.

D0-D7 (Data Bus)

The D0-D7 pins are the eight data lines used to transfer data between the processor and the R6551. These lines are bi-directional and are normally high-impedance, except during Read cycles when the R6551 is selected.

CS0, $\overline{CS1}$ (Chip Selects)

The two chip select inputs are normally connected to the processor address lines either directly or through decoders. The R6551 is selected when CS0 is high and $\overline{CS1}$ is low.

RS0, RS1 (Register Selects)

The two register select lines are normally connected to the processor address lines to allow the processor to select the various R6551 internal registers. The following table indicates the internal register select coding:

RS1	RS0	Write	Read
0	0	Transmit Data Register	Receiver Data Register
0	1	Programmed Reset (Data is "Don't Care")	Status Register
1	0	Command Register	
1	1	Control Register	

Note that only the Command and Control registers are read/write. The Programmed Reset operation does not cause any data transfer, but is used to clear Bits 0 through 4 in the Command Register and Bit 2 in the Status Register. The Programmed Reset is slightly different from the Hardware Reset ($\overline{RES}$); these differences are described in the individual register definitions.

ACIA/Modem Interface Signal Description

XTLI, XTLO (Crystal Pins)

These pins are normally directly connected to the external crystal (1.8432 MHz) used to derive the various baud rates. Alternatively, an externally generated clock may be used to drive the XTLI pin, in which case the XTLO pin must float. XTLI is the input pin for the transmit clock.

TxD (Transmit Data)

The TxD output line is used to transfer serial NRZ (non-return-to-zero) data to the modem. The LSB (least significant bit) of the Transmit Data Register is the first data bit transmitted and the rate of data transmission is determined by the baud rate selected, or under control of an external clock (as selected by the Control Register).

RxD (Receive Data)

The RxD input line is used to transfer serial NRZ data into the ACIA from the modem, LSB first. The receiver data rate is either the programmed baud rate or the rate of an externally generated receiver clock (as selected by the Control Register).

RxC (Receive Clock)

The RxC is a bi-directional pin which serves as either the receiver 16x clock input or the receiver 16x clock output. The latter mode results if the internal baud rate generator is selected for receiver data clocking.

$\overline{RTS}$ (Request to Send)

The $\overline{RTS}$ output pin is used to control the modem from the processor. The state of the $\overline{RTS}$ pin is determined by the contents of the Command Register.

$\overline{CTS}$ (Clear to Send)

The $\overline{CTS}$ input pin is used to control the transmitter operation. The enable state is with $\overline{CTS}$ low. The transmitter is automatically disabled if $\overline{CTS}$ is high.

$\overline{DTR}$ (Data Terminal Ready)

This output pin is used to indicate the status of the R6551 to the modem. A low on $\overline{DTR}$ indicates the R6551 is enabled and a high indicates it is disabled. The processor controls this pin via bit 0 of the Command Register.

$\overline{DSR}$ (Data Set Ready)

The $\overline{DSR}$ input pin is used to indicate to the R6551 the status of the modem. A low indicates the "ready" state and a high, "not-ready". $\overline{DSR}$ is a high-impedance input, and must be connected. If unused, it should be driven high or low, but not switched.

$\overline{DCD}$ (Data Carrier Detect)

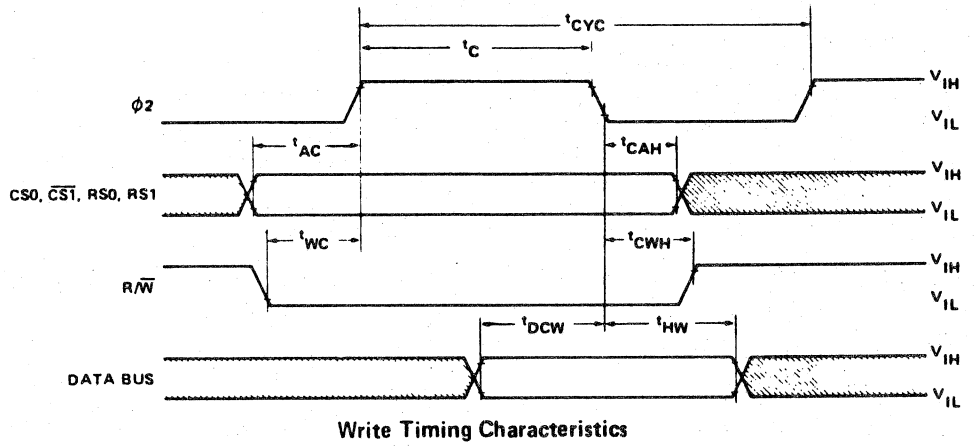
The $\overline{DCD}$ input pin is used to indicate to the R6551 the status of the carrier-detect output of the modem. A low indicates that the modem carrier signal is present and a high, that it is not. Like $\overline{DSR}$, $\overline{DCD}$ is a high-impedance input, and must be connected.

READ/WRITE CYCLE CHARACTERISTICS

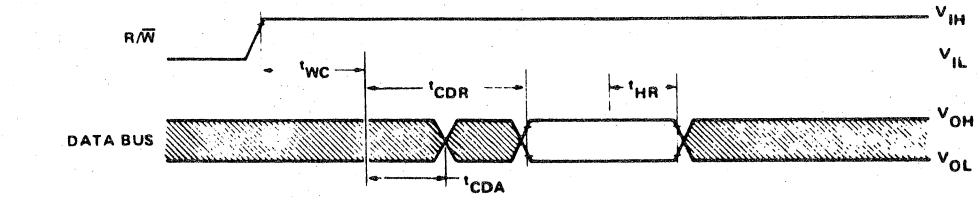
(V_{CC} = 5.0V ±5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristic	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Cycle Time	t_{CYC}	1.0	40	0.5	40	µs
Ø2 Pulse Width	t_C	400	–	200	–	ns
Address Set-Up Time	t_{AC}	120	–	70	–	ns
Address Hold Time	t_{CAH}	0	–	0	–	ns
R/$\overline{W}$ Set-Up Time	t_{WC}	120	–	70	–	ns
R/$\overline{W}$ Hold Time	t_{CWH}	0	–	0	–	ns
Data Bus Set-Up Time	t_{DCW}	150	–	60	–	ns
Data Bus Hold Time	t_{HW}	20	–	20	–	ns
Read Access Time (Valid Data)	t_{CDR}	–	200	–	150	ns
Read Hold Time	t_{HR}	20	–	20	–	ns
Bus Active Time (Invalid Data)	t_{CDA}	40	–	40	–	ns

(t_r and t_f = 10 to 30 ns)



Write Timing Characteristics



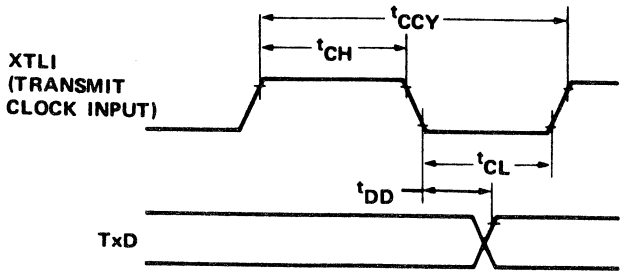
Read Timing Characteristics

TRANSMIT/RECEIVE CHARACTERISTICS

Characteristic	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Transmit/Receive Clock Rate	t_{CCY}	400*	–	400*	–	ns
Transmit/Receive Clock High Time	t_{CH}	175	–	175	–	ns
Transmit/Receive Clock Low Time	t_{CL}	175	–	175	–	ns
XTLI to TxD Propagation Delay	t_{DD}	–	500	–	500	ns
$\overline{RTS}$ Propagation Delay	t_{DLY}	–	500	–	500	ns
$\overline{IRQ}$ Propagation Delay (Clear)	t_{IRQ}	–	500	–	500	ns

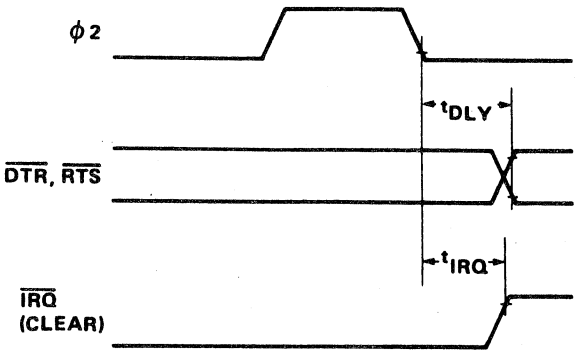
(t_r, t_f = 10 to 30 ns)

The baud rate with external clocking is: Baud Rate = $\frac{1}{16 \times T_{CCY}}$

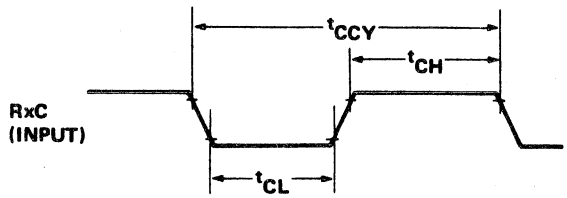


NOTE: TxD rate is 1/16 TxC rate

Transmit Timing with External Clock



Interrupt and Output Timing

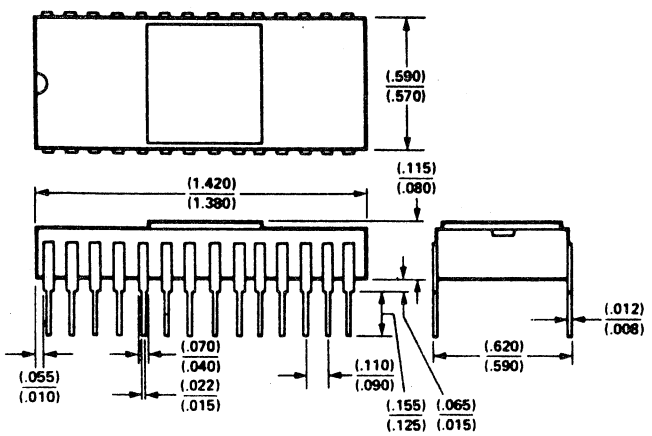


NOTE: RxD rate is 1/16 RxC rate

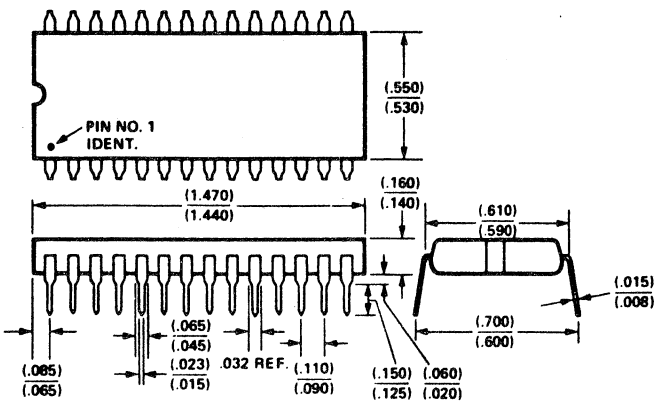
Receive External Clock Timing

PACKAGE OUTLINES

28 LEAD CERAMIC



28 LEAD PLASTIC



PRELIMINARY

8048H/8048H-1/8035HL/8035HL-1
HMOS SINGLE COMPONENT 8-BIT MICROCOMPUTER

- **8048H/8048H-1 Mask Programmable ROM**
- **8035HL/8035HL-1 CPU Only with Power Down Mode**

- **8-BIT CPU, ROM, RAM, I/O in Single Package**
- **High Performance HMOS**
- **Reduced Power Consumption**
- **1.4 usec and 1.9 usec Cycle Versions All Instructions 1 or 2 Cycles.**
- **Over 90 Instructions: 70% Single Byte**
- **1K x 8 ROM 64 x 8 RAM 27 I/O Lines**
- **Interval Timer/Event Counter**
- **Easily Expandable Memory and I/O**
- **Compatible with 8080/8085 Series Peripherals**
- **Two Single Level Interrupts**

The Intel® 8048H/8048H-1/8035HL/8035HL-1 are totally self-sufficient, 8-bit parallel computers fabricated on single silicon chips using Intel's advanced N-channel silicon gate HMOS process.

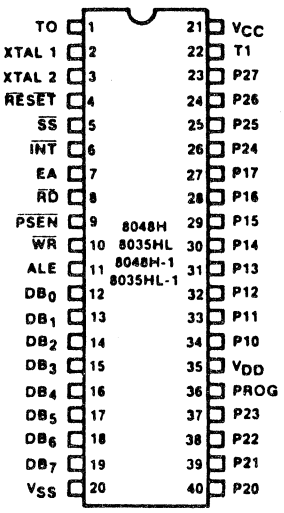
The 8048H contains a 1K X 8 program memory, a 64 X 8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to on-board oscillator and clock circuits. For systems that require extra capability the 8048H can be expanded using standard memories and MCS-80™/MCS-85™ peripherals. The 8035HL is the equivalent of the 8048H without program memory and can be used with external ROM AND RAM.

To reduce development problems to a minimum and provide maximum flexibility, a logically and functionally pin compatible version of the 8048H with UV-erasable user-programmable EPROM program memory is available. The 8748 will emulate the 8048H up to 6 MHz clock frequency with minor differences.

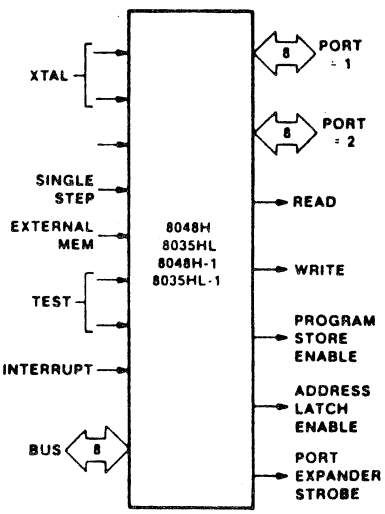
The 8048H is fully compatible with the 8048 when operated at 6 MHz.

These microcomputers are designed to be efficient controllers as well as arithmetic processors. They have extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single bit instructions and no instructions over 2 bytes in length.

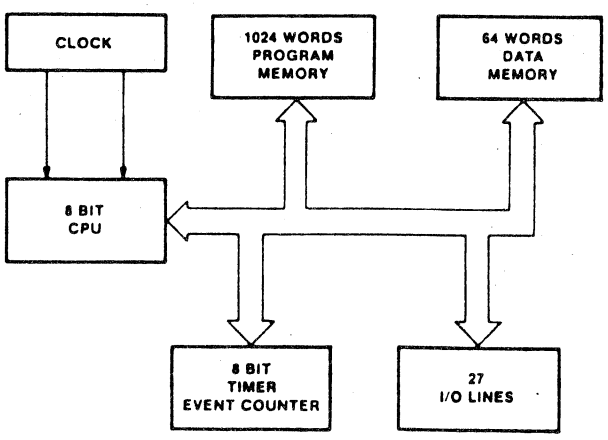
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN DESCRIPTION

Designation	Pin #	Function
V_{SS}	20	Circuit GND potential
V_{DD}	26	Low power standby pin
V_{CC}	40	Main power supply; +5V during operation.
PROG	25	Output strobe for 8243 I/O expander.
P10-P17 Port 1	27-34	8-bit quasi-bidirectional port.
P20-27 Port 2	21-24	8-bit quasi-bidirectional port.
	35-38	P20-P23 contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for 8243.
DB0-DB7 BUS	12-19	True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched.
		Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of $\overline{PSEN}$. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$, and $\overline{WR}$.
T0	1	Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 can be designated as a clock output using ENT0 CLK instruction.
T1	39	Input pin testable using the JT1, and JNT1 instructions. Can be designated the timer/counter input using the STRT CNT instruction.
$\overline{INT}$	6	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active low)
$\overline{RD}$	8	Output strobe activated during a BUS read. Can be used to enable data onto the bus from an external device.
		Used as a read strobe to external data memory. (Active low)
$\overline{RESET}$	4	Input which is used to initialize the processor. (Active low) (Non TTL V_{IH})
$\overline{WR}$	10	Output strobe during a bus write. (Active low)
		Used as write strobe to external data memory.
ALE	11	Address latch enable. This signal occurs once during each cycle and is useful as a clock output.
		The negative edge of ALE strobes address into external data and program memory.
$\overline{PSEN}$	9	Program store enable. This output occurs only during a fetch to external program memory. (Active low)
$\overline{SS}$	5	Single step input can be used in conjunction with ALE to "single step" the processor through each instruction. (Active low)
EA	7	External access input which forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification. (Active high)
XTAL1	2	One side of crystal input for internal oscillator. Also input for external source. (Non TTL V_{IH})
XTAL2	3	Other side of crystal input.

INSTRUCTION SET

Accumulator

Mnemonic	Description	Bytes	Cycles
ADD A, R	Add register to A	1	1
ADD A, @R	Add data memory to A	1	1
ADD A, # data	Add immediate to A	2	2
ADDC A, R	Add register with carry	1	1
ADDC A, @R•	Add data memory with carry	1	1
ADDC A, # data	Add immediate with carry	2	2
ANL A, R	And register to A	1	1
ANL A, @R	And data memory to A	1	1
ANL A, # data	And immediate to A	2	2
ORL A, R	Or register to A	1	1
ORL A @R	Or data memory to A	1	1
ORL A, # data	Or immediate to A	2	2
XRL A, R	Exclusive or register to A	1	1
XRL A, @R	Exclusive or data memory to A	1	1
XRL, A, # data	Exclusive or immediate to A	2	2
INC A	Increment A	1	1
DEC A	Decrement A	1	1
CLR A	Clear A	1	1
CPL A	Complement A	1	1
DA A	Decimal adjust A	1	1
SWAP A	Swap nibbles of A	1	1
RL A	Rotate A left	1	1
RLC A	Rotate A left through carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through carry	1	1

Input/Output

Mnemonic	Description	Bytes	Cycles
IN A, P	Input port to A	1	2
OUTL P, A	Output A to port	1	2
ANL P, # data	And immediate to port	2	2
ORL P, # data	Or immediate to port	2	2
INS A, BUS	Input BUS to A	1	2
OUTL BUS, A	Output A to BUS	1	2
ANL BUS, # data	And immediate to BUS	2	2
ORL BUS, # data	Or immediate to BUS	2	2
MOVD A,P	Input expander port to A	1	2
MOVD P, A	Output A to expander port	1	2
ANLD P, A	And A to expander port	1	2
ORLD P, A	Or A to expander port	1	2

Registers

Mnemonic	Description	Bytes	Cycles
INC R	Increment register	1	1
INC @R	Increment data memory	1	1
DEC R	Decrement register	1	1

Branch

Mnemonic	Description	Bytes	Cycles
JMP addr	Jump unconditional	2	2
JMPP @A	Jump indirect	1	2
DJNZ R, addr	Decrement register and skip	2	2
JC addr	Jump on carry = 1	2	2
JNC addr	Jump on carry = 0	2	2
JZ addr	Jump on A zero	2	2
JNZ addr	Jump on A not zero	2	2
JTO addr	Jump on TO = 1	2	2
JNTO addr	Jump on TO = 0	2	2
JT1 addr	Jump on T1 = 1	2	2
JNT1 addr	Jump on T1 = 0	2	2
JF0 addr	Jump on F0 = 1	2	2
JF1 addr	Jump on F1 = 1	2	2
JTF addr	Jump on timer flag	2	2
JN1 addr	Jump on INT = 0	2	2
JBb addr	Jump on accumulator bit	2	2

Subroutine

Mnemonic	Description	Bytes	Cycles
CALL addr	Jump to subroutine	2	2
RETR	Return	1	2
RETR	Return and restore status	1	2

Flags

Mnemonic	Description	Bytes	Cycles
CLR C	Clear carry	1	1
CPL C	Complement carry	1	1
CLR F0	CLear flag 0	1	1
CPL F0	Complement flag 0	1	1
CLR F1	Clear flag 1	1	1
CPL F1	Complement flag 1	1	1

Data Moves

Mnemonic	Description	Bytes	Cycles
MOV A, R	Move register to A	1	1
MOV A, @R	Move data memory to A	1	1
MOV A, # data	Move immediate to A	2	2
MOV R, A	Move A to register	1	1
MOV @R, A	Move A to data memory	1	1
MOV R, # data	Move immediate to register	2	2
MOV @R, #data	Move immediate to data memory	2	2
MOV A, PSW	Move PSW to A	1	1
MOV PSW, A	Move A to PSW	1	1
XCH A, R	Exchange A and register	1	1
XCH A, @R	Exchange A and data memory	1	1
XCHD A, @R	Exchange nibble of A and register	1	
MOVX A, @R	Move external data memory to A	1	2
MOVX @R, A	Move A to external data memory	1	2
MOVP A, @A	Move to A from current page	1	2
MOVP3 A, @	Move to A from page 3	1	2

Timer/Counter

Mnemonic	Description	Bytes	Cycles
MOV A, T	Read timer/counter	1	1
MOV T, A	Load timer/counter	1	1
STRT T	Start timer	1	1
STRT CNT	Start counter	1	1
STOP TCNT	Stop timer/counter	1	1
EN TCNT1	Enable timer/counter interrupt	1	1
DIS TCNT1	Disable timer/counter interrupt	1	1

Control

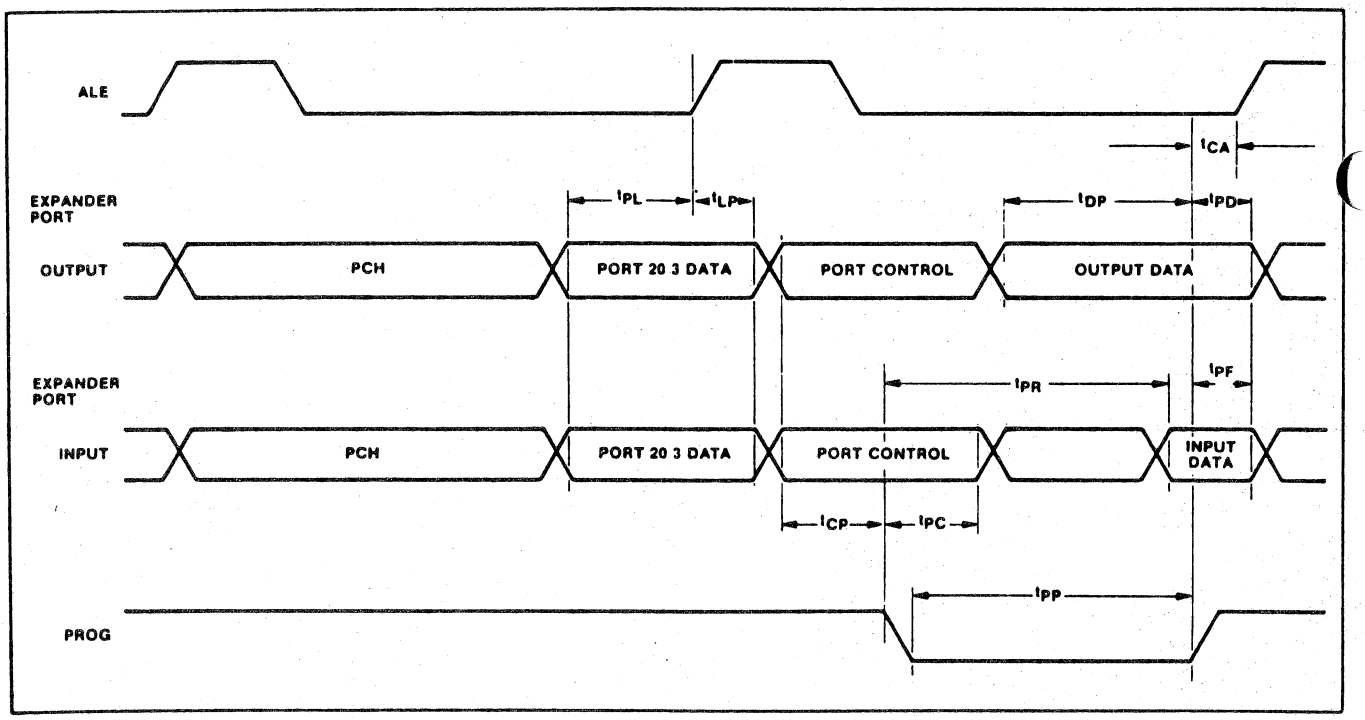
Mnemonic	Description	Bytes	Cycles
EN 1	Enable external interrupt	1	1
DIS 1	Disable external interrupt	1	1
SEL RB0	Select register bank 0	1	1
SEL RB1	Select register bank 1	1	1
SEL MB0	Select memory bank 0	1	1
SEL MB1	Select memory bank 1	1	1
ENT 0 CLK	Enable clock output on T0	1	1

Mnemonic	Description	Bytes	Cycles
NOP	No operation	1	1

A.C. CHARACTERISTICS (PORT 2 TIMING) TA = 0°C to 70°C, VCC = 5V ± 10%, VSS = 0V

Symbol	Parameter	8048H 8035HL				8048H-1 8035HL-1		Unit
		6 MHz		8 MHz		11 MHz		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CP}	Port control Setup Before Falling Edge of PROG.	110		105				ns
t_{PC}	Port Control Hold After Falling Edge of PROG.	100		90				ns
t_{PR}	PROG to Time P2 Input Must Be Valid		810		700		650	ns
t_{PF}	Input Data Hold Time	0	150	0	150	0	150	ns
t_{DP}	Output Data Setup Time	250		210		200		ns
t_{PD}	Output Data Hold Time	65		35		20		ns
t_{PP}	PROG Pulse Width	1200		970		700		ns
t_{PL}	Port 2 I/O Data Setup	350		300		250		ns
t_{LP}	Port 2 I/O Data Hold	150		65		20		ns

PORT 2 TIMING



BUS TIMING AS A FUNCTION OF TCY *

SYMBOL	FUNCTION OF TCY		
T_{LL}	7/30	T_{CY}	MIN
T_{AL}	1/10	T_{CY}	MIN
T_{LA}	1/15	T_{CY}	MIN
T_{CC} (1)	1/2	T_{CY}	MIN
T_{CC} (2)	2/5	T_{CY}	MIN
T_{DW}	2/15	T_{CY}	MIN
T_{WD}	1/15	T_{CY}	MIN
T_{DR}	0		MIN

T_{CC} (1) : $\overline{RD}/\overline{WR}$
T_{CC} (2) : $\overline{PSEN}$

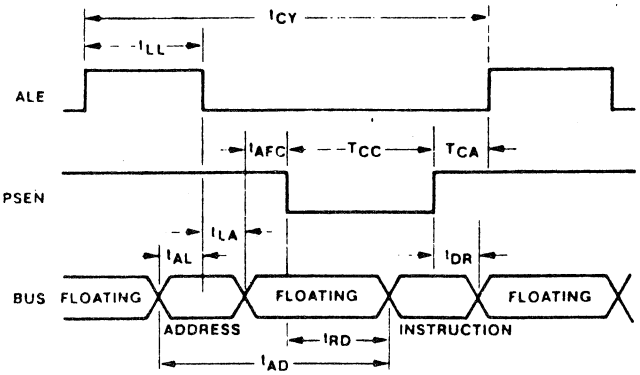
SYMBOL	FUNCTION OF TCY		
T_{RD} (1)	11/30	T_{CY}	MAX
T_{RD} (2)	3/10	T_{CY}	MAX
T_{AW}	3/10	T_{CY}	MIN
T_{AD} (1)	1/2	T_{CY}	MAX
T_{AD} (2)	1/3	T_{CY}	MAX
T_{AFC}	1/30	T_{CY}	MIN
T_{CA}	1/15	T_{CY}	MIN

T_{RD} (1) : $\overline{RD}$
T_{RD} (2) : $\overline{PSEN}$

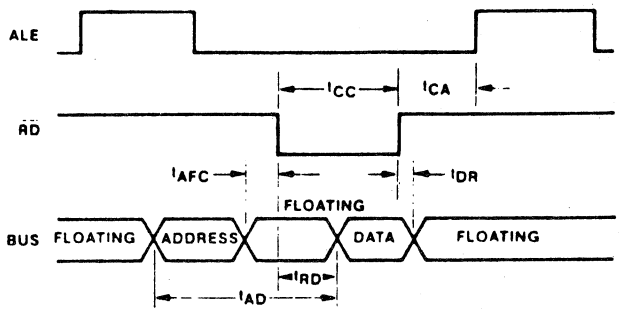
T_{AD} (1) : $\overline{RD}$
T_{AD} (2) : $\overline{PSEN}$

* APPROXIMATE VALUES NOT INCLUDING GATE DELAYS.

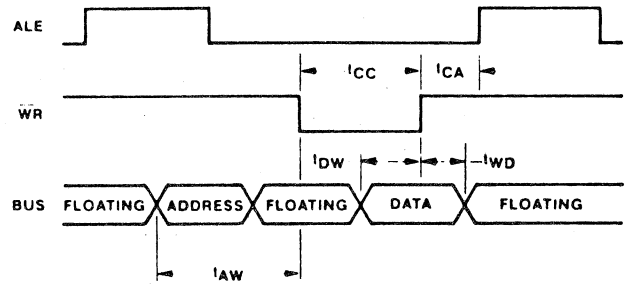
WAVEFORMS



Instruction Fetch From External Program Memory



Read From External Data Memory



Write to External Data Memory

Input and Output for A.C.Tests.

A.C. CHARACTERISTICS TA = 0°C to 70°C VCC = VDD = 5V ± 10%, VSS = 0V

Symbol	Parameter	8048H 8035HL				8048H-1 8035HL-1		Unit	Conditions (Note 1)
		6 MHz		8 MHz		11 MHz			
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{LL}	ALE Pulse Width	400		270		150		ns	
t_{AL}	Address Setup to ALE	75		75		70		ns	
t_{LA}	Address Hold from ALE	65		65		50		ns	
t_{CC}	Control Pulse Width ($\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$)	700		490		300		ns	
t_{DW}	Data Setup before $\overline{WR}$	370		370		280		ns	
t_{WD}	Data Hold after $\overline{WR}$	80		80		40		ns	CL = 20pF (NOTE 2)
t_{CY}	Cycle Time	2.5		1.875		1.36		μs	
t_{DR}	Data Hold	0	200	0	150	0	100	ns	
t_{RD}	$\overline{PSEN}$, $\overline{RD}$ to Data In		500		340		200	ns	
t_{AW}	Address Setup to $\overline{WR}$	230		210		200		ns	
t_{AD}	Address Setup to Data In		950		650		400	ns	
t_{AFC}	Address Float to $\overline{RD}$, $\overline{PSEN}$	0		0		-1		ns	
t_{CA}	Control Pulse to ALE	10		10		0		ns	

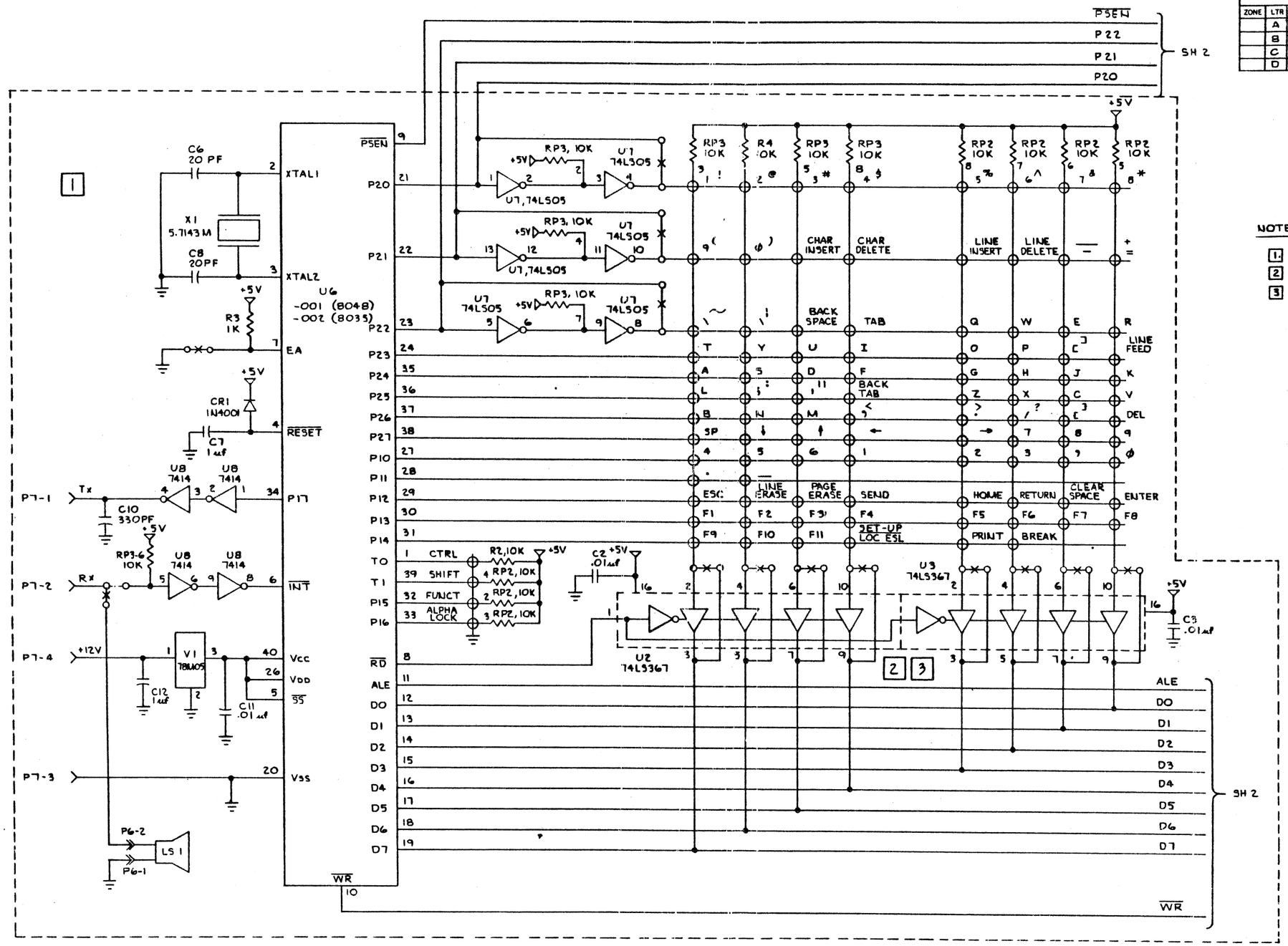
NOTE 1: Control outputs CL = 80 pF
BUS outputs CL = 150 pF

NOTE 2: BUS High Impedance Load: 20 pF

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	PROD REL PER ECO 42		
	B	" " ECO 43		
	C	" " ECO 44		
	D	" " ECO 46		

NOTES:- UNLESS OTHERWISE SPECIFIED

1. VERSION -001 AND -002
2. VERSION -002 ONLY
3. CIRCUITRY OPTIONAL



B6000003-001

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	DWN Carlos Alonso 10-1-80
NEXT ASSY	USED ON		CHK J. Cameron 10-2-80
		ANG ± PLC .3 PLC	ENGR
		SCALE NONE	APPD
		MATERIAL	FINISH

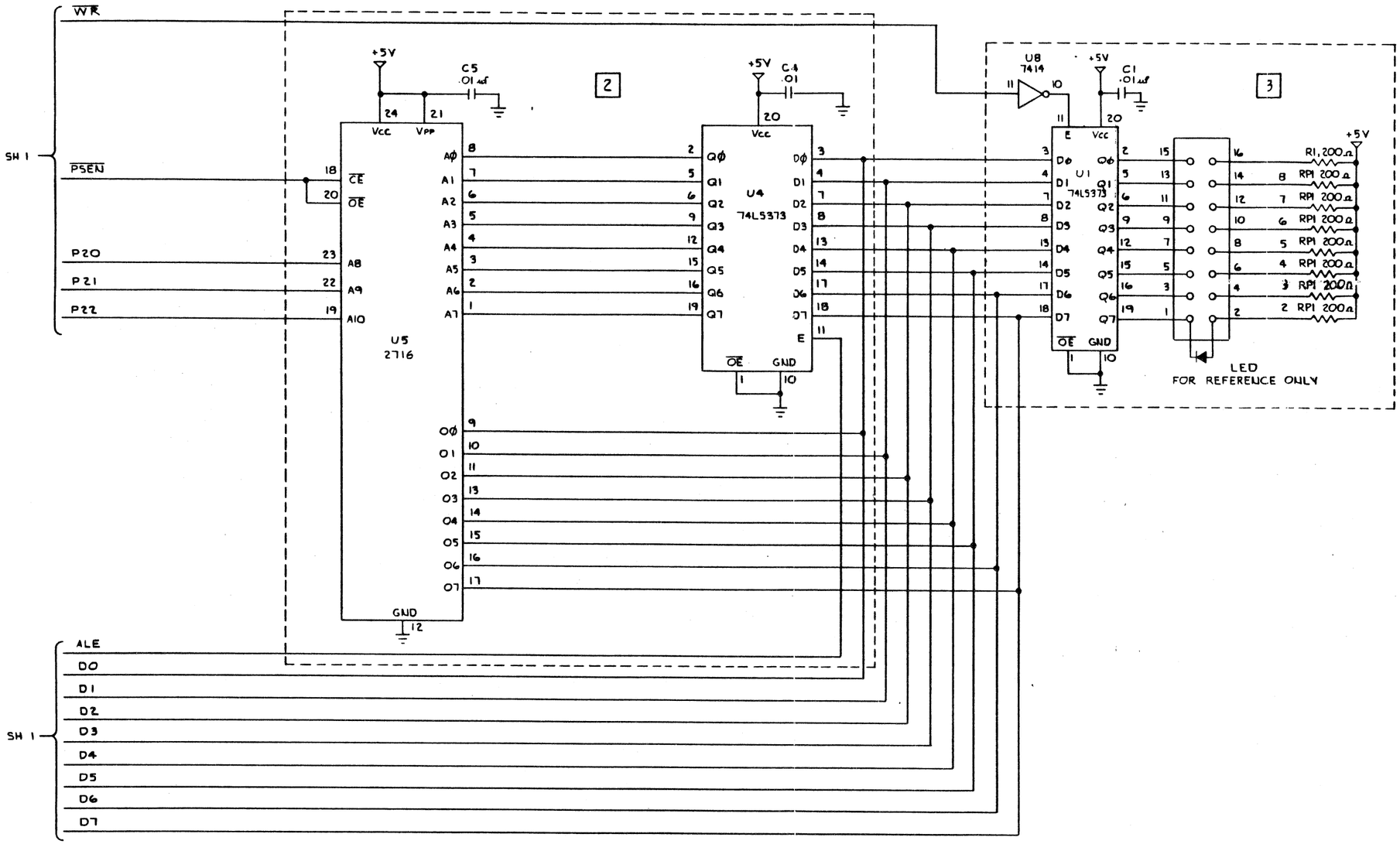
TeleVideo, Inc.

TITLE PCB SCHEMATICS 950 KEYBOARD

SIZE D | SHT 1 OF 2 | DRAWING NO 2010300 | REV D

2010300-00

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	D	SEE SHT 1		



APPLICATION		UNLESS OTHERWISE NOTED	DWN caballero 10-2-80	TeleVideo, Inc.
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK caballero 10-2-80	
		ANG ± 2 PLC ± 3 PLC ±	ENGR	TITLE PCB SCHEMATIC 950 KEYBOARD
			APPD	
		SCALE NONE	APPD	
		MATERIAL	FINISH	SIZE D SHT 1 OF 2 DRAWING NO 2010300 REV

2010300-00

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	PROD REL PER ECO 40		
	A1	" " ECO 45		
	B	" " ECO 41, 47		
	B1	" " ECO 54		
	B2	" " ECO 70, 82	9/21/81	
	B3	" " ECO 0138, 0442	9/15/82	

A69 74LS04 — A70 74LS00 — A63 74LS32 — A58 74LS32 — A62 74LS139 — A53 6502A — A42 2716/2332 — A41 2332/2564 — A52 2332

E20 E18 E17 E15 E14 E19 E16 E22 E23 E26 E21 E27 E28

R24 1K R23 1K R39 3.3K R45 9.3K R46, 3.3K

SH 5,7 IRQ — SH 7 NMI — SH 6 Φ0 — SH 6 RESET

DISP. MEM. — TOP. SEL. — SH 2,6 — SH 2,5,6,7

SCREG SEL — SH 4

AB0 SH 2,5,7
AB1 SH 2,5,7
AB2 SH 2,7
AB3 SH 2,7
AB4 – AB8 SH 2
AB9 – AB11 SH 2,5
AB12 SH 2,5
AB13 SH 2
AB14 – AB15 SH 2,6,7

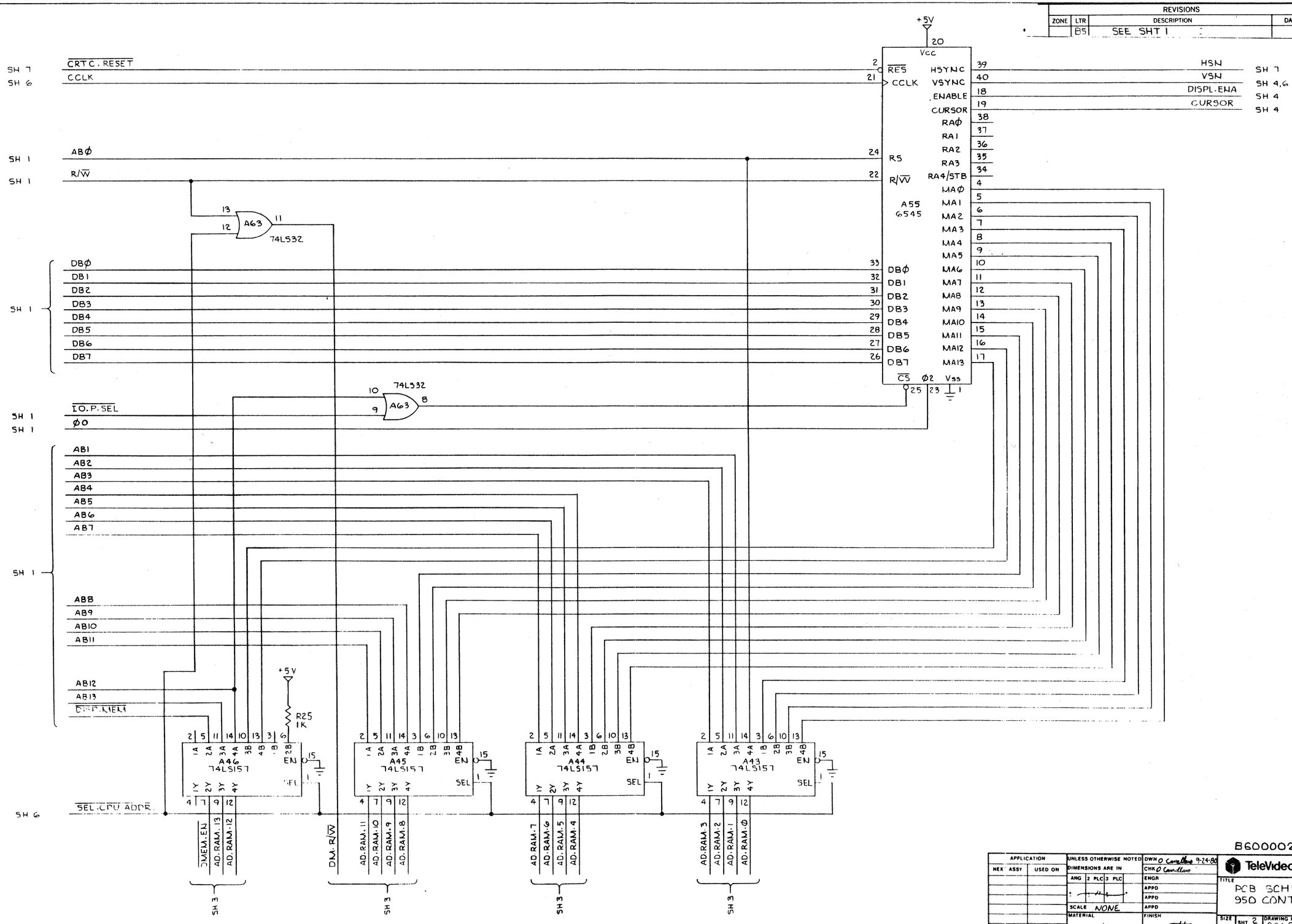
R/W SH 2,3,5,7
Φ0 SH 2,5,7
DB0 – DB7 SH 2,3,5,7

P8-1 P8-2 P8-3 P8-8 P8-7

B5	PROD REL PER ECO 0483	
B4	PROD REL PER ECO 0475	

APPLICATION		DWN O. Caballero 9-25-80	TeleVideo, Inc.
NEXT ASSY	USED ON	CHK O. Caballero 9-25-80	
UNLESS OTHERWISE NOTED DIMENSIONS ARE IN		ENGR T. Tully 9/1/82	TITLE: PCB SCHEMATIC 950 CONT. BD
ANG	2 PLC 3 PLC	APPD	
SCALE NONE		APPD	
MATERIAL		APPD	
FINISH		SIZE	SHT 1 OF 7
		DRAWING NO 7009800	REV B5

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B5	SEE SHT 1		



B600002-001

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN ANG ± 2 PLC ± 3 PLC	DWN O Carrillo 9-24-80 CHK O Carrillo ENGR APPD APPD APPD	TeleVideo, Inc.
NEXT ASSY	USED ON	SCALE NONE	MATERIAL	FINISH

TITLE: PCB SCHEMATIC 950 CONT. BD

SIZE | SHT 2 OF 7 | DRAWING NO 2002800 | REV B5

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B5	SEE SHT 1		

A15 74LS42

2 ADRAM 13 — 13 C
SH 2 AD.RAM.11 — 15 A
SH 2 AD.RAM.12 — 14 B
SH 6 QC.CLK — 12 D
3 1 8 9 6 7 5 6 4 5

A8 74LS04

A16 74LS32

A16 74LS32

SH 2 AD.RAM.10, AD.RAM.9, AD.RAM.8, AD.RAM.7, AD.RAM.6, AD.RAM.5, AD.RAM.4, AD.RAM.3, AD.RAM.2, AD.RAM.1, AD.RAM.Ø

A25 2114 — A26 2114 — A27 2114 — A28 2114

A34 6116 — A35 6116 — A36 6116 — A37 6116

SH 2 DM.R/W

SH 1 DB.7, DB.6, DB.5, DB.4, DB.3, DB.2, DB.1, DB.Ø

A14 8T245

SH 4 CH.AD.7, CH.AD.6, CH.AD.5, CH.AD.4, CH.AD.3, CH.AD.2, CH.AD.1, CH.AD.Ø

SH 2 DMEN.EN

SH 1 R/W

B600002-001

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	DWN: O Cavallero 9-25-80	TeleVideo, Inc.
NEXT ASSY	USED ON	ANG ± 2 PLC ± 3 PLC	CHK O Cavallero 9-25-80	TITLE: PCB SCHEMATIC 950 CONT. BD.
			ENGR	
			APPD	
		SCALE NONE	APPD	
		MATERIAL	FINISH	SIZE — SHT 3 OF 7 — DRAWING NO 2003800 — REV 85

REVISIONS			
ZONE	LTR	DESCRIPTION	DATE
	B5	SEE SHT 1	

SH 3 CH·AD·7 CH·AD·6 CH·AD·5 CH·AD·4 CH·AD·3 CH·AD·2 CH·AD·1 CH·AD·Ø

SH 7 CRTC·RES HSN

SH 1 SCREG SEL. DB4 DB5 DB6 DB7

A61 74LS174 A60 74LS191 A24 74LS374 A32 2332 A33 2332 A22 74LS166 A23 74LS166 A21 74S174 A31 74LS74 A20 74LS157 A19 74LS174 A18 74LS173

R38 1K R14 1K R16 1K R17 1K R18 1K R19 1K R20 1K R15 1K C75 100 pf

SH 6 SHIFT.CLK DC CARRY

SH 2 VSN

DC CARRY SH 6 CURSOR SH 2

RAØ RA3 SH 6

DOT SERIAL SH 6

DEL.DISPL.ENA DISPL.EN

SH 6 SHIFT·CLK ROW 9 DISPL.ENA VSYNC (VSN)

UNDERLINE REVERSE·VIDEO BLINK BLANK DEL.DISPL.EN– HALF·INTENSITY SH 6

P10-1

DEL CURSOR SH 6

ROW·9 SH6 DISPL·EN– SH4

B600002-001

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	DWN O. Carrillo 9-25-80	TeleVideo, Inc.
NEXT ASSY	USED ON	ANG 2 PLC 3 PLC	CHK O. Carrillo 9-	TITLE: FCB SCHEMATIC 950 CONT. BD.
			ENGR	
		SCALE NONE	APPD	
		MATERIAL	FINISH	SIZE B; SHT 4 OF 7; DRAWING NO 2003500; REV B5

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B5	SEE SHT 1		

SH 6 XTAL 1

SH 1 { IRQ, AB0, AB1, R/W, AB9, I.O.P.SEL, DB0, DB1, DB2, DB3, DB4, DB5, DB6, DB7, Ø2 }

SH 6 RESET

SH 1 AB11

SH 7 BI·DIR·ENA

SH 1 AB10

XL1 A49 6551 — IRQ, RS0, RS1, R/W, CS0, CS1, DB0–DB7, Ø2, RESET; RTS, RxD, TxD

XL1 A50 6551 — IRQ, RS0, RS1, R/W, CS0, CS1, DB0–DB7, Ø2, RESET; DTR, RTS, TxD, RxC, DSR, DCD, RxD, CTS

XL1 A51 6551 — IRQ, RS0, RS1, R/W, CS0, CS1, DB0–DB7, Ø2, RESET; RTS, TxD, DTR, DSR, DCD, RxD, CTS; RxC → PIO-14

+5V

P3-8 DCD — R37 4.7K — A57 1489 — C63 330 PF

P3-6 DSR — R35 4.7K — C60 330 PF

P3-3 RxD — C61 330 PF

P3-5 CTS — R36 4.7K — C62 330 PF

P6-3 RxBOD — A40 1489 — C34 330 PF

P4-4 RTS — E11 — E10 — R22 4.7K — C46 330 PF

P4-20 DTR — E13 — E12 — C48 330 PF

P4-2 TxD — R21 4.7K — C47 330 PF

P0-3 BEEP/TxD

P1-3 BEEPER — A68 74LS367

SH 7 OUT SPEAKER — R42 330Ω — R41 330Ω — R43 330Ω — E25 — E24 — SP1 — Q4 2N2219

C41 330 PF — C40 330 PF — C22 .01UF — C23 .01 UF — +12V — GND — RxD

A68 74LS367 — E7 — E9 — E8

+12V — R27, 510Ω 1/2W — R30 510Ω 1/2W

P7-1 P7-2 P0-4 P0-2 P0-1 P1-1 P1-2 P1-4 P3-9 P3-14

A69 74LS04 — A70 74LS00 — 74LS08 A29 — PIO-7,3 — PIO-5 — E36 E37 — PIO-11 E38 — PIO-9 E39

PIO-13 — P6-12

74LS32 A58 — A48 1488 — TxD MOD — TxD — P6-2 P3-2

C57 330 PF

74LS32 A58 — A39 1488 — DCD — P4-8

C43 330 PF

74LS32 A58 — C45 330 PF — RxD — P4-3

A39 1488 — C55 330 PF — DTR — P3-20

A48 1488 — C44 330 PF — CTS — P4-5

A39 1488 — A48 1488 — RTS — P3-4

C56 330 PF

A39 1488 — C42 330 PF — DSR — P4-6

A59 74LS157 STR — 4A 4B 4Y, 3A 3B 3Y, 2A 2B 2Y, 1A 1B 1Y, SEL

E40 → PIO-10 — P3-10

E41 → PIO-8

E42 E43 → PIO-6 PIO-4

A48 1488 — PIO-2 PIO-12

SIG. GND — P3-7

SIG. GND — P4-7

PROT. GND — P3-1

PROT. GND — P4-1

TxD1 (TTY) — P3-25

TxD2 (TTY) — P3-13

P3-12 RxD1 — TIL 117 A47 — D3 1N914 — P3-24 RxD2 — R26 100 K Ω — R28 3.3K

A38 74LS00 — E29 E30 E31

A10 7406 — R33, 68Ω — R34 510Ω — Q3 2N2907A — A56 4N38 — Q2 2N3019 — D4, 1N914 — R32 51K — R31 4.7K

APPLICATION	
NEXT ASSY	USED ON

UNLESS OTHERWISE NOTED DIMENSIONS ARE IN — ANG 2 PLC 3 PLC — SCALE NONE — MATERIAL

DWN G. Cavallero 1/20/81 — CHK — ENGR — APPD — APPD — APPD — FINISH

TeleVideo, Inc.

TITLE: PCB SCHEMATIC 950 CONT BD

R600002-001

SIZE D — SHT 5 OF 7 — DRAWING NO 7000800 — REV B5

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B5	SEE SHT 1		

SH 2 RA Ø
SH 2 RA 3
SH 7 BLACK·ON·WHITE (B·O·W)
SH 4 BLINK
SH 7 BLI·RATE
SH 4 BLANK
DOTS·SERIAL
ROW·9
UNDERLINE
DEL CURSOR
REVERSE VIDEO
DEL DISPL·EN –
HALF·INTENSITY
SH 7 FORCE·BLANK
SH 2 VSN
SH 7 $\overline{HSN}$
SH 1 $\overline{DISP·MEN}$
SH 1 IO·P·SEL
SH 1 AB13

74LS00 A11, A11, A9, A9, A1, A1, A13
74LS04 A2, A2, A12, A12, A10, A10, A10, A10, A2, A2, A8, A8, A8, A12
74LS86 A1, A1, A1
74LS32 A2, A16, A16
74LS163 A3, A4
74LS08 A7
74LS109 A6

$\overline{ROW·9}$ SH 4
C9 0.01 µf
R5 1K
R6 750 Ω
R4 270 Ω
R7 22 Ω
R3 1K
R1 1K
R2 68 Ω
D1 1N914
Q1 2N2219
C6 4.7 µf
E1 E2 E3 E4

+12V P8-5, P8-6, P6-1, P6-14
+5V P6-6, P6-9
-12V P6-5, P6-10
GND P6-7, P6-8, P8-9, P8-10
P2-4
P2-3
SH 4 COMP.V+TTL VIDEO P2-6
+VSYNC ($\overline{VSN}$) P2-5
+HSYNC. P2-1
$\overline{SEL·CPU·ADDR}$ SH 2
DC.CARRY SH 4
C.CLK SH 2
$\overline{DC.CARRY}$ SH 4
$\overline{C.CLK}$ SH 7

R8 1K
R9, 1K
R10, 1K
OSC. 1 K1114A 23.814 MHZ
E32 E33
R11 3.3K
R12 1M
R13 47K
R29 4.7K
C12 .01µf
C13 .01µf
C15 10µf
C49 .01µf
1N914 D2
A17 555 TIMER
$\overline{RESET}$ SH 1,5,7
ϕ 0 SH 1
$\overline{SHIFT·CLK}$ SH 4
SHIFT·CLK SH 4
XTAL1 SH 5
$\overline{QC·CLOCK}$ SH 3

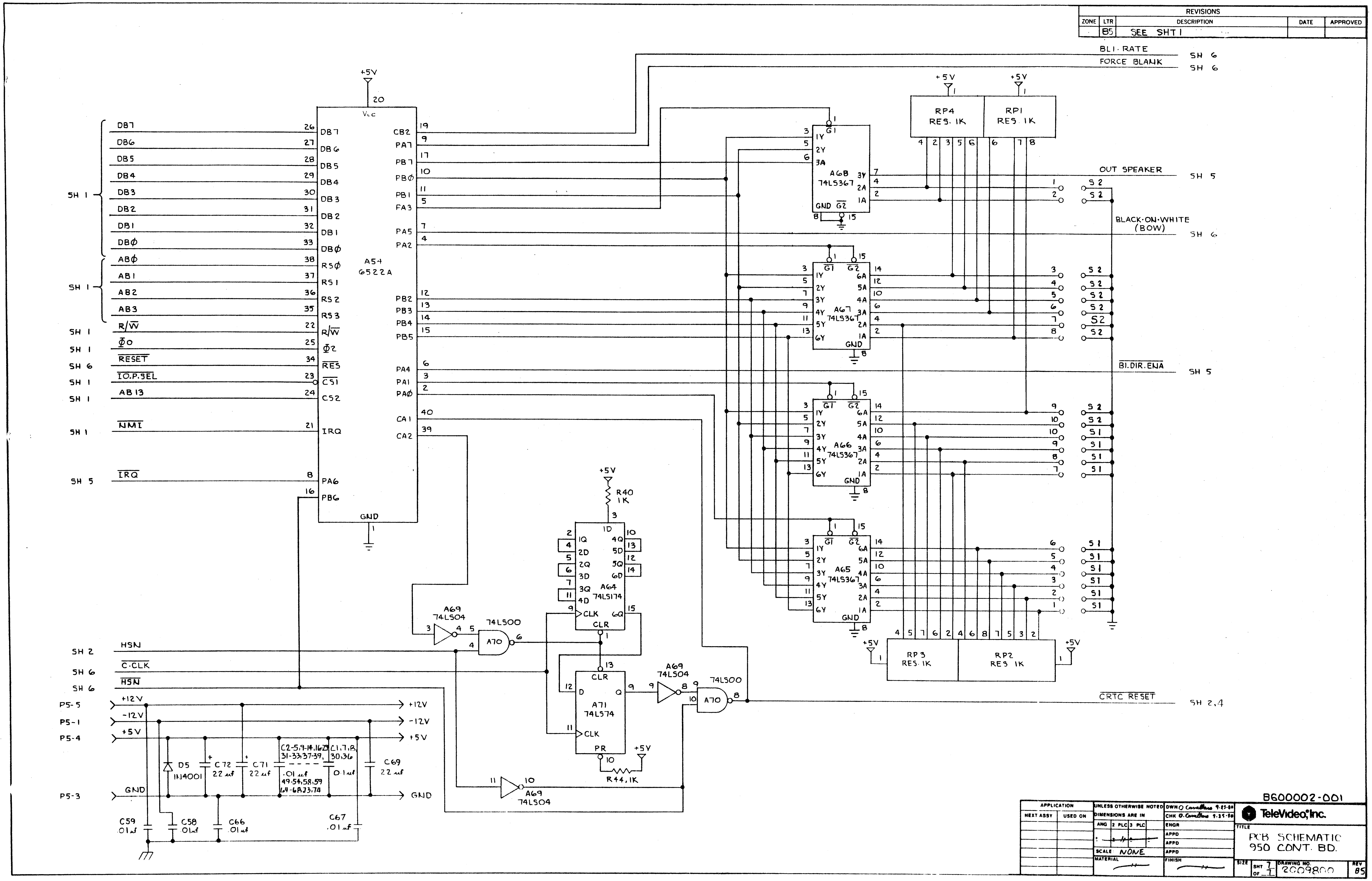
B600002-001

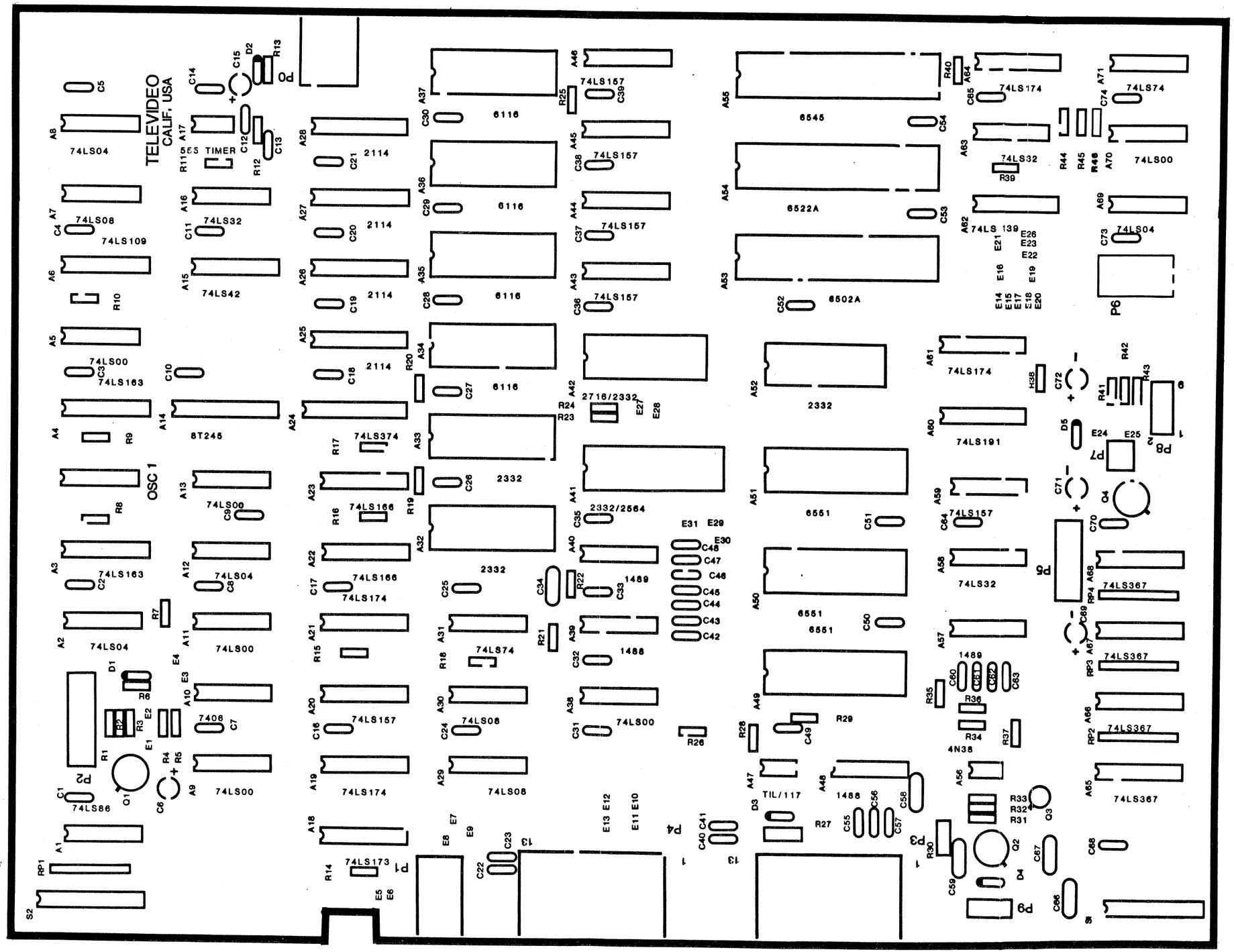
APPLICATION	
NEXT ASSY	USED ON

UNLESS OTHERWISE NOTED DIMENSIONS ARE IN ANG ± PLC .3 PLC
SCALE NONE
MATERIAL
FINISH

DWN O. Carrillo 9-25-80
CHK O. Carrillo 9-25-80
ENGR
APPD
APPD
APPD

TeleVideo, Inc.
TITLE PCB SCHEMATIC 950 CONT. BD.
SIZE D SHT 6 OF 7 DRAWING NO 2003800 REV B5


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
B5 SEE SHT 1
BLI. RATE SH 6
FORCE BLANK SH 6
OUT SPEAKER SH 5
BLACK-ON-WHITE (BOW) SH 6
BI.DIR.ENA SH 5
CRTC RESET SH 2,4
A54 6522A
A68 74LS367
A67 74LS367
A66 74LS367
A65 74LS367
A64 74LS174
A71 74LS74
A69 74LS04
A70 74LS00
RP4 RES. 1K
RP1 RES. 1K
RP3 RES. 1K
RP2 RES 1K
R40 1K
R44, 1K
S1
S2
SH 1
SH 2
SH 5
SH 6
DB7 DB6 DB5 DB4 DB3 DB2 DB1 DBØ
ABØ AB1 AB2 AB3
R/W̄
Φ0
RESET
I.O.P.SEL
AB 13
NMI
IRQ
HSN
C.CLK
P5-5 +12V
P5-1 -12V
P5-4 +5V
P5-3 GND
D5 1N4001
C72 22 uf
C71 22 uf
C2-5,9-14,16,23 31-33,37-39, 49-54,58,59 64-68,73,74 .01 uf
C1,7,8, 30,36 0.1 uf
C69 22 uf
C59 .01 uf
C58 .01 uf
C66 .01 uf
C67 .01 uf
B600002-001
TeleVideo, Inc.
PCB SCHEMATIC
950 CONT. BD.
SCALE NONE
DRAWING NO. 2009800
REV B5



950
CONTROLBOARD
REV B

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	B											
1	44									C2-5,9-14,16-29,	Cap CER .01uf 16V 20%	2028700
										31-33,37-39,49-		
										54,58,59,64-68,		
										73,74		
2	3									C69,71,72	Cap Elec 22uf 15V	2025700
3	17									C34,40-48,55-57,	Cap CER 330pf 50V 20%	2029100
										60-63		
4	1									C6	Cap Tant 4.7uf 16V 10%	2027500
5	1									C15	Cap Elec 10uf 16V 20%	2027300
6	5									C1,7,8,30,36	Cap Mono .1uf 20%	2186800
7	1									C75	Cap Mica 100pf 50V 5%	2024700
8	1									A60	IC 74LS191	2036600
9	1									A21	IC 74LS174	2044600
10	1									A6	IC 74LS109	2027000
11	6									A5,9,11,13,38,70	IC 74LS00	2024200
12	4									A2,8,12,69	IC 74LS04	2024800
13	1									A10	IC 7406	2034800
14	3									A7,29,30	IC 74LS08	2025200
15	3									A16,58,63	IC 74LS32	2025800
16	2									A31,71	IC 74LS74	2026600
17	1									A1	IC 74LS86	2026800

NOTES:

TITLE PCB ASSY CONTROL BOARD 950

DATE 11-11-82

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL B									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
18	1									A62	IC 74LS139	2027200
19	6									A20,43-46,59	IC 74LS157	2027400
20	2									A3,4	IC 74LS163	2027600
21	2									A22,23	IC 74LS166	2027800
22	1									A18	IC 74LS173	2028000
23	3									A19 ,61,64	IC 74LS174	2028200
24	4									A65-68	IC 74LS367	2028600
25	1									A24	IC 74LS374	2029000
26	2									A39,48	IC 75188N	2029200
27	2									A40,57	IC 75189AN	2029400
28	1									A47	IC TIL117	2029800
29	1									A56	IC 4N38	2035000
30	4									A25-28	IC 2114ICB RAM	2035800
31	1									A34-37	IC 6116 RAM 150ns	2049200
32	1									A53	IC 6502A Micro	2049600
33	1									A55	IC 6545 Contr CRT	2049800
34	3									A49-51	IC 6551 1MHz UART	2155700
35	1									A54	IC 6522A	2050200
36	1									A14	IC 74LS245	2036200
37	1									OSC-1	CRY K1114A 23.814MHz OSC	2035200
38	1									A41	IC 2532 EPROM F00D Sys Prg950	8000043

NOTES:

TITLE PCB ASSY CONTROL BOARD 950

DATE 11-11-82

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	B											
39	1									A33	IC ROM Up Char Gen	8000002
40	1									A32	IC ROM Low Char Gen	8000003
41	1									A42	IC 2532E0000 EPROM Sys	8000044
											Prog 950	
42	1									A15	IC 74LS42	2026000
43	1									A17	IC NE555	2030200
44	2									R6,41	Res CF 750 Ohm 1/4W 5%	2031700
45	1									R32	Res CF 51K Ohm 1/4W 5%	2032300
46	2									R2,33	Res CF 68 Ohm 1/4W 5%	2051100
47	7									R21,22,29,31,	Res CF 4700 Ohm 1/4W 5%	2053100
										35-37		
48	1									R4	Res CF 270 Ohm 1/4W 5%	2051300
49	2									R42,43	Res CF 330 Ohm 1/4W 5%	2051500
50	1									R34	Res CF 510 Ohm 1/4W 5%	2051900
51	20									R1,3,5,8,9,10,14,	Res CF 1000 Ohm 1/4W 5%	2052100
										15-20,23-25,38,		
										40,44		
52	5									R11,28,39,45,46	Res CF 3300 Ohm 1/4W 5%	2052700
53	1									R26	Res CF 100K 1/4W 5%	2032100
54	1									R12	Res CF 1M Ohm 1/4W 5%	2031500
55	4									RP1-4	Res PK 1K Ohm 8 Pin SIP	2042700

NOTES:

TITLE PCB ASSY CONTROL BOARD 950

DATE 11-11-82

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	B											
56	2									R27,30	Res CF 510 Ohm 1/2W 5%	2045100
57	1									R7	Res CF 22 Ohm 1/4W 5%	2033500
58												
59												
60												
61												
62												
63												
64												
65	2									Q1,4	Tran 2N2219A	2045300
66	1									Q2	Tran 2N3019	2045700
67	1									Q3	Tran 2N2907A	2045900
68												
69												
70	4									D1-4	Diode 1N914	2047500
71	1									D5	Diode 1N4001	2047700
72												
73	2									S1,2	Switch 10 Pos Dip/20P Side	2096800
											Adj	
74												
75												

NOTES:

TITLE PCB ASSY CONTROL BOARD 950 DATE 11-11-82

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	B											
76												
77	1									R13	Res CF 47K Ohm 1/4W 5%	2033700
78	9									XA32-37,41,42,52	Socket 24P IC Dip	2098401
80	3									XA49-51	Socket 28P IC Dip	2098404
81	3									XA53-55	Socket 40P IC Dip	2098402
82												
83	2									P3,4	Conn 25P PCB D-Sub Fem	2097800
84	2									P2,5	Plug 5P Str Waf	2098802
85	1									P1	Conn PCB RJ11 Fem (AMP)	2097900
86	1									P9	Plug 2 P Str Waf	2098800
87	3									Q1,2,4	Insul Pad Tran 3005-A Large	2180800

NOTES:

TITLE	DATE	
PCB ASSY CONTROL BOARD 950	11-11-82	TeleVideo Systems, Inc.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	PROD REL PER ECO 0333		
	A2	PROD REL PER ECO 0395		
	B	REVISED PER ECO 0456		
	B1	" " ECO 0554		
	B2	" " 0544		

ZONE D | LTR B3 | DESCRIPTION RECORD CHANGES PER ECO # 2010 | DATE 3-19-82 | APPD

SH6 E19 E16 EX

E20 E18 E17 E15 E14 E19 E16

E44 E45

+5V R16 1K

20 OE/CS
18 CS/A11
21
A20 2532

+5V VCC 24
GND 12
+5V R17 1K
E27 E28

22 PD/PGM
20 A11
23 A12
A25 2532
+5V VCC 28 VPP 1 26 VCC 14 GND 2 CS1 27 CS2

A15 2332
24 VCC
21 CS
20 CS
18 A11
8 AØ
7 A1
6 A2
5 A3
4 A4
3 A5
2 A6
1 A7
23 A8
22 A9
19 A10
GND 12
I/O1 9
I/O2 10
I/O3 11
I/O4 13
I/O5 14
I/O6 15
I/O7 16
I/O8 17

+5V R39 3.3K
SH7 IRQ 4 IRQ
+5V R38 3.3K
SH7 NMI 6 NMI

A11 G502A
8 VCC
ABØ 9
AB1 10
AB2 11
AB3 12
AB4 13
AB5 14
AB6 15
AB7 16
AB8 17
AB9 18
AB10 19
AB11 20
AB12 22
AB13 23
AB14 24
AB15 25
R/W 34
Φ2 39
DBØ 33
DB1 32
DB2 31
DB3 30
DB4 29
DB5 28
DB6 27
DB7 26
1 21

SH4 ΦØ 37 ØO
SH7 RESET 40 RESET

R23 3.3K +5V

E21 E22 E23 E26

PII-8 PII-7 PII-5 PII-3
AB Ø AB 1 } SH 2,5,7
AB 2 } SH2,7
AB 3
AB 4 AB 5 AB 6 AB 7 } SH2
AB8 SH2,6
AB9 ABI0 } SH2,5
ABI1
ABI2 SH2,6
ABI3 SH2,6,7
ABI4 ABI5 } SH 6
R/W SH2,3,5,6,7
PII-20
DBØ DB1 DB2 DB3 DB4 } SH 2,3,5,7
DB5 DB6 DB7 } SH2,3,5,6,7
P8-1
P8-2
P8-3
P8-8
P8-7
E23 SH6

NOTES UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE VALUED IN OHMS ±5% AND ARE 1/4 WATT.
2. ALL CAPACITORS ARE VALUED IN µF, 16VDC, ±20%
3. DRAWINGS COMFORMS WITH TELEVIDEO SPEC. 212730

B600002-002

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	DWN H HUR 3-8-82	TeleVideo, Inc.
NEXT ASSY	USED ON	ANG 2 PLC 3 PLC	CHK	
2009501	—	± ± ± ±	ENGR	TITLE PCB SCHEMATIC CONT. BD 950 G/A
		SCALE	APPD	
		MATERIAL	APPD	
		FINISH	APPD	SIZE D SHT 1 OF 7 DRAWING NO 2009801 REV B3

B3 2009801

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHT 1		

SH6 CRTC.RESET
SH4 CCLK
SH1 AB0, R/W
SH1 DB0, DB1, DB2, DB3, DB4, DB5, DB6, DB7
SH6 SEL CRTC
SH4 Ø0
SH1 AB1, AB2, AB3, AB4, AB5, AB6, AB7
SH1 AB8, AB9, AB10, AB11
SH1 AB12, AB13
SH6 DISP.MEM
SH6 SEL.CPU.ADDR

+5V → 20 VCC

A6 6545

2	RES	HSYNC	39
21	CCLK	VSYNC	40
		ENABLE	18
		CURSOR	19
24	RS	RAØ	38
22	R/W	RA1	37
		RA2	36
		RA3	35
		RA4/STB	34
1	VSS	MAØ	4
3	LPEN	MA1	5
33	DBØ	MA2	6
32	DB1	MA3	7
31	DB2	MA4	8
30	DB3	MA5	9
29	DB4	MA6	10
28	DB5	MA7	11
27	DB6	MA8	12
26	DB7	MA9	13
		MA10	14
		MA11	15
		MA12	16
		MA13	17
25	CS	Ø2	23

HSYNC → HSN → SH6
VSYNC → VSN → SH4,6
ENABLE → DISPLENA
CURSOR → CURSOR
DISPLENA, CURSOR → SH4
RAØ → P11-22
RA1 → P11-23

+5V → R11 4.7K

A7 74LS157
A12 74LS157
A16 74LS157
A21 74LS157

	1A	2A	3A	4A	1B	2B	3B	4B	EN	SEL B	1Y	2Y	3Y	4Y
A7	2	5	11	14	10	13	3	6	15	1	4	7	9	12
A12	2	5	11	14	3	6	10	13	15	1	4	7	9	12
A16	2	5	11	14	3	6	10	13	15	1	4	7	9	12
A21	2	5	11	14	3	6	10	13	15	1	4	7	9	12

SEL.CPU.ADDR → SEL B

A7: 1Y DMEM.EN, 2Y AD.RAM.13, 3Y AD.RAM.12, 4Y → SH3
A12: 1Y AD.RAM.11, 2Y AD.RAM.10, 3Y AD.RAM.9, 4Y AD.RAM.8 → SH3
A16: 1Y AD.RAM.7, 2Y AD.RAM.6, 3Y AD.RAM.5, 4Y AD.RAM.4 → SH3
A21: 1Y AD.RAM.3, 2Y AD.RAM.2, 3Y AD.RAM.1, 4Y AD.RAM.Ø → SH3

APPLICATION		UNLESS OTHERWISE NOTED	DWN H HUR 3-8-82
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK
2009501	—	ANG 2 PLC 3 PLC	ENGR
			APPD
		SCALE	APPD
		MATERIAL	APPD
			FINISH

B600002-002

TeleVideo, Inc.

TITLE: PCB SCHEMATIC CONT. BD 950 G/A

SIZE D | SHT 2 OF 7 | DRAWING NO 2009801 | REV B3

B3 2009801

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHT 1		

SH2 AD.RAM.13
AD.RAM.11
AD.RAM.12
SH4 QC CLK

A2 74LS42 (C, A, B, D; Ø, 9, 8, 7, 6, 5, 4)

SH2 AD.RAM.10
AD.RAM.9
AD.RAM.8
AD.RAM.7
AD.RAM.6
AD.RAM.5
AD.RAM.4
AD.RAM.3
AD.RAM.2
AD.RAM.1
AD.RAM.Ø

A3 6116 · A8 6116 · A13 6116 · A17 6116 · A22 6116
+5V, VCC, GND, CS, WE, OE, A0–A10, I/O1–I/O8

SH6 DM.R/$\overline{W}$

SH1 DB.7
DB.6
DB.5
DB.4
DB.3
DB.2
DB.1
DB.Ø

A26 BT245 (B7–B1, BØ; A7–A1, AØ; OE, DIR)

CH.AD.7
CH.AD.6
CH.AD.5
CH.AD.4
CH.AD.3
CH.AD.2
CH.AD.1
CH.AD.Ø
→ SH4

SH2 $\overline{DMEN.EN}$
SH1 R/$\overline{W}$

DB.7 → P11-24
DB.6 → P11-18
DB.5 → P11-15
DB.4 → P11-16
DB.3 → P11-13
DB.2 → P11-12
DB.1 → P11-11
DB.Ø → P11-10

P5-5 +12V
P5-1 −12V
P5-4 +5V
P5-3 GND

CR1 IN4001
C2 22 50V
C3 22 50V
C27–55, C57–68 .01
0.1
C1 22 50V
C69 .01
C70 .01
C71 .01
C72 .01

→ +12V, −12V, +5V, GND

APPLICATION		UNLESS OTHERWISE NOTED	DWN HHUR 3-9-82	TeleVideo, Inc.
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK	
2609501	—	ANG 2 PLC 3 PLC	ENGR	TITLE: PCB SCHEMATIC CONT. BD 950 G/A
			APPD	
		SCALE	APPD	
		MATERIAL	FINISH	SIZE D · SHT 3 OF 7 · DRAWING NO 2009801 · REV B3

B1000021-002

B3 2009801

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHT 1		

SH3: CH.AD.7, CH.AD.6, CH.AD.5, CH.AD.4, CH.AD.3, CH.AD.2, CH.AD.1, CH.AD.Ø

A27 74LS374 (6D 3D 4D 5D 1D 8D 2D 7D → 6Q 3Q 4Q 5Q 1Q 8Q 2Q 7Q, CLK, OE)

SH6: RAØ, RA1, RA2, RA3

R18 4.7K +5V

A30 2332 (VPP VDD; A11 A10 A9 A8 A7 A6 A5 A4 CS; AØ A1 A2 A3; Ø1 Ø2 Ø3 Ø4 Ø5 Ø6 Ø7 Ø8)

R19 4.7K +5V

A31 2332 (A0 A1 A2 A3 VPP; A11 A10 A9 A8 A7 A6 A5 A4 CS; VDD; Ø1 Ø2 Ø3 Ø4 Ø5 Ø6 Ø7 Ø8)

OSC1 K1114A 23.814 MHZ A45 (+5V, pin 14, pin 8, pin 7)

E32 E33

C24 47PF 50V

R41 33

C23 20PF 50V

LCHAD Ø LCHAD 1 LCHAD 2 LCHAD 3

CG 15 CG 14 CG 13 CG 12 CG 11 CG 10 CG 9 CG 8 CG 7 CG 6 CG 5 CG 4 CG 3 CG 2 CG 1 CG Ø

A34 GATE ARRAY I740012-008

CHAR LATCH OUT EN	
LATCH CHAR	
B.O.W.	SH 7
CLOCK EXTEND	SH 6
SHIFT CLOCK	
ROW 9	SH 6
VERT SYNC	SH 2
HORIZ SYNC	SH 6
DISP. EN	SH 2
CURSOR	
BLINK RATE	SH 7

Ø0	SH 1,2,5,6,7
XTAL 1	SH 5
CHAR CLOCK	SH 2,6
QC CLOCK	SH 3
COMPOSITE VIDEO	SH 6
HALF INTENSITY	
VIDEO	
VSS	

+5V → P6-6, P6-9, P11-1, P11-2

+12V → P6-1, P6-14, P8-5, P8-6, P11-6

-12V → P6-5, P6-10, P8-9, P8-10, P11-14

E36 → P11-25

P6-7, P6-8, P10-2, P10-12, P11-9, P11-19

SHIFT CLOCK → P11-21

P3-12 RXDI, P3-24 RXD2

CR3 IN914, TIL 117 A10

R40 100K

R15 3.3K

A14 74LS00

A18 1488

P3-10, SIG.GND P3-7 P4-7, PROT.GND P3-1 P4-1

R4 68

R5 510

4N38 A5

Q2 2N2907A

Q3 2N3019

CR2 IN914

R10 51K

R9 4.7K

SH5 TXD

TXDI (TTY) P3-25

TXD2 (TTY) P3-13

+12V R1 510 → P3-9

R2 510 → P3-14

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	DWN H HUR 3-10-82
NEXT ASSY	USED ON	ANG 2 PLC 3 PLC	CHK
2009501	—		ENGR
		SCALE	APPD
		MATERIAL	APPD
			FINISH

TeleVideo, Inc.

TITLE: PCB SCHEMATIC CONT. BD 950 G/A

SIZE D | SHT 4 OF 7 | DRAWING NO 2009801 | REV B3

B600002 002

2009801 B3

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHT 1		

SH4 XTAL 1
SH7 IRQ
SH1 AB Ø
AB 1
R/W
AB 9
SH6 IO.P.SEL
DB Ø
DB 1
DB 2
DB 3
DB 4
DB 5
DB 6
DB 7
SH1 Ø 1
SH4 Ø 2
SH7 RESET
SH6 RXD
SH1 AB 11
SH6 DTR
SH7 BI.DIR.ENA
SH1 AB 10

A36 6551 XL1
A29 6551 XL1
A33 6551 XL1
+5V
SH6 RTS
SH6 DTR

DCD P3-8
DSR P3-6
RXD P3-3
CTS P3-5
RXD MOD P6-3
RTS P4-4
DTR P4-20
TXD P4-2
BEEPER/TXD P0-3 P1-3
BEEPER P6-13
OUT SPEAKER SH 7

R12 4.7K
R13 4.7K
R14 4.7K
R2 4.7K
R3 4.7K
R7 330
R6 330
R8 330
E11 E10 E13 E12
E25 E24 E7 E8 E9

A9 1489
A32
A19 74LS32
A19 74LS37
Q1 2N2219A

C8 C4 C9 C7 C13 C14 C18 C17 330 PF 100V
C19 330PF 100V
C25 330 PF 100V
C74 .01
C73 .01
+12V
GND

P7-1
P7-2
P0-4
P0-2
P0-1
P1-1
P1-2
P9-1
P9-2
P1-4
RXD

RXD (MODEM)
RXD (HOST)
SH6

P10-11
P10-9
P10-3,7
P10-5
P10-10
P10-8
P10-6
P10-4
P10-13
P6-12
TXD SH4
TXD P3-2
TXD MOD P6-2
DCD P4-8
RXD P4-3
DTR P3-20
CTS P4-5
RTS P3-4
DSR P4-6

A28 74LS157
A18 1488
A23 1488
A24 74LS32

C10 C15 C16 C6 C11 C5 C12 330 PF 100V

E29 E30 E31
P10-14

B600002-002

APPLICATION	
NEXT ASSY	USED ON
2009501	—

UNLESS OTHERWISE NOTED DIMENSIONS ARE IN: ANG ± 2 PLC ± 3 PLC ± .x ± .xx
SCALE:
MATERIAL
FINISH

DWN HHUR 3-12-82
CHK
ENGR
APPD
APPD
APPD

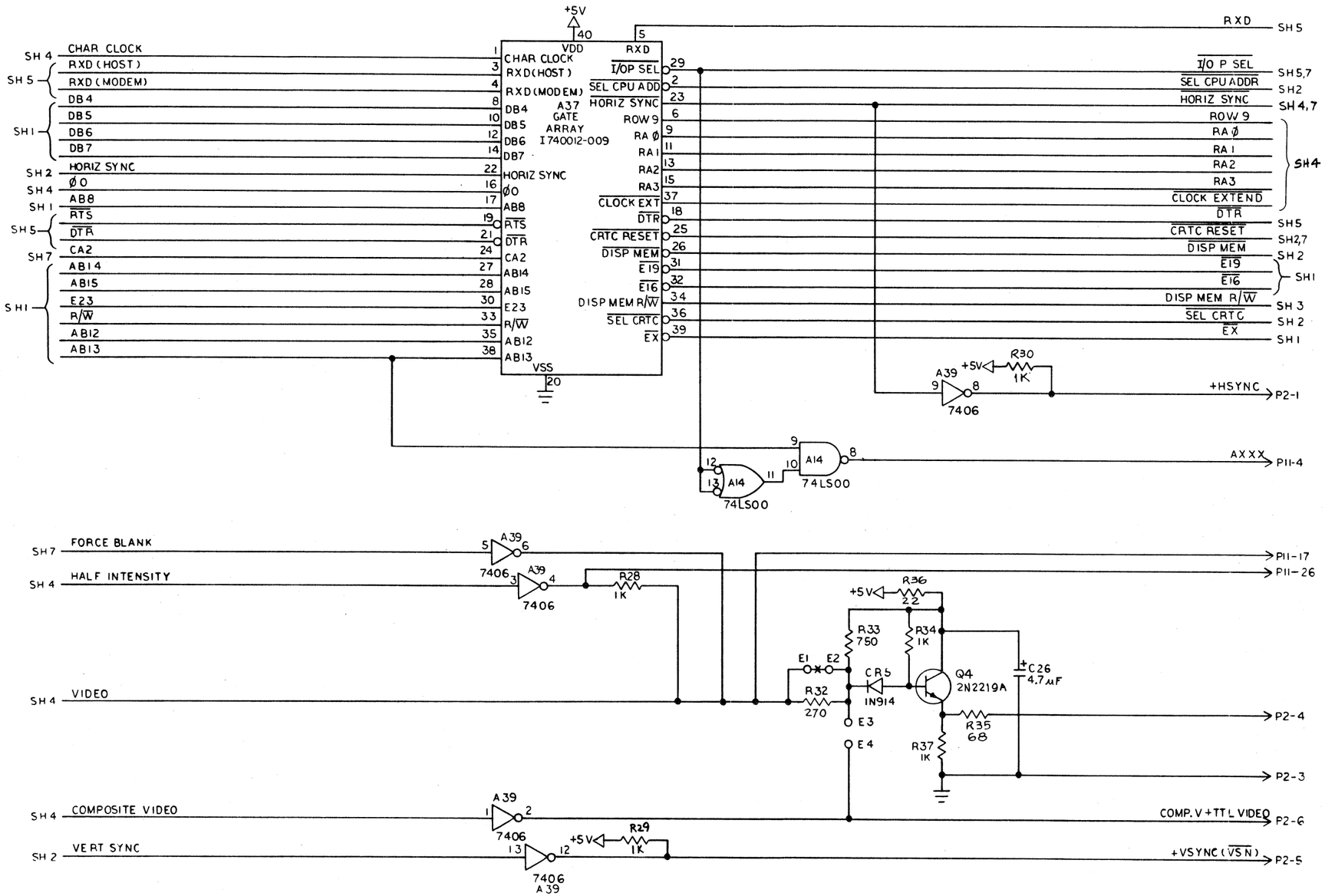
TeleVideo, Inc.

TITLE: PCB SCHEMATIC CONT. BD 950 G/A

SIZE D | SHT 5 OF 7 | DRAWING NO. 2009801 | REV B3

B3 2009801

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHT 1		



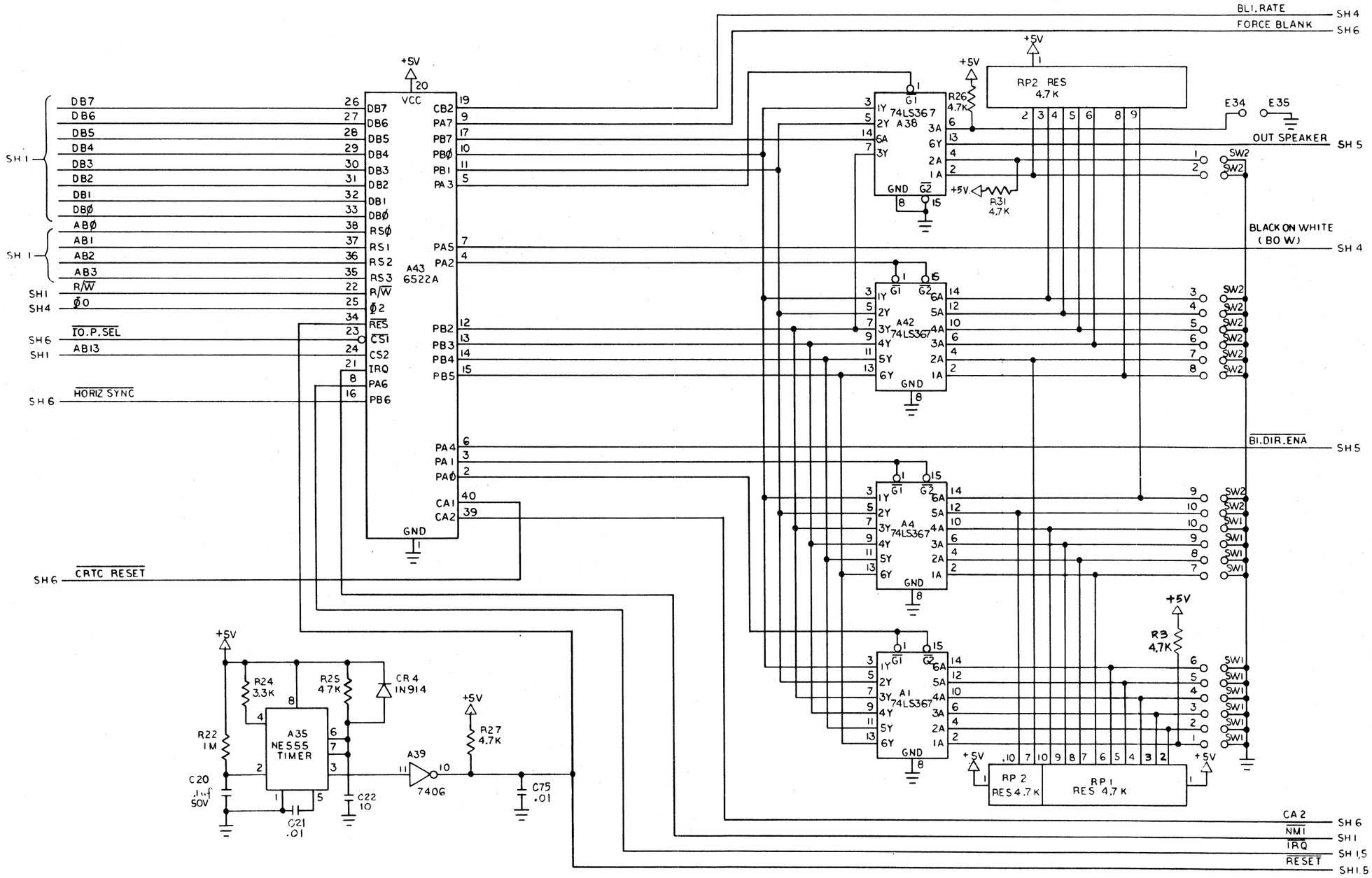
APPLICATION		UNLESS OTHERWISE NOTED	DWN HHUR 3-17-82	TeleVideo, Inc.
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK	
2009501	—	ANG 2 PLC 3 PLC	ENGR	TITLE
		± ± ±	APPD	PCB SCHEMATIC
		SCALE	APPD	CONT. BD 950 G/A
		MATERIAL	APPD	
			FINISH	

B600002-001

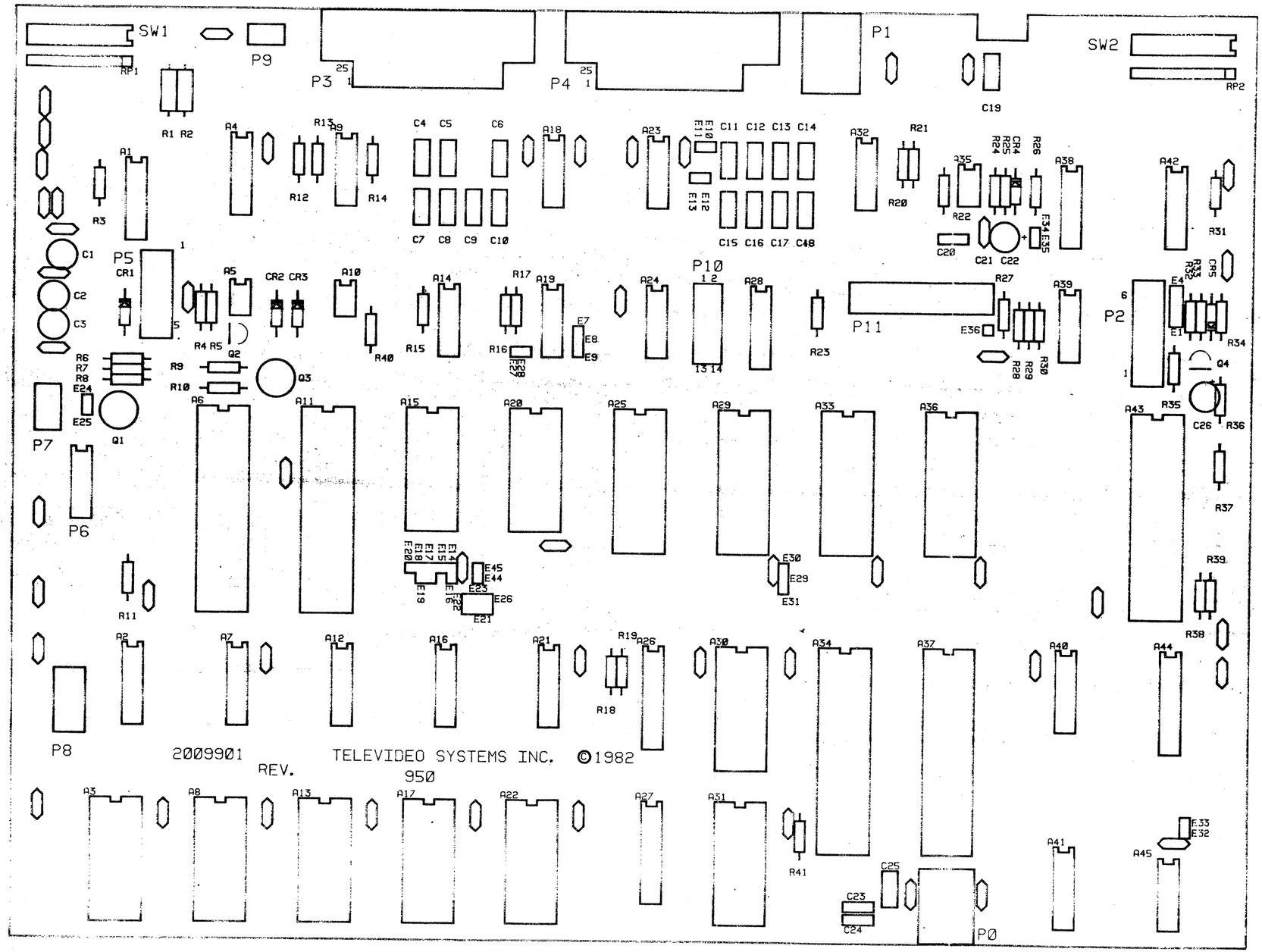
SIZE	SHT	DRAWING NO	REV
D	6 OF 7	2009801	B3

B3 2009501

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		SEE SHT 1		



APPLICATION		UNLESS OTHERWISE NOTED	DWN H HUR 3-15-82	TeleVideo, Inc.
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK	
2009501	—	ANG ± 2 PLC ± 3 PLC	ENG	TITLE
			APPD	PCB SCHEMATIC
		SCALE	APPD	CONT. BD 350 (A)
		MATERIAL	APPD	
		FINISH		SIZE D SHT 7 OF 7 DRAWING NO 2009501 REV B3



950 GATE ARRAY
CONTROL BOARD
REV B

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	B											
1												
2												
3												
4												
5												
6	1									C23	Cap Mica 20pf 50V 10%	2024300
7	1									C26	Cap Tant 4.7uf 16V 10%	2027500
8	1									C20	Cap Cer .1uf 50V 10%	2030100
9	48									C27-55,57-75	Cap Cer .01uf 16V 20%	2028700
10	1									C22	Cap Elect 10uf 16V 20%	2027300
11	17									C4-19,25	Cap Mono 330pf 100V 20%	2029300
12	3									C1,2,3	Cap Elect 22uf 50V 10%	2026100
13	1									C21	Cap Mono .01uf 50V 10%	2028900
14	1									C24	Cap Mica 47pf 50V 5%	2024900
15												
16	4									A1,4,38,42	IC 74LS367	2028600
17	1									A2	IC 74LS42	2026000
18	2									C3,22	IC 6116 RAM 150ns	2049200
19	1									A5	IC 4N38	2035000
20	1									A6	IC 6545 Contr CRT	2049800
21	5									A7,12,16,21,28	IC 74LS157	2027400

NOTES:

TITLE PCB ASSY CONTROL BOARD 950 GATE ARRAY

DATE 11-11-82

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	B											
22	2									A9,32	IC 74189AN	2029400
23	1									A10	IC TIL117	2029800
24	1									A11	IC 6502A Micro	2049600
25	1									A14	IC 74LS00	2024200
26	1									A25	IC 2532 EPROM F000 Sys	8000043
27	2									A18,23	IC 75188N	2029200
28	2									A19,24	IC 74LS32	2025800
29												
30												
31	1									A26	IC 74LS245	2036200
32	1									A27	IC 74LS374	2029000
33	3									A29,33,36	IC 6551 UART 1MHz	2155700
34	1									A34	IC G/A 950(A)	2057600
35	1									A37	IC G/A 950(B)	2057800
36	1									A35	IC NE555	2030200
37	1									A39	IC 7406	2034800
38	1									A43	IC 6522A	2050200
39	1									A45	CRY K1114A 23.814MHz OSC	2035200
40	1									A20	IC 2532 E000 EPROM Sys	8000044
41	1									A31	IC ROM UP Char Gen	8000002
42	1									A30	IC ROM Char Gen Low 950	8000003

NOTES:

TITLE PCB ASSY CONTROL BOARD 950 GATE ARRAY

DATE 11-11-82

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL										REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
	B												
43	5										XA6,11,34,37,43	Socket IC 40P IC DIP	2098402
44	3										XA29,33,36	Socket IC 28P IC DIP	2098404
45	10										XA3,8,13,15,17,	Socket IC 24P IC DIP	2098401
											20,22,25,30,31		
46													
47	1										P6	Socket 14 Pin IC DIP	2098403
48	2										SW1,2	SW 10 Pos DIP/20P Side Adj	2096800
49	2										P3,4	Conn 25P PCB D-Sub Fem	2097800
50													
51													
52													
53	1										P1	Conn PCB RJ11 Fem (AMP)	2097900
54													
55													
56	2										P2,5	Plug 5P Str Waf	2098802
57	1										Q3	Insul Pad Tran 3005-A	2180800
58													
59													
60	1										R41	Res CF 33 1/4W 5%	2034500
61	7										R16,17,28-30,34,	Res CF 1K 1/4W 5%	2052100
											37		

NOTES:

TITLE		DATE	
	PCB ASSY CONTROL BOARD 950 GATE ARRAY	11-11-82	TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL B									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
62	1									R32	Res CF 270 1/4W 5%	2051300
63	1									R33	Res CF 750 1/4W 5%	2031700
64	1									R36	Res CF 22 1/4W 5%	2033500
65	2									R4,35	Res CF 68 1/4W 5%	2051100
66	5									R15,23,24,38,39	Res CF 3.3K 1/4W 5%	2052700
67	13									R3,9,11-14,18-21,	Res CF 4.7K 1/4W 5%	2053100
										26,27,31		
68	1									R22	Res CF 1M OHM 1/4W 5%	2031500
69	1									R40	Res CF 100K 1/4W 5%	2032100
70	2									R1,2	Res CF 510 1/2W 5%	2045100
71	1									R10	Res CF 51K 1/4W 5%	2032300
72	3									R6-8	Res CF 330 1/4W 5%	2051500
73	2									RP1,2	Res DIP 4.7K 10P SIP	2041300
74	1									R25	Res CF 47K 1/4W 5%	2033700
75	1									R5	Res CF 510 1/4W 5%	2051900
76	1									CR1	Diode 1N4001	2047700
77	5									CR2-5	Diode 1N914	2047500
78	2									Q1,4	Trans 2N2219A	2045300
79	1									Q3	Trans 2N3019	2045700
80	1									Q2	Trans 2N2907A	2045900

NOTES:

TITLE	DATE	
PCB ASSY CONTROL BOARD 950 GATE ARRAY	11-11-82	TeleVideo Systems, Inc.

VIDEO MONITOR/POWER SUPPLY SCHEMATICS AND PARTS LIST

TeleVideo Systems, Inc.
1170 Morse Ave., Sunnyvale, CA 94086
(408) 745-7760 TWX 910-338-7633 "TVI VIDEO"

VIDEO MONITOR

The video monitor contains two sections: the vertical amplifier and the horizontal amplifier. These amplifiers provide the voltages necessary to drive the CRT yoke, which deflects the electron beam across the CRT.

The electron beam, which is generated by the CRT electron gun, sweeps across and down the screen to create scan lines (see section on character generation). The beam's movement is driven by vertical and horizontal sweep rates, which are determined by the display circuitry on the logic board. The horizontal sweep is approximately 16 KHz, the vertical sweep 60 Hz for domestic and 50 Hz for European applications.

The horizontal synch pulses coming into the video monitor are inverted and amplified by transistor Q301. This signal is then coupled across the drive transformer T301 and applied to the base of the ouptut transistor Q302. Q302's output drives both horizontal yoke windings, as well as the step-up transformer that produces the anode voltage and the grid voltage for the CRT grid in the neck of the CRT. Since high-frequency magnetic fields are produced and then broken, the flyback transformer is necessary to provide high voltages for the horizontal scans.

These horizontal scans start in the upper left corner and scan across to the upper right corner. Once the scan reaches the end of the line, a blank appears where the video beam is turned off and retraced to the beginning of the next scan line.

The vertical synch pulses coming into the video monitor are converted to a sawtooth waveform. Initially, this pulse goes from a negative leading edge to a positive falling edge and passes through transistor Q202, which inverts it to its usable form.

At that point, the pulse goes from a +2-volt leading edge to a -2.5-volt falling edge. Timing is critical since 250 horizontal scan lines (which comprise the total number of horizontal scan lines on the CRT) occur within one sawtooth pulse. Therefore, the sawtooth pulse has to be proportional to all previous pulses or the timing will be off for the vertical as well as the horizontal sweep.

When the vertical sweep is negative, Q201 conducts and C202 discharges. During the positive portion, Q201 cuts off and allows C202 to charge. While C202 is charging, the electron beam scans.

The vertical sweep scans from top to bottom. Once it reaches the bottom of the page, a blank occurs when the video beam is turned off and is retraced to the top of the screen. At that point, C202 discharges. After the retrace, the beam turns off again and begins its scan routine.

Adjusting SFR1 (vertical height) and SFR2 (vertical linearity) changes the rate of C202's charge, and therefore the slope of the sawtooth pulse.

POWER SUPPLY

Voltages are created and regulated as follows: A 9.8 AC voltage is rectified by diodes D105 and D108, resulting in a 9-volt output. These 9 volts are then filtered through C117 and applied at the 5-volt regulator IC2.

The raw AC voltages for the positive and negative 12 DC voltage are derived from the center top of the secondary winding of D101. The diodes D101 and D102 form a full-wave rectifier that converts the 37-volt AC waveform to a 20-volt DC level. This DC voltage is then filtered by C116 and stabilized to -12 volts by a zener-regulated circuit that consists of a resistor (R102) and the zener diode (D112).

Diodes D103 and D104 also form a full-wave rectifier that converts the 37-volt AC waveform to a +20-volt DC level.

This DC voltage is filtered by C113 and applied to the 13.8-volt regulator IC1. The 13.8 output, in turn, is dropped 1.6 volts across diodes D113 and D114 to achieve the desired +12 volts DC.

A 79-volt AC waveform is applied to the half-wave rectifier D109, which is filtered by C119. The resulting 95-volt DC level is then regulated by a series voltage regulator. The reference element is the positive 12-volt zener diode D111. The sensing and control elements are transistors Q103 and Q102.

The high voltages needed to drive the CRT tube V501 are derived from the flyback transformer T302 on the video module.

TUBE SPECIFICATION

12 INCH 90 DEGREE, HIGH RESOLUTION

DISPLAY TUBE

310KGB 31

The 310KGB31 is a 12 inch 90 degree high resolution, rectangular display tube primarily intended for use as a alpha-numerical and graphic display tube for computer peripheral devices. The tube is provided with banded type integral implosion protection (with mounting lugs). The tube features a low reflectance high contrast screen.

ELECTRICAL DATA

Heating	
Indirect by AC or DC:	
Heater voltage	12.0 volts
Heater current	75 nA
Focusing Method	Electrostatic
Deflection Method	Magnetic
Deflection Angles (Approx.)	
Diagonal	90 degrees
Horizontal	78 degrees
Vertical	61 degrees
Anode voltage	15,000 max. volts 8,000 min. volts

Using high voltage with this tube internal flash-overs may occur, which may cause damage to the cathode of the tube and to various circuit components on the video monitor board. Therefore it is necessary to provide protective circuits using spark-gaps etc. These should be connected as illustrated in figure #1 below.

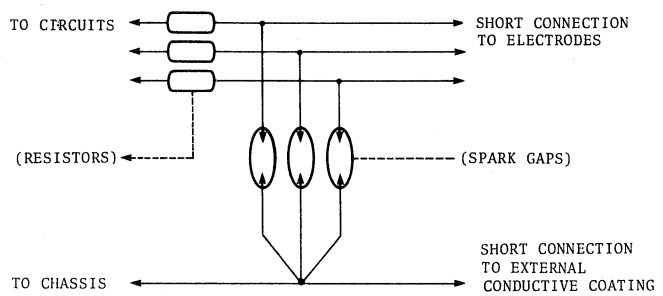


Figure 1.

No other connections between external conductive coating and chassis are permissible.

OPTICAL DATA

Faceplate	Filterglass
Anti-reflection treatment	No
Screen	Aluminized
Appearance	Low Reflective

A:
The dark-colored screen, in combination with the filterglass, produces the low reflectivity (equivalent to a 20% light transmission filterglass) for easy-to-see display.

MECHANICAL DATA

Tube Dimensions:

Overall length	278.8 max. mm
Greatest dimensions of tube (excluding lugs)	
Diagonal	318.5 +/- 2.7 mm
Width	279.6 +/- 2.7 mm
Heigth	218.7 +/- 2.7 mm
Useful screen dimensions (projected)	
Diagonal	295.0 min. mm
Width	257.0 min. mm
Heigth	195.0 min. mm

Pin Position Alignment	Pin No 5 aligns approx. with anode contact.
Operating Position	Any
Weight (approx.)	3.2 kg
Implosion Protection	Tension band (with mounting lugs)

GENERAL CONSIDERATIONS:

1. Tube handling. Care should be taken not to scratch the tube.

2. Impact. The tubes should never be exposed to impacts of more than 30G during handling or transportation.

3. Grounding. The external conductive coating of the tube should be grounded with multiple contacts (e.g. a contact plate having many fingers.) Poor contact might cause local heating resulting in tube leakage.

WARNING

SHOCK HAZARD:

The high voltage at which the tube is operated may be very dangerous. Design of the equipment should include safeguards to prevent the user from coming in contact with the high voltage. Extreme care should be taken in the servicing or adjustment of any high voltage circuit.

Caution must be exercised during the replacement or servicing of the tube since a residual electrical charge is stored within the tube. Before handling the tube remove any undersible residual high voltage charge from the tube, by shorting the anode contact button to the frame of the terminal as illustrated in figure #2. Discharging the high voltage to isolated metal parts sucha as cabinets and control brackets may produce a shock hazard.

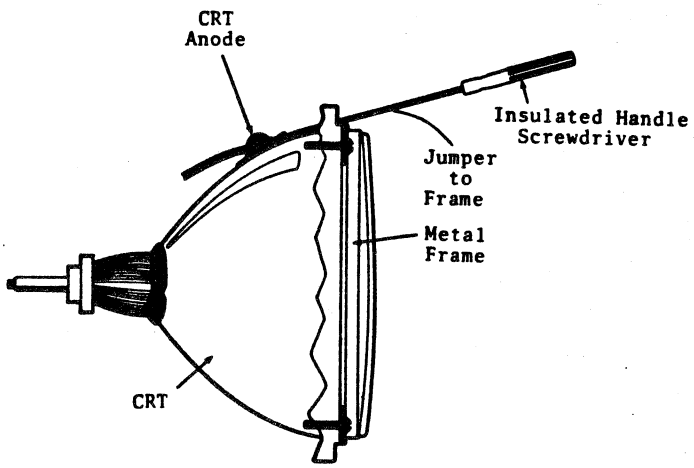
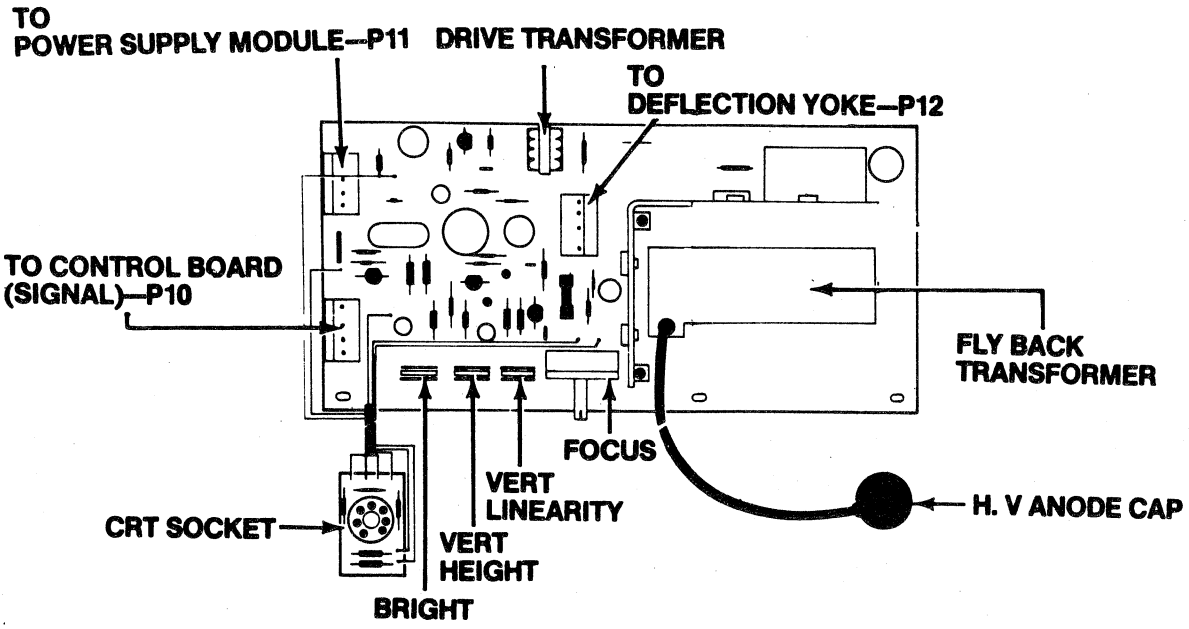
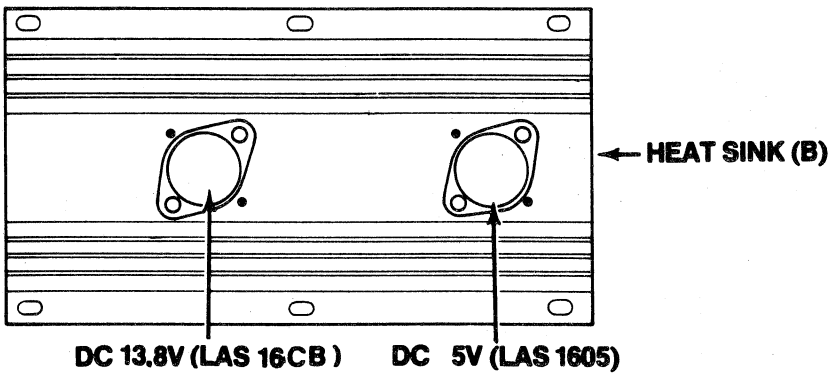
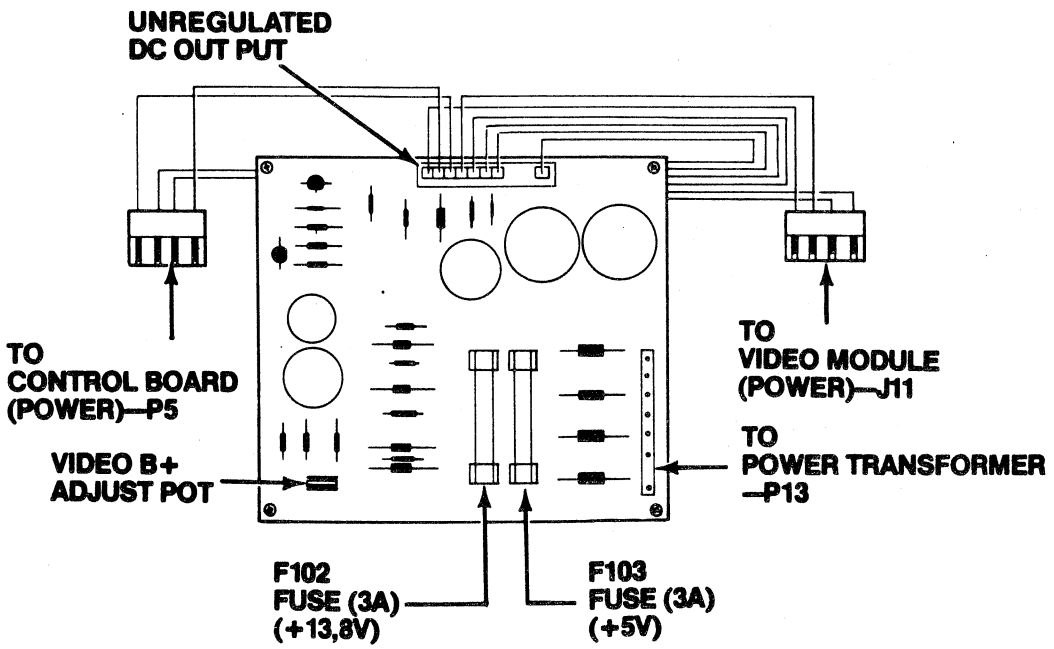


Figure 2.



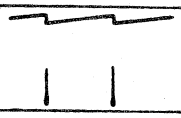
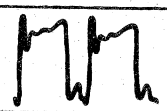
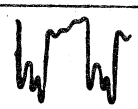
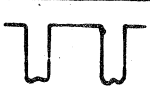
VIDEO MONITOR MODULE





POWER SUPPLY MODULE

TR WAVEFORM and VOLTAGE

Transistor			Base(In)			Collector(Out)			Emitter(GND)		
Location	Parts	Function	Vtg DC V	Vtg AC Vp-p	Wave Form	Vtg DC V	Vtg AC Vp-p	Wave Form	Vtg DC V	Vtg AC Vp-p	Wave Form
(IC)	LAS1512	Regulation	12	2.5		12	0.0	—	0.0	0.0	—
(IC)	LAS1605	〃		1.6		5	0.0	—	0.0	0.0	—
(IC)	LAS1812	〃		0.1		-12	0.0	—	0.0	0.0	—
(IC)	LAS16CB	〃		1.4		13.8	0.0	—	0.0	0.0	—
Q102	2SC509	〃	78.7	0.0	—	86.4	1.5		98.0	0.0	—
Q103	2SC983	〃	12.0	0.0	—	75.7	0.0	—	11.9	0.0	—
Q201	2SA495	Vert Pree Drive	2.0	3.0		0.6	0.57		1.0	1.7	
Q202	2SC372	Vert Drive	0.68	0.5		8.0	6.5		0.0	0.0	—
Q203	2SC1173	Vert Out	9.36	6.5		12	0.0	—	8.76	6.5	
Q204	2SA473	Vert Out	8.0	6.5		0.0	0.0	—	8.6	6.5	
Q301	2SC735	Horiz Drive	-0.25	0.64		12	20		0.0	0.0	—
Q302	2SC2233	Horiz Out	-0.08	6		12.8	124		0.0	0.0	—
Q501	2SC963	Video Amp	0.4	3		76.8	25		-0.8	2.8	
D302	DS-113A	Damping	12.8	132							

DC Voltage reading taken with VTVM from point indicated to chassis ground.

AC Voltage reading taken with Oscilloscope from point indicated to chassis ground

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

V-HEIGHT V-LINEARITY

VE
VIDEO IN
VR1 500 B
HO
CONTRAST
P10
R201 2.7K
SFR1 100K
R202 100K
C201 10U 16V
R203 2.2K
Q201 KTA1015
C202 4.7U 16V
R205 2.7K
C203 22U/10V
R206 820 1/2
SFR2 2K B
C204 4.7U 16V
R207 6.8K
R204 0.6 (2W)
SDT-100 TH-201
R208 4.7K
R209 4.7K
Q202 KTC1815
C205 100U 10V
C206 22U 10V
R210 330
R211 150
Q203 2SC1173
E1
D202
R212 0.6 (2W)
D201
R213 0.6 (2W)
C207 2200U 10V
Q204 2SA473
C209 0.01U
J12
V. YOKE
C208 0.047
R214 270
KYS-00060 L202
H. YOKE
L201 LINEARITY COIL
C306 16 U F 25V NP
R501 47
Q501 2SC983
BRIGHT
JP7
R506 220 1/2
SG 501 SPARK GAP
V501 310JLB4N (B/W) 310KGB3IN (GREEN)
H3 O
H4 O
R507 1.5K 1/2
R508 10K 1/2
JP8
JP6
C501 220P
R502 90
R503 820 1/2
R504 56K
SFR4 100KB
C503 0.01U
R505 47K
C505 22U 100V
R505 1.5K 1/2
ANODE
GND
JP5
JP9
FOCUS
VR2 2M B
C504 0.1U 600V
C506/0.47U
IN914 D501 OR KDS 1553
C502 0.01 50V
E2
L302 27UH
C305 220U 16V
C303 0.0068U/200V
H4 H3 HEATER
DRIVE TRANS
Q302 2SC2233
C307 0.039U
R301 470
Q301 2SC1166 OR KTC 200
C301 4.7U 16V
T301 HDT-19
C302 0.01U
D301 KDS8513A
D302 DSI13A
C304 0.047U 400V
T302 FBT KFS-00093
D502 DSI35B OR DSI30TB
J11

POWER SELECT SWITCH SW102
230V
115V
R101 2.2M (1/2W)
F101 FUSE 1A
SW101 POWER SWITCH
POWER TRANS T101
F103 FUSE 3A
F102 FUSE 3A
K2
K1
D105~D108 DSA17C
C105~C108 0.01UX4
D101 D102 D103 D104 DSA17C
DSI35DX2
D113
D114
C117 4700U/16V
C113 3300U 35V
IC2 LAS1605
C114 0.33U 35V
IC1 LAS16CB
C115 0.33U 35V
R102 390
C116 470U 35V
D112 EQA 02-12
C101-C104 0.01UX4
D109 DSI35D
C109 0.01U
Q102 KTC1627A
R105 4.7K
R106 4.7K
R107 3.9K
R110 30K
C118 100U 160V
C120 22U 160V
D111 EQA02.12
Q103 2SC983
R108 27K
SFR3 5K
R109 2.7K
-12V GND 5V 12V
J5

1	Vp-p 0.7	2	Vp-p 6.5	3	Vp-p 6.5	4	Vp-p 2.0	5	Vp-p 124

B C E
2SC1173 2SA473 2SC2233
E C B
2SC983 2SC1166
B C E
2SA495 2SC372
LAS1605 LAS16CB
KTC1627A KTA1015 KTC1815

1. ALL RESISTANCE VALUES IN OHM K=1,000 M=1,000,000.
2. ALL CAPACITOR VALUES IN FARAD U=10^{-6} P=10^{-12}
3. UNLESS OTHERWISE STATED, WORKING VOLTAGES OF CAPACITORS ARE 50 VOLTS.
4. THIS SCHEMATIC DIAGRAM COVERS BASIC OR REPRESENTATIVE CHASSIS ONLY. THERE MAY BE SOME COMPONENT OR PARTIAL SCHEMATIC DIFFERENCE BETWEEN ACTUAL CHASSIS AND THE SCHEMATIC DIAGRAM.

QTY REQD	FSCM NO.	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION
			PARTS LIST	

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	DWN H.H.W 3/8/83	TeleVideo, Inc.
NEXT ASSY	USED ON	ANG 2 PLC 3 PLC	CHK	
		. . . .	ENGR S.M.Kim 3/8/83	
		SCALE:	APPD	TITLE PCB SCHEMATIC DIARAM POWER SUPPLY VIDEO MONITOR
		MATERIAL	APPD	
			APPD	
			FINISH	SIZE D SHT 1 OF 1 DRAWING NO. 2281900 REV

DWG NO. 2281900 | SHT 1 | REV

BISHOP GRAPHICS INC

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
1										R101	2.2M Ohm 1/2W CFR	2186500
2										R102	390 Ohm 1/2W CFR	2186100
3										R105,106,208	4.7K Ohm 1/4W CFR	2053100
4										R107	3.9K Ohm 1/4W CFR	2177400
5										R108	27K Ohm 1/4W CFR	2037300
6										R109,201,205	2.7K Ohm 1/4W CFR	2038300
7										R110	30K Ohm 1/4W CFR	2039300
8										R202	100K Ohm 1/4W CFR	2032100
9										R203	2.2K Ohm 1/4W CFR	2038700
10										R204,212,213	0.6 Ohm 2W Wire Wound Res	2177100
11										R206,503	820 Ohm 1/2W CFR	2186200
12										R207	6.8K Ohm 1/4W CFR	2039100
13										R209,505	47K Ohm 1/4W CFR	2033700
14										R210	330 Ohm 1/4W CFR	2051500
15										R211	150 Ohm 1/4W CFR	2033900
16										R214	270 Ohm 1/4W CFR	2051300
17										R301	470 Ohm 1/4W CFR	2051700
18										R501	47 Ohm 1/4W CFR	2037700
19										R502	90 Ohm 1/4W CFR	2177600
20										R504	56K Ohm 1/2W CFR	2039500
21										R506	220 Ohm 1/2W CFR	2186000

NOTES:

TITLE VIDEO MONITOR POWER SUPPLY AND PARTS LIST DATE 1-13-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
22										R507,509	1.5K Ohm 1/2W CFR	2186300
23										R508	10K Ohm 1/2W CFR	2186400
24										SFR1, 4	100K Ohm Pot	2177700
25										SFR2	2K Ohm Pot	2177800
26										SFR3	5K Ohm Pot	2177900
27										VR1	500 Ohm Pot	2180200
28										VR2	2M Ohm Pot	2180100
29										TH201	1.1K Ohm Thrumistor	2180300
30										C101-109	0.01uF 16V Ceramic 20%	2028700
31										C113	3,300uF 35V Electrolytic	2196500
32										C114,115	0.33uF 35V Tantal	2198100
33										C116	470uF 35V Electrolytic	2198200
34										C117	4700uF 16V Electrolytic	2196600
35										C119	110uF 160V Electrolytic	2196300
36										C120	22uF 160V Electrolytic	2196400
37										C201	10uF 16V Electrolytic	2027300
38										C202,204	4.7uF 16V Tantal	2027500
39										C203	22uF 15V Electrolytic	2025700
40										C205	100uF 10V Electrolytic	2196000
41										C206	22uF 10V Electrolytic	2196100
42										C207	2200uF 10V Electrolytic	2196200

NOTES:

TITLE: VIDEO MONITOR POWER SUPPLY AND PARTS LIST

DATE: 1-13-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
43										C208	0.047uF/50V Mylar	2197100
44										C209	0.001uF/50V Mylar	2196900
45										C301	4.7uF/16V Electrolytic	2196700
46										C302	0.01uF/50V Mylar	2197000
47										C303	0.0068uF/200V Mylar	2196800
48										C304	0.047uF/400V Mylar	2197500
49										C305	220uF/16V Electrolytic	2199300
50										C306	16uF/25V NP	2280000
51										C307	0.039uF/50V Monolythic	2030500
52										C501	220PF 50V Ceramic	2195900
53										C502	0.01u 50V	2197000
54										C503	0.01uF 50V Monolythic	2028900
55										C504	0.1uF 600V Mylar	2197300
56										C505	22uF 100V Electrolytic	2196100
57										C506	0.47uF 50V Mylar	2197200
58										SG501	1KV Spark Gap	2030900
59										SW101	SPST 115V 10A/230V 5A Pwr SW	2097300
60										SW102	DPDT 115V/230V Power Line	2097400
											Slide Switch	
61										F101	1A/250V	2097000
62										F102,103	3A/125V	2193100

NOTES:

TITLE
VIDEO MONITOR POWER SUPPLY ABD PARTS LIST

DATE
1-13-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
63										M003	Fuse Clip	2180400
64										Q102	KTC 1627A or MPS-A06	2046700
65										Q103,501	2SC983 or 2N5551	2193200
66										Q201	KTA 1015 or 2N3906	2042200
67										Q202	KTC11815 or 2N3904	2046500
68										Q203	2SC1173 or 2N6121	2199700
69										Q204	2SA473 or 2N6124	2202100
70										Q301	KTC 200(2SC1166) or 2N4401	2045500
71										Q302	2SC2233 or MJE13006	2047300
72										IC1	LAS 16CB 13.8V Regulator	2126900
73										IC2	LAS 1605 5V Regulator	2126800
74										V501	B & W P4 12"	2049100
75										V501	CRT Green P31 12"	2049300
76										D101-108	DS 135D or 1N5391 Rectifier	2200600
77										D109	DS 135D Rectifier	2201400
78										D111,112	EQA01-12 or IN759A Zener	2201600
											Diode	
79		1								D302	DS-113A or MRI-1000 Damper	2201700
											Diode	
80										D501	IN914 or KDS1553 Switching	2047500
											Diode	

NOTES:

TITLE VIDEO MONITOR POWER SUPPLY AND PARTS LIST DATE 1-13-83

TeleVideo Systems, Inc.

ITEM/ FIND NO.	QTY PER ASSM/REV LEVEL									REFERENCE/ DESIGNATOR	NOMENCLATURE/DESCRIPTION	PART NUMBER/REMARKS
81										D502	DS-130TB or IN4004 600V	2202200
											Rectifier	
82										D201,202,301	KDS-8513A or IN920 Silicon	2201800
											Diode	
83										D113,114	DS 135D Rectifier	2200600
84										L202	KYS-00060 D.Y Coil	2200800
85										L201	5.4uH Linearity Coil	2200900
86										L201	Adjustable Linearity Coil	2213600
87										L302	27uH Inductor Coil	2201000
88										T101	Power Transformer	2201100
89										T301	Drive Transformer	2201200
90										T302	Flyback Transformer	2201300

NOTES:

TITLE: VIDEO MONITOR POWER SUPPLY AND PARTS LIST

DATE: 1-13-83

TeleVideo Systems, Inc.

TERMINAL TROUBLESHOOTING GUIDE

Document 2191400
Revision B

28 February 1983

Disclaimer

TeleVideo® Systems, Inc.
1170 Morse Avenue
Sunnyvale, California 94086

1. INTRODUCTION

This is a general troubleshooting guide to be used with the Operator's Manual, Maintenance Manual, and Service Bulletins as required. By following the procedures described here, you should be able to quickly isolate and repair most field failures.

The following sections are included:

2. OVERVIEW OF TERMINAL MODULES

The design of TeleVideo® terminals permits fast fault isolation since the terminal hardware is divided into four main modules:

1. Video monitor
2. Power supply
3. Main logic board
4. Keyboard

The video monitor and power supply are common to all TeleVideo terminals and may be freely interchanged. Terminal keyboards are interchangeable, as outlined in the section on the keyboard. The main logic board is the only module that provides each terminal with its unique characteristics.

The quickest and easiest way to isolate the malfunctioning module is to exchange (swap) each module with a known good module. Once the faulty module is identified, refer to the appropriate troubleshooting table.

WARNING!

High voltages are retained by the CRT tube and capacitors even after power has been turned off. As soon as you open the case, clip one end of a wire to the chassis. Attach the other end of the wire to an insulated screwdriver. Being careful not to touch the metal part of the screwdriver, gently slip the metal end of the screwdriver under the cap of the anode, as shown in Figure 2-1.

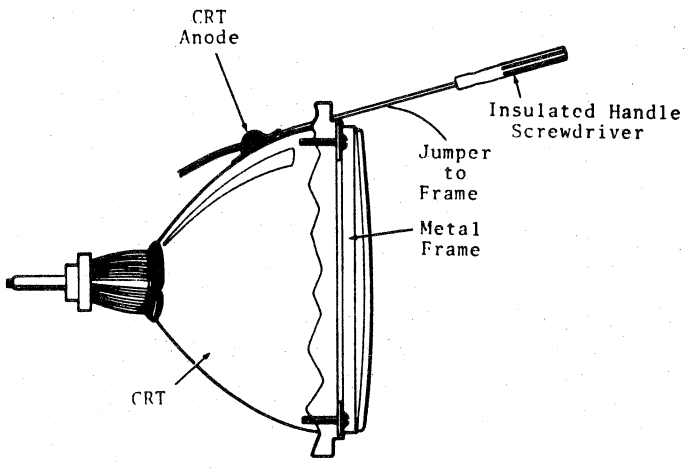


Figure 2-1 Discharging Voltages

3. FUNCTIONAL DESCRIPTION OF MODULES

Logic Board

The logic board processes and controls all data received and transmitted, and generates the video and sync signals required to display data.

The logic board consists of the following five functional areas:

1. Display processor
2. Display generator
3. Keyboard interface
4. Main port interface
5. Printer port interface

Power Supply

The power supply provides DC operating voltages to all circuits in the terminal. The power supply contains two user-replaceable 3 AG-type fuses.

Video Monitor

The video monitor contains horizontal, vertical, and intensity modulation circuits which produce a television-type conventional noninterlaced raster display on the screen. Character signals received from the display generator cause intensified dots to appear at precise intervals on a raster line. These dots, when combined with other dots on other raster lines above and/or below a given line, produce characters.

Keyboard

910/910 PLUS/912C/920C--This keyboard sends matrixed data via a ribbon cable to the logic board, where the ASCII code is generated.

This data is encoded in the 910/910 PLUS by the keyboard encoder (position A1) and in the 912C/920C by the CPU (position A54) and the multiplexers (positions A68 and A69).

The keyboards for these models are all functionally interchangeable. The 910/910 PLUS keyboard has a PRINT keycap where 912C/920C models have a BLOCK/CONV keycap. The 920C keyboard is also fitted with an additional top row of function and editing keys.

925/950--On this keyboard, data is encoded by a microprocessor on the keyboard (position U6) and sent in an ASCII serial data stream to the logic board via the coiled cable. On the logic board, the keyboard interface circuits convert the keyboard data from serial to parallel data for input to the display processor circuitry. All detachable keyboards are identical and interchangeable.

4. TROUBLESHOOTING THE LOGIC BOARD

Visual Inspection

With the Logic Board Installed--Turn off power to the terminal, open the case, and check the following possible problem areas:

* Internal and external switch settings: are they all correct?

* Socketed chips: are they all plugged tightly into their sockets?

* Connectors: look for

  Loose or damaged connectors

  Broken or loose securing clips on pins at connectors

  Bad crimps

  Dirty contacts

* Wires: are any broken, loose, or frayed?

* Components: are any overheated or burned?

With the Logic Board Removed--Make these inspections with the logic board removed. The procedure for removing the logic board varies slightly according to the model. Follow the appropriate directions for your model.

910/910 PLUS/912C/920C

To remove the logic board:

1. Turn the power off.

2. On the logic board, disconnect:

   P1 (keyboard input)
   P2 (video signals)
   P3 (RS232C port) if connected
   P4 (printer port) if connected
   P5 (voltage connector)
   P6 (modem connector) if connected
   P7 (speaker connector)

3. Remove the four (910/910 PLUS) or six (912C/920C) securing screws on the logic board.

4. Carefully remove the logic board.

1. Turn the power off.

2. On the logic board, disconnect:

   P1 (keyboard input)
   P3 (RS232C port) if connected
   P4 (printer port) if connected
   P6 (modem connector) if connected

3. Carefully slide the logic board half way out of the terminal and disconnect:

   P2 (video signals)
   P5 (voltage connector)

4. Carefully slide the logic board entirely out of the terminal.

With the logic board removed, inspect the logic board for:

* Overheated or burned components
* Missing or broken components
* Cracked, broken, or lifted traces
* Poor solder joints (loose solder balls, cold solder joints, or solder bridges)
* Bent pins

STOP!

If defects are found, correct them and recheck the terminal before continuing.

If no defects are found, reinstall the logic board before proceeding with the procedures in the next section, Large Scale Integration Failures.

Large Scale Integration Failures

Since most failures involve Large Scale Integration (LSI) chips, this step will quickly repair most failures encountered. Exchange all socketed chips, one at a time, with known good chips. If the logic board malfunctions after the chips are swapped, confirm the operation of the data lines described in the next section, Data Line Operation.

NOTE!

The remainder of this guide involves troubleshooting to the component level and requires schematics, an oscilloscope, a working knowledge of transistor-transistor logic (TTL), and basic debugging skills.

Data Line Operation

Confirm that the data lines are operating properly before proceeding further.

NOTE!

It is beyond the scope of this bulletin to list all possible data line problems.

The best place to check the data lines is directly from the CPU (see page 1 of the schematics). There should be activity on all data lines and the signals should range from 0 (ground) to +4.5 to +5.0 volts. If the malfunction persists after you have confirmed proper operation of the data lines, follow the procedures in the next section, Debugging Tables.

Debugging Tables

NOTE!

The items listed in the tables in this section are only suspect areas; they should not be automatically replaced when the symptoms listed are present.

Table 4-1 910/910 PLUS Logic Board Debugging Guide

Symptom	Suspect Areas Part No.	Position	Schematic Page
No video	6502	A39	1 of 5
	6545	A26	2 of 5
	2114	A30, A31, A36, A37	2 of 5
	or		
	6116	A24	2 of 5
	Crystal	Y2	3 of 5
	74LS163	A15	3 of 5
	2332	A45	1 of 5
	2N2219	Q2	4 of 5
Distorted video	6502	A39	1 of 5
	6545	A26	2 of 5
	6116	A24	2 of 5
	or		
	2114	A30, A31, A36, A37	2 of 5
	2332	A48	3 of 5
	74LS166	A49	3 of 5
Horizontal bar across screen	6545	A26	2 of 5
	74S04	A22	4 of 5
Loss of underline, reverse video, blinking, or blanking	74LS174	A42	3 of 5
	6545	A26	2 of 5
Loss of half intensity	74LS175	A41	3 of 5
	6545	A26	2 of 5
Loss of all attributes	6545	A26	2 of 5
	74S74	A40*	3 of 5
Unable to transmit data	75188	A10	4 of 5
	6551A	A19	4 of 5
Unable to receive data	75189	A5	4 of 5
	6551A	A19	4 of 5
Poor/no printing	75189	A5	4 of 5
	75188	A10	4 of 5
	6551A	A19	4 of 5
Incorrect/no keyboard response	AY-5-3600	A1	5 of 5
	2716	A2**	5 of 5

Notes
*Must be a Texas Instruments part.
**If used.

Table 4-1 Continued

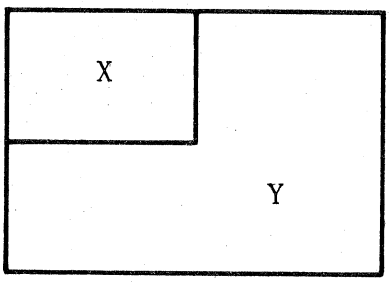
Symptom	Suspect Areas Part No.	Position	Schematic Page
SHIFT or CTRL keys do not function	A6-5-3600	A1	5 of 5
	7406	A12	5 of 5
	RP4		5 of 5
ALPHA LOCK or FUNCT keys do not function	AY-5-3600	A1	5 of 5
	74LS364	A8	5 of 5
	RP4		5 of 5
Keys repeat	AY-5-3600	A1	5 of 5

*Must be a Texas Instruments part.
**If used.

Table 4-2 912/920 Logic Board Debugging Guide

Symptom	Suspect Areas Part No.	Position	Schematic Page
No video, no beep	8035	A54	1 of 6
	5027	A23	4 of 6
	23.814-MHz Crystal	X1	4 of 6
	74LS109	A56	4 of 6
	74LS163	A57	4 of 6
	System ROMs	A49	2 of 6
	System ROMs	A50*	2 of 6
	2332	A3	5 of 6
No video, constant beep	5027	A23	4 of 6
	2114 RAM, page 1	A6, A8, A10, A12	3 of 6
	2114 RAM, page 2	A5, A7, A9, A11	3 of 6
Horizontal bar across screen	5027	A23	4 of 6
	74LS08	A32	5 of 6
	74LS05	A14	5 of 6
Bad video or incorrect character displayed in:			
Area X of screen**	2114 RAMs	A8	3 of 6
	2114 RAMs	A12	3 of 6
Area Y of screen**	2114 RAMs	A6	3 of 6
	2114 RAMs	A10	3 of 6
Bad video on entire screen	74LS157	A24, A25, A26	3 of 6
	74LS00	A40	3 of 6
	8035	A54	1 of 6
	5027	A23	4 of 6

Notes
* If installed
**



Areas X and Y of Screen

Table 4-2 Continued

Symptom	Suspect Areas Part No.	Position	Schematic Page
Distorted characters	2316	A3	5 of 6
	8035	A54	1 of 6
	2114 RAMs	A5 through A12	3 of 6
Unable to transmit	75188	A59	2 of 6
	74LS157	A78	2 of 6
	2502	A48	2 of 6
Unable to receive	75189	A60	2 of 6
	74LS157	A78	2 of 6
	2502	A48	2 of 6
Loss of blinking or blanking	74LS74	A35	4 of 6
	5027	A23	4 of 6
Loss of half intensity	74LS74	A16	5 of 6
	74LS03	A15	5 of 6
	5027	A23	4 of 6
Loss or underlining/reverse video	74LS74	A28	5 of 6
	74LS74	A29	5 of 6
	5027	A23	4 of 6
Incorrect or no keyboard input	8035	A54	1 of 6
	74LS253	A68	1 of 6
	74LS253	A69	1 of 6
ALPHA LOCK, SHIFT, CTRL, or Function keys do not function	74LS364	A76	1 of 6
	74LS42	A58	1 of 6
Unable to select one or more baud rates	74LS163 Counter	A70 through A73	6 of 6
	Baud rate switch	S1	6 of 6
	74LS00 Nand Gate	A74	6 of 6

Table 4-3 925 Logic Board Debugging Guide

Symptom	Suspect Areas Part No.	Position	Schematic Page
No beep, no video	13.6080-MHz Crystal	Y2	7 of 7
	74LS00	A55	4 of 7
	74LS139	A37	4 of 7
	6502A	A60	1 of 7
	6545A-1	A59	2 of 7
Constant beep, no video	6502A	A60	1 of 7
	6545A-1	A59	2 of 7
	74LS223	A44	7 of 7
Horizontal bar	74504	A16	7 of 7
	6545A-1	A59	2 of 7
Bad video	10uf cap	C41	1 of 7
	74LS74	A6	4 of 7
	6545A-1	A59	2 of 7
Distorted characters	74LS166	A30	2 of 7
	2332	A31	2 of 7
Unable to transmit to computer	75188	A34	5 of 7
	6551	A32	5 of 7
	74LS32	A26	5 of 7
Unable to receive from computer	75189	A9, A17	5 of 7
	6551	A32	5 of 7
Unable to transmit to printer	75188	A34, A25	5 of 7
	74LS32	A26	5 of 7
	6551	A32	5 of 7
Unable to receive from printer	75189	A9, A19	5 of 7
	74LS32	A26	5 of 7
	75188	A25	5 of 7
Loss of any video attribute	74LS173	A19, A20, A21	3 of 7
	74LS245	A40	2 of 7
	74LS374	A39	2 of o7
	2332	A50, A49	1 of 7
No keyboard communication*	1.8432-MHz Crystal	Y1	5 of 7
	6551	A33	5 of 7
	6502A	A60	1 of 7

*Refer also to Service Bulletin 2, Eliminating Keyboard Lockup

Table 4-3 Continued

Symptom	Suspect Areas Part No.	Position	Schematic Page
Unable to select switch bank S1	Switch	S1	6 of 7
	74LS244	A53, A52	6 of 7
	Resistor pack	RP5	6 of 7
Unable to select switch bank S2	Switch	S2	6 of 7
	74LS244	A51, A52, A53	6 of 7
	Resistor pack	RP1	6 of 7
Unable to select switch bank S3	Switch	S3	6 of 7
	74LS244	A43, A51,	6 of 7
	Resistor pack	RP4	6 of 7

Table 4-4 950 Logic Board Debugging Guide

Symptom	Suspect Areas Part No.	Position	Schematic Page
No video, no beep	6502	A53	1 of 7
	6551	A49, A50 A51	5 of 7
	6545	A56	2 of 7
	Program ROMs	A41, A42	1 of 7
	User ROMs	A52	1 of 7
	Character Generator ROMs	A32, A33	4 of 7
	23.824-MHz Crystal	OSC1	6 of 7
	74LS163	A3	6 of 7
	74LS109	A6	6 of 7
No video, constant beep	6545	A56	2 of 7
	2114 RAMs	A25, A26, A27, A28	3 of 7
Horizontal bar across screen	6545	A56	2 of 7
	2114 RAMs	A25, A26, A27, A28	3 of 7
Bad video, one section of screen	2114	A25	3 of 7
	2114	A26	3 of 7
	2114	A27	3 of 7
	2114	A28	3 of 7
Bad video on only one page			
Page 1	6116	A37	3 of 7
Page 2	6116	A34	3 of 7
Page 3	6116	A35	3 of 7
Page 4	6116	A36	3 of 7
Bad video on entire screen	74LS157	A43 through A46	2 of 7
	6545	A55	2 of 7
	6502	A53	1 of 7
Distorted characters	2332	A32, A33	4 of 7
	74LS166	A22, A23	4 of 7
	6502	A53	1 of 7
	All 2114's	A25 through A28	3 of 7

Table 4-4 Continued

Symptom	Suspect Areas Part No.	Position	Schematic Page
Unable to transmit to system	1488	A48	5 of 7
	74LS32	A58	5 of 7
	6551	A50	5 of 7
	74LS157	A59	5 of 7
Unable to receive from system	1489	A57	5 of 7
	74LS08	A29	5 of 7
	6551	A51	5 of 7
Unable to transmit to printer	1488	A39	5 of 7
	74LS32	A58	5 of 7
	6551	A51	5 of 7
	74LS157	A59	5 of 7
Unable to receive from printer	1489	A40	5 of 7
	6551	A51	5 of 7
Loss of any video attribute	74LS174	A19	4 of 7
	74LS157	A20	4 of 7
	74LS174	A21	4 of 7
Incorrect or no keyboard input	6502	A53	1 of 7
	6551	A49	3 of 7
Unable to select one or more baud rates	6502	A53	1 of 7
	6552	A54	7 of 7
	74LS367	A65, A66	7 of 7
	RP 2		7 of 7
	RP 3		7 of 7
	Switch 1		7 of 7

"Gate Array" Logic board, Supplement Debugging Guide

Although the components are laid out differently, "Gate Array" boards are completely interchangable with TTL boards. When troubleshooting the "Gate Array" Logic boards care should be taken when handling the CMOS devices. The "Gate Array" chip positions are listed below. When exchanging these custom CMOS chips one must be grounded to earth ground to avoid damage to the chip from static discharge.

Model No.	Televideo Part Number	Location
910, 910Plus	2057400	A22
925	2057400	A39
950, Chip A	2057600	A34
Chip B	2057800	A37

Follow the procedure in the begining of this section for a visual inspection of the logic board.

Table 4-5 910/910 PLUS GA Logic Board Debugging Guide

Symptom	Suspect Areas Part No.	Position	Schematic Page
No video	6545A-1	A20	2 of 5
	6502	A27	1 of 5
	6116	A13	2 of 5
	Crystal	Y2	3 of 5
	2532	A38	1 of 5
	74LS163	A25	3 of 5
	74LS166	A18	3 of 5
	2N2219	Q2	4 of 5
	70200-11B	A22	3 of 5
Distorted video	6545A-1	A20	2 of 5
	6116	A13	2 of 5
	70200-11B	A22	3 of 5
	74LS166	A18	3 of 5
	2532	A38	1 of 5
Horizontal Bar across screen	6545A-1	A20	2 of 5
	74LS08	A37	2 of 5
Loss of Attribute	70200-11B	A22	3 of 5
	6545A-1	A20	2 of 5
Unable to Transmit to Computer or printer	75188	A9	4 of 5
	6551A-1	A15	4 of 5
Unable to Receive from Computer or printer	75189	A10	4 of 5
	6551A-1	A15	4 of 5
Inncorect/ no keyboard response	AY-5-3600	A1	5 of 5
	2716	A2	5 of 5
	74LS367	A3,A8	5 of 5
Shift or CTRL keys inoperative	AY-5-3600	A1	5 of 5
	7406	A7	5 of 5
	resistor pack	RP2	5 of 5
Alpha Lock or Funct keys inoperative	AY-5-3600	A1	5 of 5
	74LS367	A8	5 of 5
	resistor pack	RP2	5 of 5
Repeating keys	AY-5-3600	A1	5 of 5

Table 4-6 925 GA Logic Board Debugging Guide

Symptom	Suspect Areas Part No.	Position	Schematic page
No video/ no beep	Crystal	Y2	6 of 6
	70200-11A	A39	3 of 6
	74LS139	A38	3 of 6
	6502	A11	1 of 6
	6545A-1	A28	2 of 6
Constant beep/ no video	6545A-1	A28	2 of 6
	74LS273	A26	6 of 6
	6502	A11	1 of 6
Horizontal bar across screen	6545A-1	A28	2 of 6
	74S04	A40	3 of 6
Bad video	10uF cap	C28	1 of 6
	6545A-1	A28	2 of 6
	70200-11a	A39	3 of 6
Distorted characters	2332	A17	2 of 6
	74LS166	A12	2 of 6
Loss of Attribute	70200-11A	A39	3 of 6
	2333	A14,A15	1 of 6
No transmit to computer or printer	75188	A23	4 of 6
	6551A-1	A4	4 of 6
	74LS32	A24	4 of 6
No receive from computer or printer	75189	A2	4 of 6
	6551A-1	A4	4 of 6
No keyboard response	Crystal	Y3	4 of 6
	6551A-1	A5	4 of 6
	6502	A11	1 of 6
Unable to select S1	Switch	S1	5 of 6
	74LS244	A3,A41	5 of 6
	resistor pack	RP1	5 of 6
Unable to select S2	Switch	S2	5 of 6
	74LS244	A3,A41, A34	5 of 6
	resistor pack	RP2	5 of 6
Unable to select S3	Switch	S3	5 of 6
	74LS244	A34,A29	5 of 6
	resistor pack	RP4	5 of 6

Table 4-7 950 GA Logic Board Debugging Guide

Symptom	Suspect Areas		Schematic
	Part No.	Position	Page
No video/ no beep	6502	A11	1 of 7
	6551	A29,A33	5 of 7
		A36	
	6545	A6	2 of 7
	740012	A34	4 of 7
	2532	A20,A25	1 of 7
	2332	A30,A31	4 of 7
	Crystal	OSC 1	4 of 7
No video/ constant beep	6545	A6	2 0f 7
	6116	A3	3 of 7
Horizontal bar across screen	6545	A6	2 of 7
	7406	A39	6 of 7
Bad video	6116	A8,A13	3 of 7
		A17,A22	3 of 7
	74LS157	A7,A12	2 of 7
		A16,A21	2 of 7
	6545	A6	2 of 7
	6502	A11	1 of 7
	740012	A34	4 of 7
Distorted characters	2332	A30,A31	4 of 7
	740012	A34	4 of 7
	740012	A37	6 of 7
Loss of Attributes	740012	A34	4 of 7
Unable to transmit to computer	75188	A18	5 of 7
	74LS32	A19	5 of 7
	6551	A29	5 of 7
	74LS157	A28	5 of 7
Unable to receive from computer	75189	A9	5 of 7
	740012	A37	6 of 7
	6551	A29	5 of 7
Unable to transmit to printer	75188	A23	5 of 7
	74LS32	A24	5 of 7
	6551	A33	5 of 7
	74LS157	A28	5 of 7
Unable to receive from printer	75189	A32	5 of 7
	6551	A33	5 of 7
Inncorect/ no keyboard response	6551	A36	5 of 7
	6502	A11	1 of 7
	74LS32	A19	5 of 7

Table 4-7 continued

Symptom	Suspect Areas Part No.	Position	Schematic Page
Unable to select S1	Switch	S1	7 of 7
	resistor pack	RP1,RP2	7 of 7
	74LS367	A1,A4	7 of 7
	6552	A43	7 of 7
	6502	A11	1 of 7
Unable to select S2	Switch	S2	7 of 7
	resistor pack	RP2	7 of 7
	74LS367	A4,A38 A42	7 of 7
	6552	A43	7 of 7
	6502	A11	1 of 7

5. TROUBLESHOOTING THE KEYBOARD

Visual Inspection

With the Keyboard Installed--Turn off power to the terminal. Check keyboard alignment; are any keys binding on the cover?

Open the top case.

910/910 PLUS/912/920

Remove the two screws from the bottom front corners of the terminal. Carefully tip the top case back until it rests on a firm surface.

NOTE!

The terminal will now be top heavy and may tip over if there is not sufficient table space to support the top.

925/950

Remove the four screws from the bottom of the keyboard case. Carefully life off the top of the keyboard case and set it aside.

Check the following areas:

* Key switches:

  Foreign objects (e.g., paperclips, staples, matches)

  Liquid residue (e.g., coffee, soft drinks)

  Broken keyswitches

  Missing or incorrectly placed keycaps

* Cables:

  Broken wires

  Loose wires at connectors

  Creased, kinked, or cut cables

* Connectors:

  Loose or damaged connectors

  Bent pins

  Dirty contacts

NOTE!

If defects are found, correct them and recheck the terminal before continuing.

With the Keyboard Removed--Make the following inspections with the keyboard removed from its case. The procedure for removing the keyboard varies slightly according to the model.

910/910 PLUS/912/920

To remove the keyboard:

1. Unplug the ribbon cable from the logic board.
2. Remove the two securing screws and washers from the inner bottom corners of the keyboard.
3. Carefully remove the keyboard from the surrounding case.

925/950

To remove the keyboard:

1. Disconnect on the keyboard:

   P6 (speaker connector)
   P7 (keyboard cable)

2. Remove the four screws from the bottom corners of the keyboard case.
3. Carefully remove the keyboard from the bottom case.

Inspect the keyboard for:

* Overheated, damaged, or burned components
* Cracked, shorted, broken, or lifted traces
* Poor solder joints (loose solder balls, cold solder joints, or solder bridges)
* Broken, loose, or frayed wires

NOTE!

If any defects are found, correct them and recheck before continuing.

Table 5-1 Keyboard Debugging Guide

Symptom	Suspect Areas	Models
One key inoperative/ intermittent	Respective keyswitch	A
	Open trace/bad solder joint	A
	8048 keyboard CPU, position U6	B
Several keys inoperative/intermittent	Open/shorted trace	A
	Broken/loose jumper	A
	Defective ribbon cable	C, D
	Bent pin at ribbon cable connectors	C, D
	8048 keyboard CPU, position U6	B
	10K ohm resistor packs, positions RP2, RP3	B
	10K ohm resistor, position R3	B
All keys inoperative	Open/shorted trace	A
	Defective ribbon or keyboard cable	A
	8048 keyboard CPU, position U6	B
	7805 +5V regulator, position V1	B
	5.7143-MHz crystal, position X1	B
SHIFT, FUNCT, or ALPHA LOCK keys	10K ohm resistor pack, position RP2	
	8048 keyboard CPU, position U6	B
CTRL key inoperative	10K ohm resistor pack, position R2	
	8048 keyboard CPU, position U6	B
Incorrect characters	Shorted trace	A
	Shorted/improperly plugged ribbon cable	C, D
	8048 keyboard CPU, position U6	B

Legend
A = All
B = 925/950
C = 910/910 PLUS
D = 912/920

Table 5-1 Continued

Symptom	Suspect Areas	Models
Keys repeat	Respective keyswitch*	B, D
	Shorted trace	A
	Shorted ribbon cable	C, D
	8048 keyboard CPU, position U6	B

Legend
A = All
B = 925/950
C = 910/910 PLUS
D = 912/920

Note
*On the 910/910 PLUS terminals, a key which is shorted will not repeat on power up. Instead, any key pressed will repeat until another key is pressed.

6. TROUBLESHOOTING THE VIDEO MONITOR

Visual Inspection

With the Video Monitor Installed--Turn off power to the terminal, open the case, and check the following possible problem areas:

* Connectors: look for

  Loose or damaged connectors

  Broken or loose securing clips on pins at connectors

  Bad crimps

  Dirty contacts

* Wires: are any broken, loose, or frayed?

* Components: are any overheated, leaking, or burned?

If any defects are found, correct them and recheck the terminal before continuing.

With the Video Monitor Removed--The following inspections should be made with the video monitor removed.

To remove the video monitor:

1. With the power off and the cover removed, disconnect the following connections on the video monitor:

   J10 (signal input)
   J11 (DC power)
   J12 (yoke)

2. Disconnect the following parts on the CRT tube:

   CRT socket (small printed circuit board at rear of tube)

   Anode lead (SEE WARNING ON PAGE 2-1)

   Ground wire

3. Remove the three securing screws on the video monitor.

4. Carefully remove the video monitor.

With the video monitor removed, inspect it for:

* Overheated, leaking, or burned components
* Missing or broken components
* Cracked, broken, or lifted traces
* Poor solder joints (loose solder balls, cold solder joints, or solder bridges)
* Bent pins

NOTE!

If defects are found, correct them and recheck the terminal before continuing.

If no defects are found, reinstall the video monitor.

Apply power.

WARNING!

High voltages are present on the video logic board. USE EXTREME CARE during troubleshooting.

The four adjustments which can be made to the video board are listed in Table 6-1. The controls are shown in Figure 6-1.

Table 6-1 Video Board Adjustments

Problem	Control
Characters are too bright or too dim	Brightness
Whole screen is too tall or too short	Height
Characters are not even in height from the top to the bottom of the screen	Linearity
Characters are not sharp	Focus

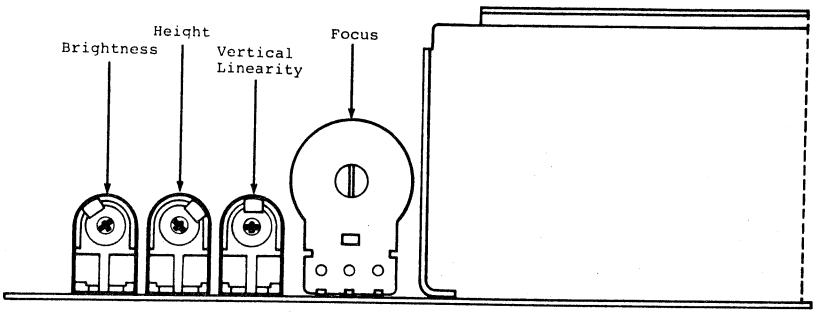


Figure 6-1 Location of Controls on Video Board

Debugging Guide

This section will help you troubleshoot specific malfunctions. Table 6-2 lists voltage levels and wave forms.

SYMPTOM: No Vertical Deflection

1. Check Q201 collector for vertical deflection.

   a. If it is present, proceed to Step 2.

   b. If it is not present, check the base of Q201.

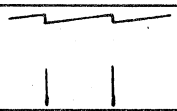
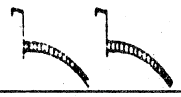
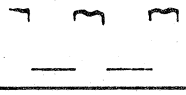
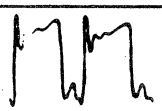
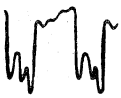
   c. If vertical deflection is present at the base, isolate the Q201 collector to see if signal is being pulled down. If there is still no output at Q201, suspect Q201.

   d. If vertical deflection is not present at the base, troubleshoot between the base of Q201 and P10 pin 5 (vertical sync signal from the logic board).

2. Check Q202 collector for vertical deflection.

   a. If it is present, proceed to Step 3.

   b. If it is not present, check the base of Q202.

Transistor			Base(In)			Collector(Out)			Emitter(GND)		
Location	Parts	Function	Vtg DC V	Vtg AC Vp-p	Wave Form	Vtg DC V	Vtg AC Vp-p	Wave Form	Vtg DC V	Vtg AC Vp-p	Wave Form
(IC 1)	LAS1512	Regulation	12	2.5		12	0.0	—	0.0	0.0	—
(IC 2)	LAS1605	〃		1.6		5	0.0	—	0.0	0.0	—
(IC 3)	LAS1812	〃		0.1		-12	0.0	—	0.0	0.0	—
(IC 4)	LAS15CB	〃		1.4		13.8	0.0	—	0.0	0.0	—
Q102	2SC509	〃	78.7	0.0	—	86.4	1.5		98.0	0.0	—
Q103	2SC983	〃	12.0	0.0	—	75.7	0.0	—	11.-	0.0	—
Q 201	2SA495	Vert Pree Drive	2.0	3.0		0.6	0.57		1.0	1.7	
Q 202	2SC372	Vert Drive	0.68	0.5		8.0	6.5		0.0	0.0	—
Q 203	2SC1173	Vert Out	9.36	6.5		12	0.0	—	8.76	6.5	
Q 204	2SA473	Vert Out	8.0	6.5		0.0	0.0	—	8.6	6.5	
Q 301	2SC735	Horiz Drive	-0.25	0.64		12	20		0.0	0.0	—
Q 302	2SC2233	Horiz Out	-0.08	6		12.8	124		0.0	0.0	—
Q 501	2SC983	Video Amp	0.4	3		76.8	25		-0.8	2.8	
D 302	DS-113A	Damping	12.8	132							

DC Voltage reading taken with VTVM from point indicated to chassis ground.

AC Voltage reading taken with Oscilloscope from point indicated to chassis ground

Table 6-2 Voltage Levels and Waveforms

c. If vertical deflection is present at the base, isolate the Q202 collector to see if signal is being pulled down. If there is still no output at Q202, suspect Q202.

d. If vertical deflection is not present at the base, troubleshoot back from the base of Q202.

3. Check the negative side of C207 for vertical deflection.

a. If vertical deflection is present, the vertical drive section of the video monitor is good. If a vertical problem still exists, check the following areas:

Connections
CRT socket
Related components (small pcb at neck of CRT)

b. If vertical deflection is not present at C207, check the Q203 emitter.

c. If vertical deflection is not present at the Q203 emitter, check the base of Q203.

d. If vertical deflection is present at the base, suspect Q203.

e. If not present at the base of Q203, troubleshoot back.

f. If Q203 emitter is good, check Q204 emitter.

g. If vertical deflection is not present at Q204 emitter, check the base of A204.

h. If present at base, suspect A204.

i. If not present at base, troubleshoot back from Q204.

NOTE!

Since Q203 and Q204 are a matched set of push/pull amplifiers, replace both if one require replacement.

SYMPTOM: No Horizontal Deflections

1. Check the Q301 deflector for horizontal deflections.

a. If horizontal deflections are present, proceed to Step 2.

b. If not present, check the base of Q301.

c. If horizontal deflections are present at the base, isolate the Q301 collector to see if signal is being pulled down.

d. If there is no output at the Q301 collector, suspect Q301.

e. If horizontal deflections are not present at the base of Q301, troubleshoot between the base of Q301 and P10 pin 1 (horizontal sync signal from the logic board).

2. Check the Q302 deflector for horizontal deflections.

a. If horizontal deflections are present, proceed to Step 3.

b. If not present, check the base of Q302.

c. If horizontal deflections are present at the base, isolate the Q302 collector to see if signal is being pulled down.

d. If there is no output at the Q302 collector, suspect A302.

e. If horizontal deflections are not present at the base of Q301, suspect T301 (drive transformer) or Q302.

f. If the proper signal is present at Q302 collector, suspect the following areas:

C306
L201

SYMPTOM: No Video

1. Suspect the following areas:

L302
Q302
Q301
T302 (FBT)
C305
Q501

2. Check for cracked, broken, or lifted traces.

SYMPTOM: Jittery Screen

1. Make sure that yoke connector J12 is not dirty.

2. Suspect C504.

3. Check for

   * Bad crimps

   * Poor solder joints (loose solder balls, cold solder joints, or solder bridges)

SYMPTOM: Poor Linearity

1. If horizontal linearity is the problem, check L201.

2. If vertical linearity is the problem, check the following:

   a. Adjust SFT 2 (linearity potentiometer)

   b. Q203 and Q204

SYMPTOM: Fuses Blow and/or Voltage is Low

1. Check T302 (FBT)

2. Check for cracked, broken, or lifted traces.

7. TROUBLESHOOTING THE POWER SUPPLY

Visual Inspection

With the Power Supply Installed--Turn off power to the terminal, open the case, and check the following possible problem areas:

* Connectors: look for

  Loose or damaged connectors

  Broken or loose securing clips on pins at connectors

  Bad crimps

  Dirty contacts

  Depressed pins in connectors

* Wires: are any broken, loose, or frayed?

* Components: are any overheated, leaking, or burned?

* Bad fuse

  NOTE!

  Check the fuse with an ohm meter. Do not rely on a visual check.

* Loose fuse holder

If defects are found, correct them and recheck the terminal before continuing.

With the Power Supply Removed--The following inspections should be made with the power supply removed.

To remove the power supply:

1. Turn the power off and remove the cover.
2. Unplug the power cord from the wall outlet.
3. Disconnect K1 (AC input) on the power supply.
4. Disconnect J11 on the video monitor.
5. Disconnect J5 on the logic board.
6. Remove the securing screws on the power supply (four on the 925/950; three on 910/910 PLUS/912/920).
7. Carefully remove the power supply.

With the Power Supply Removed--Inspect the power supply for:

* Overheated, leaking, or burned components
* Bad crimps
* Bad connectors/connections

NOTE!

If defects are found, correct them and recheck the terminal before continuing.

Disassemble the power supply by removing the four securing screws and spacers which hold the small pcb on the heat sink.

Debugging Guide

This section will help you troubleshoot specific malfunctions. Table 6-2 lists voltage levels and waveforms.

SYMPTOM: No +5V DC

1. Remove F103 and check for approximately +13V on one side of the fuseholder.

   a. If correct voltage is not present, suspect the following areas:

      C105 through C108

      D105 through D108

      Bad crimps

      Loose or damaged connectors

      Broken or loose securing clips on pins at connectors

   b. If correct voltage is present, suspect the following areas:

      F103 (fuse)

      LAS1605

      C114

      C113

      Bad crimps

      Loose or damaged connectors

      Broken or loose securing clips on pins at connectors

SYMPTOM: +5V DC is Low

1. Check the following areas:

   LAS1605

   Bad crimps

   Loose or damaged connectors

   Broken or loose securing clips on pins at connectors

SYMPTOM: No +12V DC or 13.8V DC

1. Remove F102 and check for +24V on one side of the fuseholder.

   a. If correct voltage is not present, suspect the following areas:

      C101 through C104
      D101 through D104
      Bad crimps
      Bad connectors/connections
      Broken or loose clips

   b. If correct voltage is present, suspect the following areas:

      LAS15CB/LAS16CB

      C115

      C113

      Bad crimps

      Loose or damaged connectors

      Broken or loose securing clips on pins at connectors

SYMPTOM: +12V DC or +13.8V DC is Low

1. Check the following areas:

   LAS15CB

   C113

   Bad crimps

   Loose or damaged connectors

   Broken or loose securing clips on pins at connectors

SYMPTOM: No -12V DC

1. Check the following areas:

   C101 and C102

   D101 and D102

   D112

   C116

   Bad crimps

   Loose or damaged connectors

   Broken or loose securing clips on pins at connectors

SYMPTOM: No +75V DC

1. Check the following areas:

   C109 (can be removed; do not need to be replaced)
   C120
   C119
   Q102
   Q103

SYMPTOM: +75V DC is Low

1. Adjust SFR3.

2. If +75V DC cannot be adjusted, check the following areas:

   Q103
   C109

If no defects are found, reinstall the video monitor. Make sure the securing screws are locked tight before proceeding.

Apply power.