950 Theory of Operation

CPU, Timing and Control

(Refer to Figure 1) The 23.814 Mhz oscillator (Osc 1) is used to generate all timing for the terminal. It is used directly as the dot clock (Shift Clock), divided by 13 to drive the UARTs, and divided by 14 (1.701 Mhz) to drive the CRT controller (CCLK) and the CPU (via the clock stretch circuit).

The clock stretch circuit is capable, upon command, of generating clock periods twice the normal length (588 ns versus 1175 ns) for accessing slow memory or peripheral devices. Its output drives the I_0 input of the 6502 CPU. The CPU then outputs I_2, which controls the timing of the CPU bus. I_2 is a slightly delayed version of I_0.

The result of these circuits are I_2 and CCLK, two signals of identical frequency but opposite phase, (except during clock stretched cycles). The importance of this will be made clear later in our discussion of the display controller.

The CPU fetches its program from the ROMs (Read Only Memory) A41-43. It uses the 6522 (A54) to sense switches S1 and S2 and to generate control signals for the rest of the terminal.

Display Controller

(Refer to Figure 2) Timer T2, part of the 6522, and the 6545 (A55) are used to generate the memory address, in Display RAM, of each character as it is about to be displayed, and the horizontal and vertical synchronization pulses necessary to control the deflection circuits of the monitor.

Timer T2 is used to count horizontal scan lines and interrupt the processor (via NMI) when a specified number of scans has occurred. The processor then loads the memory address of the next data row into the CRT Controller and "sets" this address by generating a carefully-timed reset to the 6545.

At this same time the processor loads a 4 bit value into latch, A61. At the time of the CRT reset this value is transferred to counter A60 and becomes the Row Address of the next data row. This value is then incremented by each horizontal sync pulse until the start of the next data row when it is again preset to a value determined by the CPU.

The CPU and the display controller share access to the System and Display RAM (Random Access Memory). This is done during alternate phases of the I_2 clock. During the positive portion of I_2 the CPU address may be gated onto the RAM address bus by Multiplexers A43-46, and bidirectional transceiver A14 is enabled to pass data between the CPU data bus and the RAM data bus.

During the negative portion of I_2 the 6545 address bus is gated onto the RAM address bus allowing the video data to be latched by A24 and held for the display generator.

This alternating access or "interleaved" access allows the processor to operate at normal speed, without waits of any kind, yet prevents degradation of the display quality that could be caused by inadvertant appropriation of the display bus by the processor to access data.

The only penalty for this scheme is the necessity for fast RAM (150 ns or faster).

Video Generation

(Refer to Figure 3) This Display Data and the Row Address (or scan address) are used to obtain the dots for the next character to be displayed from the character generator ROMs A32 and A33.

These dots are then fed in parallel to shift registers A22 and A23 and emerge serially as raw video.

Additionally, bits 0-3 of Display data and bit 7 of A33 are combined to generate the attribute signals Underline, Blink, Blank, and Reverse. ICs A19, 20, 21 and 30 latch and delay the decoded attributes from the previous data row for carry-over into the next.

Bit 6 of A33 controls the intensity of the character to be displayed.

Gates A1, 2, 10 and 11 are used to modify the raw video to the proper intensity and polarity, and gate it on or off in response to the attribute signals and control signals BOW (used to reverse the entire display), cursor, BLI-RATE (used to blink the video) and FORCE BLANK (used to blank the entire screen).

Transistor Q1 is used to drive the video to the proper voltage and current levels to drive the video module and/or an external monitor (using the composite video jumpers).

I/O Circuits

(Refer to Figure 4) UART A49 is used to receive (and optionally transmit) serial data from (and to) the keyboard. The transmit path to the keyboard is normally used to conduct the bell tone from the 6522 (via driver Q4) to the speaker in the keyboard.

UARTs A50 (Main Port, P3) and A51 (Printer Port, P4) are used to send and receive serial data from P3 and P4 via the drivers, receivers and switching circuits A39, 40, 47, 48, 56, 57, 58 and 59.

The UARTs A49, 50 and A51 (6551s) are connected to the CPU Bus and generate IRQ interrrupts when commanded by the CPU to send or receive data. Additionally these parts contain internal baud rate generators that must be programmed by the CPU to control the baud rates.

General Debugging Guidelines

The following procedures are usually done when there is no initial beep at turn on. To debug any microprocessor without an emulator, remove as many devices as possible from the bus. This includes the CPU, CRT controller, VIA, UARTs, and Program, User, and Character Generator ROMs. The address and data lines can then be checked for proper operation.

Field component failures will generally be the most complicated integrated circuits. In case of a failure of this type, first replace any of the socketed components associated with the failure symptoms. Should the problem persist, check the RAM, RS232 components, bus transceiver, and multiplexers. This failure group is the most difficult to troubleshoot. An effective way to check the RAM is to use a test wire with two clips. Connect one end to the R4/D1 junction in the video section of the logic and the other end touching the outputs of the RAM. This, in essence, uses the monitor as a scope. Compare the response on the screen with a good terminal, and using this method, a faulty terminal can be debugged quickly. Should the problem not be found in the second failure group, a simple hard failure in any area could be the cause of the problem.

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PART NUMBER
R650X and R651X

Rockwell

R6500 Microcomputer System DATA SHEET

R6500 MICROPROCESSORS (CPU's)

SYSTEM ABSTRACT

The 8-bit R6500 microcomputer system is produced with N-Channel, Silicon Gate technology. Its performance speeds are enhanced by advanced system architecture. This innovative architecture results in smaller chips — the semiconductor threshold to cost-effectivity. System cost-effectivity is further enhanced by providing a family of 10 software-compatible microprocessor (CPU) devices, described in this document. Rockwell also provides memory and microcomputer system . . . as well as low-cost design aids and documentation.

R6500 MICROPROCESSOR (CPU) CONCEPT

Ten CPU devices are available. All are software-compatible. They provide options of addressable memory, interrupt input, on-chip clock oscillators and drivers. All are bus-compatible with earlier generation microprocessors like the M6800 devices.

The family includes six microprocessors with on-board clock oscillators and drivers and four microprocessors driven by external clocks. The on-chip clock versions are aimed at high performance, low cost applications where single phase inputs, crystal or RC inputs provide the time base. The external clock versions are geared for multiprocessor system applications where maximum timing control is mandatory. All R6500 microprocessors are also available in a variety of packaging (ceramic and plastic), operating frequency (1 MHz and 2 MHz) and temperature (commercial, industrial and military) versions.

MEMBERS OF THE R6500 MICROPROCESSOR (CPU) FAMILY

Microprocessors with On-Chip Clock Oscillator

Model	Addressable Memory
R6502	65K Bytes
R6503	4K Bytes
R6504	8K Bytes
R6505	4K Bytes
R6506	4K Bytes
R6507	8K Bytes

Microprocessors with External Two Phase Clock Output

Model	Addressable Memory
R6512	65K Bytes
R6513	4K Bytes
R6514	8K Bytes
R6515	4K Bytes

FEATURES

- Single +5V supply
- N channel, silicon gate, depletion load technology
- Eight bit parallel processing
- 56 Instructions
- Decimal and binary arithmetic
- Thirteen addressing modes
- True indexing capability
- Programmable stack pointer
- Variable length stack
- Interrupt capability
- Non-maskable interrupt
- Use with any type of speed memory
- 8-bit Bidirectional Data Bus
- Addressable memory range of up to 65K bytes
- "Ready" input
- Direct Memory Access capability
- Bus compatible with M6800
- 1 MHz and 2 MHz operation
- Choice of external or on-chip clocks
- On-the-chip clock options
  - External single clock input
  - RC time base input
  - Crystal time base input
- Commercial, industrial and military temperature versions
- Pipeline architecture

Ordering Information

Order Number: R65XX___

- Temperature Range:
  - No suffix = 0°C to +70°C
  - E = -40°C to +85°C (Industrial)
  - MT = -55°C to +125°C (Military)
  - M = MIL-STD-883, Class B
- Package:
  - C = Ceramic
  - P = Plastic
  - (Not Avaible for M or MT suffix)
- Frequency Range:
  - No suffix = 1 MHz
  - A = 2 MHz
- Model Designator:
  - XX = 02, 03, 04, ... 15

NOTE: Contact your local Rockwell Representative concerning availability.

R6500 MICROPROCESSORS (CPU's)

Specifications subject to change without notice

R6500 Signal Description

Clocks (ϕ_1, ϕ_2)

The R651X requires a two phase non-overlapping clock that runs at the V_{CC} voltage level.

The R650X clocks are supplied with an internal clock generator. The frequency of these clocks is externally controlled.

Address Bus (A0-A15)

These outputs are TTL compatible, capable of driving one standard TTL load and 130 pF.

Data Bus (D0-D7)

Eight pins are used for the data bus. This is a bidirectional bus, transferring data to and from the device and peripherals. The outputs are tri-state buffers capable of driving one standard TTL load and 130 pF.

Data Bus Enable (DBE)

This TTL compatible input allows external control of the tri-state data output buffers and will enable the microprocessor bus driver when in the high state. In normal operation DBE would be driven by the phase two (ϕ_2) clock, thus allowing data output from microprocessor only during ϕ_2. During the read cycle, the data bus drivers are internally disabled, becoming essentially an open circuit. To disable data bus drivers externally, DBE should be held low.

Ready (RDY)

This input signal allows the user to halt or single cycle the microprocessor on all cycles except write cycles. A negative transition to the low state during or coincident with phase one (ϕ_1) will halt the microprocessor with the output address lines reflecting the current address being fetched. If Ready is low during a write cycle, it is ignored until the following read operation. This condition will remain through a subsequent phase two (ϕ_2) in which the Ready signal is low. This feature allows microprocessor interfacing with the low speed PROMs as well as fast (max. 2 cycle) Direct Memory Access (DMA).

Interrupt Request ($\overline{IRQ}$)

This TTL level input requests that an interrupt sequence begin within the microprocessor. The microprocessor will complete the current instruction being executed before recognizing the request. At that time, the interrupt mask bit in the Status Code Register will be examined. If the interrupt mask flag is not set, the microprocessor will begin an interrupt sequence. The Program Counter and Processor Status Register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further interrupts may occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, therefore transferring program control to the memory vector located at these addresses. The RDY signal must be in the high state for any interrupt to be recognized. A 3KΩ external resistor should be used for proper wire-OR operation.

Non-Maskable Interrupt ($\overline{NMI}$)

A negative going edge on this input requests that a non-maskable interrupt sequence be generated within the microprocessor.

$\overline{NMI}$ is an unconditional interrupt. Following completion of the current instruction, the sequence of operations defined for $\overline{IRQ}$ will be performed, regardless of the state interrupt mask flag. The vector address loaded into the program counter, low and high, are locations FFFA and FFFB respectively, thereby transferring program control to the memory vector located at these addresses. The instructions loaded at these locations cause the microprocessor to branch to a non-maskable interrupt routine in memory.

$\overline{NMI}$ also requires an external 3KΩ register to V_{CC} for proper wire-OR operations.

Inputs $\overline{IRQ}$ and $\overline{NMI}$ are hardware interrupts lines that are sampled during ϕ_2 (phase 2) and will begin the appropriate interrupt routine on the ϕ_1 (phase 1) following the completion of the current instruction.

Set Overflow Flag (S.O.)

A negative going edge on this input sets the overflow bit in the Status Code Register. This signal is sampled on the trailing edge of $\phi 1$ and must be externally synchronized.

SYNC

This output line is provided to identify those cycles in which the microprocessor is doing an OP CODE fetch. The SYNC line goes high during ϕ_1 of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the ϕ_1 clock pulse in which SYNC went high, the processor will stop in its current state and will remain in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.

Reset

This input is used to reset or start the microprocessor from a power down condition. During the time that this line is held low, writing to or from the microprocessor is inhibited. When a positive edge is detected on the input, the microprocessor will immediately begin the reset sequence.

After a system initialization time of six clock cycles, the mask interrupt flag will be set and the microprocessor will load the program counter from the memory vector locations FFFC and FFFD. This is the start location for program control.

After V_{CC} reaches 4.75 volts in a power up routine, reset must be held low for at least two clock cycles. At this time the R/W and (SYNC) signal will become valid.

When the reset signal goes high following these two clock cycles, the microprocessor will proceed with the normal reset procedure detailed above.

ADDRESSING MODES

ACCUMULATOR ADDRESSING — This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

IMMEDIATE ADDRESSING — In immediate addressing, the operand is contained in the second byte of the instruction, with no further memory addressing required.

ABSOLUTE ADDRESSING — In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Thus, the absolute addressing mode allows access to the entire 65K bytes of addressable memory.

ZERO PAGE ADDRESSING — The zero page instructions allow for shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in significant increase in code efficiency.

INDEXED ZERO PAGE ADDRESSING — (X, Y indexing) — This form of addressing is used in conjunction with the index register and is referred to as "Zero Page, X" or "Zero Page, Y". The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally due to the "Zero Page" addressing nature of this mode, no carry is added to the high order 8 bits of memory and crossing of page boundaries does not occur.

INDEXED ABSOLUTE ADDRESSING — (X, Y indexing) — This form of addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X", and "Absolute, Y". The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields resulting in reduced coding and execution time.

IMPLIED ADDRESSING — In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

RELATIVE ADDRESSING — Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is -128 to +127 bytes from the next instruction.

INDEXED INDIRECT ADDRESSING — In indexed indirect addressing (referred to as (Indirect, X)), the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents is the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

INDIRECT INDEXED ADDRESSING — In indirect indexed addressing (referred to as (Indirect), Y), the second byte of the instruction points to a memory location in page zero. The contents of this memory location is added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

ABSOLUTE INDIRECT — The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location is contained in the third byte of the instruction. The contents of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter.

INSTRUCTION SET — ALPHABETIC SEQUENCE

ADC Add Memory to Accumulator with Carry
AND "AND" Memory with Accumulator
ASL Shift left One Bit (Memory or Accumulator)

BCC Branch on Carry Clear
BCS Branch on Carry Set
BEQ Branch on Result Zero
BIT Test Bits in Memory with Accumulator
BMI Branch on Result Minus
BNE Branch on Result not Zero
BPL Branch on Result Plus
BRK Force Break
BVC Branch on Overflow Clear
BVS Branch on Overflow Set

CLC Clear Carry Flag
CLD Clear Decimal Mode
CLI Clear Interrupt Disable Bit
CLV Clear Overflow Flag
CMP Compare Memory and Accumulator
CPX Compare Memory and Index X
CPY Compare Memory and Index Y

DEC Decrement Memory by One
DEX Decrement Index X by One
DEY Decrement Index Y by One

EOR "Exclusive-or" Memory with Accumulator

INC Increment Memory by One
INX Increment Index X by One
INY Increment Index Y by One

JMP Jump to New Location
JSR Jump to New Location Saving Return Address

LDA Load Accumulator with Memory
LDX Load Index X with Memory
LDY Load Index Y with Memory
LSR Shift One Bit Right (Memory or Accumulator)

NOP No Operation

ORA "OR" Memory with Accumulator

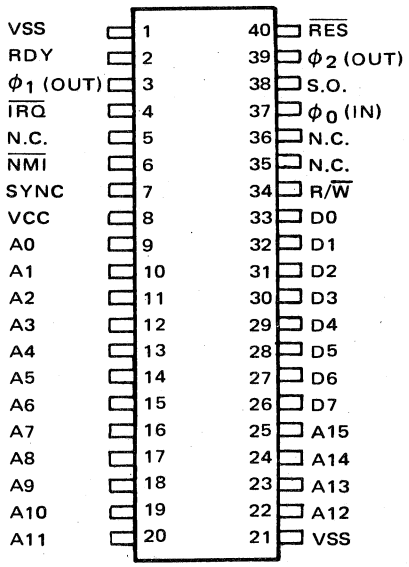
PHA Push Accumulator on Stack
PHP Push Processor Status on Stack
PLA Pull Accumulator from Stack
PLP Pull Processor Status from Stack

ROL Rotate One Bit Left (Memory or Accumulator)
ROR Rotate One Bit Right (Memory or Accumulator)
RTI Return from Interrupt
RTS Return from Subroutine

SBC Subtract Memory from Accumulator with Borrow
SEC Set Carry Flag
SED Set Decimal Mode
SEI Set Interrupt Disable Status
STA Store Accumulator in Memory
STX Store Index X in Memory
STY Store Index Y in Memory

TAX Transfer Accumulator to Index X
TAY Transfer Accumulator to Index Y
TSX Transfer Stack Pointer to Index X
TXA Transfer Index X to Accumulator
TXS Transfer Index X to Stack Register
TYA Transfer Index Y to Accumulator

R6502 – 40 Pin Package



Features of R6502

- 65K Addressable Bytes of Memory (A0-A15)
- $\overline{IRQ}$ Interrupt
- On-the-chip Clock
  - TTL Level Single Phase Input
  - RC Time Base Input
  - Crystal Time Base Input
- SYNC Signal
  (can be used for single instruction execution)
- RDY Signal
  (can be used to halt or single cycle execution)
- Two Phase Output Clock for Timing of Support Chips
- $\overline{NMI}$ Interrupt

INSTRUCTION SET

INSTRUCTIONS		IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM			IMPLIED			(IND, X)			(IND), Y			Z. PAGE, X			ABS, X			ABS, Y			RELATIVE			INDIRECT			Z PAGE, Y			PROCESSOR STATUS CODES	
MNEMONIC	OPERATION	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	7 6 5 4 3 2 1 0 N V • B D I Z C	MNEMONIC
ADC	A + M + C → A (4) (1)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3										N V • • • • Z C	ADC
AND	A ∧ M → A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3										N • • • • • Z •	AND
ASL	C ← [7 0] ← 0				0E	6	3	06	5	2	0A	2	1										16	6	2	1E	7	3													N • • • • • Z C	ASL
BCC	BRANCH ON C = 0 (2)																															90	2	2							• • • • • • • •	BCC
BCS	BRANCH ON C = 1 (2)																															B0	2	2							• • • • • • • •	BCS
BEQ	BRANCH ON Z = 1 (2)																															F0	2	2							• • • • • • • •	BEQ
BIT	A ∧ M				2C	4	3	24	3	2																															M_7 M_6 • • • Z •	BIT
BMI	BRANCH ON N = 1 (2)																															30	2	2							• • • • • • • •	BMI
BNE	BRANCH ON Z = 0 (2)																															D0	2	2							• • • • • • • •	BNE
BPL	BRANCH ON N = 0 (2)																															10	2	2							• • • • • • • •	BPL
BRK	BREAK													00	7	1																									• • • 1 • 1 • •	BRK
BVC	BRANCH ON V = 0 (2)																															50	2	2							• • • • • • • •	BVC
BVS	BRANCH ON V = 1 (2)																															70	2	2							• • • • • • • •	BVS
CLC	0 → C													18	2	1																									• • • • • • • 0	CLC
CLD	0 → D													D8	2	1																									• • • • 0 • • •	CLD
CLI	0 → I													58	2	1																									• • • • • 0 • •	CLI
CLV	0 → V													B8	2	1																									• 0 • • • • • •	CLV
CMP	A − M	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3										N • • • • • Z C	CMP
CPX	X − M	E0	2	2	EC	4	3	E4	3	2																															N • • • • • Z C	CPX
CPY	Y − M	C0	2	2	CC	4	3	C4	3	2																															N • • • • • Z C	CPY
DEC	M − 1 → M				CE	6	3	C6	5	2													D6	6	2	DE	7	3													N • • • • • Z •	DEC
DEX	X − 1 → X													CA	2	1																									N • • • • • Z •	DEX
DEY	Y − 1 → Y													88	2	1																									N • • • • • Z •	DEY
EOR	A ∨ M → A (1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3										N • • • • • Z •	EOR
INC	M + 1 → M				EE	6	3	E6	5	2													F6	6	2	FE	7	3													N • • • • • Z •	INC
INX	X + 1 → X													E8	2	1																									N • • • • • Z •	INX
INY	Y + 1 → Y													C8	2	1																									N • • • • • Z •	INY
JMP	JUMP TO NEW LOC				4C	3	3																												6C	5	3				• • • • • • • •	JMP
JSR	JUMP SUB				20	6	3																																		• • • • • • • •	JSR
LDA	M → A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3										N • • • • • Z •	LDA
LDX	M → X (1)	A2	2	2	AE	4	3	A6	3	2																			BE	4	3							B6	4	2	N • • • • • Z •	LDX
LDY	M → Y (1)	A0	2	2	AC	4	3	A4	3	2													B4	4	2	BC	4	3													N • • • • • Z •	LDY
LSR	0 → [7 0] → C				4E	6	3	46	5	2	4A	2	1										56	6	2	5E	7	3													0 • • • • • Z C	LSR
NOP	NO OPERATION													EA	2	1																									• • • • • • • •	NOP
ORA	A ∨ M → A	09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3										N • • • • • Z •	ORA
PHA	A → Ms S − 1 → S													48	3	1																									• • • • • • • •	PHA
PHP	P → Ms S − 1 → S													08	3	1																									• • • • • • • •	PHP
PLA	S + 1 → S Ms → A													68	4	1																									N • • • • • Z •	PLA
PLP	S + 1 → S Ms → P													28	4	1																									(RESTORED)	PLP
ROL	[7 0] ← [C] ←				2E	6	3	26	5	2	2A	2	1										36	6	2	3E	7	3													N • • • • • Z C	ROL
ROR	[C] → [7 0]				6E	6	3	66	5	2	6A	2	1										76	6	2	7E	7	3													N • • • • • Z C	ROR
RTI	RTRN INT													40	6	1																									(RESTORED)	RTI
RTS	RTRN SUB													60	6	1																									• • • • • • • •	RTS
SBC	A − M − $\overline{C}$ → A (1)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3										N V • • • • Z (3)	SBC
SEC	1 → C													38	2	1																									• • • • • • • 1	SEC
SED	1 → D													F8	2	1																									• • • • 1 • • •	SED
SEI	1 → I													78	2	1																									• • • • • 1 • •	SEI
STA	A → M				8D	4	3	85	3	2							81	6	2	91	6	2	95	4	2	9D	5	3	99	5	3										• • • • • • • •	STA
STX	X → M				8E	4	3	86	3	2																															• • • • • • • •	STX
STY	Y → M				8C	4	3	84	3	2													94	4	2																	• • • • • • • •	STY
TAX	A → X													AA	2	1																									N • • • • • Z •	TAX
TAY	A → Y													A8	2	1																									N • • • • • Z •	TAY
TSX	S → X													BA	2	1																									N • • • • • Z •	TSX
TXA	X → A													8A	2	1																									N • • • • • Z •	TXA
TXS	X → S													9A	2	1																									• • • • • • • •	TXS
TYA	Y → A													98	2	1																									N • • • • • Z •	TYA

(1) ADD 1 to "N" IF PAGE BOUNDARY IS CROSSED

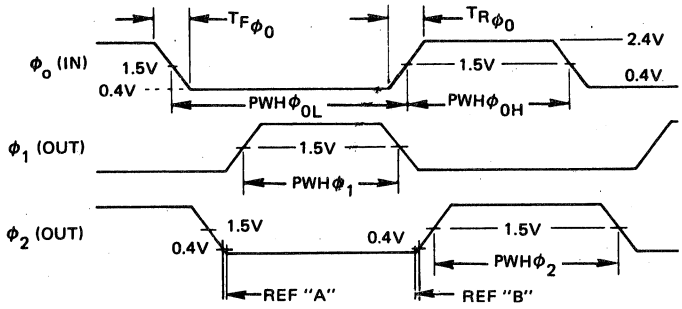
(2) ADD 1 TO "N" IF BRANCH OCCURS TO SAME PAGE
ADD 2 TO "N" IF BRANCH OCCURS TO DIFFERENT PAGE

(3) CARRY NOT = BORROW

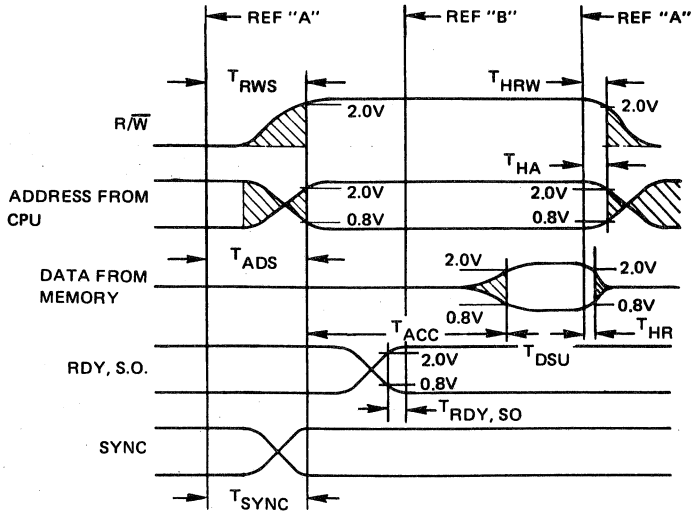
(4) IF IN DECIMAL MODE, Z FLAG IS INVALID
ACCUMULATOR MUST BE CHECKED FOR ZERO RESULT

X	INDEX X	+	ADD	M_7	MEMORY BIT 7
Y	INDEX Y	−	SUBTRACT	M_6	MEMORY BIT 6
A	ACCUMULATOR	∧	AND	n	NO. CYCLES
M	MEMORY PER EFFECTIVE ADDRESS	∨	OR	#	NO. BYTES
Ms	MEMORY PER STACK POINTER	¥	EXCLUSIVE OR		

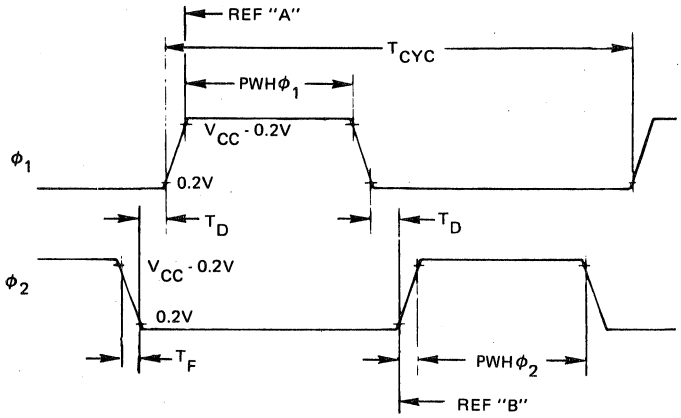
Clock Timing – R6502, 03, 04, 05, 06, 07



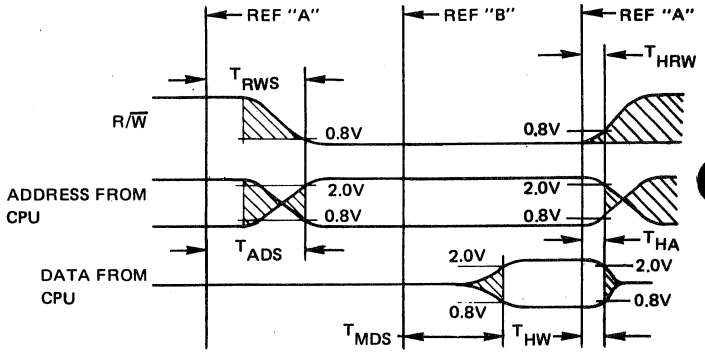
Timing for Reading Data from Memory or Peripherals



Clock Timing – R6512, 13, 14, 15

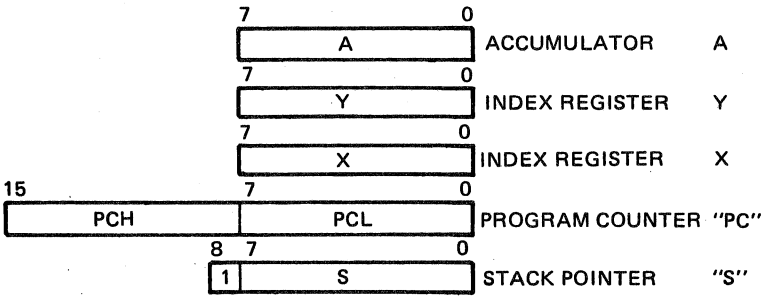


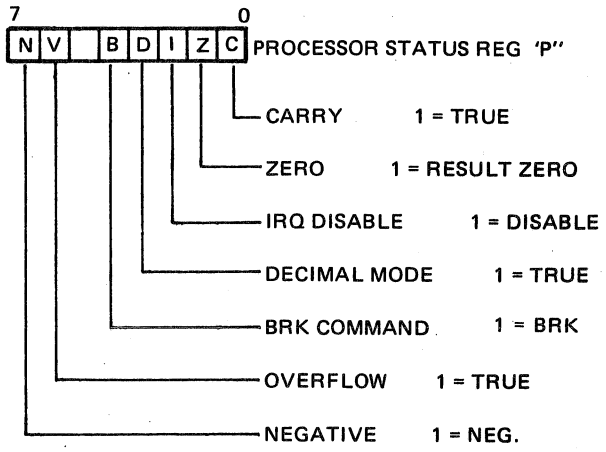
Timing for Writing Data to Memory or Peripherals

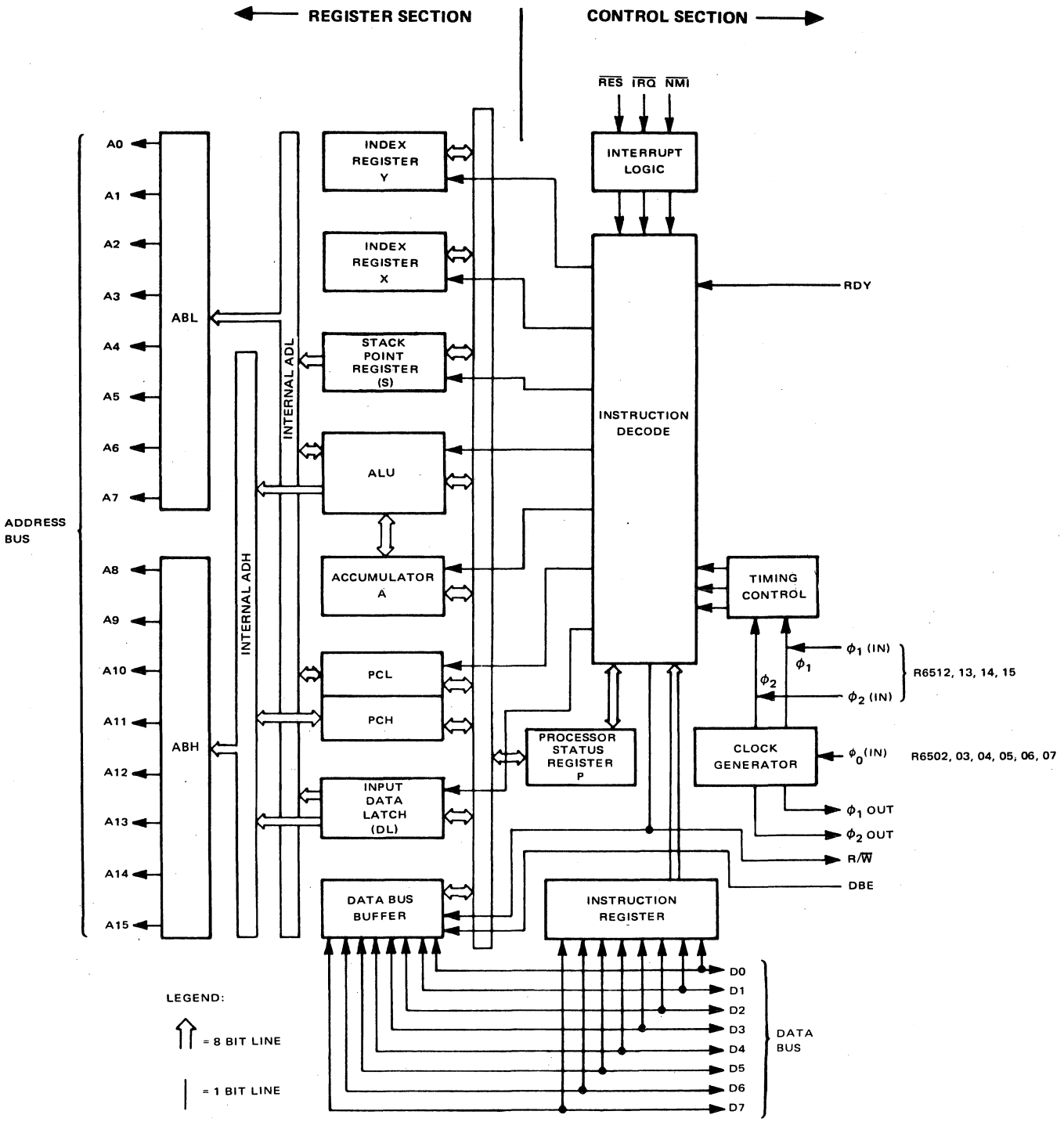


Note: "REF." means Reference Points on clocks.

PROGRAMMING MODEL







Note: 1. Clock Generator is not included on R6512, 13, 14, 15
2. Addressing Capability and control options vary with each of the R6500 Products.

R6500 Internal Architecture

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DOCUMENT NO. 29000 D47
REVISION 1, OCT. 1978

PART NUMBER
R6522

R6500 Microcomputer System

DATA SHEET

VERSATILE INTERFACE ADAPTER (VIA)

SYSTEM ABSTRACT

The 8-bit R6500 microcomputer system is produced with N-channel, silicon-gate, depletion-load technology. Its performance speeds are enhanced by advanced system architecture. Its innovative architecture results in smaller chips — the semiconductor threshold to cost-effectivity. System cost-effectivity is further enhanced by providing a family of 10 software-compatible microprocessor (CPU) devices, memory and I/O devices . . . as well as low-cost design aids and documentation.

DESCRIPTION

The R6522 VIA adds two powerful, flexible Interval Timers, a serial-to-parallel/parallel-to-serial shift register and input latching on the peripheral ports to the capabilities of the R6520 Peripheral Interface Adapter (PIA) device. Handshaking capability is expanded to allow control of bidirectional data transfers between VIAs in multiple processor systems and between peripherals.

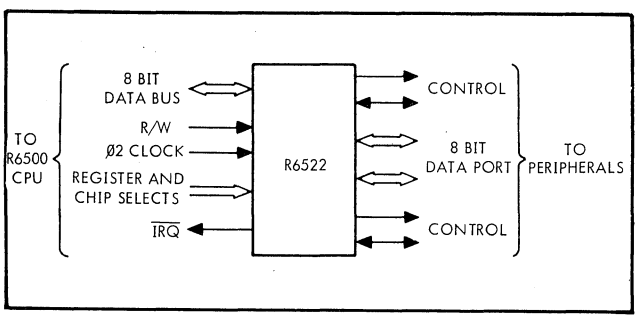
Control of peripherals is primarily through two 8-bit bidirectional ports. Each of these ports can be programmed to act as an input or an output. Peripheral I/O lines can be selectively controlled by the Interval Timers to generate programmable-frequency square waves and/or to count externally generated pulses. Positive control of VIA functions is gained through its internal register organization: Interrupt Flag Register, Interrupt Enable Register, and two Function Control Registers.

FEATURES

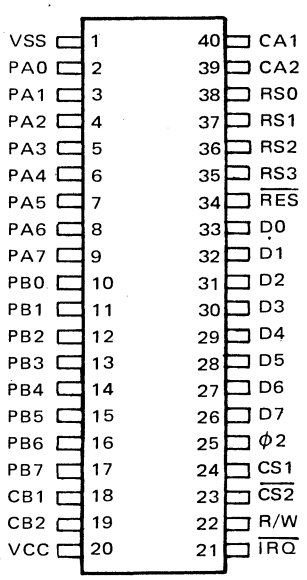
- Organized for simplified software control of many functions
- Compatible with the R650X and R651X family of microprocessors (CPUs)
- Bi-directional, 8-bit data bus for communication with microprocessor
- Two Bi-directional, 8-bit input/output ports for interface with peripheral devices
- CMOS and TTL compatible input/output peripheral ports
- Data Direction Registers allow each peripheral pin to act as either an input or an output
- Interrupt Flag Register allows the microprocessor to readily determine the source of an interrupt and provides convenient control of the interrupts within the chip
- Handshake control logic for input/output peripheral data transfer operations
- Data latching on peripheral input/output ports
- Two fully-programmable interval timers/counters
- Eight-bit Shift Register for serial interface
- Forty-pin plastic or ceramic DIP package.

Ordering Information

Order Number	Package Type	Frequency	Temperature Range
R6522P	Plastic	1 MHz	0°C to +70°C
R6522AP	Plastic	2 MHz	0°C to +70°C
R6522C	Ceramic	1 MHz	0°C to +70°C
R6522AC	Ceramic	2 MHz	0°C to +70°C
R6522PE	Plastic	1 MHz	-40°C to +85°C
R6522APE	Plastic	2 MHz	-40°C to +85°C
R6522CE	Ceramic	1 MHz	-40°C to +85°C
R6522ACE	Ceramic	2 MHz	-40°C to +85°C
R6522CMT	Ceramic	1 MHz	-55°C to +125°C



Basic R6522 Interface Diagram



Pin Configuration

R6522 VERSATILE INTERFACE ADAPTER (VIA)

Specifications subject to change without notice

OPERATION SUMMARY

Register Select Lines (RS0, RS1, RS2, RS3)

The four Register select lines are normally connected to the processor address bus lines to allow the processor to select the internal R6522 register which is to be accessed. The sixteen possible combinations access the registers as follows:

RS3	RS2	RS1	RS0	Register	Remarks	RS3	RS2	RS1	RS0	Register	Remarks
L	L	L	L	ORB		H	L	L	L	T2L-L	Write Latch
L	L	L	H	ORA	Controls Handshake					T2C-L	Read Counter
L	L	H	L	DDRB		H	L	L	H	T2C-H	Triggers T2L-L/T2C-L Transfer
L	L	H	H	DDRA							
						H	L	H		SR	
L	H	L	L	T1L-L	Write Latch	H	L	H	H	ACR	
				T1C-L	Read Counter	H	H	L	L	PCR	
L	H	L	H	T1C-H	Trigger T1L-L/T1C-L Transfer	H	H	L	H	IFR	
						H	H	H	L	IER	
L	H	H	L	T1L-L		H	H	H	H	ORA	No Effect on Handshake
L	H	H	H	T1L-H							

Note: L = 0.4V DC, H = 2.4V DC.

Timer 2 Control

RS3	RS2	RS1	RS0	R/W = L	R/W = H
H	L	L	L	Write T2L-L	Read T2C-L Clear Interrupt flag
H	L	L	H	Write T2C-H Transfer T2L-L to T2C-L Clear Interrupt flag	Read T2C-H

Writing the Timer 1 Register

The operations which take place when writing to each of the four T1 addresses are as follows:

RS3	RS2	RS1	RS0	Operation (R/W = L)
L	H	L	L	Write into low order latch
L	H	L	H	Write into high order latch Write into high order counter Transfer low order latch into low order counter Reset T1 interrupt flag
L	H	H	L	Write low order latch
X	H	H	H	Write high order latch Reset T1 interrupt flag

Reading the Timer 1 Registers

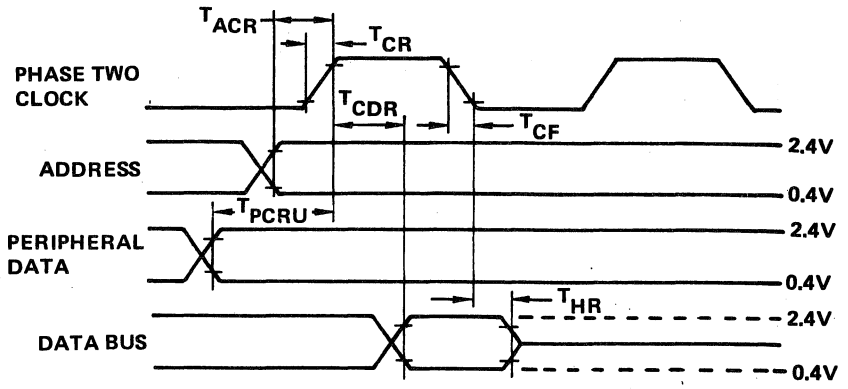
For reading the Timer 1 registers, the four addresses relate directly to the four registers as follows:

RS3	RS2	RS1	RS0	Operation (R/W = H)
L	H	L	L	Read T1 low order counter Reset T1 interrupt flag
L	H	L	H	Read T1 high order counter
L	H	H	L	Read T1 low order latch
L	H	H	H	Read T1 high order latch

TIMING CHARACTERISTICS

Read Timing Characteristics (loading 130 pF and one TTL load)

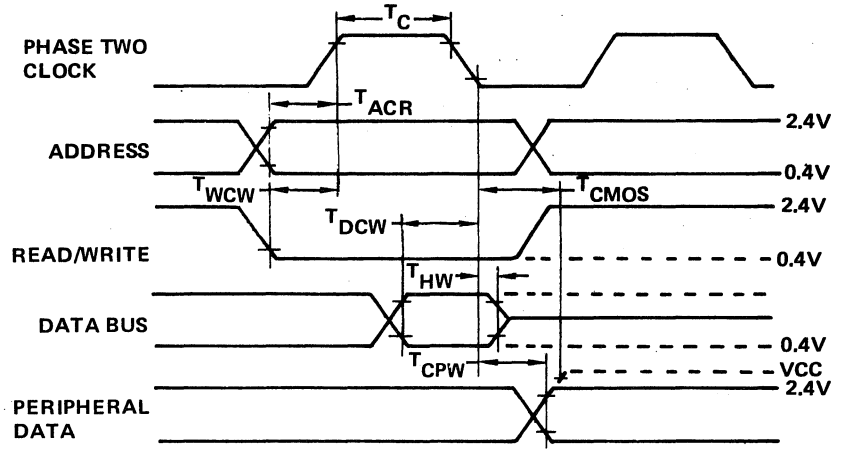
Parameter	Symbol	Min	Typ	Max	Unit
Delay time, address valid to clock positive transition	T_{ACR}	180	–	–	nS
Delay time, clock positive transition to data valid on bus	T_{CDR}	–	–	395	nS
Peripheral data setup time	T_{PCR}	300	–	–	nS
Data bus hold time	T_{HR}	10	–	–	nS
Rise and fall time for clock input	T_{RC} T_{RF}	–	–	25	nS



Read Timing Characteristics

Write Timing Characteristics

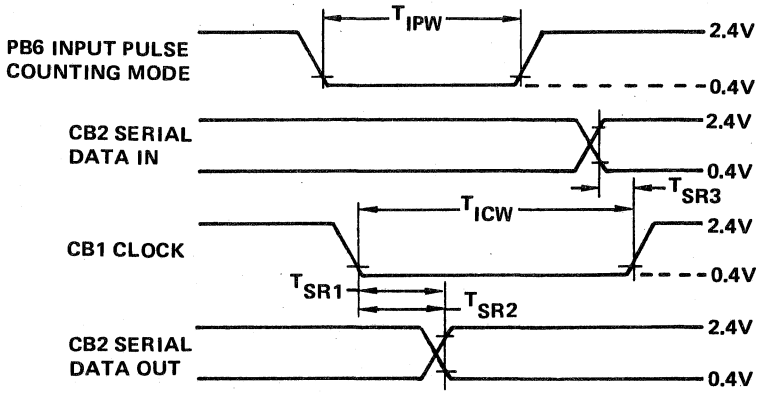
Parameter	Symbol	Min	Typ	Max	Unit
Enable pulse width	T_C	0.47	–	25	μS
Delay time, address valid to clock positive transition	T_{ACW}	180	–	–	nS
Delay time, data valid to clock negative transition	T_{DCW}	300	–	–	nS
Delay time, read/write negative transition to clock positive transition	T_{WCW}	180	–	–	nS
Data bus hold time	T_{HW}	10	–	–	nS
Delay time, Enable negative transition to peripheral data valid	T_{CPW}	–	–	1.0	μS
Delay time, clock negative transition to peripheral data valid CMOS (VCC - 30%)	T_{CMOS}	–	–	2.0	μS



Write Timing Characteristics

I/O Timing Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
Rise and fall time for CA1, CB1, CA2 and CB2 input signals	T_{RF}	–	–	1.0	μs
Delay time, clock negative transition to CA2 negative transition (read handshake or pulse mode)	T_{CA2}	–	–	1.0	μs
Delay time, clock negative transition to CA2 positive transition (pulse mode)	T_{RS1}	–	–	1.0	μs
Delay time, CA1 active transition to CA2 positive transition (handshake mode)	T_{RS2}	–	–	2.0	μs
Delay time, clock positive transition to CA2 or CB2 negative transition (write handshake)	T_{WHS}	–	–	1.0	μs
Delay time, peripheral data valid to CB2 negative transition	T_{DC}	0	–	1.5	μs
Delay time, clock positive transition to CA2 or CB2 positive transition (pulse mode)	T_{RS3}	–	–	1.0	μs
Delay time, CB1 active transition to CA2 or CB2 positive transition (handshake mode)	T_{RS4}	–	–	2.0	μs
Delay time, peripheral data valid to CA1 or CB1 active transition (input latching)	T_{IL}	300	–	–	ns
Delay time CB1 negative transition to CB2 data valid (internal SR clock, shift out)	T_{SR1}	–	–	300	ns
Delay time, negative transition of CB1 input clock to CB2 data valid (external clock, shift out)	T_{SR2}	–	–	300	ns
Delay time, CB2 data valid to positive transition of CB1 clock (shift in, internal or external clock)	T_{SR3}	–	–	300	ns
Pulse Width – PB6 Input Pulse	T_{IPW}	2	–	–	μs
Pulse Width – CB1 Input Clock	T_{ICW}	2	–	–	μs
Pulse Spacing – PB6 Input Pulse	I_{IPS}	2	–	–	μs
Pulse Spacing – CB1 Input Pulse	I_{ICS}	2	–	–	μs



I/O Timing Characteristics

Timer 1 Operating Modes

Two bits are provided in the Auxiliary Control Register to allow selection of the T1 operating modes. These bits and the four possible modes are as follows:

ACR7 Output Enable	ACR6 "Free-Run" Enable	Mode
0	0	Generate a single time-out interrupt each time T1 is loaded
0	1	Generate continuous interrupts
1	0	Generate a single interrupt and an output pulse on PB7 for each T1 load operation
1	1	Generate continuous interrupts and a square wave output on PB7

FUNCTION CONTROL

Control of the various functions and operating modes within the R6522 is accomplished primarily through two registers, the Peripheral Control Register (PCR), and the Auxiliary Control Register (ACR). The PCR is used primarily to select the operating mode for the four peripheral control pins. The Auxiliary Control Register selects the operating mode for the Interval Timers (T1, T2), and the Serial Port (SR).

Peripheral Control Register

The Peripheral Control Register is organized as follows:

Bit #	7	6	5	4	3	2	1	0
Function	CB2 Control			CB1 Control	CA2 Control			CA1 Control

Typical functions are shown below:

PCR3	PCR2	PCR1	Mode
0	0	0	Input mode — Set CA2 interrupt flag (IFR0) on a negative transition of the input signal. Clear IFR0 on a read or write of the Peripheral A Output Register.
0	0	1	Independent interrupt input mode — Set IFR0 on a negative transition of the CA2 input signal. Reading or writing ORA does not clear the CA2 interrupt flag.
0	1	0	Input mode — Set CA2 interrupt flag on a positive transition of the CA2 input signal. Clear IFR0 with a read or write of the Peripheral A Output Register.
0	1	1	Independent interrupt input mode — Set IFR0 on a positive transition of the CA2 input signal. Reading or writing ORA does not clear the CA2 interrupt flag.
1	0	0	Handshake output mode — Set CA2 output low on a read or write of the Peripheral A Output Register. Reset CA2 high with an active transition on CA1.
1	0	1	Pulse output mode — CA2 goes low for one cycle following a read or write of the Peripheral A Output Register.
1	1	0	Manual output mode — The CA2 output is held low in this mode.
1	1	1	Manual output mode — The CA2 output is held high in this mode.

Auxiliary Control Register

Many of the functions in the Auxiliary Control Register have been discussed previously. However, a summary of this register is presented here as a convenient reference for the R6522 user. The Auxiliary Control Register is organized as follows:

Bit #	7	6	5	4	3	2	1	0
Function	T1 Control		T2 Control	Shift Register Control			PB Latch Enable	PA Latch Enable

Shift Register Control

The Shift Register operating mode is selected as follows:

ACR4	ACR3	ACR2	Mode
0	0	0	Shift Register Disabled.
0	0	1	Shift in under control of Timer 2.
0	1	0	Shift in under control of system clock.
0	1	1	Shift in under control of external clock pulses.
1	0	0	Free-running output at rate determined by Timer 2.
1	0	1	Shift out under control of Timer 2.
1	1	0	Shift out under control of the system clock.
1	1	1	Shift out under control of external clock pulses.

T2 Control

Timer 2 operates in two modes. If ACR5 = 0, T2 acts as an interval timer in the one-shot mode. If ACR5 = 1, Timer 2 acts to count a predetermined number of pulses on pin PB6.

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R6500 Microcomputer System
DATA SHEET

CRT CONTROLLER (CRTC)

DESCRIPTION

The R6545-1 CRT Controller (CRTC) is designed to interface an 8-bit microprocessor to CRT raster scan video displays, and adds an advanced CRT controller to the established and expanding line of R6500 products.

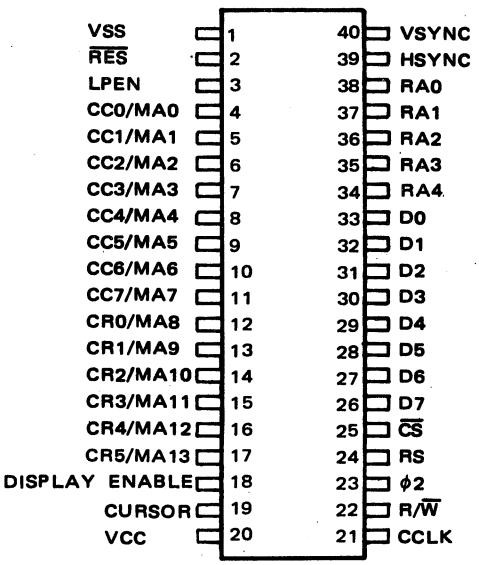
The R6545-1 provides refresh memory addresses and character generator row addresses which allow up to 16K characters with 32 scan lines per character to be addressed. A major advantage of the R6545-1 is that the refresh memory may be addressed in either straight binary or by row/column.

Other functions in the R6545-1 include an internal cursor register which generates a cursor output when its contents are equal to the current refresh address. Programmable cursor start and end registers allow a cursor of up to the full character scan in height to be placed on any scan lines of the character. Variable cursor display blink rates are provided. A light pen strobe input allows capture of the current refresh address in an internal light pen register. The refresh address lines are configured to provide direct dynamic memory refresh.

All timing for the video refresh memory signals is derived from the character clock input. Shift register, latch, and multiplex control signals (when needed) are provided by external high-speed timing. The mode control register allows non-interlaced video display modes at 50 or 60 Hz refresh rate. The internal status register may be used to monitor the R6545-1 operation. The $\overline{RES}$ input allows the CRTC-generated field rate to be dynamically-synchronized with line frequency jitter.

FEATURES

- Compatible with 8-bit microprocessors
- Up to 2.5 MHz character clock operation
- Refresh RAM may be configured in row/column or straight binary addressing
- Alphanumeric and limited graphics capability
- Up and down scrolling by page, line, or character
- Programmable Vertical Sync Width
- Fully programmable display (rows, columns, character matrix)
- Non-interlaced scan
- 50/60 Hz operation
- Fully programmable cursor
- Light pen register
- Addresses refresh RAM to 16K characters
- No external DMA required
- Internal status register
- 40-Pin ceramic or plastic DIP
- Pin-compatible with MC6845
- Single +5 ±5% Volt Power Supply



R6545-1 Pin Configuration

ORDERING INFORMATION

Part Number	Package Type	Frequency	Temperature Range
R6545-1P	Plastic	1 MHz	0°C to +70°C
R6545-1AP	Plastic	2 MHz	0°C to +70°C
R6545-1C	Ceramic	1 MHz	0°C to +70°C
R6545-1AC	Ceramic	2 MHz	0°C to +70°C

CRT CONTROLLER (CRTC)

Specifications subject to change without notice
Document No. 29000 D67
December 1980

INTERFACE SIGNAL DESCRIPTION

CPU INTERFACE

ϕ2 (Phase 2 Clock)

The input clock is the system Phase 2 (ϕ2) clock and is used to trigger all data transfers between the system processor (CPU) and the R6545-1. Since there is no maximum limit to the allowable ϕ2 clock time, it is not necessary for it to be a continuous clock. This capability permits the R6545-1 to be easily interfaced to non-6500 compatible microprocessors.

R/$\overline{W}$ (Read/Write)

The R/$\overline{W}$ input signal generated by the processor is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the R6545-1, a low on the R/$\overline{W}$ pin allows data on data lines D0-D7 to be written into the R6545-1.

$\overline{CS}$ (Chip Select)

The Chip Select input is normally connected to the processor address bus either directly or through a decoder. The R6545-1 is selected when $\overline{CS}$ is low.

RS (Register Select)

The Register Select input is used to access internal registers. A low on this pin permits writes (R/$\overline{W}$ = low) into the Address Register and reads (R/$\overline{W}$ = high) from the Status Register. The contents of the Address Register is the identity of the register accessed when RS is high.

D0-D7 (Data Bus)

D0-D7 are the eight data lines used to transfer data between the processor and the R6545-1. These lines are bidirectional and are normally high-impedance except during read cycles when the chip is selected ($\overline{CS}$ = low).

VIDEO INTERFACE

HSYNC (Horizontal Sync)

The HSYNC signal is an active-high output used to determine the horizontal position of displayed text. It may drive a CRT monitor directly or may be used for composite video generation. HSYNC time position and width are fully programmable.

VSYNC (Vertical Sync)

The VSYNC signal is an active high output used to determine the vertical position of displayed text. Like HSYNC, VSYNC may be used to drive a CRT monitor or composite video generation circuits. VSYNC time position and width are both programmable.

DISPLAY ENABLE (Display Enable)

The DISPLAY ENABLE signal is an active-high output used to indicate when the R6545-1 is generating active display information. The number of horizontal display characters per row and the number of vertical display rows are both fully programmable and together are used to generate the DISPLAY ENABLE signal. DISPLAY ENABLE can be delayed one character time by setting bit 4 of R8 equal to 1.

CURSOR (Cursor Coincidence)

The CURSOR signal is an active-high output used to indicate when the scan coincides with the programmed cursor position. The cursor position may be programmed to be any character in the address field. Furthermore, within the character, the cursor may be programmed to be any block of scan lines, since the start scan line and the end scan line are both programmable. The cursor position may be delayed by one character time by setting Bit 5 of R8 to A "1".

LPEN (Light Pen Strobe)

The LPEN signal is an edge-sensitive input used to load the internal Light Pen Register with the contents of the Refresh Scan Counter at the time the active edge occurs. The active edge of LPEN is the low-to-high transition.

CCLK (Clock)

The CCLK signal is the character timing clock input and is used as the time base for all internal count/control functions.

$\overline{RES}$

The $\overline{RES}$ signal is an active-low input used to initialize all internal scan counter circuits. When $\overline{RES}$ is low, all internal counters are stopped and cleared, all scan and video outputs are low, and control registers are unaffected. $\overline{RES}$ must stay low for at least one CCLK period. All scan timing is initiated when $\overline{RES}$ goes high. In this way, $\overline{RES}$ can be used to synchronize display frame timing with line frequency. $\overline{RES}$ may also be used to synchronize multiple CRTC's in horizontal and/or vertical split screen operation.

REFRESH RAM AND CHARACTER ROM INTERFACE

MA0-MA13 (Refresh RAM Address Lines)

These 14 signals are active-high outputs used to address the Refresh RAM for character storage and display operations. The starting scan address is fully programmable and the ending scan address is determined by the total number of characters displayed, which is also programmable, in terms of characters/line and lines/frame.

There are two selectable address modes for MA0-MA13:

In the straight binary mode (R8, Mode Control, bit 2 = "0"), characters are stored in successive memory locations. Thus, the software must be designed such that row and column character coordinates are translated into sequentially-numbered addresses. In the row/column mode (R8, Mode Control, bit 2 = "1"), MA0-MA7 become column addresses CC0-CC7 and MA8-MA13 become row addresses CR0-CR5. In this case, the software can manipulate characters in terms of row and column locations, but additional address compression circuits are needed to convert the CC0-CC7 and CR0-CR5 addresses into a memory-efficient binary address scheme.

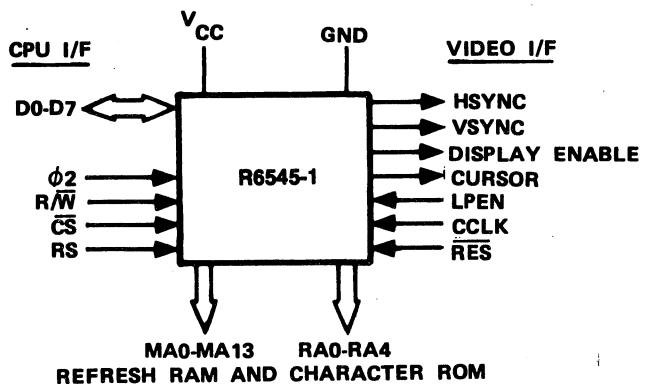
RA0-RA4 (Raster Address Lines)

These 5 signals are active-high outputs used to select each raster scan within an individual character row. The number of raster scan lines is programmable and determines the character height, including spaces between character rows.

INTERNAL REGISTER ORGANIZATION

$\overline{CS}$	RS	Address Register 4	3	2	1	0	Reg. No.	Register Name	Register Units	Read (R/$\overline{W}$ = High)	Write (R/$\overline{W}$ = Low)	Register Bit 7	6	5	4	3	2	1	0
1	X	X	X	X	X	X	X												
0	0	X	X	X	X	X	X	Address Register	Register No.		✓				4	3	2	1	0
0	0	X	X	X	X	X	X	Status Register	–	✓			6	5					
0	1	0	0	0	0	0	R0	Horizontal Total Char	No. of Characters/Row		✓	7	6	5	4	3	2	1	0
0	1	0	0	0	0	1	R1	Horizontal Displayed Char	No. of Characters/Row		✓	7	6	5	4	3	2	1	0
0	1	0	0	0	1	0	R2	Horizontal Sync Position	Character Position		✓	7	6	5	4	3	2	1	0
0	1	0	0	0	1	1	R3	YSYNC, HSYNC Widths	No. of Scan Lines, Characters		✓	7	6	5	4	3	2	1	0
0	1	0	0	1	0	0	R4	Vertical Total Rows	No. of Character Rows		✓		6	5	4	3	2	1	0
0	1	0	0	1	0	1	R5	Vertical Total Adjust Lines	No. of Scan Lines		✓				4	3	2	1	0
0	1	0	0	1	1	0	R6	Vertical Displayed Rows	No. of Character Rows		✓		6	5	4	3	2	1	0
0	1	0	0	1	1	1	R7	Vertical Sync Position	No. of Character Rows		✓		6	5	4	3	2	1	0
0	1	0	1	0	0	0	R8	Mode Control	–		✓	7	6	5	4	3	2	1	0
0	1	0	1	0	0	1	R9	Scan Line	No. of Scan Lines		✓				4	3	2	1	0
0	1	0	1	0	1	0	R10	Cursor Start Line	Scan Line No.		✓		6	5	4	3	2	1	0
0	1	0	1	0	1	1	R11	Cursor End Line	Scan Line No.		✓				4	3	2	1	0
0	1	0	1	1	0	0	R12	Display Start Address (H)	–		✓			5	4	3	2	1	0
0	1	0	1	1	0	1	R13	Display Start Address (L)	–		✓	7	6	5	4	3	2	1	0
0	1	0	1	1	1	0	R14	Cursor Position Address (H)	–	✓	✓			5	4	3	2	1	0
0	1	0	1	1	1	1	R15	Cursor Position Address (L)	–	✓	✓	7	6	5	4	3	2	1	0
0	1	1	0	0	0	0	R16	Light Pen Register (H)	–	✓				5	4	3	2	1	0
0	1	1	0	0	0	1	R17	Light Pen Register (L)	–	✓		7	6	5	4	3	2	1	0

Table 1. Overall Register Structure and Addressing



R6545-1 Interface Diagram

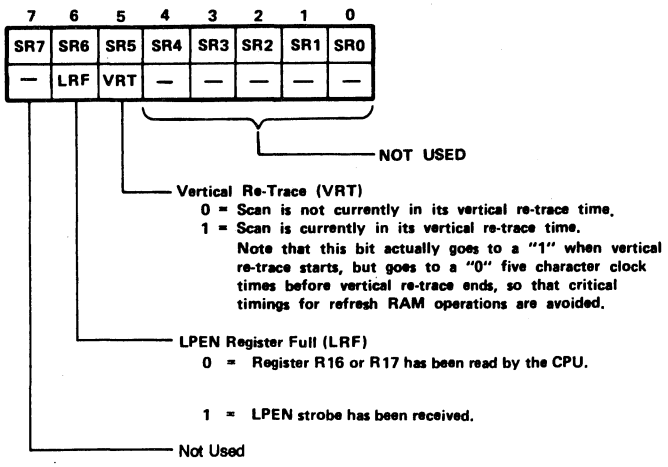
INTERNAL REGISTER DESCRIPTION

ADDRESS REGISTER

This 5-bit write-only register is used as a "pointer" to direct CRTC/CPU data transfers within the CRTC. Its contents is the number of the desired register (0-17). When $\overline{CS}$ and RS are low, then this register may be loaded; when $\overline{CS}$ is low and RS is high, then the register selected is the one whose identity is stored in this address register.

STATUS REGISTER (SR)

This 8-bit register contains the status of the CRTC. Only two bits are assigned, as follows:



NOTE: The Status Register takes the State, | – | 0 | 1 | – | – | – | – | – | immediately after power (V_{CC}) turn-on.

R0—HORIZONTAL TOTAL CHARACTERS

This 8-bit write-only register contains the total of displayed and non-displayed characters, minus one, per horizontal line. The frequency of HSYNC is thus determined by this register.

R1—HORIZONTAL DISPLAYED CHARACTERS

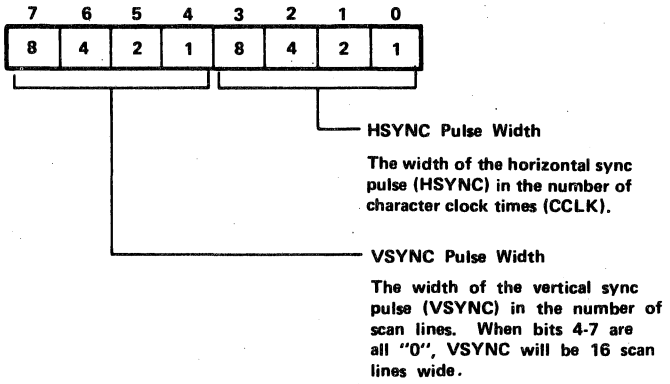
This 8-bit write-only register contains the number of displayed characters per horizontal line.

R2—HORIZONTAL SYNC POSITION

This 8-bit write-only register contains the position of the horizontal SYNC on the horizontal line, in terms of the character location number on the line. The position of the HSYNC determines the left to right location of the displayed text on the video screen. In this way, the side margins are adjusted.

R3—HORIZONTAL AND VERTICAL SYNC WIDTHS

This 8-bit write-only register contains the widths of both HSYNC and VSYNC, as follows:



Control of these parameters allows the R6545-1 to be interfaced to a variety of CRT monitors, since the HSYNC and VSYNC timing signals may be accommodated without the use of external one shot timing.

R4—VERTICAL TOTAL ROWS

The Vertical Total Register is a 7-bit register containing the total number of character rows in a frame, minus one. This register, along with R5, determines the overall frame rate, which should be close to the line frequency to ensure flicker-free appearance. If the frame time is adjusted to be longer than the period of the line frequency, then $\overline{RES}$ may be used to provide absolute synchronism.

R5—VERTICAL TOTAL LINE ADJUST

The Vertical Total Line Adjust Register (R5) is a 5-bit write-only register containing the number of additional scan lines needed to complete an entire frame scan and is intended as a fine adjustment for the video frame time.

R6—VERTICAL DISPLAYED ROWS

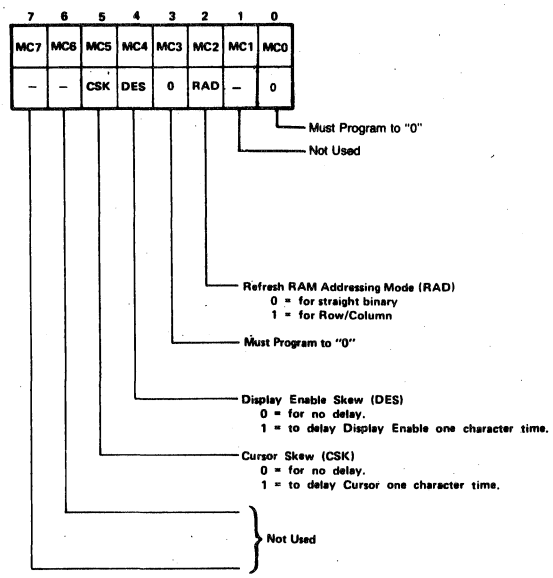
This 7-bit write-only register contains the number of displayed character rows in each frame.

R7—VERTICAL SYNC POSITION

This 7-bit write-only register is used to select the character row time at which the vertical SYNC pulse is desired to occur and, thus, is used to position the displayed text in the vertical direction.

R8—MODE CONTROL (MC)

This 8-bit write-only register selects the operating modes of the R6545-1, as follows:



R9—ROW SCAN LINES

This 5-bit write-only register contains the number of scan lines, minus one, per character row, including spacing.

R10—CURSOR START LINE
R11—CURSOR END LINE

These 5-bit write-only registers select the starting and ending scan lines for the cursor. In addition, bits 5 and 6 of R10 are used to select the cursor blink mode, as follows:

Bit 6	Bit 5	Cursor Blink Mode
0	0	Display Cursor Continuously
0	1	Blank Cursor Continuously
1	0	Blink Cursor at 1/16 Field Rate
1	1	Blink Cursor at 1/32 Field Rate

R12—DISPLAY START ADDRESS HIGH
R13—DISPLAY START ADDRESS LOW

These registers form a 14-bit register whose contents is the memory address of the first character of the displayed scan (the character on the top left of the video display, as in Figure 1). Subsequent memory addresses are generated by the R6545-1 as a result of CCLK input pulses. Scrolling of the display is accomplished by changing R12 and R13 to the memory address associated with the first character of the desired line of text to be displayed first. Entire pages of text may be scrolled or changed as well via R12 and R13.

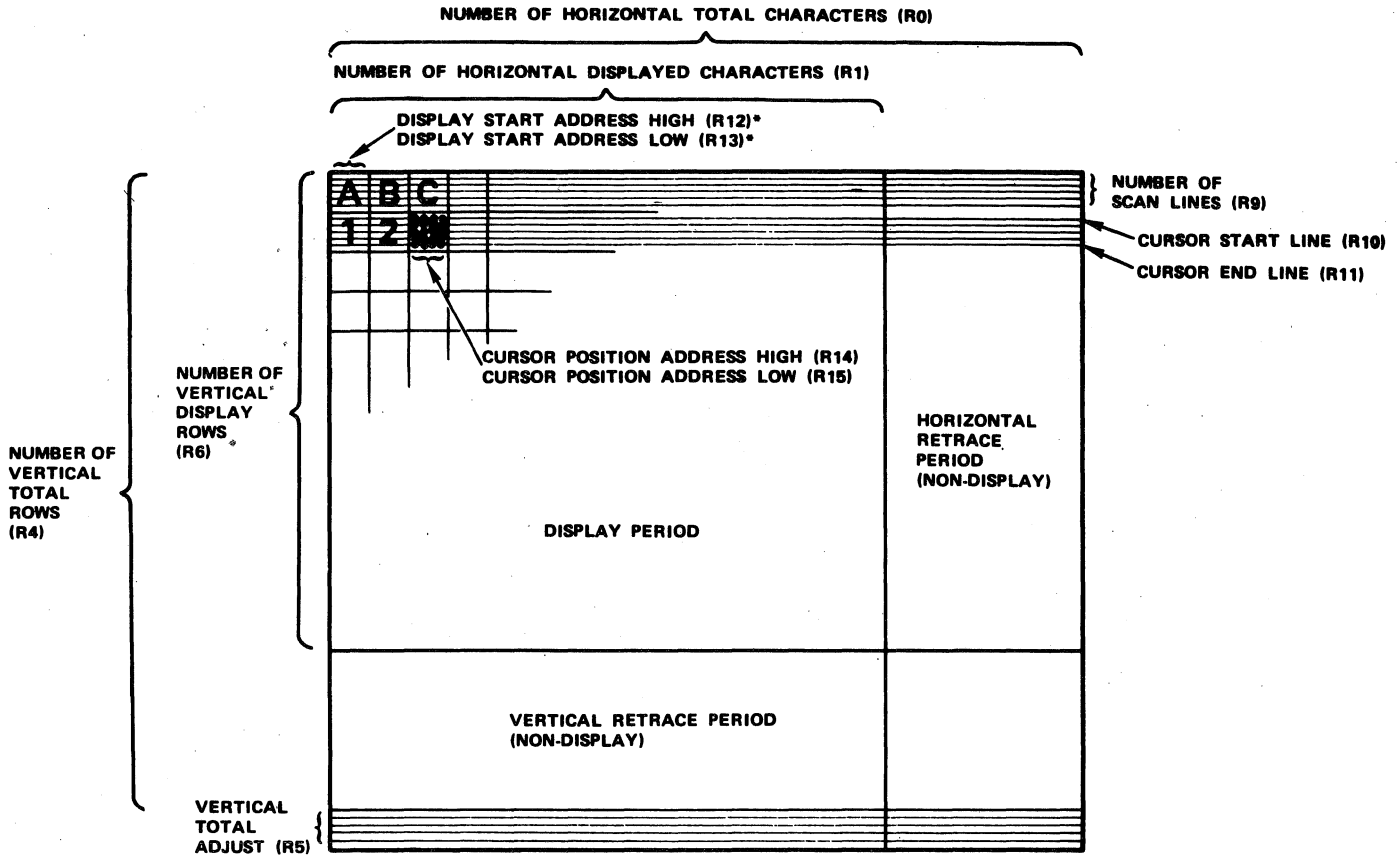


Figure 1. Video Display Format

R14—CURSOR POSITION HIGH
R15—CURSOR POSITION LOW

These registers form a 14-bit register whose contents is the memory address of the current cursor position. When the video display scan counter (MA lines) matches the contents of this register, and when the scan line counter (RA lines) falls within the bounds set by R10 and R11, then the CURSOR output becomes active. Bit 5 of the Mode Control Register (R8) may be used to delay the CURSOR output by a full CCLK time to accommodate slow access memories.

R16—LIGHT PEN HIGH
R17—LIGHT PEN LOW

These registers form a 14-bit register whose contents is the light pen strobe position, in terms of the video display address at which the strobe occurred. When the LPEN input changes from low to high, then, on the next negative-going edge of CCLK, the contents of the internal scan counter is stored in registers R16 and R17.

REGISTER FORMATS

Register pairs R12/R13, R14/R15, and R16/R17 are formatted in one of two ways:

(1) Straight binary, if register R8, bit 2 = "0".

(2) Row/Column, if register R8, bit 2 = "1". In this case the low byte is the Character Column and the high byte is the Character Row.

DESCRIPTION OF OPERATION

VIDEO DISPLAY

Figure 1 indicates the relationship of the various program registers in the R6545-1 and the resultant video display.

Non-displayed areas of the Video Display are used for horizontal and vertical retrace functions of the CRT monitor. The horizontal and vertical sync signals, HSYNC and VSYNC, are programmed to occur during these intervals and are used to trigger the retrace in the CRT monitor. The pulse widths are constrained by the monitor requirements. The time position of the pulses may be adjusted to vary the display margins (left, right, top, and bottom).

REFRESH RAM ADDRESSING

Shared Memory Mode (R8, bit 3 = "0")

In this mode, the Refresh RAM address lines (MA0-MA13) directly reflect the contents of the internal refresh scan character counter. Multiplex control, to permit addressing and selection of the RAM by both the CPU and the CRTC, must be provided external to the CRTC. In the Row/Column address mode, lines MA0-MA7 become character column addresses (CC0-CC7) and MA8-MA13 become character row addresses (CR0-CR5).

ADDRESSING MODES

Row/Column

In this mode, the CRTC address lines (MA0-MA13) are generated as 8 column (MA0-MA7) and 6 row (MA8-MA13) addresses. Extra hardware is needed to compress this addressing into a straight binary sequence in order to conserve memory in the refresh RAM.

Binary

In this mode, the CRTC address lines are straight binary and no compression circuits are needed. However, software complexity is increased since the CRT characters cannot be stored in terms of their row and column locations, but must be sequential.

USE OF DYNAMIC RAM FOR REFRESH MEMORY

The R6545-1 permits the use of dynamic RAMS as storage devices for the Refresh RAM by continuing to increment memory addresses in the non-display intervals of the scan. This is a viable technique, since the Display Enable signal controls the actual video display blanking. Figure 2 illustrates Refresh RAM addressing for the case of binary addressing for 80 columns and 24 rows with 10 non-displayed columns and 10 non-displayed rows.

TOTAL = 90

DISPLAY = 80

TOTAL = 34

DISPLAY = 24

0	1	2	3		76	77	78	79	80	81		89
80	81	82	83		156	157	158	159	160	161		169
160	161	162				237	238	239	240			249
240	241	242				317	318	319	320			329
1680	1681	1682				1757	1758	1759	1760			1769
1760	1761	1762				1837	1838	1839	1840			1849
1840	1841	1842				1917	1918	1919	1920			1929
1920	1921	1922				1997	1998	1999	2000			2009
2000	2001	2002				2077	2078	2079	2080			2089
2640	2641	2642				2717	2718	2720				2729

Figure 2. Memory Addressing Example (80 x 24)

CURSOR OPERATION

A one character wide cursor can be controlled by storing values into the Cursor Start Line (R10) and Cursor End Line (R11) registers and into the Cursor Position Address High (R14) and Cursor Position Low (R15) registers.

Bits 5 and 6 in the Cursor Start Line High Register (R10) control the cursor display and blink rate as follows:

Bit 6	Bit 5	Cursor Operating Mode
0	0	Display Cursor Continuously
0	1	Blank Cursor Continuously
1	0	Blink Cursor at 1/16 Field Rate
1	1	Blink Cursor at 1/32 Field Rate

The cursor of up to 32 characters in height can be displayed on and between the scan lines as loaded into the Cursor Start Line (R10) and Cursor End Line (R11) Registers.

The cursor is positioned on the screen by loading the Cursor Position Address High (R14) and Cursor Position Address Low (R15) registers with the desired refresh RAM address. The cursor can be positioned in any of the 16K character positions. Hardware paging and data scrolling is thus allowed without loss of cursor position. Figure 3 is an example of the display cursor scan line.

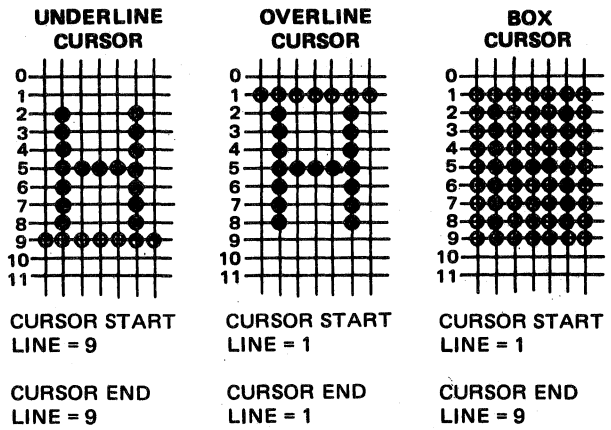


Figure 3. Cursor Display Scan Line Control Examples

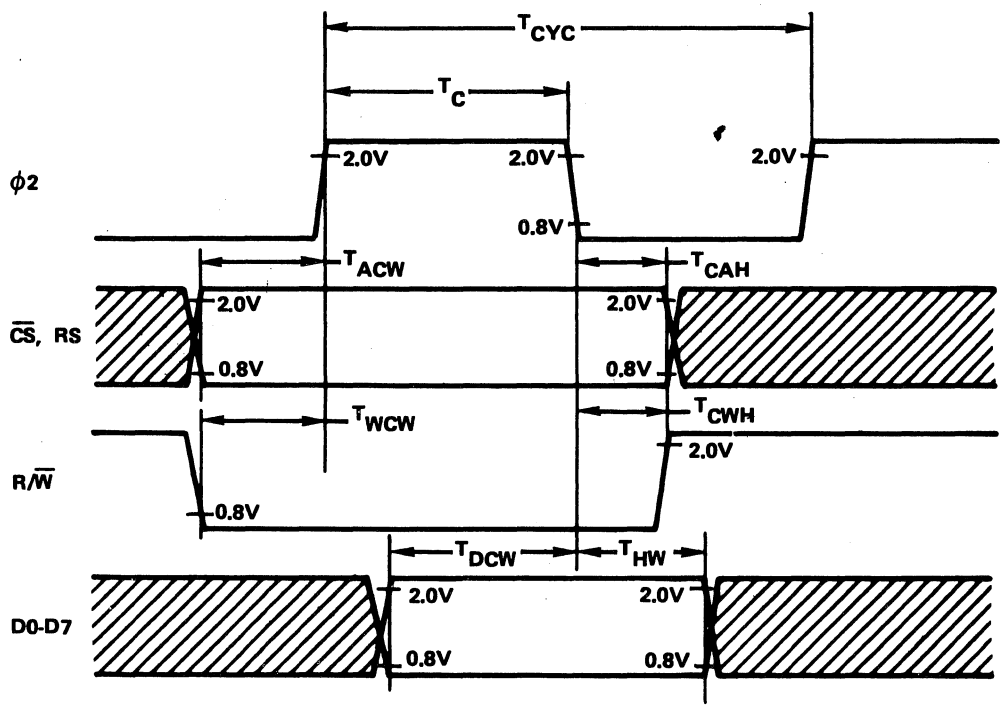
MPU WRITE TIMING CHARACTERISTICS

(V_{CC} = 5.0V ±5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristic	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Cycle Time	T_{CYC}	1.0	–	0.5	–	μs
Ø2 Pulse Width	T_C	440	–	200	–	ns
Address Set-Up Time	T_{ACW}	180	–	90	–	ns
Address Hold Time	T_{CAH}	0	–	0	–	ns
R/$\overline{W}$ Set-Up Time	T_{WCW}	180	–	90	–	ns
R/$\overline{W}$ Hold Time	T_{CWH}	0	–	0	–	ns
Data Bus Set-Up Time	T_{DCW}	265	–	100	–	ns
Data Bus Hold Time	T_{HW}	10	–	10	–	ns

(t_r and t_f = 10 to 30 ns)

WRITE CYCLE



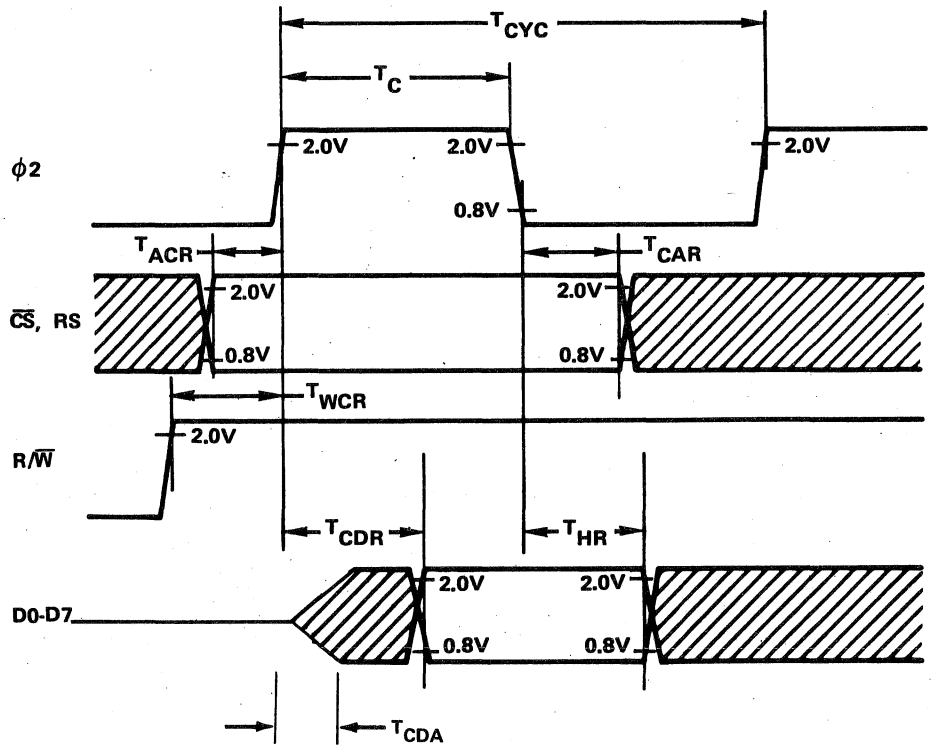
MPU READ TIMING CHARACTERISTICS

(V_{CC} = 5.0V ±5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristic	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Cycle Time	T_{CYC}	1.0	–	0.5	–	μs
Ø2 Pulse Width	T_C	440	–	200	–	ns
Address Set-Up Time	T_{ACR}	180	–	90	–	ns
Address Hold Time	T_{CAR}	0	–	0	–	ns
R/$\overline{W}$ Set-Up Time	T_{WCR}	180	–	90	–	ns
Read Access Time	T_{CDR}	–	340	–	150	ns
Read Hold Time	T_{HR}	10	–	10	–	ns
Data Bus Active Time (Invalid Data)	T_{CDA}	40	–	40	–	ns

(t_r and t_f = 10 to 30 ns)

READ CYCLE



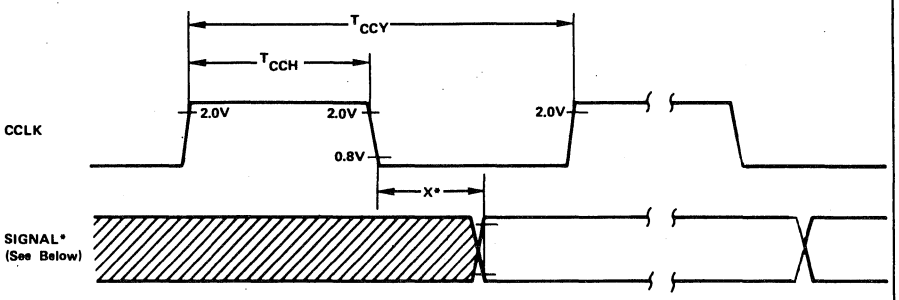
MEMORY AND VIDEO INTERFACE CHARACTERISTICS

(V_{CC} = 5.0V ±5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristics	Symbol	1 MHz		2 MHz		Units
		Min	Max	Min	Max	
Char. Clock Cycle Time	T_{CCY}	0.4	40	0.4	40	µs
Char. Clock Pulse Width	T_{CCH}	200	–	200	–	ns
MA0-MA13 Propagation Delay	T_{MAD}	–	300	–	300	ns
RA0-RA4 Propagation Delay	T_{RAD}	–	300	–	300	ns
DISPLAY ENABLE Prop. Delay	T_{DTD}	–	450	–	450	ns
HYSNC Propagation Delay	T_{HSD}	–	450	–	450	ns
VSYNC Propagation	T_{VSD}	–	450	–	450	ns
Cursor Propagation Delay	T_{CDD}	–	450	–	450	ns
LPEN Strobe Width	T_{LPH}	150	–	150	–	ns
LPEN to CCLK Delay	T_{LP1}	20	–	20	–	ns
CCLK to LPEN Delay	T_{LP2}	0	–	0	–	ns

t_r, t_f = 20 ns (max)

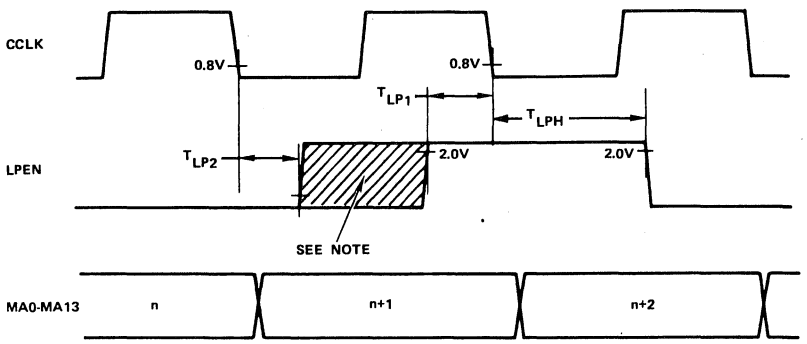
SYSTEM TIMING DEFINITIONS



*

SIGNAL	SIGNAL SYMBOL (X)
MA0-MA13	T_{MAD}
RA0-RA4	T_{RAD}
DISPLAY ENABLE	T_{DTD}
HSYNC	T_{HSD}
VSYNC	T_{VSD}
CURSOR	T_{CDD}

LIGHT PEN STROBE TIMING DEFINITIONS



NOTE:

SLASH AREA DEFINES THE "WINDOW" IN WHICH AN LPEN POSITIVE EDGE WILL CAUSE ADDRESS N+2 TO LOAD INTO LIGHT PEN REGISTER. TRANSITIONS ON EITHER SIDE OF THIS "WINDOW" WILL RESULT IN UNPREDICTABLE VALUES BEING LOADED INTO THE LIGHT PEN REGISTER.

SPECIFICATIONS

Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{IN}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_{OP}	0 to +70	^{o}C
Storage Temperature	T_{STG}	-55 to 150	^{o}C

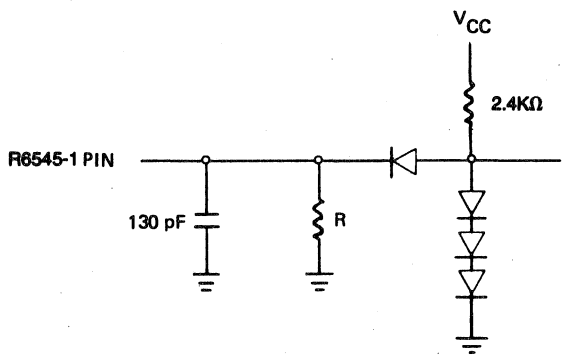
All inputs contain protection circuitry to prevent damage due to high static discharges. Care should be taken to prevent unnecessary application of voltages in excess of the allowable limits.

Electrical Characteristics

(V_{CC} = 5.0V ±5%, T_A = 0-70°C, unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	2.0	V_{CC}	Vdc
Input Low Voltage	V_{IL}	0.3	0.8	Vdc
Input Leakage (Ø2, R/$\overline{W}$, $\overline{RES}$, $\overline{CS}$, RS, LPEN, CCLK)	I_{IN}	–	2.5	µAdc
Three-State Input Leakage (D0-D7) (V_{IN} = 0.4 to 2.4V)	I_{TSI}	–	10.0	µAdc
Output High Voltage I_{LOAD} = 205 µAdc (D0-D7) I_{LOAD} = 100 µAdc (all others)	V_{OH}	2.4	–	Vdc
Output Low Voltage I_{LOAD} = 1.6 mAdc	V_{OL}	–	0.4	Vdc
Power Dissipation	P_D	–	1000	mW
Input Capacitance				
Ø2, R/$\overline{W}$, $\overline{RES}$, $\overline{CS}$, RS, LPEN, CCLK	C_{IN}	–	10.0	pF
D0-D7		–	12.5	pF
Output Capacitance	C_{OUT}	–	10.0	pF

TEST LOAD



R=11KΩ FOR D0-D7
=24KΩ FOR ALL OTHER OUTPUTS

Rockwell

R6500 Microcomputer System
DATA SHEET

Asynchronous Communication Interface Adapter (ACIA)

The R6551 Asynchronous Communication Interface Adapter (ACIA) provides a program-controlled interface between 8-bit microprocessor-based systems and serial communication data sets and modems.

With its on-chip baud rate generator, the R6551 is capable of transmitting at 15 different program-selectable rates between 50 baud and 19,200 baud, and receiving at either the transmit rate or at 16 times an external clock rate. The R6551 has programmable word lengths of 5, 6, 7, or 8 bits; even, odd or no parity; 1, 1-1/2 or 2 stop bits.

With the R6551, a crystal is the only required external support component — eliminating the multiple-component support that is typically needed.

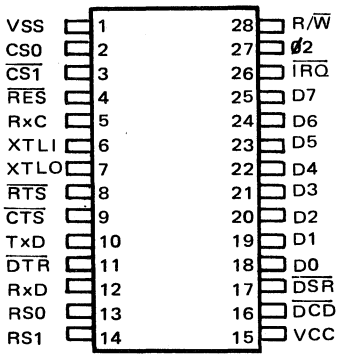
In addition, the R6551 is designed for maximum programmed control from the CPU, to simplify hardware implementation. A control register and a separate command register permit the CPU to easily select the R6551's operating modes and check data, parameters and status.

FEATURES

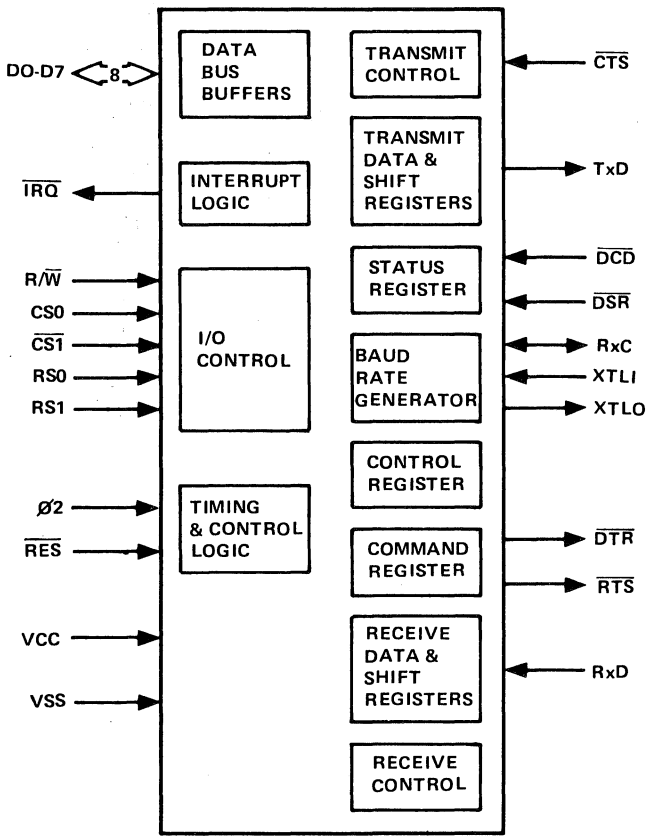
- Compatible with 8-bit microprocessors
- Full duplex or half duplex operation with buffered receiver and transmitter
- 15 programmable Baud Rates (50 to 19,200)
- Receiver data rate may be identical to baud rate or may be 16 times the external clock input
- Data set/modem control functions
- Programmable word lengths, number of stop bits, and parity bit generation and detection
- Programmable interrupt control
- Software reset
- Program-selectable serial echo mode
- Two chip selects
- 2 MHz or 1 MHz clock rate
- Single +5V ±5% power supply
- 28-pin plastic or ceramic DIP
- Full TTL compatibility

Ordering Information

Order Number	Package Type	Frequency	Temperature Range
R6551P	Plastic	1 MHz	0°C to +70°C
R6551AP	Plastic	2 MHz	0°C to +70°C
R6551C	Ceramic	1 MHz	0°C to +70°C
R6551AC	Ceramic	2 MHz	0°C to +70°C



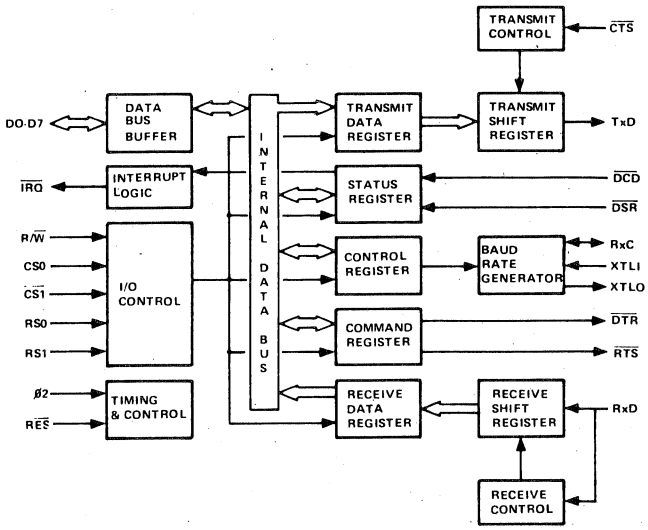
R6551 Pin Configuration



R6551 Interface Diagram

Specifications subject to change without notice
Document No. 29000 D53
Rev. 1, January 1981

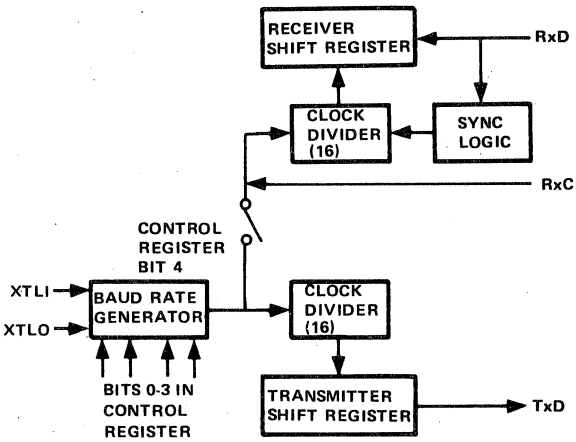
INTERNAL ORGANIZATION



R6551 Block Diagram

Transmitter/Receiver

Bits 0-3 of the Control Register select the divisor used to generate the baud rate for the Transmitter. If the Receiver clock is to use the same baud rate as the Transmitter, then RxC becomes an output pin and can be used to slave other circuits to the R6551.



Transmitter/Receiver Clock Circuits

Transmit and Receive Data Registers

These registers are used as temporary data storage for the 6551 Transmit and Receive circuits. The Transmit Data Register is characterized as follows:

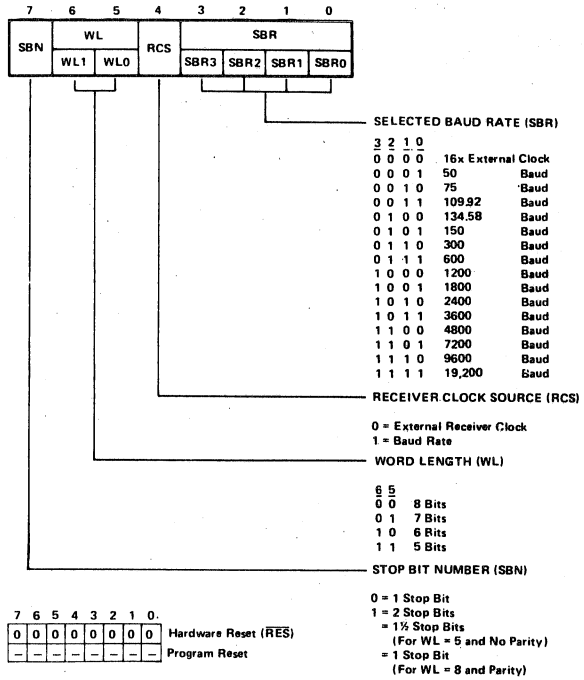
- Bit 0 is the leading bit to be transmitted.
- Unused data bits are the high-order bits and are "don't care" for transmission.

The Receive Data Register is characterized in a similar fashion:

- Bit 0 is the leading bit received.
- Unused data bits are the high-order bits and are "0" for the receiver.
- Parity bits are not contained in the Receive Data Register, but are stripped-off after being used for external parity checking. Parity and all unused high-order bits are "0".

Control Register

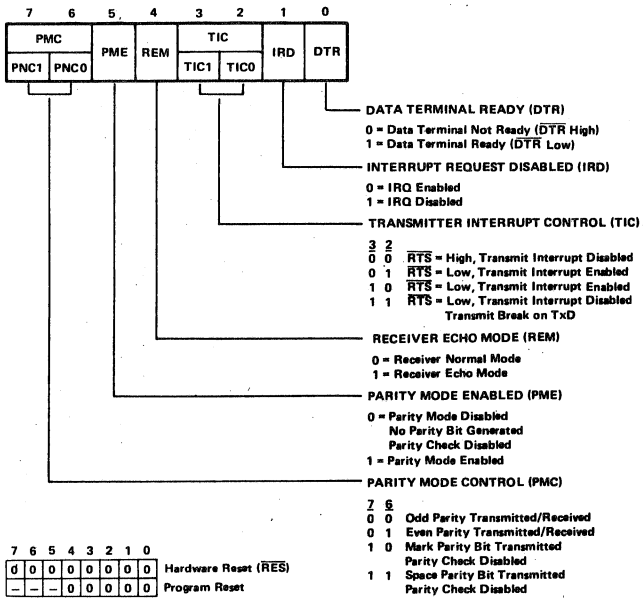
The Control Register selects the desired baud rate, frequency source, word length, and the number of stop bits.



R6551 Control Register

Command Register

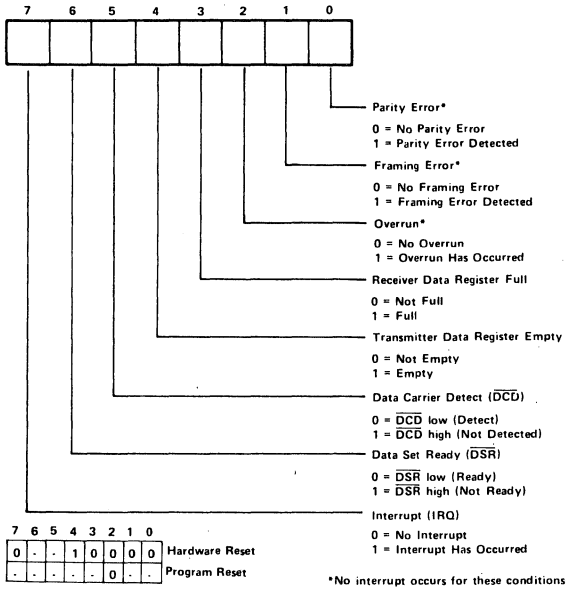
The Command Register controls specific modes and functions.



R6551 Command Register

Status Register

The Status Register reports the status of various R6551 functions



R6551 Status Register

INTERFACE SIGNAL DESCRIPTION

$\overline{\text{RES}}$ (Reset)

During system initialization a low on the $\overline{\text{RES}}$ input will cause internal registers to be cleared.

Ø2 (Input Clock)

The input clock is the system Ø2 clock and is used to synchronize all data transfers between the system microprocessor and the R6551.

R/$\overline{\text{W}}$ (Read/Write)

The R/$\overline{\text{W}}$ is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/$\overline{\text{W}}$ pin allows the processor to read the data supplied by the R6551. A low on the R/$\overline{\text{W}}$ pin allows a write to the R6551.

$\overline{\text{IRQ}}$ (Interrupt Request)

The $\overline{\text{IRQ}}$ pin is an interrupt output from the interrupt control logic. It is an open drain output, permitting several devices to be connected to the common $\overline{\text{IRQ}}$ microprocessor input. Normally a high level, $\overline{\text{IRQ}}$ goes low when an interrupt occurs.

D0-D7 (Data Bus)

The D0-D7 pins are the eight data lines used to transfer data between the processor and the R6551. These lines are bi-directional and are normally high-impedance, except during Read cycles when the R6551 is selected.

CS0, $\overline{\text{CS1}}$ (Chip Selects)

The two chip select inputs are normally connected to the processor address lines either directly or through decoders. The R6551 is selected when CS0 is high and $\overline{\text{CS1}}$ is low.

RS0, RS1 (Register Selects)

The two register select lines are normally connected to the processor address lines to allow the processor to select the various R6551 internal registers. The following table indicates the internal register select coding:

RS1	RS0	Write	Read
0	0	Transmit Data Register	Receiver Data Register
0	1	Programmed Reset (Data is "Don't Care")	Status Register
1	0	Command Register	
1	1	Control Register	

Note that only the Command and Control registers are read/write. The Programmed Reset operation does not cause any data transfer, but is used to clear Bits 0 through 4 in the Command Register and Bit 2 in the Status Register. The Programmed Reset is slightly different from the Hardware Reset ($\overline{\text{RES}}$); these differences are described in the individual register definitions.

ACIA/Modem Interface Signal Description

XTLI, XTLO (Crystal Pins)

These pins are normally directly connected to the external crystal (1.8432 MHz) used to derive the various baud rates. Alternatively, an externally generated clock may be used to drive the XTLI pin, in which case the XTLO pin must float. XTLI is the input pin for the transmit clock.

TxD (Transmit Data)

The TxD output line is used to transfer serial NRZ (non-return-to-zero) data to the modem. The LSB (least significant bit) of the Transmit Data Register is the first data bit transmitted and the rate of data transmission is determined by the baud rate selected, or under control of an external clock (as selected by the Control Register).

RxD (Receive Data)

The RxD input line is used to transfer serial NRZ data into the ACIA from the modem, LSB first. The receiver data rate is either the programmed baud rate or the rate of an externally generated receiver clock (as selected by the Control Register).

RxC (Receive Clock)

The RxC is a bi-directional pin which serves as either the receiver 16x clock input or the receiver 16x clock output. The latter mode results if the internal baud rate generator is selected for receiver data clocking.

$\overline{RTS}$ (Request to Send)

The $\overline{RTS}$ output pin is used to control the modem from the processor. The state of the $\overline{RTS}$ pin is determined by the contents of the Command Register.

$\overline{CTS}$ (Clear to Send)

The $\overline{CTS}$ input pin is used to control the transmitter operation. The enable state is with $\overline{CTS}$ low. The transmitter is automatically disabled if $\overline{CTS}$ is high.

$\overline{DTR}$ (Data Terminal Ready)

This output pin is used to indicate the status of the R6551 to the modem. A low on $\overline{DTR}$ indicates the R6551 is enabled and a high indicates it is disabled. The processor controls this pin via bit 0 of the Command Register.

$\overline{DSR}$ (Data Set Ready)

The $\overline{DSR}$ input pin is used to indicate to the R6551 the status of the modem. A low indicates the "ready" state and a high, "not-ready". $\overline{DSR}$ is a high-impedance input, and must be connected. If unused, it should be driven high or low, but not switched.

$\overline{DCD}$ (Data Carrier Detect)

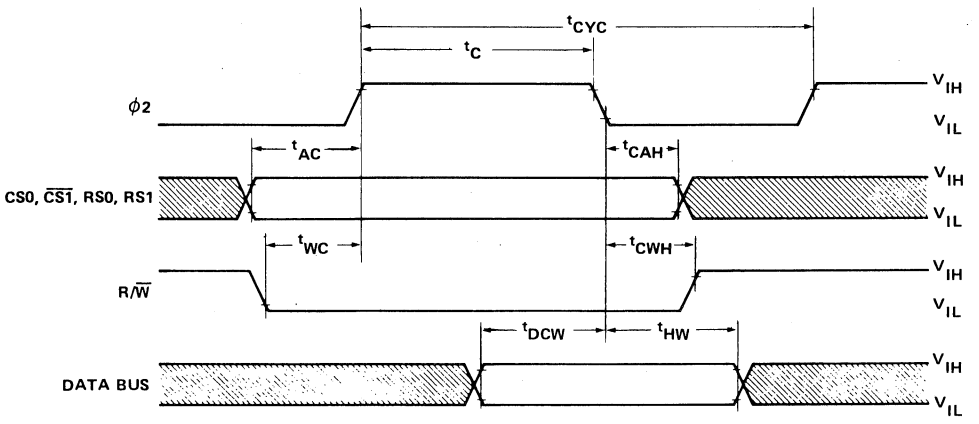
The $\overline{DCD}$ input pin is used to indicate to the R6551 the status of the carrier-detect output of the modem. A low indicates that the modem carrier signal is present and a high, that it is not. Like $\overline{DSR}$, $\overline{DCD}$ is a high-impedance input, and must be connected.

READ/WRITE CYCLE CHARACTERISTICS

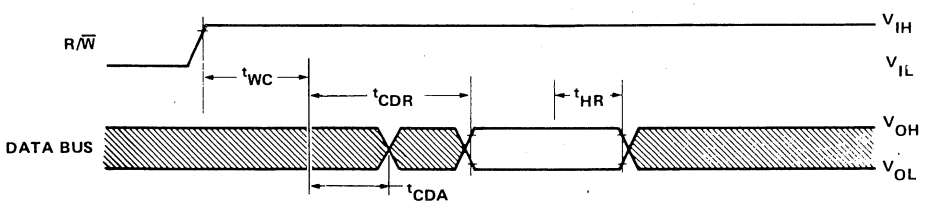
(V_{CC} = 5.0V ±5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristic	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Cycle Time	t_{CYC}	1.0	40	0.5	40	μs
Ø2 Pulse Width	t_C	400	–	200	–	ns
Address Set-Up Time	t_{AC}	120	–	70	–	ns
Address Hold Time	t_{CAH}	0	–	0	–	ns
R/$\overline{W}$ Set-Up Time	t_{WC}	120	–	70	–	ns
R/$\overline{W}$ Hold Time	t_{CWH}	0	–	0	–	ns
Data Bus Set-Up Time	t_{DCW}	150	–	60	–	ns
Data Bus Hold Time	t_{HW}	20	–	20	–	ns
Read Access Time (Valid Data)	t_{CDR}	–	200	–	150	ns
Read Hold Time	t_{HR}	20	–	20	–	ns
Bus Active Time (Invalid Data)	t_{CDA}	40	–	40	–	ns

(t_r and t_f = 10 to 30 ns)



Write Timing Characteristics



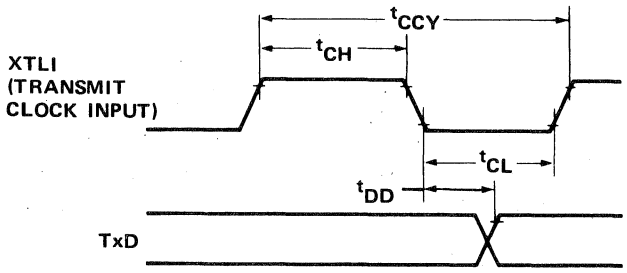
Read Timing Characteristics

TRANSMIT/RECEIVE CHARACTERISTICS

Characteristic	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Transmit/Receive Clock Rate	t_{CCY}	400*	–	400*	–	ns
Transmit/Receive Clock High Time	t_{CH}	175	–	175	–	ns
Transmit/Receive Clock Low Time	t_{CL}	175	–	175	–	ns
XTLI to TxD Propagation Delay	t_{DD}	–	500	–	500	ns
$\overline{RTS}$ Propagation Delay	t_{DLY}	–	500	–	500	ns
$\overline{IRQ}$ Propagation Delay (Clear)	t_{IRQ}	–	500	–	500	ns

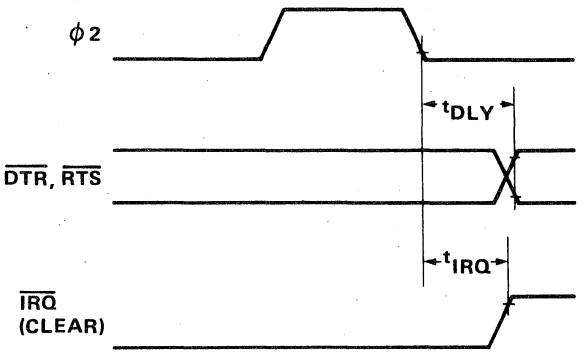
(t_r, t_f = 10 to 30 ns)

*The baud rate with external clocking is: Baud Rate = $\frac{1}{16 \times T_{CCY}}$

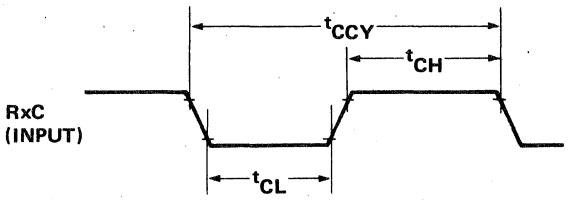


NOTE: TxD rate is 1/16 TxC rate

Transmit Timing with External Clock



Interrupt and Output Timing

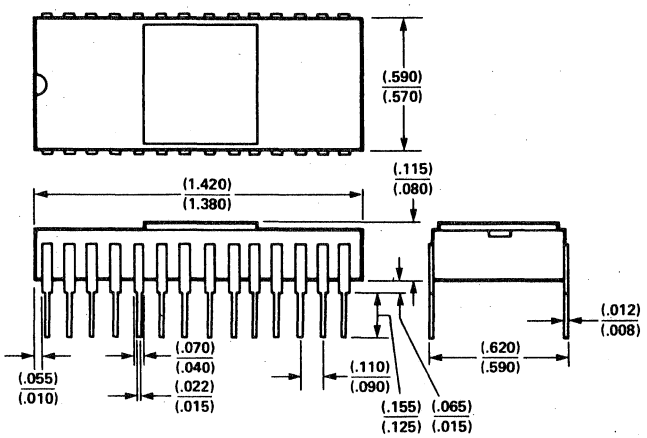


NOTE: RxD rate is 1/16 RxC rate

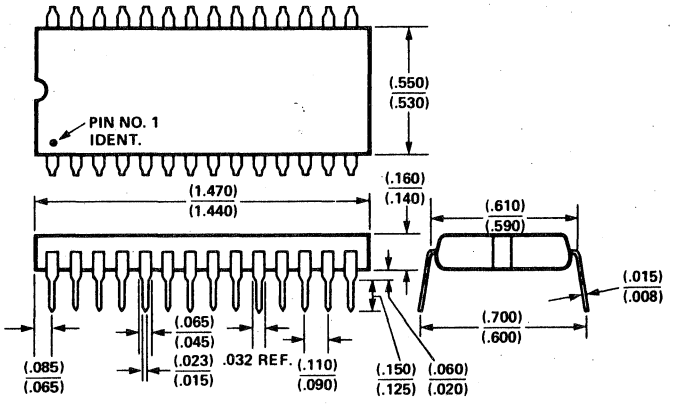
Receive External Clock Timing

PACKAGE OUTLINES

28 LEAD CERAMIC



28 LEAD PLASTIC



PRELIMINARY

8048H/8048H-1/8035HL/8035HL-1
HMOS SINGLE COMPONENT 8-BIT MICROCOMPUTER

- **8048H/8048H-1 Mask Programmable ROM**
- **8035HL/8035HL-1 CPU Only with Power Down Mode**

- **8-BIT CPU, ROM, RAM, I/O in Single Package**
- **High Performance HMOS**
- **Reduced Power Consumption**
- **1.4 usec and 1.9 usec Cycle Versions All Instructions 1 or 2 Cycles.**
- **Over 90 Instructions: 70% Single Byte**
- **1K x 8 ROM**
  64 x 8 RAM
  27 I/O Lines
- **Interval Timer/Event Counter**
- **Easily Expandable Memory and I/O**
- **Compatible with 8080/8085 Series Peripherals**
- **Two Single Level Interrupts**

The Intel® 8048H/8048H-1/8035HL/8035HL-1 are totally self-sufficient, 8-bit parallel computers fabricated on single silicon chips using Intel's advanced N-channel silicon gate HMOS process.

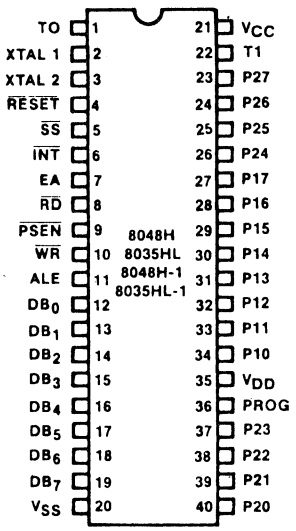
The 8048H contains a 1K X 8 program memory, a 64 X 8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to on-board oscillator and clock circuits. For systems that require extra capability the 8048H can be expanded using standard memories and MCS-80™/MCS-85™ peripherals. The 8035HL is the equivalent of the 8048H without program memory and can be used with external ROM AND RAM.

To reduce development problems to a minimum and provide maximum flexibility, a logically and functionally pin compatible version of the 8048H with UV-erasable user-programmable EPROM program memory is available. The 8748 will emulate the 8048H up to 6 MHz clock frequency with minor differences.

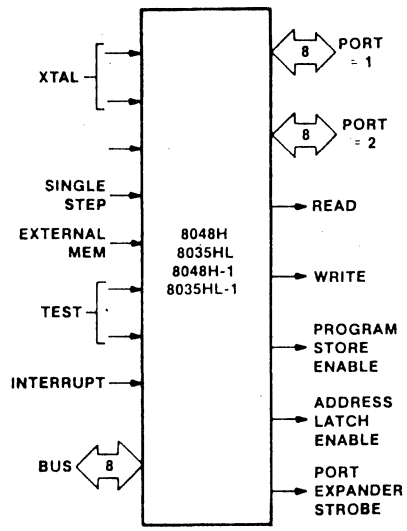
The 8048H is fully compatible with the 8048 when operated at 6 MHz.

These microcomputers are designed to be efficient controllers as well as arithmetic processors. They have extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single bit instructions and no instructions over 2 bytes in length.

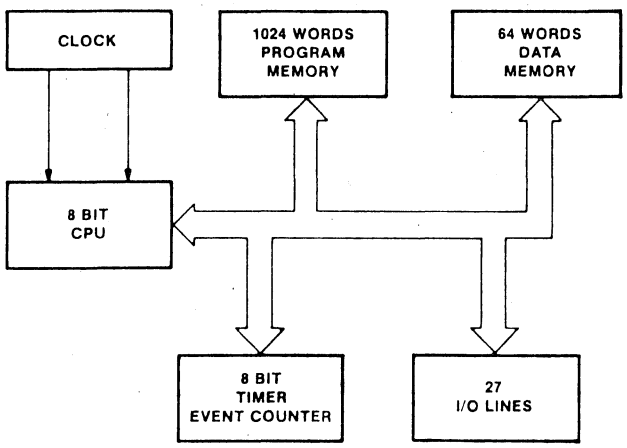
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



APPENDIX A

8035/8048/8748/ and 8049 CPU SPECIFICATIONS

This appendix contains the specifications for the CPU chips that may possibly be used with the system as its hardware design exists. Use of the 8035 is expected to compose the bulk of the applications.

PIN DESCRIPTION

Designation	Pin =	Function
V_{SS}	20	Circuit GND potential
V_{DD}	26	Low power standby pin
V_{CC}	40	Main power supply; +5V during operation.
PROG	25	Output strobe for 8243 I/O expander.
P10-P17 Port 1	27-34	8-bit quasi-bidirectional port.
P20-27 Port 2	21-24	8-bit quasi-bidirectional port.
	35-38	P20-P23 contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for 8243.
DB0-DB7 BUS	12-19	True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched.
		Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of $\overline{PSEN}$. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$, and $\overline{WR}$.
TO	1	Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 can be designated as a clock output using ENT0 CLK instruction.
T1	39	Input pin testable using the JT1, and JNT1 instructions. Can be designated the timer/counter input using the STRT CNT instruction.
$\overline{INT}$	6	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active low)
$\overline{RD}$	8	Output strobe activated during a BUS read. Can be used to enable data onto the bus from an external device.
		Used as a read strobe to external data memory. (Active low)
$\overline{RESET}$	4	Input which is used to initialize the processor. (Active low) (Non TTL V_{IH})
$\overline{WR}$	10	Output strobe during a bus write. (Active low)
		Used as write strobe to external data memory.
ALE	11	Address latch enable. This signal occurs once during each cycle and is useful as a clock output.
		The negative edge of ALE strobes address into external data and program memory.
$\overline{PSEN}$	9	Program store enable. This output occurs only during a fetch to external program memory. (Active low)
$\overline{SS}$	5	Single step input can be used in conjunction with ALE to "single step" the processor through each instruction. (Active low)
EA	7	External access input which forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification. (Active high)
XTAL1	2	One side of crystal input for internal oscillator. Also input for external source. (Non TTL V_{IH})
XTAL2	3	Other side of crystal input.

INSTRUCTION SET

Accumulator

Mnemonic	Description	Bytes	Cycles
ADD A, R	Add register to A	1	1
ADD A, @R	Add data memory to A	1	1
ADD A, # data	Add immediate to A	2	2
ADDC A, R	Add register with carry	1	1
ADDC A, @R	Add data memory with carry	1	1
ADDC A, # data	Add immediate with carry	2	2
ANL A, R	And register to A	1	1
ANL A, @R	And data memory to A	1	1
ANL A, # data	And immediate to A	2	2
ORL A, R	Or register to A	1	1
ORL A @R	Or data memory to A	1	1
ORL A, # data	Or immediate to A	2	2
XRL A, R	Exclusive or register to A	1	1
XRL A, @R	Exclusive or data memory to A	1	1
XRL, A, # data	Exclusive or immediate to A	2	2
INC A	Increment A	1	1
DEC A	Decrement A	1	1
CLR A	Clear A	1	1
CPL A	Complement A	1	1
DA A	Decimal adjust A	1	1
SWAP A	Swap nibbles of A	1	1
RL A	Rotate A left	1	1
RLC A	Rotate A left through carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through carry	1	1

Input/Output

Mnemonic	Description	Bytes	Cycles
IN A, P	Input port to A	1	2
OUTL P, A	Output A to port	1	2
ANL P, # data	And immediate to port	2	2
ORL P, # data	Or immediate to port	2	2
INS A, BUS	Input BUS to A	1	2
OUTL BUS, A	Output A to BUS	1	2
ANL BUS, # data	And immediate to BUS	2	2
ORL BUS, # data	Or immediate to BUS	2	2
MOVD A,P	Input expander port to A	1	2
MOVD P, A	Output A to expander port	1	2
ANLD P, A	And A to expander port	1	2
ORLD P, A	Or A to expander port	1	2

Registers

Mnemonic	Description	Bytes	Cycles
INC R	Increment register	1	1
INC @R	Increment data memory	1	1
DEC R	Decrement register	1	1

Branch

Mnemonic	Description	Bytes	Cycles
JMP addr	Jump unconditional	2	2
JMPP @A	Jump indirect	1	2
DJNZ R, addr	Decrement register and skip	2	2
JC addr	Jump on carry = 1	2	2
JNC addr	Jump on carry = 0	2	2
JZ addr	Jump on A zero	2	2
JNZ addr	Jump on A not zero	2	2
JTO addr	Jump on TO = 1	2	2
JNTO addr	Jump on TO = 0	2	2
JT1 addr	Jump on T1 = 1	2	2
JNT1 addr	Jump on T1 = 0	2	2
JF0 addr	Jump on F0 = 1	2	2
JF1 addr	Jump on F1 = 1	2	2
JTF addr	Jump on timer flag	2	2
JN1 addr	Jump on INT = 0	2	2
JBb addr	Jump on accumulator bit	2	2

Subroutine

Mnemonic	Description	Bytes	Cycles
CALL addr	Jump to subroutine	2	2
RETR	Return	1	2
RETR	Return and restore status	1	2

Flags

Mnemonic	Description	Bytes	Cycles
CLR C	Clear carry	1	1
CPL C	Complement carry	1	1
CLR F0	CLear flag 0	1	1
CPL F0	Complement flag 0	1	1
CLR F1	Clear flag 1	1	1
CPL F1	Complement flag 1	1	1

Data Moves

Mnemonic	Description	Bytes	Cycles
MOV A, R	Move register to A	1	1
MOV A, @R	Move data memory to A	1	1
MOV A, # data	Move immediate to A	2	2
MOV R, A	Move A to register	1	1
MOV @R, A	Move A to data memory	1	1
MOV R, # data	Move immediate to register	2	2
MOV @R, #data	Move immediate to data memory	2	2
MOV A, PSW	Move PSW to A	1	1
MOV PSW, A	Move A to PSW	1	1
XCH A, R	Exchange A and register	1	1
XCH A, @R	Exchange A and data memory	1	1
XCHD A, @R	Exchange nibble of A and register	1	
MOVX A, @R	Move external data memory to A	1	2
MOVX @R, A	Move A to external data memory	1	2
MOVP A, @A	Move to A from current page	1	2
MOVP3 A, @	Move to A from page 3	1	2

Timer/Counter

Mnemonic	Description	Bytes	Cycles
MOV A, T	Read timer/counter	1	1
MOV T, A	Load timer/counter	1	1
STRT T	Start timer	1	1
STRT CNT	Start counter	1	1
STOP TCNT	Stop timer/counter	1	1
EN TCNT1	Enable timer/counter interrupt	1	1
DIS TCNT1	Disable timer/counter interrupt	1	1

Control

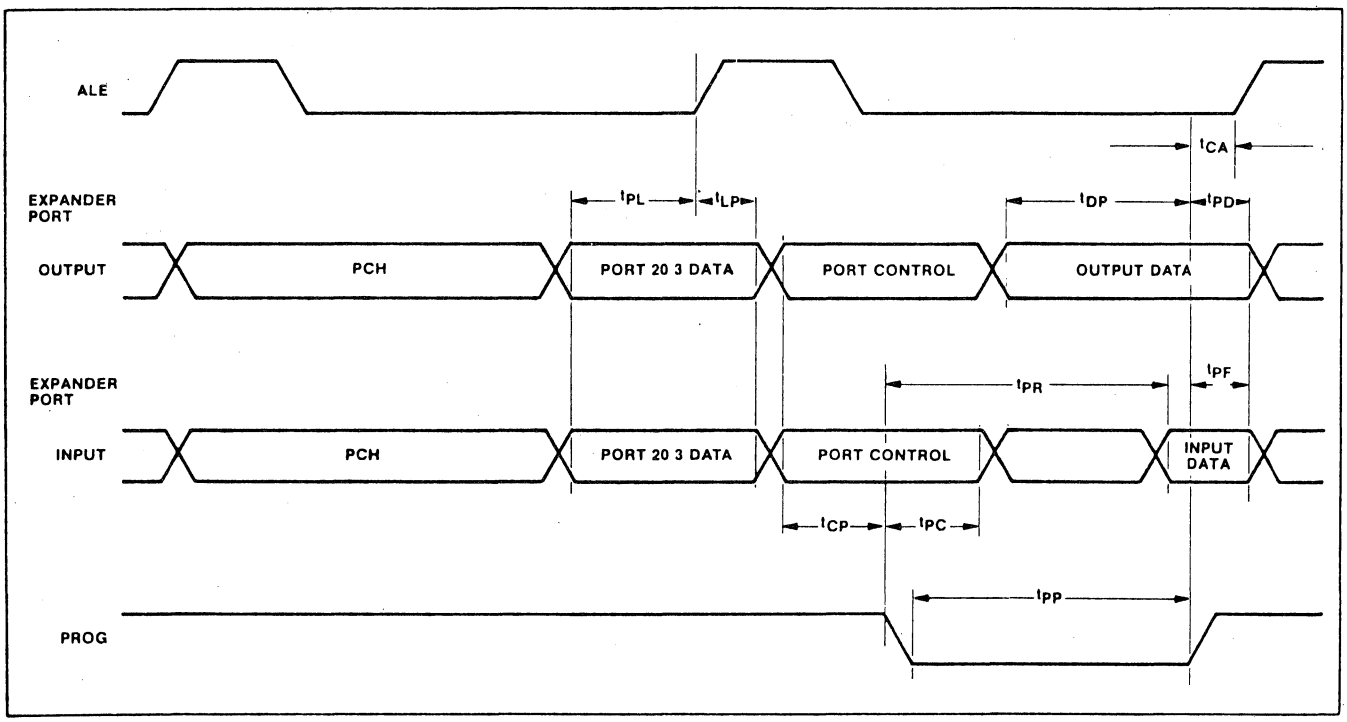
Mnemonic	Description	Bytes	Cycles
EN 1	Enable external interrupt	1	1
DIS 1	Disable external interrupt	1	1
SEL RB0	Select register bank 0	1	1
SEL RB1	Select register bank 1	1	1
SEL MB0	Select memory bank 0	1	1
SEL MB1	Select memory bank 1	1	1
ENT 0 CLK	Enable clock output on T0	1	1

Mnemonic	Description	Bytes	Cycles
NOP	No operation	1	1

A.C. CHARACTERISTICS (PORT 2 TIMING) TA = 0°C to 70°C, VCC = 5V ± 10%, VSS = 0V

Symbol	Parameter	8048H 8035HL				8048H-1 8035HL-1		Unit
		6 MHz		8 MHz		11 MHz		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CP}	Port control Setup Before Falling Edge of PROG.	110		105				ns
t_{PC}	Port Control Hold After Falling Edge of PROG.	100		90				ns
t_{PR}	PROG to Time P2 Input Must Be Valid		810		700		650	ns
t_{PF}	Input Data Hold Time	0	150	0	150	0	150	ns
t_{DP}	Output Data Setup Time	250		210		200		ns
t_{PD}	Output Data Hold Time	65		35		20		ns
t_{PP}	PROG Pulse Width	1200		970		700		ns
t_{PL}	Port 2 I/O Data Setup	350		300		250		ns
t_{LP}	Port 2 I/O Data Hold	150		65		20		ns

PORT 2 TIMING



BUS TIMING AS A FUNCTION OF TCY *

SYMBOL	FUNCTION OF TCY		
T_{LL}	7/30	T_{CY}	MIN
T_{AL}	1/10	T_{CY}	MIN
T_{LA}	1/15	T_{CY}	MIN
T_{CC} (1)	1/2	T_{CY}	MIN
T_{CC} (2)	2/5	T_{CY}	MIN
T_{DW}	2/15	T_{CY}	MIN
T_{WD}	1/15	T_{CY}	MIN
T_{DR}	0		MIN

T_{CC} (1) : $\overline{RD}/\overline{WR}$
T_{CC} (2) : $\overline{PSEN}$

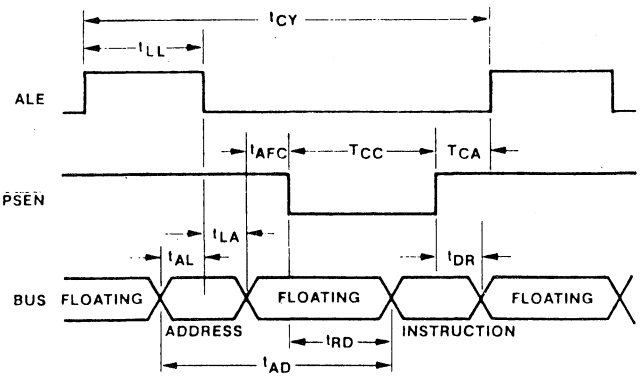
SYMBOL	FUNCTION OF TCY		
T_{RD} (1)	11/30	T_{CY}	MAX
T_{RD} (2)	3/10	T_{CY}	MAX
T_{AW}	3/10	T_{CY}	MIN
T_{AD} (1)	1/2	T_{CY}	MAX
T_{AD} (2)	1/3	T_{CY}	MAX
T_{AFC}	1/30	T_{CY}	MIN
T_{CA}	1/15	T_{CY}	MIN

T_{RD} (1) : $\overline{RD}$
T_{RD} (2) : $\overline{PSEN}$

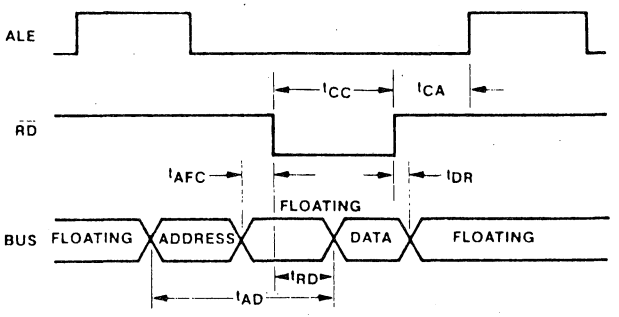
T_{AD} (1) : $\overline{RD}$
T_{AD} (2) : $\overline{PSEN}$

* APPROXIMATE VALUES NOT INCLUDING GATE DELAYS.

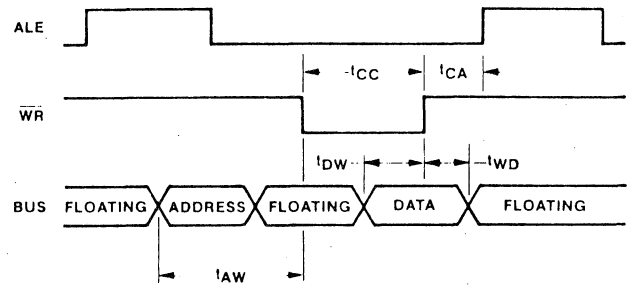
WAVEFORMS



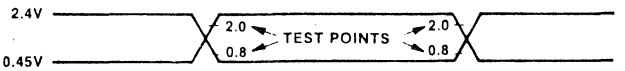
Instruction Fetch From External Program Memory



Read From External Data Memory



Write to External Data Memory



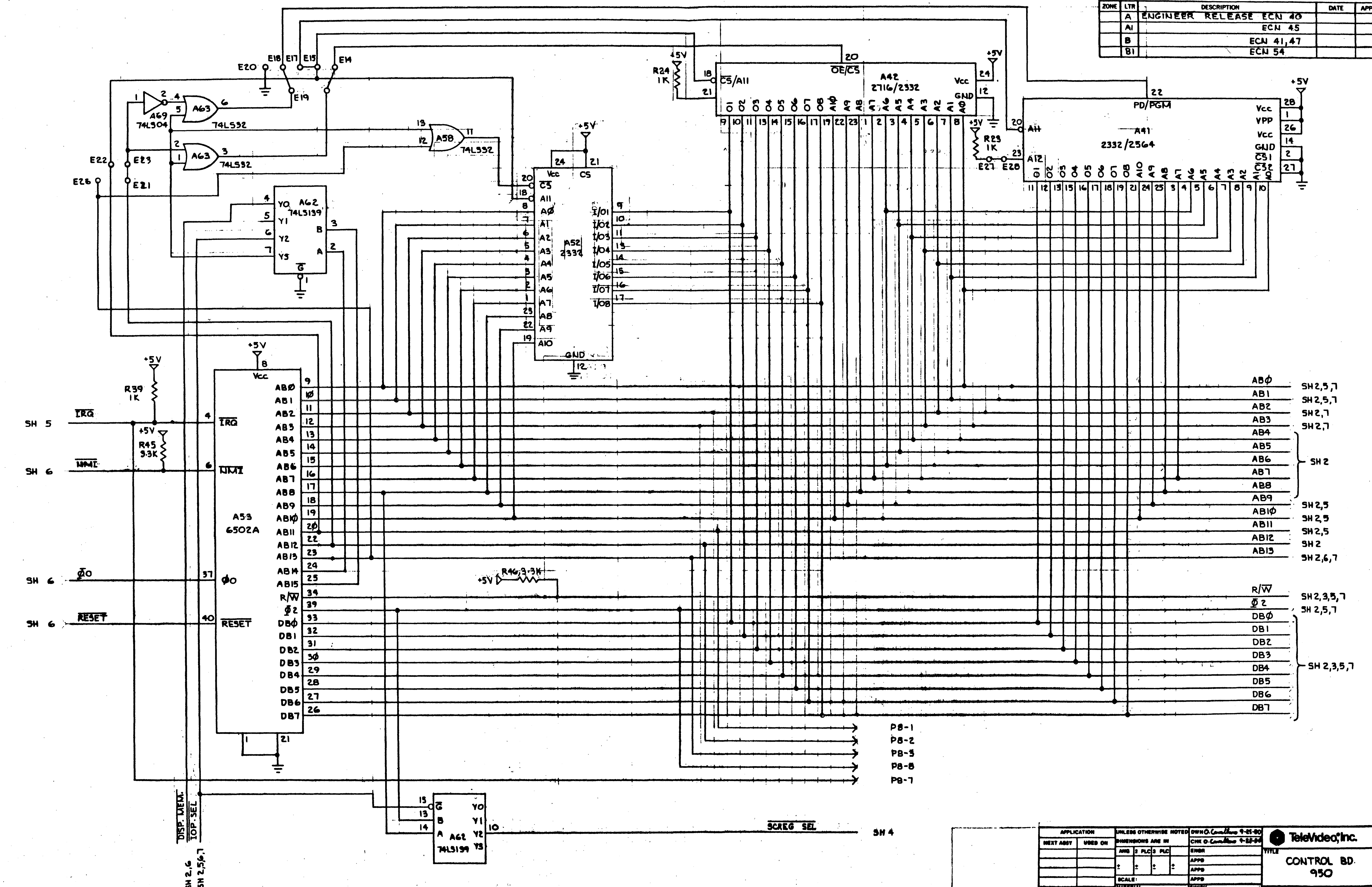
Input and Output for A.C.Tests

A.C. CHARACTERISTICS TA = 0°C to 70°C VCC = VDD = 5V ± 10%, VSS = 0V

Symbol	Parameter	8048H 8035HL				8048H-1 8035HL-1		Unit	Conditions (Note 1)
		6 MHz		8 MHz		11 MHz			
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{LL}	ALE Pulse Width	400		270		150		ns	
t_{AL}	Address Setup to ALE	75		75		70		ns	
t_{LA}	Address Hold from ALE	65		65		50		ns	
t_{CC}	Control Pulse Width ($\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$)	700		490		300		ns	
t_{DW}	Data Setup before $\overline{WR}$	370		370		280		ns	
t_{WD}	Data Hold after $\overline{WR}$	80		80		40		ns	CL = 20pF (NOTE 2)
t_{CY}	Cycle Time	2.5		1.875		1.36		μs	
t_{DR}	Data Hold	0	200	0	150	0	100	ns	
t_{RD}	$\overline{PSEN}$, $\overline{RD}$ to Data In		500		340		200	ns	
t_{AW}	Address Setup to $\overline{WR}$	230		210		200		ns	
t_{AD}	Address Setup to Data In		950		650		400	ns	
t_{AFC}	Address Float to $\overline{RD}$, $\overline{PSEN}$	0		0		-1		ns	
t_{CA}	Control Pulse to ALE	10		10		0		ns	

NOTE 1: Control outputs CL = 80 pF
BUS outputs CL = 150 pF

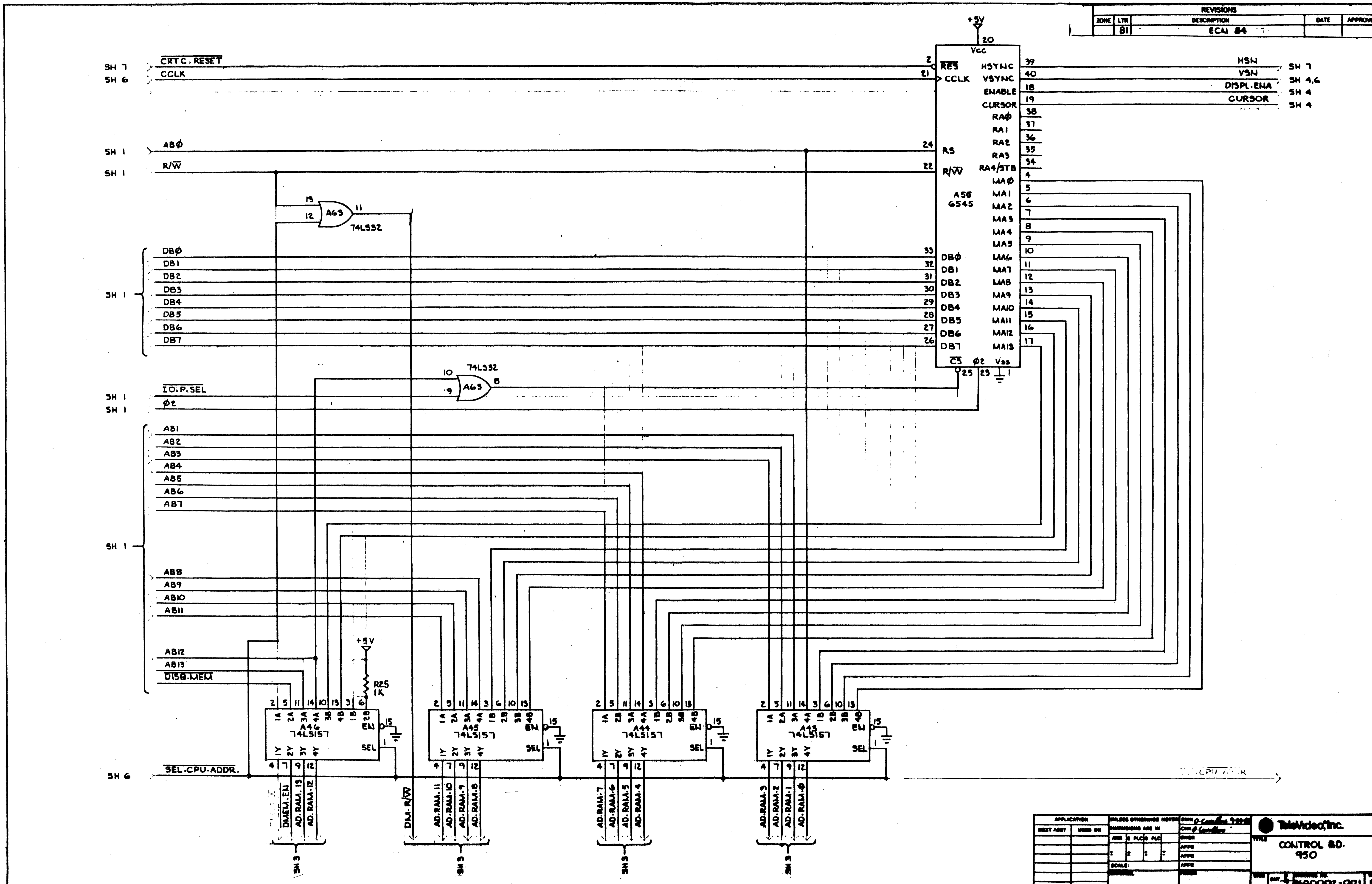
NOTE 2: BUS High Impedance Load: 20 pF



REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	ENGINEER RELEASE ECN 40		
	A1	ECN 45		
	B	ECN 41,47		
	B1	ECN 54		

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	DWN O. Camillone 9-25-80	TeleVideo, Inc.
NEXT ASSY	USED ON	ANG ± 2 PLC ± 3 PLC ±	CHK O. Camillone 9-25-80	TITLE: CONTROL BD. 950
		SCALE:	ENGR	
		MATERIAL	APPD	
			FINISH	SIZE · SHT 1 OF 7 · DRAWING NO. B600002-001 · REV B


REVISIONS
ZONE
LTR
DESCRIPTION
DATE
APPROVED
B1
ECN 84
+5V
Vcc
A56
6545
RES
CCLK
RS
R/W
DBØ
DB1
DB2
DB3
DB4
DB5
DB6
DB7
CS
Ø2
Vss
HSYNC
VSYNC
ENABLE
CURSOR
RAØ
RA1
RA2
RA3
RA4/STB
MAØ
MA1
MA2
MA3
MA4
MA5
MA6
MA7
MA8
MA9
MA10
MA11
MA12
MA13
HSN
VSN
DISPL.ENA
CURSOR
SH 7
SH 4,6
SH 4
SH 4
SH 7
SH 6
CRTC.RESET
CCLK
SH 1
ABØ
SH 1
R/W
A63
74LS32
SH 1
DBØ
DB1
DB2
DB3
DB4
DB5
DB6
DB7
74LS32
A63
SH 1
IO.P.SEL
SH 1
Ø2
SH 1
AB1
AB2
AB3
AB4
AB5
AB6
AB7
AB8
AB9
AB10
AB11
AB12
AB13
DISB.MEM
+5V
R25
1K
A46
74LS157
A45
74LS157
A44
74LS157
A43
74LS157
1A
2A
3A
4A
1B
2B
3B
4B
1Y
2Y
3Y
4Y
EN
SEL
SH 6
SEL.CPU.ADDR.
DMEM.EN
AD.RAM.13
AD.RAM.12
DMA.R/W
AD.RAM.11
AD.RAM.10
AD.RAM.9
AD.RAM.8
AD.RAM.7
AD.RAM.6
AD.RAM.5
AD.RAM.4
AD.RAM.3
AD.RAM.2
AD.RAM.1
AD.RAM.Ø
SH 3
SH 3
SH 3
SH 3
APPLICATION
NEXT ASSY
USED ON
TeleVideo, Inc.
CONTROL BD.
950
B600002-001
B

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B1	ECN 84		

SH 2 AQRAM 13
SH 2 AD.RAM.11
SH 2 AD.RAM.12
SH 6 QC.CLK
A15 74LS42
A8 74LS04
A16 74LS32
74LS32
A16 74LS32

SH 2 AD.RAM.10
AD.RAM.9
AD.RAM.8
AD.RAM.7
AD.RAM.6
AD.RAM.5
AD.RAM.4
AD.RAM.3
AD.RAM.2
AD.RAM.1
AD.RAM.Ø

A25 2114
A26 2114
A27 2114
A28 2114
A34 6116
A35 6116
A36 6116
A37 6116

SH 2 DM.R/W

SH 1 DB.7
DB.6
DB.5
DB.4
DB.3
DB.2
DB.1
DB.Ø

A14 8T245

CH.AD.7
CH.AD.6
CH.AD.5
CH.AD.4
CH.AD.3
CH.AD.2
CH.AD.1
CH.AD.Ø

SH 4

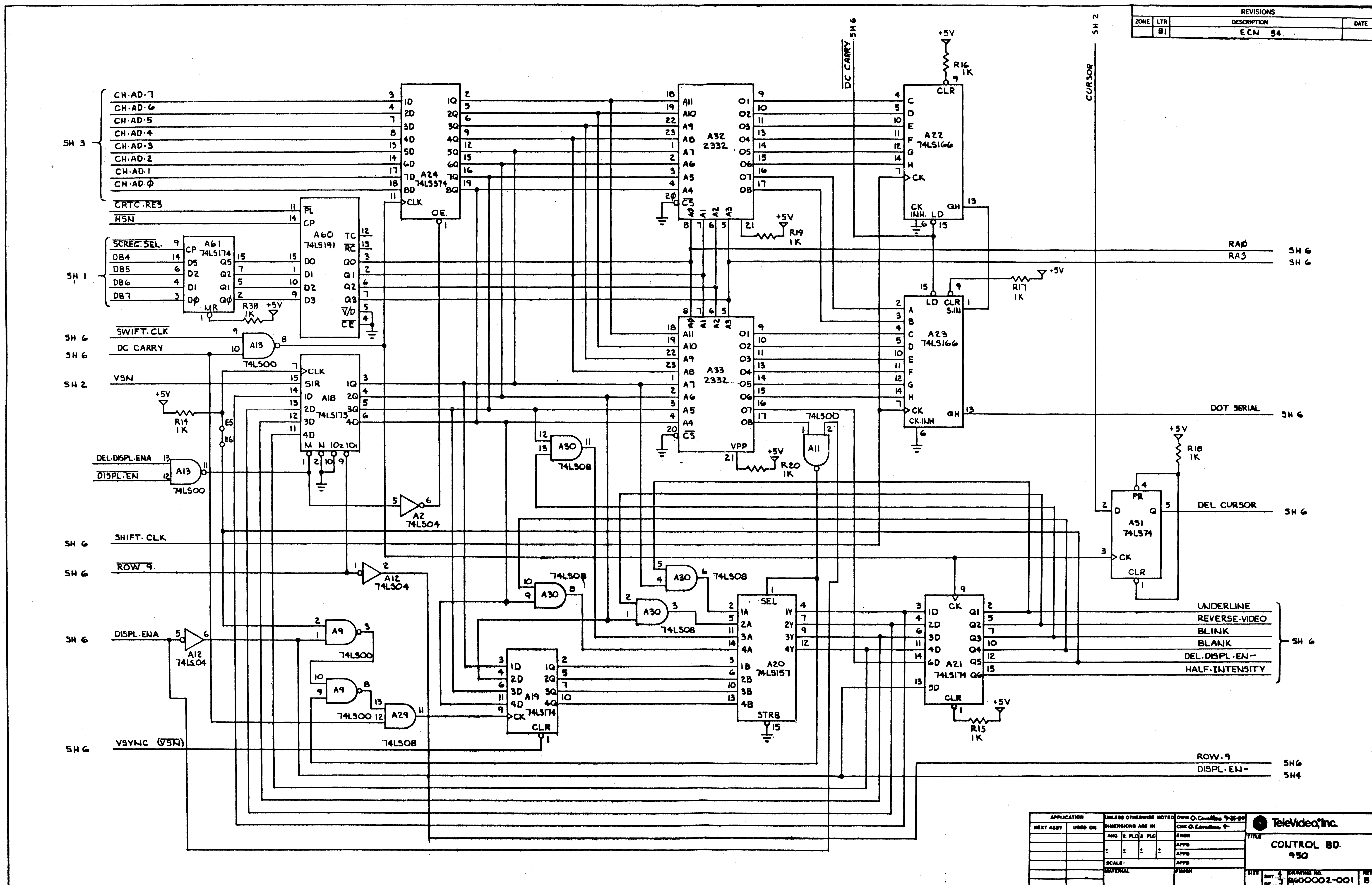
SH 2 DMEN.EN
SH 1 R/W

APPLICATION	
NEXT ASSY	USED ON

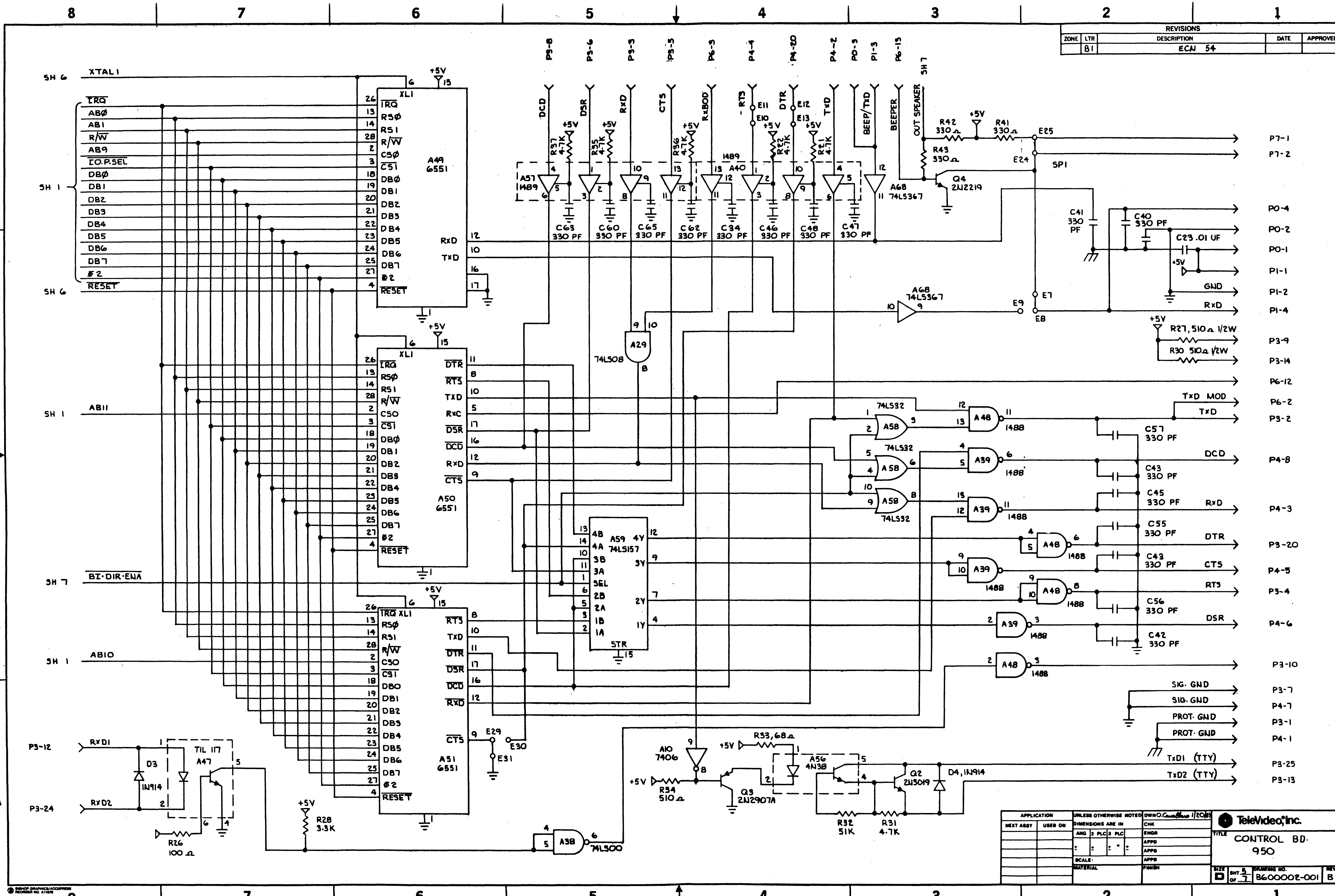
UNLESS OTHERWISE NOTED DIMENSIONS ARE IN
ANG ± 2 PLC ± 3 PLC ±
SCALE:
MATERIAL

DWN G.Connelley 9-15-89
CHK G.Connelley 9-22-89
ENGR
APPD
APPD
APPD
FINISH

TeleVideo, Inc.
TITLE: CONTROL BD 950
SIZE B | SHT 2 OF 4 | DRAWING NO. 8600002-001 | REV B

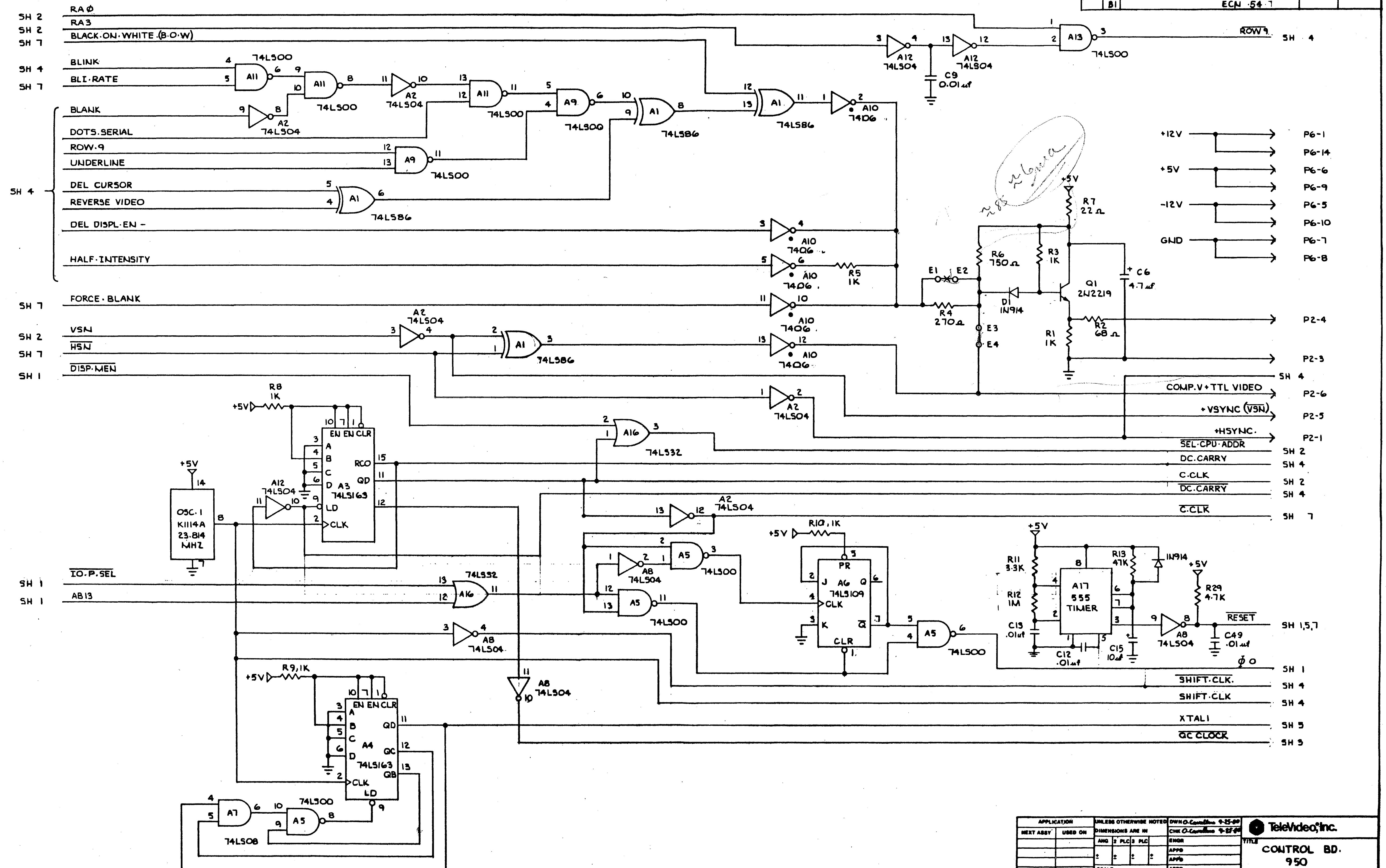


REVISIONS
ZONE LTR DESCRIPTION DATE
B1 ECN 54.
SH 3
CH·AD·7
CH·AD·6
CH·AD·5
CH·AD·4
CH·AD·3
CH·AD·2
CH·AD·1
CH·AD·Ø
CRTC·RES
HSN
SH 1
SCREG·SEL.
DB4
DB5
DB6
DB7
A61 74LS174
A60 74LS191
A24 74LS374
A32 2332
A33 2332
A22 74LS166
A23 74LS166
A18 74LS173
A13 74LS00
A30 74LS08
A11 74LS00
A2 74LS04
A12 74LS04
A9 74LS00
A29 74LS08
A19 74LS174
A20 74LS157
A21 74LS174
A31 74LS74
R14 1K
R15 1K
R16 1K
R17 1K
R18 1K
R19 1K
R20 1K
R38 1K
+5V
DC CARRY SH 6
CURSOR SH 2
SH 6 SWIFT·CLK
SH 6 DC CARRY
SH 2 VSN
DEL·DISPL·ENA
DISPL·EN
SH 6 SHIFT·CLK
SH 6 ROW 9
SH 6 DISPL·ENA
SH 6 VSYNC (VSN)
RAØ SH 6
RA3 SH 6
DOT SERIAL SH 6
DEL CURSOR SH 6
UNDERLINE
REVERSE·VIDEO
BLINK
BLANK
DEL·DISPL·EN-
HALF·INTENSITY
SH 6
ROW·9 SH6
DISPL·EN- SH4
APPLICATION
NEXT ASSY USED ON
UNLESS OTHERWISE NOTED DIMENSIONS ARE IN
DWN O. Cavallino 9-26-80
CHK O. Cavallino
TeleVideo, Inc.
TITLE
CONTROL BD. 950
SIZE SHT 4 OF 5 DRAWING NO. B600002-001 REV B

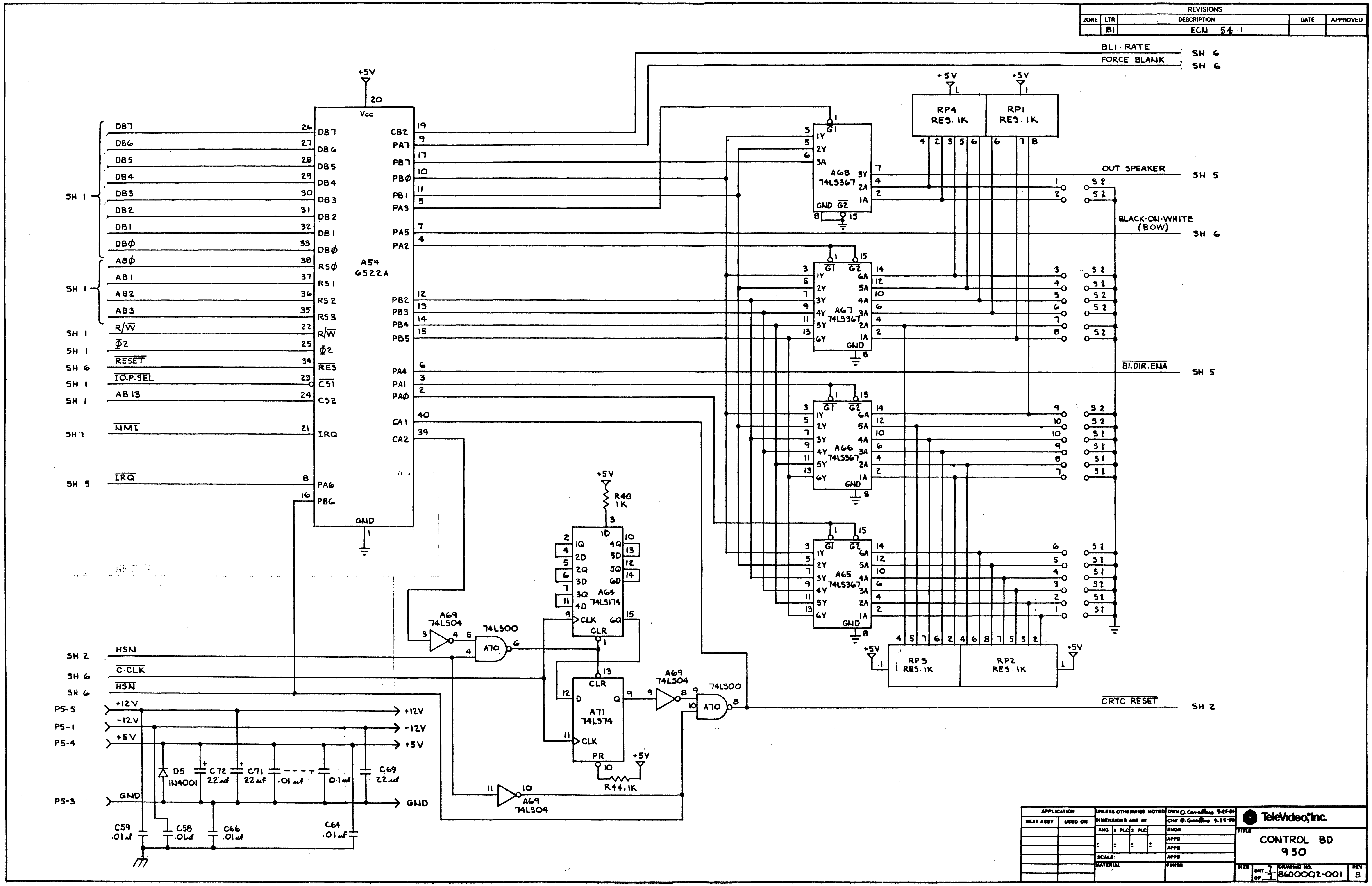


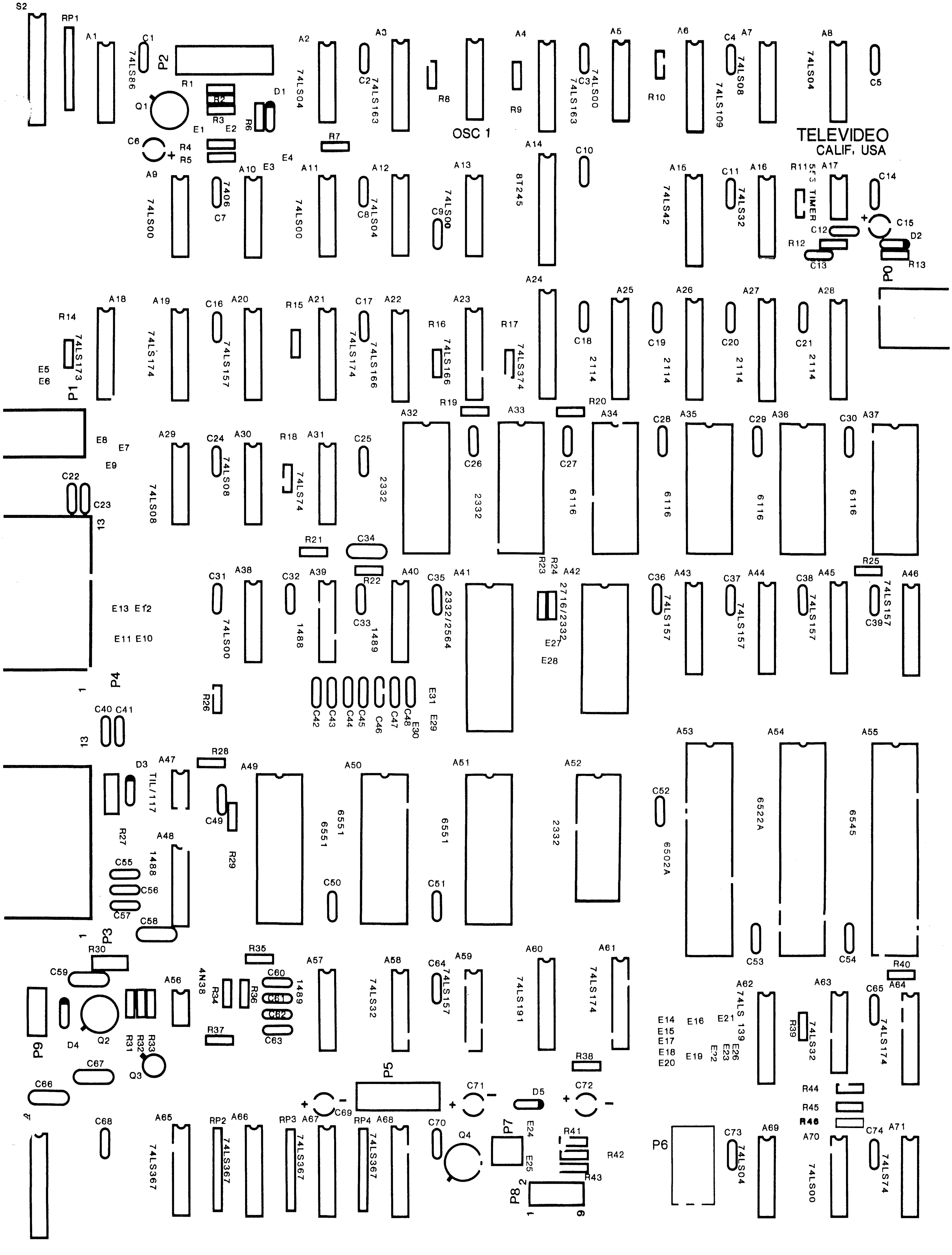
REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
B1 | B | ECN 54
A49 6551
A50 6551
A51 6551
A59 74LS157
A29 74LS08
A57 1489
A40 1489
A68 74LS367
A58 74LS32
A48 1488
A39 1488
A38 74LS00
A10 7406
A47 TIL 117
A56 4N38
Q2 2N3019
Q3 2N2907A
Q4 2N2219
D3 1N914
D4, 1N914
XTAL1
IRQ
AB0
AB1
R/W
AB9
I.O.P.SEL
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
Ø2
RESET
AB11
AB10
BI-DIR-ENA
SH 1
SH 6
SH 7
DCD
DSR
RxD
CTS
RxBOD
RTS
DTR
TxD
BEEP/TxD
BEEPER
OUT SPEAKER
TxD MOD
SIG. GND
PROT. GND
TxD1 (TTY)
TxD2 (TTY)
RxD1
RxD2
P7-1
P7-2
P0-4
P0-2
P0-1
P1-1
P1-2
P1-4
P3-9
P3-14
P6-12
P6-2
P3-2
P4-8
P4-3
P3-20
P4-5
P3-4
P4-6
P3-10
P3-7
P4-7
P3-1
P4-1
P3-25
P3-13
P3-12
P3-24
R27, 510Ω 1/2W
R30 510Ω 1/2W
R41 330Ω
R42 330Ω
R43 330Ω
R53, 68Ω
R34 510Ω
R32 51K
R31 4.7K
R28 3.3K
R26 100Ω
C41 330 PF
C40 330 PF
C23 .01 UF
TeleVideo, Inc.
TITLE CONTROL BD. 950
SIZE D
SHT 5 OF 7
DRAWING NO. B600002-001
REV B

ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B1	ECN 54 7		



APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	DWN O. Carrillo 9-25-80	TeleVideo, Inc.
NEXT ASSY	USED ON	ANG / 2 PLC / 3 PLC	CHK O. Carrillo 9-25-80	TITLE CONTROL BD. 950
		SCALE:	ENGR / APPD / APPD / APPD	
		MATERIAL	FINISH	SIZE / SHT 4 OF / DRAWING NO. B600002-001 / REV B


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
B1 ECN 5411
BLI-RATE SH 6
FORCE BLANK SH 6
+5V
RP4 RES. 1K
RP1 RES. 1K
OUT SPEAKER SH 5
BLACK-ON-WHITE (BOW) SH 6
BI.DIR.ENA SH 5
CRTC RESET SH 2
A54 6522A
Vcc
GND
DB7 DB6 DB5 DB4 DB3 DB2 DB1 DBϕ
ABϕ AB1 AB2 AB3
RSϕ RS1 RS2 RS3
R/W̄
Φ2
RESET
I.O.P.SEL
AB13
NMI
IRQ
SH 1
SH 5
SH 6
CB2 PA7 PB7 PBϕ PB1 PA3 PA5 PA2 PB2 PB3 PB4 PB5 PA4 PA1 PAϕ CA1 CA2 PA6 PB6
A68 74LS367
A67 74LS367
A66 74LS367
A65 74LS367
RP3 RES. 1K
RP2 RES. 1K
S2 S1
R40 1K
A64 74LS174
A69 74LS04
A70 74LS00
A71 74LS74
CLK CLR PR D Q
R44, 1K
SH 2 HSN
SH 6 C.CLK
SH 6 HSN
P5-5 +12V
P5-1 -12V
P5-4 +5V
P5-3 GND
D5 1N4001
C72 22uf
C71 22uf
.01uf
0.1uf
C69 22uf
C59 .01uf
C58 .01uf
C66 .01uf
C64 .01uf
APPLICATION
NEXT ASSY USED ON
UNLESS OTHERWISE NOTED DIMENSIONS ARE IN
TeleVideo, Inc.
TITLE CONTROL BD 950
SIZE B
DRAWING NO. B600002-001
REV B


S2
RP1
A1
C1
74LS86
P2
R1
R2
R3
Q1
D1
R6
E1
E2
C6
R4
R5
A2
74LS04
A3
C2
74LS163
R7
R8
OSC 1
A4
R9
A5
C3
74LS00
74LS163
R10
A6
74LS109
C4
A7
74LS08
A8
74LS04
C5
TELEVIDEO
CALIF. USA
A9
74LS00
7406
C7
A10
E3
E4
A11
74LS00
A12
C8
74LS04
A13
C9
74LS00
A14
8T245
C10
A15
74LS42
C11
74LS32
A16
R11
555 TIMER
A17
C14
C15
C12
R12
C13
D2
R13
P0
A18
R14
74LS173
E5
E6
P1
A19
74LS174
C16
74LS157
A20
R15
A21
74LS174
C17
74LS166
A22
R16
74LS166
A23
R17
74LS374
A24
C18
2114
A25
C19
2114
A26
C20
2114
A27
C21
2114
A28
R19
R20
A29
74LS08
C24
74LS08
A30
R18
A31
74LS74
C25
2332
A32
C26
2332
A33
C27
6116
A34
C28
6116
A35
C29
6116
A36
C30
6116
A37
E8
E7
E9
C22
C23
13
R21
C34
R22
R23
R24
R25
A38
C31
74LS00
C32
1488
A39
C33
1489
A40
C35
2332/2564
A41
A42
2716/2332
E27
E28
C36
74LS157
A43
C37
74LS157
A44
C38
74LS157
A45
74LS157
C39
A46
E13 E12
E11 E10
P4
1
R26
C42
C43
C44
C45
C46
C47
C48
E30
E31
E29
C40 C41
13
D3
A47
TIL/117
R28
A49
6551
A50
6551
A51
6551
A52
2332
A53
C52
6502A
6522A
A54
A55
6545
C49
R27
A48
1488
R29
C55
C56
C57
C58
C50
C51
C53
C54
1
P3
R30
R35
C59
A56
4N38
R34
R36
C60
C61
C62
C63
1489
A57
74LS32
A58
C64
74LS157
A59
A60
74LS191
A61
74LS174
R40
A64
A62
74LS 139
E14
E15
E17
E18
E20
E16
E19
E21
E22
E23
E26
R39
A63
74LS32
C65
74LS174
P9
D4
Q2
R31
R32
R33
R37
Q3
C67
C66
R38
P5
C71
D5
C72
C69
R44
R45
R46
C68
A65
74LS367
RP2
74LS367
A66
RP3
74LS367
A67
RP4
74LS367
A68
C70
Q4
P7
E24
E25
R41
R42
R43
P6
C73
74LS04
A69
A70
74LS00
C74
A71
74LS74
P8
2
1
6

SILKSCREEN

ITEM/ FIND NO.	QTY PER ASSY 02	QTY PER ASSY 01	UNIT OF MEAS	KEY(1)	KEY(2)	PART NUMBER/ REFERENCE DOCUMENT	TITLE/DESCRIPTION	REMARKS
1		1				I800C00-009	IC PROGRAMED ROM 8048	U6
2	1					I740010-036	IC MICROPROCESSOR P8035	U6
3	1	1				I740010-057	IC 7414	U8
4	1					I800000-018	IC PROGRAMED EPROM (2716)	U5
5	1					I740010-024	IC 74LS373	U4
6	2					I740010-023	IC 74LS367	U2,3
7	1					I740010-005	IC 74LS05	U7
8	1	1				R600000-001	VOLTAGE REGULATOR	V1
9	2	2				R514000-103	RES SIP (PACK) 10K Ω	RP2,3
10	1	1				R514000-006	RES C/F 1KΩ 5% 1/4W	R2
11	2	2				R514000-023	RES C/F 10KΩ 5% 1/4W	R1,R3
12								
13								
14	2	2				C600100-002	CAP DIP MICA 20pf 50V	C6,8
15	1	1				C900100-003	CAP C/D 330pf 20% 50V	C10
16	2	2				C800100-001	CAP R/L 1uf 50V	C7 C12
17								
18	7	3				C900100-002	CAP C/D 0.01uf 10% 50V	C2-5,9,11,13
19								

NOTES: 01 8048. MICROPROCESSOR
02 8035. "

REV 2 ADDS ITEM 7, 12 & 13
CORRECTION FOR ITEM 11
REV 3 ADDS ITEM 9

APPLICATION	
NEXT ASSY	USED ON

UNIT OF MEASURE:
01-EACH 04-BULK
02-INCH 05-AS REQ'D
03-FEET 09-OTHER (see notes)

KEY 1:
A-WITH B/M
D-WITHOUT B/M
R-REFERENCE
S-SPECIFICATION
O-OTHER (see notes)

DWN O. Carrillo 9-23-80
CHK O. Carrillo 9-23-80
ENGR [illegible] 9-23-80
APPD [illegible] 9/23/80
APPD [illegible] 9/23/80
APPD
KEY 2:

ENGR CHANGES			
REV	CHG NO.	DATE	APPD
D	ECN 51	1-15-81	
D1	ECN 56	2-3-81	
D2	ECN 60	4-28	

TeleVideo, Inc.

TITLE PART LIST
950 TVI KEY BOARD

SIZE	SHT	OF	BILL OF MAT'L NO.	REV
A	1	3	B900003-001	D

ITEM/ FIND NO.	QTY PER ASSY			02	01	UNIT OF MEAS	KEY(1)	KEY(2)	PART NUMBER/ REFERENCE DOCUMENT	TITLE/DESCRIPTION	REMARKS
20											
21											
22				1	1				B800003-001	P.C. BOARD	
23											
24											
25				1	1				5360100-001	DIODE IN 4001	CR1
26											
27											
28				1	1				M200401-002	CRYSTAL 5.7143 MHZ	X1
29											
30											
31				1	1				M200202-001	RJ11 FEMALE CONTROL BOARD CONNECTOR	P7
32											
33											
34				1	1				M200601-006	2PIN PLUG.	P6
35											
36											
37				1					M200301-002	IC SOCKET 24PINS	U5
38				1	1				M200301-003	IC SOCKET 40PINS	U6

NOTES:

APPLICATION	
NEXT ASSY	USED ON

UNIT OF MEASURE:
01-EACH 04-BULK
02-INCH 05-AS REQ'D
03-FEET 09-OTHER (see notes)

KEY 1:
A-WITH B/M
D-WITHOUT B/M
R-REFERENCE
S-SPECIFICATION
O-OTHER (see notes)

DWN O. Cavallero 9-23-80
CHK O. Cavallero 9-23-80
ENGR [signature] 9-23-80
APPD [signature] 9/23/80
APPD [signature] 9/23/80
APPD
KEY 2:

ENGR CHANGES			
REV	CHG NO.	DATE	APPD

TeleVideo, Inc.

TITLE PART LIST
950 TVI KEYBOARD

SIZE	SHT	BILL OF MAT'L NO.	REV
A	2 OF 3	B900003-001	D

ITEM/ FIND NO.	QTY PER ASSY					UNIT OF MEAS	KEY(1)	KEY(2)	PART NUMBER/ REFERENCE DOCUMENT	TITLE/DESCRIPTION	REMARKS
				02	01						
				102	102				KS-123456	STANDARD SWITCH.	
				1	1				KS-123457	ALPHA LOCK SWITCH.	
				2	2				K030500-003	DAMPER.	
				2	2				K030500-002	GUIDE STEM.	
				2	2				K030500-001	KEY GUIDE.	
				1	1				K030500-004	KEY GUIDE ARM.	
				1	1				CRT-010327	KEY B/D CHASSIS.	

NOTES:

APPLICATION	
NEXT ASSY	USED ON

UNIT OF MEASURE:
01-EACH 04-BULK
02-INCH 05-AS REQ'D
03-FEET 09-OTHER (see notes)

KEY 1:
A-WITH B/M
D-WITHOUT B/M
R-REFERENCE
S-SPECIFICATION
O-OTHER (see notes)

DWN O. Caballero 9-23-80
CHK O. Caballero 9-23-80
ENGR [illegible] 9-23-80
APPD [illegible] 9/23/80
APPD R E Hallett 9/23/80
APPD
KEY 2:

ENGR CHANGES			
REV	CHG NO.	DATE	APPD

TeleVideo®, Inc.

TITLE PART LIST
950 TUI KEY BOARD

SIZE	SHT	BILL OF MAT'L NO.	REV
A	3 OF 3	B900003-001	0

ITEM/ FIND NO.	QTY PER ASSY				UNIT OF MEAS	KEY(1)	KEY (2)	PART NUMBER/ REFERENCE DOCUMENT	TITLE/DESCRIPTION	REMARKS
			03	02	01					
1			52	52	52			C900100-001	CAP. .01 µF.	C1-5,7-14,16-33,35-39, 49-54,58,59,64-68,70,73,74
2			3	3	3			C700100-001	CAP. 22 uf	C69,71,72
3			17	17	17			C900100-003	CAP. 330Pf	C34,40-48,55-57,60-63
4			1	1	1			CT-16476	CAP. 4.7 uf	C6
5			1	1	1			CE-161065	CAP. 10 uf	C15
6			1	1	1			B800002-001	P.C. BOARD	
7										
8			1	1	1			I740010-063	IC 74LS191	A60
9										
10			1	1	1			I740010-015	IC 74LS109	A6
11			6	6	6			I740010-001	IC 74LS00	A5,9,11,13,38,70
12			4	4	4			I740010-004	IC 74LS04	A2,8,12,69
13			1	1	1			I740010-054	IC 7406	A10
14			3	3	3			I740010-006	IC 74LS08	A7,29,30
15			3	3	3			I740010-009	IC 74LS32	A16,58,63,
16			2	2	2			I740010-013	IC 74LS74	A31,71
17			1	1	1			I740010-014	IC 74LS86	A1
18			1	1	1			I740010-016	IC 74LS139	A62
19			6	6	6			I740010-017	IC 74LS157	A20,43-46,59

NOTES: -01 930/950 B. ONE PAGE OF DISPLAY MEMORY.
-02 " TWO " " "
-03 930/950 C FOUR " " "

APPLICATION	
NEXT ASSY	USED ON

UNIT OF MEASURE:
01-EACH 04-BULK
02-INCH 05-AS REQ'D
03-FEET 09-OTHER (see notes)

KEY 1:
A-WITH B/M
D-WITHOUT B/M
R-REFERENCE
S-SPECIFICATION
O-OTHER (see notes)

DWN S. Lee
CHK
ENGR DM
APPD
APPD
APPD
KEY 2:

ENGR CHANGES

REV	CHG NO.	DATE	APPD
A	ECN 40		
B	ECN 41 47	1-12-81	
B1	ECN 48	1-14-81	
B2	ECN 52	1-16-81	
B3	ECN 57	2-3-81	
B4	ECN 59	2-26-81	

TeleVideo, Inc.

TITLE PARTS LIST
CONTROL BOARD
TVI 950

SIZE	SHT	BILL OF MAT'L NO.	REV
A	1 OF 5	B900002-001	B4

ITEM/ FIND NO.	QTY PER ASSY					UNIT OF MEAS	KEY(1)	KEY (2)	PART NUMBER/ REFERENCE DOCUMENT	TITLE/DESCRIPTION	REMARKS	
			03	02	01							
20			2	2	2				I740010-018	IC 74LS 163	A3,4	
21			2	2	2				I740010-019	IC 74LS 166	A22,23	
22			1	1	1				I740010-020	IC 74LS 173	A18	
23			4	4	4				I740010-021	IC 74LS 174	A19,21,61,64	
24			4	4	4				I740010-023	IC 74LS 367	A65-67	
25			1	1	1				I740010-025	IC 74LS 374	A24	
26			2	2	2				I740010-026	IC 75188	A39,48	
27			2	2	2				I740010-027	IC 75189	A40,57	
28			1	1	1				I740010-029	IC TIL 117	A47	
29			1	1	1				I740010-055	IC 4N38	A56	
30			4	4	4				I740010-059	IC 2114 (150nSec)	A25-28,	
31			4	2	1				I740011-000	IC 6116 RAM 2KX8	A34-37	
32			1	1	1				I740011-002	IC 6502A MICROPROCESSOR	A53	
33			1	1	1				I740011-003	IC 6545 CRT CONT	A55	
34			3	3	3				I740011-004	IC 6551 UART	A49-51	
35			1	1	1				I740011-005	IC 6522A V.I.A.	A54	
36			1	1	1				I740010-061	IC N8T245N	A14	
37			1	1	1				I740010-056	IC K1114A OR EQUI CRYSTAL OS	23.814 MHZ	OSC.1
38			1	1	1				I800000-001	SYS ROM 2332 (F000)	A41	

NOTES:

APPLICATION	
NEXT ASSY	USED ON

UNIT OF MEASURE:
01-EACH 04-BULK
02-INCH 05-AS REQ'D
03-FEET 09-OTHER (see notes)

KEY 1:
A-WITH B/M
D-WITHOUT B/M
R-REFERENCE
S-SPECIFICATION
O-OTHER (see notes)

DWN
CHK
ENGR Dm
APPD
APPD
APPD
KEY 2:

ENGR CHANGES			
REV	CHG NO.	DATE	APPD

TeleVideo® Inc.

TITLE PARTS LIST
CONTROL BOARD
TVI 950

SIZE	SHT 2 OF 5	BILL OF MAT'L NO.	REV
A		B900002-001	B4

ITEM/ FIND NO.	QTY PER ASSY					UNIT OF MEAS	KEY(1)	KEY(2)	PART NUMBER/ REFERENCE DOCUMENT	TITLE/DESCRIPTION	REMARKS
			03	02	01						
39			1	1	1				I800000-002	IC CHAR GEN ROM 2332 (UPPER BYTE). A33	
40			1	1	1				I800000-003	IC CHAR GEN ROM 2332 (LOWER BYTE). A32	
41			1	1	1				I800000-007	SYS .ROM. 2332 (E000)	A42
42			1	1	1				I740010-010	IC 74LS42	A15
43			1	1	1				I740010-031	IC NE555	A17
44			2	2	2				R514000-015	RES. C/F 750 Ω 5% 1/4 W	R6,41
45			1	1	1				R514000-018	RES. 51 KΩ 5% 1/4 W	R32
46			2	2	2				R514000-001	RES 68Ω 5% 1/4W.	R2,33
47			7	7	7				R514000-011	RES 4.7K 5% 1/4 W	R21,22,29,31,35-37
48			1	1	1				R514000-002	RES 270Ω 5% 1/4W.	R4
49			2	2	2				R514000-003	RES 330Ω 5% 1/4W.	R42 43
50			1	1	1				R514000-005	RES 510Ω 5% 1/4W.	R34
51			20	20	20				R514000-006	RES 1KΩ 5% 1/4W.	R1,3,5,8-10,14-20,23-25,38 ~~40,44~~
52			5	5	5				R514000-009	RES 3.3KΩ 5% 1/4W.	R11,28,39,45,46
53			1	1	1				R514000-017	RES 100 KΩ 5% 1/4W.	R26
54			1	1	1				R514000-014	RES 1M 5% 1/4 W	R12
55			4	4	4				R514000-100	RES PACK 1KΩ	RP1-4
56			2	2	2				R514000-022	RES 510Ω 1/2 W.	R27,30
57			1	1	1				R514000-024	RES 22 Ω 5% 1/4 W	R7

NOTES:

APPLICATION	
NEXT ASSY	USED ON

UNIT OF MEASURE:
01-EACH 04-BULK
02-INCH 05-AS REQ'D
03-FEET 09-OTHER (see notes)

KEY 1:
A-WITH B/M
D-WITHOUT B/M
R-REFERENCE
S-SPECIFICATION
O-OTHER (see notes)

DWN
CHK
ENGR Dm
APPD
APPD
APPD
KEY 2:

ENGR CHANGES			
REV	CHG NO.	DATE	APPD

TeleVideo, Inc.

TITLE PARTS LIST
CONTROL BOARD
TVI 950

SIZE	SHT 3 OF 5	BILL OF MAT'L NO.	REV
A		B900002-001	B4

ITEM/ FIND NO.	QTY PER ASSY					UNIT OF MEAS	KEY(1)	KEY(2)	PART NUMBER/ REFERENCE DOCUMENT	TITLE/DESCRIPTION	REMARKS
			03	02	01						
77			1	1	1				RC-40473J	RES 47K 1/4W 5%	R13
78			7	7	7				M200301-002	IC SOCKET 24 PINS	A32-34 37,41,42,52
79											
80			3	3	3				M200301-005	IC SOCKET 28 PINS	A49-51
81			3	3	3				M200301-003	IC SOCKET 40 PINS	A53-55
82											
83			2	2	2				M200201-001	CONNECTOR RS232 R/A	P3,4
84			2	2	2				M200601-002	PLUG 5 PINS	P2,5
85			1	1	1				M200202-001	RJ11 FEMALE KEY BOARD CONNECTOR 520221-2	P1
86			1	1	1				M200601-001	PLUG 2 PINS	P9
87			3	3	3				M200100-002	TRANS PAD LARGE	Q1,2,4
88											
89											
90											
91											
92											
93											
94											
95											

NOTES:

APPLICATION	
NEXT ASSY	USED ON

UNIT OF MEASURE:
01-EACH 04-BULK
02-INCH 05-AS REQ'D
03-FEET 09-OTHER (see notes)

KEY 1:
A-WITH B/M
D-WITHOUT B/M
R-REFERENCE
S-SPECIFICATION
O-OTHER (see notes)

DWN
CHK
ENGR DM
APPD
APPD
APPD
KEY 2:

ENGR CHANGES			
REV	CHG NO.	DATE	APPD

TeleVideo, Inc.

TITLE PARTS LIST
CONTROL BOARD
TVI 950

SIZE	SHT	BILL OF MAT'L NO.	REV
A	4 OF 5	B900002-001	B4

ITEM/ FIND NO.	QTY PER ASSY					UNIT OF MEAS	KEY(1)	KEY (2)	PART NUMBER/ REFERENCE DOCUMENT	TITLE/DESCRIPTION	REMARKS
			03	02	01						
58											
59											
60											
61											
62											
63											
64											
65			2	2	2				S350100-000	2N 2219 TRANSISTOR	Q1,4
66			1	1	1				S350100-002	2N 3019 TRANSISTOR	Q2
67			1	1	1				5350100-003	2N 2907A TRANSISTOR	Q3
68											
69											
70			4	4	4				S360100-000	IN 914 DIODE	D1-4
71			1	1	1				S360100-001	IN 4001 DIODE	D5
72											
73			2	2	2				M200101-003	DIP SWITCH 10POS. SIDE	S1,2
74											
75											
76											

NOTES:

APPLICATION	
NEXT ASSY	USED ON

UNIT OF MEASURE:
01-EACH 04-BULK
02-INCH 05-AS REQ'D
03-FEET 09-OTHER (see notes)

KEY 1:
A-WITH B/M
D-WITHOUT B/M
R-REFERENCE
S-SPECIFICATION
O-OTHER (see notes)

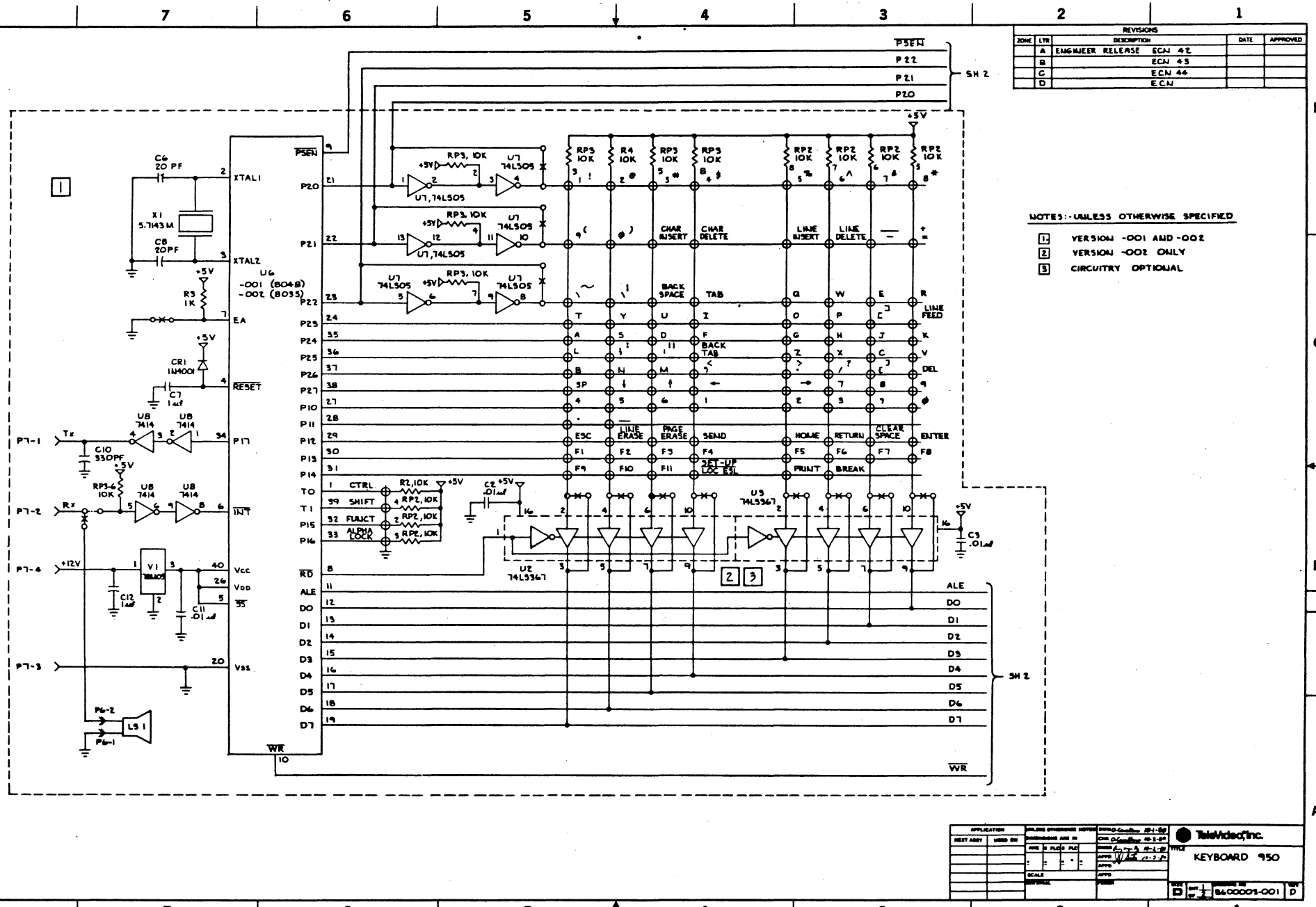
DWN
CHK
ENGR DM
APPD
APPD
APPD
KEY 2:

ENGR CHANGES			
REV	CHG NO.	DATE	APPD

TeleVideo, Inc.

TITLE PART LIST
CONTROL BOARD
TVI 950

SIZE	SHT 5 OF 5	BILL OF MAT'L NO.	REV
A		B900002-001	B4



NOTES:- UNLESS OTHERWISE SPECIFIED

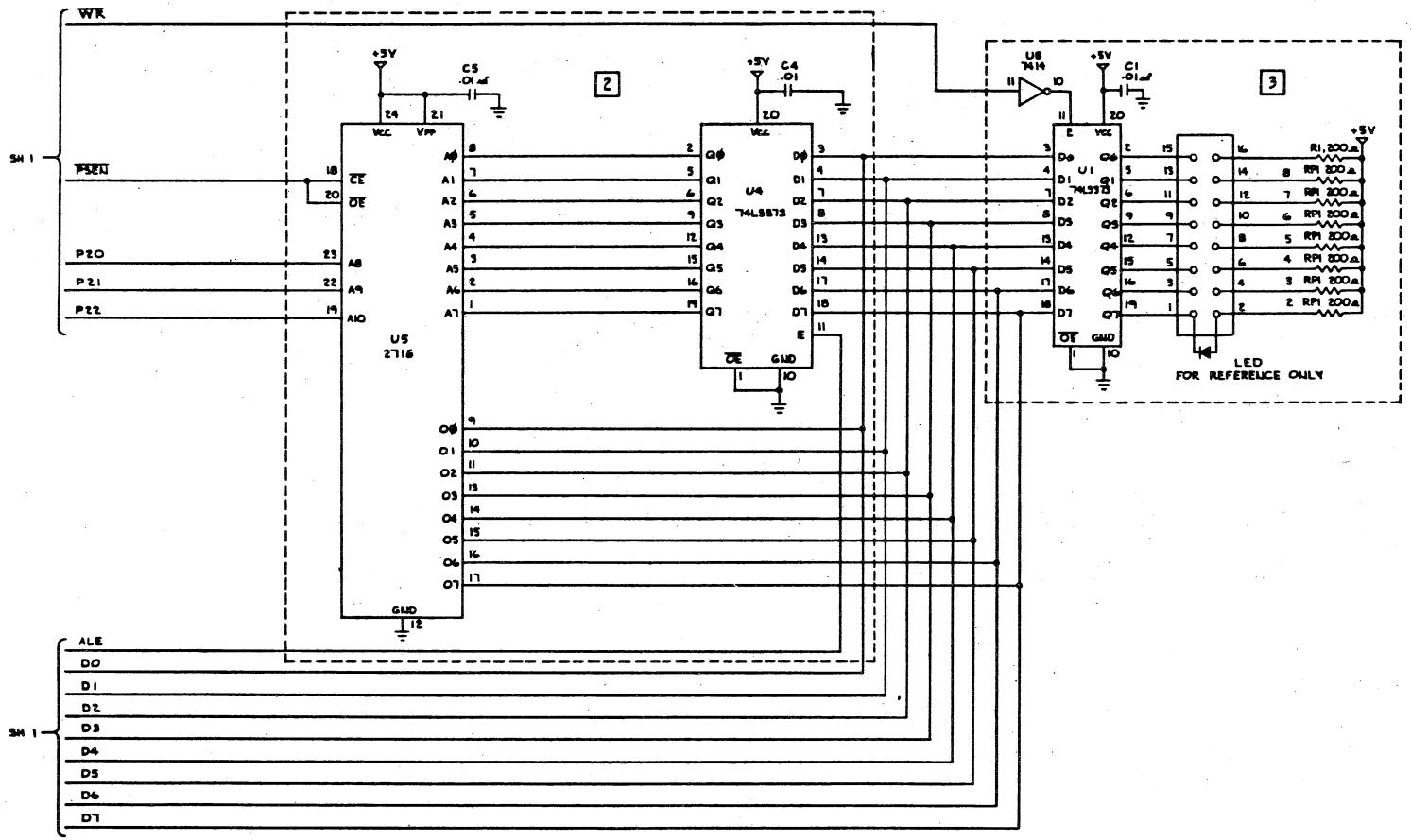
1. VERSION -001 AND -002
2. VERSION -002 ONLY
3. CIRCUITRY OPTIONAL

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	ENGINEER RELEASE ECN 42		
	B	ECN 43		
	C	ECN 44		
	D	ECN		

TeleVideo, Inc.

TITLE: KEYBOARD 950

SIZE D | SHT 1 OF 2 | DRAWING NO 8600009-001 | REV D



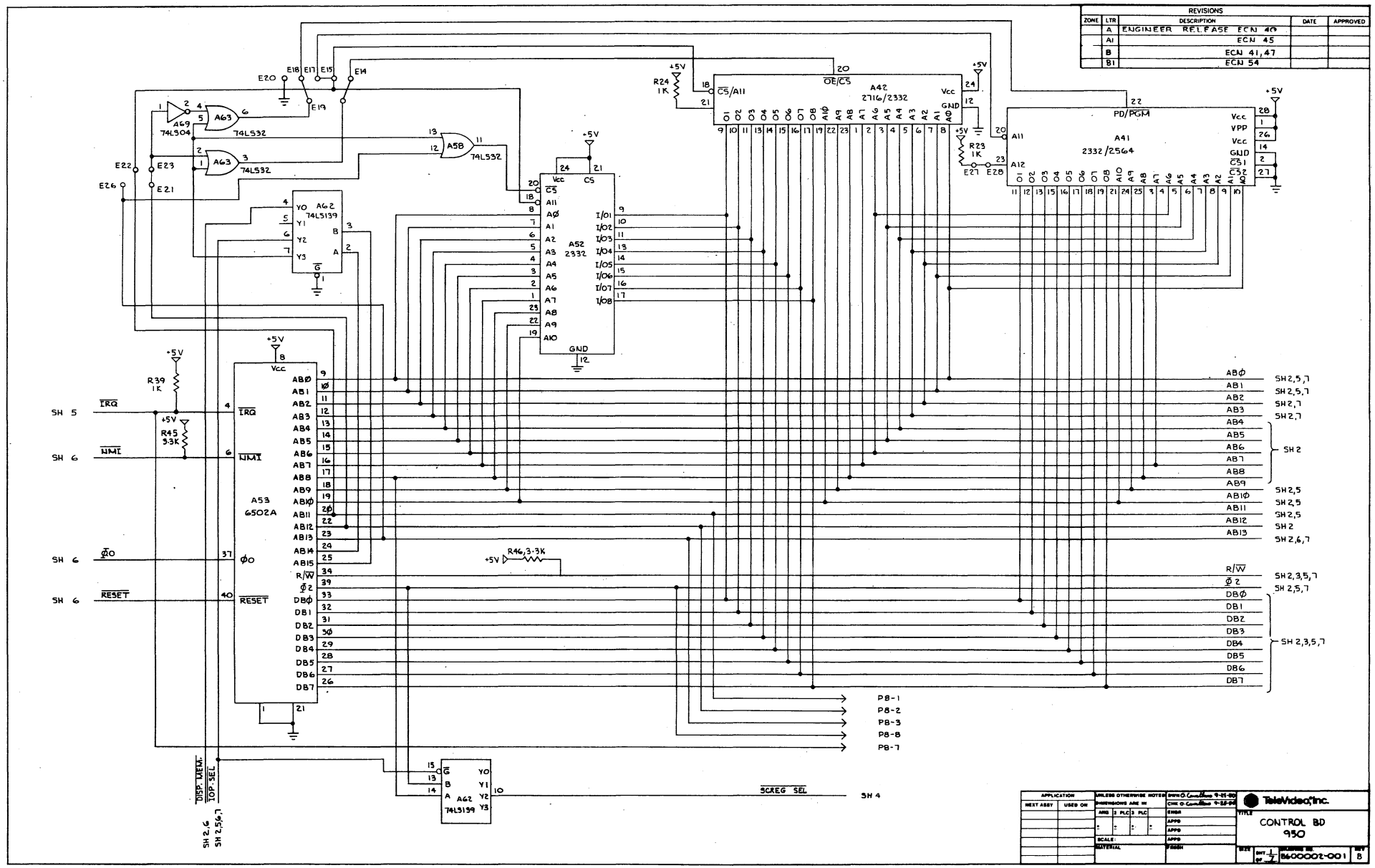
REVISIONS

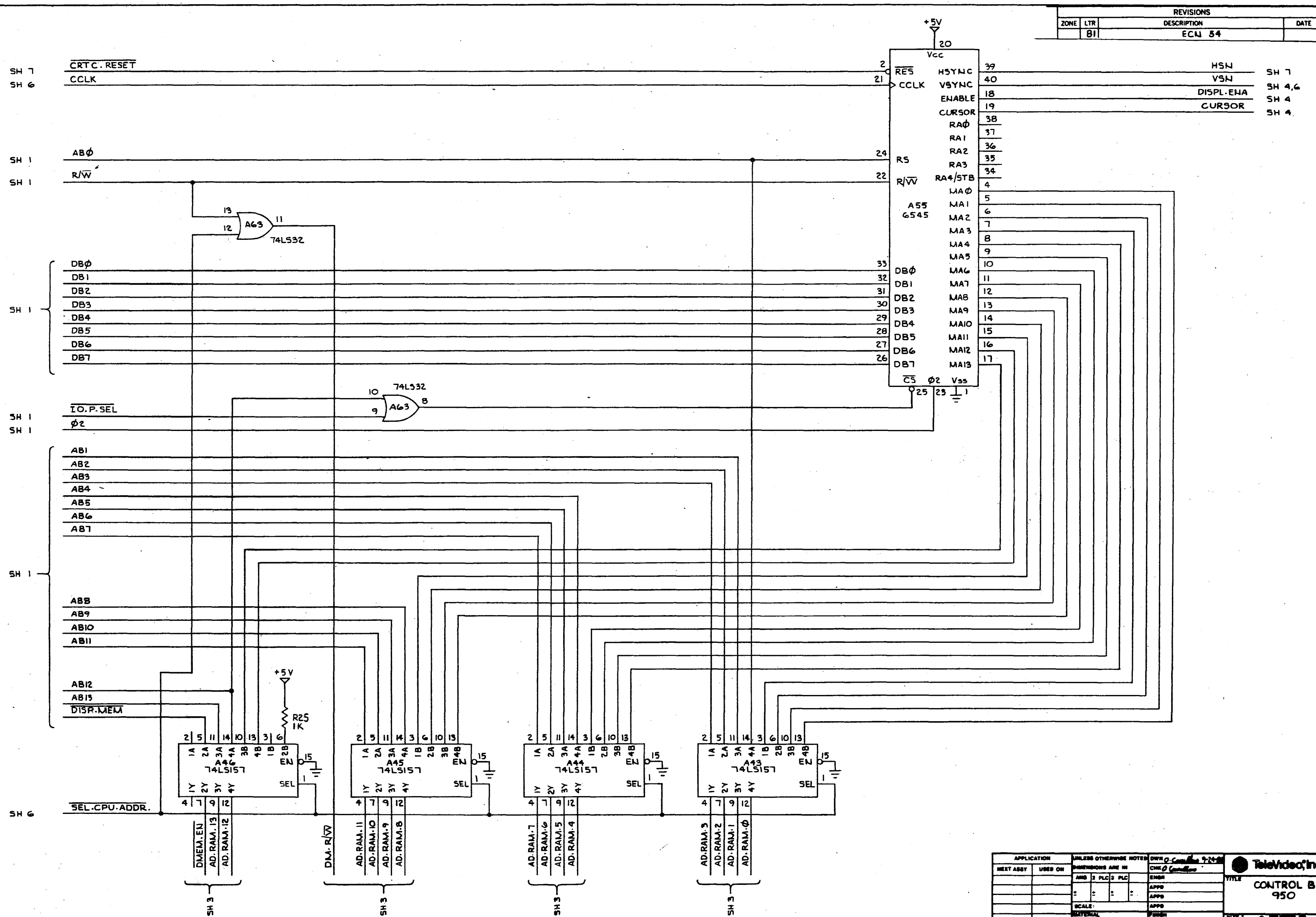
ZONE	LTR	DESCRIPTION	DATE	APPROVED

TeleVideo, Inc.

KEY BOARD 950

84000008-001


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
A ENGINEER RELEASE ECN 40
A1 ECN 45
B ECN 41,47
B1 ECN 54
A69 74LS04
A63 74LS32
A58 74LS32
A62 74LS139
A42 2716/2332
A41 2332/2564
A52 2332
A53 6502A
R24 1K
R23 1K
R39 1K
R45 3.3K
R46, 3.3K
+5V
E20 E18 E17 E15 E14 E19 E22 E23 E26 E21 E27 E28
SH 5 IRQ
SH 6 NMI
SH 6 ϕO
SH 6 RESET
R/W
ϕ2
DISP. MEM.
TOP. SEL.
SH 2,6
SH 2,5,6,7
SCREG SEL
SH 4
P8-1
P8-2
P8-3
P8-8
P8-7
SH 2,5,7
SH 2,7
SH 2
SH 2,6,7
SH 2,3,5,7
TeleVideo, Inc.
CONTROL BD
950
B600001-001
REV B

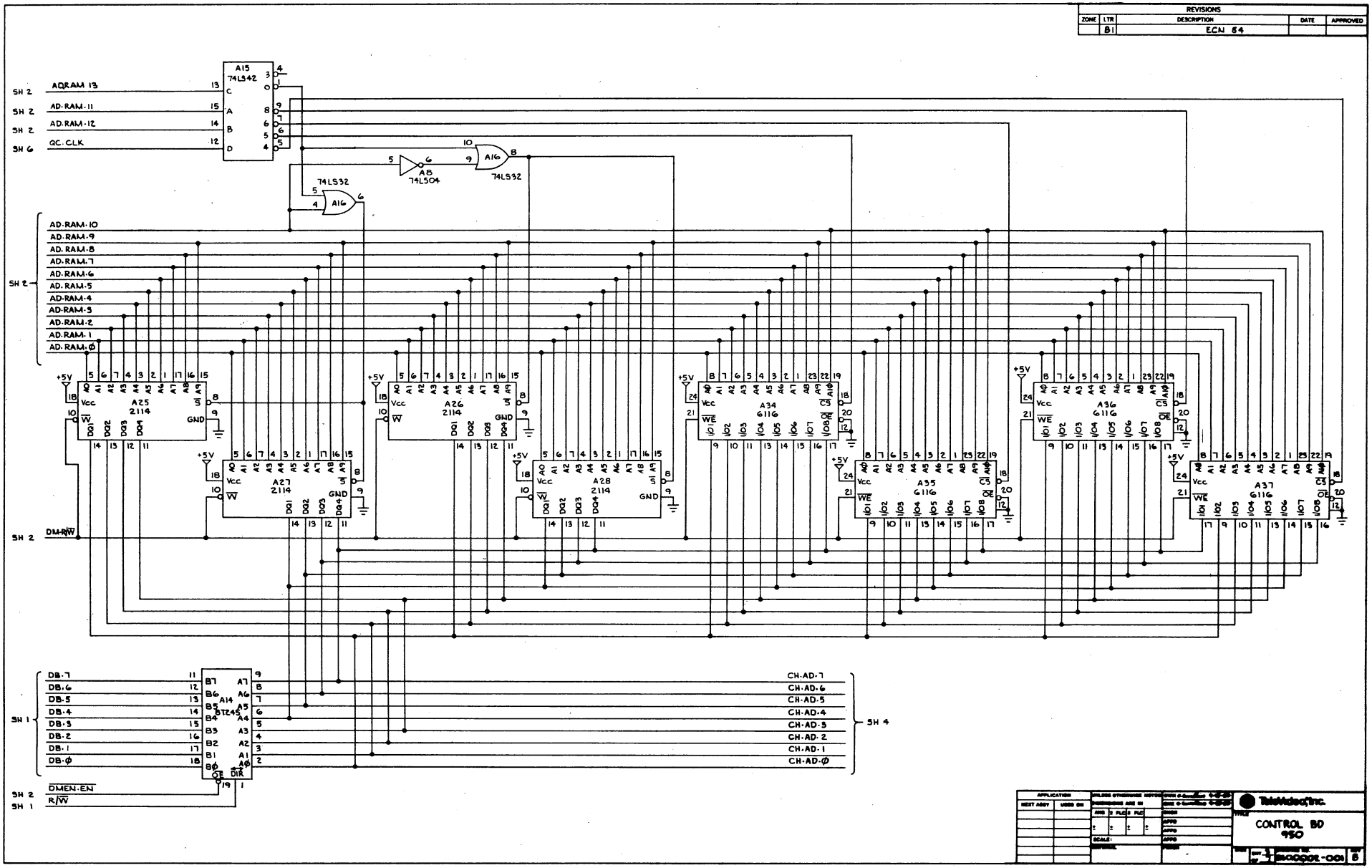


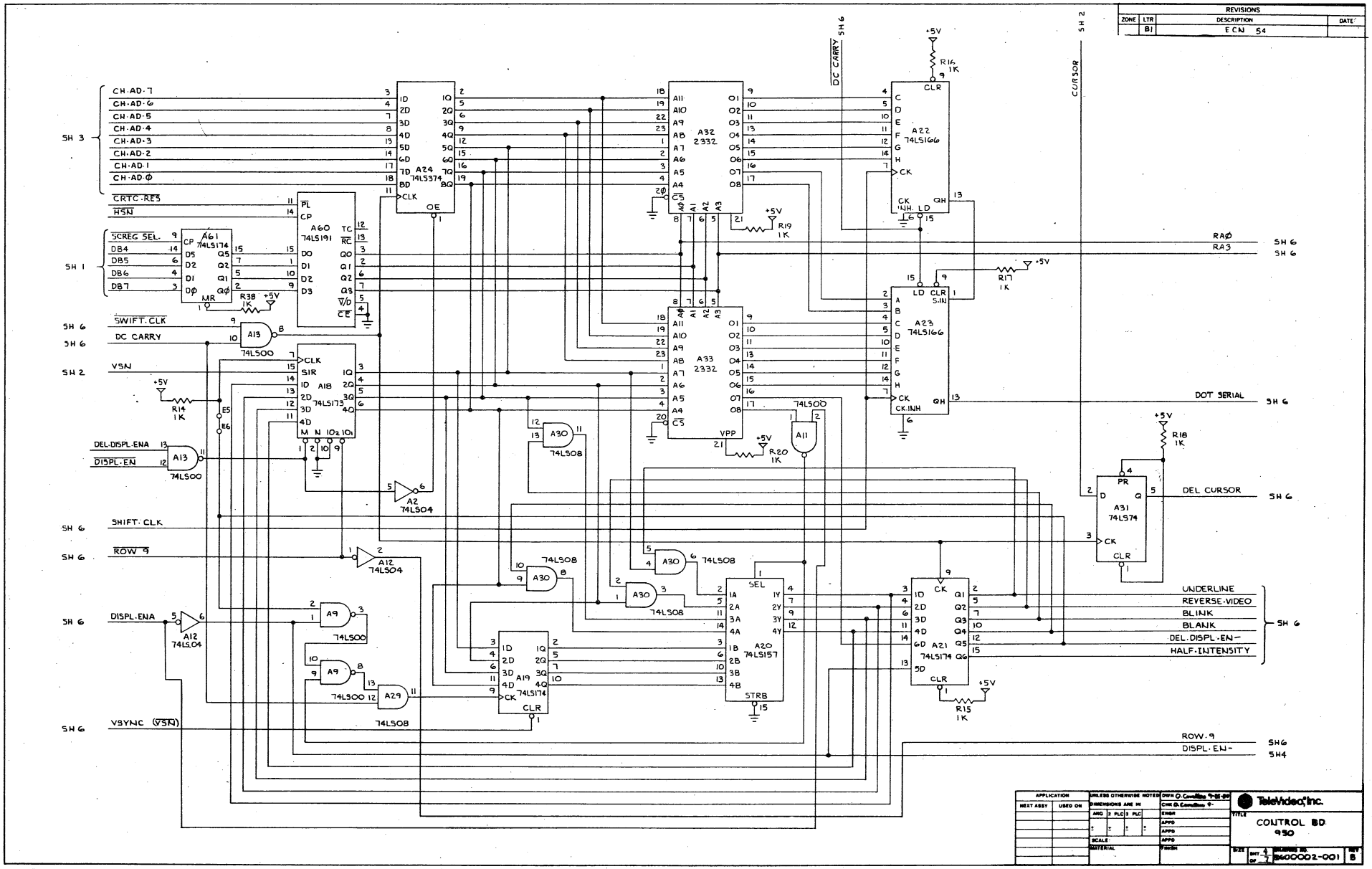
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	B1	ECN 54		

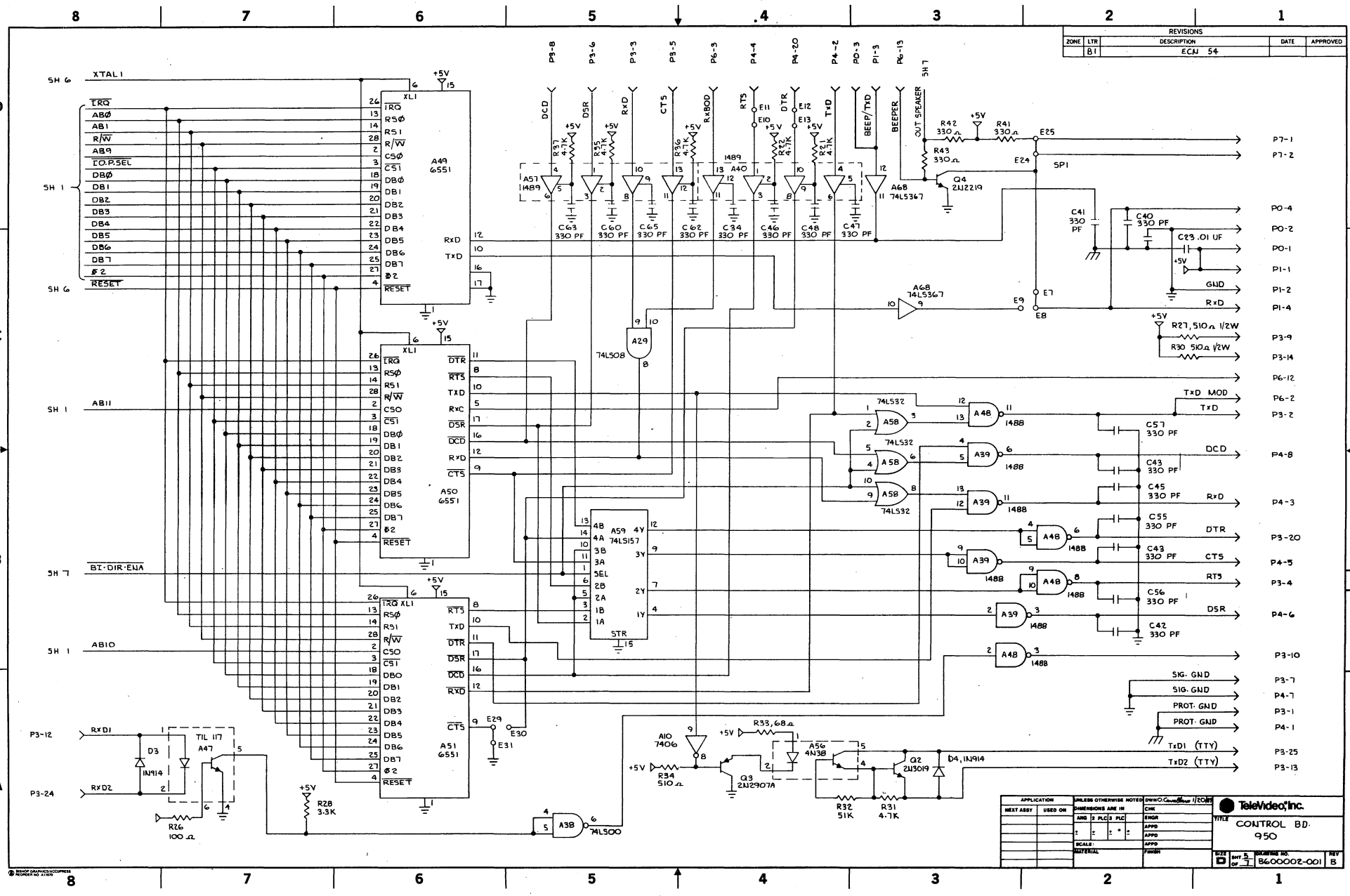
TeleVideo, Inc.

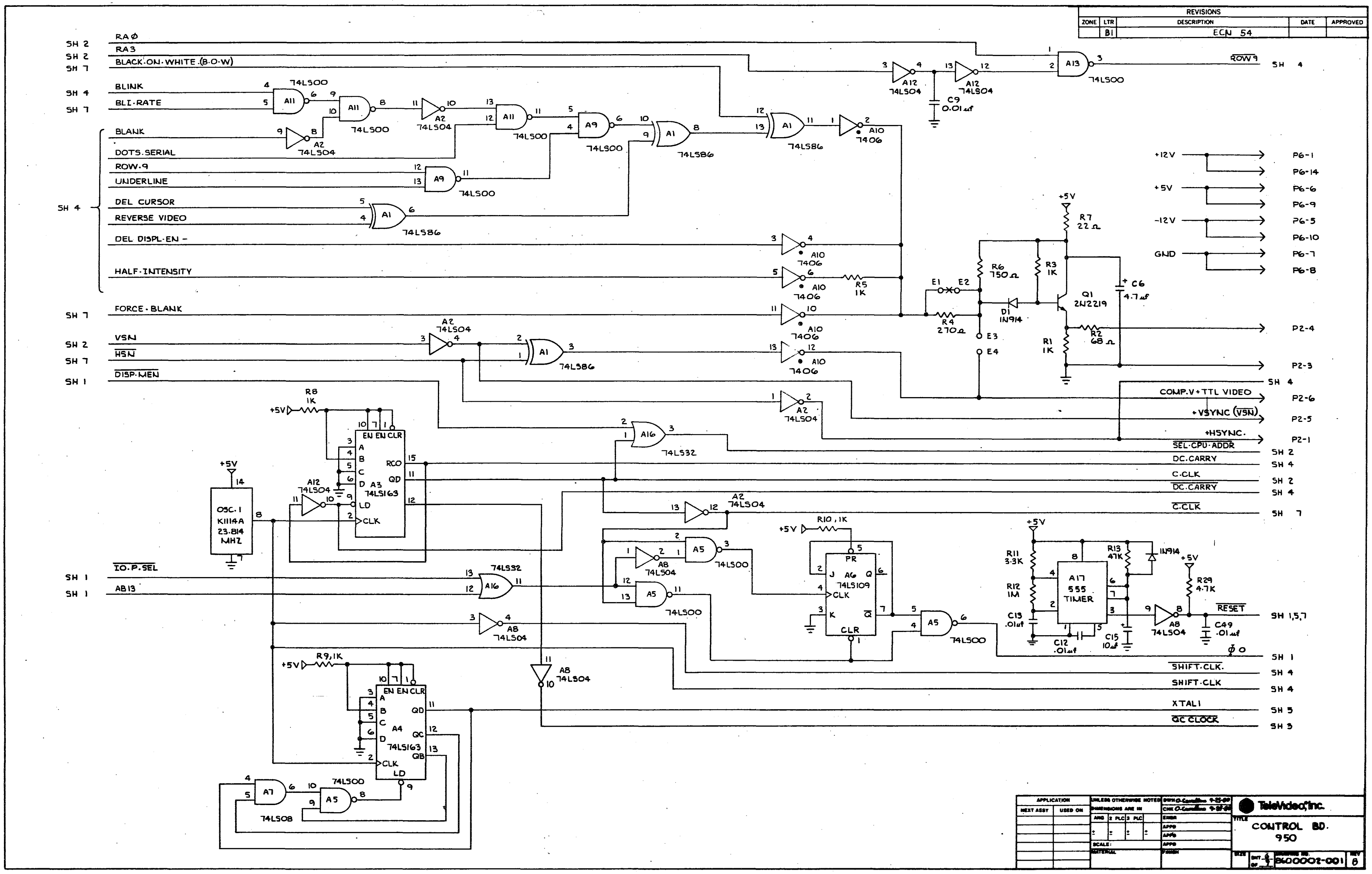
CONTROL BD. 950

860002-001 REV B

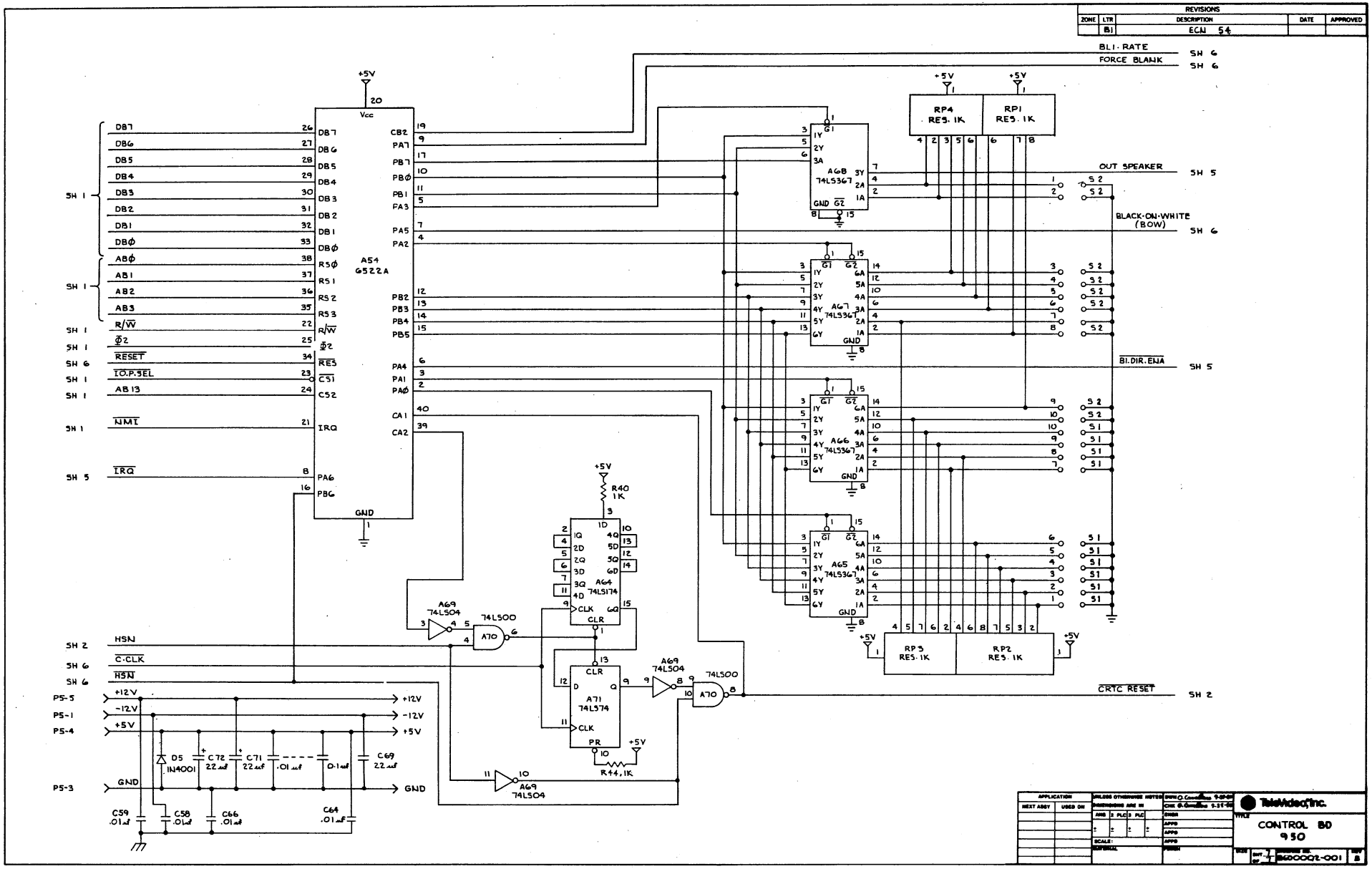

REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
B1 ECN 84
A15 74LS42
ADRAM 13
AD-RAM-11
AD.RAM-12
QC.CLK
A16 74LS32
A8 74LS04
AD-RAM-10
AD-RAM-9
AD.RAM-8
AD-RAM-7
AD-RAM-6
AD.RAM-5
AD-RAM-4
AD-RAM-3
AD-RAM-2
AD.RAM-1
AD-RAM-Ø
A25 2114
A26 2114
A27 2114
A28 2114
A34 6116
A35 6116
A36 6116
A37 6116
+5V
GND
Vcc
DM-R/W
A14 8T245
DB-7
DB-6
DB-5
DB-4
DB-3
DB-2
DB-1
DB-Ø
DMEN-EN
R/W
CH-AD-7
CH-AD-6
CH-AD-5
CH-AD-4
CH-AD-3
CH-AD-2
CH-AD-1
CH-AD-Ø
SH 1
SH 2
SH 4
SH 6
TeleMedia Inc.
CONTROL BD
950
B40008-001
B


REVISIONS
ZONE | LTR | DESCRIPTION | DATE
B1 | ECN 54
CH·AD·7
CH·AD·6
CH·AD·5
CH·AD·4
CH·AD·3
CH·AD·2
CH·AD·1
CH·AD·Ø
SH 3
CRTC·RES
HSN
SCREG SEL.
DB4
DB5
DB6
DB7
SH 1
A61 74LS174
A60 74LS191
A24 74LS374
R38 1K
+5V
SWIFT.CLK
DC CARRY
SH 6
A13 74LS00
VSN
SH 2
R14 1K
E5
E6
DEL·DISPL·ENA
DISPL·EN
A13 74LS00
74LS173
A2 74LS04
SHIFT·CLK
ROW·9
A12 74LS04
DISPL·ENA
A9 74LS00
A29 74LS08
VSYNC (VSN)
A19 74LS174
A20 74LS157
STRB
SEL
A30 74LS08
A11 74LS00
A32 2332
A33 2332
VPP
R20 1K
R19 1K
DC CARRY
A22 74LS166
A23 74LS166
R16 1K
R17 1K
CURSOR
RAØ
RA3
DOT SERIAL
A31 74LS74
R18 1K
DEL CURSOR
A21 74LS174
R15 1K
UNDERLINE
REVERSE·VIDEO
BLINK
BLANK
DEL·DISPL·EN–
HALF·INTENSITY
ROW·9
DISPL·EN–
SH 4
SH 6
SH 2
APPLICATION
NEXT ASSY
USED ON
UNLESS OTHERWISE NOTED
DIMENSIONS ARE IN
INCH
2 PLC
3 PLC
SCALE
MATERIAL
FINISH
DWN
CHK
ENGR
APPD
TeleVideo, Inc.
TITLE
CONTROL BD
950
SIZE
B
DWG NO
3600002-001
REV
B


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
B1 ECN 54
XTAL I
IRQ
AB0
AB1
R/W
AB9
IO.P.SEL
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
Ø2
RESET
A49 6551
A50 6551
A51 6551
XL1
RxD
TxD
DTR
RTS
RxC
DSR
DCD
CTS
RS0
RS1
CS0
CS1
DB0
BI-DIR-ENA
AB11
AB10
A59 74LS157
STR
A29 74LS08
A68 74LS367
A57 1489
A40 1489
A58 74LS32
A39 1488
A48 1488
A38 74LS00
A10 7406
A56 4N38
Q1 2N2219
Q2 2N3019
Q3 2N2907A
Q4 2N2219
D3 IN914
D4, IN914
TIL 117 A47
P3-8
P3-6
P3-3
P3-5
P6-3
P4-4
P4-20
P4-2
P0-3
P1-3
P6-13
DCD
DSR
RxD
CTS
RxBOD
RTS
DTR
TxD
BEEPER
BEEP/TXD
OUT SPEAKER
SP1
P7-1
P7-2
P0-4
P0-2
P0-1
P1-1
P1-2
P1-4
P3-9
P3-14
P6-12
P6-2
P3-2
P4-8
P4-3
P3-20
P4-5
P3-4
P4-6
P3-10
P3-7
P4-7
P3-1
P4-1
P3-25
P3-13
TxD MOD
SIG. GND
PROT. GND
TxD1 (TTY)
TxD2 (TTY)
P3-12
P3-24
RxD1
RxD2
R26 100Ω
R28 3.3K
R34 510Ω
R33, 68Ω
R32 51K
R31 4.7K
R27, 510Ω 1/2W
R30 510Ω 1/2W
R42 330Ω
R41 330Ω
R43 330Ω
C63 330 PF
C60 330 PF
C65 330 PF
C62 330 PF
C34 330 PF
C46 330 PF
C48 330 PF
C47 330 PF
C41 330 PF
C40 330 PF
C23 .01 UF
C57 330 PF
C43 330 PF
C45 330 PF
C55 330 PF
C43 330 PF
C56 330 PF
C42 330 PF
GND
+5V
SH 1
SH 6
SH 7
TeleVideo, Inc.
TITLE CONTROL BD. 950
SIZE D
DRAWING NO. B600002-001
REV B



REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
B1 ECN 54
SH 2 RAØ
SH 2 RA3
SH 7 BLACK·ON·WHITE (B·O·W)
SH 4 BLINK
SH 7 BLI·RATE
BLANK
DOTS.SERIAL
ROW·9
UNDERLINE
DEL CURSOR
REVERSE VIDEO
DEL DISPL·EN -
HALF·INTENSITY
SH 4
SH 7 FORCE·BLANK
SH 2 VSN
SH 7 HSN
SH 1 DISP·MEN
74LS00
74LS04
74LS86
7406
A13
ROW 9 SH 4
C9 0.01uf
+12V P6-1 P6-14
+5V P6-6 P6-9
-12V P6-5 P6-10
GND P6-7 P6-8
R7 22Ω
R6 750Ω
R3 1K
Q1 2N2219
C6 4.7uf
R5 1K
D1 1N914
R4 270Ω
R2 68Ω
R1 1K
E1 E2 E3 E4
P2-4
P2-3
SH 4
COMP.V+TTL VIDEO P2-6
+VSYNC (VSN) P2-5
+HSYNC. P2-1
R8 1K
A3 74LS163
A16 74LS32
SEL·CPU·ADDR SH 2
DC.CARRY SH 4
C·CLK SH 2
DC.CARRY SH 4
C.CLK SH 7
OSC·1 K1114A 23.814 MHZ
R10, 1K
A6 74LS109
A17 555 TIMER
R11 3.3K
R12 1M
R13 47K
1N914
R29 4.7K
C13 .01uf
C12 .01uf
C15 10uf
C49 .01uf
SH 1 IO.P.SEL
SH 1 AB13
RESET SH 1,5,7
Ø0 SH 1
SHIFT·CLK. SH 4
SHIFT·CLK SH 4
XTAL1 SH 5
QC CLOCK SH 5
R9, 1K
A4 74LS163
A7 74LS08
A5 74LS00
A8 74LS04
TeleVideo, Inc.
CONTROL BD. 950
8600002-001


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
B1 | ECN 54
BLI-RATE
FORCE BLANK
SH 6
OUT SPEAKER
SH 5
BLACK-ON-WHITE (BOW)
BI.DIR.ENA
CRTC RESET
SH 2
A54 G522A
A68 74LS367
A67 74LS367
A66 74LS367
A65 74LS367
A64 74LS174
A71 74LS74
A69 74LS04
A70 74LS00
RP4 RES. 1K
RP1 RES. 1K
RP3 RES. 1K
RP2 RES. 1K
R40 1K
R44, 1K
D5 IN4001
C72 22 mf
C71 22 mf
.01 mf
0.1 mf
C69 22 mf
C59 .01 mf
C58 .01 mf
C66 .01 mf
C64 .01 mf
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DBØ
ABØ
AB1
AB2
AB3
R/W
Ø2
RESET
IO.P.SEL
AB13
NMI
IRQ
HSN
C-CLK
P5-5
P5-1
P5-4
P5-3
+12V
-12V
+5V
GND
TeleVideo, Inc.
CONTROL BD
950
B000012-001