TEXAS INSTRUMENTS

9900

TMS9909
Floppy Disk Controller

MICROPROCESSOR SERIES™

Preliminary Data Manual

IMPORTANT NOTICES

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1. INTRODUCTION

1.1 DESCRIPTION

The TMS9909 Floppy Disk Controller (FDC) is designed to interface between almost any microprocessor and a standard disk drive. It responds to macro-level commands from the Microprocessor Unit (MPU), such as "seek and read", "seek and write", and "load the head". Data transfer is accomplished by Direct Memory Access (DMA), requiring no action from the MPU until either an error condition occurs or the operation is completed. With overall efficiency as a focal point, the TMS9909 architecture removes the necessity for a complex control system for storing and retrieving data between a disk drive and its host microprocessor. Since diskettes are now a popular bulk storage medium in micro- and minicomputer systems, the TMS9909 offers the designing engineer a single-chip solution to the diskette interface problem.

1.2 KEY FEATURES

- Compatible with IBM 3740/System 34
- Supports up to four double-sided standard 8-inch or mini 5 1/4-inch drives
- Flexible track formatting features include programmable
  - Gap lengths and contents
  - SYNC field length and contents
  - ID and data field length and contents
  - Number of ID/Data Address Marks (AMs) (1 or 3)
- Supports single density Frequency Modulation (FM), double density Modified Frequency Modulation (MFM) and Modified Modified Frequency Modulation (M^2FM) encoding algorithms
- Memory-mapped MPU interface for command/status transfer reduces software overhead
- Programmable on-chip write precompensation and low write current selection
- Programmable data transfer rates of 125, 250 and 500 kilobits/sec (Direct Memory Access (DMA) compatible)
- On-chip Cyclic Redundancy Check (CRC) generation and verification
- Single or multiple sector read/write for soft- and hard-sectored disks
- Partial sector read/write with CRC verification
- Capability to intermix disk types
- On-chip clock generation, only a 6 MHz crystal needed
- Programmable track step, settle, and head load times
- Single 5 V supply, fully TTL compatible

1.3 TYPICAL APPLICATION

Figure 1 shows the TMS9909 Floppy Disk Controller (FDC) in a typical TMS9995 system. Here the FDC interfaces the microprocessor to four disk drives. The TMS9995 controls the TMS9909 by means of a memory-mapped interface that utilizes eight sequential decode memory locations to facilitate an exchange of command information and status returns.

A Direct Memory Access Controller (DMAC) is implemented to provide fast transfer of large blocks of data. The TMS9995's memory interface sets up the DMAC prior to the start of each transfer. Typical setup data includes the start address of the memory area and the direction of data flow, i.e., a memory read or memory write. When a read or write command is written to the command register (along with the appropriate parameters specifying the drive(s), track sector(s), etc.), the FDC selects the specified drive(s) and checks the requested location on the diskette(s) before a DMA transfer. If no error condition is encountered, the specified number of bytes are read or written to the diskette(s). At the conclusion of the task, the FDC interrupts the MPU (TMS9995) with a status return, indicating either a successful operation or a problem condition.

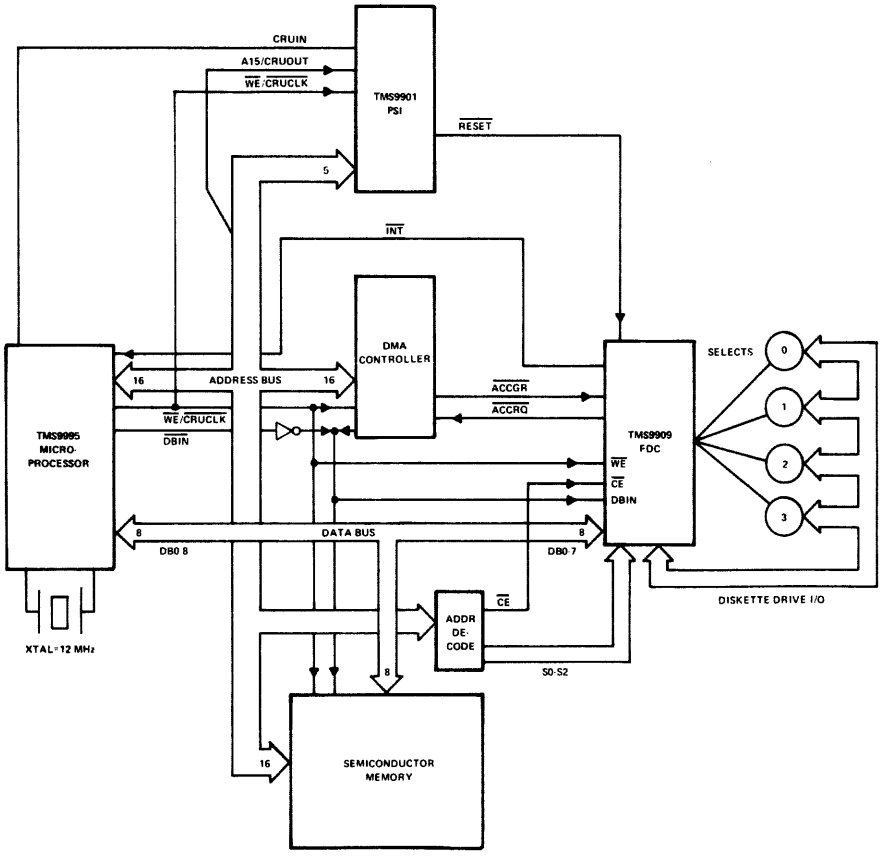


FIGURE 1 — TMS9995 TYPICAL SYSTEM CONFIGURATION

1.4 FLOPPY TERMINOLOGY

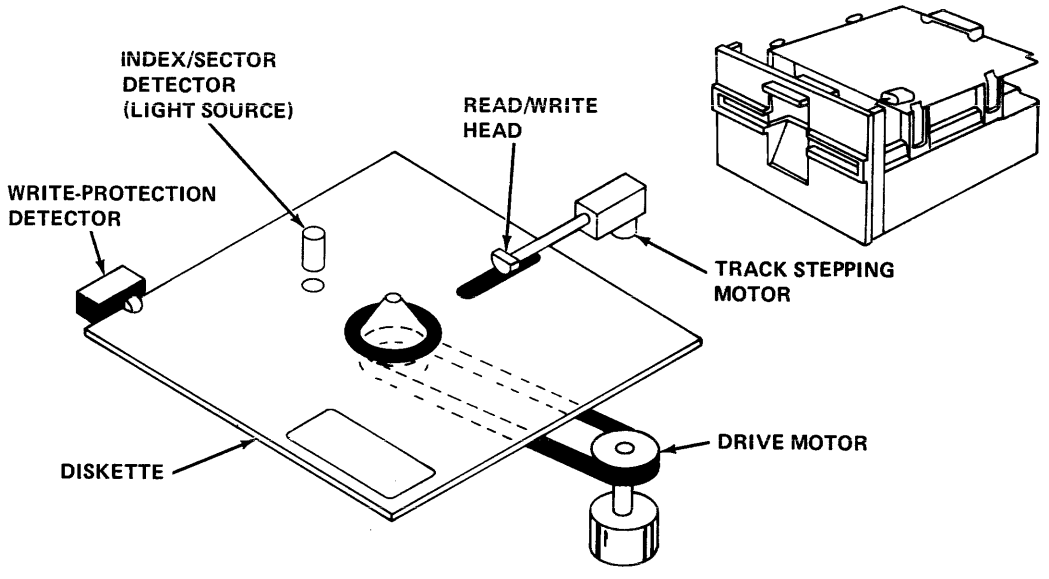


FIGURE 2 — TYPICAL DISK DRIVE

1.4.1 Physical Characteristics

Track Thin circular path on a diskette used for storing information.

Cylinder Term used for a track in a dual head sense, i.e., a double-sided track is a cylinder.

Sector Subdivision of a track.

Index Hole Single hole punched in a diskette to mark the beginning of each track.

Sector Hole For hard-sectored diskettes, a hole is punched to mark the beginning of each sector in a track.

Head Step Time Duration of the track stepping pulses to the head step motor.

Head Settling Time After positioning to a new track, time allowed for the head to settle, i.e., time between the last step pulse and any further action (such as a head load signal).

Head Load Time Delay from the moment the head load signal becomes active until the head is loaded and the read/write begins.

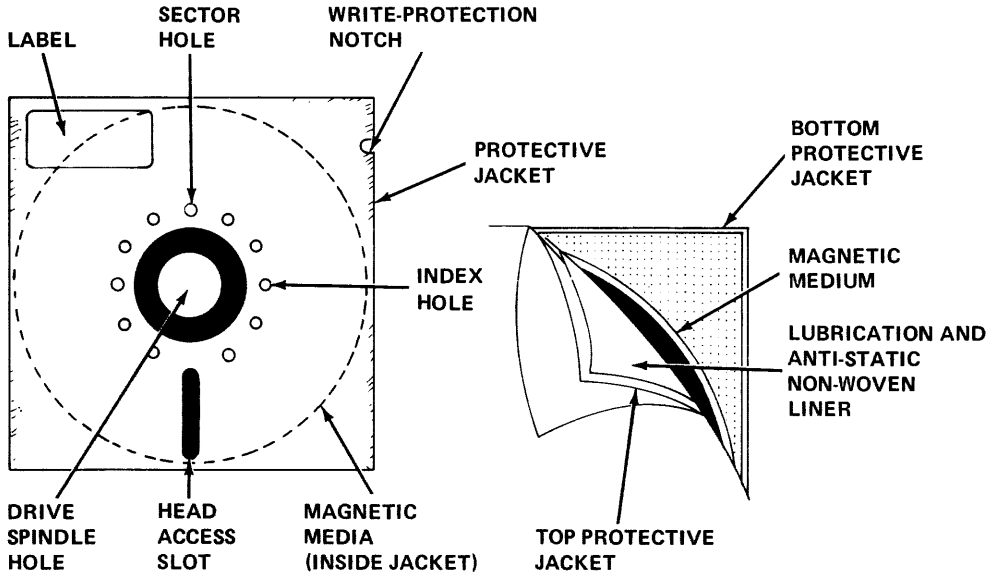


FIGURE 3 — FLOPPY DISKETTE (HARD-SECTORED)

1.4.2 Format Options

Hard-Sectored Diskette Type of diskette that uses sector holes instead of an ID field to define a data field. One of the holes on the diskette is an index hole.

Soft-Sectored Diskette Type of diskette that has one index hole and no sector holes. Each track sector is defined by an ID field.

ID Field (Soft) Part of a sector used for sector ID parameters.

Data Field Part of a sector used for storing data.

SYNC Field Used on hard- and soft-sectored diskettes to synchronize the controller to read the upcoming Address Marks.

Address Marks (ID and Data) Formed by interleaving an AM clock byte (a unique bit pattern that differs from normal encoding rules) with an AM data byte. Either one or three AM(s) follow the SYNC field on both hard- and soft-sectored diskettes. Used for field identification.

ID Bytes (Soft) Four bytes used during a soft-sectored read or write command to determine whether the track and sector are correct. May be appended by a maximum ten bytes of any value.

CRC Bytes (ID and Data) Check bytes used in error detection.

Record Data field plus Address Marks. Maximum combined length is 4095 bytes.

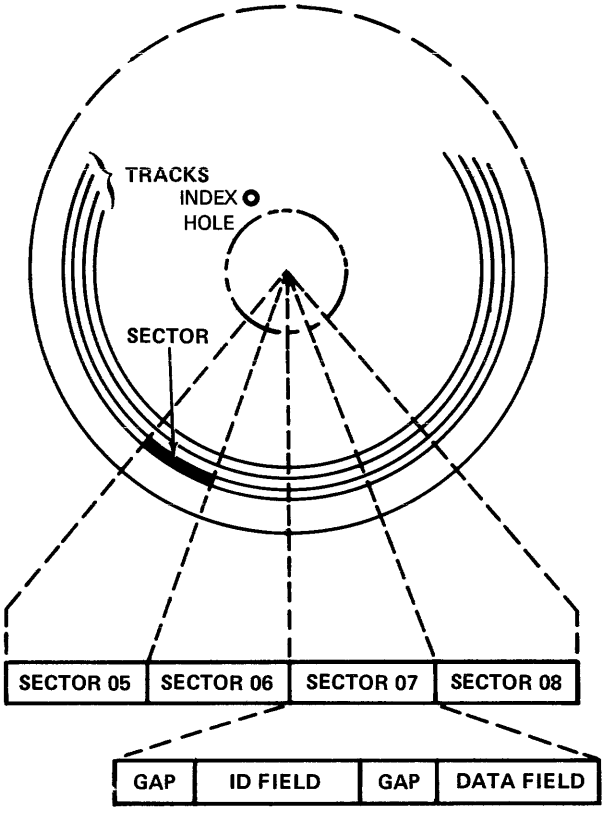


FIGURE 4 — DISKETTE FORMAT (SOFT-SECTORED)

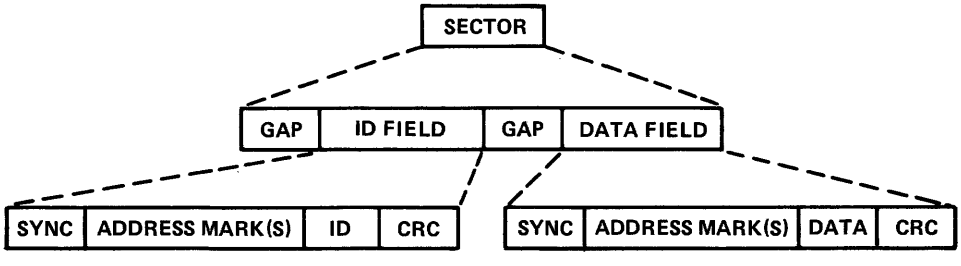


FIGURE 5 — DIAGRAM OF SECTOR CONTENTS (SOFT)

1.4.3 Data Encoding Terminology

Bit Cell Two consecutive bits of information with the leading bit always being a clock bit and the second bit always being a data bit. A half-bit cell may be either a clock or data bit.

Bit-Shift The spatial shift of the maximum of a magnetic flux transition pulse as it is recorded on the magnetic media due to the close proximity of its neighboring pulses.

Data Precompensation The data dependent on slight advancing or retarding of the moment a pulse is written to ensure that the pulse maximum is recorded as close as possible to the proper half-bit cell interval.

Single Density (FM) Standard recording format.

Double Density (MFM,M^2FM) Packed recording techniques to increase the number of bits per track. Requires a more sophisticated technique of data separation than single-density recording to ensure reliable operation.

Low Write Current A reduction of current to the read/write head so as to lessen the total flux magnitude recorded on the diskette. This option is implemented to prevent bit-shift.

Data Separation The data separation function, which in fact does not actually separate data, involves regenerating a clock or strobe signal to sample information coded onto the serial bit stream being read from the diskette.

2. ARCHITECTURE

The TMS9909 FDC is a memory-mapped device designed as a peripheral for almost any 8 or 16-bit microprocessor. The internal architecture of the FDC is shown in Figure 6. The device consists of five main functional subsystems:

1) Disk Interface — Output lines controlling the drive mechanics and input lines sensing its current status.
2) MPU Interface — Buffers and registers used by the host MPU to control the device's operation and read status.
3) Direct Memory Access Interface — Lines used to communicate with a DMAC to control the read or write data transfers.
4) Read/Write Channel — Logic that executes the serial/parallel and parallel/serial conversions, interleaves clock and data into one stream of serial and provides the interface to the disk drive(s).
5) Microcontroller ROM — Supervises the overall operation of the device, sequences the instruction executions and sets the status codes.

2.1 HOST SYSTEM INTERFACE

Communication between the host (MPU) and the TMS9909 is handled by a number of memory-mapped registers. They are accessed by placing the address on lines S0-S2 and carrying out a memory read (to obtain status information) or a memory write (to issue commands or set parameters). These register select lines are usually connected to the three least significant address lines of the host microprocessor (S0 = MSB, S2 = LSB) so that the TMS9909 appears to consist of eight consecutive memory locations.

2.1.1 Register Structure

The register structure of the TMS9909 is given in Table 1. The command register and the status register share the same address location, S0-S2 = 000. The state of DBIN determines whether a command is being written into the command register (write only) or whether status is being read from the status register (read only). When the FDC is required to execute an instruction, a command byte is written to this location by the host microprocessor. This has two effects: 1) selection of the command to be executed and 2) selection of the RAM partition (defined by D0 and D1 of the command byte) within the TMS9909 that must be loaded with parameters before the command is actually executed.

After execution of a command, the FDC's status may be read by addressing the status register with S0-S2 = 000 and DBIN = 1. Table 10 contains the status return codes.

The remaining seven registers within each partition of the TMS9909 determine the mode of operation of the FDC. For maximum flexibility, almost every variable factor is user-programmable, e.g., head movement timing, sector size and format. Most of these variables are set once during the initialization of the TMS9909 and do not have to be rewritten. Others, such as the track(s) and sector(s) to be accessed, must be loaded at each execution of the command unless the same disk area is required, e.g., a retry. Since different parameters are needed for each command, the two most significant bits of the command byte, D0 and D1, select the partition of RAM that is addressed. A list of the partitions and their associated commands and parameters is given in Table 1.

2.1.2 Direct Memory Access DMA Interface

To execute a data transfer between the floppy disk and system memory, a DMA scheme may be implemented. A DMAC enables the rapid transfer of large blocks of information with minimum disruption to the host MPU so other tasks may be performed.

The TMS9909 has two interface lines that connect to a DMAC: Access Request ($\overline{\text{ACCRQ}}$) and Access Grant ($\overline{\text{ACCGR}}$). Their pin connections are shown in Figure 7.

During a disk read operation, the byte to be read is assembled from the incoming data/clock stream. When a complete byte has been received, the Access Request line is pulled low to indicate that a data transfer is required. The DMAC then responds with an Access Grant signal which indicates that it has halted the MPU. With the occurrence of the Access Grant, the TMS9909 resets the $\overline{\text{ACCRQ}}$ line high and places the byte on the data bus.

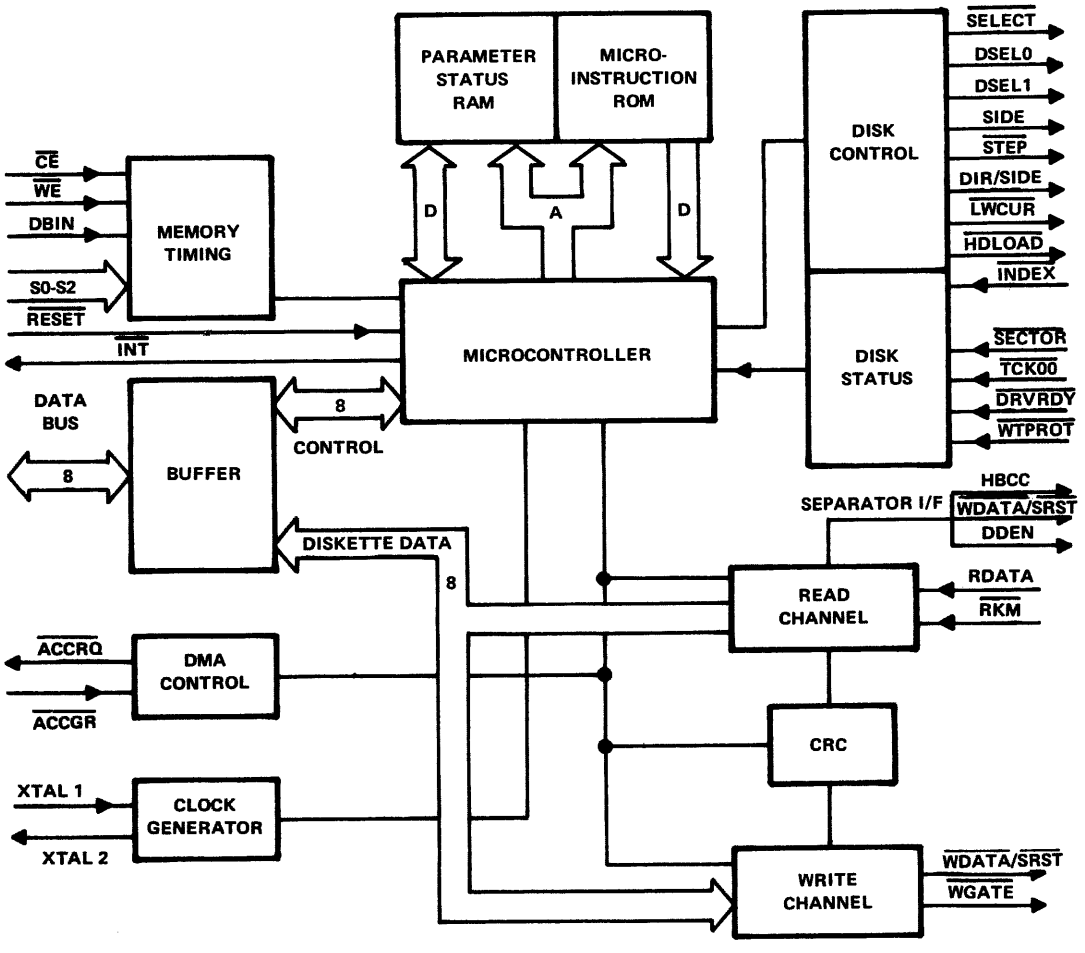


FIGURE 6 — TMS9909 INTERNAL ARCHITECTURE

TABLE 1 — REGISTER STRUCTURE

PARTITION REFERENCE		ADDRESS			COMMAND/STATUS REGISTER COMMAND PARAMETERS	COMMAND REGISTER								COMMAND
D0	D1	S0	S1	S2		D0	D1	D2	D3	D4	D5	D6	D7	
					PARTITION 00									
0	0	0	0	0	Command/status register									
0	0	0	0	1	ID AM clock pattern	0	0	0	0	X	X	X	X	CINT
0	0	0	1	0	ID AM data pattern	0	0	0	1	X	X	X	X	ABEX
0	0	0	1	1	ID byte 1 (soft sector)/	0	0	1	0	X	X	X	X	RSTC
					Starting sector−1 (hard sector, read or write)	0	0	1	1	X	X	X	X	AIDA
0	0	1	0	0	ID byte 2									
0	0	1	0	1	ID byte 3									
0	0	1	1	0	ID byte 4									
0	0	1	1	1	ID field information									
					PARTITION 01									
0	1	0	0	0	Command/status register									
0	1	0	0	1	Head step time A	0	1	0	0	DD3	DD2	DD1	DD0	RDAR
0	1	0	1	0	Head settle time A	0	1	0	1	X	X	X	X	DEST
0	1	0	1	1	Head load time A	0	1	1	0	X	X	X	X	HDUN
0	1	1	0	0	Head step time B	0	1	1	1	X	X	X	X	HDLD
0	1	1	0	1	Head settle time B									
0	1	1	1	0	Head load time B									
0	1	1	1	1	Rate allocation map									
					PARTITION 10									
1	0	0	0	0	Command/status register									
1	0	0	0	1	Encode, xfer rate and	1	0	0	0	0	S	D	D	HARD
					Record length (MSN)	1	0	0	0	1	S	D	D	SORD
1	0	0	1	0	Record length (LSB)/	1	0	0	1	0	S	D	D	HAWR
					Starting sector−1 (hard sector format)	1	0	0	1	1	S	D	D	SOWR
1	0	0	1	1	$\overline{\text{LWCUR}}$, Precompensation, No. of records	1	0	1	0	0	S	D	D	HAFT
					to xfer	1	0	1	0	1	S	D	D	SOFT
1	0	1	0	0	New physical track	1	0	1	1	1	S	D	D	UTRD
1	0	1	0	1	Data AM clock pattern	1	0	1	1	0	X	X	X	ILLE-
1	0	1	1	0	Data AM data pattern									GAL
1	0	1	1	1	Data field information									
					PARTITION 11									
1	1	0	0	0	Command/status register									
1	1	0	0	1	FILL byte	1	1	0	0	X	X	X	X	AFAS
1	1	0	1	0	SYNC byte	1	1	0	1	X	X	X	X	NOP
1	1	0	1	1	SYNC bytes before field	1	1	1	0	X	X	X	X	NOP
1	1	1	0	0	Physical track of DR0	1	1	1	1	X	X	X	X	NOP
1	1	1	0	1	Physical track of DR1									
1	1	1	1	0	Physical tarck of DR2									
1	1	1	1	1	Physical track of DR3									

NOTES:
a. The NOP command bytes may be used as instructions.
b. Command register (write-only) and status register (read-only) share same address location, S0-S2 = 000, in all four partitions.
c. DD0-3 = Disk Drive nos. 0-3.
d. DD= D6 D7
00 = Drive 0
01 = Drive 1
10 = Drive 2
11 = Drive 3
DSEL0 and DSEL1 are connected to D6 and D7 of the command register of Partition 10 for all read, write and format operations.
e. S = side

A similar process occurs during disk write operations with the DMAC driving the DBIN line high to get a byte from memory and transfer it to the TMS9909. The sense of the DBIN line is inverted with respect to the TMS9909 during DMA accesses (low for DMA read, high for MPU read, high for DMA write, low for MPU write). This is taken into account when the internal data bus buffers are enabled. However, if external buffers are used, a small amount of logic is required to ensure correct operation.

During read and write operations, the DMAC must respond within a time interval dependent upon the transfer rate (since the next byte is being read from (or written to) the drive while the previous byte is being transferred to (or from) memory). The $\overline{\text{ACCGR}}$ line must make a complete transition, i.e., from high to low and back to high within the following times:

TRANSFER RATE	500 kHz	250 kHz	125 kHz
$\overline{\text{ACCGR}}$ Hi-Lo-Hi (μs)	13 μs	27 μs	55 μs

If the DMAC does not respond within these times, the FDC will abort the current operation. If a read operation was in progress, the FDC:

1) Sets the Handshake Abort bit in the status register.
2) Stops issuing $\overline{\text{ACCRQs}}$.
3) Reads until the end of the sector.
4) Checks the CRC bytes, if the data CRC bit is set.
5) Sets the status return with a data field CRC error if one is found; otherwise, a return of data overflow.
6) Issues an interrupt to the host MPU and resets the status register Busy bit to one (1 = Not Busy).

NOTE

The DMA device must be reconfigured if another attempt is to be made to read the diskette.

If a write operation is in progress when an abort occurs, the FDC:

1) Sets the Handshake Abort bit in the status register.
2) Writes the last byte transferred to the remainder of the field.
3) Writes two CRC bytes (if selected) and one FILL byte.
4) Stops writing ($\overline{\text{WGATE}}$ goes high).
5) Sets the correct status return for a data underflow error.
6) Issues an interrupt to the host MPU and resets the status register Busy bit to one.

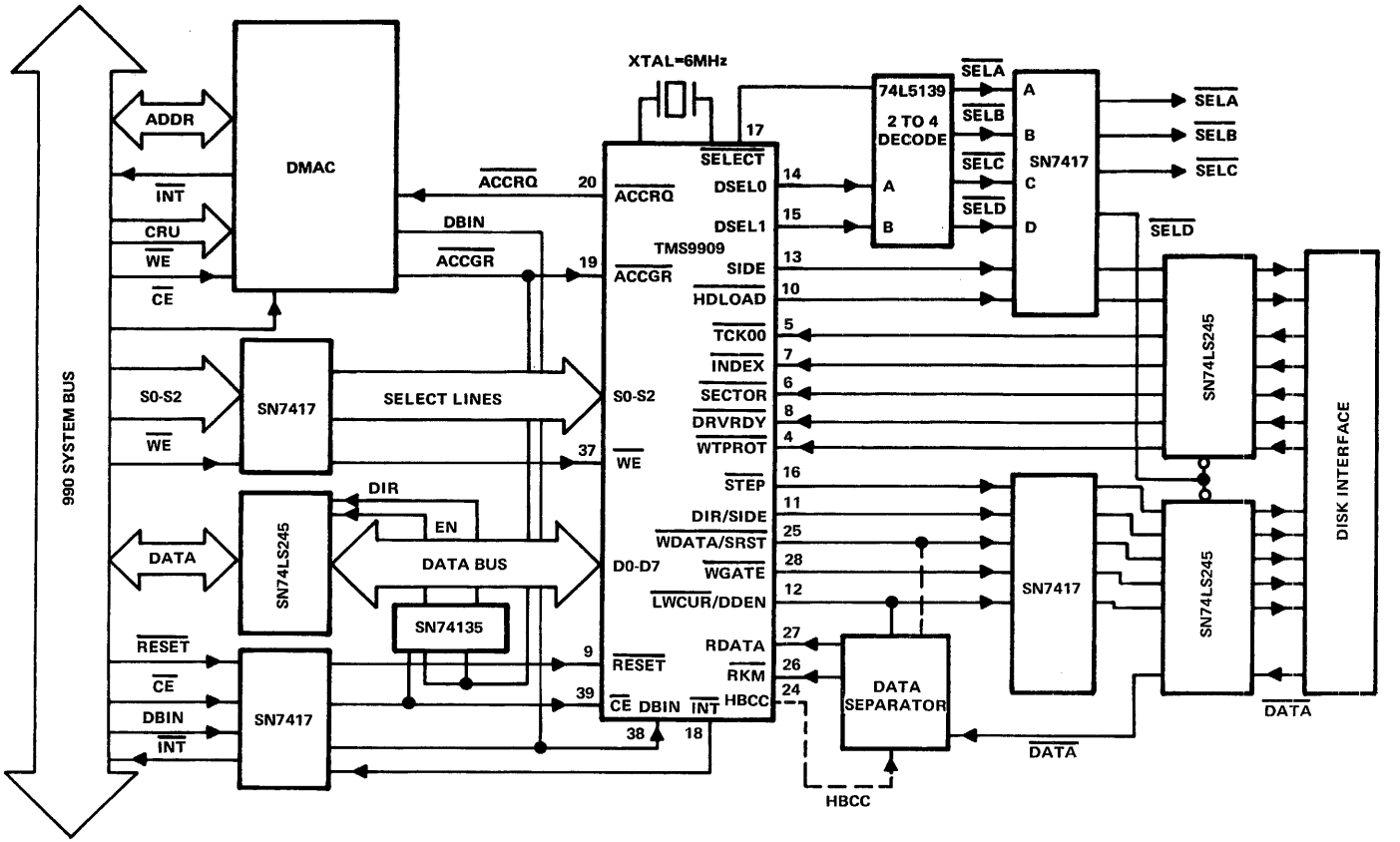


FIGURE 7 — TYPICAL DISK DRIVE/MPU INTERFACE

2.2 DISKETTE DRIVE INTERFACE

The TMS9909 provides all necessary signals for interfacing as many as four double-sided drives. The outputs from the TMS9909 are push-pull and will drive TTL inputs. They are usually connected to the drives by means of buffer devices. A diagram showing the connections between the TMS9909 and a typical diskette drive is shown in Figure 7.

During a write operation, the clock and data pulses are generated within the FDC. The encoding scheme implemented for this data stream is selected by the user when the internal FDC RAM (Partition 10, parameter 001) is set up. Standard algorithms are used to decide whether or not a clock pulse is to be generated in the cases of MFM and M^2FM encoding. For FM encoding, all clock bits are set.

During a read operation, the interleaved data and clock pulses are separated within the TMS9909. An external data separator circuit is required to gate these alternating clock and data pulses into the FDC. The TMS9909 utilizes the rising edge of the $\overline{RKM}$ input as a strobe for the data. In the case of low-density FM encoding, this circuit may be a simple monostable multivibrator. For high density MFM and M^2FM encoding, a more sophisticated technique is required to clock the incoming data stream. (See Appendix A.) Whatever the circuit implementation, $\overline{RKM}$ must have a rising (strobe) edge twice during each 'bit cell'. A 'bit cell' is defined as two consecutive bits of information with the leading bit always being a clock bit and the second bit always being a data bit. The rising edge of $\overline{RKM}$ should occur once in the middle of the clock bit (1/4 of the way through the bit cell) and once in the middle of the data bit (3/4 of the way through the bit cell). Refer to Figure 8 for an example of clocking incoming data for MFM encoding.

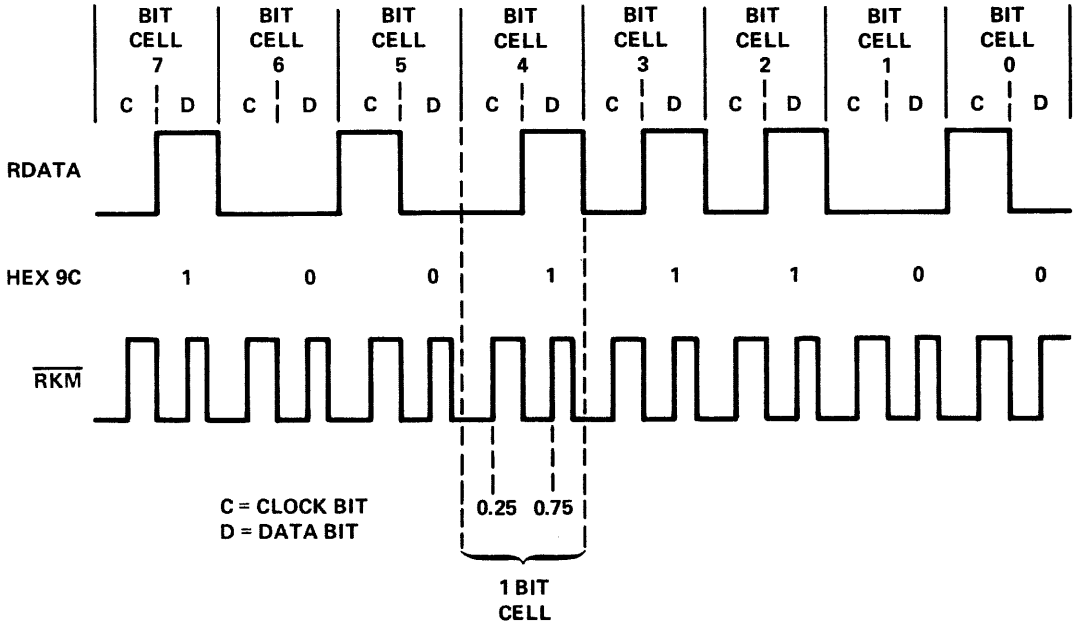


FIGURE 8 — MFM ENCODING OF HEX 9C AND $\overline{RKM}$

2.3 PIN ASSIGNMENTS

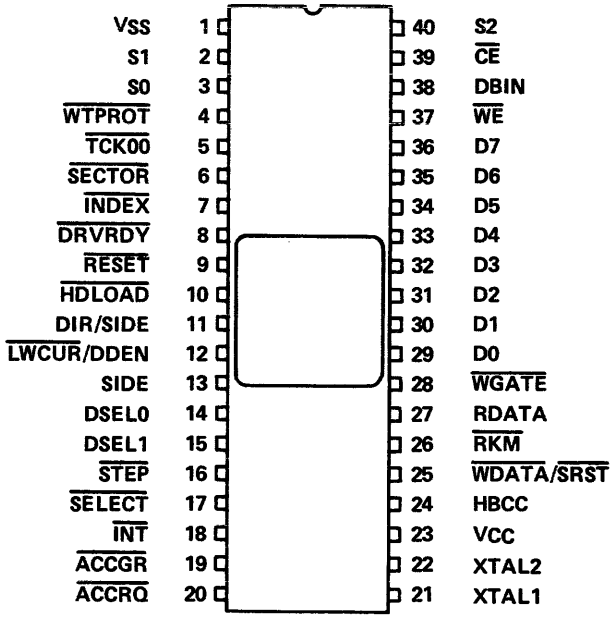


FIGURE 9 — TMS9909 PIN ASSIGNMENTS

2.4 PIN DESCRIPTIONS

TABLE 2 — TMS9909 PIN DESCRIPTIONS

SIGNATURE	PIN	I/O	DESCRIPTION
$\overline{\text{ACCRQ}}$	20	O	Access Request. This output is set low to indicate to the DMA controller that a byte is ready for transfer to or from memory. It is reset by $\overline{\text{ACCGR}}$ within a maximum of 100 ns.
$\overline{\text{ACCGR}}$	19	I	Access Grant. This input is the DMA response to $\overline{\text{ACCRQ}}$. It enables the data I/O buffers of the TMS9909 and resets the $\overline{\text{ACCRQ}}$ output during byte transfers.
$\overline{\text{CE}}$	39	I	Chip Enable. When pulled low, the interface with the host microprocessor is enabled. Commands and parameters may be written and the status of the FDC may be read. $\overline{\text{CE}}$ is obtained by decoding the address bus.
DBIN	38	I	Data Bus In. This is the bus signal that defines the direction of data transfer between system memory and the FDC. It is high for MPU reads and DMA writes. It is low for MPU writes and DMA reads.

TABLE 2 — TMS9909 PIN DESCRIPTIONS (Continued)

SIGNATURE	PIN	I/O	DESCRIPTION
$\overline{WE}$	37	I	Write Enable. When active (low), $\overline{WE}$ indicates that data from the host processor is available for transfer to the FDC. It acts as a strobe for data being sent from the host to the FDC.
S0 S1 S2	3 2 40	I I I	Internal Register Select. The particular register accessed during a read or write operation is determined by the state of these lines.
$\overline{INT}$	18	O	Interrupt. This output goes active low when the TMS9909 requires service from the host microprocessor. It indicates the termination of an executable command or a software reset and is reset by a CINT command.
$\overline{RESET}$	9	I	Power-Up Reset. The FDC will be initialized after the following sequence of events: 1) V_{CC} within specification 2) $\overline{RESET}$ active (low) for 1 microsecond (MIN), 3) RSTC executed, 4) CINT executed.
XTAL1 XTAL2	21 22		Crystal. XTAL1 and XTAL2 are normally connected to a 6 MHz crystal to drive the on-board clock generator. Alternatively, a 6 MHz reference may be connected to XTAL1 with XTAL2 unconnected.
V_{CC} V_{SS}	23 1	I I	Supply voltage (+ 5 V nominal). Ground reference voltage.
DSEL0 DSEL1 $\overline{SELECT}$	14 15 17	O O O	Drive Select Lines. Binary encoded drive select lines for up to four diskette drives. DSEL0 and DSEL1 give a valid drive select code when $\overline{SELECT}$ is active (low).
SIDE	13	O	Side Select. Indicates to the drive which diskette surface is active (0 for single-sided).
$\overline{HDLOAD}$	10	O	Head Load. This output is connected to the disk drives and causes the head of the selected drive to be brought into contact with the diskette surface.
$\overline{STEP}$	16	O	Track Access Step. A 50-percent duty cycle pulse is output on this pin to cause the head position to be stepped over one track. The period of the pulse is programmable.
DIR/SIDE	11	O	Step Direction/Side. When the head is stepping, the output is DIR. As DIR, a low output defines stepping towards the outside of the disk while a high will cause stepping towards the center. After stepping, this output functions the same as the SIDE output pin.
$\overline{DRVRDY}$	8	I	Drive Ready. An active low on this pin indicates that the selected drive is ready for track accessing or data transfer. $\overline{DRVRDY}$ must be activated within 1.25 seconds of drive selection or the command will be aborted.

TABLE 2 — TMS9909 PIN DESCRIPTIONS (Continued)

SIGNATURE	PIN	I/O	DESCRIPTION
$\overline{\text{TCK00}}$	5	I	Track 00. $\overline{\text{TCK00}}$ is set active (low) by the drive when the head is at its maximum radius from the center of the diskette, i.e., track zero.
$\overline{\text{INDEX}}$	7	I	Index Hole. The selected disk drive produces a pulse (active low) on this line each time an index hole is detected by the drive.
$\overline{\text{SECTOR}}$	6	I	Sector Hole. Active low transitions on the $\overline{\text{SECTOR}}$ line are produced each time a sector hole is encountered on a hard-sectored diskette.
$\overline{\text{WTPROT}}$	4	I	Write-Protected Diskette. When active (low), the diskette has been mechanically protected and cannot be written to by the FDC.
$\overline{\text{WDATA}}/\overline{\text{SRST}}$	25	O	Write Data/Separator Reset. The inverted data stream appears on this output while $\overline{\text{WGATE}}$ is low. When $\overline{\text{WGATE}}$ is high, a low signal ($\overline{\text{SRST}}$) indicates that the FDC is reading from the disk.
$\overline{\text{WGATE}}$	28	O	Write Gate. This output becomes active low at least 1 μs before data appears on the $\overline{\text{WDATA}}$ output and stays active until after the last valid $\overline{\text{WDATA}}$ transition has occurred.
$\overline{\text{LWCUR}}$/DDEN	12	O	Low Write Current/Double Density. This may be activated by the host on any write command. DDEN is activated on MFM/M^{2}FM reads and is used by the data separator. It is high for double density and low for single density.
RDATA	27	I	Read Serial Data Line. RDATA consists of interleaved clock and data bits from the diskette being read.
$\overline{\text{RKM}}$	26	I	Strobe Pulse for RDATA. Read data is assumed valid on the rising edge of the $\overline{\text{RKM}}$ pulse. $\overline{\text{RKM}}$ must be generated by the data separator circuit. Since this input is used for internal $\overline{\text{RKM}}$ "time-outs", i.e., leaving a gap at the end of a sector, $\overline{\text{RKM}}$ must always be locked.
HBCC	24	O	Half-Bit Cell Frequency Clock. This is 2 X transfer rate. HBCC may be used to start the data separator near frequency lock.
D0	29	I/O	Data Bus.
D1	30	I/O	
D2	31	I/O	
D3	32	I/O	
D4	33	I/O	
D5	34	I/O	
D6	35	I/O	
D7	36	I/O	

3. DEVICE OPERATION

The host microprocessor controls the TMS9909 by issuing commands over the system data bus. The commands are written to a register in the FDC called the command register when the internal register select lines equal zero (S0-S2=000) and DBIN = 0. A MPU read to this location is executed when DBIN = 1 and results in a status return. Thus the same location serves as both command and status register. There are three basic types of commands that may be issued by the host microprocessor to the TMS9909 command register: state commands, setup commands and executable commands.

1) State commands: (Clear Interrupt, Abort Execution, and Reset) These commands change the state of the FDC. Reset is the only state command that provides a status return. Abort Execution leaves the FDC in an unknown state.

2) Setup commands: (Assign ID attributes, define step rates, assign FILL and SYNC bytes) These commands load the information used in read/write/recalibrate and format commands into the parameter registers.

3) Executable commands: These commands cause the TMS9909 to interact with one or more of the disk drives. Executable commands do not initiate execution until the last required parameter byte is written into the appropriate register. The command then returns a status byte or error condition after execution.

Ten executable commands are listed as follows:

- Recalibrate Drive Assign Rates (RDAR)
- Head Load/Unload (HDLD/HDUN)
- Hard/Soft Sector Read (HARD/SORD)
- Hard/Soft Sector Write (HAWR/SOWR)
- Hard/Soft Sector Format (HAFT/SOFT)
- Unformatted Track Read (UTRD)

Sector seeks are performed as an integral part of these read, write, and format commands to save software. For example, a single read command will step the head to a new track, load it, read the data and return a status report.

The TMS9909 RAM is divided up into four partitions (see Table 1) of seven consecutive bytes (the command byte being a common byte located at address S0-S2 = 000, followed by seven consecutive parameter bytes in each partition). Each partition is defined by a unique set of commands. The partition is selected by decoding the first two bits of the command byte (D0, D1), e.g., 00 = Partition 00, 01 = Partition 01, etc.

A list of the various commands, the command byte for each, and a brief description of their action is given in Table 3. A detailed explanation of individual commands and parameters is discussed in the following section. A flowchart of the FDC command priorities and options is given in Figure 10.

TABLE 3 – TMS9909 COMMANDS

COMMAND	MNEMONIC*	COMMAND CODE** D0-D7	FUNCTION
Reset Controller	RSTC	0010XXXX	Initialize FDC internal status and output pins.
Abort Execution	ABEX	0001XXXX	Terminate active command (at sector end for writes).
Clear Interrupt	CINT	0000XXXX	Deactivate $\overline{INT}$ pin (HIGH).
Assign ID Attributes	AIDA	0011XXXX	Define Address Marks and contents of ID fields.
Define Stepping Rates	DEST	0101XXXX	Define stepping rates used during track seeks.
Assign FILL and SYNC	AFAS	1100XXXX	Define FILL and SYNC bytes for current format.
Recalibrate Drives, Assign Rates	RDAR	0100DDDD	Define stepping rates and step selected drives to track 00 (where D = 1).
Head Unload	HDUN	0110XXXX	Select drive, unload disk head.
Head Load	HDLD	0111XXXX	Select drive, load disk head.
Hard Sector Read	HARD	10000SDD	Seek physical track, locate and transfer data from hard-sectored diskette.
Soft Sector Read	SORD	10001SDD	Seek physical track, locate ID and transfer data from soft-sectored diskette.
Hard Sector Write	HAWR	10010SDD	Seek physical track, locate sector hole and write data to hard-sectored diskette.
Soft Sector Write	SOWR	10011SDD	Seek physical track, locate ID and write data to soft-sectored diskette.
Hard Sector Format Track	HAFT	10100SDD	Seek physical track, locate sector hole and format track to next sector hole.

TABLE 3 — TMS9909 COMMANDS (Continued)

COMMAND	MNEMONIC*	COMMAND CODE** D0-D7	FUNCTION
Soft Sector Format Track	SOFT	10101SDD	Seek physical track, locate index pulse and format track to next index pulse.
Unformatted Track Read	UTRD	10111SDD	Seek physical track, read data until SYNC followed by data AM is detected; then read data to host.

*Commands may be grouped as follows:

Read Commands ..... HARD, SORD, UTRD
Write Commands..... HAWR, SOWR
Format Commands..... HAFT, SOFT

**Codes may be interpreted as follows:

X = Don't Care
DDDD = Drive(s) to recalibrate with Drive 0 represented by D7 and Drive 3 represented by D4. For example: if DDDD = 0101, then recalibrate Drives 2 and 0.
S = Disk side. (S = 0 for single-sided disks.)
DD = Drive selected. For example: if DD = >10 (> = hex), Drive 2 is selected.

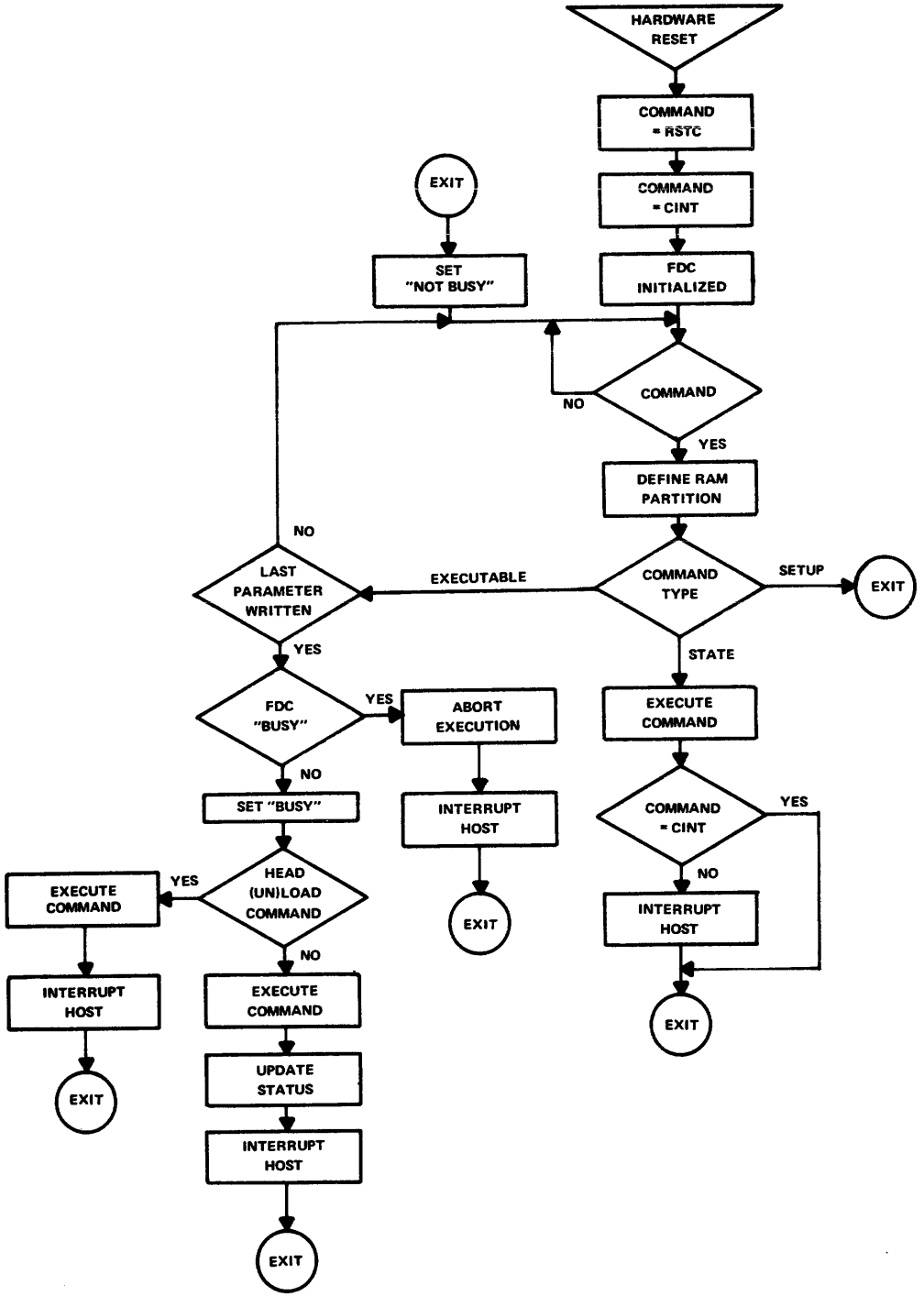


FIGURE 10 — FDC COMMAND FLOW

3.1 STATE COMMANDS

No parameters are required for these commands. The action occurs immediately after the byte is written to the command register.

3.1.1 Clear Interrupt (CINT)

	MSB D0	D1	D2	D3	D4	D5	D6	LSB D7	
CINT	0	0	0	0	X	X	X	X	COMMAND REGISTER

Following the termination of a command (either normal or error), an interrupt is given to the MPU by a low on the $\overline{INT}$ line. The CINT command byte is sent by the host microprocessor to acknowledge the interrupt and causes the $\overline{INT}$ line to return to the idle state (high).

3.1.2 Abort Execution (ABEX)

	MSB D0	D1	D2	D3	D4	D5	D6	LSB D7	
ABEX	0	0	0	1	X	X	X	X	COMMAND REGISTER

If a write operation is in progress, the FDC does the following:

1) Stops the DMA handshakes.
2) Continues writing to the end of the sector using the last byte received.
3) Writes two CRC bytes (if selected) and one FILL byte.
4) Puts $\overline{WGATE}$ high and indicates termination by pulling the interrupt output $\overline{(INT)}$ low.

If a read operation is in progress, the abort causes the Access Requests to be stopped and the diskette read halted before the interrupt line is pulled low to indicate termination.

There are no status returns from this instruction and the FDC is not left in a known state. Also, parameter registers such as track or sector counts may or may not have been updated. An ABEX command should normally be followed by a hardware $\overline{RESET}$ or a RSTC command once the $\overline{INT}$ output has gone low.

Writing any command to the command register while in the busy state will cause the current command execution to be aborted in the same manner as an ABEX command.

3.1.3 Reset Controller (RSTC)

	MSB D0	D1	D2	D3	D4	D5	D6	LSB D7	
RSTC	0	0	1	0	X	X	X	X	COMMAND REGISTER

The RSTC command byte is used to reset the FDC to a known state. The output pins are set to the following states within 10 μs (MAX):

$\overline{DSEL}$ 0/1 = 0	SIDE = 0	DIR/SIDE = 0	$\overline{HDLOAD}$ = 1
$\overline{SELECT}$ = 1	$\overline{LWCUR}$ = 1	$\overline{STEP}$ = 1	$\overline{WDATA}$/$\overline{SRST}$ = 1
$\overline{WGATE}$ = 1	$\overline{ACCRQ}$ = 1	D0-D7 = Hi-Z	$\overline{INT}$ = 0

The status register is set to hex FF(> FF), but the RAM parameters are unchanged. The $\overline{INT}$ pin is set low upon completion of this command. Note that RSTC should be used following a hardware $\overline{RESET}$ at power-up since a hardware $\overline{RESET}$, by itself, does not cause the $\overline{INT}$ output from the FDC to become active (low).

3.2 SETUP COMMANDS

The purpose of the setup command is to load the parameter registers with the format information used in the read, write, recalibrate and format commands. They allow almost any user-defined format to be used.

Note that the setup command parameters for AIDA and AFAS are different from the parameters used in a recalibration (RDAR) or format (HAFT,SOFT) command.

3.2.1 Assign ID Attributes (AIDA)

	MSB D0	D1	D2	D3	D4	D5	D6	LSB D7	
AIDA	0	0	1	1	X	X	X	X	COMMAND REGISTER

The ID parameters are selected when the two most significant bits of the command byte are zero. The register select lines, S0-S2, are then used to read or write the parameters located in the AIDA partition (00). Table 4 shows the seven parameter bytes for the AIDA command. These may be accessed in any order and at any time if the Busy bit (D0 or MSB) in the primary status register (S0-S2 = 000) is not active (low). With the exception of the byte at S0-S2 = 011, these parameters are used only for soft sector operations. For a hard sector read or write, the starting-sector-minus-one register is used to determine the number of sectors after the index hole before the read/write is started. (Note that the starting sector minus one must actually be loaded.) The AIDA parameters are differentiated in terms of soft or hard format in Table 4:

TABLE 4 — AIDA PARAMETERS (PARTITION 00)

ADDRESS			MSB		PARAMETER REGISTERS					LSB
S0 0	S1 0	S2 0	D0 0	D1 0	D2 X	D3 X	D4 X	D5 X	D6 X	D7 X
0	0	1	ID AM CLOCK (SOFT ONLY)							
0	1	0	ID AM DATA (SOFT ONLY)							
0	1	1	ID BYTE 1 (SOFT)/STARTING SECTOR-1 (HARD)							
1	0	0	ID BYTE 2 (SOFT ONLY)							
1	0	1	ID BYTE 3 (SOFT ONLY)							
1	1	0	ID BYTE 4 (SOFT ONLY)							
1	1	1	ID CRC (SOFT ONLY)	IBM MFM (SOFT ONLY)	SECTOR LOCATION (SOFT ONLY)		ID LENGTH (SOFT ONLY)			

Soft Only:

- ID Address Mark (AM) — Formed by interleaving the ID AM clock byte (a unique bit pattern that differs from normal encoding rules) with the ID AM data byte.
- Four ID bytes — These bytes are compared with the ID bytes on the disk in a soft sector read or write command to determine whether the track and sector are correct. The ID bytes may be appended by a maximum of ten additional bytes of any value.
- ID CRC = 1 — There will be a two-byte CRC after the ID which will be checked by the FDC in a read command. The CRC check includes the AM. The polynomial used is G(x) = x**16 + x**12 + x**5 + 1.
- ID CRC = 0 — No CRC checks will be done.
- IBM MFM = 1 — The Address Mark will be repeated three times in the ID field before the ID bytes occur.

- IBM MFM = 0 — There will be one Address Mark in the ID field.
- Sector location — A number from 0 to 3 indicates which ID byte contains the sector number. The sector byte is incremented after each sector transferred on multiple sector reads.
- ID length — The number of ID bytes in the ID field (max = 14). The ID length includes the number of ID bytes and Address Marks but does not include the CRC bytes.

Hard Only:

- Starting Sector-1 — The binary value of this byte is the number of sector pulses that are counted before a read or write is carried out to a hard-sectored disk. This is the only parameter in the partition that must be loaded for a hard sector operation. Note that the starting sector location for formatting hard-sectored disks is defined in Partition 10, Table 7.

3.2.2 Define Stepping Rates (DEST)

	MSB D0	D1	D2	D3	D4	D5	D6	LSB D7	
DEST	0	1	0	1	X	X	X	X	COMMAND REGISTER

The purpose of the DEST command is to set the timing parameters used by the FDC when it accesses the disk drives. If one or more of the drives requires recalibration, i.e., stepped to track 00, the same parameters may be loaded as part of the Recalibrate Drives command (RDAR) instead of implementing DEST.

There are three different drive timing parameters which are defined in the DEST partition (01), shown in Table 5:

Head stepping time — Duration of the step pulses to the head step motor. (S0-S2 = 001 for A rate, = 100 for B rate)

Head settling time — After positioning to a new track, time between the last step pulse and any further action, e.g., head load. (S0-S2 = 010 for A rate, = 101 for B rate)

Head load time — Delay from the moment the head load ($\overline{\text{HDLOAD}}$) signal becomes active (low) until the head is loaded and the read/write begins. (S0-S2 = 011 for A rate, = 110 for B rate)

The last parameter byte of Partition 01 is the rate allocation map (S0-S2 = 111). This byte assigns either A (S0-S2 = 001-011) or B (S0-S2 = 100-110) rates to each floppy drive. Refer to Section 4.1 for an initialization example. For instance, if the last byte (S0-S2 = 111) is written as 10010001, Drive 3 would be accessed using the first three head parameter rates (A) while Drives 2 and 0 would use the second three rates (B). Note that Drive 1 has no rates assigned to it and any read, write, format or recalibrate attempted on this drive will cause an error terminated with the appropriate status return. (See Status Returns, Table 10.) The same error also occurs if both sets of rates are assigned to the same drive.

The binary values loaded into the registers are twice the actual times required, giving a range of .5 to 127.5 ms and a resolution of 1/2 ms. To insure a minimum time, it is recommended that the user add 1 to twice the actual time required. For example, if a 5 ms time is desired, ↠0B ((5 X 2 + 1) = 11 = ↠0B) should be written to the register.

The head unload time is determined by the index timings of the drive used. That is, after the $\overline{\text{INT}}$ from command completion, the FDC waits four index pulses to unload the head (HDLOAD inactive high). For this reason, the $\overline{\text{INDEX}}$ pin should always be enabled.

TABLE 5 — DEST PARAMETERS (PARTITION 01)

ADDRESS			MSB		PARAMETER REGISTERS					LSB
S0	S1	S2	D0	D1	D2	D3	D4	D5	D6	D7
0	0	0	0	1	X	X	X	X	X	X
0	0	1	HEAD STEPPING TIME A (ms/2)							
0	1	0	HEAD SETTLING TIME A (ms/2)							
0	1	1	HEAD LOAD TIME A (ms/2)							
1	0	0	HEAD STEPPING TIME B (ms/2)							
1	0	1	HEAD SETTLING TIME B (ms/2)							
1	1	0	HEAD LOAD TIME B (ms/2)							
1	1	1	DRIVE 3		DRIVE 2		DRIVE 1		DRIVE 0	
			A	B	A	B	A	B	A	B

3.2.3 Assign FILL and SYNC Bytes (AFAS)

	MSB D0	D1	D2	D3	D4	D5	D6	LSB D7	
AFAS	1	1	0	0	X	X	X	X	COMMAND REGISTER

The AFAS command has the following parameters in Partition 11, as shown in Table 6:

- FILL byte — A data byte used to fill in between fields. One byte is written after the data field before $\overline{\text{WGATE}}$ is deactivated on disk writes. (S0-S2 = 001)
- SYNC byte — The SYNC field data contents that appear before any Address Mark. SYNC contents are used by the FDC to set the phase of the incoming read data. This is the first field that is written in a write operation. (S0-S2 = 010)
- Number of SYNC bytes before data field — In a read operation, this byte defines how long the FDC will look for SYNC. In a write operation, this byte defines the number of SYNC bytes written. (S0-S2 = 011)
- Track location register — The FDC uses S0-S2 = 100-111 to store the physical track location of the four system drives. These registers are zeroed during a recalibrate command (RDAR) and are updated by the internal controller as each head is stepped. The registers can be read and written to by the MPU using the AFAS command so that a new track location can be specified for a physical track on the disk, e.g., to skip bad tracks. Otherwise, these registers are not normally written to during device operation.

TABLE 6 – AFAS PARAMETERS (PARTITION 11)

ADDRESS			MSB		PARAMETER REGISTERS					LSB
S0 0	S1 0	S2 0	D0 1	D1 1	D2 X	D3 X	D4 X	D5 X	D6 X	D7 X
0	0	1	FILL BYTE							
0	1	0	SYNC BYTE							
0	1	1	NUMBER OF SYNC BYTES BEFORE DATA FIELD							
1	0	0	TRACK LOCATION REGISTER (DRIVE 0)							
1	0	1	TRACK LOCATION REGISTER (DRIVE 1)							
1	1	0	TRACK LOCATION REGISTER (DRIVE 2)							
1	1	1	TRACK LOCATION REGISTER (DRIVE 3)							

3.3 EXECUTABLE COMMANDS

Executable commands are those commands which cause the TMS9909 to interact with one or more of the diskette drives. Although writing the command byte code into the command register selects the instruction to be carried out and also determines the parameter partition, it does not initiate execution. The required action begins only after the last parameter byte required by the particular command is written to the appropriate register. If the command is being executed for the first time, then all pertinent parameters must be written (HDUN and HDLD require no parameters) before execution. This may be done in any order with the provision that the last parameter register to be loaded must be S0-S2 = 111 for read, write or recalibrate commands and S0-S2 = 100 for formatting commands. If the parameters have already been set up (from a setup command or from the last execution), then only the command byte (S0-S2 = 000) and the last required parameter byte need to be loaded in order to initiate the disk access.

Note that if the host microprocessor needs to read any of the parameters in these partitions, the command byte may be written and the registers read without actually executing the command. However, the FDC must not be busy during this operation. If the FDC is busy and a write attempt is made, the command currently being executed will be aborted.

Executable commands return a status byte to indicate the successful completion of the instruction or the error condition which prevented its complete execution.

3.3.1 Recalibrate, Head (Un)Load Commands

3.3.1.1 Recalibrate Drives Assign Rates (RDAR)

	MSB D0	D1	D2	D3	D4	D5	D6	LSB D7	
RDAR	0	1	0	0	DD3	DD2	DD1	DD0	COMMAND REGISTER

The RDAR command has two functions:

1) RDAR selects Partition 01 (Table 5) for the necessary head timing parameters. These parameters may also be set using the DEST command and are fully described in the DEST command section.

2) Upon execution of RDAR, the FDC steps the head of each drive selected to track 00 and zeros the track location register in Partition 11 (Table 6, S0-S2 = 100-111) for the relevant drive.

If the head timing parameters have been previously set up by a DEST command, only the command byte and the last parameter byte need to be loaded for execution of RDAR command. Upon execution, the FDC first looks at the four least significant bits in the command register (shown as D4-D7 above) to determine which drive(s) is (are) to be recalibrated, i.e., if any of the bits have been set to one. (DD3 represents Drive 3, DD2 represents Drive 2, etc.) The following operations are then performed by the FDC:

1) The $\overline{\text{SELECT}}$ line is set high to deselect all drives while the outputs listed below are deactivated:

DIR/SIDE	–	LOW
SIDE	–	LOW
$\overline{\text{LWCUR}}$	–	HIGH
$\overline{\text{STEP}}$	–	HIGH
$\overline{\text{HDLOAD}}$	–	HIGH
$\overline{\text{WDATA/SRST}}$	–	HIGH
$\overline{\text{WGATE}}$	–	HIGH

2) The DSEL0 and DSEL1 lines indicate to the MPU which diskette drive is to be recalibrated:

00	=	Drive 0
01	=	Drive 1
10	=	Drive 2
11	=	Drive 3

3) The $\overline{\text{SELECT}}$ line is then set low (active), and the FDC waits for up to 1.25 seconds for the $\overline{\text{DRVRDY}}$ line to be pulled low in response. If the drive does not become ready, the command is ended with the status return indicating that Drive XX (XX = 00 = Drive 0, XX = 01 = Drive 1, XX = 10 = Drive 2, XX = 11 = Drive 3) is not ready after 1.25 seconds.

	MSB D0	D1	D2	D3	D4	D5	D6	LSB D7	
RDAR	–	–	0	0	0	0	X	X	STATUS REGISTER

Note that if the desired drive is already selected, the above procedure is skipped and the FDC assumes that the drive is still ready. (DRVRDY is not sampled.)

If the drive selected has no A or B rates defined or both A and B rates selected, the command is stopped with the status return indicating that rates are not defined for Drive XX (XX = 00 = Drive 0, XX = 01 = Drive 1, etc).

	MSB D0	D1	D2	D3	D4	D5	D6	LSB D7	
RDAR	–	–	0	0	0	1	X	X	STATUS REGISTER

4) Once selected, the FDC steps the disk head three tracks in towards the center. If $\overline{\text{TCK00}}$ is low, the head is positioned over track 00. If $\overline{\text{TCK00}}$ is high, the drive is stepped out (away from the center) until $\overline{\text{TCK00}}$ goes low. The DIR/SIDE output functions as DIR when stepping the disk head. DIR defines the direction of stepping, i.e., high = to the center, low = away from the center. The $\overline{\text{STEP}}$ output goes low for every step pulse. The step pulse train has a normal duty cycle of 50 percent with the period equal to the applicable head step time (A or B rate). If the $\overline{\text{TCK00}}$ input is still high after 255 steps, the command is ended with the status return indicating track 00 was not reached for the drive in question.

	MSB D0	D1	D2	D3	D4	D5	D6	LSB D7	
RDAR	–	–	0	0	1	0	X	X	STATUS REGISTER

If track 00 is found, the internal track location register (Partition 11, S0-S2 = 100-111) for the drive is reset to hex 00(>00). The host MPU may then access this parameter by an AFAS command.

5) Following the initialization of the first drive, the FDC works sequentially from Drive 0 to Drive 3 testing for another drive to be recalibrated. If an error occurs, all recalibration will terminate and the status will be reported. When all the required drives have been successfully recalibrated, the $\overline{INT}$ output is pulled low to interrupt the MPU thereby signaling completion of the command.

NOTE

The new physical track register (parameter byte 4, Partition 10) is set to hex 00 or 03 (>00 or >03) by the RDAR command even if no drives are recalibrated. If an error occurs while recalibrating a particular drive, then no further drives will be recalibrated regardless of the command register contents.

Last Required Parameter for Execution : Partition 01, S0-S2 = 111.

3.3.1.2 Head Unload Command (HDUN)

	MSB D0	D1	D2	D3	D4	D5	D6	LSB D7	
HDUN	0	1	1	0	X	X	X	X	COMMAND REGISTER

The HDUN command allows the disk head to be raised at any time earlier than the FDC would normally raise it, i.e., after the four index pulses that follow the end of the previous command. There are two operating modes:

1) The drive is already selected when the HDUN command is sent. The FDC sets $\overline{HDLOAD}$ high (lifting the read/write head from the diskette surface of the selected drive) and stops the command currently under execution. The drive then remains selected for four index pulses.

2) No drive is selected when the HDUN command is sent. The FDC selects the drive implemented by the previous command. Again, the drive remains selected for four index pulses.

The HDUN command is a single-byte immediately-executable instruction (no parameter bytes). Writing the command byte >6X to the command register causes the FDC to go busy. Information regarding which drive's read/write head is to be unloaded is decoded from the DSEL1, DSEL0 and SIDE outputs set up by the previous command. This command typically takes 20 microseconds to execute.

Last Required Parameter for Execution: No parameters required.

3.3.1.3 Head Load Command (HDLD)

	MSB D0	D1	D2	D3	D4	D5	D6	LSB D7	
HDUN	0	1	1	1	X	X	X	X	COMMAND REGISTER

The HDLD command allows independent loading of a diskette's head(s). Writing the command byte >7X to the command register causes the FDC to go busy and set $\overline{HDLOAD}$ low on the currently selected drive. HDLD is a single-byte, immediately executable command (no parameter bytes). If no new commands are sent to the FDC within four index pulses after the execution of this command, the disk head is raised and the drive deselected. Head calibration could represent an appropriate application of the HDLD command. This command typically takes 20 microseconds to execute.

Last Required Parameter for Execution: No parameters required.

3.3.2 Diskette Read, Write and Format Parameters

There are seven executable commands that read data from and write data to a selected diskette: HARD, SORD, UTRD, HAWR, SOWR, HAFT, SOFT). Four of these commands (HARD, SORD, HAWR, SOWR) seek a track and a sector and read or write data in a user-defined format. Two commands (HAFT, SOFT) are used to format a diskette with a series of Address Marks, SYNC bytes, etc., specified by the user. Lastly, the UTRD command seeks a starting point (track, first data AM past the index marker), then reads bytes and transfers them to the memory of the host MPU.

These read, write and format commands have a common set of seven parameter bytes located in the parameter section of Partition 10. Since most of the parameters have the same or a similar use during each of the commands, they do not all have to be loaded at each execution. For example, a read check can be carried out after a write by writing only the command byte, the number of records to transfer, and the last parameter. The last parameter in Partition 10 required for execution of read and write commands is S0-S2 = 111. For format commands, the last parameter required for execution in Partition 10 is S0-S2 = 100. Refer to Table 7 for a map of the read/write/format parameters in Partition 10.

TABLE 7 – READ/WRITE/FORMAT PARAMETERS (PARTITION 10)

ADDRESS			MSB		PARAMETER REGISTERS					LSB
S0	S1	S2	D0	D1	D2	D3	D4	D5	D6	D7
0	0	0	1	0	X	X	X	5	0	0
0	0	1	ENCODE		XFER RATE		RECORD LENGTH (MSN)			
0	1	0	RECORD LENGTH (LSB)/STARTING SECTOR-1							
0	1	1	$\overline{\text{LWCUR}}$	PRECOM	NUMBER OF RECORDS TO XFER					
1	0	0	NEW PHYSICAL TRACK							
1	0	1	DATA AM CLOCK BYTE							
1	1	0	DATA AM DATA BYTE							
1	1	1	DATA IBM MFM	XFER DATA	DATA CRC	SECTOR TO DATA GAP LENGTH				

NOTE: The Recalibrate Drives command does not use any of the bytes in Partition 10.

ADDRESS			READ/WRITE/FORMAT PARAMETER DESCRIPTION (PARTITION 10)
S0	S1	S2	
0	0	1	ENCODE – Selects the encoding method for the diskette data. Note that a "bit cell" is defined as two consecutive bits of information with the leading bit always being a clock bit and the second bit being a data bit. D0 D1 0 0 ... Not used. 0 1 ... FM encode rules: 1) Write data bits at the center of the bit cell, and 2) write clock bits at the beginning of the bit cell. 1 0 ... MFM encoding rules: 1) Write data bits at the center of the bit cell, and 2) write clock bits at the beginning of the bit cell if: a) no data has been written in the previous bit cell, and b) no data will be written in the present bit cell.

ADDRESS			READ/WRITE/FORMAT PARAMETER DESCRIPTION (PARTITION 10) (Continued)
S0 0	S1 0	S1 1	1 1 ... M^2FM encode rules: 1) Write data bits at the center of the bit cell, and 2) write clock bits at the beginning of the bit cell if: a) no data or clock bit has been written in the previous bit cell, and b) no data bit will be written in the present bit cell. XFER RATE – The rate of the diskette data transfer: D2 D3 0 0 ..... 125k Bits/Sec 15 5/8k Bytes/Sec 0 1 ..... 125k Bits/Sec 15 5/8k Bytes/Sec 1 0 ..... 250k Bits/Sec 31 1/4k Bytes/Sec 1 1 ..... 500k Bits/Sec 65 1/2k Bytes/Sec RECORD LENGTH (MSN) – Data field + AM length may be up to 4095 bytes.
0	1	0	RECORD LENGTH (LSB)/STARTING SECTOR-1 – For hard sector formatting, the parameter represents the starting sector-1 where track formatting is to begin.
0	1	1	$\overline{\text{LWCUR BIT}}$ – Low write current: D0 0 ..... $\overline{\text{LWCUR}}$/DDEN output goes low during a write operation. 1 ..... $\overline{\text{LWCUR}}$/DDEN output stays high during a write operation. PRECOM BIT – Precompensation select: D1 PRECOM = 0...No write precompensation. PRECOM = 1...Write precompensation selected. NUMBER OF RECORDS TO TRANSFER – The number of successive records to transfer to the host or diskette. This parameter must be up-dated between every command execution: (D2-D7) = 1 .....Single sector transfer. = Number greater than one ... Multi-sector transfer.
1	0	0	NEW PHYSICAL TRACK – Target data is on this track.
1	1	1	DATA FIELD INFORMATION: DATA IBM MFM BIT D0 IBM MFM = 0 ... Use 1 AM in the data field. IBM MFM = 1 ... Use 3 AMs in the data field. XFER DATA BIT D1 XFER DATA = 0...FDC will do seek and quit execution with no $\overline{\text{HDLOAD}}$ output. XFER DATA = 1...FDC will seek, then read, write, or format.

ADDRESS			READ/WRITE/FORMAT PARAMETER DESCRIPTION (PARTITION 10) (Continued)
S0	S1	S1	
0	0	1	DATA CRC BIT D2 CRC = 0...CRC is not appended or checked at the end of the data field. CRC = 1...CRC is appended or checked at the end of the data field. SECTOR-TO-DATA GAP LENGTH The number of bytes between the end of the ID field (or the high-to-low transition of the $\overline{\text{SECTOR}}$ input for hard-sectored disks) and the start of the SYNC bytes for the data field (D3-D7).

3.3.3 Track Seek Operation

All the read, write and format operations share a common procedure for locating the desired track. This is described in detail below.

1) The $\overline{\text{SELECT}}$ line is set high to deselect all drives, and the following outputs are set by the TMS9909:

DIR/SIDE	– LOW	$\overline{\text{LWCUR}}$	– HIGH	$\overline{\text{WGATE}}$	– HIGH
SIDE	– LOW	$\overline{\text{STEP}}$	– HIGH	$\overline{\text{WDATA}}/\overline{\text{SRST}}$	– HIGH
$\overline{\text{HDLOAD}}$	– HIGH				

2) The DSEL0 and DSEL1 lines set up the two least significant bits (D6,D7) of the command register in Partition 10 as the address for the appropriate diskette drive to be read, written, or formatted:

	D6	D7	
DD =	0	0	= Drive 0
	0	1	= Drive 1
	1	0	= Drive 2
	1	1	= Drive 3

Refer to Table 1 for illustration.

3) The $\overline{\text{SELECT}}$ line is then set low and the FDC waits up to 1.25 seconds for the $\overline{\text{DRVRDY}}$ line to be pulled low in response. If the drive does not become ready, the command is ended with the status return indicating that the drive is not ready after 1.25 seconds.

STATUS REGISTER

	MSB D0	D1	D2	D3	D4	D5	D6	LSB D7
READ	–	–	1	0	0	0	X	X
WRITE	–	–	1	1	0	0	X	X
FORMAT	–	–	0	1	0	0	X	X

Note that if the desired drive is already selected, the above procedure is skipped and the FDC assumes that the drive is still ready. ($\overline{\text{DRVRDY}}$ is not sampled.)

4) When the drive has been selected and is ready, a check is made to ensure that a set of stepping rates has been assigned, i.e., the FDC looks at the memory map in Partition 01 for the DEST (RDAR) parameters. If neither or both the A or B bits are set for the selected drive, the command is stopped with a status return indicating that the rates are not defined.

STATUS REGISTER

	MSB D0	D1	D2	D3	D4	D5	D6	LSB D7
READ	–	–	1	0	0	1	X	X
WRITE	–	–	1	1	0	1	X	X
FORMAT	–	–	0	1	0	1	X	X

If the rates are defined, the $\overline{\text{LWCUR}}$/DDEN output is set high for double density (MFM or M^{2}FM) or low for single density (FM) encoding. The track seek preliminaries are now complete.

5) The FDC compares the new physical track parameter in Partition 10 with its own record of the disk head position, i.e., the track location register in Partition 11 (S0-S2 = 100-111). If they are not equal, the DIR/SIDE output is set low to step outwards (new track parameter less than current track parameter) or high to step inwards (new track parameter greater than current track parameter), and the $\overline{\text{STEP}}$ output is pulsed low. $\overline{\text{HDLOAD}}$ remains unaffected by the stepping. The frequency of the step pulses is set by the stepping time in Partition 01 and has a 50 percent duty cycle. The track location register in Partition 11 is updated and compared with the desired track during the high portion of each step pulse until they are equal.

After each step and before again comparing the contents of the track location register in Partition 11 with the new physical track parameter in Partition 10, the $\overline{\text{TCK00}}$ input is tested to see if it is consistent with the current track location. An error is detected if:

a) $\overline{\text{TCK00}}$ is high and the track location register equals zero.

b) $\overline{\text{TCK00}}$ is low and the track location register is not equal to zero.

If an error occurs, the command ends with a status return indicating that $\overline{\text{TCK00}}$ is not equal to the disk track on the drive.

	MSB D0	D1	D2	D3	D4	D5	D6	LSB D7	
READ, WRITE, FORMAT	–	–	0	0	1	1	X	X	STATUS REGISTER

6) After the completion of the head seek and if the FDC has stepped any tracks, the FDC delays for the period specified in the head settling time parameter. If the Xfer Data bit in Partition 10, parameter byte 7, is low, the command stops and the Busy bit in the status register is set high (1 = Not Busy). If the XFER Data bit is set to one and the head is currently unloaded, the $\overline{\text{HDLOAD}}$ output is set low and the FDC delays for the head load time specified by either the A or B parameter in Partition 01.

7) If a track seek operation is all that is required, the procedure is as follows:

   1) Load the new physical track register (Partition 10, parameter byte 4) with the desired physical track.

   2) Set the Xfer Data bit in the data field information register (Partition 10, parameter byte 7) low for no data transfer.

Generally, the track seek operation is part of a read/write/format command and is transparent to the user.

3.3.4 Read, Write and Format Commands

Now that the "drive select" and "track seek" operations utilized in the execution of read, write, or format commands have been described, it is appropriate to discuss each command individually. What follows is a brief description of each command's requirements for successful execution along with the status returns for the most probable errors.

(The 'S' in the command field represents the side of the media (0 or 1), while 'DD' represents the code for the Drive number, i.e., 00 is Drive 0, 01 is Drive 1, etc.)

NOTE

With the exception of the data field information parameter byte (Partition 10, S0-S2 = 111) for read/write commands and the new physical track parameter byte (Partition 10, S0-S2 = 100) for format commands, the parameters for read/write/format commands may be loaded in any order. If these parameters have been previously set up, then the read/write/format command may be initiated by writing the command byte (DBIN = 0, S0-S2 = 000) and the last required parameter byte for execution.

3.3.4.1 Hard Sector Read (HARD)

	MSB D0	D1	D2	D3	D4	D5	D6	LSB D7	
HARD	1	0	0	0	0	S	D	D	COMMAND REGISTER

The HARD command will step to the desired track and read the sector of data that follows the correct sector hole. This data may be transferred to the host by means of DMA. The two CRC bytes (if present) will be checked and their correctness (or otherwise) indicated in the status register. Optionally, the user may specify a multi-sector transfer: the FDC will locate the next sector hole and repeat the process.

For HARD as well as for HAWR, the starting-1 parameter (Partition 00, parameter byte 3) defines the first sector to be transferred. For example, to transfer data after sector 1, code this byte as 00.

If there are two few sector pulses between two index pulses, the FDC stops the command and loads the status register with the error return indicating that the hard sector was not found.

	MSB D0	D1	D2	D3	D4	D5	D6	LSB D7	
HARD	–	–	1	0	1	0	0	0	STATUS REGISTER

Last Required Parameter for Execution: Partition 10, S0-S2 = 111.

3.3.4.2 Hard Sector Write (HAWR)

	MSB D0	D1	D2	D3	D4	D5	D6	LSB D7	
HAWR	1	0	0	1	0	S	D	D	COMMAND REGISTER

The HAWR command will step to the desired track and write data to the sector following the correct sector hole. This data may be transferred to the diskette by means of DMA. The FDC will begin writing after 'timing-out' for the sector, i.e., after the sector-to-data gap length defined by parameter byte 7, Partition 10. The two CRC bytes (if selected) will be generated by the TMS9909 and written to the diskette after the data field. The last byte to be written will be the FILL byte specified in parameter byte 1, Partition 11. Optionally, the user may specify a multi-sector transfer: the FDC will locate the next sector hole and repeat the process.

For HAWR as well as for HARD, the starting sector-1 parameter (Partition 00, parameter byte 3) defines the first sector to be transferred. For example, to transfer data after sector 1, code this byte as 00.

If there are too few sector pulses between two index pulses, the FDC stops the command and loads the status register with the error return that indicates the hard sector was not found.

	MSB D0	D1	D2	D3	D4	D5	D6	LSB D7	
HAWR	–	–	1	1	1	0	0	0	STATUS REGISTER

Last Required Parameter for Execution: Partition 10, S0-S2 = 111.

3.3.4.3 Unformatted Track Read (UTRD)

	MSB D0	D1	D2	D3	D4	D5	D6	LSB D7	
UTRD	1	0	1	1	1	S	D	D	COMMAND REGISTER

The UTRD command will step to the desired track and read that track for the first occurrence of the SYNC/Data Address Mark combination following the index hole. The FDC will then read the number of bytes defined by the record length parameter in Partition 10 (S0-S2 = 001-010). The Address Mark bytes for UTRD are also defined in Partition 10 (S0-S2 = 101-110). The SYNC bytes for all commands are located in Partition 11.

Last Required Parameter for Execution: Partition 10, S0-S2 = 111.

3.3.4.4 Soft Sector Read (SORD)

	MSB D0	D1	D2	D3	D4	D5	D6	LSB D7	
SORD	1	0	0	0	1	S	D	D	COMMAND REGISTER

The SORD command will step to the desired track and read the sector of data that follows the specified ID field. This data may be transferred to the host by means of DMA. The two CRC bytes (if present) will be checked against the calculated CRC value and the result (correct or otherwise) indicated in the status register. Optionally, the user may specify a multi-sector transfer: the FDC will locate the next ID field and repeat the process.

Last Required Parameter for Execution: Partition 10, S0-S2 = 111.

3.3.4.5 *Soft Sector Write (SOWR)*

	MSB D0	D1	D2	D3	D4	D5	D6	LSB D7	
SOWR	1	0	0	1	1	S	D	D	COMMAND REGISTER

The SOWR command will step to the desired track and write data to the sector following the specified ID field. This data may be transferred to the diskette by means of DMA. The two CRC bytes (if selected) will be generated by the TMS9909 and written to the diskette after the data field. The last byte to be written will be the FILL byte specified in Partition 11, parameter byte 1. Optionally, the user may specify a multi-sector transfer: the FDC will locate the next ID field and repeat the process.

NOTE

$\overline{\text{INDEX}}$ must not become active during a SOWR in order to guarantee proper execution of this command. If $\overline{\text{INDEX}}$ does become active, the FDC will abort the operation and write the last byte transferred to the end of the specified field.

Last Required Parameter for Execution: Partition 10, S0-S2 = 111.

3.3.4.6 *Notes on UTRD, SORD, and SOWR Commands*

Three commands share a common algorithm for locating the first AM (UTRD) or ID field (SORD, SORW). For UTRD, the AM is the data AM located in parameter bytes 5 and 6 of Partition 10. The SORD and SOWR commands use the ID AM in parameter bytes 1 and 2 of Partition 00 when finding the ID field. Three AMs are sought if either the Data IBM MFM bit (UTRD) in the data field information byte (Partition 10, S0-S2 = 111) or the ID IBM MFM bit (SORD, SOWR) in the ID field information byte (Partition 00, S0-S2 = 111) is set.

When the disk head is properly loaded, the FDC checks the incoming RDATA against the SYNC byte in parameter byte 2 of Partition 11. The FDC looks for a SYNC byte containing a valid clock and data pattern, i.e., 16 consecutive correct bits. SYNC must be repeated every second "bit cell" (a 'bit cell' is defined as two consecutive bits of information with the leading bit always being a clock bit and the second bit always being a data bit). A list of valid SYNC bytes is given in Table 8.

TABLE 8 – VALID SYNC BYTES

	DATA	CLOCK	DATA	CLOCK	DATA	CLOCK	DATA	CLOCK
FM	>FF	>FF	>00	>FF	>AA	>FF	>55	>FF
MFM	>FF	>00	>00	>FF	>AA	>00	>55	>00
M²FM	>FF	>00	>00	>AA >55	>AA	>00	>55	>00

NOTE: > = hex

The FDC will generate the correct clock pattern for comparison internally. Note that for M²FM formats with hex > 00 as the SYNC pattern, the clock pattern may be either > AA or > 55.

When a SYNC byte is found, the FDC locks onto SYNC until a different incoming pattern is detected. This usually occurs when an AM is encountered. The following applies for AM detection:

1) In a UTRD command, DMA transfers start as described below for the read and write commands.

2) In a SORD or SORW command, the FDC checks the ID bytes in Partition 00 and the CRC bytes, if programmed, against the incoming RDATA.

If, after encountering a different pattern, the AM or ID bytes do not match the ones specified in the RAM partition, the FDC returns to scanning the disk for another SYNC byte.

If the FDC detects an error, the command is stopped. The following returns are then loaded into the status register:

1) If no SYNC bytes are found between two index pulses, the error return indicates that ID SYNC bytes were not found..

STATUS REGISTER

	MSB D0	D1	D2	D3	D4	D5	D6	LSB D7
SORD	–	–	1	0	1	0	0	1
	D0	D1	D2	D3	D4	D5	D6	D7
SOWR	–	–	1	1	1	0	0	1

2) If no ID AM is found after any of the SYNC fields, the error return indicates that the ID AM was not found.

STATUS REGISTER

	MSB D0	D1	D2	D3	D4	D5	D6	LSB D7
SORD	–	–	1	0	1	0	1	0
	D0	D1	D2	D3	D4	D5	D6	D7
SOWR	–	–	1	1	1	0	1	0

3) If there is a CRC error after the current ID AM and ID bytes, the error return indicates an ID CRC error.

STATUS REGISTER

	MSB D0	D1	D2	D3	D4	D5	D6	LSB D7
SORD	–	–	1	0	1	0	1	1
	D0	D1	D2	D3	D4	D5	D6	D7
SOWR	–	–	1	1	1	0	1	1

4) If the correct ID bytes are not found after the ID AM, the following error returns are loaded into the status register:

STATUS REGISTER

	MSB D0	D1	D2	D3	D4	D5	D6	LSB D7
SORD	–	–	1	0	1	1	0	0
	D0	D1	D2	D3	D4	D5	D6	D7
SOWR	–	–	1	1	1	1	0	0

Once the correct ID field has been found, the FDC prepares to transfer data. All read and write commands share a common algorithm for transferring data. The AM referred to below is the data AM in parameter bytes 5 and 6 of Partition 10. If the data IBM MFM bit is set, the AM is three bytes long. The following applies for read and write operations:

READ

After the ID field or sector hole and the sector-to-data gap (data field information, Partition 10, S0-S2 = 111), the FDC looks for the data SYNC field. Following the data SYNC field and the data AM, data may be send from the disk to the host MPU using DMA. The SYNC field length parameter (Partition 11, S0-S2=011) is used by the FDC to look for a specified number of data SYNC bytes preceding the data field AM bytes. If the data SYNC bytes are not found within this time period or if the data field AM bytes are not found, the read command is terminated. The following error return is then loaded into the status register:

	MSB D0	D1	D2	D3	D4	D5	D6	LSB D7	
READ	–	–	1	0	1	1	0	1	STATUS REGISTER

After a field has been read, the $\overline{\text{ACCRQ}}$ signals from the FDC to the DMAC stop, and two CRC bytes (if CRC = 1 in the data field information byte: Partition 10, S0-S2 = 111) are checked. If there is a CRC error, the read command is terminated. The following error return is then loaded into the status register.

	MSB D0	D1	D2	D3	D4	D5	D6	LSB D7	
READ	–	–	1	0	1	1	1	1	STATUS REGISTER

WRITE

For a write operation, the FDC puts the $\overline{\text{LWCUR}}$ bit (Partition 10, parameter byte 3) onto the $\overline{\text{LWCUR}}$/DDEN output. If the $\overline{\text{WTPROT}}$ input is low, the write command stops with the following status return:

	MSB D0	D1	D2	D3	D4	D5	D6	LSB D7	
WRITE	–	–	1	1	1	1	0	1	STATUS REGISTER

The update write starts at the beginning of the data field with the SYNC bytes (the number of SYNC bytes written is defined by the SYNC field length parameter: Partition 11, S0-S2 = 011), and then writes the AM and data bytes. The data bytes are requested by the FDC, singly, at the rate they are written to the disk.

With all read and write commands, the FDC uses the record length parameter (Partition 10, S0-S2 = 001-010) to control the $\overline{\text{ACCRQ}}$/$\overline{\text{ACCGR}}$ (DMA) sequence. At the end of the field, the $\overline{\text{ACCRQ}}$ signals stop and two CRC bytes are written or checked (if CRC = 1 in the data field information byte: Partition 10, S0-S2 111).

If a partial sector read or write is executed, or, if a timing problem occurs such that $\overline{\text{ACCRQ}}$ is not answered in time by an $\overline{\text{ACCGR}}$, the FDC will do the following:

1) Stop issuing $\overline{\text{ACCRQ}}$ signals.
2) Set the Handshake Abort bit in the status register low.
3) Continue reading to the end of the field or writing the last byte received to the end of the sector.
4) Write two CRC bytes or check the two CRC bytes.
5) For a write, write one FILL byte to the disk and put $\overline{\text{WGATE}}$ high.
6) Stop the command and, if there was no CRC error, load the status register with the data overflow (read)/ underflow (write) status return:

STATUS REGISTER

	MSB D0	D1	D2	D3	D4	D5	D6	LSB D7
READ	–	0	1	0	1	1	1	0
	D0	D1	D2	D3	D4	D5	D6	D7
WRITE	–	0	1	1	1	1	1	0

3.3.4.7 Hard Sector Format Track (HAFT)

	MSB D0	D1	D2	D3	D4	D5	D6	LSB D7	
HAFT	1	0	1	0	0	S	D	D	COMMAND REGISTER

The HAFT command will step to the desired track and write on the diskette from the desired sector hole to the next sector hole. Information on gap bytes, SYNC bytes, AM bytes and data bytes may be sent to the TMS9909 by means of a DMAC. These bytes are NOT picked up from the FDC internal RAM. Two CRC bytes (if specified) will be written following each field. The HAFT command is used to initialize a hard-sectored diskette by formatting each sector from sector hole to sector hole and is not defined for multi-sector transfers. The DMA sequence for a hard sector format is the same as for a soft sector format and is described in Section 3.3.4.9.

The first four parameter bytes of Partition 10 are required for the execution of the HAFT command.

Last Required Parameter for Execution: Partition 10, S0-S2 = 100.

3.3.4.8 Soft Sector Format Track (SOFT)

	MSB D0	D1	D2	D3	D4	D5	D6	LSB D7	
SOFT	1	0	1	0	1	S	D	D	COMMAND REGISTER

The SOFT command will step to the desired track and write the whole track from index pulse to index pulse. Information on gap bytes, AM bytes and data bytes may be sent to the TMS9909 by means of a DMA transfer. The DMA sequence for a soft sector format is the same as for a hard sector format and is described in Section 3.3.4.9.

The first four parameter bytes of Partition 10 are required for the execution of the SOFT command.

Last Required Parameter for Execution: Partition 10, S0-S2 = 100.

3.3.4.9 Format Command DMA Sequence

The hard and soft sector formats work in a similar manner. After the disk head is properly loaded (and, for a hard-sectored disk, the starting sector-1 found), the FDC puts the $\overline{\text{ACCRQ}}$ output low. The DMAC must respond with five bytes defining the first field to be formatted (generally a gap). Subsequent fields are then requested for DMA transfer. Table 9 illustrates the DMA handshake sequence.

TABLE 9 – FORMAT COMMAND DMA PARAMETERS*

BYTE NO.	MSB D0	D1	D2	D3	D4	D5	D6	D7 LSB
1	CRC	FILL	IBM MFM	X X	FIELD LENGTH MS 4 BITS			
2	FIELD LENGTH LS BYTE (LSB)							
3	CLOCK PATTERN OF ADDRESS MARK							
4	DATA PATTERN OF ADDRESS MARK							
5	DATA BYTE							

*Sent to the FDC in response to $\overline{\text{ACCRQ}}$.

Each field has the following options:

1) One Address Mark is written at the start if IBM MFM=0. Three Address Marks are written at the start if IBM MFM=1.

2) A data byte that is written for the duration of the field if the FILL bit = 1. If the FILL bit = 0, no data bytes are written.

3) A two-byte CRC is written at the end of the field if the CRC bit = 1. If the CRC bit = 0, no CRC bytes are written.

The field length includes the AM and data bytes but excludes the CRC bytes. For fields with repeated bytes, e.g., gaps, SYNC, these five bytes fully define the field when the following conditions are met: the FILL bit is set high; the data AM byte is set equal to the data byte, and the clock AM obeys the normal encoding rules, e.g., =>FF in an FM format.

For fields in which every data byte is different, e.g., ID field, the FILL bit is set low. As soon as the FDC begins writing the AM, it also sets $\overline{\text{ACCRQ}}$ low. The DMAC must then respond with the next byte. These single-byte DMA requests continue for the length of the field. Two CRC bytes will be written at the end of the field if CRC = 1.

As soon as the FDC begins writing a field (and all the DMA bytes defining it have been sent), the $\overline{\text{ACCRQ}}$ output will go low to request the next block of five bytes for the following field.

After the FDC has received the five bytes of format data, it will begin formatting when the diskette drive encounters an index pulse (soft-sectored disks) or a sector pulse (hard-sectored disks). The formatting will continue until the next index or sector pulse is encountered. Refer to Section 4 for more information regarding DMA format.

3.4 STATUS RETURNS

The host system may read the status from the FDC by addressing the appropriate register. With DBIN=1 and S0-S2 000, the host may read the primary status register. This register tells the host whether the FDC is currently busy and, if not, whether the previous command was successfully completed. If the previous command did not execute successfully, comprehensive information about the error is provided in encoded form by the status register.

Additional information concerning the error is available to the host by reading any of the parameter registers, some of which are updated during execution of a command. To read a parameter register, a command byte pointing to the correct partition must be written (DBIN=0) to the command register at address S0-S2=000. Following this, the parameter registers may be addressed and read.

3.4.1 Status Return Listings

The status return is divided into three parts:

1) Bit 0 (MSB=D0) — Busy bit (0 = Busy, 1 = Not Busy)

2) Bit 1 (D1) — Handshake Abort bit (0 = Abort)

3) Bits 2-7 (D2-D7) — Encoded status return

The sequence in which these status returns are set is as follows:

1) Handshake Abort bit is set as soon as the error condition is detected.

2) The encoded status is returned.

3) The Busy bit goes high, i.e., Not Busy.

TABLE 10 — STATUS RETURN CODES

CODE BITS D2 - D7	DESCRIPTION	AFFECTED COMMANDS
00	Drive 0 not RDY after 1.25 S	Recalibrate Drives Command (RDAR)
01	Drive 1 not RDY after 1.25 S	
02	Drive 2 not RDY after 1.25 S	
03	Drive 3 not RDY after 1.25 S	
04	Rates not defined for DRV 0	
05	Rates not defined for DRV 1	
06	Rates not defined for DRV 2	
07	Rates not defined for DRV 3	
08	TRK 00 not reached on DRV 0	
09	TRK 00 not reached on DRV 1	
0A	TRK 00 not reached on DRV 2	
0B	TRK 00 not reached on DRV 3	
0C	TRK 00 not equal to PTRACK 0	All commands
0D	TRK 00 not equal to PTRACK 1	
0E	TRK 00 not equal to PTRACK 2	
0F	TRK 00 not equal to PTRACK 3	
10	Drive 0 not RDY after 1.25 S	Format Track Commands (HAFT, SOFT)
11	Drive 1 not RDY after 1.25 S	
12	Drive 2 not RDY after 1.25 S	
13	Drive 3 not RDY after 1.25 S	
14	Rates not defined for DRV 0	
15	Rates not defined for DRV 1	
16	Rates not defined for DRV 2	
17	Rates not defined for DRV 3	
18	Requested sector not found	
19	Not used	
1A	Not used	
1B	Not used	
1C	Not used	
1D	Diskette write-protected	
1E	Not used	
1F	Not used	

TABLE 10 — STATUS RETURN CODES (Continued)

CODE BITS D2 - D7	DESCRIPTION	AFFECTED COMMANDS
20	Drive 0 not RDY after 1.25 S	Read Data Commands (HARD, SORD, UTRD)
21	Drive 1 not RDY after 1.25 S	
22	Drive 2 not RDY after 1.25 S	
23	Drive 3 not RDY after 1.25 S	
24	Rates not defined for DRV 0	
25	Rates not defined for DRV 1	
26	Rates not defined for DRV 2	
27	Rates not defined for DRV 3	
28	Hard sector not found	
29	ID SYNC bytes not found	
2A	ID Address Mark not found	
2B	ID CRC error	
2C	ID bytes not found	
2D	Data SYNC or AM not found	
2E	Data overflow error	
2F	Data CRC error	
30	Drive 0 not RDY after 1.25 S	Write Data Commands (HAWR, SOWR)
31	Drive 1 not RDY after 1.25 S	
32	Drive 2 not RDY after 1.25 S	
33	Drive 3 not RDY after 1.25 S	
34	Rates not defined for DRV 0	
35	Rates not defined for DRV 1	
36	Rates not defined for DRV 2	
37	Rates not defined for DRV 3	
38	Hard sector not found	
39	ID SYNC bytes not found	
3A	ID Address Mark not found	
3B	ID CRC error	
3C	ID bytes not found	
3D	Diskette write-protected	
3E	Data underflow error	
3F	Data underflow error	Format Track Commands (HAFT, SOFT)

Termination of the present command is given by the Busy bit (bit 0 of the status register) going high (Not Busy). Successful termination will result in a status return of >FF. Other values indicate an error of some kind. The status register will be set at >7F at the start of the next executable command.

4. TMS9909 FDC APPLICATIONS

The TMS9909 Floppy Disk Controller may be used to lower the cost and complexity of virtually any flexible disk system. Its two main modes of operation are the stand-alone mode and as a dedicated microprocessor. In the stand-alone mode, the TMS9909 completely controls the disk interface so that time and software overhead demands upon the MPU are minimized. State, setup and executable commands are issued from the MPU while data transfers are handled by a DMAC. The MPU may then be used for other computational, control, or I/O task, thereby maximizing throughput.

A larger micro- or minicomputer, possibly with multi-user capability, could implement the dedicated microprocessor scheme. This involves communication between the central processor and the TMS9909 at a very high level, i.e., all file manipulations, block searching, etc., are executed by a dedicated processor configured for non-DMA data transfers. Figure 11 shows a block diagram of the TMS9909 FDC in a system without a DMAC and utilizing the TMS9995 as a dedicated microprocessor.

4.1 INITIALIZATION

This section of code would normally be run once at power-up in order to reset the TMS9909 and place the disk drives in a known starting condition. A hardware reset should be active for 1 microsecond for proper initialization. The RSTC command is issued to put the FDC in the reset state, shown in Section 3.1.3. A RDAR command is then used to set the stepping times and to step the disks (two in this case) to track 00. (Refer to Table 5 for details.)

It is assumed in this example that one of the drives (Drive 0) is an 8-inch standard drive while the other drive (Drive 1) is a 5 1/4-inch mini-floppy. The head stepping and load parameters required by the drives are set to the following configuration:

	8-inch DRIVE	5 1/4-inch DRIVE
Track-to-track access (step) time	10 ms	20 ms
Head settling time	8 ms	12 ms
Head load time	35 ms	50 ms

The binary values loaded into the parameter registers are given by:

rate = (time multiplied by two) plus one

Therefore, the register values are as follows:

	A RATES 8-inch DRIVE	B RATES 5 1/4-inch DRIVE
Head step	10 ms >15	20 ms >29
Head settling	8 ms >11	12 ms >19
Head load	35 ms >47	50 ms >65

Note: >hex

The last byte to be loaded is the rate allocation map (Partition 01, S0-S2 = 111) which, for this example, selects A rates for Drive 0 and B rates for Drive 1, i.e., the last byte equals >06.

When the RDAR command is complete, the FDC issues an interrupt to the microprocessor and sets the BUSY bit in the status register high to indicate that a new command may be accepted. A status return of >FF indicates successful completion of the execution. If this is not the case, the status register will have an error return in it that may be decoded from Table 10.

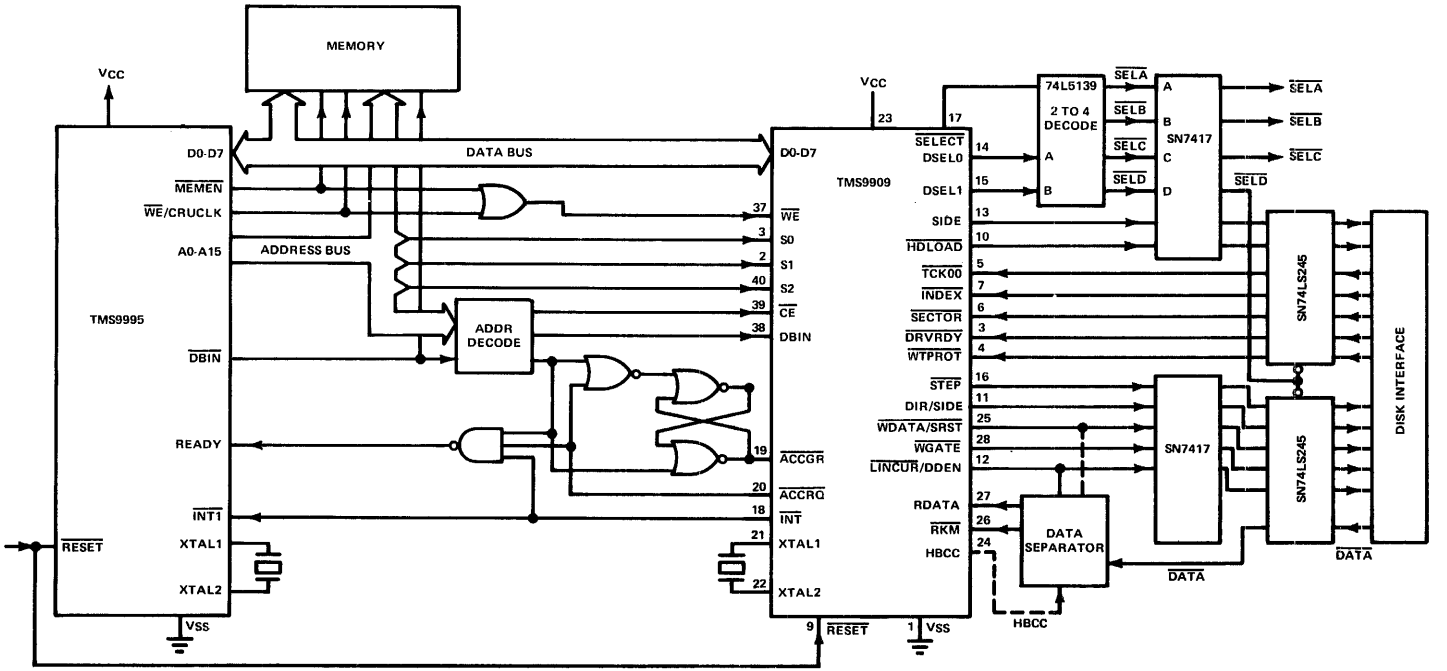


FIGURE 11 — BLOCK DIAGRAM OF TMS9995 DEDICATED MICROPROCESSOR SYSTEM

4.2 TMS9909 FORMAT CAPABILITIES

TABLE 11 — TYPICAL TRACK SECTOR ON A SOFT-SECTORED DISK

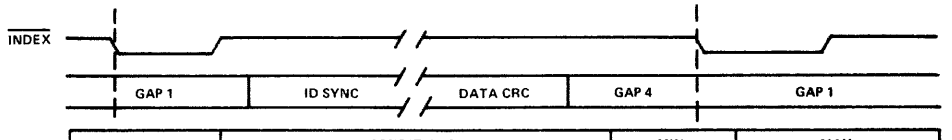
ID SYNC	ID AM	ID BYTES	ID CRC	GAP2	DATA SYNC	DATA AM	DATA FIELD	DATA CRC	GAP3

FIELD LENGTHS (IN BYTES) ALLOWED BY THE TMS9909

FIELD	CONDITIONS	MIN	MAX
ID SYNC		3	
ID AM	ONLY	1	3
ID BYTES	1 AM	1	14
	3 AMs	1	12
ID CRC	ONLY	0	2
GAP 2	XFER=125 kHz, ID CRC	3	17
	NO ID CRC	5	19
	=250 kHz, ID CRC	5	31
	NO ID CRC	7	31
	=500 kHz, ID CRC	8	31
	NO ID CRC	9	31
DATA SYNC		3	31
DATA AM	ONLY	1	3
DATA FIELD	1 AM	2	4094
	3 AMs	2	4092
DATA CRC	ONLY	0	2
GAP 3	XFER=125 kHz	8	
	=250 kHz	10	
	=500 kHz	14	

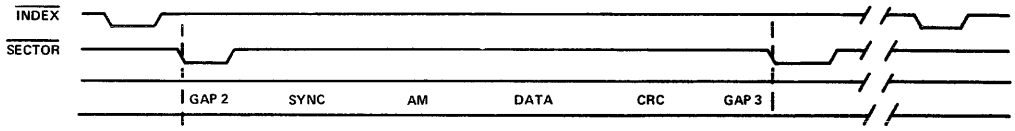
NOTE: "ONLY" means the field component can have either the maximum or minimum number of bytes shown. Otherwise, minimum and maximum define a range.

TABLE 12 — BEGINNING AND END OF TRACK GAPS



FIELD	CONDITIONS	MIN	MAX
GAP 1	ALL DATA RATES	5	
GAP 4		5	

TABLE 13 — HARD-SECTORED DISK FORMATS



FIELD	CONDITIONS	MIN	MAX
GAP 2	XFER = 125 KHz = 250 KHz = 500 KHz	3 5 8	16 31 31
GAP 3	XFER = 125 KHz = 250 KHz = 500 KHz	8 10 14	

4.3 IBM 3740 FORMAT EXAMPLE

The format selected for the purpose of this demonstration is IBM 3740. It is a single-density, soft-sectored format where each diskette contains 74 active tracks (two are spares) with each track having 26 sectors of 128 data bytes.

A formatted track is divided into fields. Each field is defined by the user. As shown in Table 14, the field definition parameters are sent to the FDC by a block of five DMA handshakes.

TABLE 14 — DMA FORMAT PARAMETERS

BYTE NO.	MSB				LSB
1	CRC	FILL	IBM MFM	X X	FIELD LENGTH MS 4 BITS (MSN)
2	FIELD LENGTH LS BYTE (LSB)				
3	CLOCK PATTERN OF ADDRESS MARK				
4	DATA PATTERN OF ADDRESS MARK				
5	DATA BYTE				

Each field has the following options:

1) One Address Mark is written at the start if IBM MFM = 0. Three Address Marks are written at the start if IBM MFM = 1.

2) A data byte that is written for the duration of the field if the FILL bit = 1. If the FILL bit = 0, no data bytes are written.

3) A two-byte CRC is written at the end of the field if the CRC bit = 1. If the CRC bit = 0, no CRC bytes are written.

If the FILL bit is low, the data byte is written once at the start of the field (after the Address Mark). The FDC will then request further bytes until it has written to the end of the field. In this case, the number of bytes that define the field will be four plus the number of data bytes in the field. The field length includes the Address Mark(s) but excludes the CRC bytes (if present). The minimum field length is three bytes if one Address Mark is used and five bytes if three Address Marks are used. The maximum field length is 4095 bytes. Table 15 summarizes the IBM 3740 single-density format for a soft-sectored disk.

TABLE 15 — IBM 3740 SINGLE-DENSITY FORMAT

NUMBER OF BYTES	DATA HEX VALUE	DESCRIPTION
40	FF	Gap 4A
6	00	SYNC bytes
1	FC*	Index AM
26****	FF	FILL bytes
6****	00	ID SYNC
1****	FE**	ID AM
1****	1A	Track number
1****	00	Side 0
1****	01	Sector 1
1****	01	Sector length of 128 bytes
2****		ID CRC
11****	FF	Gap 2
6****	00	Data SYNC
1****	FB***	Data AM
128****		Data field
2****		Data CRC
27****	FF	WGOFF + Gap 3
250*****	FF	Gap 4B

* Index AM clock pattern = >D7
** ID AM clock pattern = >C7
*** Data AM clock pattern = >C7
**** Repeat 26 times to format all the sectors on the track.
***** This number is approximate since its purpose is to write > FF as a FILL byte until the next index pulse is detected by the FDC.

Table 16 gives an example of a soft-sectored disk, formatted according to the IBM 3740 single-density standard:

TABLE 16 — IBM 3740 SINGLE-DENSITY FORMAT EXAMPLE

LINE	DMA BYTE No.	BYTE VALUE (HEX)	CONTENTS
1	1	40	First track field
2	2	28	
3	3	FF	
4	4	FF	Gap 4A...40 bytes of >FF
5	5	FF	
6	1	40	Second field
7	2	06	
8	3	FF	SYNC bytes preceding Index Address Mark
9	4	00	
10	5	00	
11	1	40	Third field
12	2	1B	
13	3	D7	Index AM followed by Gap 1...26 bytes
14	4	FC	of >FF
15	5	FF	

TABLE 16 — IBM 3740 SINGLE-DENSITY FORMAT EXAMPLE (Continued)

LINE	DMA BYTE No.	BYTE VALUE (HEX)	CONTENTS
16	1	40	Fourth field
17	2	06	
18	3	FF	SYNC bytes preceding ID field AM
19	4	00	
20	5	00	
21	1	80	Fifth field
22	2	05	
23	3	C7	ID field 1
24	4	FE	
25	5	1A	Track number
26	6	00	Side 0
27	7	01	Sector 1
28	8	01	Sector length 128 bytes
29	1	40	Sixth field
30	2	0B	
31	3	FF	Gap 2...11 bytes ≯FF
32	4	FF	
33	5	FF	
34	1	40	Seventh field
35	2	06	
36	3	FF	SYNC bytes preceding data field AM
37	4	00	
38	5	00	
39	1	C0	Eighth field
40	2	81	
41	3	C7	Data field of ≯FF plus 2 CRC bytes
42	4	FB	
43	5	FF	
44	1	40	Ninth field
45	2	1B	
46	3	FF	WGOFF plus Gap 3
47	4	FF	
48	5	FF	

TABLE 16 — IBM 3740 SINGLE-DENSITY FORMAT EXAMPLE (Continued)

LINE	DMA BYTE No.	BYTE VALUE (HEX)	CONTENTS
	Lines 16-48 inclusive are repeated with line 27 incremented up to hex 1A. This gives the requisite 26 sectors.		
874	1	4F	160th Field
875	2	FF	
876	3	FF	Gap 4B...Fill track with >FF to
877	4	FF	next index
878	5	FF	
879	1	4F	161st Field
880	2	FF	
881	3	FF	GAP 4B...Extra field supplied at end
882	4	FF	
883	5	FF	

NOTES

A. The only difference between an Address Mark and an ordinary data byte is the user's ability to define the clock pattern. For fields that do not have a true Address Mark at the beginning, the clock pattern is defined without any missing bits.

B. For a data field with 128 bytes, the field length is 129 for one Address Mark and 131 for three Address Marks.

C. The FDC will stop writing at the following index pulse. Therefore, the last field should be the maximum length to allow for disk speed variations.

D. The FDC requests the following field as soon as it starts writing the current field. In the case of the final field, a further field is requested. This field may be the same as the last field or may take any other value.

E. After the format command is issued, the FDC waits indefinitely for the first five DMA handshakes. The FDC will remain "busy" until these five DMA bytes are issued.

F. For formats with double-density encoding, the first data byte following a CRC field should have the MSB set to a 1 in order to ensure that the encoding rules are not violated.

Following the first five DMA handshakes, the first field will be written by the FDC upon detection of the index (soft) or sector (hard) pulse. The FDC will request the five DMA handshakes defining the next field when the Address Mark(s) is (are) written and the field is a fill field or, for a non-fill field, after the last byte is requested. When requesting the five DMA bytes, the FDC holds the $\overline{\text{ACCRQ}}$ line low until the fifth byte is received. If the fifth byte is not received by the time the FDC is ready to write the next field, an error is detected. An error is also detected when single bytes are being transferred for a non-fill field and the FDC has to write the next byte before it has been received. In both cases, the Handshake Abort bit (bit 1 of the status register) is set low and no more DMA bytes are requested. Following a Handshake Abort, the FDC continues to format until the next index (soft) or sector (hard) pulse. However, the contents of the written field cannot be guaranteed. The required timings are given in Table 17.

TABLE 17 — TIMING FOR DMA TRANSFER

1 or 5 BYTE XFER	PREVIOUS FILL	FIELD CRC	IBM MFM	TIMING FROM $\overline{ACCRQ}$ LOW TO LAST BYTE TRANSFERRED
5	Yes	No	No	Field length — 1 byte -3 μs
5	Yes	No	Yes	Field length — 3 byte -3 μs
5	Yes	Yes	No	Field length — 1 byte -3 μs
5	Yes	Yes	Yes	Field length — 1 byte -3 μs
5	No	No	XXX	1 Byte — 2 μs
5	No	Yes	XXX	3 Bytes — 2 μs
1 Current Field, FILL = No				1 Byte — 3 μs

NOTE: At the end of the formatting operation and following the next index or sector pulse, the disk head remains loaded for another four index pulses before the HDLOAD pin is forced high.

4.4 DATA SEPARATION

The FDC requires an external data separator circuit to generate the $\overline{RKM}$ input necessary for clocking in data from a floppy disk. Several techniques are available for generating $\overline{RKM}$. The FDC itself provides three signals to facilitate the implementation of this circuit: Half-Bit Cell Clock (HBCC), Double-Density Enable (DDEN), and Separator Reset ($\overline{SRST}$).

HBCC and DDEN are correctly configured from the encoding and transfer rate information in parameter byte 1 of Partition 10. These signals are made valid by the first execution of an executable command (typically RDAR in the initialization sequence). The HBCC clock runs at exactly twice the programmed transfer rate frequency which is nominally the same frequency as that required by $\overline{RKM}$. The DDEN signal to the data separator indicates that the FDC is expecting double-density enclosed data (MFM or M^{2}FM). $\overline{SRST}$ signals the data separator that the FDC is actively reading the data it is receiving on its read channel (RDATA). $\overline{SRST}$ is valid any time $\overline{WGATE}$ is high. These conditions are summarized as follows:

1) $\overline{SRST}$ is active whenever the FDC is reading data from the disk.

2) $\overline{SRST}$ makes the transition from an idle state to an active state when the FDC begins to look for SYNC (ID or data) coming from the disk.

3) $\overline{SRST}$ makes the transition from an active state to an idle state when the FDC has read the desired ID field or has read the desired data field or has detected an error.

NOTE

If CRC is not selected for the desired field, $\overline{SRST}$ goes inactive three bytes into the following gap field. If CRC is selected for the desired field, $\overline{SRST}$ goes inactive one byte into the following gap field.

4) When the FDC is seeking a sector on a soft-sectored disk, $\overline{SRST}$ will not go inactive until the FDC has read its desired ID field or has encountered two index pulses.

$\overline{SRST}$ may be used to switch between RDATA and HBCC as inputs to the data separator, i.e., to run the data separator on RDATA when $\overline{SRST}$ is active and run the data separator on HBCC when $\overline{SRST}$ is inactive. This scheme allows the data separator to be running at the correct frequency until such a time as the FDC needs the disk data. When RDATA is switched in, the data separator has only to correct for the phase error. This is easily accomplished in the SYNC field since there is no bit-shift (bit-shift being the spatial shift of the maximum of a magnetic flux transition pulse as it is recorded on the media due to the close proximity of its neighboring pulses). In addition, the data separator has the capability of ignoring the noisy portion of the ID-data gap associated with turning on $\overline{WGATE}$ when the selected ID field has been found. (This noise may be considerable on magnetic media.)

4.4.1 Data Separator Circuit

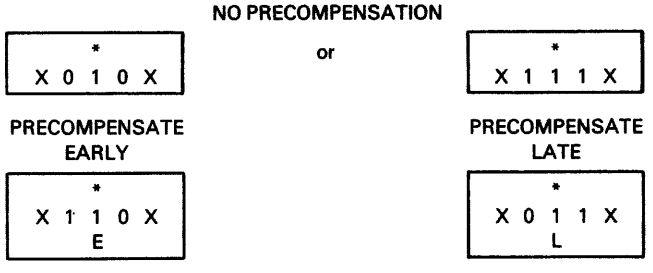
See Appendix A.

4.5 DATA PRECOMPENSATION

Information is stored as magnetic flux transitions on diskettes and other magnetic media. Data and clock bits that are ones are represented as flux transitions, while data and clock bits that are zeros are represented as the absense of such flux transitions. The flux transitions are written for one bits (or not written for zero bits) at evenly spaced "half-bit cell" intervals as the diskette passes under the read/write head of the drive. (A "bit cell" is defined as two consecutive bits of information with the leading bit always being a clock bit and the second bit always being a data bit.) When there is a high spatial density of these flux transitions, bit-shift may occur. Magnetic interactions cause a variance in position of the pulse being written with respect to the edge of its nearest neighbor and may move the maximum of the pulse being written away from that neighbor. This can greatly complicate data recovery. Precompensation is the data-dependent slight advancing or retarding of the moment a pulse is written to ensure that the pulse maximum is recorded as close as possible to the proper half-bit cell interval. If precompensation is selected on the TMS9909, certain $\overline{\text{WDATA}}$ pulses will be advanced or retarded by 167ns. The TMS9909 has two precompensation algorithms: one for single density (FM) and one for double density (MFM and M^{2}FM).

4.5.1 Single-Density Precompensation

In FM encoding, the decision whether or not to precompensate a $\overline{\text{WDATA}}$ pulse is based only upon the presence or absence of pulses in the former and subsequent half-bit cells. That is, if both the nearest half-bit cells contain zeros or ones (symmetric configuration), then the pulse being written will not be precompensated. If the former half-bit cell contains a one and the subsequent half-bit cell contains a zero (asymmetric configuration), then the pulse being written will be precompensated early (advanced). If the subsequent half-bit cell contains a one and the former half-bit cell contains a zero (asymmetric configuration), then the pulse being written will be precompensated late (retarded).



SINGLE-DENSITY PRECOMPENSATION

4.5.2 Double-Density Precompensation

In MFM and M^{2}FM encoding, adjacent half-bit cells must never contain both pulses. The decision whether or not to precompensate a $\overline{\text{WDATA}}$ pulse is based upon the value of the bits one bit cell away on either side. If the configuration of these two cells (one bit cell away on either side) is symmetric, then, as with FM encoding, there is no precompensation. However, for an asymmetric configuration in MFM and M^{2}FM encoding, one of the following applies:

1) If both sides have nearest neighbors more than one bit cell away, then the pulse being written is not precompensated.

2) If there is a nearest neighbor one bit cell away (two half-bit cells) and if the nearest neighboring pulse on the other side is three or more half-bit cells away, then the pulse being written will be precompensated toward the nearest neighbor accordingly.

NO PRECOMPENSATION

```
        *
X X 1 0 1 0 1 X X
```

```
        *
X X 0 0 1 0 0 X X
```

PRECOMPENSATE EARLY

```
        *
X X 1 0 1 0 0 X X
      E
```

PRECOMPENSATE LATE

```
        *
X X 0 0 1 0 1 X X
      L
```

DOUBLE-DENSITY PRECOMPENSATION

4.5.3 Half-Bit Cell Clock (HBCC)

HBCC is a clock that runs at twice the programmed transfer rate frequency (125,250 or 500 kilobits/sec). The width of the HBCC pulse is 500 ns. In the write mode, HBCC defines the half-bit cell interval with WDATA nominally located in the middle of the HBCC pulse. With early precompensation, the WDATA pulse occurs during the first 167 ns of HBCC. With late precompensation, the WDATA pulse occurs during the last 167 ns of HBCC.

5. TMS9909 PRELIMINARY ELECTRICAL SPECIFICATIONS

5.1 ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)*

Supply voltage, VCC** ..... -0.3 to 10 V
All input voltages ..... -0.3 to 10 V
Output voltage ..... -2 to 7 V
Continuous power dissipation ..... 1.05 W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... -55°C to 150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**All voltage values are with respect to V_{SS}.

5.2 RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH}	2		VCC	V
Low-level input voltage, V_{IL}			.8	V
High-level output current, I_{OH}			400	μA
Low-level output current, I_{OL}			2	mA
Operating free-air temperature range, T_A	0		70	°C

5.3 ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS (UNLESS OTHERWISE NOTED)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_I	Input current, all inputs	V_I=2V to V_{CC}		± 10		μA
V_{OH}	High level output voltage, any output	V_{CC} = MIN I_{OH} = MAX	2.4			V
V_{OL}	Low level output voltage, any output	V_{CC} = MIN I_{OL} = MAX			0.6	V
I_{CC}	Supply current from V_{CC}	V_{CC} = MAX		150	200	mA
C_I	Small signal input capacitance	f = 1 MHz Unmeasured pins at V_{SS}		15		pF

5.4 CLOCK CHARACTERISTICS

The TMS9909 has an internal oscillator controlled by an external crystal. The user may disable the oscillator and directly inject a frequency source into XTAL1 with XTAL2 left unconnected.

5.4.1 Internal Clock Option

The internal oscillator is enabled by connecting a crystal across XTAL1 and XTAL2. Note that the crystal must be of the parallel-resonant type. The capacitors are optional but they will enhance reliability over the operating temperature range of the TMS9909.

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
F_{OSC} source frequency	0 – 70°C	5.9997	6	6.0003	MHz
C	0 – 70°C	10	15	25	pF

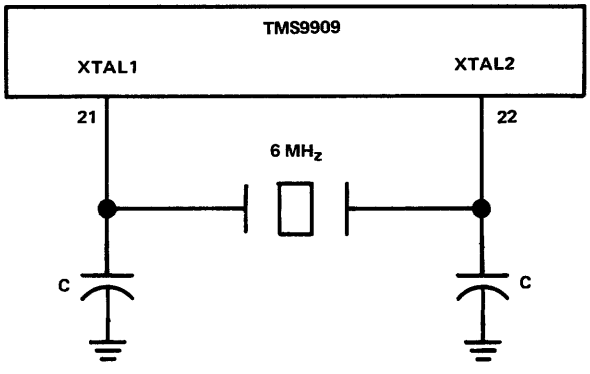


FIGURE 12 – CRYSTAL CONNECTION

5.4.2 External Clock Option

An external frequency source may be used by injecting the frequency directly into XTAL1 with XTAL2 left unconnected. The external frequency must conform to the following specifications.

PARAMETER		MIN	NOM	MAX	UNIT
f_{ext}	External source frequency	5.9997	6	6.0003	MHz
t_{ri}	Input oscillator rise time		5	20	ns
t_{whi}	Input oscillator pulse width high	75	80	85	ns
t_{fi}	Input oscillator fall time		5	20	ns
t_{wli}	Input oscillator pulse width low	75	80	85	ns

5.5 TIMING REQUIREMENTS OVER RECOMMENDED OPERATING CONDITIONS

5.5.1 MPU to FDC Interface

PARAMETER			MIN	NOM	MAX	UNIT
$t_{wh(CE)}$	Pulse width, $\overline{CE}$ high		500	670		ns
t_{su} (EMPU-WE)	Setup time for enabled MPU signals. Time from S0-S2, DBIN, $\overline{CE}$ valid to $\overline{WE}$↑		400	500		ns
$t_{wl(WE)}$	Pulse width, WE input low		200	330		ns
$t_{su(DWH)}$	Setup time, data prior to $\overline{WE}$↑	($\overline{CE}$ low) ($\overline{ACCGR}$ low)	250 200	350 250		ns ns
$t_{h(WHD)}$	Hold time, data after $\overline{WE}$↑		50	100		ns
$t_{a(EMPU-D)}$	Access time for enabled MPU signals. Time from S0-S2, DBIN, $\overline{CE}$ valid to valid data.			300	400	ns
$t_{d(CE-Z)}$	Delay time, $\overline{CE}$ high to D0-D7 high Z			90	200	ns
$t_{h(WE-EMPU)}$	Hold time for enabled MPU signals			50		ns

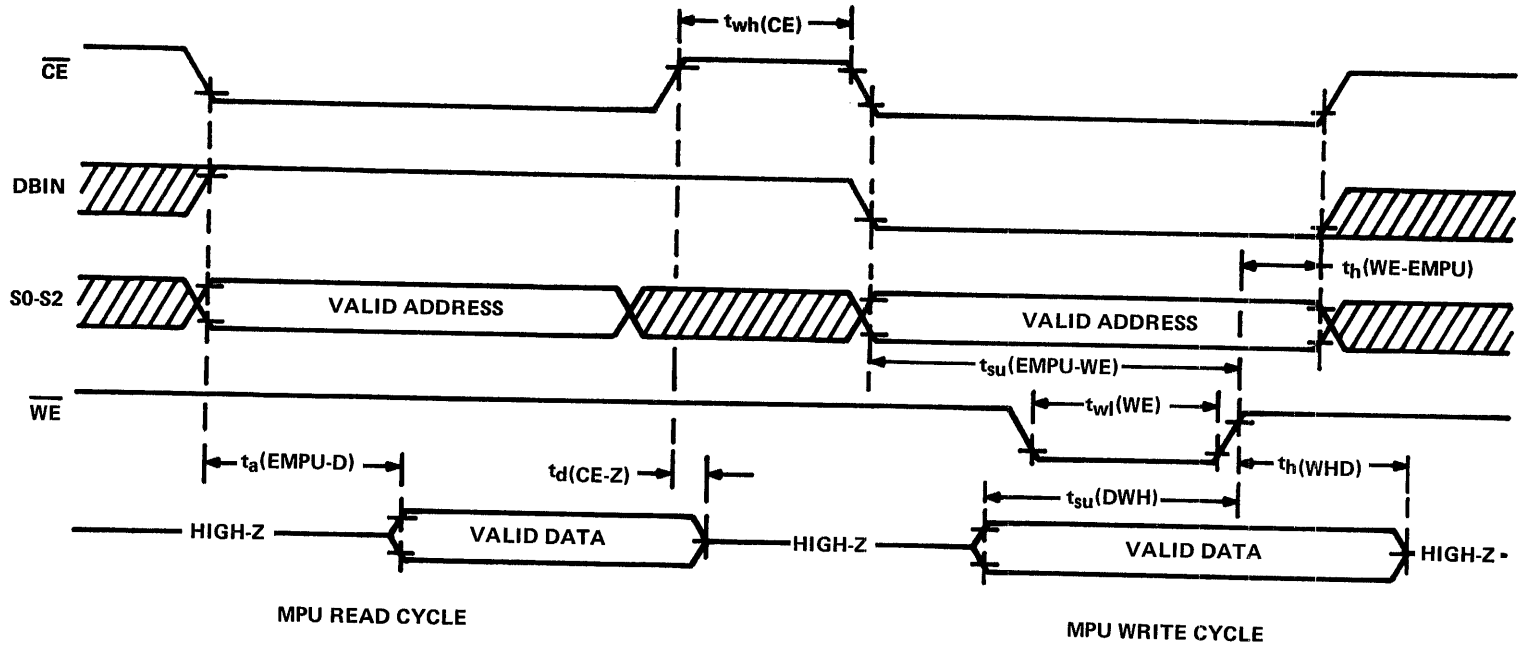
5.5.2 DMA Interface

PARAMETER		MIN	NOM	MAX	UNIT
$t_{wl(AG)}$	Pulse width, $\overline{ACCGR}$ low	400	667		ns
t_{wh} (AG)	Pulse width, $\overline{ACCGR}$ high	500			ns
t_{su} (DB-AG)	Setup time, DBIN low prior to $\overline{ACCGR}$ low	0	50		ns
t_{su} (DB-AG)	Setup time, DBIN high prior to $\overline{ACCGR}$ low	0	50		ns
t_{su} (EDMA-WE)	Setup time for enabled DMA signals. Time from $\overline{ACCGR}$ and DBIN valid to $\overline{WE}$↑	400	500		ns
t_h (WE-EDMA)	Hold time, enabled DMA signals DBIN, $\overline{ACCGR}$ after $\overline{WE}$↑	30	50		ns
t_d (AG-AR)	Delay time, $\overline{ACCGR}$ low to $\overline{ACCRQ}$ high		50	100	ns
t_a (EDMA-D)	Access time for enabled DMA signals. Time from $\overline{ACCGR}$ and DBIN valid to valid data.		100	200	ns
t_d (AG-Z)	Delay time, $\overline{ACCGR}$ high to data bus high Z		110	200	ns
$t_{d(AR-AG)}$	Delay time, $\overline{ACCRQ}$ low to 5th $\overline{ACCGR}$	See Section 4.3, Table 17			

5.5.3 FDC to Disk Drive Interface

PARAMETER		MIN	NOM	MAX	UNIT
$t_{a(SL-DY)}$	Access time, $\overline{SELECT}$ low to $\overline{DRVRDY}$ low			1.25	s
$t_{wl(DY)}$	Pulse width low, $\overline{DRVRDY}$ input	10			μs
$t_{su(DY-DD)}$	Setup time, $\overline{DRVRDY}$ prior to DDEN valid	30	70	100	μs
$t_{wl(TK)}$	Pulse width low, $\overline{TCK00}$ input	2*tc(st)			
$t_{su(RD-RC)}$	Setup time, RDATA prior to $\overline{RKM}$↑	50			ns
$t_{h(RD-RC)}$	Hold time RDATA after $\overline{RKM}$	30			ns
$t_{wh(RC)}$	Pulse width high, $\overline{RKM}$ input	300		3000	ns
$t_{wl(RC)}$	Pulse width low, $\overline{RKM}$ input	150		3000	ns
$t_{su(WP-WG)}$	Setup time, $\overline{WTPROT}$ prior to WGATE low	150			μs
$t_{h(WP-WG)}$	Hold time, $\overline{WTPROT}$ after $\overline{WGATE}$ low	10			μs
$t_{c(I-I)}$	Cycle time, $\overline{INDEX}$ to next $\overline{INDEX}$	.5	167		ms
$t_{wl(I)}$	Pulse width low, $\overline{INDEX}$ input	6			μs
$t_{a(S-I)}$	Access time, $\overline{SECTOR}$ to $\overline{INDEX}$	0	2.6		ms
$t_{d(I-S)}$	Delay time, $\overline{INDEX}$ to $\overline{SECTOR}$	0	2.6		ms
$t_{wl(S)}$	Pulse width low, $\overline{SECTOR}$ input	6			us
$t_{c(S-S)}$	Cycle time, $\overline{SECTOR}$ to $\overline{SECTOR}$	0.5	5.2		ms
$t_{a(ST-TK)}$	Access time, $\overline{STEP}$ low to $\overline{TCK00}$ input		$3/4t_{c(st)}$	$t_{c(st)}$	
$t_{d(P-SL)}$	Delay time, $\overline{SELECT}$ high after static signals	2	4		μs
$t_{d(SL-P)}$	Delay time, $\overline{SELECT}$ high prior to static change	2	4		μs
$t_{d(ST-HL)}$	Delay time, $\overline{STEP}$ to $\overline{HDLOAD}$ low	.5		127.5	ms
$t_{c(ST)}$	Cycle time, $\overline{STEP}$ output	.5		127.5	ms
$t_{wl(ST)}$	Pulse width low, $\overline{STEP}$ output	$0.4t_{c(st)}$	$0.5t_{c(st)}$	$0.6\ t_{c(st)}$	ms
$t_{d(DR-ST)}$	Delay time, DIR valid to $\overline{STEP}$ low	12	16	20	μs
$t_{d(LW-WG)}$	Delay time, $\overline{LWCUR}$ valid to $\overline{WGATE}$ low	4	6		μs
$t_{d(WG-LW)}$	Delay time, $\overline{LWCUR}$ valid after $\overline{WGATE}$ high	12	15		μs

PARAMETER			MIN	NOM	MAX	UNIT
$t_{d(WG-WD)}$	Delay time, $\overline{WGATE}$ low to $\overline{WDATA}$ valid	rate=500 kHz		2		µs
		rate=250 kHz		4		
		rate=125 kHz		8		
$t_{wl(WD)}$	Pulse width low, $\overline{WDATA}$ output		140	167	180	ns
$t_{d(WD-WG)}$	Delay time, last $\overline{WDATA}$ to $\overline{WGATE}$ high			1 bit cell		
$t_{wl(HB)}$	Pulse width low HBCC output	rate=500 kHz		0.5		µs
		rate=250 kHz		1.5		
		rate=125 kHz		3.5		
$t_{wh(HB)}$	Pulse width high, HBCC output			500		ns
$t_{d(CR-SR)}$	Delay time, LSB of CRC to $\overline{WDATA}/\overline{SRST}$ high	rate=500 kHz		16		µs
		rate=250 kHz		32		
		rate=125 kHz		64		
$t_{d(SY-SR)}$	Delay time, MSB of SYNC to $\overline{WDATA}/\overline{SRST}$ low	rate=500 kHz		0		µs
		rate=250 kHz		16		
		rate=125 kHz		40		



NOTE: All switching times are assumed to be at 10% or 90% values unless otherwise drawn.

FIGURE 13 – MPU TO FDC INTERNAL TIMING

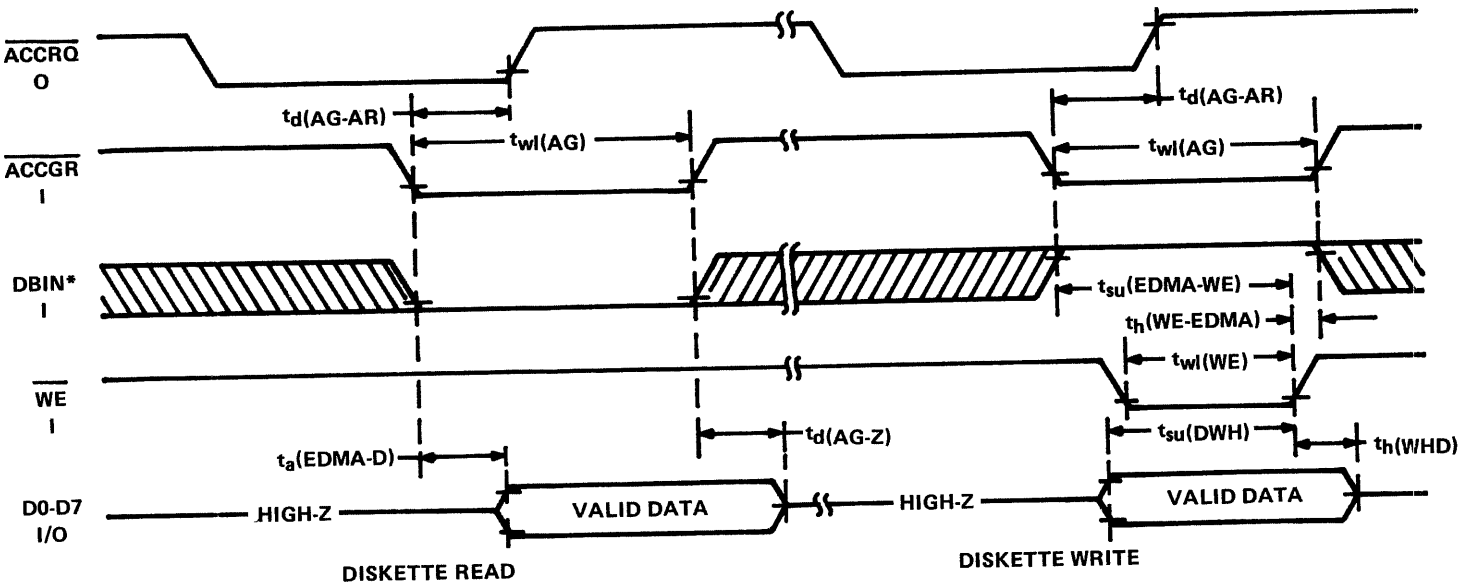
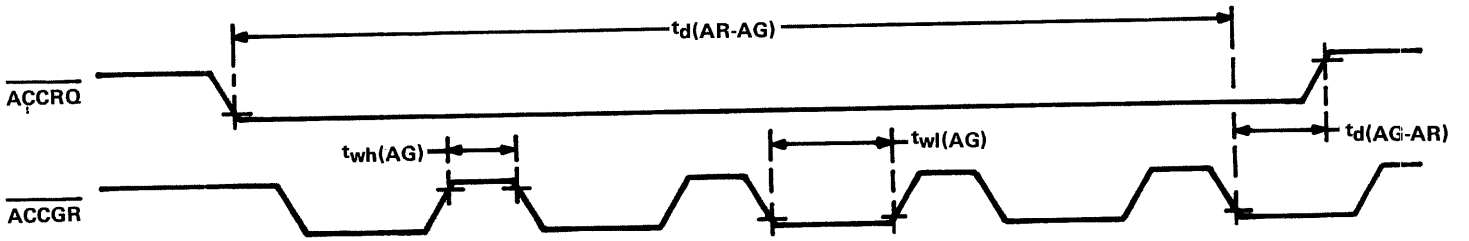
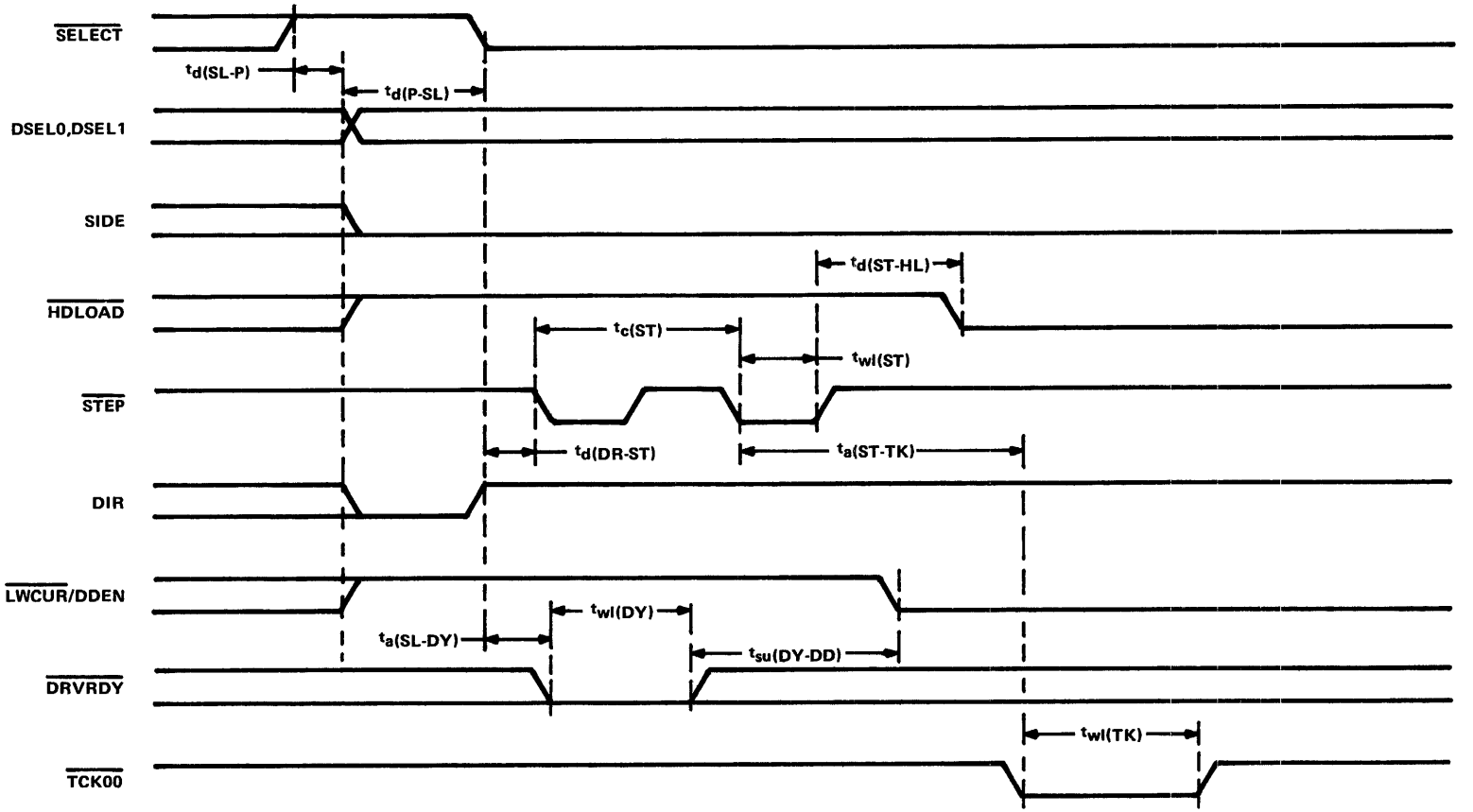


FIGURE 14 – DMA INTERFACE TIMING



* DBIN as driven by the DMAC – The sense of DBIN is inverted with respect to the MPU when the FDC is in the DMA mode.
NOTE: All switching times are assumed to be at 10% or 90% values unless otherwise drawn.

FIGURE 15 – DISKETTE FORMAT DMA HANDSHAKE SEQUENCE



NOTE: All switching times are assumed to be at 10% or 90% values.

FIGURE 16 — FDC TO DISK INTERFACE TIMING

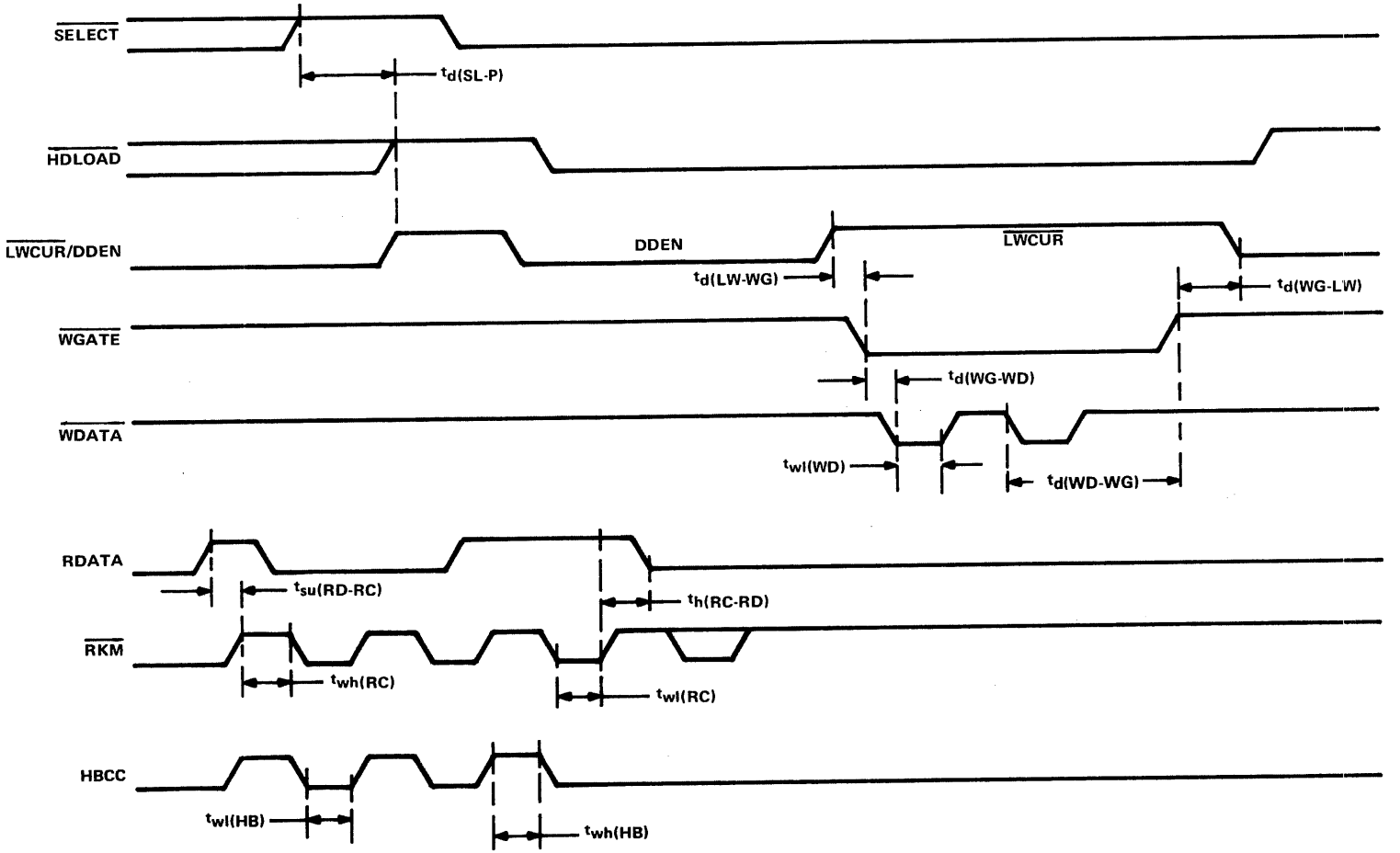


FIGURE 16 — FDC TO DISK INTERFACE TIMING (Continued)

NOTE: All switching times are assumed to be at 10% or 90% values.

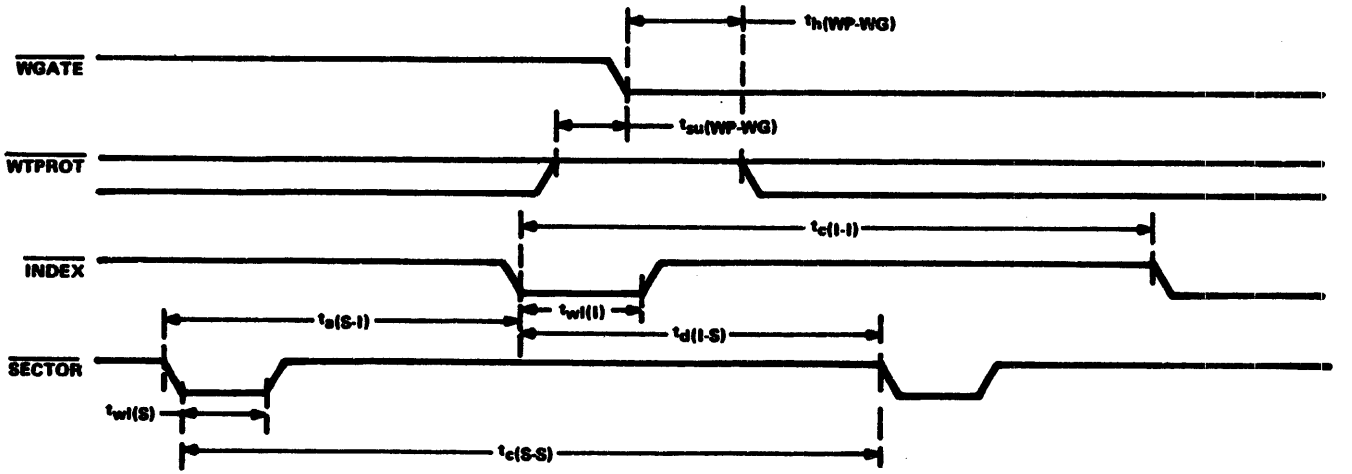
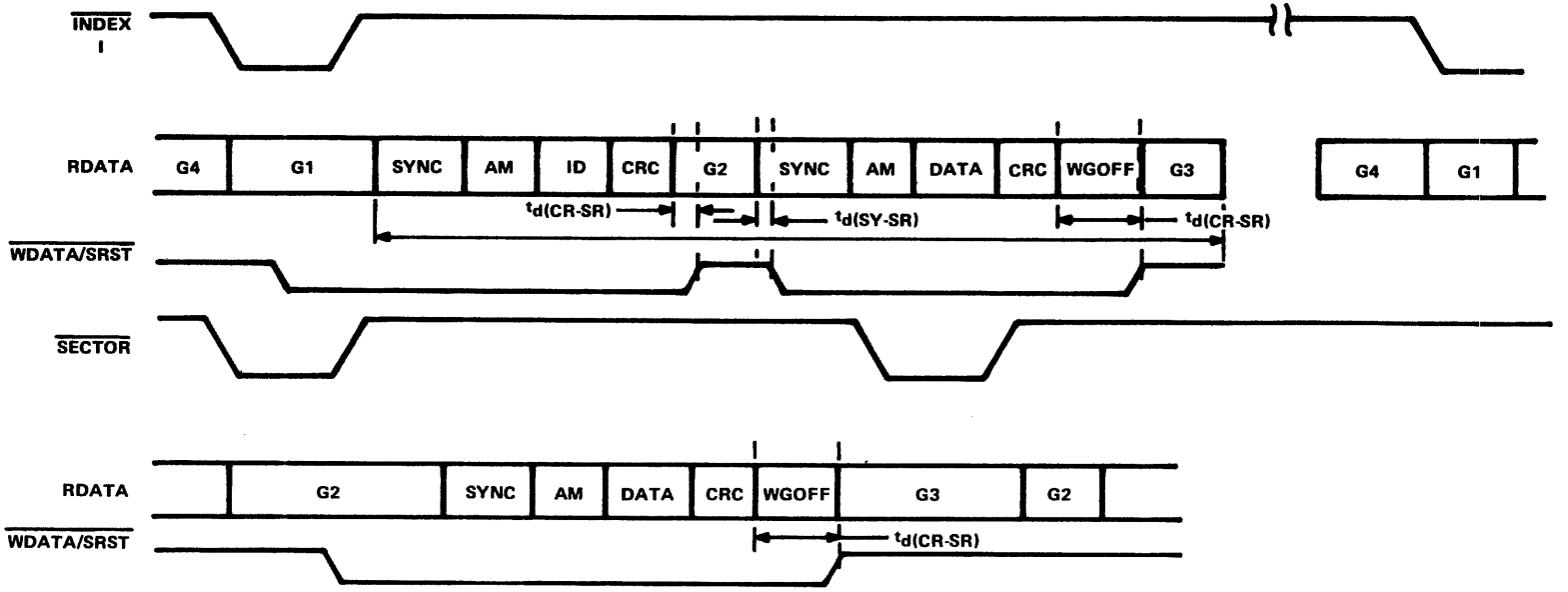


FIGURE 16 — FDC TO DISK INTERFACE TIMING (Concluded)

NOTE: All switching times are assumed to be at 10% or 90% values.



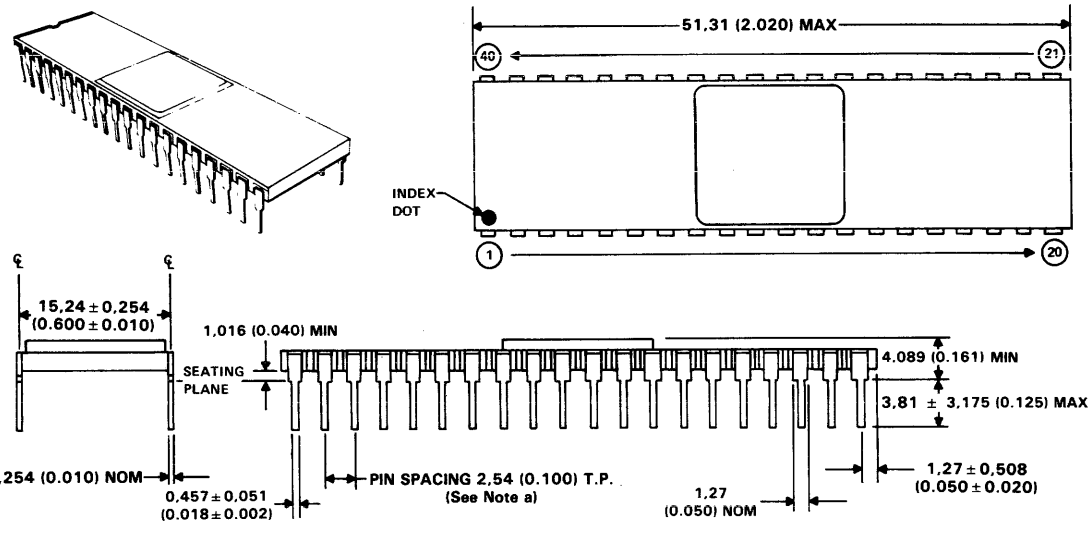
NOTE: All switching times are assumed to be at 10% or 90% values.

FIGURE 17 — SECTOR FORMAT AND READ INTERFACE TIMING

6. MECHANICAL SPECIFICATIONS

6.1 TMS9909JL — 40-PIN CERAMIC PACKAGE

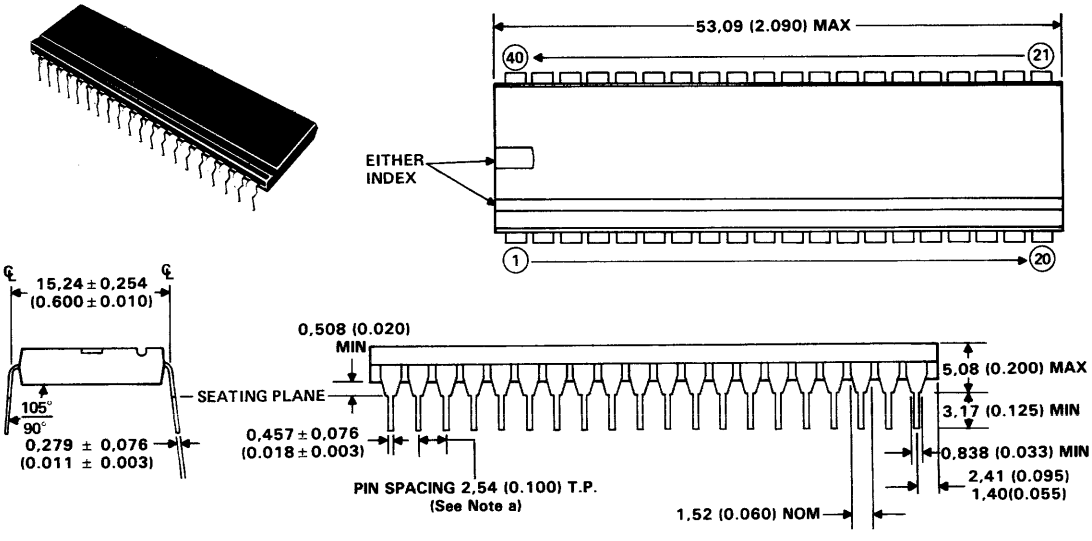
Ceramic packages with side-brazed leads and metal, epoxy, or glass lid seal



NOTES: a. Each pin centerline is located within 0,254 (0.010) of its true longitudinal position.
b. All linear dimensions are in millimeters and parenthetically in inches. Inch dimensions govern.

6.2 TMS9909NL — 40-PIN PLASTIC PACKAGE

Plastic packages



NOTES: a. Each pin centerline is located within 0,254 (0.010) of its true longitudinal position.
b. All linear dimensions are in millimeters and parenthetically in inches. Inch dimensions govern.

APPENDIX A

EXAMPLE OF A DATA SEPARATOR CIRCUIT FOR THE TMS9909

A.1 INTRODUCTION

Data separation is an important aspect of floppy disk controller design that has both analog and digital solutions. As an example of a flexible, cost-effective data separator design, the circuit described here can be used to provide data separation for systems implementing any combination of 8-inch or 5 1/4-inch single- or double-density floppy disk drives.

A.2 TMS9909 DATA SEPARATION REQUIREMENTS

The data separation function, which in fact does not actually separate data, involves regenerating a clock or strobe signal to sample information coded onto the serial bit stream (DATA) being read from the disk. Drive motor speed variations and bit-shift on the magnetic media (diskettes) complicate clock regeneration by causing the data waveform to jitter. This jitter is especially significant during 8-inch double-density recording and requires a data separator circuit to compensate for it dynamically if reliable FDC operation is to be assured.

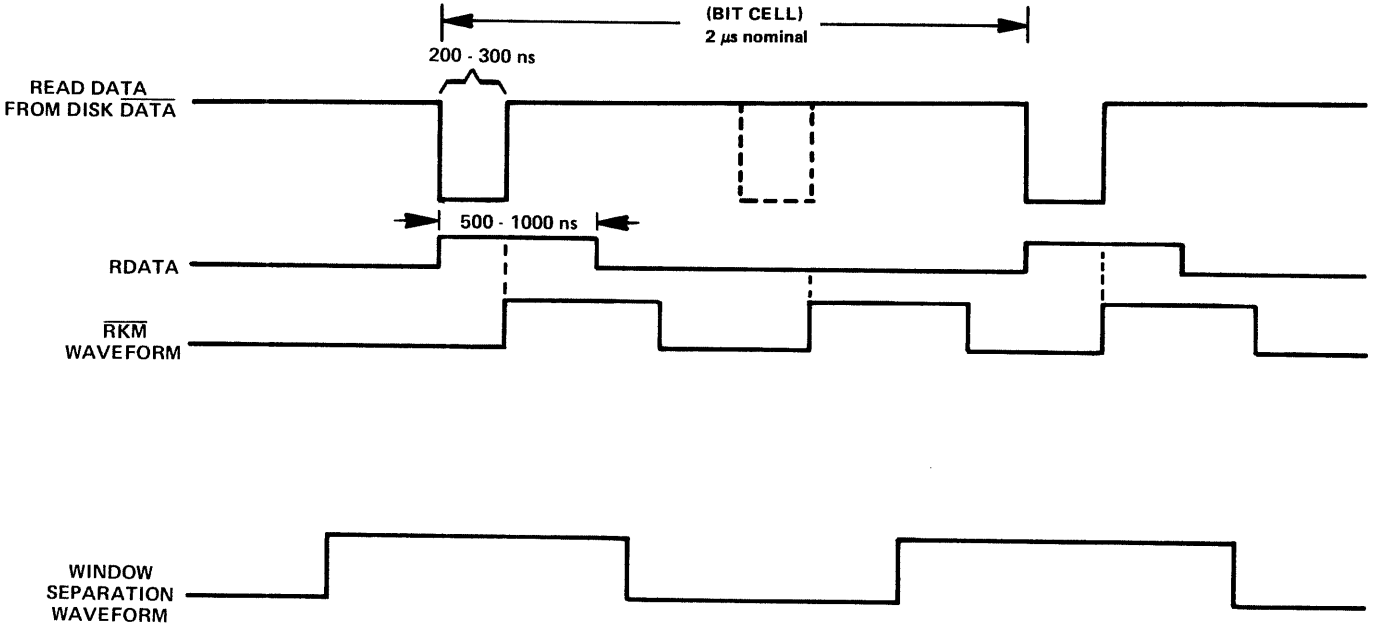
Some FDC chips use a window separation approach, i.e., the regenerated clock signal must make either a high-to-low or low-to-high transition at a point nominally midway between the information bits as they arrive from the disk. The TMS9909's timing requirements specify that the regenerated clock signal, RKM, must make a low-to-high transition which sustains 50 ns setup and 30 ns hold times with respect to the data. The data separation approach described here "stretches" the data pulses (DATA) from 200-300 ns to 500-1000 ns to provide a wider margin in meeting the TMS9909's timing requirements. Both the window separation approach and the TMS9909 timing requirements are illustrated in Figure A-1.

A.3 CIRCUIT OPERATION

The data separator circuit is designed around the FDC 9216 data separator chip made by Standard Microsystems Corporation. The FDC 9216 generates a signal that makes a transition at a point between the incoming data bits. The chip's logic compensates for timing variations in the data waveform and allows the data separator circuit in Figure A-2 to function reliably over a wide range of operating conditions. The remaining circuitry generates RKM so that it is consistent with the TMS9909's timing requirements.

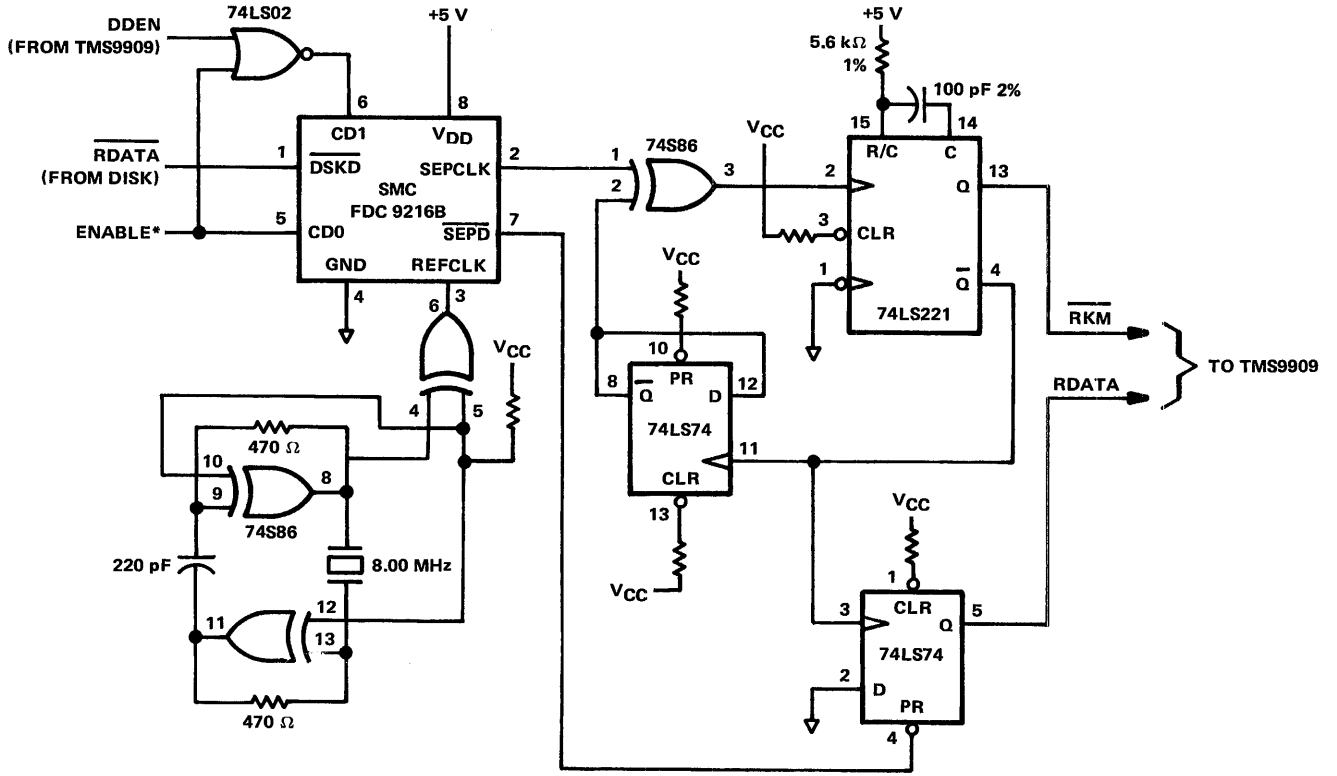
Specifically, when the SEPCLK signal from the FDC 9216 changes state, the output of the XOR gate will go high, triggering the SN74LS221 one-shot to generate RKM as a 375 ns pulse. The inverted version of this signal (RKM) is then used to clock the flip-flop which toggles to provide the correct state at the input of the XOR gate for the next transition of SEPCLK. Note that the second input of the XOR gate is assumed to be in the correct state to produce a high-going pulse at the output of the XOR gate on transitions of SEPCLK. This only occurs if the input is in the same state as SEPCLK before each transition. This may not be true for the first SEPCLK transition after power-up, but will be true for the next one, i.e., the next pulse will occur within a few ms of power-up. So, if one RKM pulse is missed, the system will not be affected.

The second flip-flop in the circuit is used to generate a stretched version of each data pulse (RDATA). The rising edge of RKM occurs in the middle of this data pulse while the falling edge of RKM clears the data pulse. This guarantees that the rising edge of RKM will fall well within the TMS9909's timing requirements over large variations of the data waveform. A timing diagram of the major signals in the circuit is shown in Figure A-3.



NOTE: This figure references a 500 kHz data rate.

FIGURE A-1 — DATA SEPARATION TIMING WAVEFORMS (8-INCH DOUBLE-DENSITY DISK)



* The enable signal should be set by the user ONLY for 8-inch single-density and 5¼-inch double-density disks.

NOTE: TI cannot assume responsibility for any circuits shown or represent that they are free from patent infringement.

FIGURE A-2 – TYPICAL DATA SEPARATOR CIRCUIT FOR TMS9909

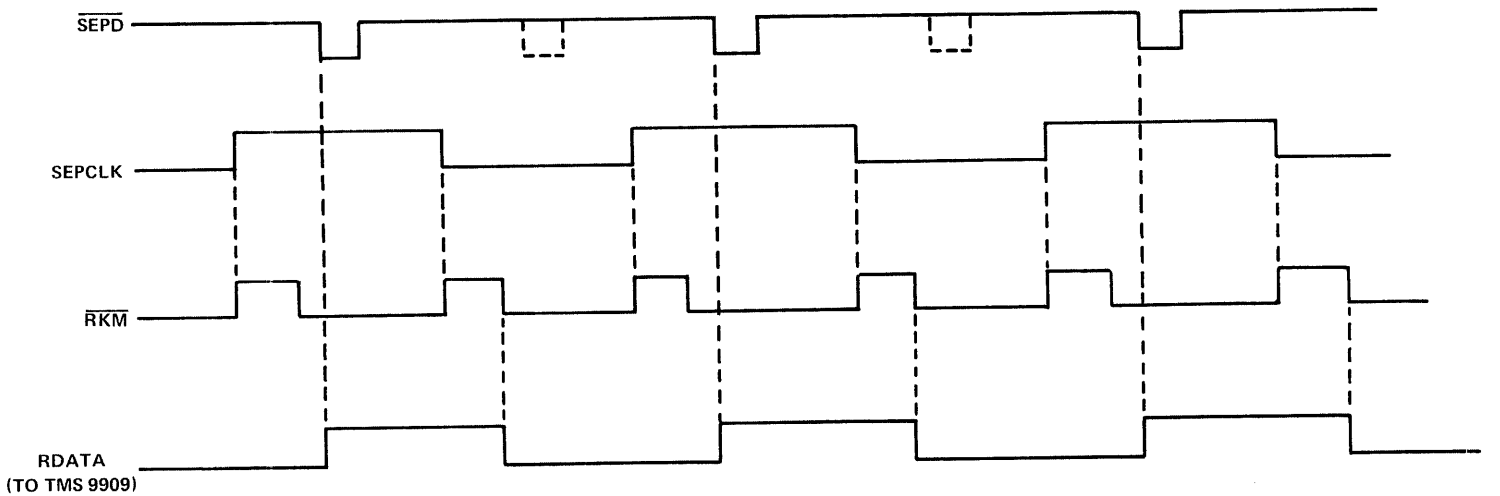


FIGURE A-3 — TYPICAL DATA SEPARATION CIRCUIT TIMING DIAGRAM
(8-INCH DOUBLE-DENSITY DISK)

A.4 DATA RATE SELECTION

In this circuit, selection of data rates is implemented by two signals: DDEN from the TMS9909, and ENABLE, a signal which must be generated by the user. With the TMS9909 correctly initialized (see Section 4.1 of the TMS9909 Data Manual), the DDEN signal identifies double-density data on 8-inch or 5 1/4-inch disks. For proper data rate selection, the ENABLE signal must be set to one in only two cases: 8-inch single-density and 5 1/4-inch double-density data. Table A-1 summarizes the ENABLE signal states for each data rate.

TABLE A-1 — ENABLE SIGNAL STATES FOR DATA RATE SELECTION

DATA RATE	ENABLE
8-inch double density	0
8-inch single density	1
5 1/4-inch double density	1
5 1/4-inch single density	0

If all four disk types are not implemented in a system, various other configurations may be used for data rate selection. For example, if only 8-inch disks are being used, the NOR gate may be omitted and an inverter added for DDEN. DDEN is then connected to CD0 with CD1 grounded. In addition, CD1 and CD0, which are the data rate control signals, may be made jumper-selectable or hard-wired if only one data rate is implemented. Table A-2 summarizes the data rate selection control signals.

TABLE A-2 — DATA RATE SELECTION CONTROL SIGNALS

DATA RATE	CD1	CD0
8-inch double density	0	0
8-inch single density	0	1
5 1/4-inch double density	0	1
5 1/4-inch single density	1	0

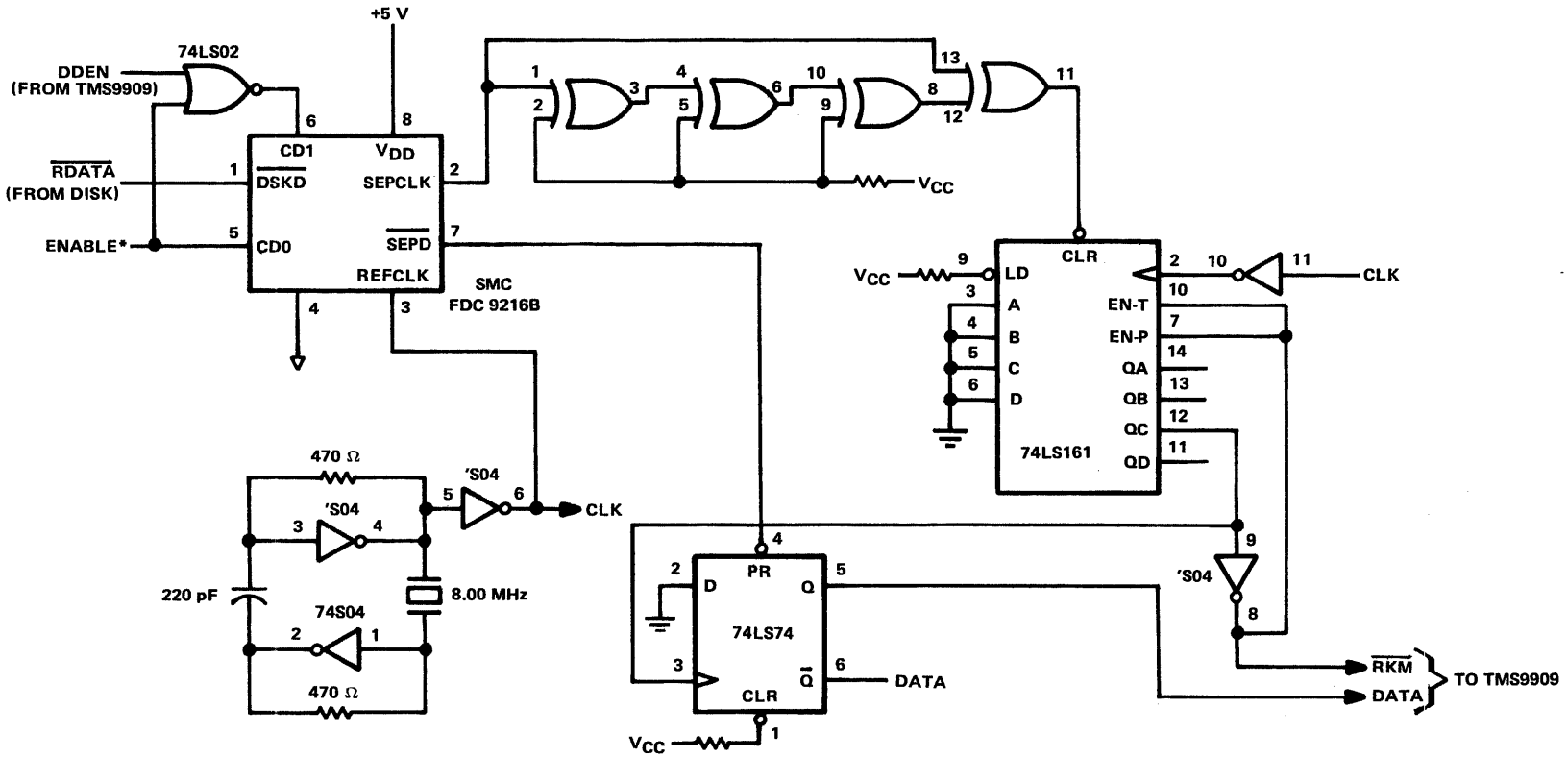
A.5 CIRCUIT PERFORMANCE

Performance of the data separator circuit was evaluated by continuously reading data from a disk and noting the number of errors which occurred during a given time period. The circuit produced overall system error rates in the neighborhood of one-data-bit error rate for each ten-to-the-ninth data bits read. This error rate has been recommended as a desirable target value by disk drive manufacturers.

The $\overline{\text{RKM}}$ pulse width is determined by the resistor/capacitor connections to the 74LS221. Although this pulse width may vary within the range of 300 to 500 ns, optimum data separator performance was achieved with a pulse width of 375 ns. The appropriate resistor/capacitor values and their tolerances are given in Figure A-2. Note that a variable resistor may be used to trim the $\overline{\text{RKM}}$ pulse width to 375 ns.

It is assumed that the data input waveform is compatible with TTL specifications. A Schmitt trigger buffer may be used to obtain a clean wave from the disk drive. It should also be understood that most disk drives require pull-up resistors on their interface signals.

This circuit was designed to minimize chip count and maximize chip usage. A more efficient incorporation of this data separator into a system's circuitry may be achieved by substituting inverters for the oscillator or omitting the oscillator and supplying an 8 MHz signal. Also, for applications where a one-shot design may be undesirable, a variation of this circuit is shown in Figure A-4. The error rates for this alternate circuit are comparable to those of the basic circuit.



* The enable signal should be set by the user ONLY for 8-inch single-density and 5¼-inch double-density disks.

NOTE: TI cannot assume responsibility for any circuits shown or present that they are free from patent infringement.

FIGURE A-4 – ALTERNATE DATA SEPARATOR CIRCUIT EXAMPLE

A.6 OTHER DATA SEPARATION APPROACHES

A number of other data separation approaches exist, each with their own various trade-offs. These approaches include analog PLL IC techniques, circuits using VCO ICs (such as the SN74LS624) to implement a PLL and digital PLLs. Users with expertise in these areas may implement alternate data separator designs.

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Printed in U.S.A.

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December 1982
MP007

Post Office Box 1443 / Houston, Texas 77001
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Printed in U.S.A.