VISUAL 100 AND VISUAL 400

VIDEO DISPLAY TERMINAL
MAINTENANCE MANUAL

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SAFETY WARNING

Hazardous voltages 115, 220 VAC and 15 KV DC are present when the terminal is on, and may remain after power is removed. Use caution when working on internal circuits, and do not work alone.

When handling the cathode ray tube caution is required as the internal phosphor is toxic. Safety goggles and gloves must be used whenever the CRT tube is handled. Should the tube break, skin or eyes exposed to the phosphor, rinse the affected area with cold water and consult a physician.

This terminal is supplied with a cord set which includes a safety ground. Do not use this terminal with an ungrounded outlet, missing ground pin, or use any adaptor which will defeat the safety ground.

Insure that power is turned off before connecting or disconnecting the keyboard cable.

This manual is published and distributed by Visual Technology Inc. Every effort has been exercised to insure its accuracy and completeness. The contents are subject to change without notice and this manual may not reflect the latest changes. Consult the sales department for latest changes.

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1. ARCHITECTURE

The Visual 100/400 is a microprocessor (Z80) based terminal composed of SSI and MSI logic elements. The communications receiver, the printer interface transmitter, (USARTS), and the video refresh are interrupt driven. The video refresh utilizes a DMA cycle in order to minimize processor overhead.

Program memory consists of a maximum of 128K bits of either PROM or ROM memory organized in 8-2K x 8 devices or 4-4K x 8 devices or 2-8K x 8 devices.

RAM memory is organized into two groups. A video buffer RAM provides 256 x 12 bits of memory which is used as a refresh buffer between main data RAM and the screen. Up to 8K x 8 RAM is provided for main memory and is organized as follows; 4K x 8 data memory, 4K x 4 character attributes, and 1K x 4 printer buffer.

A non-volatile RAM (100 x 14) is provided to store SET-UP parameters.

All timing is derived from crystal oscillators. Each frame is refreshed at a 50 or 60 Hz rate in an overlapped manner rather than an interlaced scan. This provides all of the video information required and allows refresh to occur twice as often as compared with television, resulting in reduced flicker while allowing the use of faster, brighter phosphor.

Each character is created by a dot matrix as follows; 80 character mode has a 10 x 10 field in which upper-case characters are 8 x 7 and lower-case characters are 8 x 9, 132 character mode has a 9 x 10 field in which upper-case characters are 8 x 7 and lower-case characters are 8 x 9. While 80 (132) characters are displayed on each line, the timing allows 102 (170) character times per line including Horizontal Sync. timing, resulting in the display being centered horizontally on the screen.

Vertically, each frame consists of 24 lines, each 10 raster lines tall. While this requires 240 (216 in 132 mode) raster lines, the Visual 100 generates 260 lines (60 Hz) or 312 (50 Hz) to center the display vertically and to provide proper synchronizing with the power line frequency. The following calculations describe the above relationships:

80 character 60 Hz mode

60 Hz (10 dots/character) (102 characters/line) (260 lines/frame) (3) = 47.736 MHz

80 character 50 Hz mode

50 Hz (10 dots/character) (102 characters/line) (312 lines/frame) (3) = 47.736 MHz

132 character 60 Hz mode

60 Hz (9 dots/character) (170 characters/line) (260 lines/frame) (2) = 47.736 MHz

132 character 50 Hz mode

50 Hz (9 dots/character) (170 characters/line) (312 lines/frame) (2) = 47.736 MHz

The Visual 400 differs from the Visual 100 hardware in that RAM memory is a full 8K x 8, the optional character generator ROM/PROM is present, and an expanded keyboard is present. The Visual 400 firmware and functionality is totally different from the Visual 100 (see the appropriate users manual).

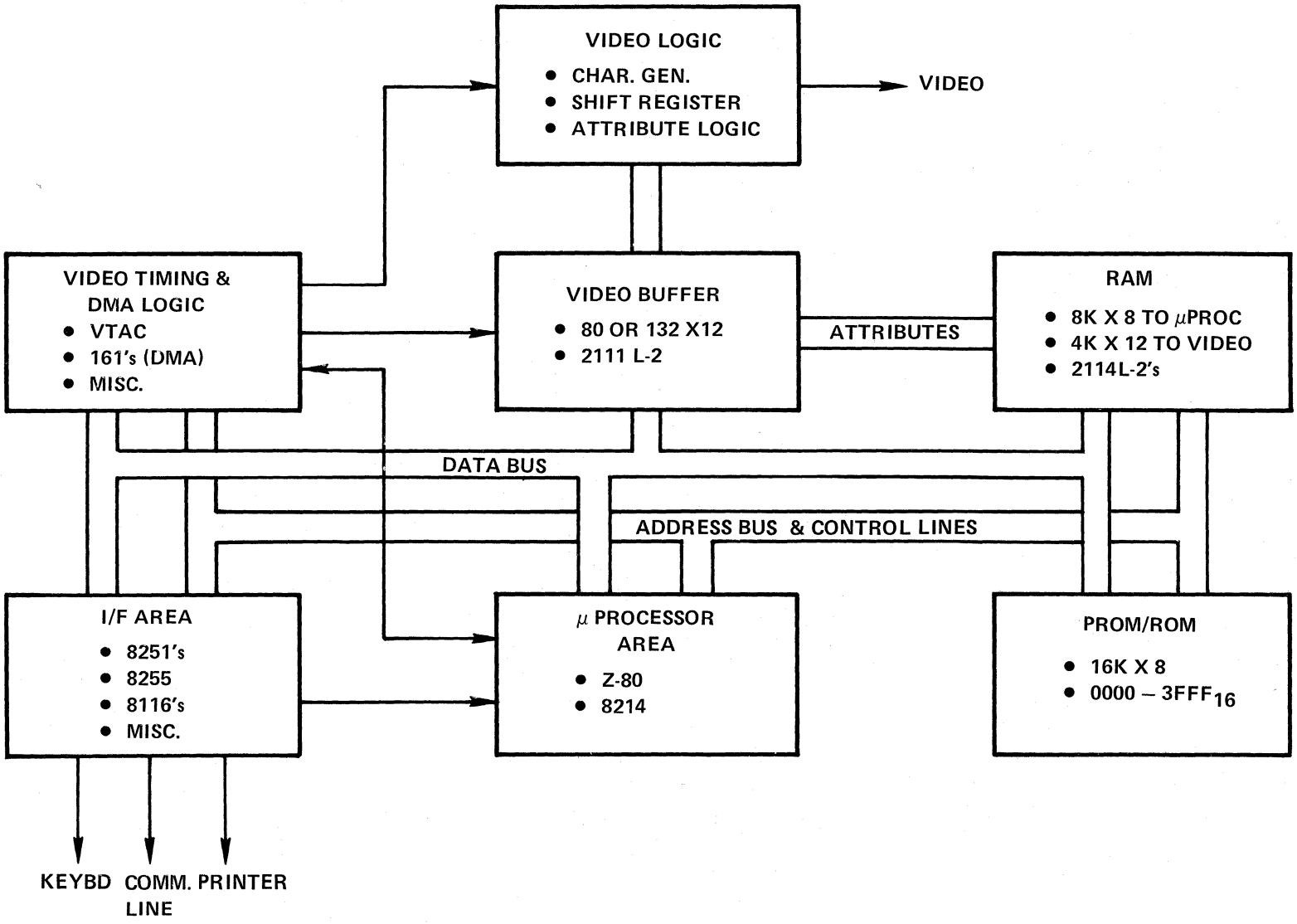


Figure 1-1 Block Diagram

2. THEORY OF OPERATION

The Visual 100/400 electronics are located on three circuit boards; TV monitor electronics, Power Supply, and Logic. The logic PCB is organized in columns of IC's designated by a U number. These IC's are numbered sequentially starting in the top left corner and proceeding from top to bottom and from left to right. The schematic diagrams contained in this manual utilize this numbering system which eliminates the need for a parts location diagram.

2.1 MASTER TIMING AND VIDEO REFRESH TIMING

Sheet 1 of the schematics contains the crystal oscillator operating at 47.736 MHz which provides all timing except for data rates. This clock is divided by 2 and then by 10 to form the processor clock (PCLOCK) at 2.387 MHz. The crystal oscillator is also divided by 3 (80 character mode) or 2 (132 character mode) using flops U11 to form CK. CK is divided by 10 (80 character mode) or 9 (132 character mode) to form the character clocks (DCA,DCB, DCC,DCD,DCE). These character clocks represent the number of dot spaces for each character.

2.2 DATA RATE TIMING

Sheet 7 of the schematics contains the data rate crystal oscillator. Y2 operating at 1.8432 MHz is divided by the baud rate generators U84 and U83 to provide outputs at pins 17 and 3 which are 16 times the programmed data rate. U84 pin 3 provides the transmit clock to the communications interface. U84 pin 17 is the communications receive clock. U83, when present, provides the data rate clock to the printer interface.

2.3 MICROPROCESSOR OPERATION

On sheet 7 of the schematics, the microprocessor (Z80) is shown as chip U53. The Z80 generates 16 bits of address (AB$\emptyset$ – AB15) for all operations except during the DMA cycle. These addresses are decoded by decoders to determine memory or device addresses.

The microprocessor operates normally via the I/O bus except during DMA cycles when it is disconnected from both the address bus and data bus. The Z80 also accepts and processes interrupts, operating in mode 2 (vectored Interrupt).

In the vectored interrupt mode, the Z80 detects an interrupt on its maskable interrupt input (INT) and transfers the contents of its I register to the high order eight bits of the address bus and transfers the low order seven bits (bit $\emptyset$ – 6) from the interrupting device via the data bus (DB) to the low order bits of the address bus, thus forming a data memory address from which two bytes will be extracted which point to the appropriate interrupt servicing routine. The vector address is created by chip U72 (sheet 7) as a result of a receiver interrupt (RCVI), printer interrupt (PIPT), video interrupt (VIDIPT), bell interrupt, or one of three optional interrupts which are reserved for future use (OI1, OI2, OI3).

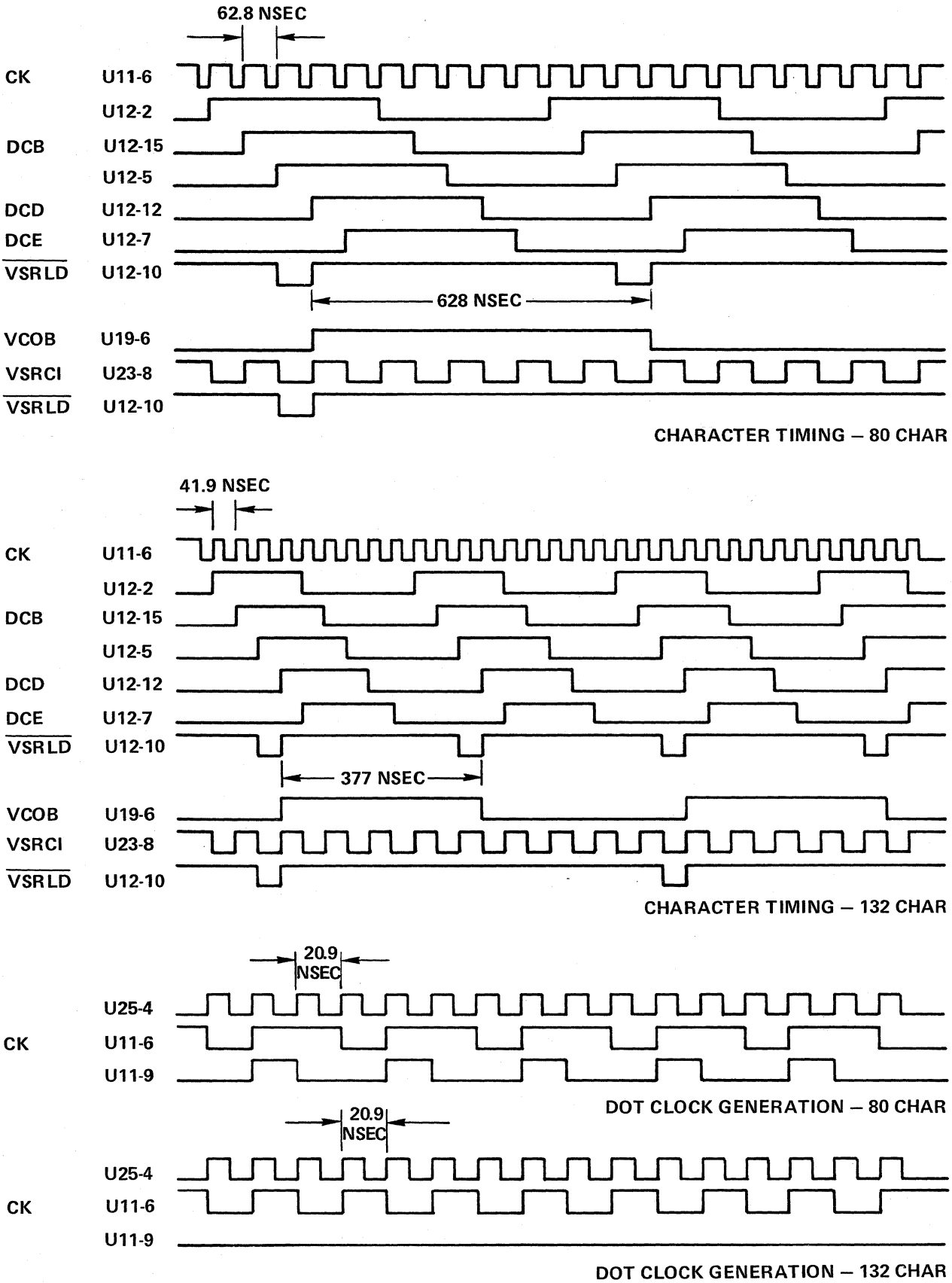


Figure 2-1 Character and Dot Timing

2.4 MEMORY ADDRESS DECODING

The program memory address is decoded on sheet 8 by chip U98. The decoding is affected by jumpers W1 through W6. These are selectively installed depending upon the size of the ROMS or PROMS used in locations U108 through U115. The table at the top of sheet 8 details the device size and jumper configuration.

The data memory address is decoded on sheet 6 by chips U77 and U90. U77 pin 11 decodes address 4XXX hex, while U77 pin 10 decodes address 5XXX hex. Chip U90 decodes the next most significant digit of address. The following table details the addresses for each RAM.

I/O Address	RAMS Enabled
4000 – 43FF	U99,U91
4400 – 47FF	U100,U92
4800 – 4BFF	U101,U93
4C00 – 4FFF	U102,U94
5000 – 53FF	U71,U82
5400 – 57FF	U70,U81
5800 – 5BFF	U69,U80
5C00 – 5FFF	U68,U79

RAMS U80 through U82 are not normally present, and U79 is present only when the printer interface is installed.

Figure 2-2 RAM Addressing

Gates U89 modify the address of RAMS U68 through U71 and U79 through U82 during a DMA cycle. DBAK causes these RAMS to be addressed using the 4XXX address at the same time as RAMS U91 through U94 and U99 through U102 are selected. This allows extraction of not only data to be presented to the screen, but also allows extraction of the character attributes which are associated with this data. The configuration which results has the ASCII code for a display character located at an address in the 4XXX bank while its attribute is located at the same address in the 5XXX bank. The attributes thus located are BLINK, UNDERLINE, REVERSE CHARACTER, and BOLD (AT0, AT1, AT2, and AT3 respectively).

2.5 DEVICE ADDRESS DECODING

Chips U55 and U56 on sheet 7 decode the device addresses for I/O operation.

Address	Mnemonic	Description
00–0F	SVTAC	Select VTAC
10–11		Set Communications Baud Rate
12 – 13	SSIO	Select Communications USART
14 – 15	SOSIO	Select Printer USART
16 – 17		Set Printer Baud Rate

Address	Mnemonic	Description
2X	RSTAT	Read Status
3X		Not Used
4Ø		Read Keyboard Data
4Ø–47	Scan Strobe	Write Keyboard Scan
48	Status Strobe	Write Keyboard LED's
5X		Not Used
6X	SIL	Set Interrupt Level
7X	SPIO	Select PIO

Figure 2-3 Device Addressing

2.5.1 Keyboard Operation

The Visual 100/400 uses a capacitive scan keyboard which is arbitrarily encoded. This allows language variation merely by altering keycaps. The V100 firmware assigns the appropriate ASCII code to the detected key. Operation of the keyboard is initiated by the Z80 sending a matrix address (4Ø – 47) via the scan strobe (sheet 7). Referring to the keyboard schematic, 65-02131, this address is loaded into Z2 and selects one of the vertical matrix lines. Any and all of the keys along this matrix line is loaded into the detector chip Z1. When the Z80 reads address 4Ø hex, this keyboard data is stored in chip U63 (sheet 7) and read on the data bus. At the time this data is read, Latch Reset is also generated which will reset the keyboard detector chip. In a similar manner, each vertical matrix line is selected and keys are detected. The firmware reads a given key on four consecutive scans before it determines validity and generates the code for that key. Status Strobe (48 hex) together with its data bus bits are sent to keyboard to light the keyboard LED's and ring the bell.

2.5.2 PIO

The parallel input output chip (PIO) on sheet 9 of the schematics, provides three eight bit channels operated in the output mode. Five bits of channel A (DTAØ – DTA4) are used to determine the screen intensity. One bit of channel A (S8Ø) alters the main timing chain for 80 or 132 character modes. One bit of channel A (VIDENB) inhibits video from reaching the screen; one bit of channel A (PREV) selects screen presentation, Reversed or Normal. Note that the character attribute REVERSE operates in addition to the screen REVERSE. (A reversed character within a reversed screen appears as normal video).

Channel B of the PIO provides the scroll control count (SCCØ–SCC3) which is used to control smooth scroll and determines the scrolling region, when enabled. Three bits of channel B (NVC1 – NVC3) are used to select the operating mode of the non-volatile RAM. The last bit of channel B (BLKCUR) determines the appearance of the cursor (block or underscore).

Two bits of channel C (NVCK,NVDO), provide the clock and data to the non-volatile RAM. Three bits (RDE,LDE,TXDE) provide control for the communications interface. RDE enables receive data between the level shifters and the USART. LDE enables transmit data into the receiver for local operation and for Local Echo operation when On Line. TXDE enables the communications USART output data to reach the EIA and Current Loop level shifters.

SPDS, another channel C output, drives pin 23 of the EIA interface, providing speed selection when a modem, so equipped, is attached. One bit of channel C (SCRTS) provides secondary channel Request-to-Send signal on pin 11 or 19 of the EIA interface for use by modems having the secondary channel capability. The last bit of channel C (ACTS) enables received Clear-to-Send signal to be detected.

2.5.3 VTAC

The video timing and control chip, U32 sheet 2, provides all of the basic timing for the TV monitor. Beside generating horizontal sync. (HSYNC pin 15), vertical sync. (VSYNC pin 11) and composite sync. (CSYNC pin 10), it also provides an output defining the current character line (pins 26 – 30), the current raster line (slice) within the character line (pins 4,5,7 and 8), the current character count within the present line (VCØ– VC7), present cursor position (pin 16) and a blanking signal (pin 17) which is used to blank the screen outside 80 or 132 characters horizontally and outside of the 24 lines vertically.

The VTAC is initialized immediately after the completion of self test and after each time the terminal is reset. Switching between 80 and 132 character modes also causes the VTAC to be reinitialized. The following addresses (low order byte) are decoded within the VTAC and are used for the functions indicated.

Address	Function
ØØ	Load Register Ø
Ø1	Load Register 1
Ø2	Load Register 2
Ø3	Load Register 3
Ø4	Load Register 4
Ø5	Load Register 5
Ø6	Load Register 6
Ø7	Initialize, Start Command
Ø8	Not Used
Ø9	Not Used
ØA	Reset VTAC
ØB	Not Used
ØC	Load Cursor Character Address
ØD	Load Cursor Line Address
ØE	Start VTAC Command
ØF	Not Used

During initialize, registers Ø through 6 are set to the operating parameters as follows:

Figure 2-4 VTAC Addressing

Register	Mode	60 Hz Value	50 Hz Value	Description
Ø	8Ø	65	65	Horiz. line count 1Ø2 Char.
Ø	132	A9	A9	Horiz. line count 17Ø Char.
1	8Ø	4B	4B	Non-interlace, Hsync, width 8
1	132	7B	7B	Non-interlace, Hsync, width 15
2	8Ø	4D	4D	1Ø scans, 8Ø characters/row
2	132	4F	4F	9 scans, 132 characters/row
3	8Ø	17	17	24 lines per frame
3	132	17	17	24 lines per frame
4	8Ø	Ø2	1C	260 (60 Hz) 312 (50 Hz) raster lines/frame
4	132	Ø2	1C	260 (60 Hz) 312 (50 Hz) raster lines/frame
5	8Ø	1Ø	2A	Vsync delay 16 lines (60 Hz) 42 lines (50 Hz)
5	132	1Ø	2A	Vsync delay 16 lines (60 Hz) 42 lines (50 Hz)
6	8Ø	17	17	Last line is 24
6	132	17	17	Last line is 24

Figure 2-5 VTAC Initialize Values

2.5.4 USARTS

The Visual 100/400 utilizes two Universal Synchronous, Asynchronous Receiver Transmitter chips, one for the communications channel, and the other for the printer interface. The USART converts parallel data to serial for transmission, and converts serial data to parallel for receive. It appends start, stop, and parity bits to transmitted data and checks received data for presence and significance of these bits. The USART also generates modem control signals Request-to-Send (RTS), Data-Terminal-Ready (DTR), and is used to detect modem originated signals Clear-to-Send (CTS), and Data-Set-Ready (DSR). The USART also generates an interrupt, which can be enabled when the receiver has received a character, and/or when the transmitter has finished sending a character. The data rate at which the receiver and transmitter operate is determined by the baud rate generator which operates at 16 times the baud rate selected. Schematic sheet 7 contains both data rate generators and both USARTS.

2.5.5 Communications Interfaces

Sheet 9 of the schematic diagrams contains the logic for the EIA and current loop receivers and transmitters. U86 and U106 convert the RS232 level signals for both data and control signals to TTL levels. Note that the modem control signals, CD,CTS,SCCD,DSR, and RI have pull-up resistors connected to the nodes of their receivers. These resistors shift the RS 232 threshold from ±3 volts to +2 volts and –4 volts. This causes control signals not supplied by the modem (floating) to be detected as true. It is, as a result, not necessary to jumper the EIA cable in order to force nonexisting control signals. Normally this threshold

shift presents no problems, as most interfaces operate with voltages significantly removed from the minimums (typically ±12 volts). Should an interface be encountered where signal levels are at the RS 232 minimums, the threshold of the receivers used, may be shifted back to standard levels by disconnecting the node pull-up resistor.

Transmitted EIA signals are generated by U96 and U116. These drivers generate ±12 volt signals.

Received current loop data is converted by the optical isolator U74. Receive threshold is set to approximately 9 ma., yet the receiver is designed to receive data up to 50 ma. Q6 shunts current above 20 ma. away from the MCT-2, preventing saturation at higher currents. Note that the output of the MCT-2 (U74) is coupled through switch U73-2 to the EIA receive input. EIA and current loop receivers can not be used simultaneously. Transmit data is converted to EIA levels (U96) and to current loop levels (U75) simultaneously. Q4, Q5, and CR8 provides 50 ma. sinking capability on the current loop transmit output. Switch U73 provides selection between EIA and Current Loop interfaces, and selects active or passive current loop operation. Active current loop operation causes the terminal to supply the source of the current, while in passive mode the source of the current is external to the terminal.

Switch	Function On	Function Off
U73-1	Alternate Character Generator PROM/ROM installed	Alternate Character Generator PROM/ROM not installed
U73-2	Current Loop Mode	EIA Mode
U73-3	Passive Current Loop Receiver	Active Current Loop Receiver
U73-4	Active Current Loop Receiver	Passive Current Loop Receiver
U73-5	Passive Current Loop Transmitter	Active Current Loop Transmitter
U73-6	Active Current Loop Transmitter	Passive Current Loop Transmitter
U73-7	EIA pin 19 is Secondary Request-to-Send	EIA pin 19 is not Secondary Request-to-Send
U73-8	EIA pin 11 is Secondary Request-to-Send	EIA pin 11 is not Secondary Request-to-Send

Figure 2-6 Communications Switch

2.5.6 Printer Interface

Sheet 9 details the printer port EIA level shifters, U116 and U106. These IC's are installed only when the printer interface is present. Connector J5 is the rear panel connector. J4 is an internal PCB edge connector reserved for future use. Note that the printer interface is limited to EIA levels only and that the interface responds to a printer busy signal at EIA levels on connector pin 4.

2.6 NON-VOLATILE RAM

U45 shown on sheet 8 is the non-volatile RAM which is used to maintain SET-UP parameters when the terminal is disconnected from power. U33, a DC to DC converter uses +5 volts to generate −23 volts used by the NV RAM. The PIO provides the clock (NVCK),

data (NVDO), and mode control (NVC1 – NVC4). Data is loaded into and read from pin 12 of the NV RAM under control of the control of the three control lines detailed below. U47 shifts read data from Ø and +12 volts to TTL levels.

Function	NVC1	NVC2	NVC3
Standby	Ø	Ø	Ø
Address Enable	Ø	1	1
Read Address	1	Ø	Ø
Shift Data Out	1	Ø	1
Erase Data	Ø	1	Ø
Accept Data	1	1	1
Write Data	1	1	Ø
Not Used	Ø	Ø	1

Figure 2-7 Non-Volatile RAM Controls

2.7 DMA

The DMA cycle is initiated at the beginning of each slice Ø (the start of each character line display) by flop U17 pin 5, on sheet 2. BUSRQ (bus request) is generated for each line unless inhibited by U17 pin 8. This inhibit is set after the DMA cycle begins for line 23 (last line) and is reset after vertical reset. The VTAC remains at a line count of 23 during vertical retrace, and would normally cause several DMA cycles serving no purpose. BUSRQ is presented to the Z80 which will relinquish the address and data buses at the end of the current instruction and acknowledges this by generating BUSAK (bus acknowledge).

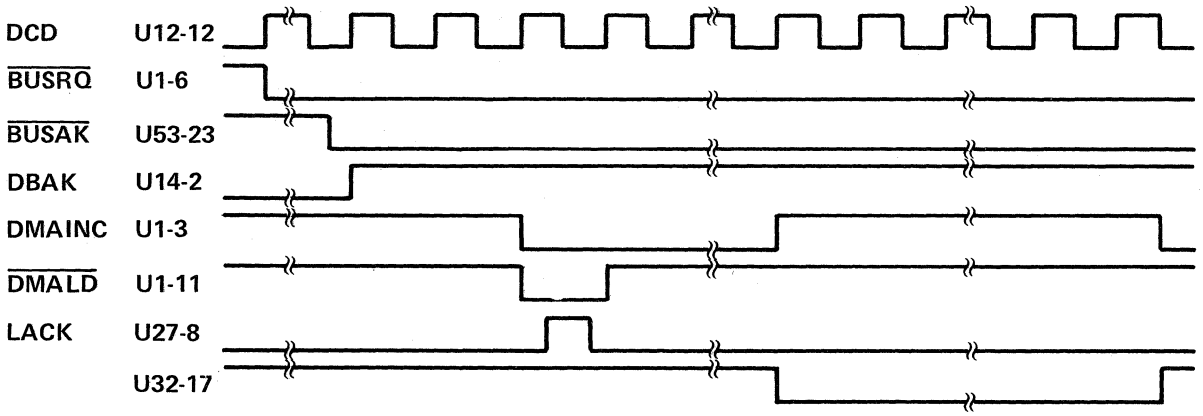


Figure 2-8 DMA Timing Diagram

Upon receiving BUSAK, DBAK is generated and the DMA cycle begins. Referring to the timing diagram for the DMA cycle in figure 2-8 and the U14 flops on sheet 2 of the schematics you will note that two DCD clocks occur before DMAINC (DMA increment) becomes active. The DCD clocks cause a video shift register load command (VSRLD) sheet 1, which causes the first byte of data to be loaded into chips U31 and U38 on sheet 3. The second DCD and VSRLD causes the contents of U31 and U38 to be transferred to U30 and U39. At the same time a second byte is loaded into U31 and U38. The output of these two sets of registers VDØ-ACGR and RBØ-RB7 now contain a pointer to the location where the data to be displayed on this line of the screen is stored in RAM. On sheet 5, these two bytes of information are loaded into chips U51, U50, U52, through U60, U59, and U61 create the address of the data location. Line attribute clock (LACK), sheet 2, is generated at the same time. A delay, indicated by the blanking signal from the VTAC (U32-17), inhibits DMA increments (DMAINC) and data transfers until the character counter (VCØ-VC7) gets to zero. Each character time hereafter, the address registers are incremented, the VTAC advances the character count (VCØ-VC7) and causes data read from RAM to be stored in the DMA buffers U43, U42, and U41 on sheet 3. This operation continues until the VTAC reaches 8Ø or 132 characters and generates the blanking signal which inhibits gate U1 on sheet 2 and causes DMAINC to halt. DMAINC stopping, leaves the address register U51, U50, and U52 set to the location where the next DMA cycle will find the next pointer bytes. Immediately after video blanking occurs HSYNC occurs which resets the bus request flop (BUSRQ) on sheet 2. This ends the DMA cycle and allows the Z8Ø to return to normal operation.

At the end of display of the last line of the screen, VSYNC occurs which causes the DMA address register (U51, U50, and U52) to be reset so that the pointer for the first lines' data will again begin at 4ØØØ hex.

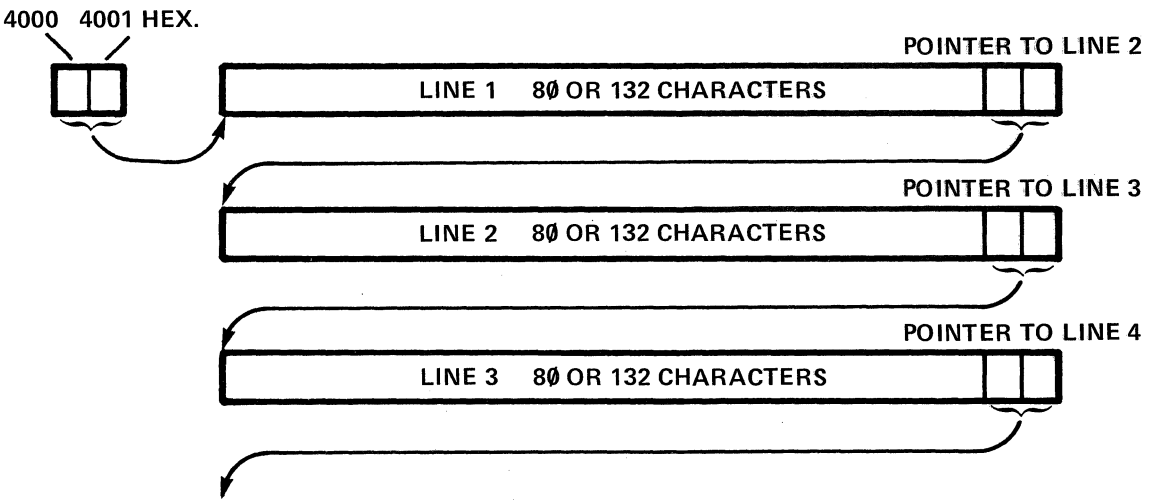


Figure 2-9 Memory Organization

The first byte of the pointer becomes the low order address for memory. The second byte contains two nibbles. The low order nibble is used for the next higher 4 bits of the memory address. The high order nibble is used to determine line attributes, Double Height, Double Width, Blanked, or Scroll.

2.8 SMOOTH SCROLL

Smooth scroll is accomplished by scrolling one raster line each frame refresh cycle. The multiplexer, U2Ø on sheet 5, provides control of scrolling for the entire screen or for that region used when a scrolling region is defined. When a line is extracted from memory during a DMA cycle which is within a scrolling region, U2Ø pin 1 is held at ground. This allows the SCCØ-SCC3 bits from the PIO to become the scroll counter bits (SCRØ-SCR3). The PIO counts from 6 to 15 (8Ø character mode) or 6 to 14 (132 character mode) each frame refresh cycle, and only for those lines within the scrolling region. Whenever lines are extracted that are not in the scrolling region, U2Ø pin 1 is switched high forcing the scroll counter bits to a fixed decimal value of 6. Whenever scrolling region is not enabled, the firmware treats each line as if it were within the region. If scrolling region is not enabled, then the scroll counter bits (SCRØ-SCR3) are counted by the PIO from 6 to 15 (8Ø character mode) each frame refresh cycle. This value is added to the slice counts from the VTAC by adder U8 on sheet 2. If the result of this addition is less than 15 (no carry), U7 adder will add 1Ø. When the first addition results in a carry, U7 adds Ø.

Assuming that a normal line is being processed (not a double height top line), multiplexer U6 passes this count unchanged. U5 added will add Ø if the current line is not the bottom half of a double height line, resulting in slice counts VSØ-VS3. These video slice counts address the character generator PROM/ROM together with the character code to locate the appropriate dot pattern. Figure 2-10 illustrates smooth scrolling during an 8Ø character line.

Scroll Counter (SCRØ-SCR3)	+	VTAC Slice (SCØ-SC3)	=	U8	+	U7	+	U6	+	U5	=	VSC	=	Effective Slice
6		Ø		6		1Ø		Ø		Ø		16		Ø
6		1		7		1Ø		Ø		Ø		17		1
6		2		8		1Ø		Ø		Ø		18		2
6		3		9		1Ø		Ø		Ø		19		3
6		4		1Ø		1Ø		Ø		Ø		2Ø		4
6		5		11		1Ø		Ø		Ø		21		5
6		6		12		1Ø		Ø		Ø		22		6
6		7		13		1Ø		Ø		Ø		23		7
6		8		14		1Ø		Ø		Ø		24		8
6		9		15		1Ø		Ø		Ø		25		9
This line is displayed in its normal position (SCX=Effective Slice)														
7		Ø		7		1Ø		Ø		Ø		17		1
7		1		8		1Ø		Ø		Ø		18		2
7		2		9		1Ø		Ø		Ø		19		3
7		3		1Ø		1Ø		Ø		Ø		2Ø		4
7		4		11		1Ø		Ø		Ø		21		5
7		5		12		1Ø		Ø		Ø		22		6
7		6		13		1Ø		Ø		Ø		23		7
7		7		14		1Ø		Ø		Ø		24		8
7		8		15		1Ø		Ø		Ø		25		9
7		9		Ø + carry		Ø		Ø		Ø		Ø		Ø
														Slice Ø of the next character line

Figure 2-10 Smooth Scroll

2.9 LINE ATTRIBUTES

U49 on sheet 5, stores the line attribute codes as each line is extracted during a DMA cycle. Scrolling Region (RB7), Logical Blanking (RB6), Double Width (DBW), Double Height Bottom (DHB), and Double Height (DHT) are decoded on sheet 5.

2.9.1 Scrolling Region

Scrolling Region is discussed above in section 2.8.

2.9.2 Logical Blanking

The Logical Blanking is used by the microprocessor to inhibit video display of selected lines. Typically this is used during the display of the SET-UP modes to insure that the blank areas of the screen remain blank.

2.9.3 Double Height

The double height bit is set for both the top and bottom half of a double height line. It is used to alter the slice counts by halving the number and doubling the use of each of these slices. DHT switches multiplexer U6 on sheet 2 so that each of the slice bits are shifted to the next lower bit of significance, resulting in doubling the time of each slice count. When the input to U6 is counts Ø and 1 the output will be Ø and Ø, 2 and 3 in results in 1 and 1 out. Slices 8 and 9 on the input results in slices 4 and 4 on the output. The output of U6 for a double height line, top or bottom half, is two slices each from Ø through 4.

2.9.4 Double Height Bottom

When the bottom half of a double height line is extracted during a DMA cycle, the slice counts, defined above for a double height line, are further modified by U5 on sheet 2. When double height bottom (DHB) is true, U5 adds 5 to the slice counts defined in section 2.9.3 resulting in the following sequence: 5,5,6,6,7,7,8,8,9,9.

2.9.5 Double Width

When a double width line is extracted from memory during a DMA cycle, DBW is set true (sheet 5). Double width modifies the main timing chain on sheet 1. The flop (VSCRI), U23 divides CK by 2 and creates an inhibit to the video shift register for every other CK, thereby doubling the time (width) of each dot. In addition, flop (VSRLD), U12, is set at character times Ø, 2, 4 etc. instead of each character time. This doubles the time that the character code associated dots are available to the video shift register, thereby doubling the width of each displayed character.

2.10 VIDEO

Once the character generator PROM/ROM has generated the dots for a character they must be modified as a result of screen reverse (PREV), character reverse video (RVID), blink (BLINK), and highlighted video (BOLD). Underline is treated similarly to the underscored cursor.

On sheet 4 of the schematics, gate U64 allows dots (VSRO) through whenever logical blanking (LBLANK) does not inhibit dots. If the cursor mode selected is underline (BLKCUR is false), a row of dots is forced at the cursor location (CURF) during slice 8 (SC8) by the top gate input of U64. Gate U57, output pin 3, creates the block cursor display (BLKCUR is true) by combining the cursor (DCUR) with the reversing inputs PREV and RVID. Because there is no slice count in this gating the cursor will appear as a block rather than an underline. RVID and PREV act so that the cursor is the opposite video as compared to the character. U64, dots, are exclusive or'd with this cursor by U57 pins 11 and 13. This results in the video, at the cursor location inhibiting the block if the block is white on black, or enabling video if the cursor is black on white, thereby allowing both the cursor and the character to be visible.

The two U48 flops form a video divider creating three levels of intensity, low, average, and high. The bold, reverse, and blink gating combine with the video so that the bold video is presented at the highest level. Normal data is presented at average video levels. Blink of normal data switches between average and low levels. Blink of bold data switches between bold and average levels. Q1 combines this video data with the composite sync. and provides a composite video output for an external monitor. Q2 provides video drive for the internal monitor.

2.10.1 Screen Intensity

On sheet 4 of the schematics, the internal video driver, Q2, has a ladder network attached to its collector. DTAØ— DTA4 signals, generated by the PIO, provide 32 intensity levels for the screen.

2.11 SELF TEST

Each time the terminal is turned on and each time it is reset a self test is initiated. A checksum is calculated for program memory and compared to a sum stored in the PROM/ROM. Should an error be detected the Z8Ø is halted. After passing the checksum test data RAM is tested, then the attribute RAM. Again the Z8Ø is halted whenever an error is detected. Upon completing the PROM/ROM and RAM tests the screen is initialized. The screen lacking intensity and cursor is an indication that self test has failed as in this case the VTAC is not started. Verification of a halted Z8Ø is available on pin 18 of the Z8Ø. Pin 18 will be ground only when the Z8Ø is halted.

After the VTAC is initialized, a check is performed on the non-volatile RAM. If the NVRAM is ok, stored parameters are utilized to define SET-UP parameters. If the NVRAM check detects an error, the bell is sounded 6 times and the firmware sets default values for SET-UP parameters. Operation of the terminal is permitted in this case, as the operator may alter these default parameters using the SET-UP modes.

The keyboard lights are used within the self test and can be used to determine the nature of the fault. The following chart illustrates the states of the LED's after the indicated fault has occurred.

Fault	LED Illuminated						
	Line	Local	Keyboard Lock	1	2	3	4
ROM		X					
RAM		X	X				
RAM, Attribute		X	X	X			
RAM, Printer		X	X		X		
*DATA	X				X		
*CONTROL	X			X			

*These two errors are described below.

Figure 2-11 Self Test Fault Indications

2.11.1 Communications Tests

When the terminal is placed in ANSI mode and either a Current Loop Turn-around Connector or an EIA Turn-around Connector is installed, the Visual 100 can execute its own test including data, control signals and data rates.

EIA Test – Install EIA Turn-around Connector (Pin 2 to 3, 4 to 8, and 6 to 20). Set DIP switches 1 through 7 OFF, 8 ON. Set terminal on line in ANSI mode (ESC <). Type ESC[2;14y. A repeating pattern will be displayed until either a failure is detected or the SET-UP key is depressed. If a data failure occurs the Line and 2 LED's will be illuminated. If a control signal error occurs, the Line and 1 LED's will be illuminated.

Current Loop Test – Install Current Loop Turn-around Connector (pins 7 to 17, and 18 to 25). Set DIP switches 2,3,6 ON, all others OFF. Set terminal on line in ANSI mode (ESC <). Type ESC[2;1Øy. The same repeating pattern will appear. Failure in this mode, (data) is indicated by the Line and 2 LED's being illuminated.

2.12 JUMPER ASSIGNMENTS

Nine jumpers are provided on the Visual 100 PCB to alter the configuration. Figure 2-12 details the location of these jumpers described below.

Jumpers W1-W6 are configured per the chart located on schematic sheet 8 as a function of the size of the PROM/ROM's installed in locations U108 through U115.

Jumper W7 connects DC ground to chassis ground. This jumper normally is not installed.

Jumper W8 is installed when the printer interface logic is not installed.

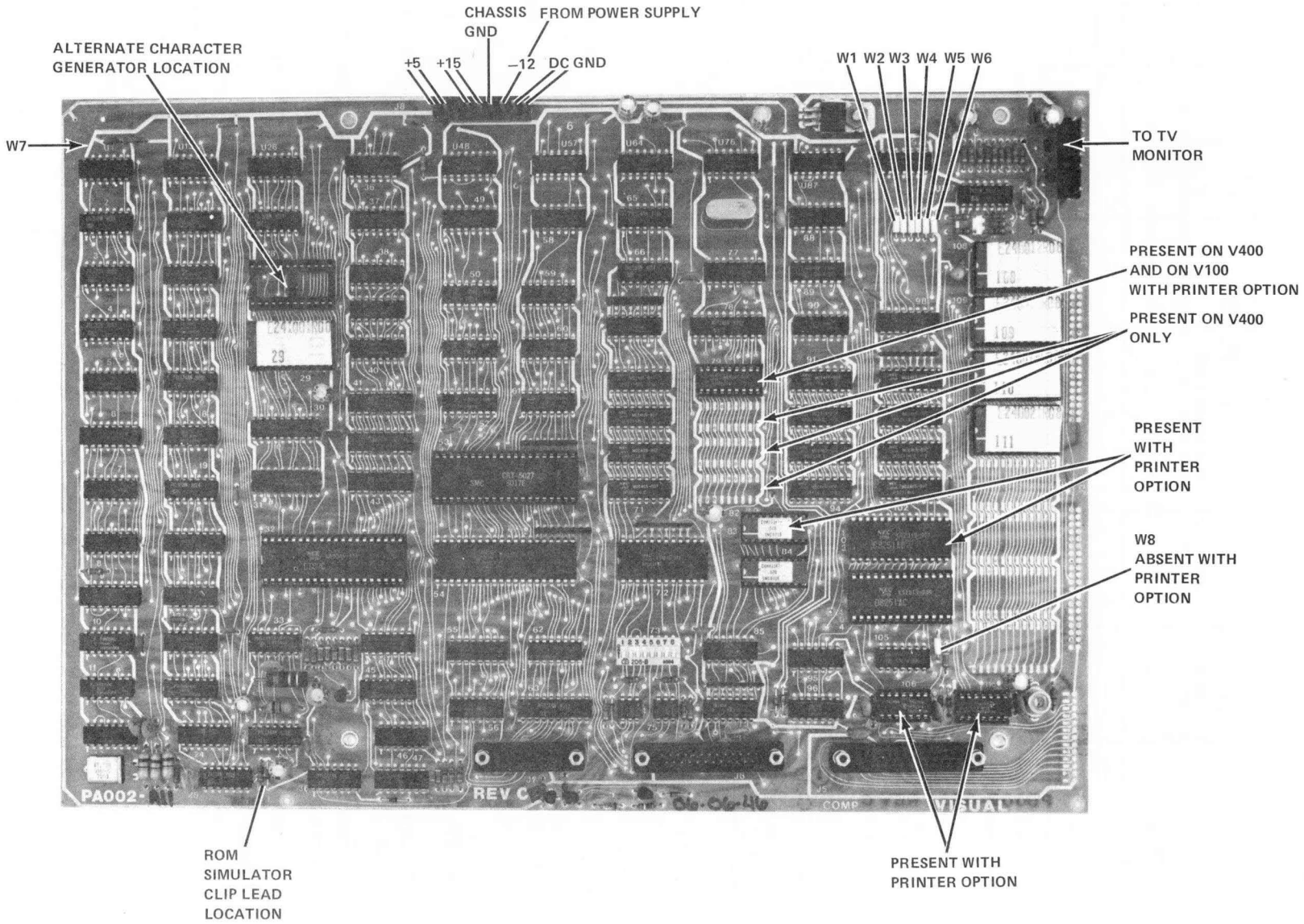


Figure 2-12 Jumper Location

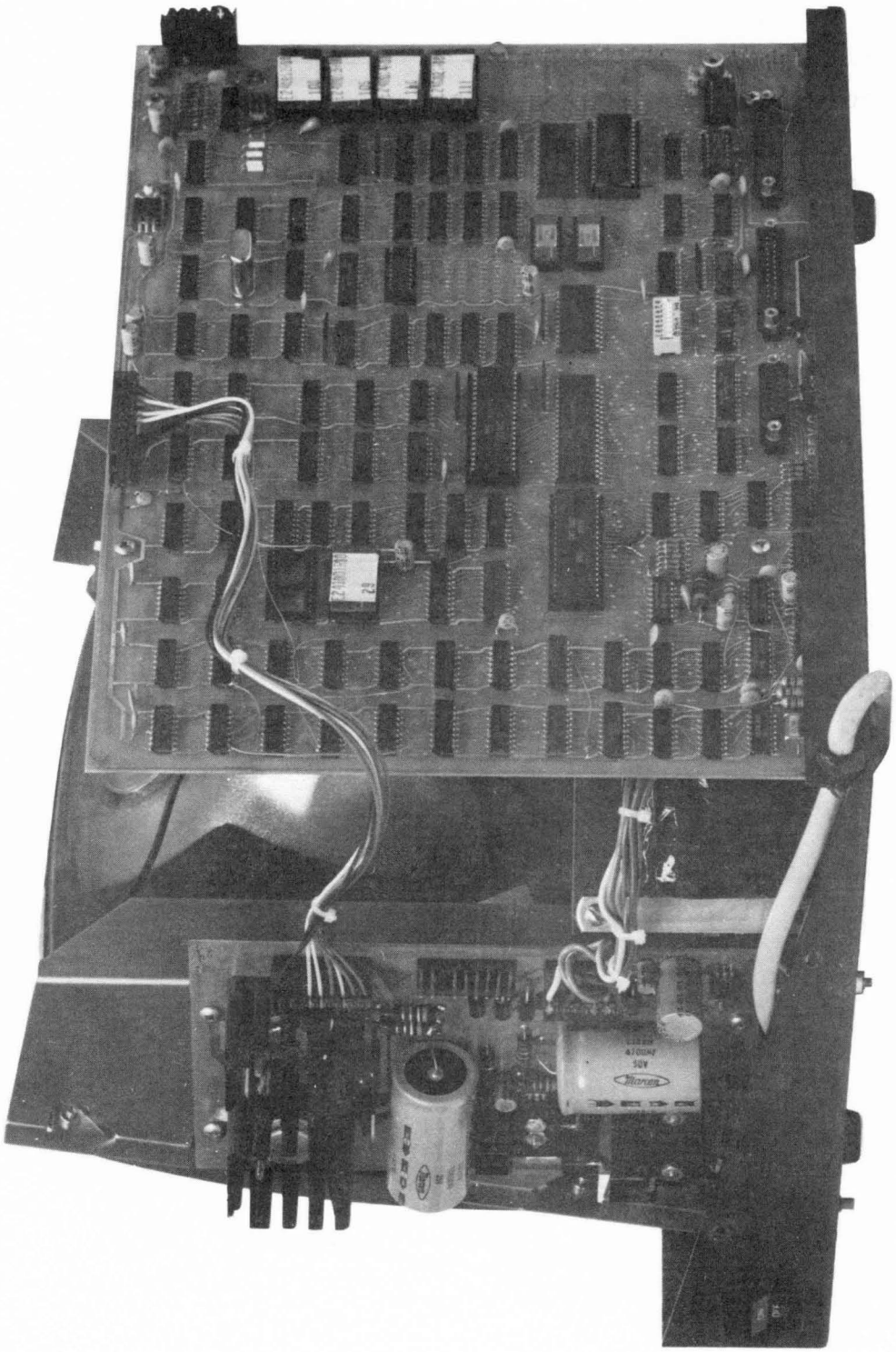


Figure 2-13

* Video Display Reference Manual UM-400-001-0B
$5.00

* keyswitches (includes spring)
- no part no. - $1.50

3. SPARE PARTS AND TOOLS

3.1 SPARE PARTS

Each Visual 100/400 terminal is composed of four major subassemblies and is designed to be serviced on site by replacing subassemblies only.

3.1.1 TV Monitor Subassembly

The Zenith model D 12 NK 21 monitor consists of the following subassemblies.

Description	Zenith P.N.	Visual P.N.
Monitor Kit (total)	D 12 NK 21	MN 002-000
PCB	A8046	MN 002-002
Flyback Transformer	A8438	MN 002-001
CRT & Yoke	F6348	MN 002-003
(CRT is Panasonic 310JLB4N)		

3.1.2 Keyboard Assembly

One keyboard is used on the Visual 100/400. It is manufactured by KTC and carries the following part numbers: KTC 65-2131-00, Visual KB ØØ2-ØØ1. The Visual 400 keyboard is part number KTC 65-2220-00, Visual KB ØØ3-001.

3.1.3 Power Supply Assembly

One power supply is used which has the Visual part number PA-ØØ3-AØ1, or PA-ØØ5-AØ1.

3.1.4 Main PCB (Visual 100)

The main PCB (PA ØØ2-AØ1) contains all logic except for character generator, firmware and printer logic. These must be additionally specified when ordering spare PCB's.

PROM/ROM	Location	Part Number
Character Generator	U29	IC or E 241-001
Firmware	U108	IC or E 240-012
Firmware	U109	IC or E 240-013
Firmware	U110	IC or E 240-014
Firmware	U111	IC or E 240-015*

The revision on all PROM/ROM's used as firmware must be the same.

*On early Visual 100 terminals the baud rate generator lacked 200 baud. As a result the baud rate generator(s) in location U83 and U84 must be matched with the firmware PROM/ROM U111, and the crystal Y2 as follows.

Crystal Freq.	BGR P.N.	PCB Assy No.	U111 PROM/ROM
5.0688 MHz	8116	A01	IC or E 240-015
1.8432 MHz	8116 – 020	A11	IC or E 240-021

3.1.4.1 Main PCB (Visual 400)

The main PCB (PA ØØ2 – A4Ø/A41) contains all logic except for character generators, firmware and printer logic. These must be additionally specified when ordering PCB's.

PROM/ROM	Location	Part Number
Character Generator	U28	IC or E 241-002
Character Generator	U29	IC or E 241-001
Firmware	U108	IC or E 240-040
Firmware	U109	IC or E 240-041
Firmware	U110	IC or E 240-042
Firmware	U111	IC or E 240-043
Firmware	U112	IC or E 240-044
Firmware	U113	IC or E 240-045
Firmware	U114	IC or E 240-046
Firmware	U115	IC or E 240-047

The revision on all PROM/ROM's used as firmware must be the same.

3.2 SPARE SUBASSEMBLY RECOMMENDATIONS

To service 1ØØ terminals by subassembly exchange, the following subassemblies should be stocked at the quantities indicated.

Quantity	Description	Part Number
5	Main PCB	PA 002-A01 (PA 002-A40 for V
3	Power Supply PCB	PA 003-A01
3	TV Monitor PCB	MN 002-002
3	Keyboard	KB 002-001 (KB 003-001 for V

3.2.1 Active Component Recommendations

The following list contains all active components found on the Main PCB, the Power Supply PCB, and on the Keyboard. Total quantities per terminal and recommended stocking levels are indicated. The recommendations are based on one depot repairing subassemblies from approximately 100 terminals. See Section 7 for TV Monitor components.

Part	Visual P.N.	Qty./Terminal	Recommended Spares
74LS00	IC 000-000	3	15
74LS02	IC 000-002	1	10
74LS04	IC 000-004	4	20
74LS08	IC 000-008	4	20
74LS32	IC 000-032	1	10
74LS51	IC 000-051	1	10
74LS74	IC 000-074	4	20
74LS83	IC 000-083	3	15

Part	Visual P.N.	Qty./Terminal	Recommended Spares
74LS93	IC 000-093	2	15
74LS138	IC 000-138	4	20
74LS139	IC 000-139	2	15
74LS161	IC 000-161	3	15
74LS174	IC 000-174	1	10
74LS175	IC 000-175	3	15
74LS245	IC 000-145	2	15
74LS257	IC 000-257	2	15
74LS273	IC 000-273	1	10
74LS367	IC 000-367	4	20
74LS368	IC 000-368	1	10
74LS374	IC 000-374	1	10
7416	IC 010-016	1	10
7426	IC 010-026	2	15
74166	IC 010-166	1	10
74196	IC 010-196	1	10
74S00	IC 020-000	3	15
74S02	IC 020-002	1	10
74S04	IC 020-004	1	10
74S10	IC 020-010	1	10
74S64	IC 020-064	1	10
74S74	IC 020-074	4	20
74S86	IC 020-086	2	15
74S174	IC 020-174	1	10
74S175	IC 020-175	2	15
1488	IC 340-001	2	15
1489	IC 340-002	2	15
Z80(UPD 780)	IC 440-001	1	10
PIO(UPD 8255)	IC 440-002	1	10
VTAC(CRT5037)	IC 440-004	1	10
USART(UPD 8251)	IC 440-005	2	15
8214	IC 440-006	1	10
MCT-2	IC 340-004	2	15
2111A-2	IC 140-003	3	15
2114L-2	IC 140-004	12 (16 for V400)	30 (40 for V400)
ER1400	IC 248-001	1	10
TL479	IC 340-006	1	10
LM339	IC 340-007	1	10
1N914	DA 000-001	10	30
1N5401	DA 320-001	4	20
CR1	DA 350-001	4	20
MCL1301	DA 440-001	1	10
2N4901	TR 010-001	1	10
TIP32	TR 020-001	1	10
TIP34	TR 030-001	2	15

PN3644	TR 000-001	3	15
MPSA05	TR 010-002	2	15
MPSA55	TR 000-012	1	10
7805	UR 100-005	1	10
7812	UR 000-012	1	10
7815	UR 000-015	1	10
7912	UR 010-012	1	10
22-00950-003	KEYTRONIC	1	10
22-00908-003	KEYTRONIC	1	10
*8116	IC 340-004	2	10
*8116-020	IC 340-005	2	10

*Replace with whichever part was originally supplied.

3.3 TOOLS

In order to gain access to the Visual 100 and to replace any subassembly, only a cross-head and common blade screwdriver are required. The following listed tools, or their equivalent, are recommended for depot level where subassemblies are repaired.

Qty.	Description	Manufacturer	Part Number
1	Oscilloscope 30 MHz	Tektronix	465
1	Romaid 2700 ROM Simulator with 716 Personality Module	Microlink	2700-716
1	V100/V400 TEST PROM	Visual	V100TEST

4. TEST METHODS

Test procedures for use of the Romaid ROM Simulator and the V100 TEST PROM are included with the test PROM. This combination allows the depot to exercise the Z8Ø, P10, VTAC, USART, and memory.

5. MNEMONIC LIST

MNEMONIC LIST

Mnemonic	Source Chip	Source Schematic Page	Definition
ACGR	U30	3	Select Character Generator A
ACTS	U54	9	Auxiliary Clear-to-Send
ADBØ	U60 & U53	5 & 7	Address Bus Bit Ø
ATØ	U67	6	Attribute Bit Ø
$\overline{\text{BLANK V}}$	U16	2	Video Blanking
BLINK	U40	3	Blink Attribute
$\overline{\text{BLKCUR}}$	U54	9	Block Cursor
BOLD	U40	3	Bold Video Attribute
BTIME	U2	2	Blink Time
BUSAK	U53	7	Bus Acknowledge
BUSRQ	U1	2	Bus Request
CD	U86	9	Carrier Detect
CK	U11	1	Clock 23,868 MHz
COMP VIDEO	Q1	4	Composite Video Output
CSYNC	U18	2	Composite Sync.
CTS	U85	9	Clear-to-Send
CURF	U13	2	Cursor Flop
DATACK	U88	7	Data Clock
DBAK	U14	2	Data Bus Acknowledge
DBW	U22	5	Double Width
DBØ	Several	—	Data Bus Bit Ø
DCB	U25	1	Decoded Character Clock B
DCD	U12	1	Decoded Character Clock D
DCE	U12	1	Decoded Character Clock E
DCUR	U27	2	Decoded Cursor
DHB	U66	5	Double Height Bottom Half
DHT	U49	5	Double Height
DIRVID	Q2	4	Video Output to Internal Monitor
DMAINC	U1	2	DMA Increment
DMALD	U1	2	DMA Load
DSR	U86	9	Data Set Ready
DTAØ	U54	9	Display Amplitude (Screen-Intensity)
DTR	U103	7	Data Terminal Ready

MNEMONIC LIST (Continued)

Mnemonic	Source Chip	Source Schematic Page	Definition
HALT	U53	7	CPU Halted
HSY	U32	2	Horizontal Sync
HSYNC	U18	2	Horizontal Sync Buffered
INT	U35	7	Maskable Interrupt
IORQ	U53	7	I/O Request
$\overline{\text{KBPRES}}$	KBD	7	Keyboard Present
KDØ	U63	7	Keyboard Data Bit Ø
LACK	U27	2	Line Attribute Clock
LATCH RESET	U46	7	Keyboard Latch Reset
L BLANK	U49	5	Logical Blanking (Set-up)
LDE	U54	9	Local Data Enable
MREQ	U61 & U53	5 & 7	Memory Request
M1	U53	7	M1 CPU Cycle
NMI	U53	7	Non-maskable Interrupt
NVCK	U54	9	Non-volatile RAM Clock
NVC1	U54	9	Non-volatile RAM Control Bit 1
NVDI	U47	8	Non-volatile Data Input (To CPU)
NVDO	U54	9	Non-volatile Data Output
PBUSY	U106	9	Printer Busy
PCLOCK	U21	1	Processor Clock
PDTR	U104	7	Printer Data-Terminal-Ready
PIPT	U105	7	Printer Interrupt
PRD	U106	9	Printer Receive Data
PREV	U54	9	Page Reverse Video
PXD	U104	7	Printer Transmit Data
RBØ	U31	3	Rebuffered Memory Data (Video)
RCVI	U85	7	Receive Data Interrupt
RD	U61 & U53	5 & 7	Read
RDE	U54	9	Read Enable
RESET	U25	1	Initialize Reset
RFSH	U53	7	Refresh (Memory)
RI	U106	9	Ring Indicator
RSTAT	U55	7	Read Status
RTS	U103	7	Request-to-Send
RVID	U40	3	Reversed Video
RXD	U95	9	Received and Xmitted Data
S8Ø	U54	9	8Ø Character Mode

MNEMONIC LIST (Continued)

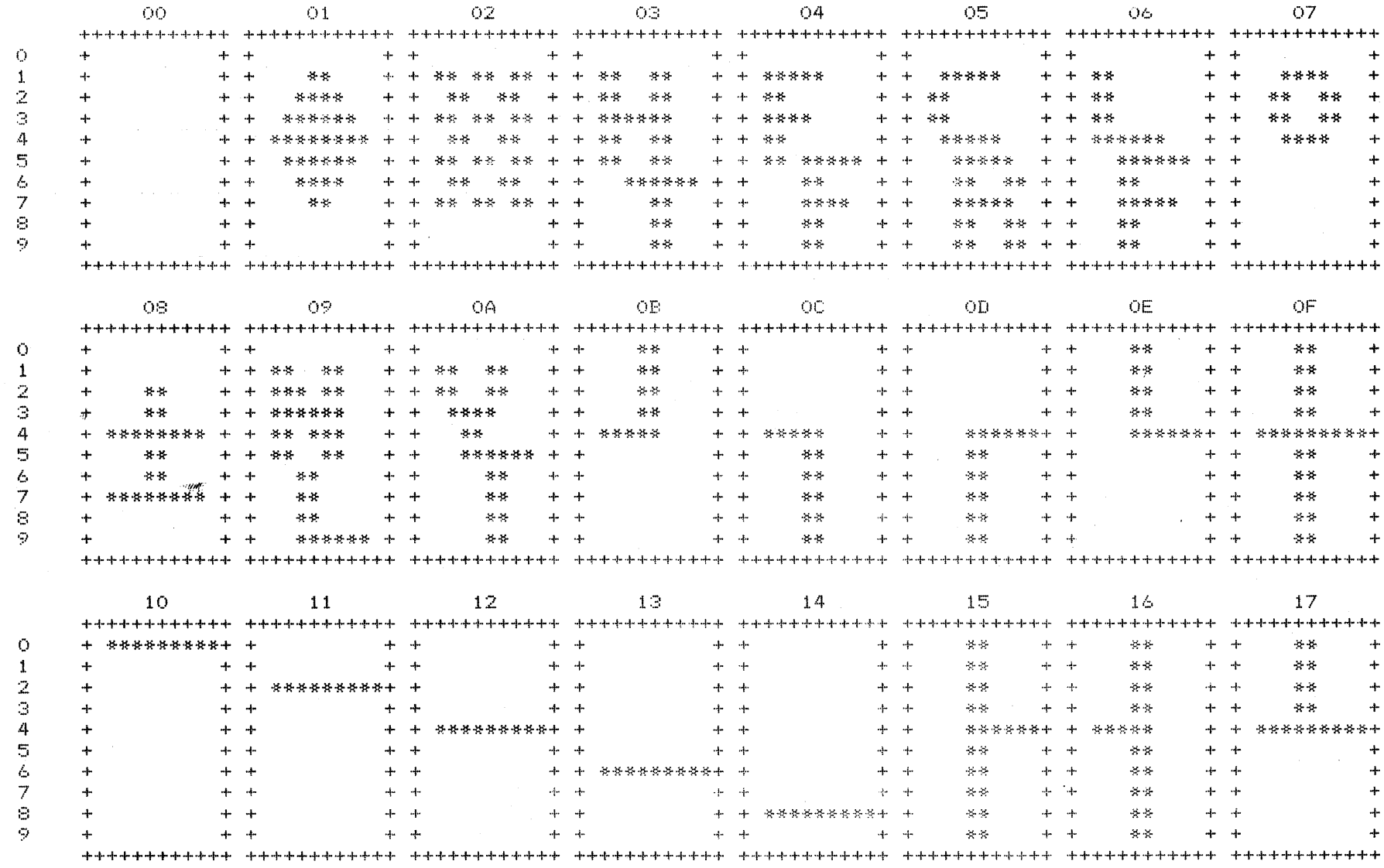
Mnemonic	Source Chip	Source Schematic Page	Definition
SCØ	U32	2	Scroll Count Bit Ø
SCCØ	U54	9	Scroll Count Bit Ø (Scroll Region)
SCCD	U106	9	Secondary Channel Carrier Detect
SCRØ	U20	5	Scroll Region Scroll Count Bit Ø
$\overline{\text{SCRTS}}$	U54	9	Secondary Channel Request-to-Send
SIL	U55	7	Set Interrupt Level
$\overline{\text{SPDS}}$	U54	9	Speed Select
$\overline{\text{SPIO}}$	U55	7	Select PIO
$\overline{\text{SSIO}}$	U56	7	Select SIO (USART)
STASTB	U56	7	Keyboard Status Strobe
SVTAC	U55	7	Select VTAC
TXD	U103	7	Transmit Data
TXDE	U54	9	Transmit Data Enable
U/L	U40	3	Underline Attribute
VCØ	U19	2	Video Character Count Bit Ø
VDØ	U30	3	Video Data Bit Ø
$\overline{\text{VIDENB}}$	U54	9	Video Enable
VIDIPT	U35	2	Video Interrupt
VREF	R47	1	Voltage Reference (+5V)
VSØ	U5	2	Video Slice Bit Ø
VSRCI	U23	1	Video Shift Register Clock Inhibit
VSRLD	U12	1	Video Shift Register Load
VSRO	U76	3	Video Shift Register Output
VSYNC	U32	2	Vertical Sync
VSYNCA	U58	5	Vertical Sync Buffered
WAIT	U53	7	CPU Wait Input
WR	U53	7	CPU Write
+5	Q2	1	P.S. Sch. +5 Volts
+12	VRI	10	P.S. Sch. +12 Volts
+15	Q4	1	P.S. Sch. +15 Volts
−12	VR3	1	P.S. Sch. −12 Volts
−23V	U33	8	P.S. Sch. −23 Volts

6. I.C. DATA SHEETS

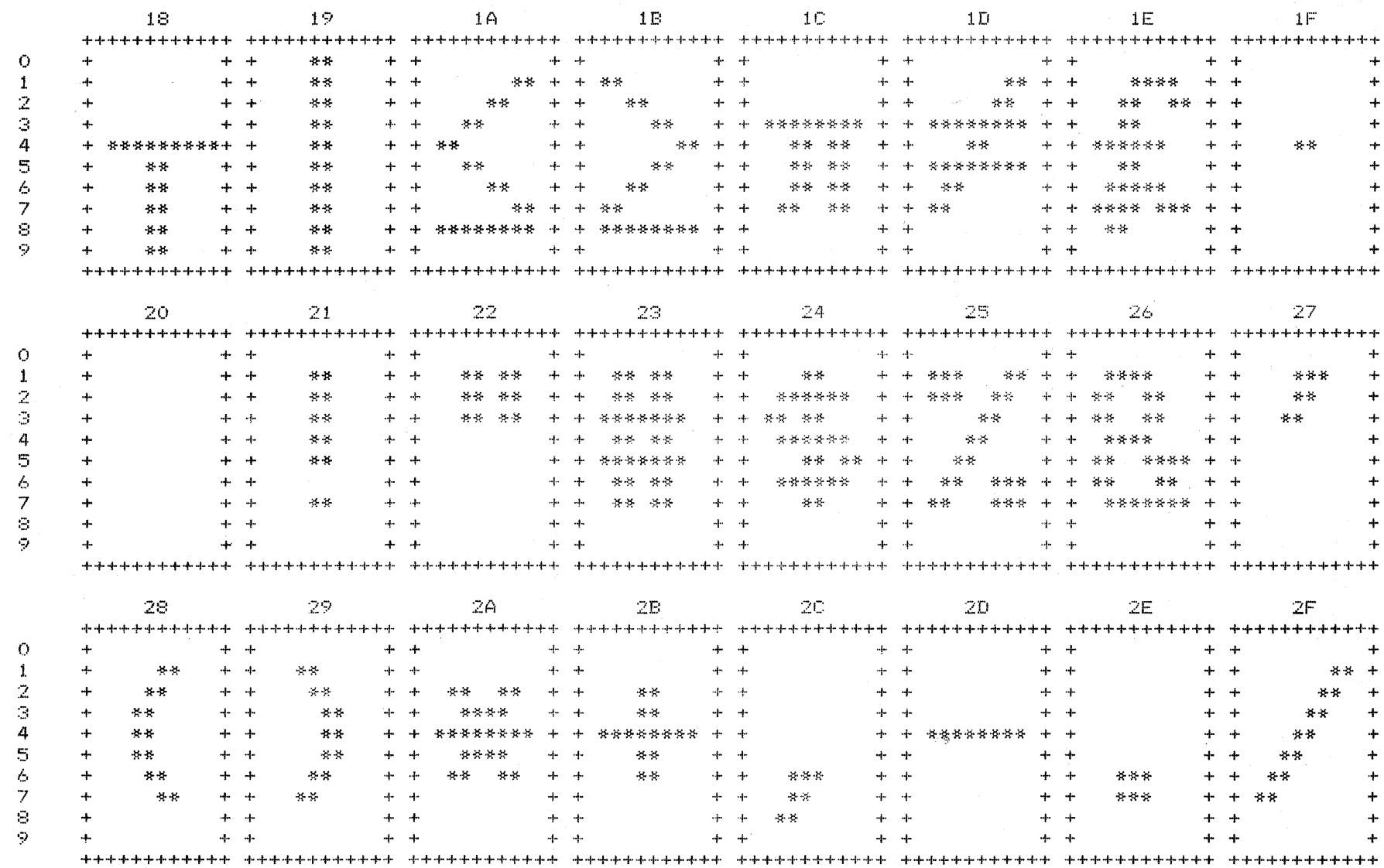
Included in this section are specifications for the following I.C.'s.

IC/E 241-ØØ1	Standard Character Generator
UPD 78Ø	Z8Ø CPU
2114L-2	1K RAM
2111	256X4 RAM
UPD 8251	USART
UPD 8255	PIO
8116-Ø2Ø	Baud Rate Generator
CRT 5027	VTAC
8214	Interrupt controller
ER14ØØ	Non-Volatile RAM

CGR100. 0. 0


00 01 02 03 04 05 06 07
08 09 0A 0B 0C 0D 0E 0F
10 11 12 13 14 15 16 17
0 1 2 3 4 5 6 7 8 9

CGR100. 0. 0



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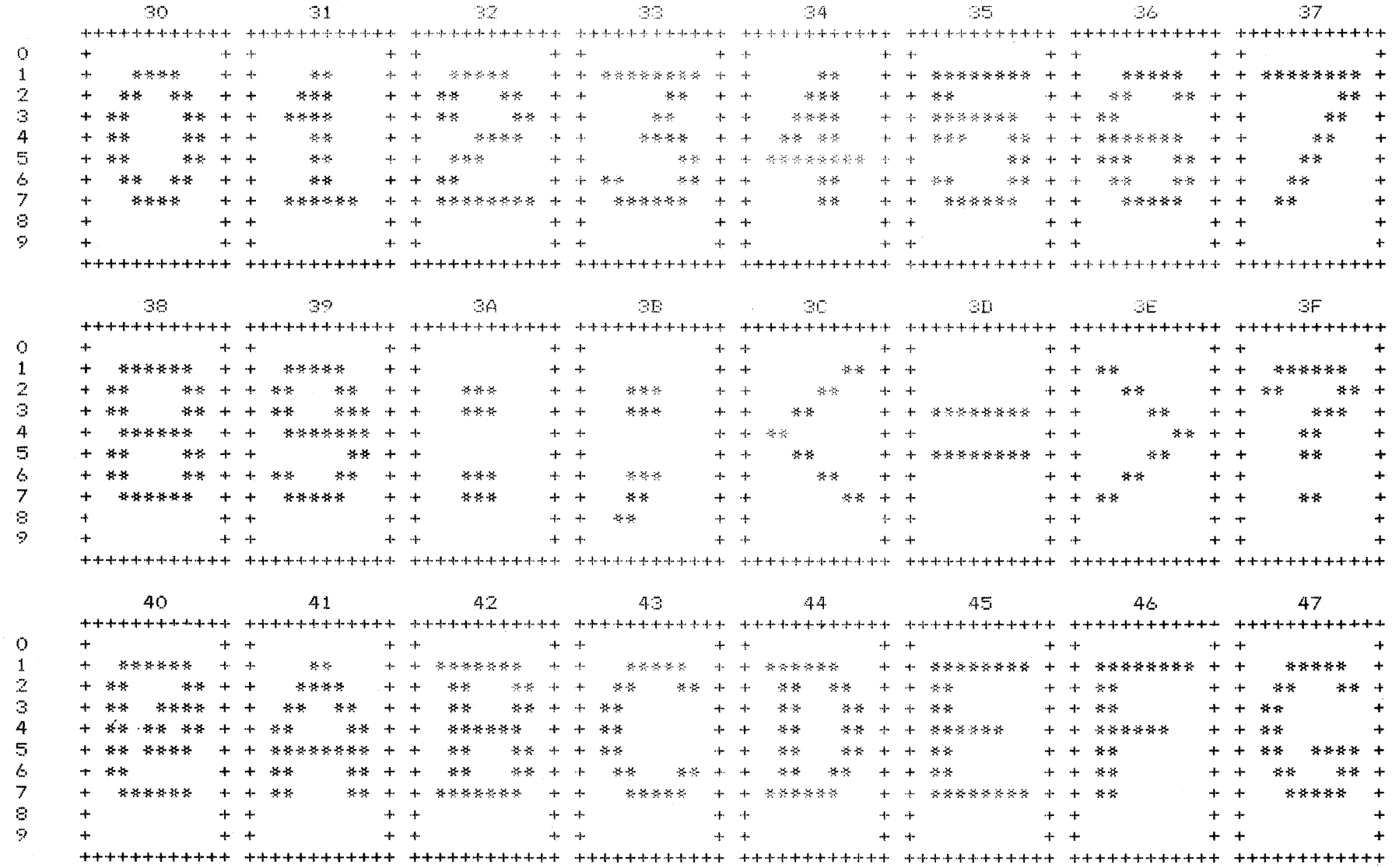

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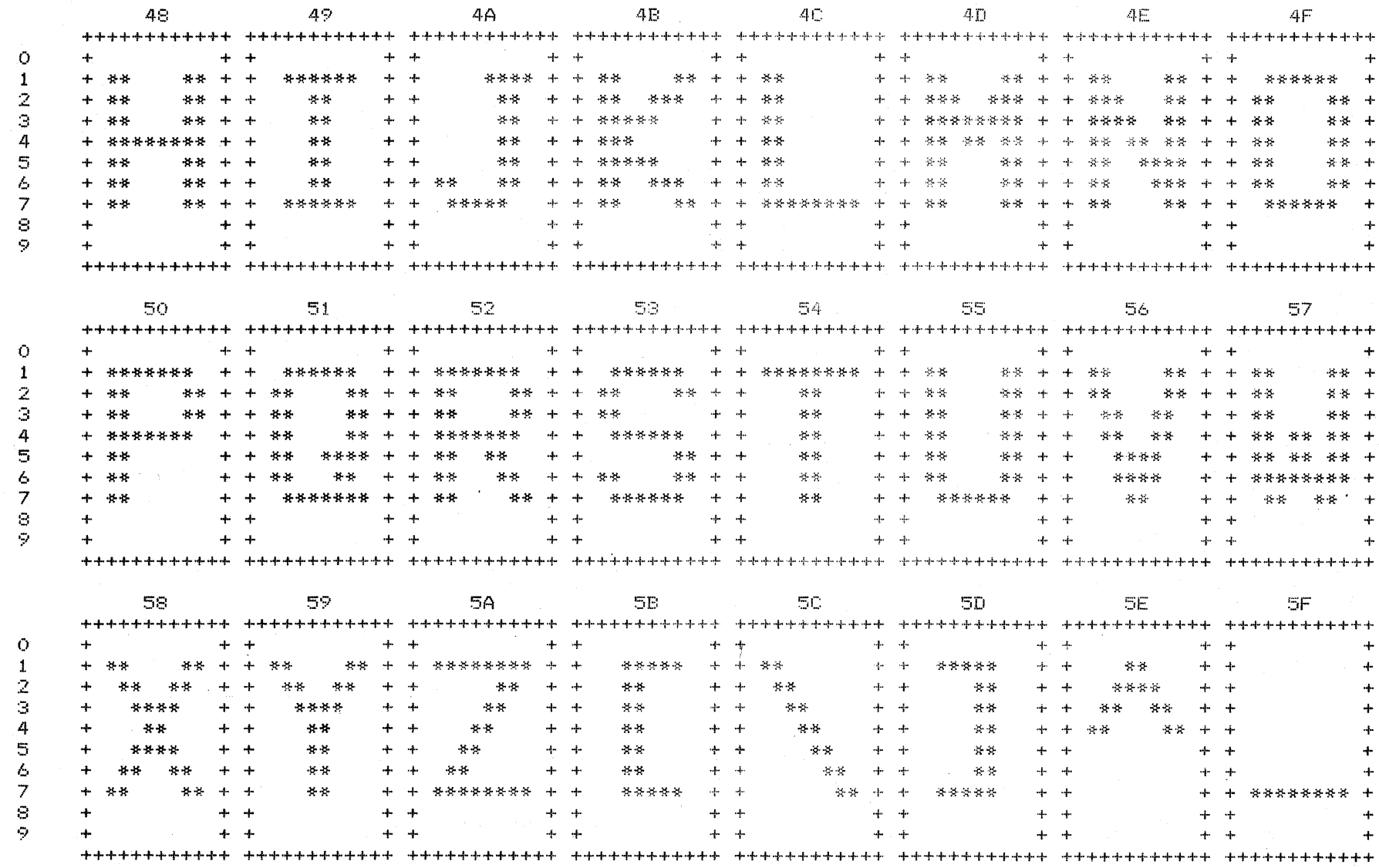
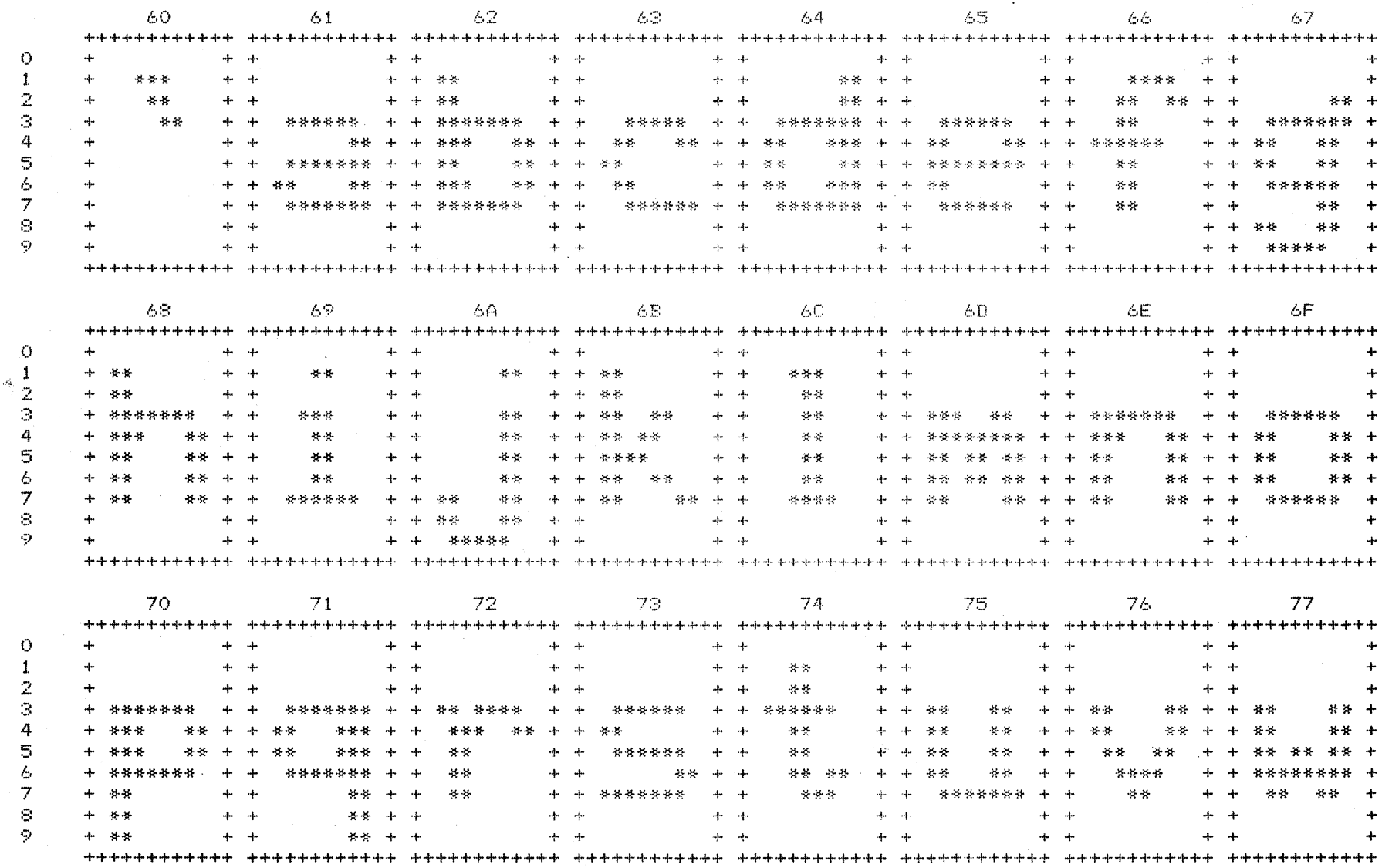
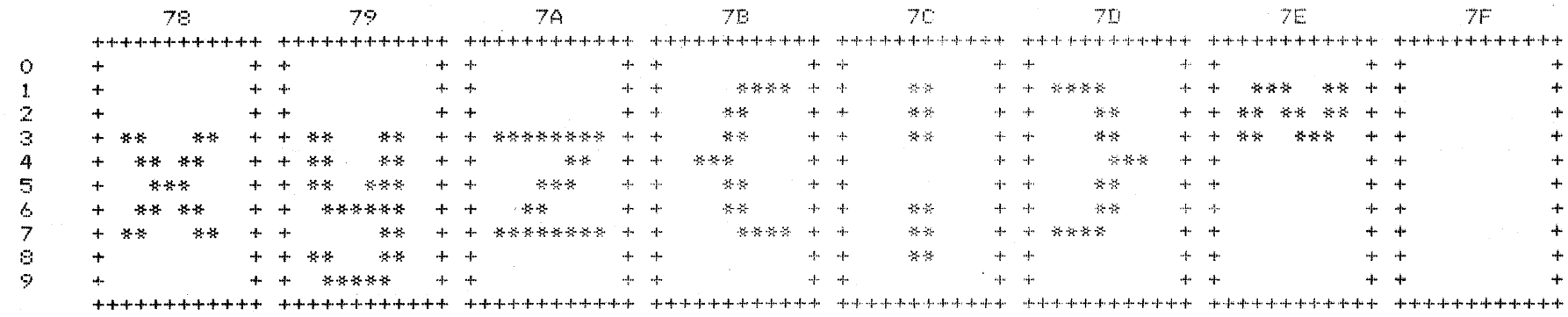

48 49 4A 4B 4C 4D 4E 4F
50 51 52 53 54 55 56 57
58 59 5A 5B 5C 5D 5E 5F
0
1
2
3
4
5
6
7
8
9

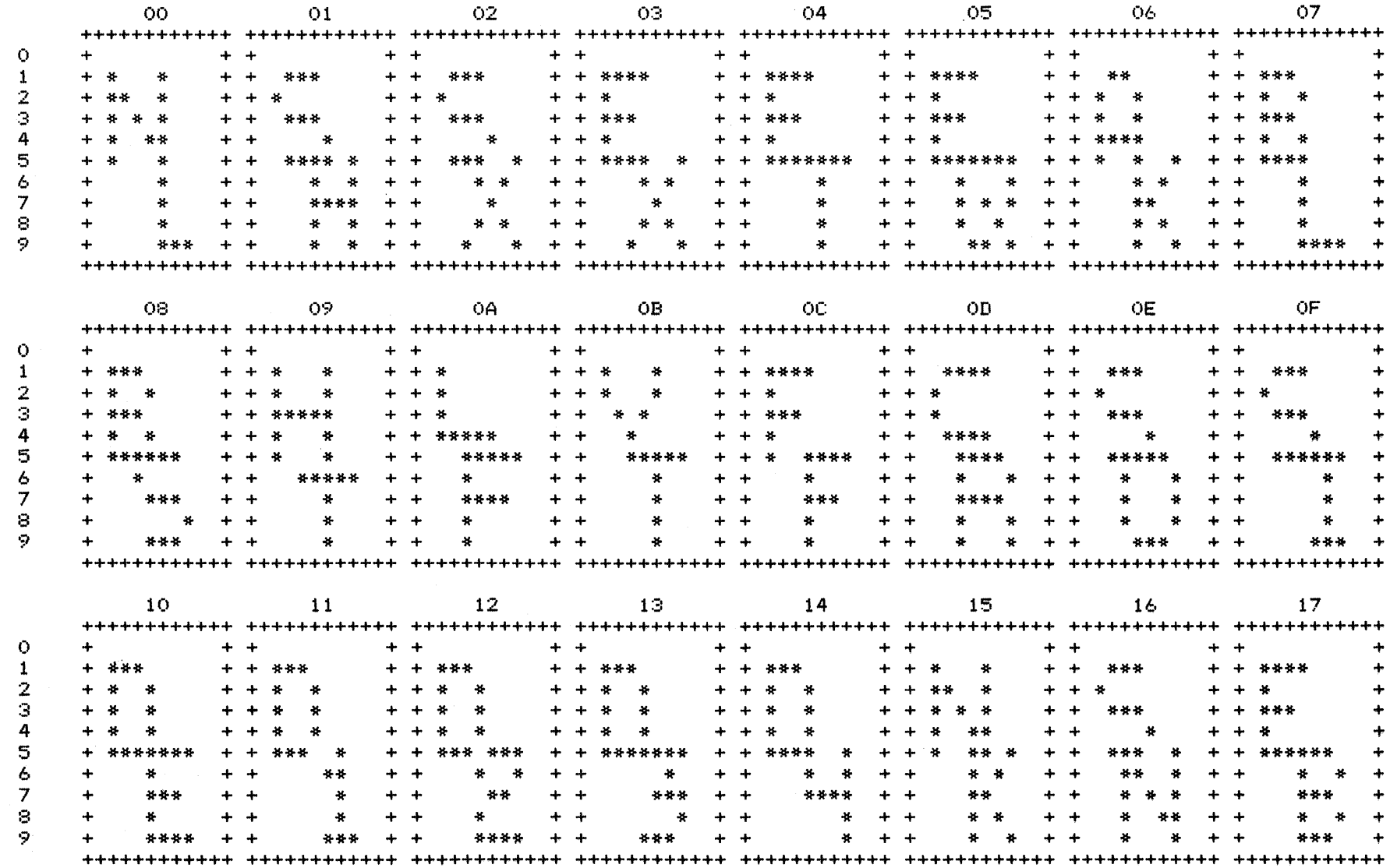
CGR100. 0. 0


60 61 62 63 64 65 66 67
68 69 6A 6B 6C 6D 6E 6F
70 71 72 73 74 75 76 77
0 1 2 3 4 5 6 7 8 9

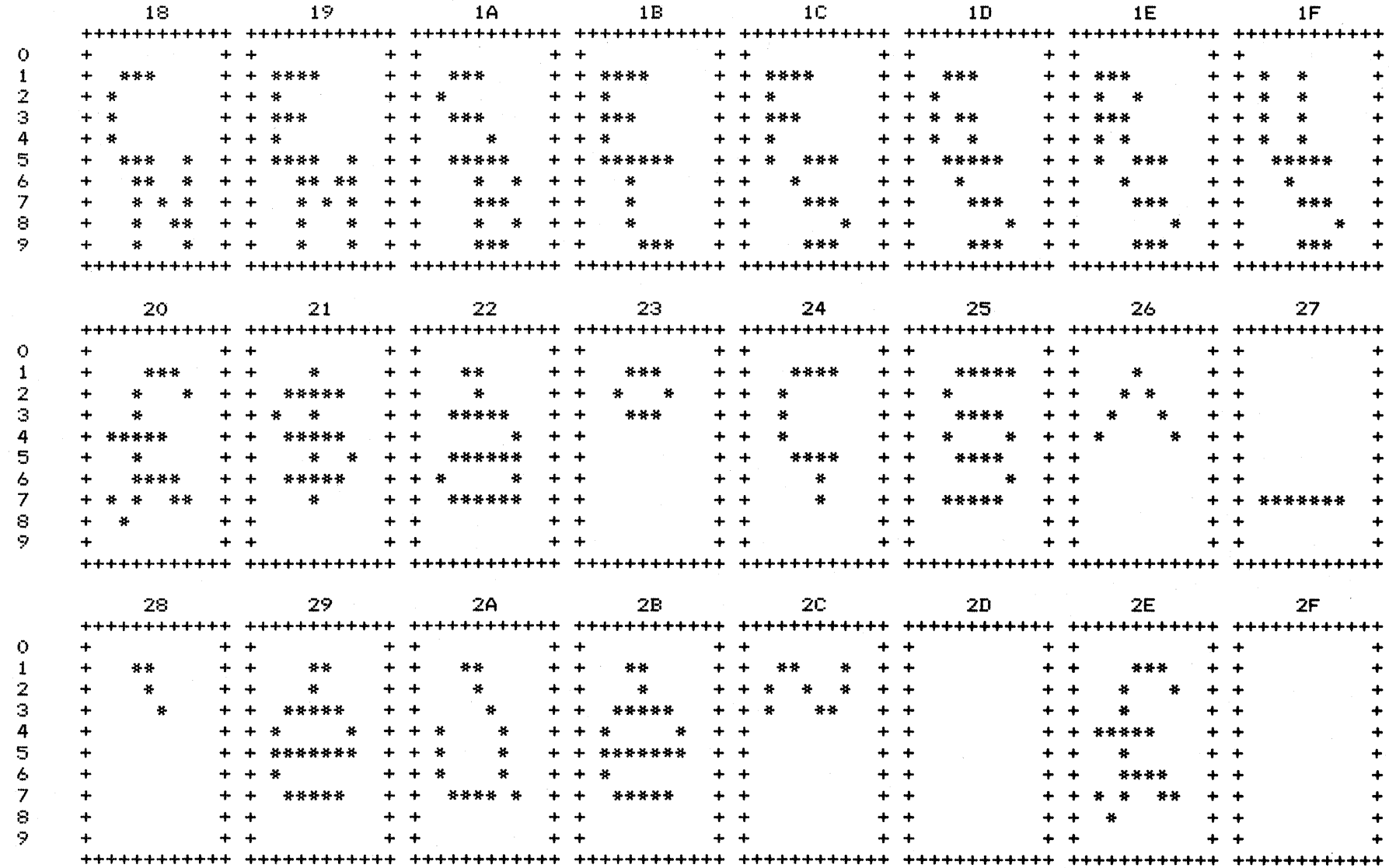
CGR100. 0. 0



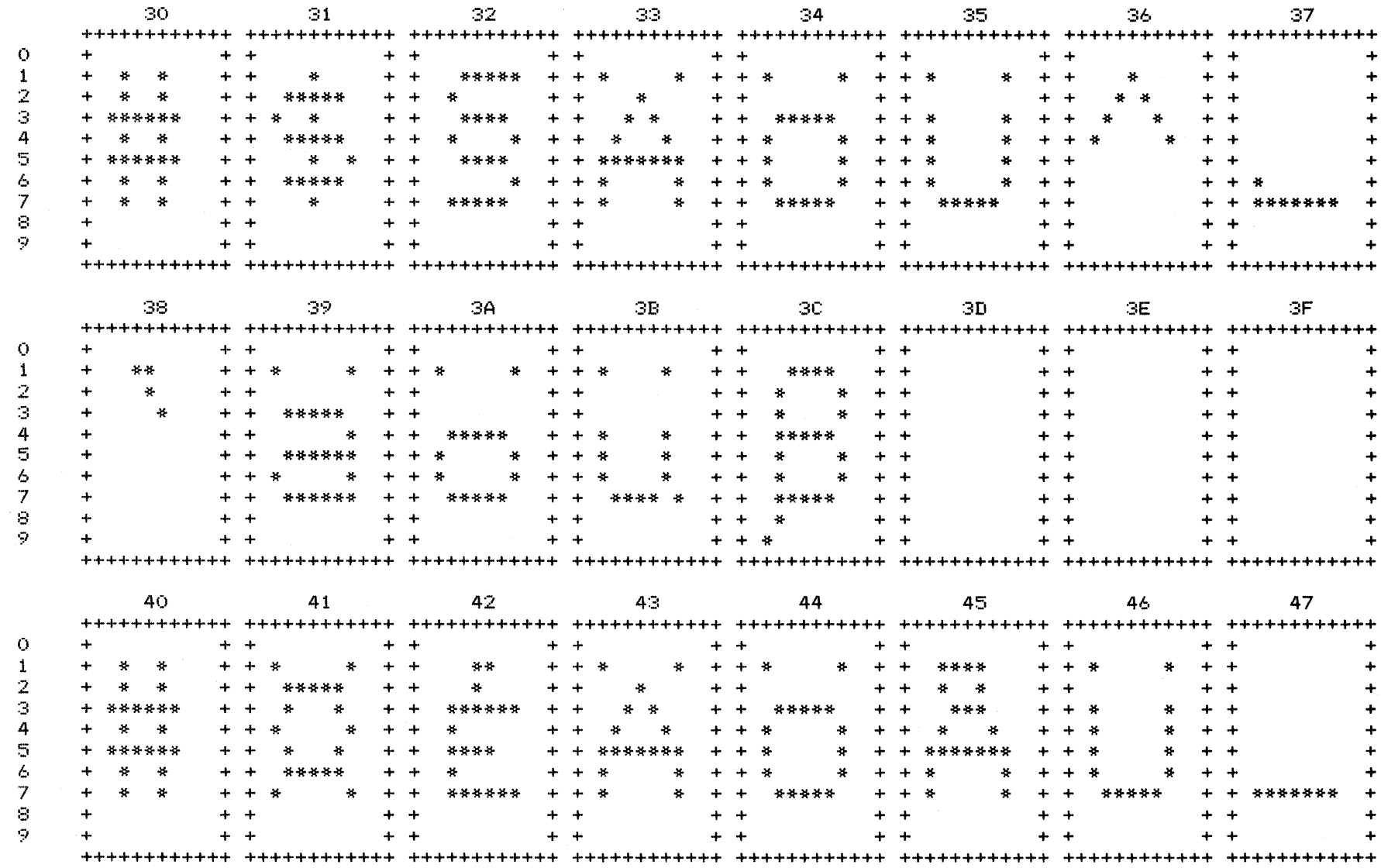
CGR100.1.0 VISUAL 400 ALTERNATE CHARACTER GENERATOR



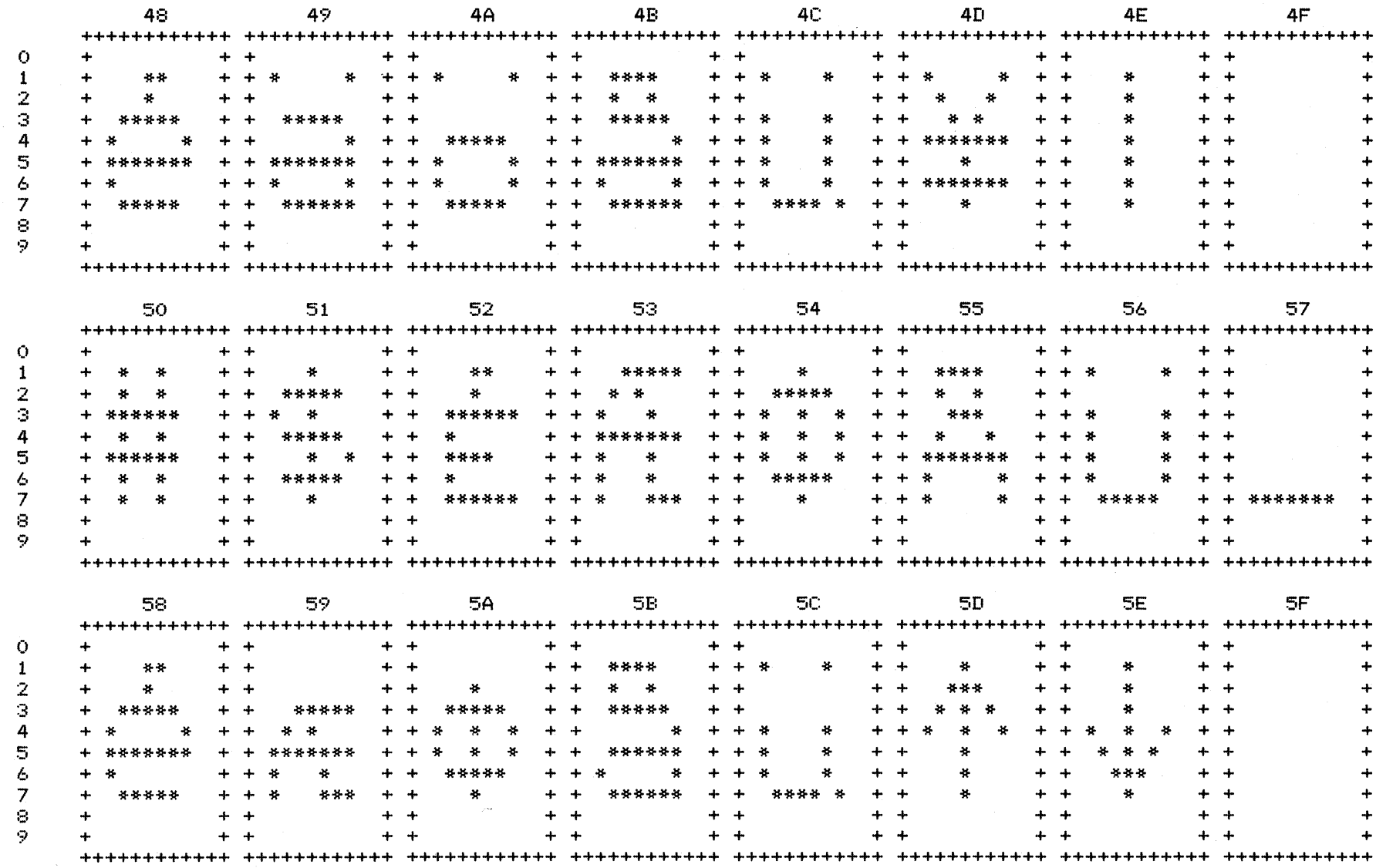
CGR100.1.0 VISUAL 400 ALTERNATE CHARACTER GENERATOR



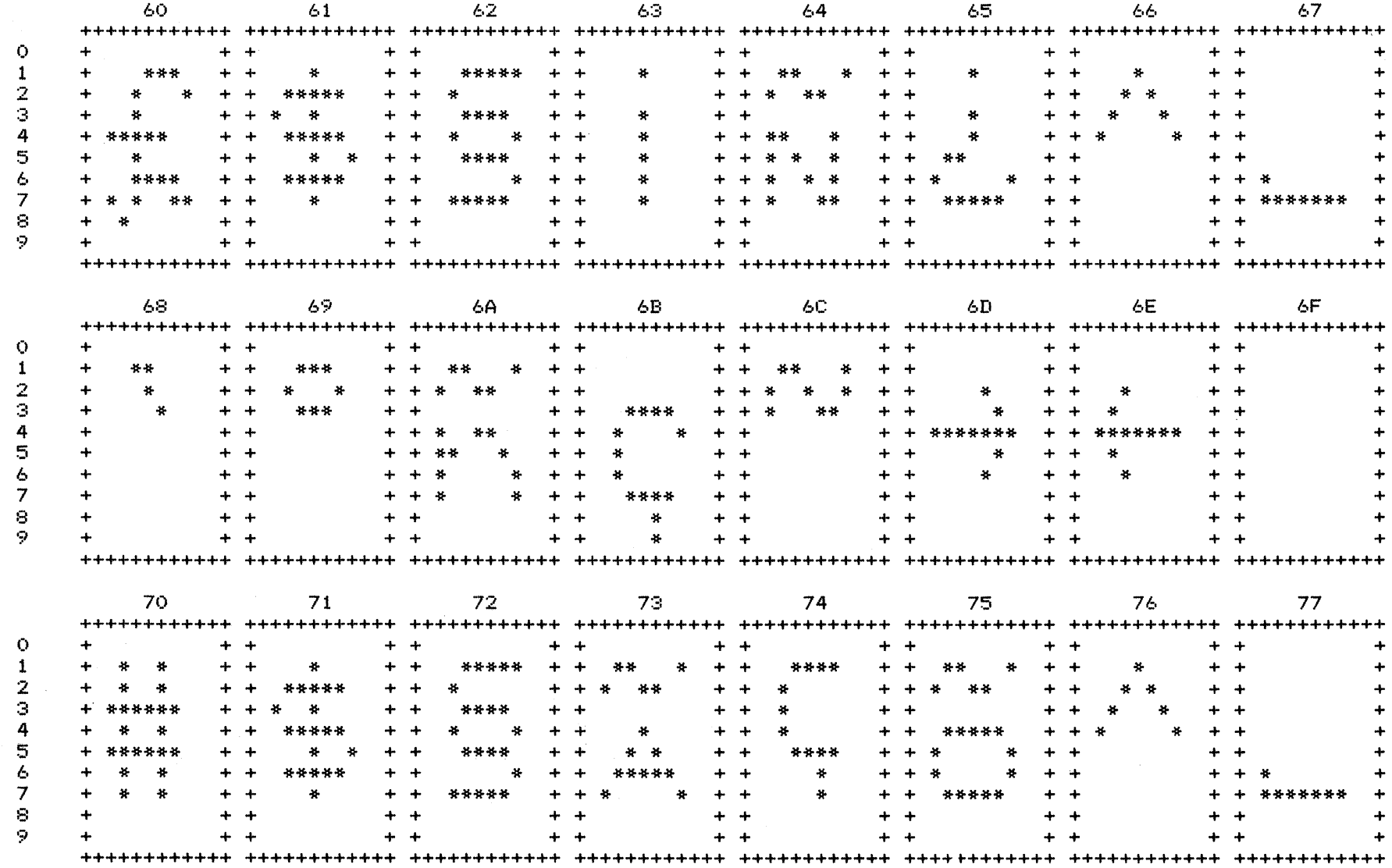
CGR100.1.0 VISUAL 400 ALTERNATE CHARACTER GENERATOR



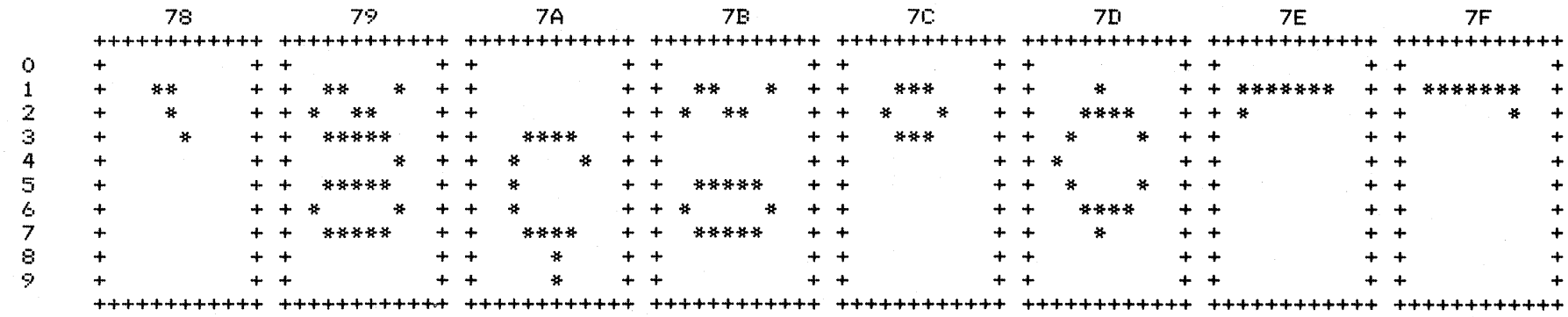
CGR100. 1. 0 VISUAL 400 ALTERNATE CHARACTER GENERATOR



CGR100.1.0 VISUAL 400 ALTERNATE CHARACTER GENERATOR



CGR100.1.0 VISUAL 400 ALTERNATE CHARACTER GENERATOR



8-BIT N-CHANNEL MICROPROCESSOR COMPLETELY Z80™ COMPATIBLE

DESCRIPTION

The μPD780 and μPD780-1 processors are single chip microprocessors developed from third generation technology. Their increased computational power produces higher system through-put and more efficient memory utilization, surpassing that of any second generation microprocessor. The single voltage requirement of the μPD780 and μPD780-1 processors makes it easy to implement them into a system. All output signals are fully decoded and timed to either standard memory or peripheral circuits. An N-channel, ion implanted, silicon gate MOS process is utilized in implementing the circuit.

The block diagram shows the functions of the processor and details the internal register structure. The structure contains 26 bytes of Read/Write (R/W) memory available to the programmer. Included in the registers are two sets of six general purpose registers, which may be used as 8-bit registers individually, or as 16-bit register pairs. Also included are two sets of accumulator and flag registers.

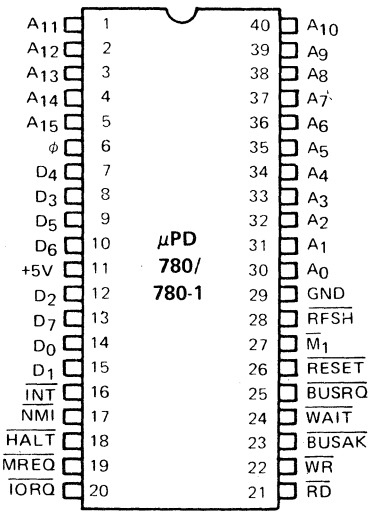
Through a group of exchange instructions the programmer has access to either set of main or alternate registers. The alternate register permits foreground/background mode of operation, or may be used for fast interrupt response. A 16-bit stack pointer is also included in each processor, simplifying implementation of multiple level interrupts, permitting unlimited subroutine nesting, and simplifying many types of data handling.

The two 16-bit index registers simplify implementation of relocatable code and manipulation of tabular data. The Refresh register will automatically refresh external dynamic memories. A powerful interrupt response mode will use the I register to form the upper 8-bits of a pointer to an interrupt service address table, while the interrupting apparatus supplies the lower 8-bits of the pointer. An indirect call will then be made to service this address.

FEATURES

- Single Chip, N-Channel Silicon Gate Processor
- 158 Instructions – Including all 78 of the 8080A Instructions, Permitting Total Software Compatibility
- New 4-, 8-, and 16-Bit Operations Featuring Useful Addressing Modes such as Indexed, Bit and Relative
- 17 Internal Registers
- Three Modes of Rapid Interrupt Response, and One Non-Maskable Interrupt
- Directly Connects Standard Speed Dynamic or Static Memories, with Minimum Support Circuitry
- Single-Phase +5 Volt Clock and 5 VDC Supply
- TTL Compatibility
- Automatic Dynamic RAM Refresh Circuitry
- Available in Plastic Package

PIN CONFIGURATION



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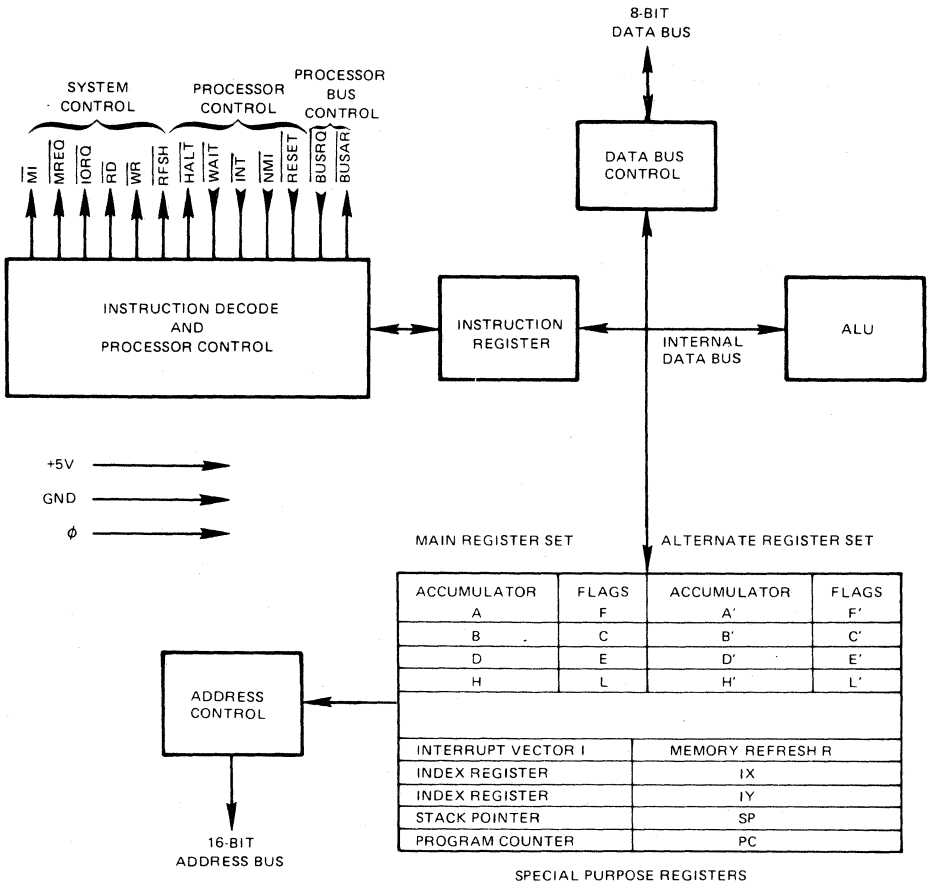
BLOCK DIAGRAM



PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
1-5, 30-40	A_0-A_{15}	Address Bus	3-State Output, active high. Pins A_0-A_{15} constitute a 16-bit address bus, which provides the address for memory and I/O device data exchanges. Memory capacity 65,536 bytes. A_0-A_7 is also needed as refresh cycle.
7-10, 12-15	D_0-D_7	Data Bus	3-State input/output, active high. Pins D_0-D_7 compose an 8-bit, bidirectional data bus, used for data exchanges with memory and I/O devices.
27	$\overline{M_1}$	Machine Cycle One	Output, active low. $\overline{M_1}$ indicates that the machine cycle in operation is the op code fetch cycle of an instruction execution.
19	$\overline{MREQ}$	Memory Request	3-State output, active low. $\overline{MREQ}$ indicates that a valid address for a memory read or write operation is held in the address.
20	$\overline{IORQ}$	Input/Output Request	3-State output, active low. The I/O request signal indicates that the lower half of the address bus holds a valid address for an I/O read or write operation. The $\overline{IORQ}$ signal is also used to acknowledge an interrupt command, indicating that an interrupt response vector can be placed on the data bus.
21	$\overline{RD}$	Memory Read	3-State output, active low. $\overline{RD}$ indicates that the processor is requesting data from memory or an I/O device. The memory or I/O device being addressed should use this signal to gate data onto the data bus.

PIN IDENTIFICATION (CONT.)

PIN NO.	PIN SYMBOL	NAME	FUNCTION
22	$\overline{WR}$	Memory Write	3-State output, active low. The memory write signal indicates that the processor data bus is holding valid data to be stored in the addressed, memory or I/O device.
28	$\overline{RFSH}$	Refresh	Output, active low. $\overline{RFSH}$ indicates that a refresh address for dynamic memories is being held in the lower 7-bits of the address bus. The $\overline{MREQ}$ signal should be used to implement a refresh read to all dynamic memories.
18	$\overline{HALT}$	Halt State	Output, active low. $\overline{HALT}$ indicates that the processor has executed a HALT software instruction, and will not resume operation until either a non-maskable or a maskable (with mask enabled) interrupt has been implemented. The processor will execute NOP's while halted, to maintain memory refresh activity.
24	$\overline{WAIT}$	Wait	Input, active low. $\overline{WAIT}$ indicates to the processor that the memory or I/O devices being addressed are not ready for a data transfer. As long as this signal is active, the processor will reenter wait states.
16	$\overline{INT}$	Interrupt Request	Input, active low. The $\overline{INT}$ signal is produced by I/O devices. The request will be honored upon completion of the current instruction, if the interrupt enable flip-flop (IFF) is enabled by the internal software. There are three modes of interrupt response. Mode 0 is identical to 8080 interrupt response mode. The Mode 1 response is a restart location at 0038_H. Mode 2 is for simple vectoring to an interrupt service routine anywhere in memory.
17	$\overline{NMI}$	Non-Maskable Interrupt	Input, active low. The non-maskable interrupt has a higher priority than $\overline{INT}$. It is always acknowledged at the end of the current instruction, regardless of the status of the interrupt enable flip-flop. When the $\overline{NMI}$ signal is given, the μPD780 processor automatically restarts to location 0066_H.
26	$\overline{RESET}$	Reset	Input, active low. The $\overline{RESET}$ signal causes the processor to reset the interrupt enable flip-flop (IFF), clear PC and I and R registers, and set interrupt to 8080A mode. During the reset time, the address bus and data bus go to a state of high impedance, and all control output signals become inactive, after which processing continues at 0000H.
25	$\overline{BUSRQ}$	Bus Request	Input, active low. $\overline{BUSRQ}$ has a higher priority than $\overline{NMI}$, and is always honored at the end of the current machine cycle. It is used to allow other devices to take control over the processor address bus, data bus signals; by requesting that they go to a state of high impedance.
23	$\overline{BUSAK}$	Bus Acknowledge	Output, active low. $\overline{BUSAK}$ is used to inform the requesting device that the processor address bus, data bus and 3-state control bus signals have entered a state of high impedance, and the external device can now take control of these signals.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
Voltage on any Pin	-0.3 to +7 Volts ①
Power Dissipation	1.5W

Note: ① With Respect to Ground

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 5% unless otherwise specified.

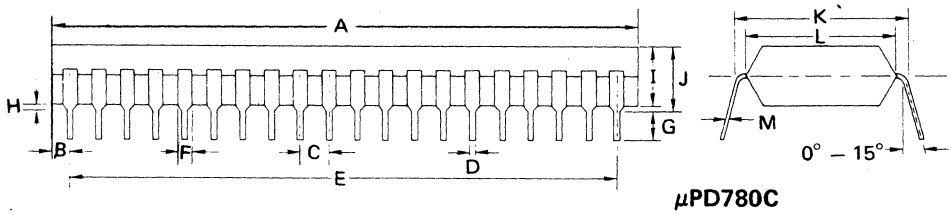
PARAMETER		SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Input Low Voltage		V_{ILC}	-0.3		0.45	V	
Clock Input High Voltage		V_{IHC}	V_{CC}-0.2		V_{CC}	V	
Input Low Voltage		V_{IL}	-0.3		0.8	V	
Input High Voltage		V_{IH}	2.0		V_{CC}	V	
Output Low Voltage		V_{OL}			0.4	V	I_{OL} = 1.8 mA
Output High Voltage		V_{OH}	2.4			V	I_{OH} = -250 μA
Power Supply Current	μPD780	I_{CC}			150	mA	t_c = 400 ns
	μPD780-1	I_{CC}		90	200	mA	t_c = 250 ns
Input Leakage Current		I_{LI}			10	μA	V_{IN} = 0 to V_{CC}
Tri-State Output Leakage Current in Float		I_{LOH}			10	μA	V_{OUT} = 2.4 to V_{CC}
Tri-State Output Leakage Current in Float		I_{LOL}			-10	μA	V_{OUT} = 0.4 V
Data Bus Leakage Current in Input Mode		I_{LD}			±10	μA	$0 \leqslant V_{IN} \leqslant V_{CC}$

CAPACITANCE

T_a = 25°C

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Capacitance	C_ϕ			35	pF	f_c = 1 MHz
Input Capacitance	C_{IN}			5	pF	Unmeasured Pins
Output Capacitance	C_{OUT}			10	pF	Returned to Ground

PACKAGE OUTLINES
μPD780C/D



μPD780C
μPD780C-1
(Plastic)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

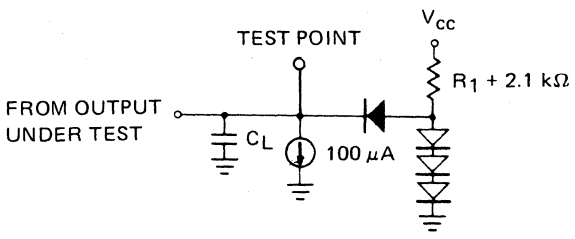
AC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 5%, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS μPD780 MIN	LIMITS μPD780 MAX	LIMITS μPD780-1 MIN	LIMITS μPD780-1 MAX	UNIT	TEST CONDITIONS
Clock Period	t_c	0.4	⑫	0.25	⑫	μs	
Clock Pulse Width, Clock High	$t_w(\Phi H)$	180		110		ns	
Clock Pulse Width, Clock Low	$t_w(\Phi L)$	180	2000	110	2000	ns	
Clock Rise and Fall Time	$t_{r,f}$		30		30	ns	
Address Output Delay	$t_{D(AD)}$		145		110	ns	
Delay to Float	$t_{F(AD)}$		110		90	ns	
Address Stable Prior to $\overline{MREQ}$ (Memory Cycle)	t_{acm}	①		①		ns	C_L = 50 pF
Address Stable Prior to $\overline{IORQ}$, $\overline{RD}$ or $\overline{WR}$ (I/O Cycle)	t_{aci}	②		②		ns	
Address Stable from $\overline{RD}$ or $\overline{WR}$	t_{ca}	③		③		ns	
Address Stable from $\overline{RD}$ or $\overline{WR}$ During Float	t_{caf}	④		④		ns	
Data Output Delay	$t_{D(D)}$		230		150	ns	
Delay to Float During Write Cycle	$t_{F(D)}$		90		90	ns	
Data Setup Time to Rising Edge of Clock During M1 Cycle	$t_{S\Phi(D)}$	50		35		ns	
Data Setup Time to Falling Edge of Clock During M2 to M5 Cycles	$t_{S\bar{\Phi}(D)}$	60		50		ns	C_L = 200 pF
Data Stable Prior to $\overline{WR}$ (Memory Cycle)	t_{dcm}	⑤		⑤		ns	
Data Stable Prior to $\overline{WR}$ (I/O Cycle)	t_{dci}	⑥		⑥		ns	
Data Stable from $\overline{WR}$	t_{cdf}	⑦		⑦		ns	
Any Hold Time for Setup Time	t_H	0			0	ns	
$\overline{MREQ}$ Delay from Falling Edge of Clock to $\overline{MREQ}$ Low	$t_{DL\bar{\Phi}(MR)}$		100		85	ns	
$\overline{MREQ}$ Delay from Rising Edge of Clock to $\overline{MREQ}$ High	$t_{DH\Phi(MR)}$		100		85	ns	
$\overline{MREQ}$ Delay from Falling Edge of Clock to $\overline{MREQ}$ High	$t_{DH\bar{\Phi}(MR)}$		100		85	ns	
Pulse Width, $\overline{MREQ}$ Low	$t_{w(\overline{MRL})}$	⑧		⑧		ns	
Pulse Width, $\overline{MREQ}$ High	$t_{w(\overline{MRH})}$	⑨		⑨		ns	
$\overline{IORQ}$ Delay from Rising Edge of Clock to $\overline{IORQ}$ Low	$t_{DL\Phi(IR)}$		90		75	ns	
$\overline{IORQ}$ Delay from Falling Edge of Clock to $\overline{IORQ}$ Low	$t_{DL\bar{\Phi}(IR)}$		110		85	ns	
$\overline{IORQ}$ Delay from Rising Edge of Clock to $\overline{IORQ}$ High	$t_{DH\Phi(IR)}$		100		85	ns	
$\overline{IORQ}$ Delay from Falling Edge of Clock to $\overline{IORQ}$ High	$t_{DH\bar{\Phi}(IR)}$		110		85	ns	C_L = 50 pF
$\overline{RD}$ Delay from Rising Edge of Clock to $\overline{RD}$ Low	$t_{DL\Phi(RD)}$		100		85	ns	
$\overline{RD}$ Delay from Falling Edge of Clock to $\overline{RD}$ Low	$t_{DL\bar{\Phi}(RD)}$		130		95	ns	
$\overline{RD}$ Delay from Rising Edge of Clock to $\overline{RD}$ High	$t_{DH\Phi(RD)}$		100		85	ns	
$\overline{RD}$ Delay from Falling Edge of Clock to $\overline{RD}$ High	$t_{DH\bar{\Phi}(RD)}$		110		85	ns	
$\overline{WR}$ Delay from Rising Edge of Clock to $\overline{WR}$ Low	$t_{DL\Phi(WR)}$		80		65	ns	
$\overline{WR}$ Delay from Falling Edge of Clock to $\overline{WR}$ Low	$t_{DL\bar{\Phi}(WR)}$		90		80	ns	
$\overline{WR}$ Delay from Falling Edge of Clock to $\overline{WR}$ High	$t_{DH\Phi(WR)}$		100		80	ns	
Pulse Width to $\overline{WR}$ Low	$t_{w(\overline{WRL})}$	⑩		⑩		ns	
$\overline{M1}$ Delay from Rising Edge of Clock to $\overline{M1}$ Low	$t_{DL(M1)}$		130		100	ns	C_L = 30 pF
$\overline{M1}$ Delay from Rising Edge of Clock to $\overline{M1}$ High	$t_{DH(M1)}$		130		100	ns	
$\overline{RFSH}$ Delay from Rising Edge of Clock to $\overline{RFSH}$ Low	$t_{DL(RF)}$		180		130	ns	
$\overline{RFSH}$ Delay from Rising Edge of Clock to $\overline{RFSH}$ High	$t_{DH(RF)}$		150		120	ns	
$\overline{WAIT}$ Setup Time to Falling Edge of Clock	$t_{s(WT)}$	70		70		ns	
$\overline{HALT}$ Delay Time from Falling Edge of Clock	$t_{D(HT)}$		300		300	ns	C_L = 50 pF
$\overline{INT}$ Setup Time to Rising Edge of Clock	$t_{s(IT)}$	80		80		ns	
Pulse Width, $\overline{NMI}$ Low	$t_{w(\overline{NML})}$	80		80		ns	
$\overline{BUSRQ}$ Setup Time to Rising Edge of Clock	$t_{s(BQ)}$	80		50		ns	
$\overline{BUSAK}$ Delay from Rising Edge of Clock to $\overline{BUSAK}$ Low	$t_{DL(BA)}$		120		100	ns	C_L = 50 pF
$\overline{BUSAK}$ Delay from Falling Edge of Clock to $\overline{BUSAK}$ High	$t_{DH(BA)}$		110		100	ns	
$\overline{RESET}$ Setup Time to Rising Edge of Clock	$t_{s(RS)}$	90		60		ns	
Delay to Float ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$ and $\overline{WR}$)	$t_{F(C)}$		100		80	ns	
$\overline{M1}$ Stable Prior to $\overline{IORQ}$ (Interrupt Ack.)	t_{mr}	⑪		⑪		ns	

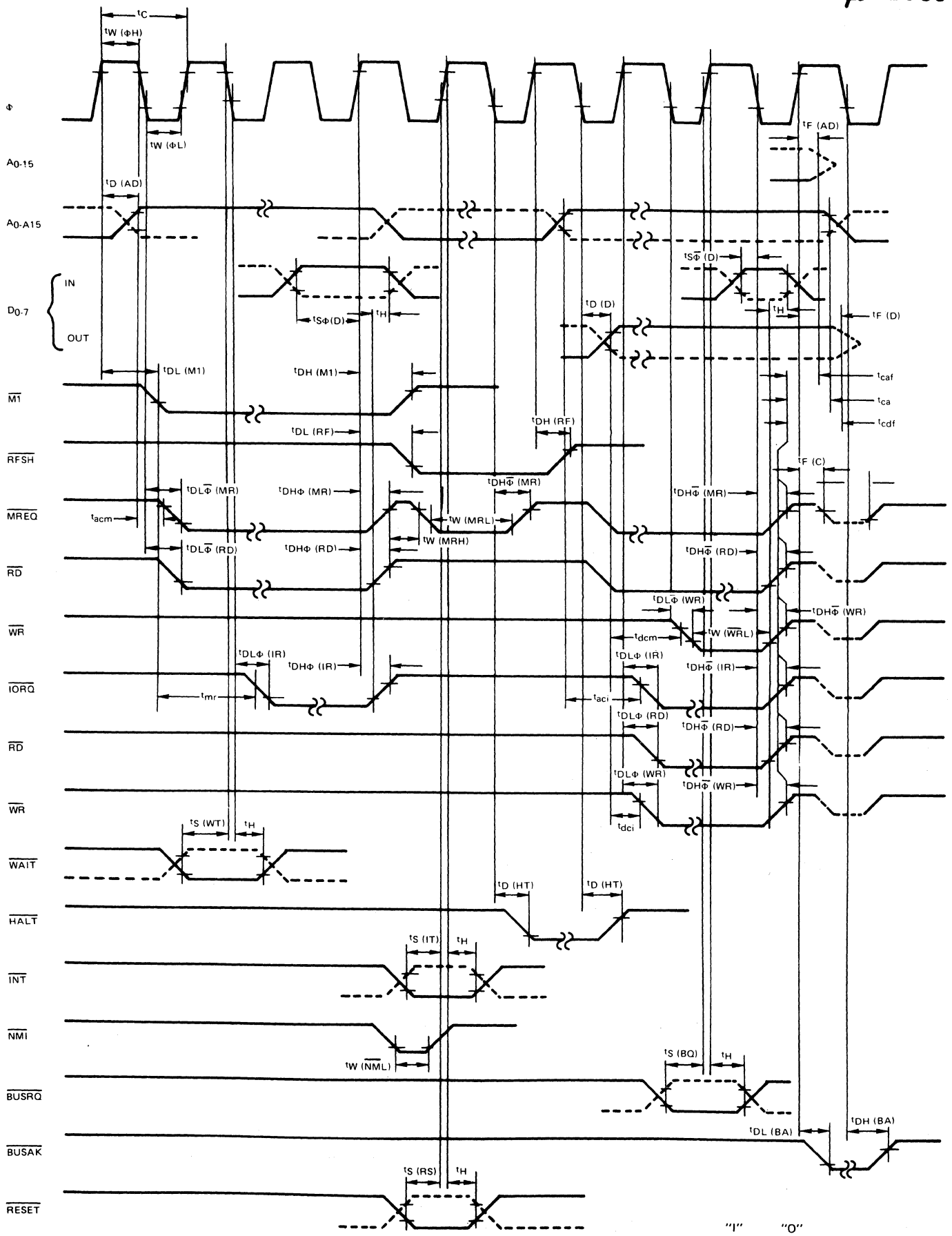
Notes:
① $t_{acm} = t_w(\Phi H) + t_f - 65$ (75)*
② $t_{aci} = t_c - 70$ (80)*
③ $t_{ca} = t_w(\Phi L) + t_r - 50$ (40)*
④ $t_{caf} = t_w(\Phi L) + t_r - 45$ (60)*
⑤ $t_{dcm} = t_c - 170$ (210)*
⑥ $t_{dci} = t_w(\Phi L) + t_r - 170$ (210)*
⑦ $t_{cdf} = t_w(\Phi L) + t_r - 70$ (80)*
⑧ $t_{w(\overline{MRL})} = t_c - 30$ (40)*
⑨ $t_{w(\overline{MRH})} = t_w(\Phi H) + t_f - 20$ (30)*
⑩ $t_{w(\overline{WR})} = t_c - 30$ (40)*
⑪ $t_{mr} = 2t_c + t_w(\Phi H) + t_f - 65$ (80)*
⑫ $t_c = t_w(\Phi H) + t_w(\Phi L) + t_r + t_f$

*These values apply to the μPD780.



LOAD CIRCUIT FOR OUTPUT

TIMING WAVEFORM ①

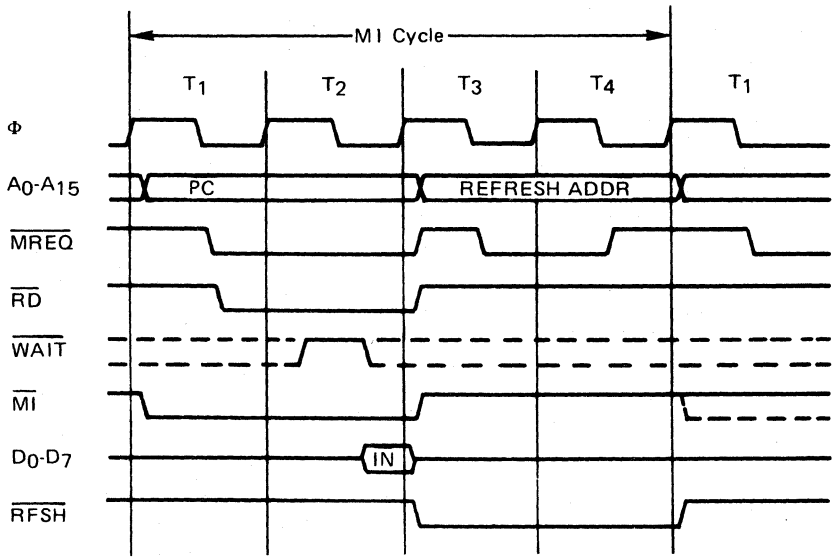


Note: ① Timing measurements are made at the following voltages unless otherwise specified:

	"I"	"O"
CLOCK	4.2V	0.8V
OUTPUT	2.0V	0.8V
INPUT	2.0V	0.8V
FLOAT	ΔV	±0.5V

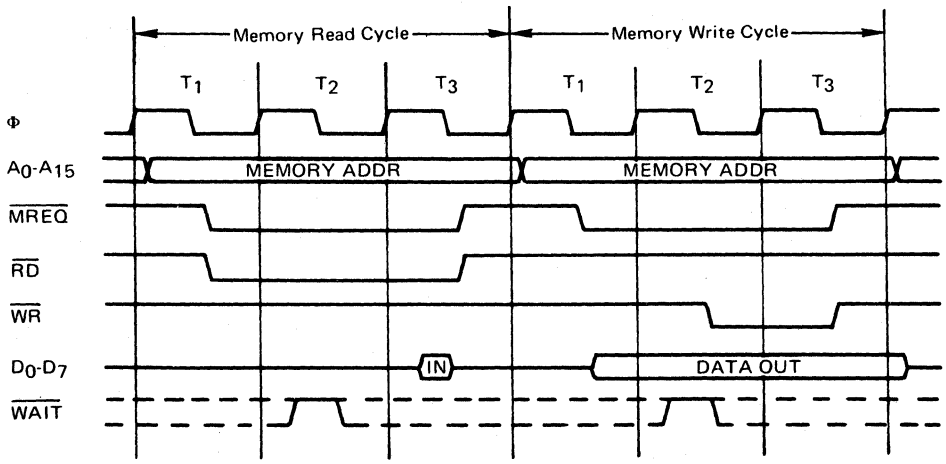
Instruction Op Code Fetch

The contents of the program counter (PC) are placed on the address bus at the start of the cycle. $\overline{MREQ}$ goes active one-half clock cycle later, and the falling edge of this signal can be used directly as a chip enable to dynamic memories. The memory data should be enabled onto the processor data bus when $\overline{RD}$ goes active. The processor takes data with the rising edge of the clock state T_3. The processor internally decodes and executes the instruction, while clock states T_3 and T_4 of the fetch cycle are used to refresh dynamic memories. The refresh control signal $\overline{RFSH}$ indicates that a refresh read should be done to all dynamic memories.



Memory Read or Write Cycles

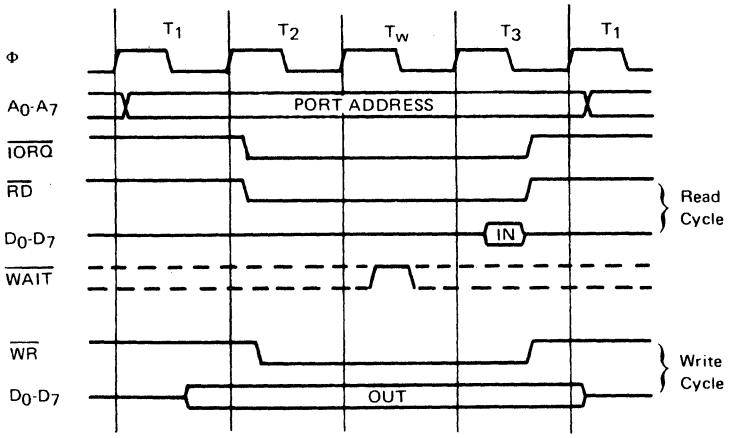
This diagram illustrates the timing of memory read or write cycles other than an op code fetch (M_1 cycle). The function of the $\overline{MREQ}$ and $\overline{RD}$ signals is exactly the same as in the op code fetch cycle. When a memory write cycle is implemented, the $\overline{MREQ}$ becomes active and is used directly as a chip enable for dynamic memories, when the address bus is stable. The $\overline{WR}$ line is used directly as a R/W pulse to any type of semiconductor memory, and is active when data on the data bus is stable.



TIMING WAVEFORMS (CONT.)

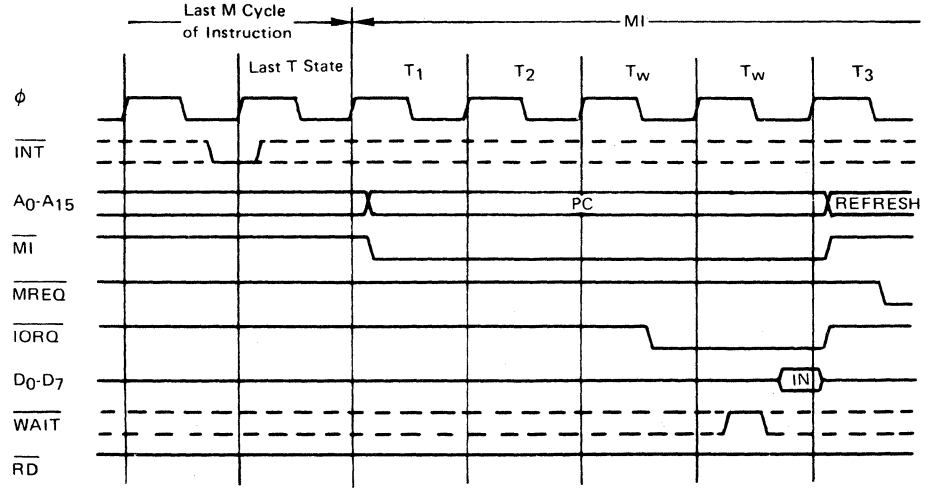
Input or Output Cycles

This illustrates the timing for an I/O read or I/O write operation. A single wait state (T_W) is automatically inserted in I/O operations to allow sufficient time for an I/O port to decode its address and activate the $\overline{WAIT}$ line, if necessary.



Interrupt Request/Acknowledge Cycle

The processor samples the interrupt signal with the rising edge of the last clock at the end of any instruction. A special M_1 cycle is started when an interrupt is accepted. During the M_1 cycle, the $\overline{IORQ}$ (instead of $\overline{MREQ}$) signal becomes active, indicating that the interrupting device can put an 8-bit vector on the data bus. Two wait states (T_W) are automatically added to this cycle. This makes it easy to implement a ripple priority interrupt scheme.



INSTRUCTION SET

The following summary shows the assembly language mnemonic and the symbolic operation performed by the instructions of the μPD780 and μPD780-1 processors. The instructions are divided into 16 categories:

Miscellaneous Group	8-Bit Loads
Rotates and Shifts	16-Bit Loads
Bit Set, Reset and Test	Exchanges
Input and Output	Memory Block Moves
Jumps	Memory Block Searches
Calls	8-Bit Arithmetic and Logic
Restarts	16-Bit Arithmetic
Returns	General Purpose Accumulator and Flag Operations

The addressing Modes include combinations of the following:

Indexed	Immediate
Register	Immediate Extended
Implied	Modified Page Zero
Register Indirect	Relative
Bit	Extended

INSTRUCTION SET TABLE

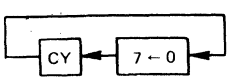
MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
ADC HL, ss	HL ← HL + ss + CY	Add with carry reg. pair ss to HL	1	11	↕	↕	V	↕	0	X	11 101 101 (A) 01 ss1 010
ADC A, r	A ← A + r + CY	Add with carry Reg. r to ACC	1	4	↕	↕	V	↕	0	↕	10 001 rrr (B)
ADC A,n	A ← A + n + CY	Add with carry value n to ACC		7	↕	↕	V	↕	0	↕	11 001 110 nn nnn nnn
ADC A, (HL)	A ← A + (HL) + CY	Add with carry loc. (HL) to ACC		7	↕	↕	V	↕	0	↕	10 001 110
ADC A, (IX + d)	A ← A + (IX + d) + CY	Add with carry loc. (IX + d) to ACC		19	↕	↕	V	↕	0	↕	11 011 101 10 001 110 dd ddd ddd
ADC A, (IY + d)	A ← A + (IY + d) + CY	Add with carry loc. (IY + d) to ACC		19	↕	↕	V	↕	0	↕	11 111 101 10 001 110 dd ddd ddd
ADD A, n	A ← A + n	Add value n to ACC	2	7	↕	↕	V	↕	0	↕	11 000 110 nn nnn nnn
ADD A, r	A ← A + r	Add Reg. r to ACC	1	4	↕	↕	V	↕	0	↕	10 000 rrr (B)
ADD A, (HL)	A ← A + (HL)	Add location (HL) to ACC	1	7	↕	↕	V	↕	0	↕	10 000 110
ADD A, (IX + d)	A ← A + (IX + d)	Add location (IX + d) to ACC	3	19	↕	↕	V	↕	0	↕	11 011 101 10 000 110 dd ddd ddd
ADD A, (IY + d)	A ← A + (IY + d)	Add location (IY + d) to ACC	3	19	↕	↕	V	↕	0	↕	11 111 101 10 000 110 dd ddd ddd
ADD HL, ss	HL ← HL + ss	Add Reg. pair ss to HL	1	11	↕	•	•	•	0	X	00 ss 1 001 (A)
ADD IX, pp	IX ← IX + pp	Add Reg. pair pp to IX	2	15	↕	•	•	•	0	X	11 011 101 (C) 00 pp1 001
ADD IY, rr	IY ← IY + rr	Add Reg. pair rr to IY	2	15	↕	•	•	•	0	X	11 111 101 (D) 00 rr1 001
AND r	A ← A∧r	Logical 'AND' of Reg. r ∧ ACC		4	0	↕	P	↕	0	↕	10 100 rrr (B)
AND n	A ← A∧n	Logical 'AND' of value n ∧ ACC		7	0	↕	P	↕	0	↕	11 100 110 nn nnn nnn
AND (HL)	A ← A∧(HL)	Logical 'AND' of loc. (HL) ∧ ACC		7	0	↕	P	↕	0	↕	10 100 110
AND (IX + d)	A ←A∧(IX + d)	Logical 'AND' of loc. (IX + d) ∧ ACC		19	0	↕	P	↕	0	↕	11 011 101 10 100 110 dd ddd ddd
AND (IY + d)	A ←A∧(IY + d)	Logical 'AND' of loc. (IY + d) ∧ ACC		19	0	↕	P	↕	0	↕	11 111 101 10 100 110 dd ddd ddd
BIT b, (HL)	Z ← $(\overline{HL})_b$	Test BIT b of location (HL)	2	12	•	↕	X	X	0	1	11 001 011 (E) 01 bbb 110
BIT b, (IX + d)	Z ← $(\overline{IX + d})_b$	Test BIT b at location (IX + d)	4	20	•	↕	X	X	0	1	11 011 101 (E) 11 001 011 dd ddd ddd 01 bbb 110
BIT b, (IY + d)	Z ← $(\overline{IY + d})_b$	Test BIT b at location (IY + d)	4	20	•	↕	X	X	0	1	11 111 101 (E) 11 001 011 dd ddd ddd 01 bbb 110
BIT b, r	Z ← $\overline{r}_b$	Test BIT of Reg. r	2	8	•	↕	X	X	0	1	11 001 011 01 bbb rrr (B)(E)
CALL cc, nn	If condition cc false continue, else same as CALL nn	Call subroutine at location nn if condition cc is true	3	10	•	•	○	•	•	•	11 ←cc→ 100 (H) nn nnn nnn nn nnn nnn
CALL nn	(SP – 1) ← PC_H (SP – 2) ← PC_L PC ← nn	Unconditional call subroutine at location nn	3	17	•	•	•	•	•	•	11 001 101 nn nnn nnn nn nnn nnn
CCF	CY ← CY	Complement carry flag	1	4	↕	•	•	•	0	X	00 111 111
CP r	A – r	Compare Reg. r with ACC		4	↕	↕	V	↕	1	↕	10 111 rrr (B)
CP n	A – n	Compare value n with ACC		7	↕	↕	V	↕	1	↕	11 111 110 nn nnn nnn
CP (HL)	A – (HL)	Compare loc. (HL) with ACC		7	↕	↕	V	↕	1	↕	10 111 110
CP (IX + d)	A – (IX + d)	Compare loc. (IX + d) with ACC		19	↕	↕	V	↕	1	↕	11 011 101 10 111 110 dd ddd ddd
CP (IY + d)		Compare loc. (IY + d) with ACC		19	↕	↕	V	↕	1	↕	11 111 101 10 111 110 dd ddd ddd
CPD	A – (HL) HL ← HL – 1 BC ← BC – 1	Compare location (HL) and ACC, decrement HL and BC	2	16	•	↕(2)	↕(1)	↕	1	↕	11 101 101 10 101 001
CPDR	A – (HL) HL ← HL – 1 BC ← BC – 1 until A = (HL) or BC = 0	Compare location (HL) and ACC, decrement HL and BC, repeat until BC = 0	2	21 if BC = 0 and A ≠ (HL) 16 if BC = 0 or A = (HL)	•	↕(2)	↕(1)	↕	1	↕	11 101 101 10 111 001

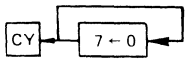
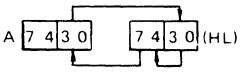
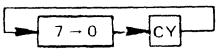
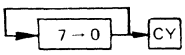
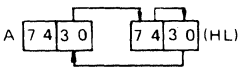
MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
CPI	A – (HL) HL ← HL + 1 BC ← BC – 1	Compare location (HL) and ACC, increment HL and decrement BC	2	16	•	↕②	↕①	↕	1	↕	11 101 101 10 100 001
CPIR	A – (HL) HL ← HL + 1 BC ← BC – 1 until A = (HL) or BC = 0	Compare location (HL) and ACC, increment HL, decrement BC Repeat until BC = C	2	21 if BC = 0 and A ≠ (HL) 16 if BC = 0 or A = (HL)	•	↕②	↕①	↕	1	↕	11 101 101 10 110 001
CPL	A ← A	Complement ACC (1's comp.)	1	4	•	•	•	•	1	1	00 101 111
DAA		Decimal adjust ACC	1	4	↕	↕	P	↕	•	↕	00 100 111
DEC r	r ← r – 1	Decrement Reg. r		4	•	↕	V	↕	1	↕	00 rrr 101Ⓑ
DEC (HL)	(HL) ← (HL) – 1	Decrement loc. (HL)		11	•	↕	V	↕	1	↕	00 110 101
DEC (IX + d)	(IX + d) ← (IX + d) – 1	Decrement loc. (IX + d)		23	•	↕	V	↕	1	↕	11 011 101 00 110 101 dd ddd ddd
DEC (IY + d)	(IY + d) ← (IY + d) – 1	Decrement loc. (IY + d)		23	•	↕	V	↕	1	↕	11 111 101 00 110 101 dd ddd ddd
DEC IX	IX ← IX – 1	Decrement IX	2	10	•	•	•	•	•	•	11 011 101 00 101 011
DEC IY	IY ← IY – 1	Decrement IY	2	10	•	•	•	•	•	•	11 111 101 00 101 011
DEC ss	ss ← ss – 1	Decrement Reg. pair ss	1	6	•	•	•	•	•	•	00 ss1 011Ⓐ
DI	IFF ← 0	Disable interrupts	1	4	•	•	•	•	•	•	11 110 011
DJNZ, e	B ← B – 1 if B = 0 continue if B ≠ 0 PC ← PC + e	Decrement B and jump relative if B = 0	2	8	•	•	•	•	•	•	00 010 000 ◄—e-2—►
EI	IFF ← 1	Enable interrupts	1	4	•	•	•	•	•	•	11 111 011
EX (SP), HL	H ↔ (SP + 1) L ↔ (SP)	Exchange the location (SP) and HL	1	19	•	•	•	•	•	•	11 100 011
EX (SP), IX	IX_H ↔ (SP + 1) IX_L ↔ (SP)	Exchange the location (SP) and IX	2	23	•	•	•	•	•	•	11 011 101 11 100 011
EX (SP), IY	IY_H ↔ (SP + 1) IY_L ↔ (SP)	Exchange the location (SP) and IY	2	23	•	•	•	•	•	•	11 111 101 11 100 011
EX AF, AF'	AF ↔ AF'	Exchange the contents of AF AF	1	4	•	•	•	•	•	•	00 001 000
EX DE, HL	DE ↔ HL	Exchange the contents of DE and HL	1	4	•	•	•	•	•	•	11 101 011
EXX	BC ↔ BC' DE ↔ DE' HL ↔ HL'	Exchange the contents of BC, DE, HL with contents of BC', DE', HL', respectively	1	4	•	•	•	•	•	•	11 011 001
HALT	Processor Halted	HALT (wait for interrupt or reset)	1	4	•	•	•	•	•	•	01 110 110
IM 0		Set Interrupt mode 0	2	8	•	•	•	•	•	•	11 101 101 01 000 110
IM 1		Set Interrupt mode 1	2	8	•	•	•	•	•	•	11 101 101 01 010 110
IM 2		Set Interrupt mode 2	2	8	•	•	•	•	•	•	11 101 101 01 011 110
IN A, (n)	A ← (n)	Load ACC with input from device n	2	11	•	•	•	•	•	•	11 011 011 nn nnn nnn
IN r, (C)	r ← (C)	Load Reg. r with input from device (C)	2	12	•	↕	P	↕	0	↕	11 101 101Ⓘ 01 rrr 000
INC (HL)	(HL) ← (HL) + 1	Increment location (HL)	1	11	•	↕	V	↕	0	↕	00 110 100
INC IX	IX ← IX + 1	Increment IX	2	10	•	•	•	•	•	•	11 011 101 00 100 011
INC (IX + d)	(IX + d) ← (IX + d) + 1	Increment location (IX + d)	3	23	•	↕	V	↕	0	↕	11 011 101 00 110 100 dd ddd ddd
INC IY	IY ← IY + 1	Increment IY	2	10	•	•	•	•	•	•	11 111 101 00 100 011
INC (IY + d)	(IY + d) ← (IY + d) + 1	Increment location (IY + d)	3	23	•	↕	V	↕	0	↕	11 111 101 00 110 100 dd ddd ddd
INC r	r ← r + 1	Increment Reg. r	1	4	•	↕	V	↕	0	↕	00 rrr 100Ⓑ
INC ss	ss ← ss + 1	Increment Reg. pair ss	1	6	•	•	•	•	•	•	00 ss0 011Ⓐ
IND	(HL) ← (C) B ← B – 1 HL ← HL – 1	Load location (HL) with input from port (C), decrement HL and B	2	16	•	↕③	X	X	1	X	11 101 101 10 101 010

MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
INDR	(HL) ← (C) B ← B – 1 HL ← HL – 1 until B = 0	Load location (HL) with input from port (C), decrement HL and decrement B, repeat until B = 0	2	21	•	1	X	X	1	X	11 101 101 10 111 010
INI	(HL) ← (C) B ← B – 1 HL ← HL + 1	Load location (HL) with input from port (C); and increment HL and decrement B	2	16	•	↕③	X	X	1	X	11 101 101 10 100 010
INIR	(HL) ← (C) B ← B – 1 HL ← HL + 1 until B = 0	Load location (HL) with input from port (C), increment HL and decrement B, repeat until B = 0	2	21	•	1	X	X	1	X	11 101 101 10 110 010
JP (HL)	PC ← HL	Unconditional jump to (HL)	1	4	•	•	•	•	•	•	11 101 001
JP (IX)	PC ← IX	Unconditional jump to (IX)	2	8	•	•	•	•	•	•	11 011 101 11 101 001
JP (IY)	PC ← IY	Unconditional jump to (IY)	2	8	•	•	•	•	•	•	11 111 101 11 101 001
JP cc, nn	If cc true PC ← nn else continue	Jump to location nn if condition cc is true	3	10	•	•	•	•	•	•	11 ←cc→ 010Ⓗ nn nnn nnn nn nnn nnn
JP nn	PC ← nn	Unconditional jump to location nn	3	10	•	•	•	•	•	•	11 000 011 nn nnn nnn nn nnn nnn
JR C, e	If C = 0 continue If C = 1 PC ← PC + e	Jump relative to PC + e, if carry = 1	2	7 if condition met. 12, if not	•	•	•	•	•	•	00 111 000 ◄— e-2 —►
JR e	PC ← PC + e	Unconditional jump relative to PC + e	2	12	•	•	•	•	•	•	00 011 000 ◄— e-2 —►
JR NC, e	If C = 1 continue If C = 0 PC ← PC + e	Jump relative to PC + e if carry = 0	2	7	•	•	•	•	•	•	00 110 000 ◄— e-2 —►
JR NZ, e	If Z = 1 continue	Jump relative to PC + e if non-zero (Z = 0)	2	7	•	•	•	•	•	•	00 100 000 ◄— e-2 —►
JR Z, e	If Z = 0 continue	Jump relative to PC + e if zero (Z = 1)	2	7	•	•	•	•	•	•	00 101 000 ◄— e-2 —►
LD A, (BC)	A ← (BC)	Load ACC with location (BC)	1	7	•	•	•	•	•	•	00 001 010
LD A, (DE)	A ← (DE)	Load ACC with location (DE)	1	7	•	•	•	•	•	•	00 011 010
LD A, I	A ← I	Load ACC with I	2	9	•	↕	IFF	↕	0	0	11 101 101 01 010 111
LD A, (nn)	A ← (nn)	Load ACC with location nn	3	13	•	•	•	•	•	•	00 111 010 nn nnn nnn nn nnn nnn
LD A, R	A ← R	Load ACC with Reg. R	2	9	•	↕	IFF	↕	0	0	11 101 101 01 011 111
LD (BC), A	(BC) ← A	Load location (BC) with ACC	1	7	•	•	•	•	•	•	00 000 010
LD (DE), A	(DE) ← A	Load location (DE) with ACC	1	7	•	•	•	•	•	•	00 010 010
LD (HL), n	(HL) ← n	Load location (HL) with value n	2	10	•	•	•	•	•	•	00 110 110 nn nnn nnn
LD ss, nn	ss ← nn	Load Reg. pair ss with value nn	4	20	•	•	•	•	•	•	00 ss0 001Ⓐ nn nnn nnn nn nnn nnn
LD HL, (nn)	H ← (nn + 1) L ← (nn)	Load HL with location (nn)	3	16	•	•	•	•	•	•	00 101 010 nn nnn nnn nn nnn nnn
LD (HL), r	(HL) ← r	Load location (HL) with Reg. r	1	7	•	•	•	•	•	•	01 110 rrrⒷ
LD I, A	I ← A	Load I with ACC	2	9	•	•	•	•	•	•	11 101 101 01 000 111
LD IX, nn	IX ← nn	Load IX with value nn	4	19	•	•	•	•	•	•	11 011 101 00 100 001 nn nnn nnn nn nnn nnn
LD IX, (nn)	IX_H ← (nn + 1) IX_L ← (nn)	Load IX with location (nn)	4	20	•	•	•	•	•	•	11 011 101 00 101 010 nn nnn nnn nn nnn nnn
LD (IX + d), n	(IX + d) ← n	Load location (IX + d) with value n	4	19	•	•	•	•	•	•	11 011 101 00 110 110 dd ddd ddd nn nnn nnn
LD (IX + d), r	(IX + d) ← r	Load location (IX + d) with Reg. r	3	19	•	•	•	•	•	•	11 011 101Ⓑ 01 110 rrr dd ddd ddd

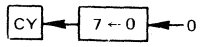
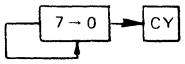
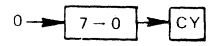
MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
LD IY, nn	IY ← nn	Load IY with value nn	4	14	•	•	•	•	•	•	11 111 101 00 100 001 nn nnn nnn nn nnn nnn
LD IY, (nn)	IY_H ← (nn + 1) IY_L ← (nn)	Load IY with location (nn)	4	20	•	•	•	•	•	•	11 111 101 00 101 010 nn nnn nnn nn nnn nnn
LD ss, (nn)	ss_H ← (nn + 1) ss_L ← (nn)	Load Reg. pair dd with location (nn)	4	20	•	•	•	•	•	•	11 101 101 Ⓐ 01 ss1 011 nn nnn nnn nn nnn nnn
LD (IY + d), n	(IY + d) ← n	Load (IY + d) with value n	4	19	•	•	•	•	•	•	11 111 101 00 110 110 dd ddd ddd nn nnn nnn
LD (IY + d), r	(IY + d) ← r	Load location (IY + d) with Reg. r	3	19	•	•	•	•	•	•	11 111 101 Ⓑ 01 110 rrr dd ddd ddd
LD (nn), A	(nn) ← A	Load location (nn) with ACC	3	13	•	•	•	•	•	•	00 110 010 nn nnn nnn nn nnn nnn
LD (nn), ss	(nn + 1) ← ss_H (nn) ← ss_L	Load location (nn) with Reg. pair dd	4	20	•	•	•	•	•	•	11 101 101 Ⓐ 01 ss0 011 nn nnn nnn nn nnn nnn
LD (nn), HL	(nn + 1) ← H (nn) ← L	Load location (nn) with HL	3	16	•	•	•	•	•	•	00 100 010 nn nnn nnn nn nnn nnn
LD (nn), IX	(nn + 1) ← IX_H (nn) ← IX_L	Load location (nn) with IX	4	20	•	•	•	•	•	•	11 011 101 00 100 010 nn nnn nnn nn nnn nnn
LD (nn), IY	(nn + 1) ← IY_H (nn) ← IY_L	Load location (nn) with IY	4	20	•	•	•	•	•	•	11 111 101 00 100 010 nn nnn nnn nn nnn nnn
LD R, A	R ← A	Load R with ACC	2	9	•	•	•	•	•	•	11 101 101 01 001 111
LD r, (HL)	r ← (HL)	Load Reg. r with location (HL)	1	7	•	•	•	•	•	•	01 rrr 110 Ⓑ
LD r, (IX + d)	r ← (IX + d)	Load Reg. r with location (IX + d)	3	19	•	•	•	•	•	•	11 011 101 Ⓑ 01 rrr 110 dd ddd ddd
LD r, (IY + d)	r ← (IY + d)	Load Reg. r with location (IY + d)	3	19	•	•	•	•	•	•	11 111 101 Ⓑ 01 rrr 110 dd ddd ddd
LD r, n	r ← n	Load Reg. r with value n	2	7	•	•	•	•	•	•	00 rrr 110 Ⓑ nn nnn nnn
LD, r, r'	r ← r'	Load Reg. r with Reg. r	1	4	•	•	•	•	•	•	01 rrr r'r'r' Ⓕ
LD SP, HL	SP ← HL	Load SP with HL	1	6	•	•	•	•	•	•	11 111 001
LD SP, IX	SP ← IX	Load SP with IX	2	10	•	•	•	•	•	•	11 011 101 11 111 001
LD SP, IY	SP ← IY	Load SP with IY	2	10	•	•	•	•	•	•	11 111 101 11 111 001
LDD	(DE) ← (HL) DE ← DE − 1 HL ← HL − 1 BC ← BC − 1	Load location (DE) with location (HL), decrement DE, HL and BC	2	16	•	•	↕	•	0	0	11 101 101 10 101 000
LDDR	(DE) ← (HL) DE ← DE − 1 HL ← HL − 1 BC ← BC − 1 until BC = 0	Load location (DE) with location (HL)	2	21	•	•	0	•	0	0	11 101 101 10 111 000
LDI	(DE) ← (HL) DE ← DE + 1 HL ← HL + 1 BC ← BC − 1	Load location (DE) with location (HL), increment DE, HL; decrement BC	2	16	•	•	↕①	•	0	0	11 101 101 10 100 000
LDIR	(DE) ← (HL) DE ← DE + 1 HL ← HL + 1 BC ← BC − 1 until BC = 0	Load location (DE) with location (HL), increment DE, HL; decrement BC and repeat until BC = 0	2	21 if BC ≠ 0 16 if BC = 0	•	•	0	•	0	0	11 101 101 10 110 000
NEG	A ← 0 − A	Negate ACC (2's complement)	2	8	↕	↕	V	↕	1	↕	11 101 101 01 000 100

INSTRUCTION SET TABLE (CONT.)

MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
NOP		No operation	1	4	•	•	•	•	•	•	00 000 000
OR r	A ← AV r	Logical 'OR' of Reg. r and ACC		4	0	↕	P	↕	0	↕	10 110 rrr (B)
OR n	A ← AV n	Logical 'OR' of value n and ACC		7	•	↕	P	↕	0	↕	11 110 110 nn nnn nnn
OR (HL)	A ← AV (HL)	Logical 'OR' of loc. (HL) and ACC		7	•	↕	P	↕	0	↕	10 110 110
OR (IX + d)	A ← (IX + d)	Logical 'OR' of loc. (IX + d) Λ ACC		19	•	↕	P	↕	0	↕	11 011 101 10 110 110 dd ddd ddd
OR (IY + d)	A ← AV (IY + d)	Logical 'OR' of loc. (IY + d) Λ ACC		19	•	↕	P	↕	0	↕	11 111 101 10 110 110 dd ddd ddd
OTDR	(C) ← (HL) B ← B − 1 HL ← HL − 1 until B = 0	Load output port (C) with contents of location (HL), decrement HL and B, repeat until B = 0	2	21 if B ≠ 0 16 if B = C	•	1	X	X	1	X	11 101 101 10 111 011
OTIR	(C) ← (HL) B ← B − 1 HL ← HL + 1 until B = 0	Load output port (C) with location (HL), increment HL, decrement B, repeat until B = 0	2	21 if B ≠ 0 16 if B = C	•	1	X	X	1	X	11 101 101 10 110 011
OUT (C), r	(C) ← r	Load output port (C) with Reg. r	2	12	•	•	•	•	•	•	11 101 101 (B) 01 rrr 001
OUT (n), A	(n) ← A	Load output port (n) with ACC	2	11	•	•	•	•	•	•	11 010 011 nn nnn nnn
OUTD	(C) ← (HL) B ← B − 1 HL ← HL − 1	Load output port (C) with location (HL), increment HL and decrement B	2	16	•	↕ (3)	X	X	1	X	11 101 101 10 101 011
OUTI	(C) ← (HL) B ← B − 1 HL ← HL + 1	Load output port (C) with location (HL), increment HL and decrement B	2	16	•	↕ (3)	X	X	1	X	11 101 101 10 100 011
POP IX	IX_H ← (SP + 1) IX_L ← (SP)	Load IX with top of stack	2	14	•	•	•	•	•	•	11 011 101 11 100 001
POP IY	IY_H ← (SP + 1) IY_L ← (SP)	Load IY with top of stack	2	14	•	•	•	•	•	•	11 111 101 11 100 001
POP qq	qq_H ← (SP + 1) qq_L ← (SP)	Load Reg. pair qq with top of stack	1	10	•	•	•	•	•	•	11 qq0 001 (G)
PUSH IX	(SP − 2) ← IX_L (SP − 1) ← IX_H	Load IX onto stack	2	15	•	•	•	•	•	•	11 011 101 11 100 101
PUSH IY	(SP − 2) ← IY_L (SP − 1) ← IY_H	Load IY onto stack	2	15	•	•	•	•	•	•	11 111 101 11 100 101
PUSH qq	(SP − 2) ← qq_L (SP − 1) ← qq_H	Load Reg. pair qq onto stack	1	11	•	•	•	•	•	•	11 qq0 101 (G)
RES b, r	S_b ← 0	Reset Bit b of Reg. r		8	•	•	•	•	•	•	11 001 011 (B) 10 bbb rrr (E)
RES b, (HL)	S_b ← 0, (HL)	Reset Bit b of loc. (HL)		15	•	•	•	•	•	•	11 001 011 10 bbb 110
RES b, (IX + d)	S_b ← 0, (IX + d)	Reset Bit b of loc. (IX + d)		23	•	•	•	•	•	•	11 011 101 11 001 011 dd ddd ddd 10 bbb 110
RES b, (IY + d)	S_b ← 0, (IY + d)	Reset Bit b of loc. (IY + d)		23	•	•	•	•	•	•	11 111 101 11 001 011 dd ddd ddd 10 bbb 110
RET	PC_L ← (SP) PC_H ← (SP + 1)	Return from subroutine	1	10	•	•	•	•	•	•	11 001 001
RET cc	If condition cc is false cont. else (PC_L ← (SP) PC_H ← (SP + 1)	Return from subroutine if condition cc is true	1	5 if CC false 11 if CC true	•	•	•	•	•	•	11 ←cc→ 000 (H)
RETI		Return from interrupt	2	14	•	•	•	•	•	•	11 101 101 01 001 101
RETN		Return from non-maskable interrupt	2	14	•	•	•	•	•	•	11 101 101 01 000 101
RL r		Rotate left through carry Reg. r		2	↕	↕	P	↕	0	0	11 001 011 (B) 00 010 rrr
RL (HL)		Rotate left through carry loc. (HL)		4	↕	↕	P	↕	0	0	11 001 011 00 010 110
RL (IX + d)		Rotate left through carry loc. (IX + d)		6	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 010 110
RL (IY + d)	m ≡ r, (HL), (IX + d), (IY + d), A	Rotate left through carry loc. (IY + d)		6	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 010 110
RLA		Rotate left ACC through carry	1	4	↕	•	•	•	0	0	00 010 111

MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
RLC (HL)		Rotate location (HL) left circular	2	15	↕	↕	P	↕	0	0	11 001 011 00 000 110
RLC (IX + d)		Rotate location (IX + d) left circular	4	23	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 000 110
RLC (IY + d)	 m ≡ r, (HL), (IX + d), (IY + d), A	Rotate location (IY + d) left circular	4	23	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 000 110
RLC r		Rotate Reg. r left circular	2	8	↕	↕	P	↕	0	0	11 001 011 (B) 00 000 rrr
RLCA		Rotate left circular ACC	1	4	↕	•	•	•	0	0	00 000 111
RLD		Rotate digit left and right between ACC and location (HL)	2	18	•	↕	P	↕	0	0	11 101 101 01 101 111
RR r		Rotate right through carry Reg. r		2	↕	↕	P	↕	0	0	11 001 011 (B) 00 011 rrr
RR (HL)		Rotate right through carry loc. (HL)		4	↕	↕	P	↕	0	0	11 001 011 00 011 110
RR (IX + d)		Rotate right through carry loc. (IX + d)		6	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 011 110
RR (IY + d)	 m ≡ r, (HL), (IX + d), (IY + d), A	Rotate right through carry loc. (IY + d)		6	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 011 110
RRA		Rotate right ACC through carry	1	4	↕	•	•	•	0	0	00 011 111
RRC r		Rotate Reg. r right circular		2	↕	↕	P	↕	0	0	11 001 011 (B) 00 001 rrr
RRC (HL)		Rotate loc. (HL) right circular		4	↕	↕	P	↕	0	0	11 001 011 00 001 110
RRC (IX + d)		Rotate loc. (IX + d) right circular		6	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 001 110
RRC (IY + d)	 m ≡ r, (HL), (IX + d), (IY + d), A	Rotate loc. (IY + d) right circular		6	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 001 110
RRCA		Rotate right circular ACC	1	4	↕	•	•	•	0	0	00 001 111
RRD		Rotate digit right and left between ACC and location (HL)	2	18	•	↕	P	↕	0	0	11 101 101 01 100 111
RST_t	(SP − 1) ← PC_H (SP − 2) ← PC_L PC_H ← 0, PC_L ← T	Restart to location T	1	11	•	•	•	•	•	•	11 ttt 111
SBC A, r	A ← A − r − CY	Subtract Reg. r from ACC w/carry	1	4	↕	↕	V	↕	1	↕	10 011 rrr (B)
SBC A, n	A ← A − n − CY	Subtract value n from ACC with carry		7	↕	↕	V	↕	1	↕	11 011 110 nn nnn nnn
SBC A, (HL)	A ← A − (HL) − CY	Sub. loc. (HL) from ACC w/carry		7	↕	↕	V	↕	1	↕	10 011 110
SBC A, (IX + d)	A ← A − (IX + d) − CY	Subtract loc. (IX + d) from ACC with carry		19	↕	↕	V	↕	1	↕	11 011 101 10 011 110 dd ddd ddd
SBC A, (IY + d)	A ← A − (IY + d) − CY	Subtract loc. (IY + d) from ACC with carry		19	↕	↕	V	↕	1	↕	11 111 101 10 011 110 dd ddd ddd
SBC HL, ss	HL ← HL − ss − CY	Subtract Reg. pair ss from HL with carry	2	15	↕	↕	V	↕	1	X	11 101 101 (A) 01 ss0 010
SCF	CY ← 1	Set carry flag (C = 1)	1	4	1	•	•	•	0	0	00 110 111
SET b, (HL)	$(HL)_b$ ← 1	Set Bit b of location (HL)	2	15	•	•	•	•	•	•	11 001 011 (E) 11 bbb 110
SET b, (IX + d)	$(IX + d)_b$ ← 1	Set Bit b of location (IX + d)	4	23	•	•	•	•	•	•	11 011 101 (E) 11 001 011 dd ddd ddd 11 bbb 110

INSTRUCTION SET TABLE (CONT.)

MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
SET b, (IY + d)	$(IY + d)_b \leftarrow 1$	Set Bit b of location (IY + d)	4	23	•	•	•	•	•	•	11 111 101 Ⓔ 11 001 011 dd ddd ddd 11 bbb 110
SET b, r	$r_b \leftarrow 1$	Set Bit b of Reg. r	2	8	•	•	•	•	•	•	11 001 011 Ⓑ 11 bbb rrr
SLA r		Shift Reg. r left arithmetic		8	↕	↕	P	↕	0	0	11 001 011 Ⓑ 00 100 rrr
SLA (HL)		Shift loc. (HL) left arithmetic		15	↕	↕	P	↕	0	0	11 001 011 00 100 110
SLA (IX + d)		Shift loc. (IX + d) left arithmetic		23	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 100 110
	m ≡ r, (HL), (IX + d), (IY + d)										
SLA (IY + d)		Shift loc. (IY + d) left arithmetic		23	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 100 110
SRA r		Shift Reg. r right arithmetic		8	↕	↕	P	↕	0	0	11 001 011 Ⓑ 00 101 rrr
SRA (HL)		Shift loc. (HL) right arithmetic		15	↕	↕	P	↕	0	0	11 001 011 00 101 110
SRA (IX + d)		Shift loc. (IX + d) right arithmetic		23	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 101 110
	m ≡ r, (HL), (IX + d), (IY + d)										
SRA (IY + d)		Shift loc. (IY + d) right arithmetic		23	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 101 110
SRL r		Shift Reg. r right logical		8	↕	↕	P	↕	0	0	11 001 011 Ⓑ 00 111 rrr
SRL (HL)		Shift loc. (HL) right logical		15	↕	↕	P	↕	0	0	11 001 011 00 111 110
SRL (IX + d)		Shift loc. (IX + d) right logical		23	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 111 110
	m ≡ r, (HL), (IX + d), (IY + d)										
SRL (IY + d)		Shift loc. (IY + d) right logical		23	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 111 110
SUB r	A ← A − r	Subtract Reg. r from ACC		4	↕	↕	V	↕	1	↕	10 010 rrr Ⓑ
SUB n	A ← A − n	Subtract value n from ACC		7	↕	↕	V	↕	1	↕	11 010 110 nn nnn nnn
SUB (HL)	A ← A − (HL)	Subtract loc. (HL) from ACC		7	↕	↕	V	↕	1	↕	10 010 110
SUB (IX + d)	A ← A − (IX + d)	Subtract loc. (IX + d) from ACC		19	↕	↕	V	↕	1	↕	11 011 101 10 010 110 dd ddd ddd
SUB (IY + d)	A ← A − (IY + d)	Subtract loc. (IY + d) from ACC		19	↕	↕	V	↕	1	↕	11 111 101 10 010 110 dd ddd ddd
XOR r	A ← A∀r	Exclusive 'OR' Reg. r and ACC		4	↕	↕	P	↕	1	↕	10 101 rrr Ⓑ
XOR n	A ← A∀n	Exclusive 'OR' value n and ACC		7	↕	↕	P	↕	1	↕	11 101 110 nn nnn nnn
XOR (HL)	A ← A∀ (HL)	Exclusive 'OR' loc. (HL) and ACC		7	↕	↕	P	↕	1	↕	10 101 110
XOR (IX + d)	A ← A∀ (IX + d)	Exclusive 'OR' loc. (IX + d) and ACC		19	↕	↕	P	↕	1	↕	11 011 101 10 101 110 dd ddd ddd
XOR (IY + d)	A ← A∀ (IY + d)	Exclusive 'OR' loc. (IY + d) and ACC		19	↕	↕	P	↕	1	↕	11 111 101 10 101 110 dd ddd ddd

FLAG NOTES:

① P/V flag is 0 if B-1=0, else P/V=1

② Z=1 if A=(HL), else Z=0

③ If B-1=0, Z flag set, else reset

FLAG DEFINITIONS:

• = Flag not affected

0 = Flag reset

1 = Flag set

X = Flag unknown

↕ = Flag affected according to result of operation

V = Overflow set

P = Parity set

IFF = Interrupt flip-flop set

Ⓐ

Reg	ss
BC	00
DE	01
HL	10
SP	11

Ⓑ

Reg	r
A	111
B	000
C	001
D	010
E	011
H	100
L	101

Ⓒ

Reg	pp
BC	00
DE	01
IX	10
SP	11

Ⓓ

Reg	rr
BC	00
DE	01
IY	10
SP	11

Ⓔ

Bit	b
0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

Ⓕ

Reg	r,r'
A	111
B	000
C	001
D	010
E	011
H	100
L	101

Ⓖ

Reg	qq
BC	00
DE	01
HL	10
AF	11

Ⓗ

CC	Condition		Relevant Flag
000	NZ	Non Zero	Z
001	Z	Zero	Z
010	NC	Non Carry	C
011	C	Carry	C
100	PO	Parity Odd	P/V
101	PE	Parity Even	P/V
110	P	Sign Positive	S
111	M	Sign Negative	S

Ⓘ

Reg	r
B	000
C	001
D	010
E	011
H	100
L	101
F	110
A	111

FLAG DESCRIPTION:

C = Carry/Link
Z = Zero
P/V = Parity/Overflow
S = Sign
N = Add/Subtract
H = Half Carry

PRINTED IN USA

SP780-7-78-3K-GN

μPD2114L
μPD2114L-1
μPD2114L-2
μPD2114L-3
μPD2114L-5

4096 BIT (1024 × 4 BITS) STATIC RAM

DESCRIPTION

The NEC μPD2114L is a 4096 bit static Random Access Memory organized as 1024 words by 4 bits using N-channel Silicon-gate MOS technology. It uses fully DC stable (static) circuitry throughout, in both the array and the decoding, and therefore requires no clocks or refreshing to operate and simplify system design. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

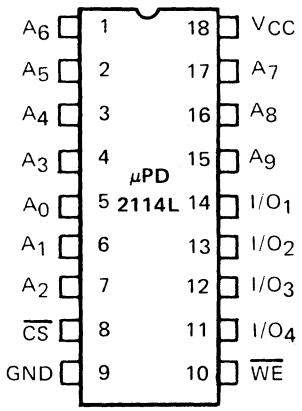
The μPD2114L is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. The μPD2114L is placed in an 18-pin package for the highest possible density.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate Chip Select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are OR-Tied.

FEATURES

- Access Time: Selection from 150-450 ns
- Single +5 Volt Supply
- Directly TTL Compatible — All Inputs and Outputs
- Completely Static — No Clock or Timing Strobe Required
- Low Operating Power — Typically 0.06 mW/Bit
- Identical Cycle and Access Times
- Common Data Input and Output using Three-State Output
- High Density 18-pin Plastic and Ceramic Packages
- Replacement for 2114L and Equivalent Devices

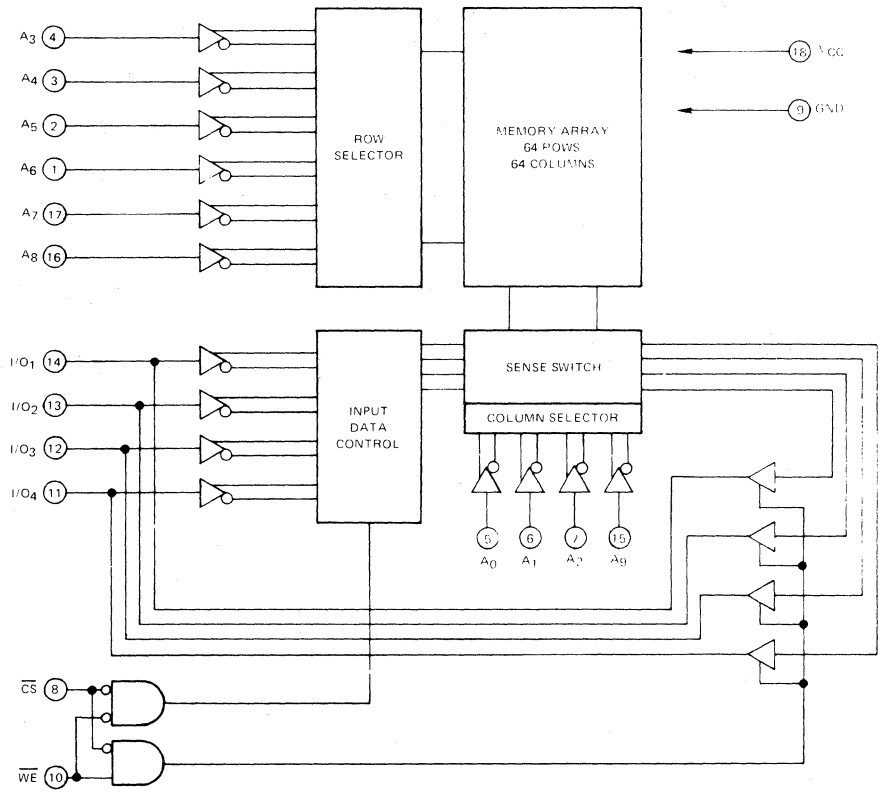
PIN CONFIGURATION



PIN NAMES

A_0-A_9	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
I/O_1-I/O_4	Data Input/Output
V_{CC}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . −10°C to +80°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on any Pin . . . . . −0.5 to +7 Volts ①
Power Dissipation . . . . . 1 Watt

Note: ① With respect to ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

CAPACITANCE

T_a = 25°C; f = 1.0 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input/Output Capacitance	$C_{I/O}$			12	pf	$V_{I/O}$ = 0V
Input Capacitance	C_{IN}			5	pf	V_{IN} = 0V

DC CHARACTERISTICS

T_a = 0°C to 70°C; V_{CC} = +5V ± 10% unless otherwise noted.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Load Current (All Input Pins)	I_{LI}			10	μA	V_{IN} = 0 to 5.5V
I/O Leakage Current	I_{LO}			10	μA	$\overline{CS}$ = 2V, $V_{I/O}$ = 0.4V to V_{CC}
Power Supply Current	I_{CC1}			65	mA	V_{IN} = 5.5V, $I_{I/O}$ = 0 mA, T_a = 25°C
Power Supply Current	I_{CC2}			70	mA	V_{IN} = 5.5V, $I_{I/O}$ = 0 mA, T_a = 0°C
Input Low Voltage	V_{IL}	−0.5		0.8	V	
Input High Voltage	V_{IH}	2.0		6.0	V	
Output Low Current	I_{OL}	3.2			mA	V_{OL} = 0.4V
Output High Current	I_{OH}			−1.0	mA	V_{OH} = 2.4V, V_{CC} = 4.75V
						V_{OH} = 2.2V, V_{CC} = 4.5V

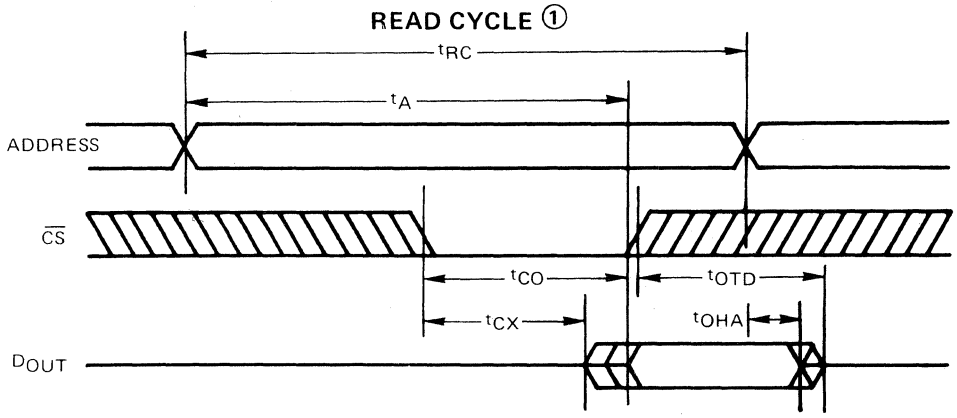
AC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 10%, unless otherwise noted.

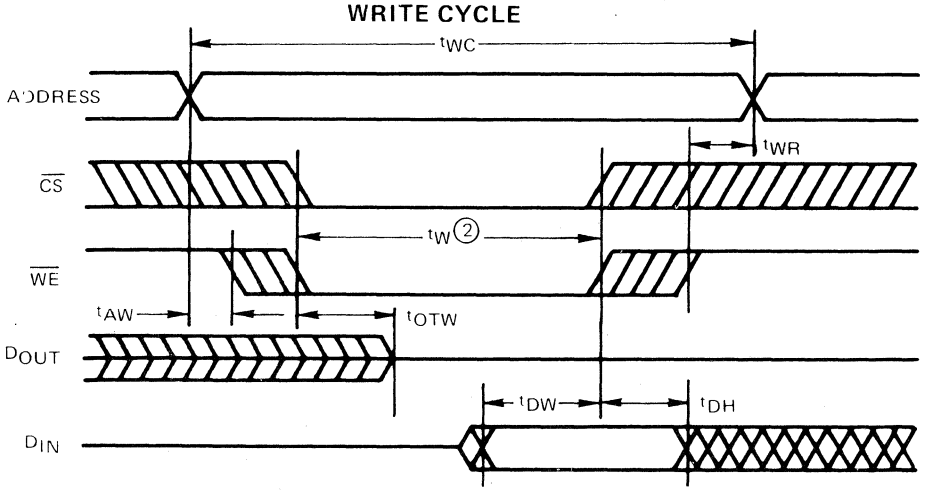
PARAMETER	SYMBOL	LIMITS										UNIT	TEST CONDITIONS
		2114L		2114L-1		2114L-2		2114L-3		2114L-5			
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ CYCLE													
Read Cycle Time	t_{RC}	450		300		250		200		150		ns	$t_T = t_r = t_f = 10$ ns
Access Time	t_A		450		300		250		200		150	ns	C_L = 100 pF
Chip Selection to Output Valid	t_{CO}		120		100		80		70		60	ns	Load = 1 TTL gate
Chip Selection to Output Active	t_{CX}	20		20		20		20		20		ns	Input Levels = 0.8 and 2.0V
Output 3-State from Deselection	t_{OTD}		100		80		70		60		50	ns	V_{ref} = 1.5V
Output Hold from Address Change	t_{OHA}	50		50		50		50		50		ns	
WRITE CYCLE													
Write Cycle Time	t_{WC}	450		300		250		200		150		ns	$t_T = t_r = t_f = 10$ ns
Write Time	t_W	200		150		120		120		80		ns	C_L = 100 pF
Write Release Time	t_{WR}	0		0		0		0		0		ns	Load = 1 TTL gate
Output 3-State from Write	t_{OTW}		100		80		70		60		50	ns	Input Levels = 0.8 and 2.0V
Data to Write Time Overlap	t_{DW}	200		150		120		120		80		ns	V_{ref} = 1.5V
Data Hold from Write Time	t_{DH}	0		0		0		0		0		ns	
Address to Write Setup Time	t_{AW}	0		0		0		0		0		ns	

TIMING WAVEFORMS

READ CYCLE ①



WRITE CYCLE

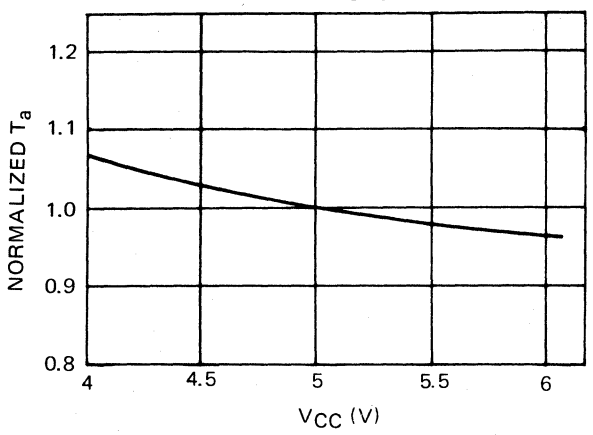


Notes: ① $\overline{WE}$ is high for Read Cycle

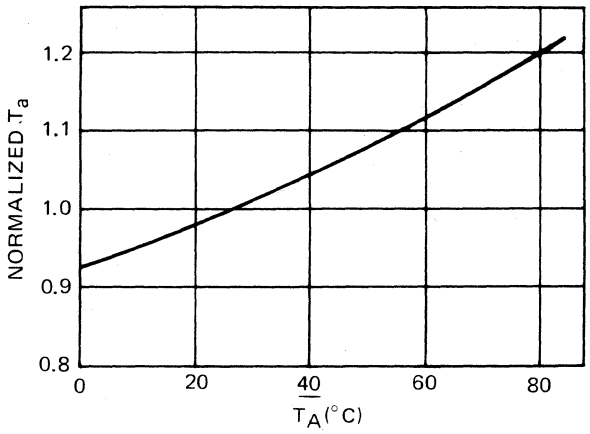
② t_W is measured from the latter of $\overline{CS}$ or $\overline{WE}$ going low to the earlier of $\overline{CS}$ or $\overline{WE}$ going high.

TYPICAL OPERATING CHARACTERISTICS

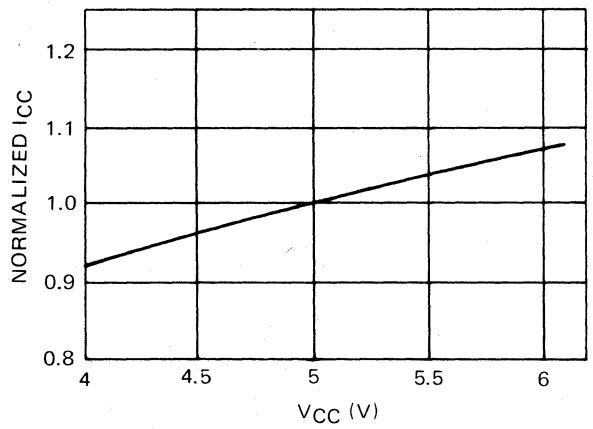
NORMALIZED ACCESS TIME VS. SUPPLY VOLTAGE



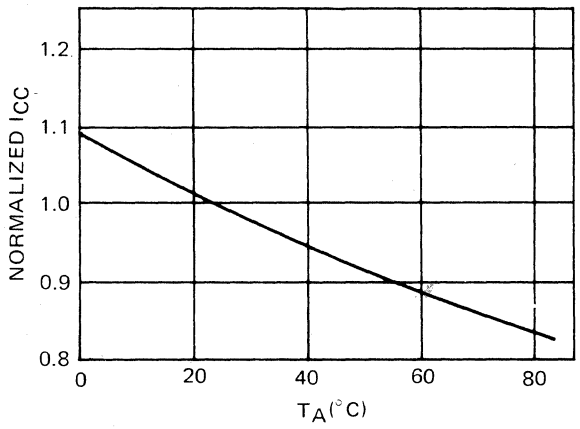
NORMALIZED ACCESS TIME VS. AMBIENT TEMPERATURE



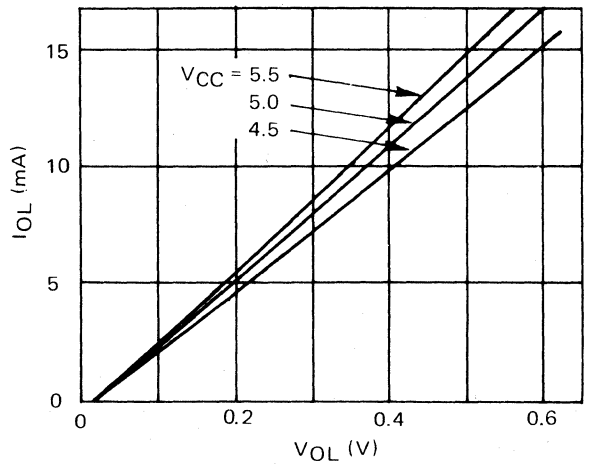
NORMALIZED POWER SUPPLY CURRENT VS. SUPPLY VOLTAGE



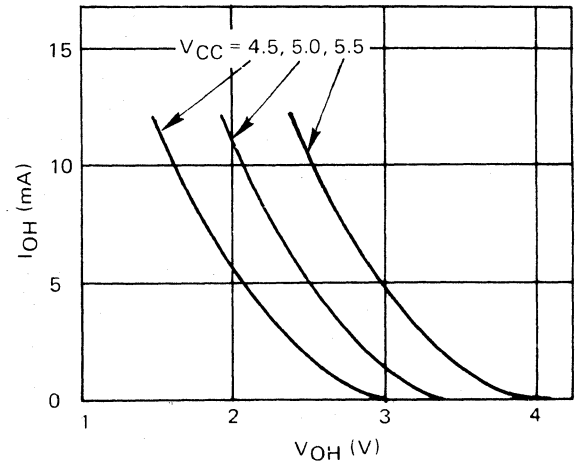
NORMALIZED POWER SUPPLY CURRENT VS. AMBIENT TEMPERATURE



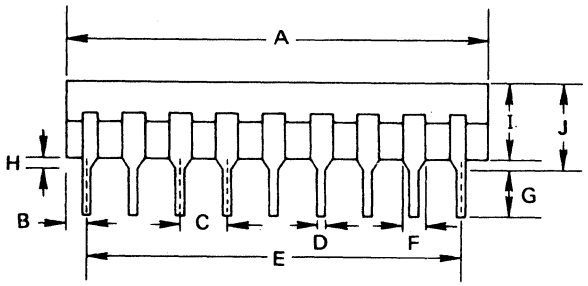
OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE

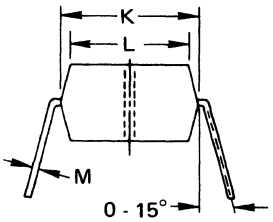


OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



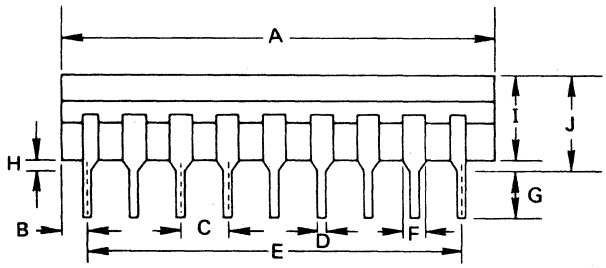
PACKAGE OUTLINES
μPD2114LC/D

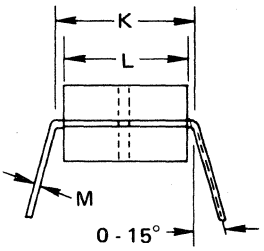




μPD2114LC (Plastic)

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01





μPD2114LD (Cerdip)

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

μPD2111AL
μPD2111AL-2
μPD2111AL-4

1024 BIT (256 x 4) STATIC MOS RAM WITH COMMON I/O AND OUTPUT DISABLE

DESCRIPTION

The μPD2111AL is a 256 words by 4 bits static random access memory fabricated with N-channel MOS technology. It uses fully static circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

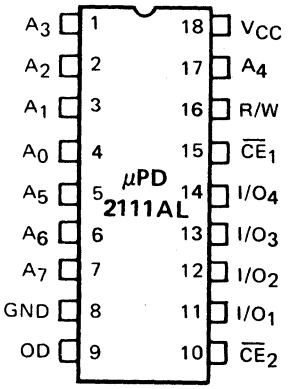
It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. Separate chip enable ($\overline{CE}$) leads allow easy selection of an individual package when outputs are OR-tied.

All members in the μPD2111AL family feature a low standby power mode with the supply voltage being reduced to +1.5V.

FEATURES

- 256 Words x 4 Bits Organization
- Common Data Input and Output
- Single +5V Supply Voltage
- Directly TTL Compatible – All Inputs and Outputs
- Static MOS – No Clocks or Refreshing Required
- Access Time – 250 ns to 450 ns max.
- Simple Memory Expansion – Chip Enable Inputs
- Fully Decoded – On Chip Address Decode
- Inputs Protected – All Inputs have Protection Against Static Charge
- Low Cost Packaging – 18 Pin Plastic Dual-In-Line Configuration
- Three-State Output – OR-Tie Capability
- Low Standby Power

PIN CONFIGURATION



PIN NAMES

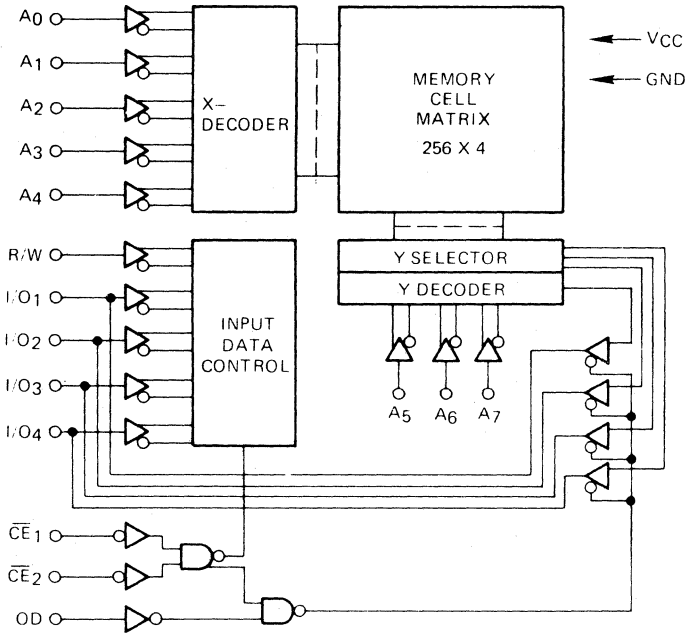
$A_0 - A_7$	Address Inputs
OD	Output Disable
R/W	Read/Write Input
$\overline{CE}_1$	Chip Enable 1
$\overline{CE}_2$	Chip Enable 2
$I/O_1 - I/O_4$	Data Input/Output

OPERATION MODES

CE_1	CE_2	OD	Chip Output Status	
0	1	0	Selected	Data Output
0	1	1		High Z
Others			Unselected	State

μPD2111AL

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−65°C to +125°C
All Output Voltages	−0.5 to +7 Volts
All Input Voltages	−0.5 to +7 Volts
Supply Voltage V_{CC}	−0.5 to +7 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = -10 to +70° C; V_{CC} = +5V ± 5%

PARAMETER		SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input High Voltage		V_{IH}	+2.0		V_{CC}	V	
Input Low Voltage		V_{IL}	−0.5		+0.8	V	
Output High Voltage	2111AL-4	V_{OH}	+2.4			V	I_{OH} = −150 μA
	2111AL 2111AL-2		+2.4			V	I_{OH} = −200 μA
Output Low Voltage		V_{OL}			+0.4	V	I_{OL} = +2.1 mA
Input Leakage Current High		I_{LIH}			+10	μA	$V_I = V_{CC}$
Input Leakage Current Low		I_{LIL}			−10	μA	V_I = 0V
Output Leakage Current High		I_{LOH}			+5	μA	V_O = +2.4V to V_{CC} $\overline{CE}$ = +2.0V
Output Leakage Current Low		I_{LOL}			−10	μA	V_O = +0.4V $\overline{CE}$ = +2.0V
Power Supply Current	2111AL-4	I_{CC1}			50	mA	V_I = +5.25V
	2111AL 2111AL-2				55	mA	I_O = 0 mA T_a = +25° C
Power Supply Current	2111AL-4	I_{CC2}			60	mA	V_I = +5.25V
	2111AL 2111AL-2				65	mA	I_O = 0 mA T_a = −10 to +70°C

AC CHARACTERISTICS

READ CYCLE

$T_a = -10°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$

PARAMETER	SYMBOL	LIMITS									UNIT
		2111AL-4			2111AL			2111AL-2			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Read Cycle Time	t_{RC}	450			350			250			ns
Access Time	t_A			450			350			250	ns
Chip Enable to Output	t_{CO}			310			240			180	ns
Output Disable to Output	t_{OD}			250			180			130	ns
Data Output to High Z State	t_{DF} ①	0		200	0		150	0		130	ns
Previous Read Data Valid After Change of Address	t_{OH}	40			40			40			ns

Note: ① t_{DF} is with respect to the trailing edge of $\overline{CE}_1$, $\overline{CE}_2$, or OD, whichever occurs first.

WRITE CYCLE

$T_a = -10°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$

PARAMETER	SYMBOL	LIMITS									UNIT
		2111AL-4			2111AL			2111AL-2			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Write Cycle Time	t_{WC}	270			220			170			ns
Write Delay	t_{AW}	20			20			20			ns
Chip Enable to Write	t_{CW}	250			200			150			ns
Data Setup Time	t_{DW}	250			200			150			ns
Data Hold Time	t_{DH}	0			0			0			ns
Write Pulse Width	t_{WP}	250			200			150			ns
Write Recovery	t_{WR}	0			0			0			ns
Output Disable Setup	t_{DS}	20			20			20			ns

Note: OD is a logical 1 for common I/O and "don't care" for separate I/O operation.

AC CONDITIONS OF TEST

Input Pulse Levels ..... +0.8V to +2.0V
Input Pulse Rise and Fall Times ..... 20 ns
Timing Measurement Reference Level 1.5V
Output Load ..... 1 TTL + 100 pF

STANDBY CHARACTERISTICS

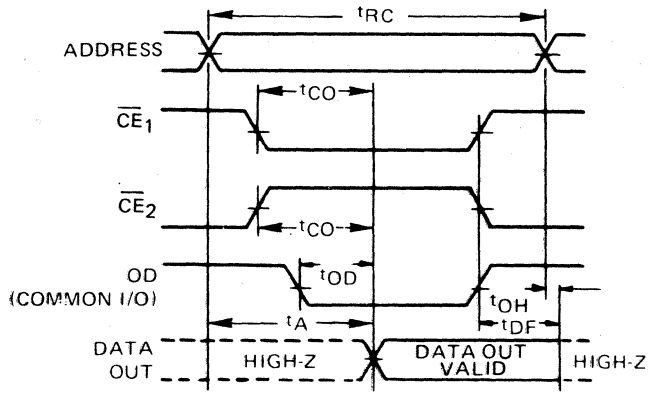
$T_a = -10°C$ to $+70°C$

PARAMETER		SYMBOL	LIMITS			UNIT	TEST CONDITIONS
			MIN	TYP ①	MAX		
V_{CC} in Standby		V_{PD}	1.5			V	
$\overline{CE}_1$ Bias in Standby		V_{CES}	2.0			V	$2.0V \leq V_{PD} \leq 5.25V$
			V_{PD}			V	$1.5V \leq V_{PD} < 2.0V$
Standby Current Drain	2111AL-4	I_{PD_1}			36	mA	All Inputs = V_{PD_1} = 1.5V
	2111AL/AL-2				38		
Standby Current Drain	2111AL-4	I_{PD_2}			45	mA	All Inputs = V_{PD_2} = 2.0V
	2111AL/AL-2				48		
Chip Deselect to Standby Time		t_{CP}	0			ns	
Standby Recovery		t_R	t_{RC} ②			ns	

Notes: ① Typical values are for $T_a = 25°C$ and nominal supply voltage
② $t_R = t_{RC}$ (Read Cycle Time)

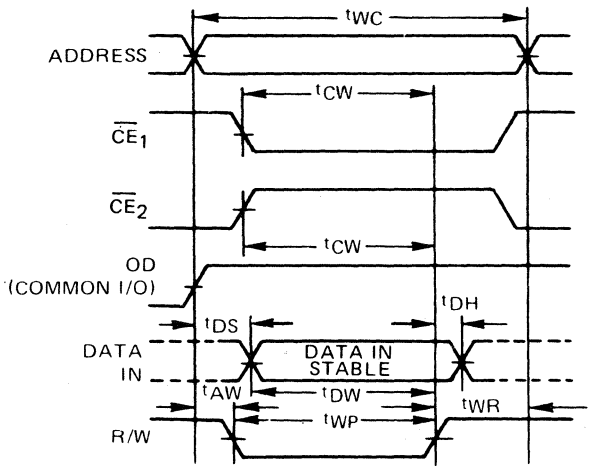
TIMING WAVEFORMS

READ CYCLE



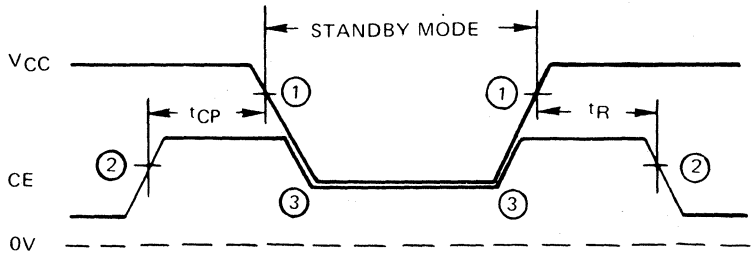
Notes: (1) OD should be tied low for separate I/O operation.
(2) R/W is high for read operation.

WRITE CYCLE



Note: OD is a logical 1 for common I/O and "don't care" for separate I/O operation.

STANDBY WAVEFORMS



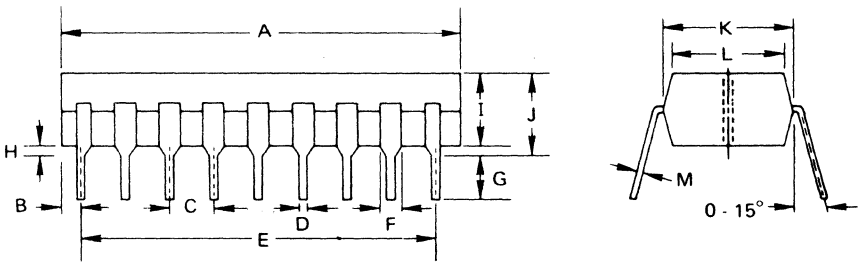
Notes: (1) 4.75V
(2) 2.0V
(3) 1.5V
(4) If the standby voltage (V_{PD}) is between 5.25V (V_{CC} Max) and 2.0V, then $\overline{CE}$ must be held at 2.0V Min (V_{IH}). If the standby voltage is less than 2.0V but greater than 1.5V (V_{PD} Min), then $\overline{CE}$ and standby voltage must be at least the same value or, if they are different, $\overline{CE}$ must be the more positive of the two. $\overline{CE}$ may be either of $\overline{CE_1}$ or $\overline{CE_2}$.

CAPACITANCE

$T_a = 25°C$; f = 1 MHz

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C_{IN}			8	pf	V_I = 0V
Output Capacitance	C_{OUT}			12	pf	V_O = 0V

PACKAGE OUTLINE μPD2111ALC



ITEM	MILLIMETERS	INCHES
A	22.5 MAX.	0.89
B	1.09	0.04
C	2.54	0.10
D	0.50 ± 0.10	0.02
E	20.32	0.80
F	1.2 MIN.	0.05
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.05 MAX.	0.16 MAX.
J	4.55 MAX.	0.18 MAX.
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	0.01

PROGRAMMABLE COMMUNICATION INTERFACE

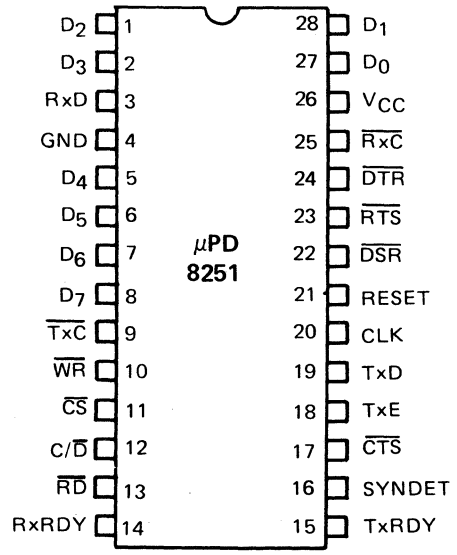
DESCRIPTION

The μPD8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART) is designed for microcomputer systems data communications. The USART is used as a peripheral and is programmed by the μPD8080 or other processor to communicate in commonly used serial data transmission techniques including IBM Bi-Sync. The USART receives serial data streams and converts them into parallel data characters for the processor. While receiving serial data, the USART will also accept data characters from the processor in parallel format, convert them to serial format and transmit. The USART will signal the processor when it has completely received or transmitted a character and requires service. Complete USART STATUS including data format errors and control signals such as TxE and SYNDET is available to the processor at any time.

FEATURES

- Asynchronous or Synchronous Operation
  - Asynchronous:
    - 5-8 Bit Characters
    - Clock Rate — 1, 16 or 64 x Baud Rate
    - Break Character Generation
    - Select 1, 1-1/2, or 2 Stop Bits
    - False Start Bit Detector
  - Synchronous:
    - 5-8 Bit Characters
    - Internal or External Character Synchronization
    - Automatic Sync Insertion
    - Single or Double Sync Characters
- Baud Rate — Synchronous — DC to 56K Baud
  — Asynchronous — DC to 9.6K Baud
- Full Duplex, Double Buffered Transmitter and Receiver
- Parity, Overrun and Framing Flags
- Fully Compatible with 8080
- All Inputs and Outputs are TTL Compatible
- Single +5 Volt Supply
- Separate Device, Receive and Transmit TTL Clocks
- 28 Pin Plastic DIP Package
- N-Channel MOS Technology

PIN CONFIGURATION



PIN NAMES

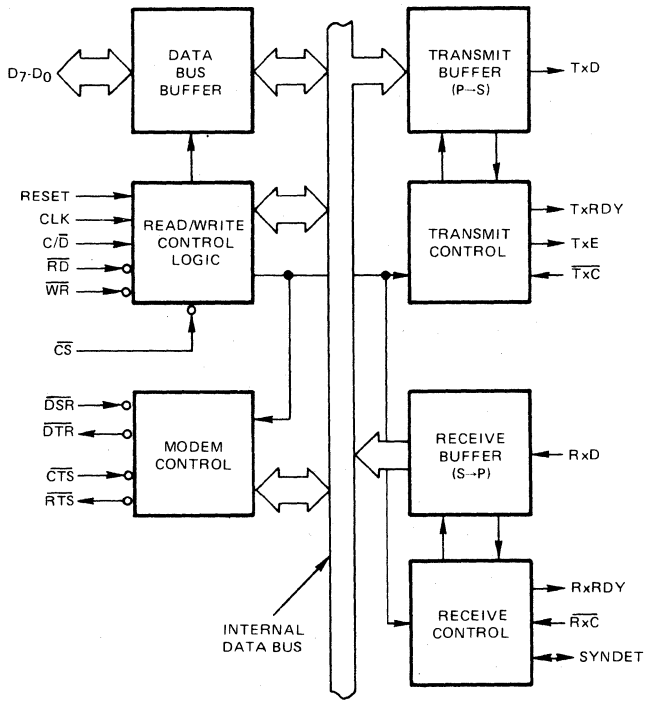
D_7-D_0	Data Bus (8 bits)
C/D	Control or Data is to be Written or Read
RD	Read Data Command
WR	Write Data or Control Command
CS	Chip Enable
CLK	Clock Pulse (TTL)
RESET	Reset
TxC	Transmitter Clock (TTL)
TxD	Transmitter Data
RxC	Receiver Clock (TTL)
RxD	Receiver Data
RxRDY	Receiver Ready (has character for 8080)
TxRDY	Transmitter Ready (ready for char. from 8080)
DSR	Data Set Ready
DTR	Data Terminal Ready
SYNDET	Sync Detect
RTS	Request to Send Data
CTS	Clear to Send Data
TxE	Transmitter Empty
V_{CC}	+5 Volt Supply
GND	Ground

FUNCTIONAL DESCRIPTION

The μPD8251 Universal Synchronous/Asynchronous Receiver/Transmitter is designed specifically for 8080 microcomputer systems but works with most 8-bit processors. Operation of the 8251, like other I/O devices in the 8080 family, is programmed by system software for maximum flexibility.

In the receive mode, a communication interface device must convert incoming serial format data into parallel data and make certain format checks on the data. And in the transmit mode, the device must format data into serial data. The device must also supply or remove characters or bits that are unique to the communication format in use. By performing conversion and formatting services automatically, the USART appears to the processor as a simple or "transparent" input or output of byte-oriented parallel data.

BLOCK DIAGRAM



BASIC OPERATION

C/D	RD	WR	CS	
0	0	1	0	8251 → Data Bus
0	1	0	0	Data Bus → 8251
1	0	1	0	Status → Data Bus
1	1	0	0	Data Bus → Control
X	X	X	1	Data Bus → 3-State
X	1	1	0	

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	-0°C to +70°C
Storage Temperature	-65°C to +125°C
All Output Voltages	-0.5 to +7 Volts
All Input Voltages	-0.5 to +7 Volts
Supply Voltages	-0.5 to +7 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

$T_a = 0°C$ to $70°C$; $V_{CC} = 5.0V \pm 5\%$; GND = 0V

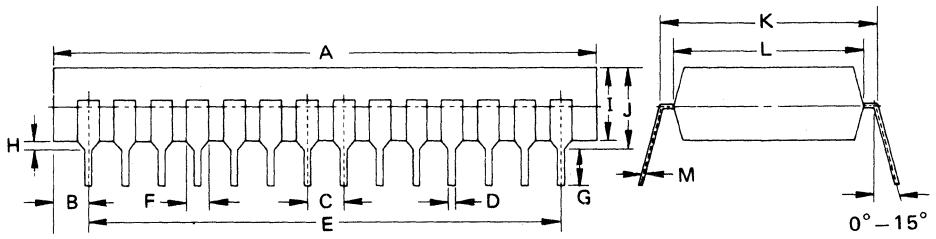
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	GND –.5		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC}	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 1.7 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = –100 μA
Data Bus Leakage	I_{DL}			–50	μA	V_{OUT} = 0.45V
				10		$V_{OUT} = V_{CC}$
Input Load Current	I_{IL}			10	μA	@5.5V
Power Supply Current	I_{CC}		45	80	mA	

CAPACITANCE

$T_a = 25°C$; V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	fc = 1 MHz
I/O Capacitance	$C_{I/O}$			20	pF	Unmeasured pins returned to GND

PACKAGE OUTLINE μPD8251C



ITEM	MILLIMETERS	INCHES
A	38.0 MAX.	1.496 MAX.
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

AC CHARACTERISTICS

BUS PARAMETERS: ①

T_a = 0°C to 70°C; V_{CC} = 5.0V ± 5%; GND = 0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
READ						
Address Stable before $\overline{READ}$, ($\overline{CS}$, C/$\overline{D}$)	t_{AR}	50			ns	
Address Hold Time for $\overline{READ}$, ($\overline{CS}$, $\overline{CD}$)	t_{RA}	5			ns	
$\overline{READ}$ Pulse Width	t_{RR}	430			ns	
Data Delay from $\overline{READ}$	t_{RD}			350	ns	C_L = 100 pF
$\overline{READ}$ to Data Floating	t_{DF}			200	ns	C_L = 100 pF
		25				C_L = 15 pF
Recovery Time Between WRITES ②	t_{RV}	6			t_{CY}	
WRITE						
Address Stable before $\overline{WRITE}$	t_{AW}	20			ns	
Address Hold Time for $\overline{WRITE}$	t_{WA}	20			ns	
$\overline{WRITE}$ Pulse Width	t_{WW}	400			ns	
Data Set-Up Time for $\overline{WRITE}$	t_{DW}	200			ns	
Data Hold Time for $\overline{WRITE}$	t_{WD}	40			ns	
OTHER TIMING						
Clock Period ③	t_{CY}	.420		1.35	μs	
Clock Pulse Width	$t_{\phi W}$	220		0.7t_{CY}	ns	
Clock Rise and Fall Time	t_R, t_F	0		50	ns	
TxD Delay from Falling Edge of $\overline{TxC}$	t_{DTx}			1	μs	C_L = 100 pF
Rx Data Set-Up Time to Sampling Pulse	t_{SRx}	2			μs	C_L = 100 pF
Rx Data Hold Time to Sampling Pulse	t_{HRx}	2			μs	C_L = 100 pF
Transmitter Input Clock Frequency	f_{Tx}					
1X Baud Rate		DC		56	KHz	
16X and 64X Baud Rate		DC		520	KHz	
Transmitter Input Clock Pulse Width	t_{TPW}					
1X Baud Rate		12			t_{CY}	
16X and 64X Baud Rate		1			t_{CY}	
Transmitter Input Clock Pulse Delay	t_{TPD}					
1X Baud Rate		15			t_{CY}	
16X and 64X Baud Rate		3			t_{CY}	
Receiver Input Clock Frequency	f_{Rx}					
1X Baud Rate		DC		56	KHz	
16X and 64X Baud Rate		DC		520	KHz	
Receiver Input Clock Pulse Width	t_{RPW}					
1X Baud Rate		12			t_{CY}	
16X and 64X Baud Rate		1			t_{CY}	
Receiver Input Clock Pulse Delay	t_{RPD}					
1X Baud Rate		15			t_{CY}	
16X and 64X Baud Rate		3			t_{CY}	
TxRDY Delay from Center of Data Bit	t_{Tx}			16	t_{CY}	C_L = 50 pF
RxRDY Delay from Center of Data Bit	t_{Rx}			20	t_{CY}	
Internal Syndet Delay from Center of Data Bit	t_{IS}			25	t_{CY}	
External Syndet Set-Up Time before Falling Edge of $\overline{RxC}$	t_{ES}	16		16	t_{CY}	
TxEMPTY Delay from Center of Data Bit	t_{TxE}			16	t_{CY}	C_L = 50 pF
Control Delay from Rising Edge of WRITE (TxE, $\overline{DTR}$, $\overline{RTS}$)	t_{WC}				t_{CY}	
Control to READ Set-Up Time ($\overline{DSR}$, $\overline{CTS}$)	t_{CR}	16			t_{CY}	

Notes: ① AC timings measured at V_{OH} = 2.0, V_{OL} = 0.8, and with load circuit of Figure 1.

② This recovery time is for initialization only, when MODE, SYNC1, SYNC2, COMMAND and first DATA BYTES are written into the USART. Subsequent writing of both COMMAND and DATA are only allowed when TxRDY = 1.

③ The TxC and RxC frequencies have the following limitations with respect to CLK.
For 1X Baud Rate, f_{Tx} or $f_{Rx} \leq 1/(30\ t_{CY})$
For 16X and 64X Baud Rate, f_{Tx} or $f_{Rx} \leq 1/(4.5\ t_{CY})$

④ Reset Pulse Width = 6 t_{CY} minimum.

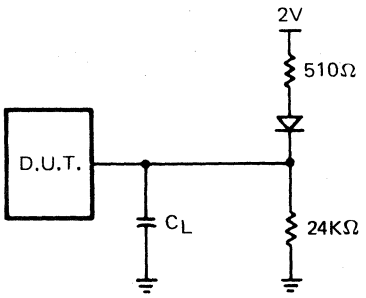
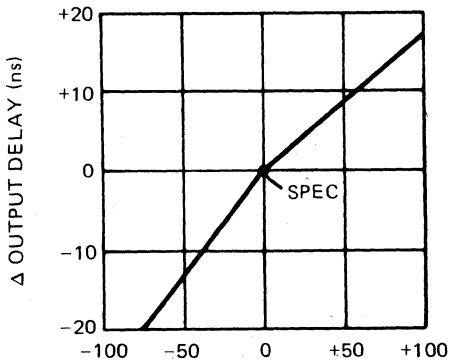


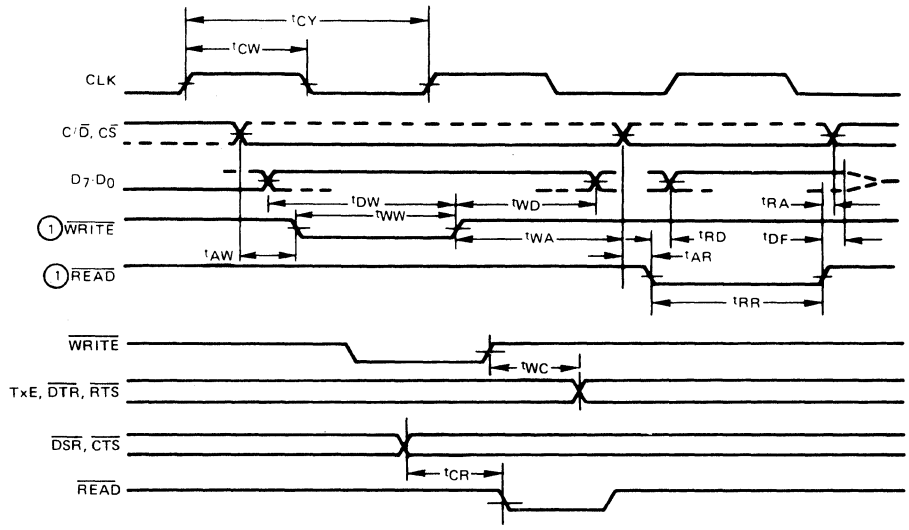
Figure 1.

TEST LOAD CIRCUIT

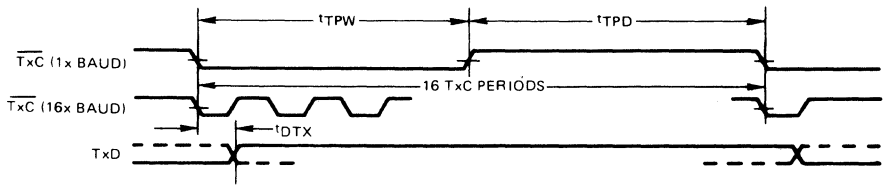


Typical Δ Output Delay Versus Δ Capacitance (pF)

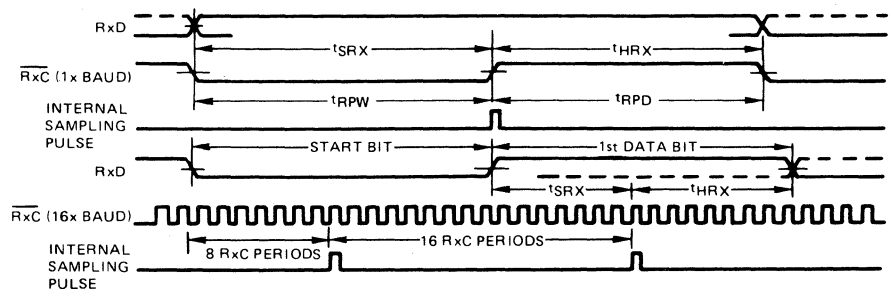
TIMING WAVEFORMS



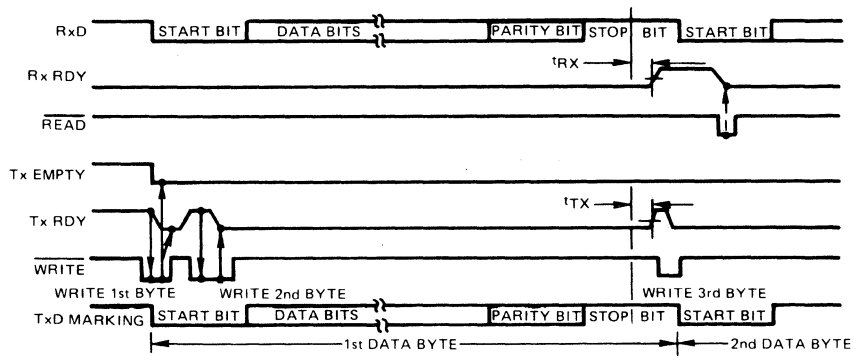
READ AND WRITE TIMING



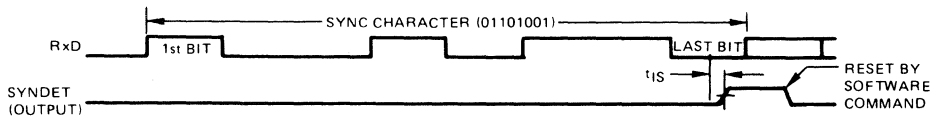
TRASNMITTER CLOCK AND DATA



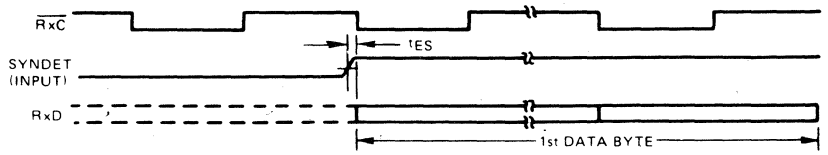
RECEIVER CLOCK AND DATA



TxRDY AND RxRDY TIMING (ASYNC MODE)



INTERNAL SYNC DETECT



EXTERNAL SYNC DETECT

Note: (1) Write and Read pulses have no timing limitation with respect to CLK.

PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
1, 2, 27, 28 5 – 8	$D_7 - D_0$	Data Bus Buffer	An 8-bit, 3-state bi-directional buffer used to interface the 8251 to the processor data bus. Data is transmitted or received by the buffer in response to input/output or Read/Write instructions from the processor. The Data Bus Buffer also transfers Control words, Command words, and Status.
26	V_{CC}	V_{CC} Supply Voltage	+5 volt supply
4	GND	Ground	Ground
Read/Write Control Logic			This logic block accepts inputs from the processor Control Bus and generates control signals for overall USART operation. The Mode Instruction and Command Instruction registers that store the control formats for device functional definition are located in the Read/ Write Control Logic.
21	RESET	Reset	A "one" on this input forces the USART into the "Idle" mode where it will remain until reinitialized with a new set of control words. Minimum RESET pulse width is t_{CY}.
20	CLK	Clock Pulse	The CLK input provides for internal device timing and is usually connected to the Phase 2 (TTL) output of the μPB8224 Clock Generator. External inputs and outputs are not referenced to CLK, but the CLK frequency must be 30 times the Receiver or Transmitter clocks in the synchronous mode and 4.5 times for the asynchronous mode.
10	$\overline{WR}$	Write Data	A "zero" on this input instructs the μPD8251 to accept the data or control word which the processor is writing out to the USART via the data bus.
13	$\overline{RD}$	Read Data	A "zero" on this input instructs the μPD8251 to place the data or status information onto the Data Bus for the processor to read.
12	C/$\overline{D}$	Control/Data	The Control/Data input, in conjunction with the $\overline{WR}$ and $\overline{RD}$ inputs, informs USART to accept or provide either a data character, control word or status information via the Data Bus. 0 = Data; 1 = Control.
11	$\overline{CS}$	Chip Select	A "zero" on this input enables the USART for reading and writing to the processor.
Modem Control			The μPD8251 has a set of control inputs and outputs which may be used to simplify the interface to a Modem.
22	$\overline{DSR}$	Data Set Ready	The Data Set Ready input can be tested by the processor via Status information. The $\overline{DSR}$ input is normally used to test Modem Data Set Ready condition.
24	$\overline{DTR}$	Data Terminal Ready	The Data Terminal Ready output can be controlled via the Command word. The $\overline{DTR}$ output is normally used to drive Modem Data Terminal Ready or Rate Select lines.
23	$\overline{RTS}$	Request to Send	The Request to Send output can be controlled via the Command word. The $\overline{RTS}$ output is normally used to drive the Modem Request to Send line.
17	$\overline{CTS}$	Clear to Send	A "zero" on the Clear to Send input enables the USART to transmit serial data if the TxEN bit in the Command Instruction register is enabled (one).

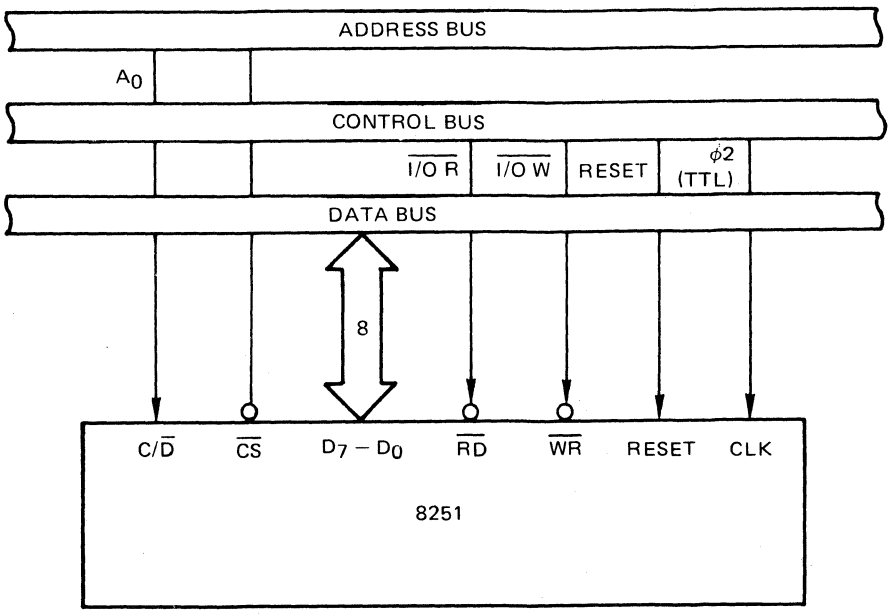
TRANSMIT BUFFER/ CONVERTER

The Transmit Buffer/Converter receives parallel data from the Data Bus Buffer via the internal data bus, converts parallel to serial data, inserts the necessary characters or bits needed for the programmed communication format and outputs composite serial data on the TxD output.

PIN IDENTIFICATION (CONT.)

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
Transmit Control Logic			The Transmit Control Logic accepts and outputs all external and internal signals necessary for serial data transmission.
15	TxRDY	Transmitter Ready	Transmitter Ready signals the processor that the transmitter is ready to accept a data character. TxRDY can be used as an interrupt or may be tested through the Status information for Polled operation. Loading a character from the processor automatically resets TxRDY.
18	TxE	Transmitter Empty	The Transmitter Empty output signals the processor that the USART has no further characters to transmit. TxE is automatically reset upon receiving a data character from the processor. In half-duplex, TxE can be used to signal end of a transmission and request the processor to "turn the line around." The TxEn bit in the command instruction does not effect TxE. In the Synchronous mode, a "one" on this output indicates that a Sync character or characters are about to be automatically transmitted as "fillers" because the next data character has not been loaded.
9	$\overline{TxC}$	Transmitter Clock	The Transmitter Clock controls the serial character transmission rate. In the Asynchronous mode, the $\overline{TxC}$ frequency is a multiple of the actual Baud Rate. Two bits of the Mode Instruction select the multiple to be 1x, 16x, or 64x the Baud Rate. In the Synchronous mode, the $\overline{TxC}$ frequency is automatically selected to equal the actual Baud Rate. Note that for both Synchronous and Asynchronous modes, serial data is shifted out of the USART by the falling edge of $\overline{TxC}$.
19	TxD	Transmitter Data	The Transmit Control Logic outputs the composite serial data stream on this pin.

8251 INTERFACE TO 8080 STANDARD SYSTEM BUS



RECEIVER BUFFER

The Receiver Buffer accepts serial data input at the $\overline{RxD}$ pin and converts the data from serial to parallel format. Bits or characters required for the specific communication technique in use are checked and then an eight-bit "assembled" character is readied for the processor. For communication techniques which require less than eight bits, the μPD8251 sets the extra bits to "zero."

PIN IDENTIFICATION (CONT.)

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
Receiver Control Logic			This block manages all activities related to incoming data.
14	RxRDY	Receiver Ready	The Receiver Ready output indicates that the Receiver Buffer is ready with an "assembled" character for input to the processor. For Polled operation, the processor can check RxRDY using a Status Read or RxRDY can be connected to the processor interrupt structure. Note that reading the character to the processor automatically resets RxRDY.
25	$\overline{RxC}$	Receiver Clock	The Receiver Clock is the rate at which the incoming character is received. In the Asynchronous mode, the $\overline{RxC}$ frequency may be 1,16 or 64 times the actual Baud Rate but in the Synchronous mode the $\overline{RxC}$ frequency must equal the Baud Rate. Two bits in the mode instruction select Asynchronous at 1x, 16x or 64x or Synchronous operation at 1x the Baud Rate. Unlike $\overline{TxC}$, data is sampled by the μPD8251 on the rising edge of $\overline{RxC}$. ①
3	RxD	Receiver Data	A composite serial data stream is received by the Receiver Control Logic on this pin.
16	SYNDET	Sync Detect	The SYNC Detect pin is only used in the Synchronous mode. The μPD8251 may be programmed through the Mode Instruction to operate in either the internal or external Sync mode and SYNDET then functions as an output or input respectively. In the internal Sync mode, the SYNDET output will go to a "one" when the μPD8251 has located the SYNC character in the Receive mode. If double SYNC character (bi-sync) operation has been programmed, SYNDET will go to "one" in the middle of the last bit of the second SYNC character. SYNDET is automatically reset to "zero" upon a Status Read or RESET. In the external SYNC mode, a "zero" to "one" transition on the SYNDET input will cause the μPD8251 to start assembling data character on the next falling edge of $\overline{RxC}$. The length of the SYNDET input should be at least one $\overline{RxC}$ period, but may be removed once the μPD8251 is in SYNC.

Note: ① Since the μPD8251 will frequently be handling both the reception and transmission for a given link, the Receive and Transmit Baud Rates will be same. $\overline{RxC}$ and $\overline{TxC}$ then require the same frequency and may be tied together and connected to a single clock source or Baud Rate Generator.

Examples:

If the Baud Rate equals 110 (Async):
- $\overline{RxC}$ or $\overline{TxC}$ equals 110 Hz (1x)
- $\overline{RxC}$ or $\overline{TxC}$ equals 1.76 KHz (16x)
- $\overline{RxC}$ or $\overline{TxC}$ equals 7.04 KHz (64x)

If the Baud Rate equals 300:
- $\overline{RxC}$ or $\overline{TxC}$ equals 300 Hz (1x) A or S
- $\overline{RxC}$ or $\overline{TxC}$ equals 4800 Hz (16x) A only
- $\overline{RxC}$ or $\overline{TxC}$ equals 19.2 KHz (64x) A only

OPERATIONAL DESCRIPTION

A set of control words must be sent to the μPD8251 to define the desired mode and communications format. The control words will specify the BAUD RATE FACTOR (1x, 16x, 64x), CHARACTER LENGTH (5 to 8), NUMBER OF STOP BITS (1, 1-1/2, 2), ASYNCHRONOUS or SYNCHRONOUS MODE, SYNDET (IN or OUT), PARITY, etc.

After receiving the control words, the μPD8251 is ready to communicate. TxRDY is raised to signal the processor that the USART is ready to receive a character for transmission. When the processor writes a character to the USART, TxRDY is automatically reset.

Concurrently, the μPD8251 may receive serial data; and after receiving an entire character, the RxRDY output is raised to indicate a completed character is ready for the processor. The processor fetch will automatically reset RxRDY.

Note: The μPD8251 may provide faulty RxRDY for the first read after power-on or for the first read after receive is re-enabled by a command instruction (RxE). A dummy read is recommended to clear faulty RxRDY. But this is not the case for the first read after hardware or software reset after the device operation has once been established.

The μPD8251 cannot transmit until the TxEN (Transmitter Enable) bit has been set by a Command Instruction and until the $\overline{CTS}$ (Clear to Send) input is a "zero". TxD is held in the "marking" state after Reset awaiting new Command Words.

μPD8251 PROGRAMMING

The USART must be loaded with a group of two to four control words provided by the processor before data reception and transmission can begin. A Reset (internal or external) must immediately proceed the control words which are used to program the complete operational description of the communications interface. If an external RESET is not available, three successive 00 Hex or two successive 80 Hex command instructions ($C/\overline{D}$ = 1) followed by a software reset command instruction (40 Hex) can be used to initialize the 8251.

There are two control word formats:

1. Mode Instruction
2. Command Instruction

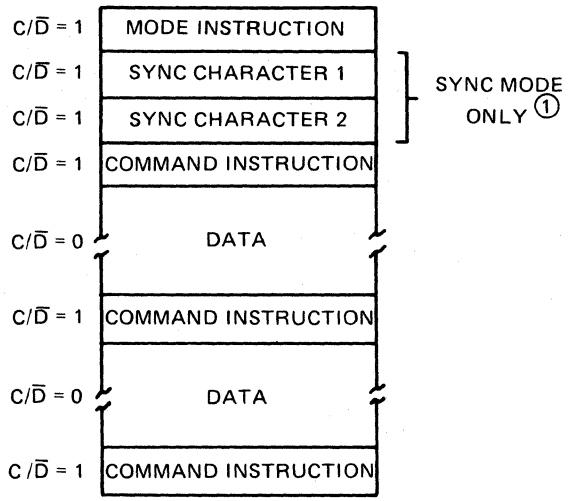
MODE INSTRUCTION

This control word specifies the general characteristics of the interface regarding the SYNCHRONOUS or ASYNCHRONOUS MODE, BAUD RATE FACTOR, CHARACTER LENGTH, PARITY, and NUMBER OF STOP BITS. Once the Mode Instruction has been received, SYNC characters or Command Instructions may be inserted depending on the Mode Instruction content.

COMMAND INSTRUCTION

This control word will be interpreted as a SYNC character definition if immediately preceded by a Mode Instruction which specified a Synchronous format. After the SYNC character(s) are specified or after an Asynchronous Mode Instruction, all sub sequent control words will be interpreted as an update to the Command Instruction. Command Instruction updates may occur at any time during the data block. To modify the Mode Instruction, a bit may be set in the Command Instruction which causes an internal Reset which allows a new Mode Instruction to be accepted.

TYPICAL DATA BLOCK



NOTE ① The second SYNC character is skipped if MODE instruction has programmed the 8251 to single character Internal SYNC Mode. Both SYNC characters are skipped if MODE instruction has programmed the 8251 to ASYNC mode.

MODE INSTRUCTION DEFINITION

The μPD8251 can operate in either Asynchronous or Synchronous communication modes. Understanding how the Mode Instruction controls the functional operation of the USART is easiest when the device is considered to be two separate components, one asynchronous and the other synchronous, which share the same support circuits and package. Although the format definition can be changed at will or "on the fly", the two modes will be explained separately for clarity.

ASYNCHRONOUS TRANSMISSION

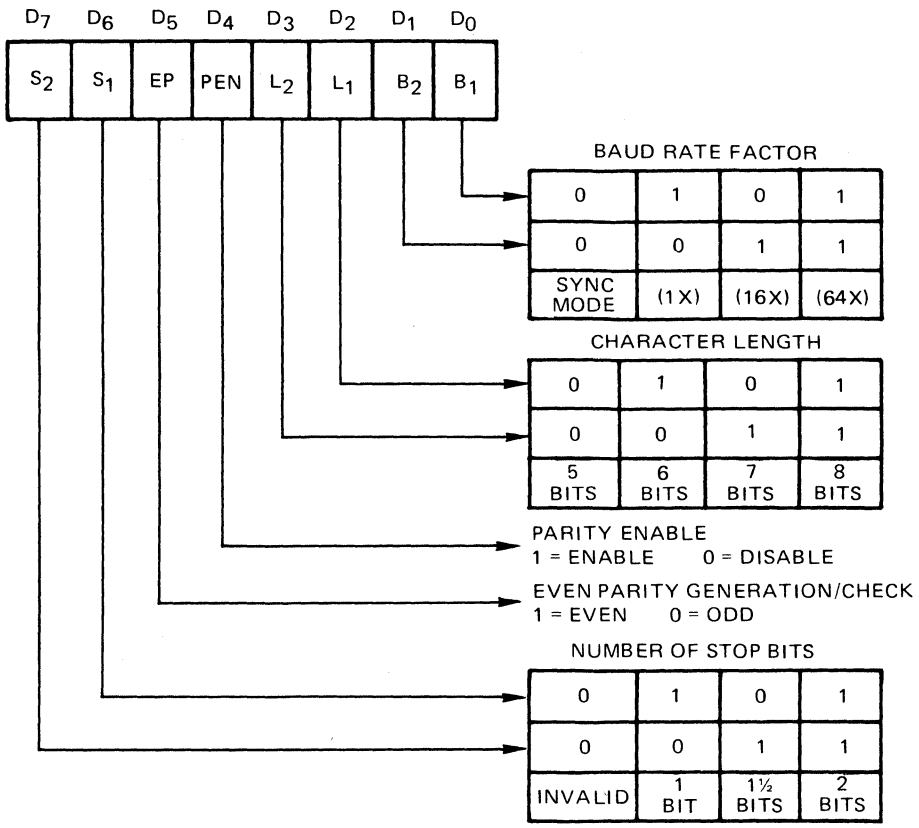
When a data character is written into the μPD8251, the USART automatically adds a START bit (low level or "space") and the number of STOP bits (high level or "mark") specified by the Mode Instruction. If Parity has been enabled, an odd or even Parity bit is inserted just before the STOP bits(s), as specified by the Mode Instruction. Then, depending on $\overline{CTS}$ and TxEN, the character may be transmitted as a serial data stream at the TxD output. Data is shifted out by the falling edge of $\overline{TxC}$ at $\overline{TxC}$, $\overline{TxC}/16$ or $\overline{TxC}/64$, as defined by the Mode Instruction.

If no data characters have been loaded into the μPD8251, or if all available characters have been transmitted, the TxD output remains "high" (marking) in preparation for sending the START bit of the next character provided by the processor. TxD may be forced to send a BREAK (continuously low) by setting the correct bit in the Command Instruction.

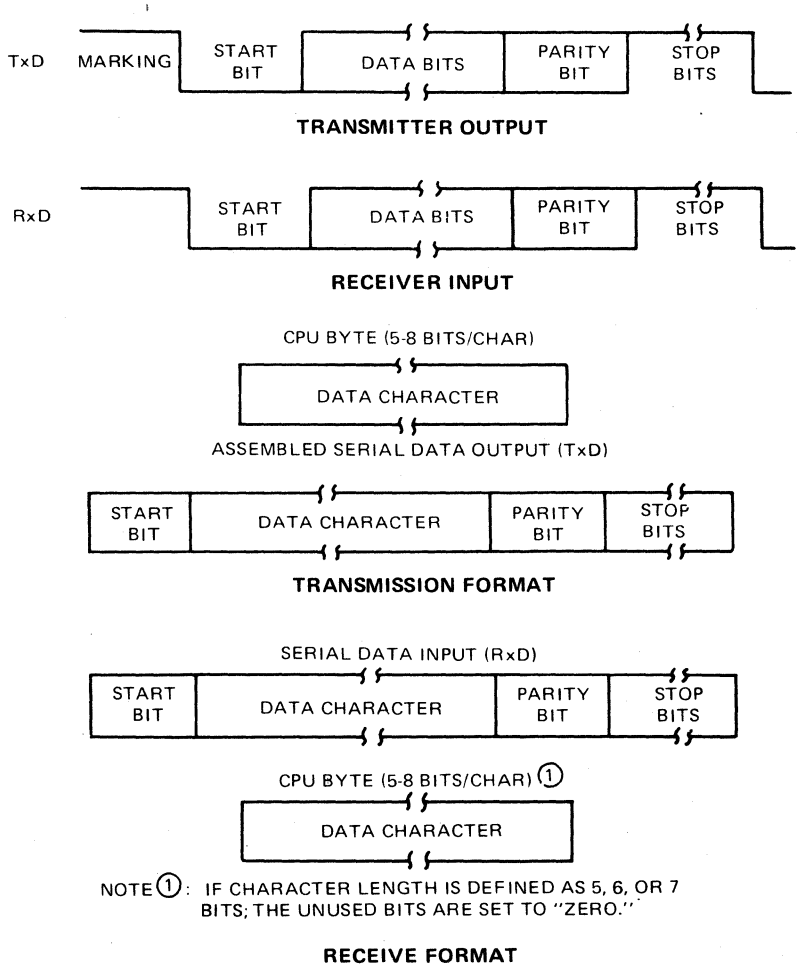
ASYNCHRONOUS RECEIVE

The RxD input line is normally held "high" (marking) by the transmitting device. A falling edge at RxD signals the possible beginning of a START bit and a new character. The START bit is checked by testing for a "low" at its nominal center as specified by the BAUD RATE. If a "low" is detected again, it is considered valid, and the bit assembling counter starts counting. The bit counter locates the approximate center of the data, parity (if specified), and STOP bits. The parity error flag (PE) is set, if a parity error occurs. Input bits are sampled at the RxD pin with the rising edge of $\overline{RxC}$. If a high is not detected for the STOP bit, which normally signals the end of an input character, a framing error (FE) will be set. After a valid STOP bit, the input character is loaded into the parallel Data Bus Buffer of the μPD8251 and the RxRDY signal is raised to indicate to the processor that a character is ready to be fetched. If the processor has failed to fetch the previous character, the new character replaces the old and the overrun flag (OE) is set. All the error flags can be reset by setting a bit in the Command Instruction. Error flag conditions will not stop subsequent USART operation.

MODE INSTRUCTION FORMAT ASYNCHRONOUS MODE



TRANSMIT/RECEIVE FORMAT ASYNCHRONOUS MODE



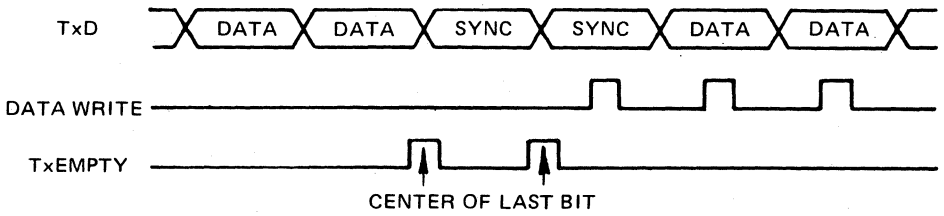
SYNCHRONOUS TRANSMISSION

As in Asynchronous transmission, the TxD output remains "high" (marking) until the μPD8251 receives the first character from the processor which is usually a SYNC character. After a Command Instruction has set TxEN and after Clear to Send ($\overline{CTS}$) goes low, the first character is serially transmitted. Data is shifted out on the falling edge of $\overline{TxC}$ and the same rate as $\overline{TxC}$.

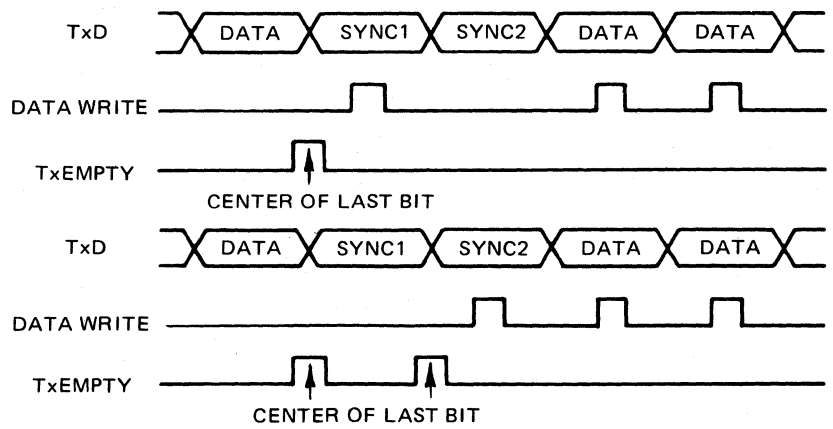
Once transmission has started, Synchronous Mode format requires that the serial data stream at TxD continue at the $\overline{TxC}$ rate or SYNC will be lost. If a data character is not provided by the processor before the μPD8251 Transmitter Buffer becomes empty, the SYNC character(s) loaded directly following the Mode Instruction will be automatically inserted in the TxD data stream. The SYNC character(s) are inserted to fill the line and maintain synchronization until new data characters are available for transmission. If the μPD8251 becomes empty, and must send the SYNC character(s), the TxEMPTY output is raised to signal the processor that the Transmitter Buffer is empty and SYNC characters are being transmitted. TxEMPTY is automatically reset by the next character from the processor.

TxEMPTY go high at the middle of the last data bit when the Transmit Register is EMPTY. TxEMPTY goes low again as sync characters are transmitted. See figure below.

FOR SINGLE SYNC CHARACTER OPERATION



FOR DOUBLE SYNC CHARACTER OPERATION (BISYNC)



SYNCHRONOUS RECEIVE

In Synchronous Receive, character synchronization can be either external or internal. If the internal SYNC mode has been selected, and the Enter HUNT (EH) bit has been set by a Command Instruction, the receiver goes into the HUNT mode.

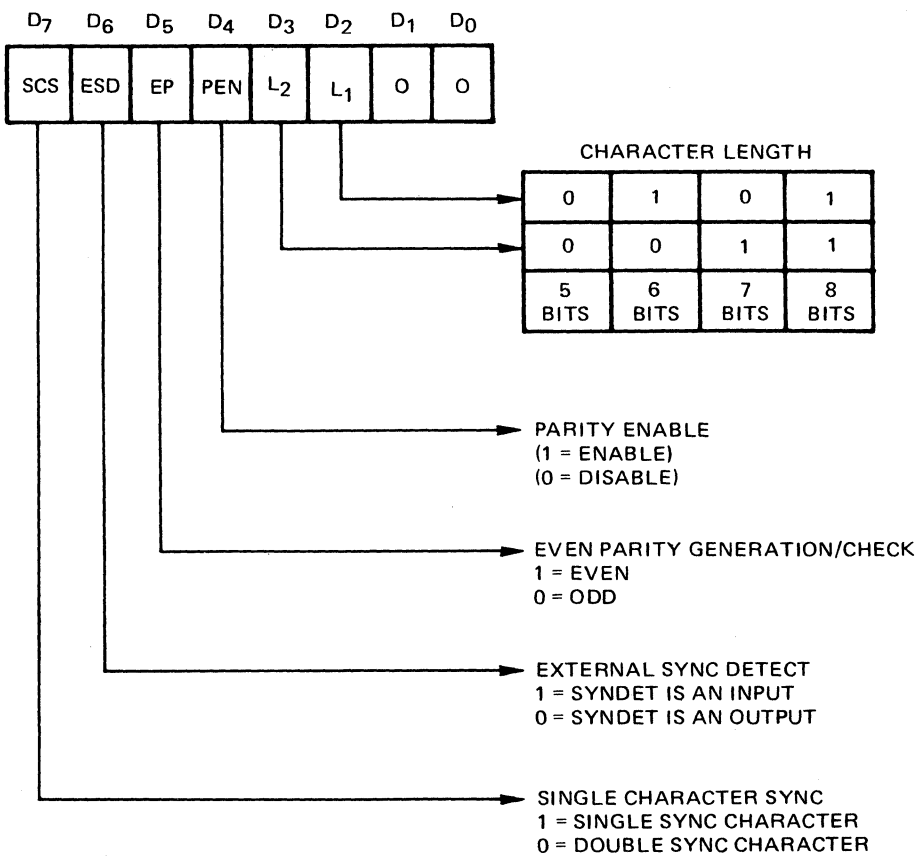
Incoming data on the RxD input is sampled on the rising edge of $\overline{RxC}$, and the Receiver Buffer is compared with the first SYNC character after each bit has been loaded until a match is found. If two SYNC characters have been programmed, the next received character is also compared. When the SYNC character(s) programmed have been detected, the μPD8251 leaves the HUNT mode and is in character synchronization. At this time, the SYNDET (output) is set high. SYNDET is automatically reset by a STATUS READ.

If external SYNC has been specified in the Mode Instruction, a "one" applied to the SYNDET (input) for at least one $\overline{RxC}$ cycle will synchronize the USART.

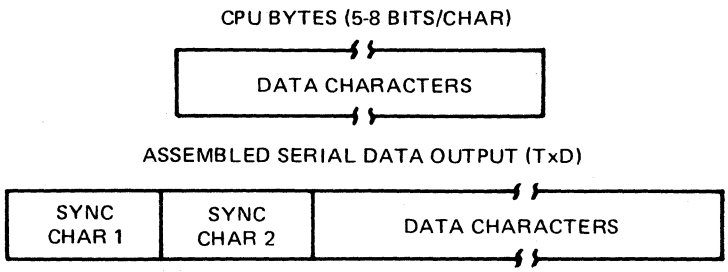
Parity and Overrun Errors are treated the same in the Synchronous as in the Asynchronous Mode. Framing errors do not apply in the Synchronous format.

The processor may command the receiver to enter the HUNT mode with a Command Instruction which sets Enter HUNT (EH) if synchronization is lost.

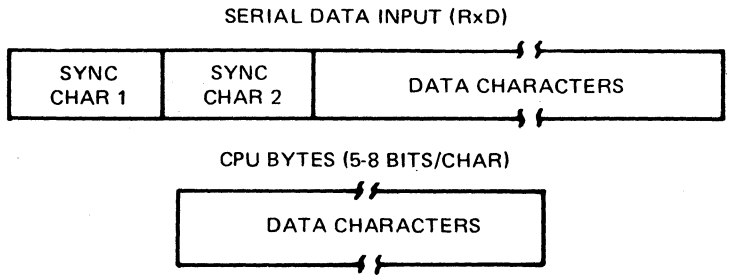
MODE INSTRUCTION FORMAT SYNCHRONOUS MODE



TRANSMIT/RECEIVE FORMAT SYNCHRONOUS MODE



TRANSMIT FORMAT



RECEIVE FORMAT

COMMAND INSTRUCTION FORMAT

After the functional definition of the μPD8251 has been specified by the Mode Instruction and the SYNC character(s) have been entered, if in SYNC mode, the USART is ready to receive Command Instructions and begin communication. A Command Instruction is used to control the specific operation of the format selected by the Mode Instruction. Enable Transmit, Enable Receive, Error Reset and Modem Controls are controlled by the Command Instruction.

After the Mode Instruction and the SYNC character(s), as needed, are loaded, all subsequent "control writes" ($C/\overline{D} = 1$) will load or overwrite the Command Instruction register. A Reset operation (internal via CMD IR or external via the RESET input) will cause the μPD8251 to interpret the next "control write", which must immediately follow the reset, as a Mode Instruction.

STATUS READ FORMAT

It is frequently necessary for the processor to examine the "status" of an active interface device to determine if errors have occurred or to notice other conditions which require a response from the processor. The μPD8251 has features which allow the processor to "read" the device status at any time. A data fetch is issued by the processor while holding the $C/\overline{D}$ input "high" to obtain device Status Information. Many of the bits in the status register are copies of external pins. This dual status arrangement allows the μPD8251 to be used in both Polled and interrupt driven environments. Status update can have a maximum delay of a 16 clock period.

PARITY ERROR

When a parity error is detected, the PE flag is set, and is cleared by setting the ER bit in a subsequent Command Instruction. PE being set does not inhibit USART operation.

OVERRUN ERROR

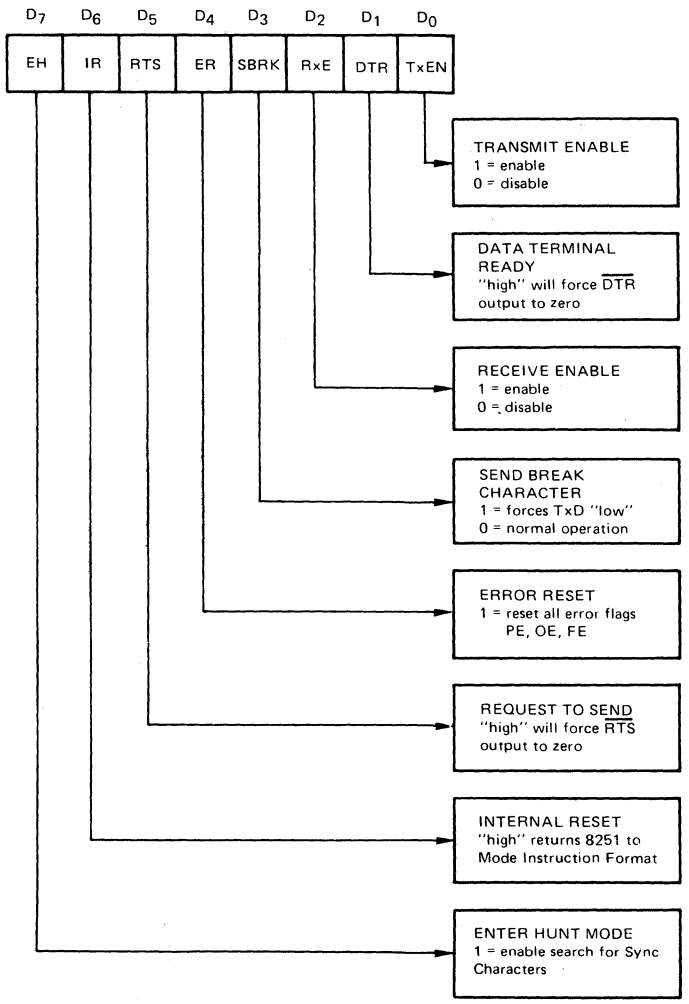
If the processor fails to read a data character before the one following is available, the OE flag is set, and is cleared by setting the ER bit in a subsequent Command Instruction. Although OE being set does not inhibit USART operation, the previously received character is overwritten and lost.

FRAMING ERROR ①

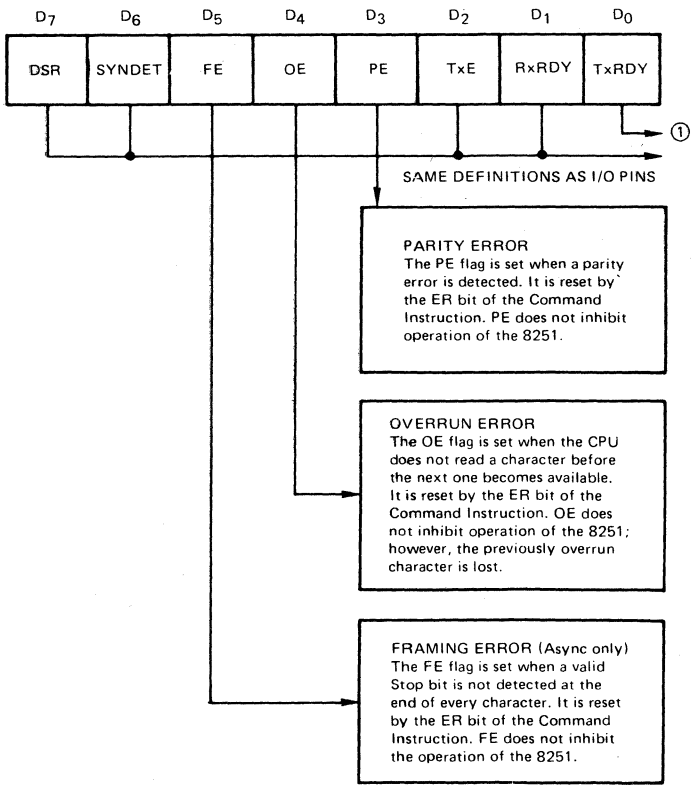
If a valid STOP bit is not detected at the end of a character, the FE flag is set, and is cleared by setting the ER bit in a subsequent Command Instruction. FE being set does not inhibit USART operation.

Note: ① ASYNC mode only.

COMMAND INSTRUCTION FORMAT



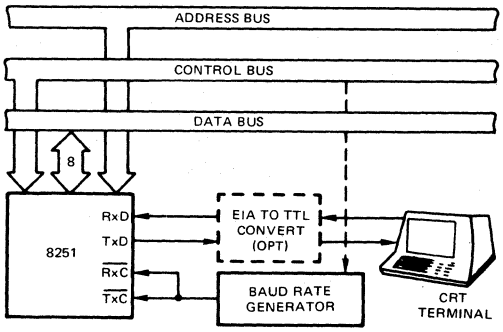
STATUS READ FORMAT



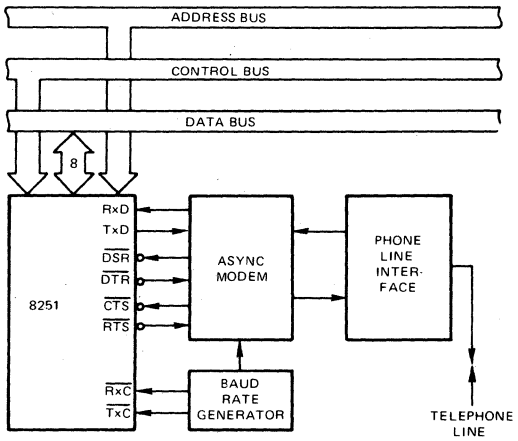
Note: ① TxRDY status bit is not totally equivalent to the TxRDY output pin, the relationship is as follows:

TxRDY status bit = DB Buffer Empty

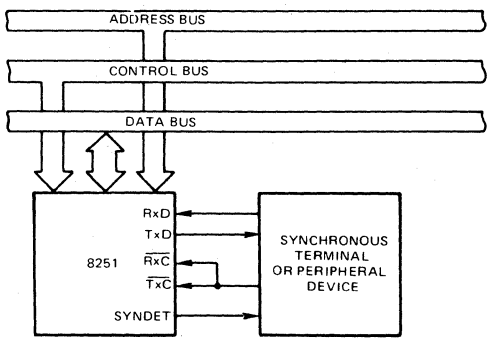
TxRDY (pin 15) = DB Buffer Empty • CTS • TxEn



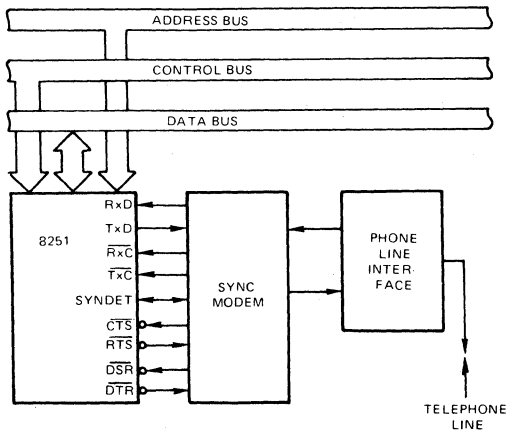
ASYNCHRONOUS SERIAL INTERFACE TO CRT TERMINAL, DC to 9600 BAUD



ASYNCHRONOUS INTERFACE TO TELEPHONE LINES



SYNCHRONOUS INTERFACE TO TERMINAL OR PERIPHERAL DEVICE



SYNCHRONOUS INTERFACE TO TELEPHONE LINES

PROGRAMMABLE PERIPHERAL INTERFACES

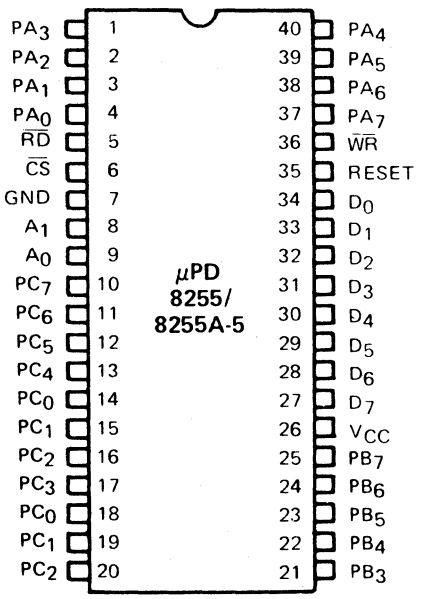
DESCRIPTION

The μPD8255 and μPD8255A-5 are general purpose programmable INPUT/OUTPUT devices designed for use with the 8080A/8085A microprocessors. Twenty-four (24) I/O lines may be programmed in two groups of twelve (group I and group II) and used in three modes of operation. In the Basic mode, (MODE 0), each group of twelve I/O pins may be programmed in sets of 4 to be input or output. In the Strobed mode, (MODE 1), each group may be programmed to have 8 lines of input or output. Three of the remaining four pins in each group are used for handshaking strobes and interrupt control signals. The Bidirectional Bus mode, (MODE 2), uses the 8 lines of Port A for a bidirectional bus, and five lines from Port C for bus control signals. The μPD8255 and μPD8255A-5 are packaged in 40 pin plastic dual-in-line packages.

FEATURES

- Fully Compatible with the 8080A/8085 Microprocessor Families
- All Inputs and Outputs TTL Compatible
- 24 Programmable I/O Pins
- Direct Bit SET/RESET Eases Control Application Interfaces
- 8 – 2 mA Darlington Drive Outputs for Printers and Displays (μPD8255)
- 8 – 4 mA Darlington Drive Outputs for Printers and Displays (μPD8255A-5)
- LSI Drastically Reduces System Package Count
- Standard 40 Pin Dual-In-Line Plastic Package

PIN CONFIGURATION



PIN NAMES

D_7-D_0	Data Bus (Bi-Directional)
RESET	Reset Input
$\overline{CS}$	Chip Select
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A_0, A_1	Port Address
PA_7-PA_0	Port A (Bit)
PB_7-PB_0	Port B (Bit)
PC_7-PC_0	Port C (Bit)
V_{CC}	+5 Volts
GND	0 Volts

*All data pertaining to the μPD8255A-5 is preliminary.

FUNCTIONAL DESCRIPTION

General

The μPD8255 and μPD8255A-5 Programmable Peripheral Interfaces (PPI) are designed for use in 8080A/8085A microprocessor systems. Peripheral equipment can be effectively and efficiently interfaced to the 8080A/8085A data and control busses with the μPD8255 and μPD8255A-5. The μPD8255 and μPD8255A-5 are functionally configured to be programmed by system software to avoid external logic for peripheral interfaces.

Data Bus Buffer

The 3-state, bidirectional, eight bit Data Bus Buffer (D_0-D_7) of the μPD8255 and μPD8255A-5 can be directly interfaced to the processor's system Data Bus (D_0-D_7). The Data Bus Buffer is controlled by execution of IN and OUT instructions by the processor. Control Words and Status information are also transmitted via the Data Bus Buffer.

Read/Write and Control Logic

This block manages all of the internal and external transfers of Data, Control and Status. Through this block, the processor Address and Control busses can control the peripheral interfaces.

Chip Select, $\overline{CS}$, pin 6

A Logic Low, V_{IL}, on this input enables the μPD8255 and μPD8255A-5 for communication with the 8080A/8085A.

Read, $\overline{RD}$, pin 5

A Logic Low, V_{IL}, on this input enables the μPD8255 and μPD8255A-5 to send Data or Status to the processor via the Data Bus Buffer.

Write, $\overline{WR}$, pin 36

A Logic Low, V_{IL}, on this input enables the Data Bus Buffer to receive Data or Control Words from the processor.

Port Select 0, A_0, pin 9

Port Select 1, A_1, pin 8

These two inputs are used in conjunction with $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ to control the selection of one of three ports on the Control Word Register. A_0 and A_1 are usually connected to A_0 and A_1 of the processor Address Bus.

Reset, pin 35

A Logic High, V_{IH}, on this input clears the Control Register and sets ports A, B, and C to the input mode. The input latches in ports A, B, and C are not cleared.

Group I and Group II Controls

Through an OUT instruction in System Software from the processor, a control word is transmitted to the μPD8255 and μPD8255A-5. Information such as "MODE," "Bit SET," and "Bit RESET" is used to initialize the functional configuration of each I/O port.

Each group (I and II) accepts "commands" from the Read/Write Control Logic and "control words" from the internal data bus and in turn controls its associated I/O ports.

Group I – Port A and upper Port C (PC_7-PC_4)
Group II – Port B and lower Port C (PC_3-PC_0)

While the Control Word Register can be written into, the contents cannot be read back to the processor.

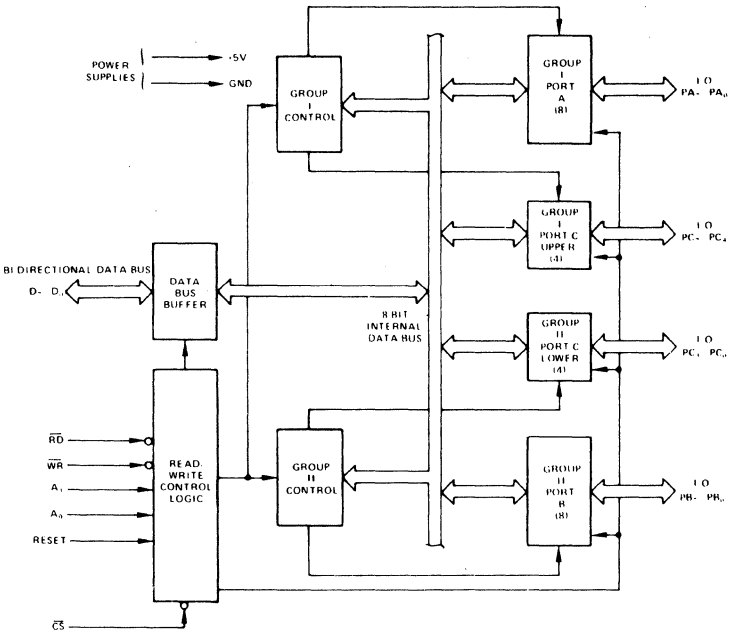
Ports A, B, and C

The three 8-bit I/O ports (A, B, and C) in the μPD8255 and μPD8255A-5 can all be configured to meet a wide variety of functional requirements through system software. The effectiveness and flexibility of the μPD8255 and μPD8255A-5 is further enhanced by special features unique to each of the ports.

Port A = An 8-bit data output latch/buffer and data input latch.
Port B = An 8-bit data input/output latch/buffer and an 8-bit data input buffer.
Port C = An 8-bit output latch/buffer and a data input buffer (input not latched).

Port C may be divided into two independent 4-bit control and status ports for use with Ports A and B.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +125°C
All Output Voltages ①	-0.5 to +7 Volts
All Input Voltages ①	-0.5 to +7 Volts
Supply Voltages ①	-0.5 to +7 Volts

Note: ① With respect to V_{SS}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C, V_{CC} = +5V ± 5%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS μPD8255 MIN	μPD8255 TYP	μPD8255 MAX	μPD8255A-5 MIN	μPD8255A-5 TYP	μPD8255A-5 MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	V_{SS}-0.5		0.8	-0.5		0.8	V	
Input High Voltage	V_{IH}	2		V_{CC}	2		V_{CC}	V	
Output Low Voltage	V_{OL}			0.4			0.45	V	②
Output High Voltage	V_{OH}	2.4			2.4			V	③
Darlington Drive Current	I_{OH} ①	1	2	4	-1	-2	-4	mA	V_{OH} = 1.5V, R_{EXT} = 750Ω
Power Supply Current	I_{CC}		40	120		40	120	mA	V_{CC} = +5V, Output Open
Input Leakage Current	I_{LIH}			10			10	μA	V_{IN} = V_{CC}
Input Leakage Current	I_{LIL}			-10			-10	μA	V_{IN} = 0.4V
Output Leakage Current	I_{LOH}			10			10	μA	V_{OUT} = V_{CC}, $\overline{CS}$ = 2.0V
Output Leakage Current	I_{LOL}			-10			-10	μA	V_{OUT} = 0.4V, $\overline{CS}$ = 2.0V

Notes: ① Any set of eight (8) outputs from either Port A, B, or C can source 2 mA into 1.5V for μPD8255, or 4 mA into 1.5V for μPD8255A-5.
② For μPD8255 I_{OL} = 1.7 mA
For μPD8255A-5 I_{OL} = 2.5 mA for DB Port, 1.7 mA for Peripheral Ports.
③ For μPD8255 I_{OH} = -100 μs for DB Port, -50 μs for Peripheral Ports.
For μPD8255A-5 I_{OH} = -400 μs for DB Port, -200 μs for Peripheral Ports.

CAPACITANCE

T_a = 25°C; V_{CC} = V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	f_c = 1 MHz
I/O Capacitance	$C_{I/O}$			20	pF	Unmeasured pins returned to V_{SS}

μPD8255/8255A-5

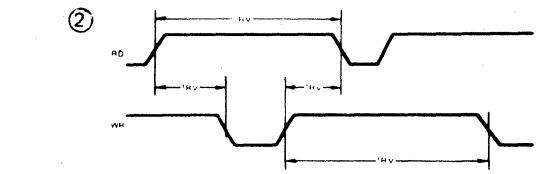
AC CHARACTERISTICS

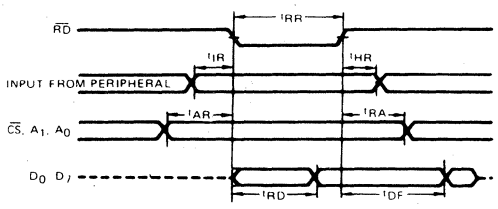
T_a = 0°C to +70°C; V_{CC} = +5V ± 5%; V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS μPD8255 MIN	LIMITS μPD8255 MAX	LIMITS μPD8255A-5 MIN	LIMITS μPD8255A-5 MAX	UNIT	TEST CONDITIONS
READ							
Address Stable Before $\overline{READ}$	t_{AR}	50		0		ns	
Address Stable After $\overline{READ}$	t_{RA}	0		0		ns	
$\overline{READ}$ Pulse Width	t_{RR}	405		300		ns	
Data Valid From $\overline{READ}$	t_{RD}		295		200	ns	8255: C_L = 100 pF 8255A-5: C_L = 150 pF
Data Float After $\overline{READ}$	t_{DF}	10	150	10	100	ns ns	C_L = 100 pF C_L = 15 pF
Time Between $\overline{READS}$ and/or $\overline{WRITES}$	t_{RV}	850		850		ns	②
WRITE							
Address Stable Before $\overline{WRITE}$	t_{AW}	20		0		ns	
Address Stable After $\overline{WRITE}$	t_{WA}	20		20		ns	
$\overline{WRITE}$ Pulse Width	t_{WW}	400		300		ns	
Data Valid To $\overline{WRITE}$ (L.E.)	t_{DW}	10		100		ns	
Data Valid After $\overline{WRITE}$	t_{WD}	35		30		ns	
OTHER TIMING							
$\overline{WR}$ = 0 To Output	t_{WB}		500		350	ns	8255: C_L = 50 pF 8255A-5: C_L = 150 pF
Peripheral Data Before $\overline{RD}$	t_{IR}	0		0		ns	
Peripheral Data After $\overline{RD}$	t_{HR}	50		0		ns	
$\overline{ACK}$ Pulse Width	t_{AK}	500		300		ns	
$\overline{STB}$ Pulse Width	t_{ST}	350		500		ns	
Per. Data Before T.E. Of $\overline{STB}$	t_{PS}	60		0		ns	
Per. Data After T.E. Of $\overline{STB}$	t_{PH}	150		180		ns	
$\overline{ACK}$ = 0 To Output	t_{AD}		400		300	ns	8255: C_L = 50 pF 8255A-5: C_L = 150 pF
$\overline{ACK}$ = 0 To Output Float	t_{KD}	20	300	20	250	ns	8255 { C_L = 50 pF C_L = 15 pF
$\overline{WR}$ = 1 To $\overline{OBF}$ = 0	t_{WOB}		300		650	ns	
$\overline{ACK}$ = 0 To $\overline{OBF}$ = 1	t_{AOB}		450		350	ns	
$\overline{STB}$ = 0 To IBF = 1	t_{SIB}		450		300	ns	8255: C_L = 50 pF
$\overline{RD}$ = 1 To IBF = 0	t_{RIB}		360		300	ns	
$\overline{RD}$ = 0 To INTR = 0	t_{RIT}		450		400	ns	
$\overline{STB}$ = 1 To INTR = 1	t_{SIT}		400		300	ns	8255A-5: C_L = 150 pF
$\overline{ACK}$ = 1 To INTR = 1	t_{AIT}		400		350	ns	
$\overline{WR}$ = 0 To INTR = 0	t_{WIT}		850		850	ns	

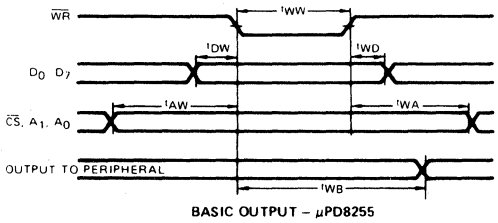
Notes: ① Period of Reset pulse must be at least 50 μs during or after power on. Subsequent Reset pulse can be 500 ns min.

TIMING WAVEFORMS
MODE 0

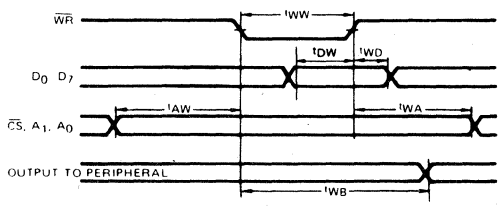




BASIC INPUT



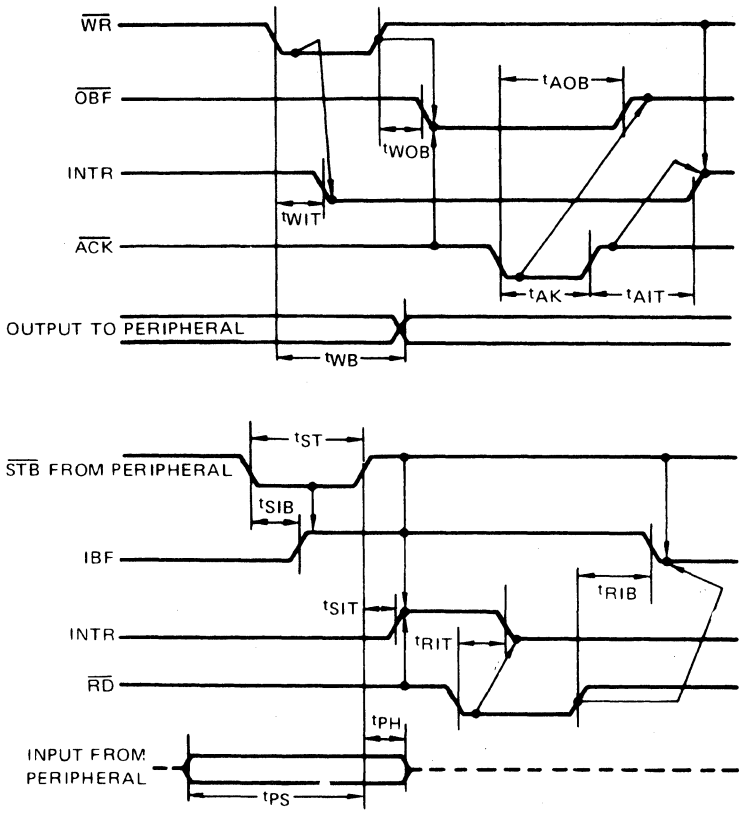
BASIC OUTPUT – μPD8255



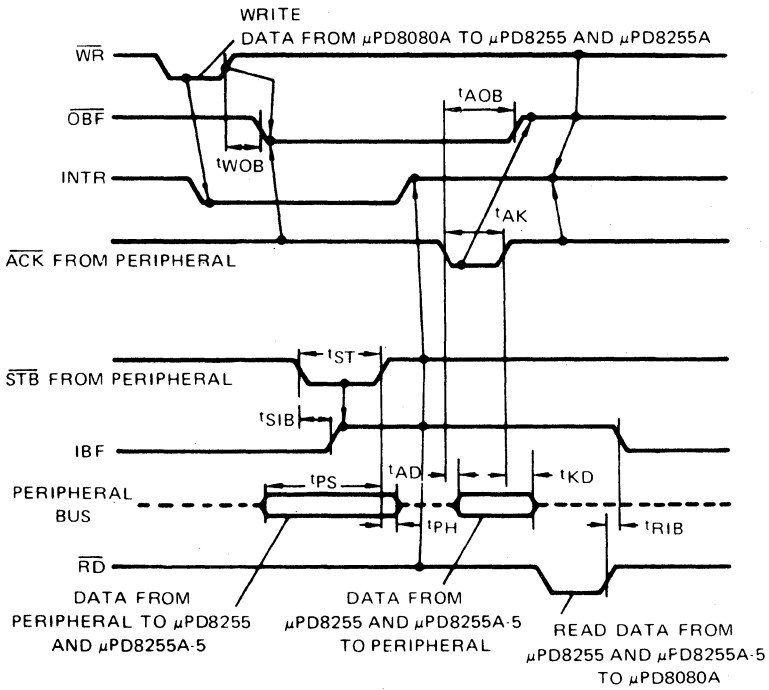
BASIC OUTPUT – μPD8255A-5

TIMING WAVEFORMS (CONT.)

MODE 1



MODE 2



Note: ① Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
(INTR = IBF · $\overline{MASK}$ · $\overline{STB}$ · $\overline{RD}$ + $\overline{OBF}$ · $\overline{MASK}$ · $\overline{ACK}$ · $\overline{WR}$)

② When the μPD8255A-5 is set to Mode 1 or 2, $\overline{OBF}$ is reset to be high (logic 1).

μPD8255/8255A-5

MODES

The μPD8255 and μPD8255A-5 can be operated in modes (0, 1 or 2) which are selected by appropriate control words and are detailed below.

MODE 0

- MODE 0 provides for basic Input and Output operations through each of the ports A, B, and C. Output data is latched and input data follows the peripheral. No "handshaking" strobes are needed.

  16 different configurations in MODE 0

  Two 8-bit ports and two 4-bit ports

  Inputs are not latched

  Outputs are latched

MODE 1

MODE 1 provides for Strobed Input and Output operations with data transferred through Port A or B and handshaking through Port C.

Two I/O Groups (I and II)

Both groups contain an 8-bit data port and a 4-bit control/data port

Both 8-bit data ports can be either Latched Input or Latched Output

MODE 2

MODE 2 provides for Strobed bidirectional operation using PA_{0-7} as the bidirectional latched data bus. PC_{3-7} is used for interrupts and "handshaking" bus flow controls similar to Mode 1. Note that PB_{0-7} and PC_{0-2} may be defined as Mode 0 or 1, input or output in conjunction with Port A in Mode 2.

An 8-bit latched bidirectional bus port (PA_{0-7}) and a 5-bit control port (PC_{3-7})

Both inputs and outputs are latched

An additional 8-bit input or output port with a 3-bit control port

BASIC OPERATION

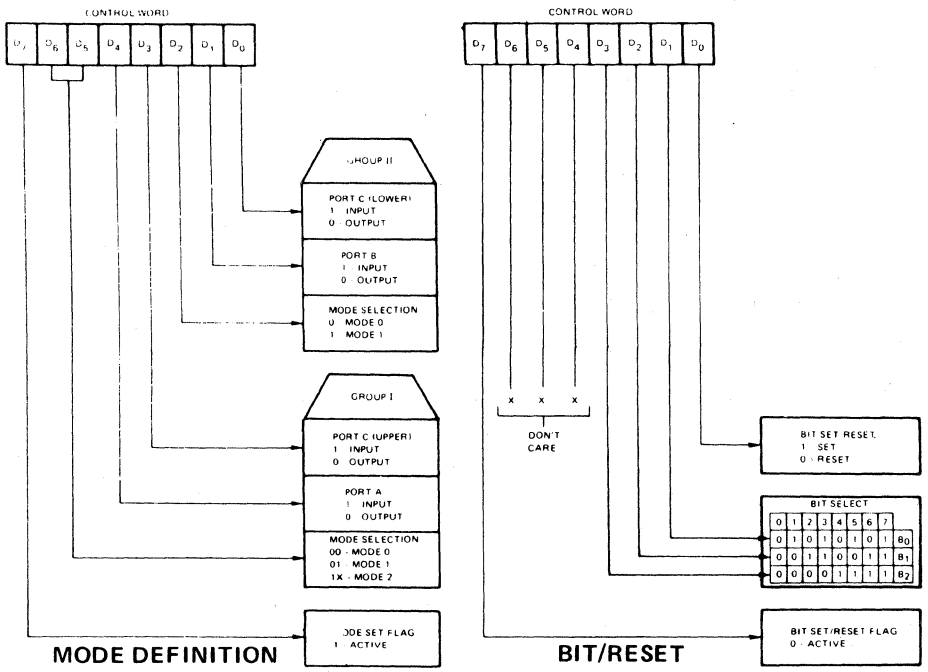
INPUT OPERATION (READ)					
A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	0	1	0	PORT A → DATA BUS
0	1	0	1	0	PORT B → DATA BUS
1	0	0	1	0	PORT C → DATA BUS

OUTPUT OPERATION (WRITE)					
A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	0	DATA BUS → PORT A
0	1	1	0	0	DATA BUS → PORT B
1	0	1	0	0	DATA BUS → PORT C
1	1	1	0	0	DATA BUS → CONTROL

DISABLE FUNCTION					
A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
X	X	X	X	1	DATA BUS → HIGH Z STATE
X	X	1	1	0	DATA BUS → HIGH Z STATE

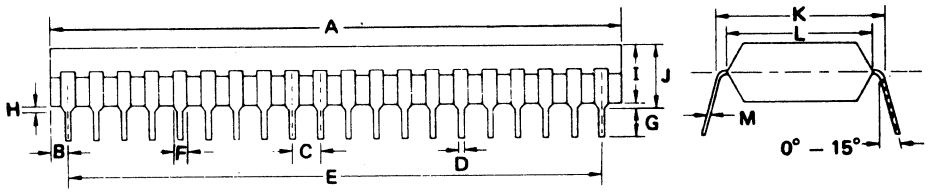
NOTES: ① X means "DO NOT CARE."
② All conditions not listed are illegal and should be avoided.

FORMATS



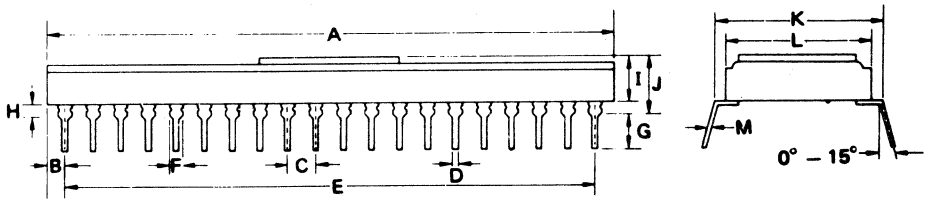
PACKAGE OUTLINE
μPD8255C/D
μPD8255AC/D-5

Members of the μPD8085 Family are housed in both plastic and ceramic 40 pin packages. The drawings and tables below apply to all five of the NEC Microcomputer parts covered in this data sheet.



Plastic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{0.05}$	$0.010^{+0.004}_{0.002}$



Ceramic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.100 ± 0.004
D	0.50 ± 0.1	0.0197 ± 0.004
E	48.26 ± 0.2	1.900 ± 0.008
F	1.27	0.050
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.17 MAX
J	5.2 MAX	0.205 MAX
K	15.24 ± 0.1	0.6 ± 0.004
L	$13.5^{+0.2}_{-0.25}$	$0.531^{+0.008}_{-0.010}$
M	0.30 ± 0.1	0.012 ± 0.004

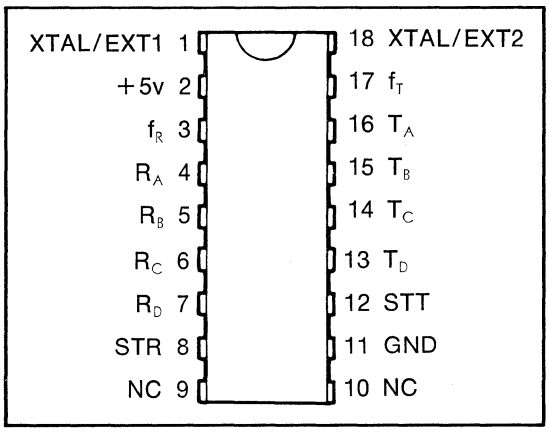
COM 8116
COM 8116T

Dual Baud Rate Generator
Programmable Divider

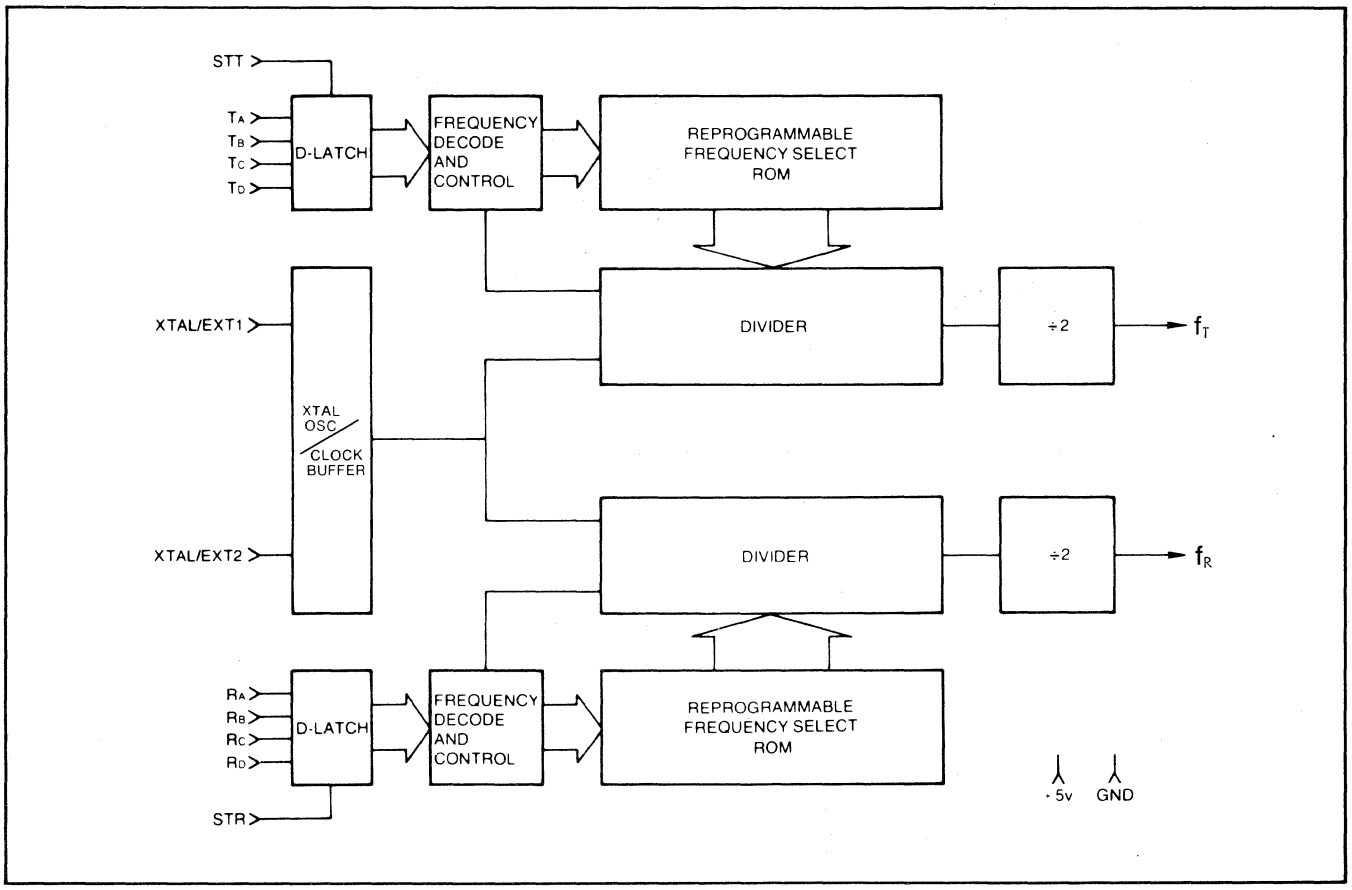
FEATURES

- ☐ On chip crystal oscillator or external frequency input
- ☐ Single +5v power supply
- ☐ Choice of 2 x 16 output frequencies
- ☐ 16 asynchronous/synchronous baud rates
- ☐ Direct UART/USRT/ASTRO/USYNRT compatibility
- ☐ Full duplex communication capability
- ☐ Re-programmable ROM via CLASP™ technology allows generation of other frequencies
- ☐ TTL, MOS compatibility
- ☐ Compatible with COM 5016

PIN CONFIGURATION



BLOCK DIAGRAM



General Description

The Standard Microsystem's COM 8116 is an enhanced version of the COM 5016 Dual Baud Rate Generator. It is fabricated using SMC's patented COPLAMOS® and CLASP™ technologies and employs depletion mode loads, allowing operation from a single +5v supply.

The standard COM 8116 is specifically dedicated to generating the full spectrum of 16 asynchronous/synchronous data communication frequencies for 16X UART/USRT devices. A large number of the frequencies available are also useful for 1X and 32X ASTRO/USYNRT devices.

The COM 8116 features an internal crystal oscillator which may be used to provide the master reference frequency. Alternatively, an external reference may be supplied by applying complementary TTL level signals to pins 1 and 18. Parts suitable for use only with an external TTL reference are marked COM 8116T. TTL outputs used to drive the COM 8116 or COM 8116T XTAL/EXT inputs should not be used to drive other TTL inputs, as noise immunity may be compromised due to excessive loading.

The output of the oscillator/buffer is applied to the dividers for generation of the output frequencies f_T, f_R. The dividers are capable of dividing by any integer from 6 to $2^{19} + 1$, inclusive. If the divisor is even, the output will be square; otherwise the output will be high longer than it is low by one fx clock period.

Each of the two divisor ROMs contains 16 divisors, each 19 bits wide, and is fabricated using SMC's unique CLASP™ technology allowing up to 32 different divisors on custom parts. This process permits reduction of turn-around time for ROM patterns. Each group of four divisor select bits is held in an externally strobed data latch. The strobe input is level sensitive: while the strobe is high, data is passed directly through to the ROM. Initiation of a new frequency is effected within 3.5μs of a change in any of the four divisor select bits (strobe activity is not required). The divisor select inputs have pull-up resistors; the strobe inputs do not.

Description of Pin Functions

Pin No.	Symbol	Name	Function
1	XTAL/EXT1	Crystal or External Input 1	This input is either one pin of the crystal package or one polarity of the external input.
2	V_{CC}	Power Supply	+5 volt supply
3	f_R	Receiver Output Frequency	This output runs at a frequency selected by the Receiver divisor select data bits.
4-7	R_A, R_B, R_C, R_D	Receiver-Divisor Select Data Bits	The logic level on these inputs, as shown in Table 1, selects the receiver output frequency, f_R.
8	STR	Strobe-Receiver	A high level input strobe loads the receiver data (R_A, R_B, R_C, R_D) into the receiver divisor select register. This input may be strobed or hard-wired to a high level.
9	NC	No Connection	
10	NC	No Connection	
11	GND	Ground	Ground
12	STT	Strobe-Transmitter	A high level input strobe loads the transmitter data (T_A, T_B, T_C, T_D) into the transmitter divisor select register. This input may be strobed or hard-wired to a high level.
13-16	T_D, T_C, T_B, T_A	Transmitter-Divisor Select Data Bits	The logic level on these inputs, as shown in Table 1, selects the transmitter output frequency, f_T.
17	f_T	Transmitter Output Frequency	This output runs at a frequency selected by the Transmitter divisor select data bits.
18	XTAL/EXT2	Crystal or External Input 2	This input is either the other pin of the crystal package or the other polarity of the external input.

COM 8116T-020

Reference Frequency = 1.8432 MHz

Divisor Select DCBA	Desired Baud Rate	Clock Factor	Desired Frequency (KHz)	Divisor	Actual Baud Rate	Actual Frequency (KHz)	Deviation
0000	50.0	16X	0.800	2,304	50.00	0.800	0.0%
0001	75.0	16X	1.200	1,807	75.00	1.200	0.0%
0010	110.0	16X	1.760	1,047	110.00	1.761	0.0%
0011	134.5	16X	2.152	856	134.52	2.151	0.0%
0100	150.0	16X	2.400	768	150.00	2.400	0.0%
0101	200.0	16X	3.200	576	200.00	3.200	0.0%
0110	300.0	16X	4.800	384	300.00	4.800	0.0%
0111	600.0	16X	9.600	192	600.00	9.600	0.0%
1000	1,200.0	16X	19.200	96	1,200.00	19.200	0.0%
1001	1,800.0	16X	28.000	64	1,800.00	28.801	0.0%
1010	2,000.0	16X	32.200	57	1,986.00	31.780	1.3%
1011	2,400.0	16X	38.400	48	2,400.00	38.402	0.0%
1100	3,600.0	16X	57.600	32	3,600.00	57.602	0.0%
1101	4,800.0	16X	76.800	24	4,800.00	76.803	0.0%
1110	9,600.0	16X	153.600	12	9,600.00	153.607	0.0%
1111	19,200.0	16X	307.200	6	19,200.00	307.213	0.0%

Standard Microsystems Corporation
35 Marcus Boulevard
Hauppauge, New York 11787
(516) 273-3100
TWX: 510-227-8898

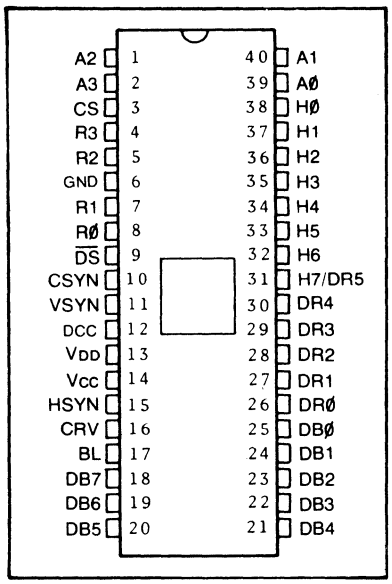
CRT 5027
CRT 5037
μPC FAMILY

CRT Video Timer-Controller VTAC®

FEATURES

- ☐ Fully Programmable Display Format
  - Characters per data row (1-200)
  - Data rows per frame (1-64)
  - Raster scans per data row (1-16)
- ☐ Programmable Monitor Sync Format
  - Raster Scans/Frame (256-1023)
  - "Front Porch"
  - Sync Width
  - "Back Porch"
  - Interlace/Non-Interlace
  - Vertical Blanking
- ☐ Direct Outputs to CRT Monitor
  - Horizontal Sync
  - Vertical Sync
  - Composite Sync
  - Blanking
  - Cursor coincidence
- ☐ Programmed via:
  - Processor data bus
  - External PROM
  - Mask Option ROM
- ☐ Standard or Non-Standard CRT Monitor Compatible
- ☐ Refresh Rate: 60Hz, 50Hz,...
- ☐ Scrolling
  - Single Line
  - Multi-Line
- ☐ Cursor Position Registers
- ☐ Character Format: 5x7, 7x9,...
- ☐ Programmable Vertical Data Positioning
- ☐ Balanced Beam Current Interlace (CRT 5037)

PIN CONFIGURATION



- ☐ Split-Screen Applications
  - Horizontal
  - Vertical
- ☐ Graphics Compatible
- ☐ Interlace or Non-Interlace operation
- ☐ TTL Compatibility
- ☐ BUS Oriented
- ☐ High Speed Operation
- ☐ COPLAMOS® N-Channel Silicon Gate Technology
- ☐ Compatible with CRT 8002 VDAC™
- ☐ Compatible with CRT 7004

General Description

The CRT Video Timer-Controller Chip (VTAC)® is a user programmable 40-pin COPLAMOS® n channel MOS/LSI device containing the logic functions required to generate all the timing signals for the presentation and formatting of interlaced and non-interlaced video data on a standard or non-standard CRT monitor.

With the exception of the dot counter, which may be clocked at a video frequency above 25 MHz and therefore not recommended for MOS implementation, all frame formatting, such as horizontal, vertical, and composite sync, characters per data row, data rows per frame, and raster scans per data row and per frame are totally user programmable. The data row counter has been designed to facilitate scrolling.

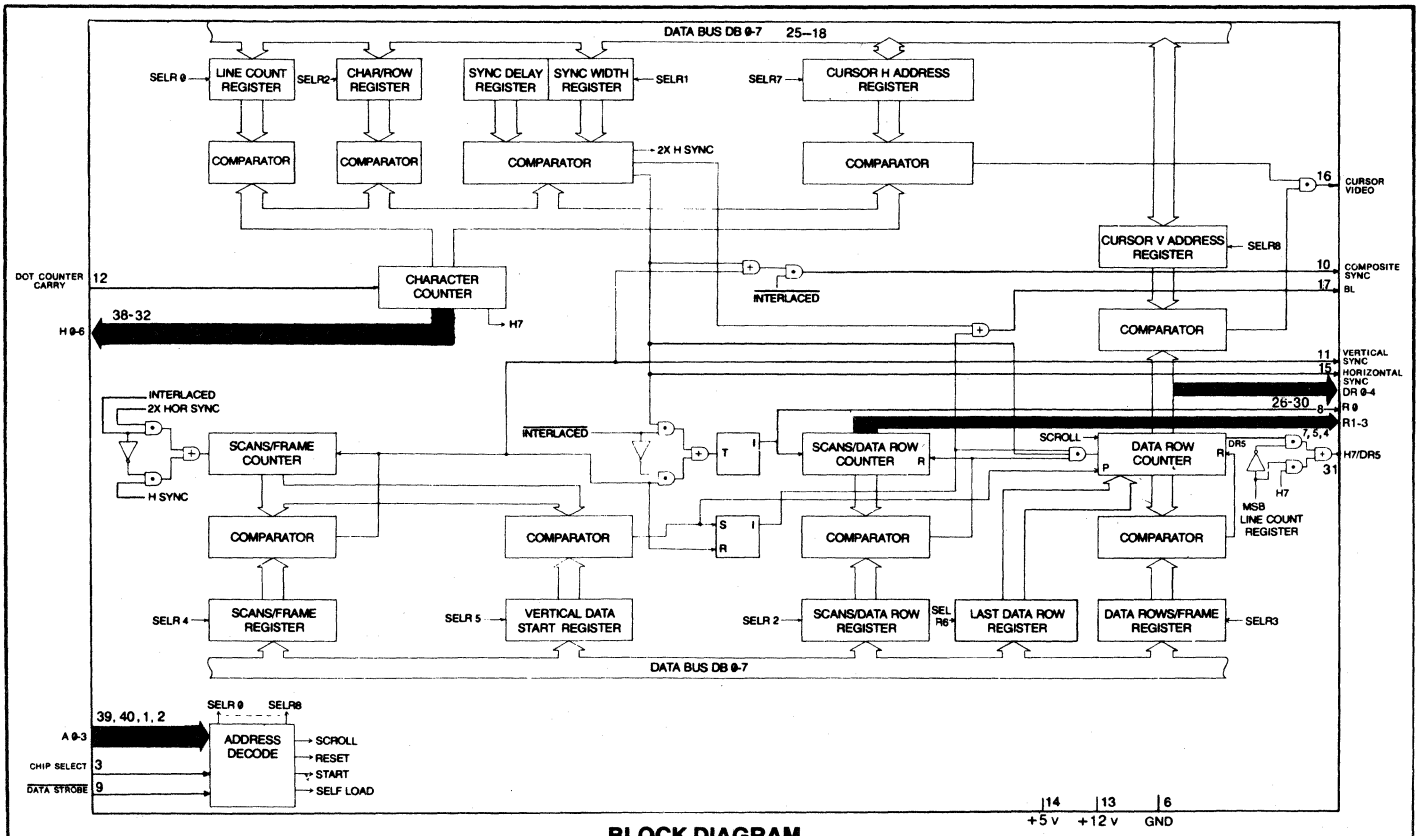
Programming is effected by loading seven 8 bit control registers directly off an 8 bit bidirectional data bus. Four register address lines and a chip select line provide complete microprocessor compatibility for program controlled set up. The device can be "self loaded" via an external PROM tied on the data bus as described in the OPERATION section. Formatting can also be programmed by a single mask option.

In addition to the seven control registers two additional registers are provided to store the cursor character and data row addresses for generation of the cursor video signal. The contents of these two registers can also be read out onto the bus for update by the program.

Two versions of the VTAC® are available. The CRT 5027 provides non-interlaced operation with an even or odd number of scan lines per data row, or interlaced operation with an even number of scan lines per data row. The CRT 5037 may be programmed for an odd or even number of scan lines per data row in both interlaced and non-interlaced modes. Programming the CRT 5037 for an odd number of scan lines per data row eliminates character distortion caused by the uneven beam current normally associated with odd field/even field interlacing of alphanumeric displays.

Description of Pin Functions

Pin No.	Symbol	Name	Input/ Output	Function
25-18	DBØ–7	Data Bus	I/O	Data bus. Input bus for control words from microprocessor or PROM. Bidirectional bus for cursor address.
3	CS	Chip Select	I	Signals chip that it is being addressed
39, 40, 1, 2	AØ-3	Register Address	I	Register address bits for selecting one of seven control registers or either of the cursor address registers
9	$\overline{DS}$	Data Strobe	I	Strobes DBØ-7 into the appropriate register or outputs the cursor character address or cursor line address onto the data bus
12	DCC	DOT Counter Carry	I	Carry from off chip dot counter establishing basic character clock rate. Character clock.
38-32	HØ-6	Character Counter Outputs	O	Character counter outputs.
7, 5, 4	R1-3	Scan Counter Outputs	O	Three most significant bits of the Scan Counter; row select inputs to character generator.
31	H7/DR5	H7/DR5	O	Pin definition is user programmable. Output is MSB of Character Counter if horizontal line count (REG.Ø) is ≥128; otherwise output is MSB of Data Row Counter.
8	RØ	Scan Counter LSB	O	Least significant bit of the scan counter. In the interlaced mode with an even number of scans per data row, RØ will toggle at the field rate; for an odd number of scans per data row in the interlaced mode, RØ will toggle at the data row rate.
26-30	DRØ-4	Data Row Counter Outputs	O	Data Row counter outputs.
17	BL	Blank	O	Defines non active portion of horizontal and vertical scans.
15	HSYN	Horizontal Sync	O	Initiates horizontal retrace.
11	VSYN	Vertical Sync	O	Initiates vertical retrace.
10	CSYN	Composite Sync	O	Active in non-interlaced mode only. Provides a true RS-170 composite sync waveform.
16	CRV	Cursor Video	O	Defines cursor location in data field.
14	V_{CC}	Power Supply	PS	+5 volt Power Supply
13	V_{DD}	Power Supply	PS	+12 volt Power Supply



BLOCK DIAGRAM

Operation

The design philosophy employed was to allow the device to interface effectively with either a microprocessor based or hardwire logic system. The device is programmed by the user in one of two ways; via the processor data bus as part of the system initialization routine, or during power up via a PROM tied on the data bus and addressed directly by the Row Select outputs of the chip. (See figure 4). Seven 8 bit words are required to fully program the chip. Bit assignments for these words are shown in Table 1. The information contained in these seven words consists of the following:

Horizontal Formatting:

Characters/Data Row	A 3 bit code providing 8 mask programmable character lengths from 20 to 132. The standard device will be masked for the following character lengths; 20, 32, 40, 64, 72, 80, 96, and 132.
Horizontal Sync Delay	3 bits assigned providing up to 8 character times for generation of "front porch".
Horizontal Sync Width	4 bits assigned providing up to 16 character times for generation of horizontal sync width.
Horizontal Line Count	8 bits assigned providing up to 256 character times for total horizontal formatting.
Skew Bits	A 2 bit code providing from a 0 to 2 character skew (delay) between the horizontal address counter and the blank and sync (horizontal, vertical, composite) signals to allow for retiming of video data prior to generation of composite video signal. The Cursor Video signal is also skewed as a function of this code.

Vertical Formatting:

Interlaced/Non-interlaced	This bit provides for data presentation with odd/even field formatting for interlaced systems. It modifies the vertical timing counters as described below. A logic 1 establishes the interlace mode.
Scans/Frame	8 bits assigned, defined according to the following equations: Let X = value of 8 assigned bits. 1) in interlaced mode—scans/frame = 2X + 513. Therefore for 525 scans, program X = 6 (00000110). Vertical sync will occur precisely every 262.5 scans, thereby producing two interlaced fields. Range = 513 to 1023 scans/frame, odd counts only. 2) in non-interlaced mode—scans/frame = 2X + 256. Therefore for 262 scans, program X = 3 (00000011). Range = 256 to 766 scans/frame, even counts only. In either mode, vertical sync width is fixed at three horizontal scans (≡ 3H).
Vertical Data Start	8 bits defining the number of raster scans from the leading edge of vertical sync until the start of display data. At this raster scan the data row counter is set to the data row address at the top of the page.
Data Rows/Frame	6 bits assigned providing up to 64 data rows per frame.
Last Data Row	6 bits to allow up or down scrolling via a preload defining the count of the last displayed data row.
Scans/Data Row	4 bits assigned providing up to 16 scan lines per data row.

Additional Features

Device Initialization:

Under microprocessor control—The device can be reset under system or program control by presenting a 1Ø1Ø address on A3-Ø. The device will remain reset at the top of the even field page until a start command is executed by presenting a 111Ø address on A3-Ø.

Via "Self Loading"—In a non-processor environment, the self loading sequence is effected by presenting and holding the 1111 address on A3-Ø, and is initiated by the receipt of the strobe pulse ($\overline{DS}$). The 1111 address should be maintained long enough to insure that all seven registers have been loaded (in most applications under one millisecond). The timing sequence will begin one line scan after the 1111 address is removed. In processor based systems, self loading is initiated by presenting the Ø111 address to the device. Self loading is terminated by presenting the start command to the device which also initiates the timing chain.

Scrolling—In addition to the Register 6 storage of the last displayed data row a "scroll" command (address 1Ø11) presented to the device will increment the first displayed data row count to facilitate up scrolling in certain applications.

Control Registers Programming Chart

Horizontal Line Count:

Total Characters/Line = N+1, N=0 to 255 (DBØ=LSB)

Characters/Data Row:

DB2	DB1	DBØ		
0	0	0	= 20	Active Characters/Data Row
0	0	1	= 32	
0	1	0	= 40	
0	1	1	= 64	
1	0	0	= 72	
1	0	1	= 80	
1	1	0	= 96	
1	1	1	= 132	

Horizontal Sync Delay:

=N, from 1 to 7 character times (DBØ=LSB) (N=0 Disallowed)

Horizontal Sync Width:

=N, from 1 to 15 character times (DB3=LSB) (N=0 Disallowed)

Skew Bits

DB7	DB6	Sync/Blank Delay (Character Times)	Cursor Delay
0	0	0	0
1	0	1	0
0	1	2	1
1	1	2	2

Scans/Frame

8 bits assigned, defined according to the following equations: Let X = value of 8 assigned bits. (DBØ=LSB)

1) in interlaced mode—scans/frame = 2X + 513. Therefore for 525 scans, program X = 6 (00000110). Vertical sync will occur precisely every 262.5 scans, thereby producing two interlaced fields.
Range = 513 to 1023 scans/frame, odd counts only.

2) in non-interlaced mode—scans/frame = 2X + 256. Therefore for 262 scans, program X = 3 (00000011).
Range = 256 to 766 scans/frame, even counts only.

In either mode, vertical sync width is fixed at three horizontal scans (≡3H).

Vertical Data Start:

N= number of raster lines delay after leading edge of vertical sync of vertical start position. (DBØ=LSB)

Data Rows/Frame:

Number of data rows = N+1, N=0 to 63 (DBØ=LSB)

Last Data Row:

N= Address of last displayed data row, N=0 to 63, ie; for 24 data rows, program N=23. (DBØ=LSB)

Mode:

Register 1, DB7 = 1 establishes Interlace.

Scans/Data Row:

Interlace Mode

CRT 5027: Scans per Data Row = N + 1 where N = programmed number of data rows. N = 0 to 15. Scans per data row must be even counts only.

CRT 5037: Scans per data Row = N + 2. N = 0 to 14, odd or even counts.

Non-Interlace Mode

CRT 5027, CRT 5037: Scans per Data Row = N + 1 odd or even count. N = 0 to 15.

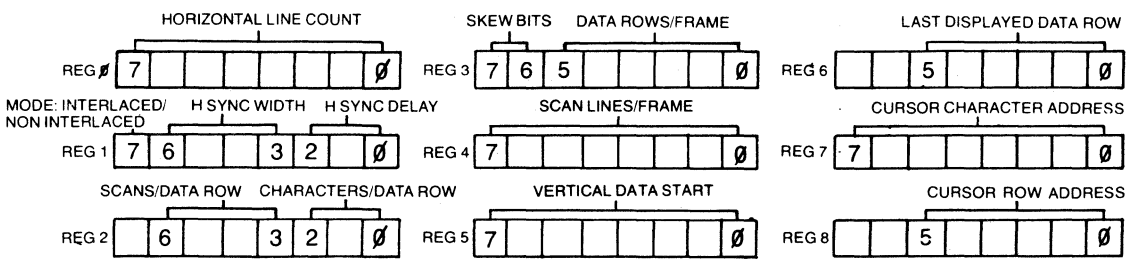
Register Selects/Command Codes

A3	A2	A1	AØ	Select/Command	Description
0	0	0	0	Load Control Register Ø	See Table 1
0	0	0	1	Load Control Register 1	
0	0	1	0	Load Control Register 2	
0	0	1	1	Load Control Register 3	
0	1	0	0	Load Control Register 4	
0	1	0	1	Load Control Register 5	
0	1	1	0	Load Control Register 6	
0	1	1	1	Processor Initiated Self Load	Command from processor instructing VTAC® to enter Self Load Mode (via external PROM)
1	0	0	0	Read Cursor Line Address	
1	0	0	1	Read Cursor Character Address	
1	0	1	0	Reset	Resets timing chain to top left of page. Reset is latched on chip by $\overline{DS}$ and counters are held until released by start command.
1	0	1	1	Up Scroll	Increments address of first displayed data row on page. ie; prior to receipt of scroll command—top line = 0, bottom line = 23. After receipt of Scroll Command—top line = 1, bottom line = 0.
1	1	0	0	Load Cursor Character Address*	
1	1	0	1	Load Cursor Line Address*	
1	1	1	0	Start Timing Chain	Receipt of this command after a Reset or Processor Self Load command will release the timing chain approximately one scan line later. In applications requiring synchronous operation of more than one CRT 5027 the dot counter carry should be held low during the $\overline{DS}$ for this command.
1	1	1	1	Non-Processor Self Load	Device will begin self load via PROM when $\overline{DS}$ goes low. The 1111 command should be maintained on A3-Ø long enough to guarantee self load. (Scan counter should cycle through at least once). Self load is automatically terminated and timing chain initiated when the all "1's" condition is removed, independent of $\overline{DS}$. For synchronous operation of more than one VTAC®, the Dot Counter Carry should be held low when the command is removed.

*NOTE: During Self-Load, the Cursor Character Address Register (REG 7) and the Cursor Row Address Register (REG 8) are enabled during states Ø111 and 1ØØØ of the R3-RØ Scan Counter outputs respectively. Therefore, Cursor data in the PROM should be stored at these addresses.

TABLE 1

BIT ASSIGNMENT CHART



AC TIMING DIAGRAMS

FIGURE 1 VIDEO TIMING

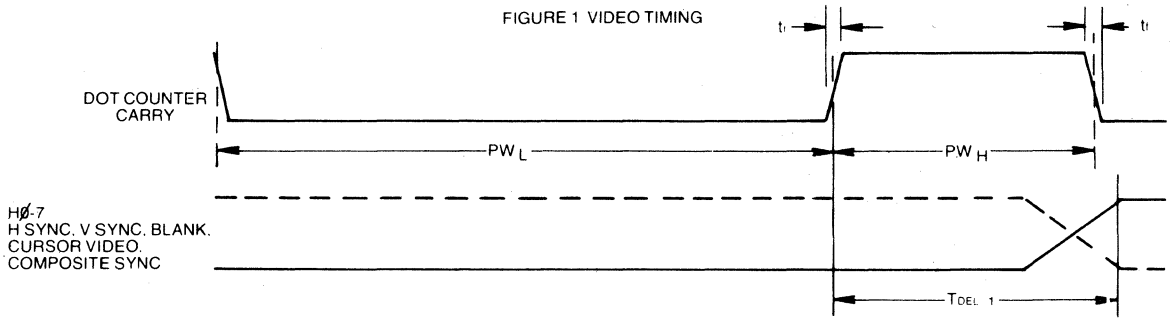


FIGURE 2 LOAD/READ TIMING

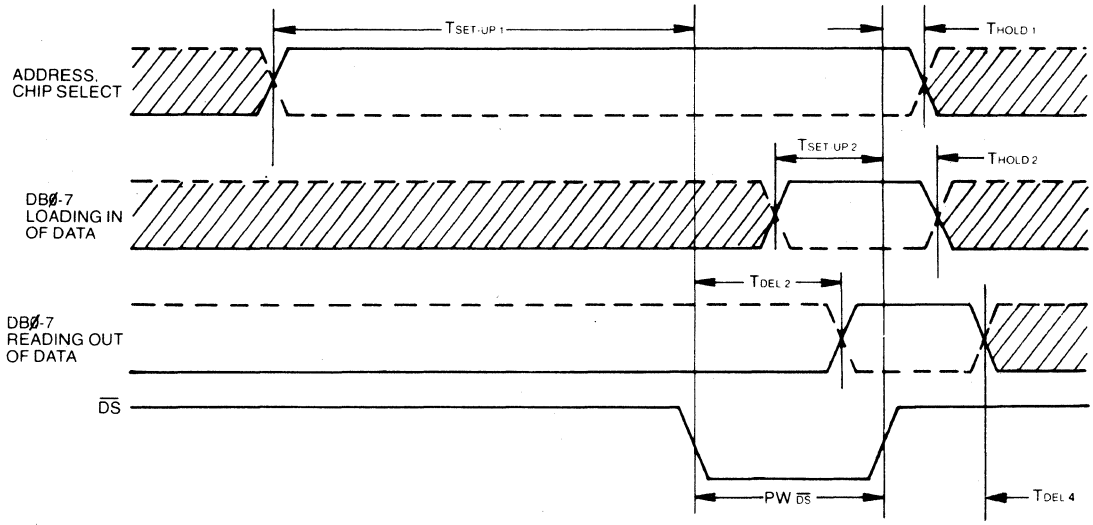
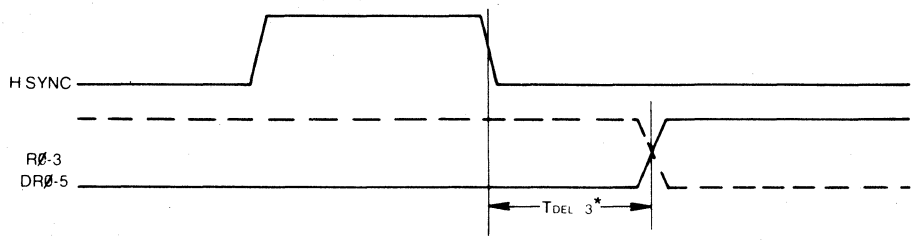
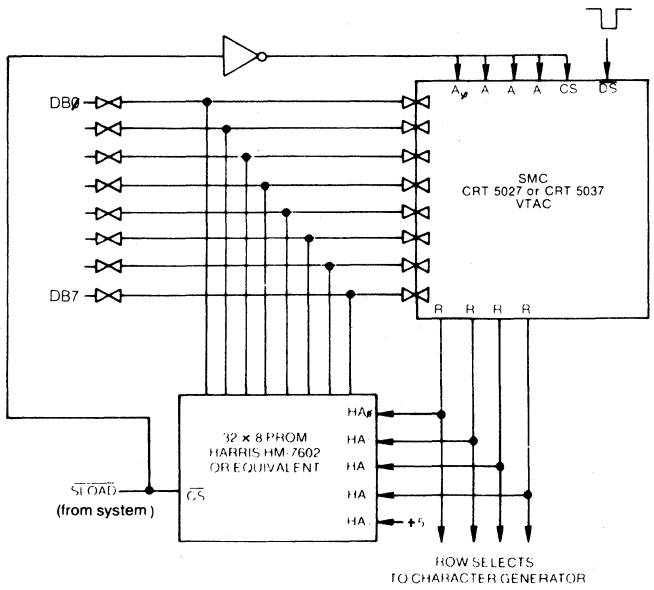


FIGURE 3 SCAN AND DATA ROW COUNTER TIMING



*RØ-3 and DRØ-5 may change prior to the falling edge of H sync

Figure 4. SELF LOADING SCHEME FOR VTAC SET-UP



MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +18.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. For example, the bench power supply programmed to deliver +12 volts may have large voltage transients when the AC power is switched on and off. If this possibility exists it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C, V_{CC}=+5V±5%, V_{DD}=+12V±5%, unless otherwise noted)

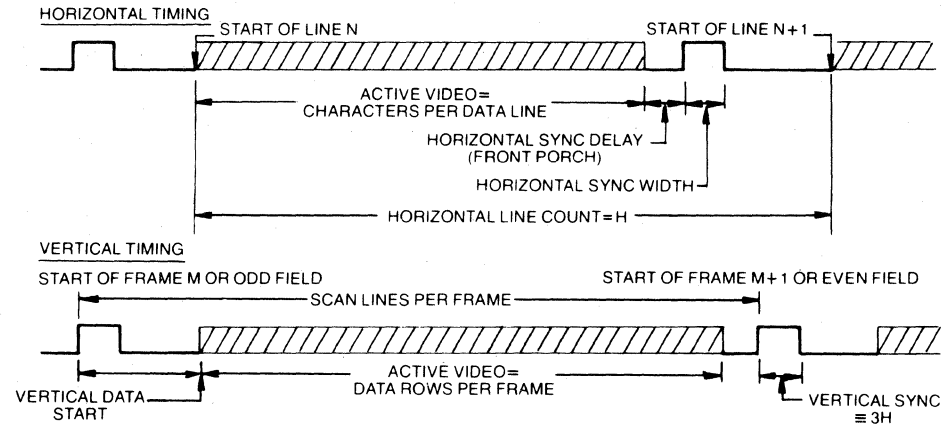
Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low Level, V_{IL}			0.8	V	
High Level, V_{IH}	V_{CC}−1.5		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low Level—V_{OL} for RØ-3			0.4	V	I_{OL}=3.2ma
Low Level—V_{OL} all others			0.4	V	I_{OL}=1.6ma
High Level—V_{OH} for RØ-3, DBØ-7	2.4				I_{OH}=80μa
High Level—V_{OH} all others	2.4				I_{OH}=40μa
INPUT CURRENT					
Low Level, I_{IL}			250	μA	V_{IN}=0.4V
High Level, I_{IH}			10	μA	V_{IN}=V_{CC}
INPUT CAPACITANCE					
Data Bus, C_{IN}		10	15	pF	
$\overline{DS}$, Clock, C_{IN}		25	40	pF	
All other, C_{IN}		10	15	pF	
DATA BUS LEAKAGE in INPUT MODE					
I_{DB}			10	μA	0.4V ≤ V_{IN} ≤ 5.25V
POWER SUPPLY CURRENT					
I_{CC}		80	100	mA	
I_{DD}		40	60	mA	
A.C. CHARACTERISTICS					T_A = 25°C
DOT COUNTER CARRY					
frequency	0.2		4.0	MHz	Figure 1
PW_H	35			ns	Figure 1
PW_L	215			ns	Figure 1
t_r, t_f		10	50	ns	Figure 1
DATA STROBE					
$PW_{\overline{DS}}$	150ns		10μs		Figure 2
ADDRESS, CHIP SELECT					
Set-up time	125			ns	Figure 2
Hold time	50			ns	Figure 2
DATA BUS—LOADING					
Set-up time	125			ns	Figure 2
Hold time	75			ns	Figure 2
DATA BUS—READING					
T_{DEL2}			125	ns	Figure 2, CL=50pF
T_{DEL4}	5		60	ns	Figure 2, CL=50pF
OUTPUTS: HØ-7, HS, VS, BL, CRV, CS-T_{DEL1}			125	ns	Figure 1, CL=20pF
OUTPUTS: RØ-3, DRØ-5					
T_{DEL3}	*		500	ns	Figure 3, CL=20pF

*RØ-3 and DRØ-5 may change prior to the falling edge of H sync

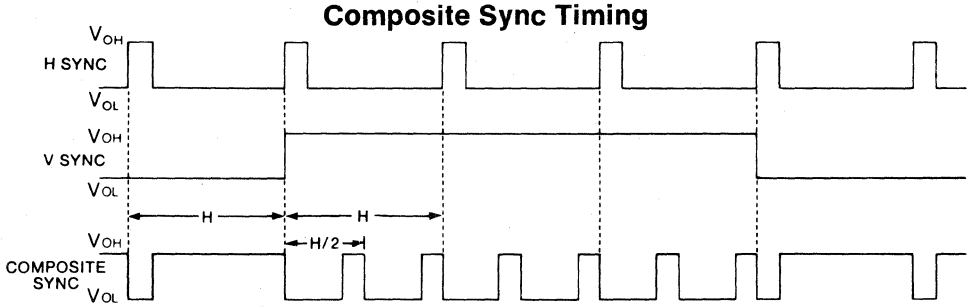
Restrictions

1. Only one pin is available for strobing data into the device via the data bus. The cursor X and Y coordinates are therefore loaded into the chip by presenting one set of addresses and outputed by presenting a different set of addresses. Therefore the standard WRITE and READ control signals from most microprocessors must be "NORed" externally to present a single strobe ($\overline{DS}$) signal to the device.
2. In interlaced mode the total number of character slots assigned to the horizontal scan must be even to insure that vertical sync occurs precisely between horizontal sync pulses.

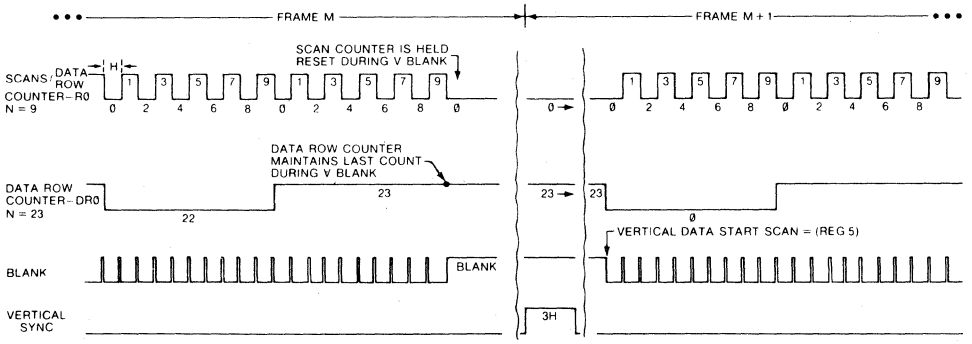
General Timing



Composite Sync Timing



Vertical Sync Timing



EXAMPLE BASED ON: Non-Interlaced (Reg 1, Bit 7 = 0), 24 data rows, 10 scans/data row

Start-up, CRT 5027

When employing microprocessor controlled loading of the CRT 5027's registers, the following sequence of instructions is necessary:

ADDRESS	COMMAND
1 1 1 0	Start Timing Chain
1 0 1 0	Reset
0 0 0 0	Load Register 0
•	•
•	•
•	•
0 1 1 0	Load Register 6
1 1 1 0	Start Timing Chain

The sequence of START RESET LOAD START is necessary to insure proper initialization of the registers.

This sequence is not required if register loading is via either of the Self Load modes. This sequence is optional with the CRT 5037.

Standard Microsystems Corporation
35 Marcus Blvd., Hauppauge, N.Y. 11787 Phone (516) 273-3100 TWX 510-227-8898

PRIORITY INTERRUPT CONTROLLER

DESCRIPTION

The μPB8214 is an eight-level priority interrupt controller. Designed to simplify interrupt driven microcomputer systems, the μPB8214 requires a single +5V power supply and is packaged in a 24 pin plastic Dual-in-line package.

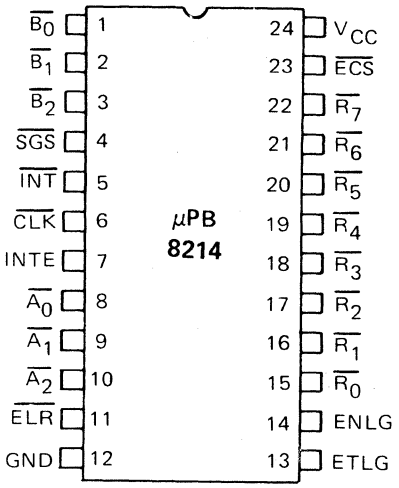
The μPB8214 accepts up to eight interrupts, determines which has the highest priority and then compares that priority with a software created current status register. If the incoming requires is of a higher priority than the interrupt currently being serviced, an interrupt request to the processor is generated. Vector information that identifies the interrupting device is also generated.

The interrupt structure of the microcomputer system can be expanded beyond eight interrupt levels by cascading μPB8214s. The μPB8214's interrupt and vector information outputs are open collector and control signals are provided to simplify expansion of the interrupt structure.

FEATURES

- Eight Priority Levels
- Current Status Register and Priority Comparator
- Easily Expanded Interrupt Structure
- Single +5 Volt Supply

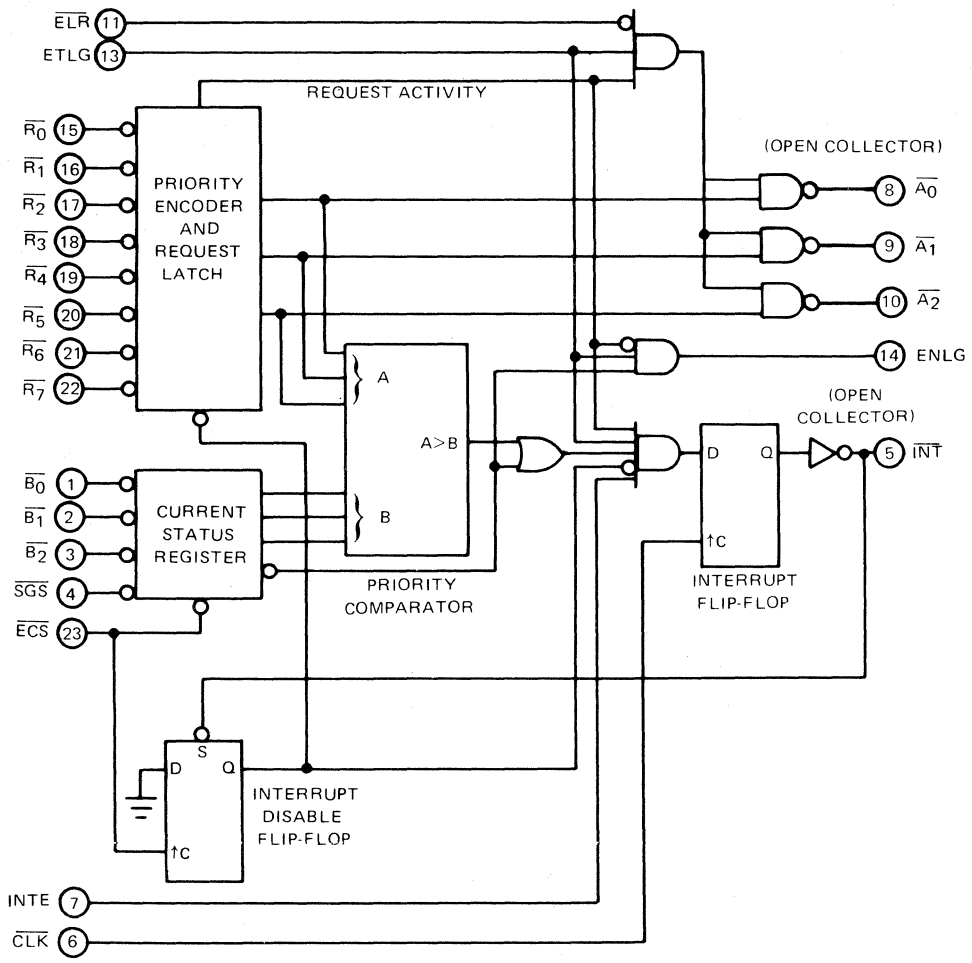
PIN CONFIGURATION



PIN NAMES

Inputs:		
$\overline{R_0}$ $\overline{R_7}$	Request Levels ($\overline{R_7}$ Highest Priority)	
$\overline{B_0}$ $\overline{B_2}$	Current Status	
$\overline{SGS}$	Status Group Select	
$\overline{ECS}$	Enable Current Status	
INTE	Interrupt Enable	
$\overline{CLK}$	Clock (INT F-F)	
$\overline{ELR}$	Enable Level Read	
ETLG	Enable This Level Group	
Outputs:		
$\overline{A_0}$ $\overline{A_2}$	Request Levels	Open
$\overline{INT}$	Interrupt (Act. Low)	Collector
ENLG	Enable Next Level Group	

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

General

The μPB8214 is an LSI device designed to simplify the circuitry required to implement an interrupt driven microcomputer system. Up to eight interrupting devices can be connected to a μPB8214, which will assign priority to incoming interrupt requests and accept the highest. It will also compare the priority of the highest incoming request with the priority of the interrupt being serviced. If the serviced interrupt has a higher priority, the incoming request will not be accepted.

A system with more than eight interrupting devices can be implemented by interconnecting additional μPB8214s. In order to facilitate this expansion, control signals are provided for cascading the controllers so that there is a priority established among the controllers. In addition, the interrupt and vector information outputs are open collector.

Priority Encoder and Request Latch

The priority encoder portion of the μPB8214 accepts up to eight active low interrupt requests ($\overline{R_0}$–$\overline{R_7}$). The circuit assigns priority to the incoming requests, with $\overline{R_7}$ having the highest priority and $\overline{R_0}$ the lowest. If two or more requests occur simultaneously, the μPB8214 accepts the one having the highest priority. Once an incoming interrupt request is accepted, it is stored by the request latch and a three-bit code is output. As shown in the following table, the outputs, ($\overline{A_0}$–$\overline{A_2}$) are the complement of the request level (modulo 8) and directly correspond to the bit pattern required to generate the one byte RESTART (RST) instructions recognized by an 8080A. Simultaneously with the $\overline{A_0}$–$\overline{A_2}$ outputs, a system interrupt request ($\overline{INT}$) is output by the μPB8214. It should be noted that incoming interrupt requests that are *not* accepted are not latched and must remain as an input to the μPB8214 in order to be serviced.

FUNCTIONAL DESCRIPTION (CONT.)

RESTART GENERATION TABLE

PRIORITY REQUEST		RST	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
			1	1	$\overline{A_2}$	$\overline{A_1}$	$\overline{A_0}$	1	1	1
LOWEST	$\overline{R_0}$	7	1	1	1	1	1	1	1	1
	$\overline{R_1}$	6	1	1	1	1	0	1	1	1
	$\overline{R_2}$	5	1	1	1	0	1	1	1	1
	$\overline{R_3}$	4	1	1	1	0	0	1	1	1
	$\overline{R_4}$	3	1	1	0	1	1	1	1	1
	$\overline{R_5}$	2	1	1	0	1	0	1	1	1
	$\overline{R_6}$	1	1	1	0	0	1	1	1	1
HIGHEST	$\overline{R_7}$	0*	1	1	0	0	0	1	1	1

*CAUTION: RST 0 will vector the program counter to location 0 (zero) and invoke the same routine as the "RESET" input to 8080A.

Current Status Register

The current status register is designed to prevent an incoming interrupt request from overriding the servicing of an interrupt with higher priority. Via software, the priority level of the interrupt being serviced by the microprocessor is written into the current status register on $\overline{B_0}$–$\overline{B_2}$. The bit pattern written should be the complement of the interrupt level.

The interrupt level currently being serviced is written into the current status register by driving $\overline{ECS}$ (Enable Current Status) low. The μPB8214 will only accept interrupts with a higher priority than the value contained by the current status register. Note that the programmer is free to use the current status register for other than as above. Other levels may be written into it. The comparison may be completely disabled by driving $\overline{SGS}$ (Status Group Select) low when $\overline{ECS}$ is driven low. This will cause the μPB8214 to accept incoming interrupts only on the basis of their priority to each other.

Priority Comparator

The priority comparator circuitry compares the level of the interrupt accepted by the priority encoder and request latch with the contents of the current status register. If the incoming request has a priority level higher than that of the current status register, the $\overline{INT}$ output is enabled. Note that this comparison can be disabled by loading the current status register with $\overline{SGS}$=0.

Expansion Control Signals

A microcomputer design may often require more than eight different interrupts. The μPB8214 is designed so that interrupt system expansion is easily performed via the use of three signals: ETLG (Enable This Level Group); ENLG (Enable Next Level Group); and $\overline{ELR}$ (Enable Level Read). A high input to ETLG indicates that the μPB8214 may accept an interrupt. In a typical system, the ENLG output from one μPB8214 is connected to the ETLG input of another μPB8214, etc. The ETLG of the μPB8214 with the highest priority is tied high. This configuration sets up priority among the cascaded μPB8214's. The ENLG output will be high for any device that does not have an interrupt pending, thereby allowing a device with lower priority to accept interrupts. The $\overline{ELR}$ input is basically a chip enable and allows hardware or software to selectively disable/enable individual μPB8214's. A low on the $\overline{ELR}$ input enables the device.

FUNCTIONAL DESCRIPTION (CONT.)

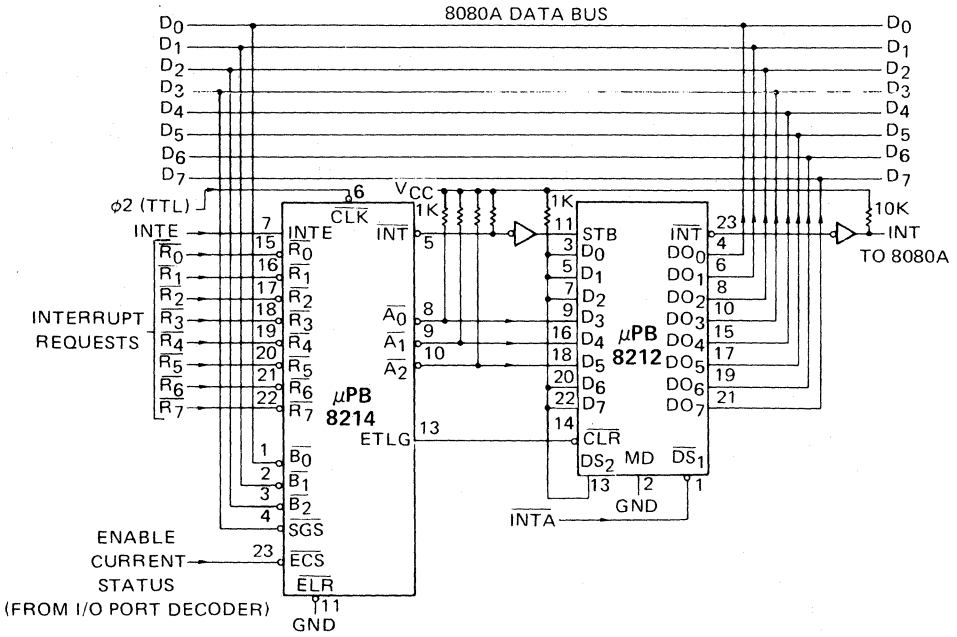
Interrupt Control Circuitry

The μPB8214 contains two flip-flops and several gates which determine whether an accepted interrupt request to the μPB8214 will generate a system interrupt to the 8080A. A condition gate drives the D input of the interrupt flip-flop whenever an interrupt request has been completely accepted. This requires that: the ETLG (Enable This Level Group) and INTE (Interrupt Enable) inputs to the μPB8214 are high; the $\overline{ELR}$ input is low; the incoming request must be of a higher priority than the contents of the current status register; and the μPB8214 must have been enabled to accept interrupt requests by the clearing of the interrupt disable flip-flop.

Once the condition gate drives the D input of the interrupt flip-flop high, a system interrupt ($\overline{INT}$) to the 8080A is generated on the next rising edge of the $\overline{CLK}$ input to the μPB8214. This $\overline{CLK}$ input is typically connected to the $\phi 2$ (TTL) output of an 8224 so that 8080A set-up time specifications are met. When $\overline{INT}$ is generated, it sets the interrupt disable flip-flop so that no additional system interrupts will be generated until it is reset. It is reset by driving $\overline{ECS}$ (Enable Current Status) low, thereby writing into the current status register.

It should be noted that the open collector $\overline{INT}$ output from the μPB8214 is active for only one clock period and thus must be externally latched for inputting to the 8080A. Also, because the $\overline{INT}$ output is open collector, when μPB8214's are cascaded, an $\overline{INT}$ output from any one will set all of the interrupt disable flip-flops in the array. Each μPB8214's interrupt disable flip-flop must then be cleared individually in order to generate subsequent system interrupts.

TYPICAL μPB8214 CIRCUITRY



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +125°C
All Output and Supply Voltages	−0.5 to +7 Volts
All Input Voltages	−1.0 to +5.5 Volts
Output Currents	100 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.①	LIMITS MAX.	UNIT	TEST CONDITIONS
Input Clamp Voltage (all inputs)	V_C			-1.0	V	I_C=-5mA
Input Forward Current: ETLG input	I_F		-.15	-0.5	mA	V_F=0.45V
all other inputs			-.08	-0.25	mA	
Input Reverse Current: ETLG input	I_R			80	μA	V_R=5.25V
all other inputs				40	μA	
Input LOW Voltage: all inputs	V_{IL}			0.8	V	V_{CC}=5.0V
Input HIGH Voltage: all inputs	V_{IH}	2.0			V	V_{CC}=5.0V
Power Supply Current	I_{CC}		90	130	mA	②
Output LOW Voltage: all outputs	V_{OL}		.3	.45	V	I_{OL}=10mA
Output HIGH Voltage: ENLG output	V_{OH}	2.4	3.0		V	I_{OH}=-1mA
Short Circuit Output Current: ENLG output	I_{OS}	-20	-35	-55	mA	V_{OS}=0V, V_{CC}=5.0V
Output Leakage Current: $\overline{INT}$ and $\overline{A_0}$–$\overline{A_2}$	I_{CEX}			100	μA	V_{CEX}=5.25V

CAPACITANCE ③

$T_a = 25°C$

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.①	LIMITS MAX.	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		5	10	pF	V_{BIAS}=2.5V
Output Capacitance	C_{OUT}		7	12	pF	V_{CC}=5V f=1mHz

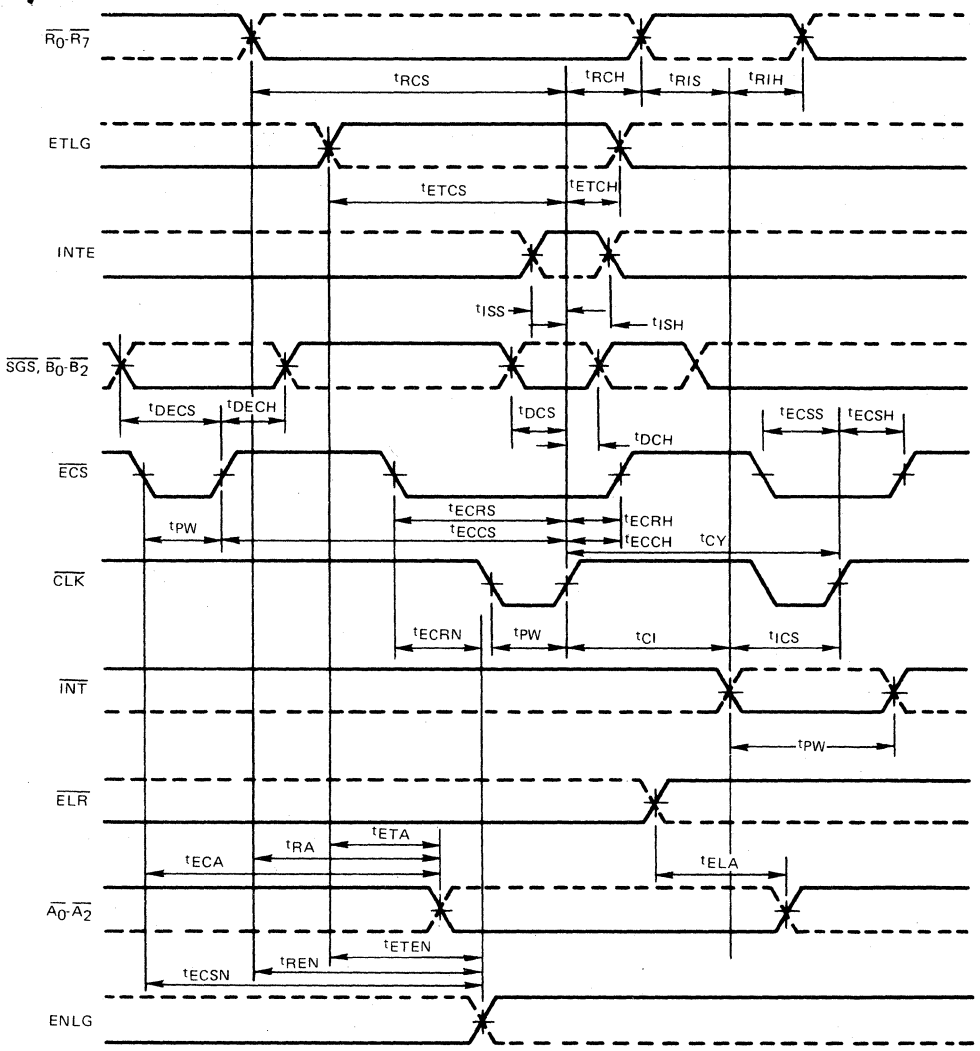
AC CHARACTERISTICS

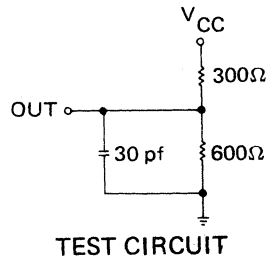
$T_a = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.①	LIMITS MAX.	UNIT	TEST CONDITIONS
$\overline{CLK}$ Cycle Time	t_{CY}	80	50		ns	Input pulse amplitude: 2.5 Volts
$\overline{CLK}$, $\overline{ECS}$, $\overline{INT}$ Pulse Width	t_{PW}	25	15		ns	
INTE Setup Time to $\overline{CLK}$	t_{ISS}	16	12		ns	
INTE Hold Time after $\overline{CLK}$	t_{ISH}	20	10		ns	
ETLG Setup Time to $\overline{CLK}$	t_{ETCS}④	25	12		ns	Input rise and fall times: 5 ns between 1 and 2 Volts
ETLG Hold Time After $\overline{CLK}$	t_{ETCH}④	20	10		ns	
$\overline{ECS}$ Setup Time to $\overline{CLK}$	t_{ECCS}④	80	50		ns	
$\overline{ECS}$ Hold Time After $\overline{CLK}$	t_{ECCH}⑤	0			ns	
$\overline{ECS}$ Setup Time to $\overline{CLK}$	t_{ECRS}⑤	110	70		ns	
$\overline{ECS}$ Hold Time After $\overline{CLK}$	t_{ECRH}⑤	0				Output loading of 15 mA and 30 pF
$\overline{ECS}$ Setup Time to $\overline{CLK}$	t_{ECSS}④	75	70		ns	
$\overline{ECS}$ Hold Time After $\overline{CLK}$	t_{ECSH}④	0			ns	
$\overline{SGS}$ and $\overline{B_0}$–$\overline{B_2}$ Setup Time to $\overline{CLK}$	t_{DCS}④	70	50		ns	
$\overline{SGS}$ and $\overline{B_0}$–$\overline{B_2}$ Hold Time After $\overline{CLK}$	t_{DCH}④	0			ns	Speed measurements taken at the 1.5 Volts levels.
$\overline{R_0}$–$\overline{R_7}$ Setup Time to $\overline{CLK}$	t_{RCS}⑤	90	55		ns	
$\overline{R_0}$–$\overline{R_7}$ Hold Time After $\overline{CLK}$	t_{RCH}⑤	0			ns	
$\overline{INT}$ Setup Time to $\overline{CLK}$	t_{ICS}	55	35		ns	
$\overline{CLK}$ to $\overline{INT}$ Propagation Delay	t_{CI}		15	25	ns	
$\overline{R_0}$–$\overline{R_7}$ Setup Time to $\overline{INT}$	t_{RIS}⑥	10	0		ns	
$\overline{R_0}$–$\overline{R_7}$ Hold Time After $\overline{INT}$	t_{RIH}⑥	35	20		ns	
$\overline{R_0}$–$\overline{R_7}$ to $\overline{A_0}$–$\overline{A_2}$ Propagation Delay	t_{RA}		80	100	ns	
$\overline{ELR}$ to $\overline{A_0}$–$\overline{A_2}$ Propagation Delay	t_{ELA}		40	55	ns	
$\overline{ECS}$ to $\overline{A_0}$–$\overline{A_2}$ Propagation Delay	t_{ECA}		100	120	ns	
ETLG to $\overline{A_0}$–$\overline{A_2}$ Propagation Delay	t_{ETA}		35	70	ns	
$\overline{SGS}$ and $\overline{B_0}$–$\overline{B_2}$ Setup Time to $\overline{ECS}$	t_{DECS}⑥	15	10		ns	
$\overline{SGS}$ and $\overline{B_0}$–$\overline{B_2}$ Hold Time After $\overline{ECS}$	t_{DECH}⑥	15	10		ns	
$\overline{R_0}$–$\overline{R_7}$ to ENLG Propagation Delay	t_{REN}		45	70	ns	
ELTG to ENLG Propagation Delay	t_{ETEN}		20	25	ns	
$\overline{ECS}$ to ENLG Propagation Delay	t_{ECRN}		85	90	ns	
$\overline{ECS}$ to ENLG Propagation Delay	t_{ECSN}		35	55	ns	

Notes:
① Typical values are for T_a=25°C, V_{CC}=5.0V
② $\overline{B_0}$–$\overline{B_2}$, $\overline{SGS}$, $\overline{CLK}$, $\overline{R_0}$–$\overline{R_4}$ grounded, all other inputs and all outputs open.
③ This parameter is periodically sampled and not 100% tested.
④ Required for proper operation if INTE is enabled during next clock pulse.
⑤ These times are not required for proper operation but for desired change in interrupt flip-flop.
⑥ Required for new request or status to be properly loaded.

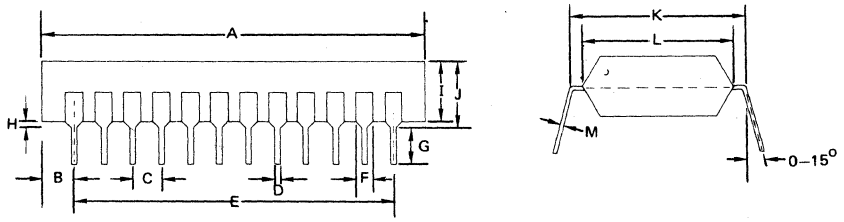
TIMING WAVEFORMS





TEST CIRCUIT

PACKAGE OUTLINE
μPB8214C



ITEM	MILLIMETERS	INCHES
A	33 MAX.	1.28
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	3.2 MIN.	0.125 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24	0.6
L	13.2	0.52
M	0.25 ± 0.1	0.01 ± 0.004

1400 Bit Serial Electrically Alterable Read Only Memory

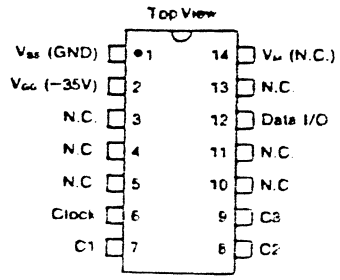
FEATURES

- 100 Word x 14 bit organization
- Addressing by two consecutive one-of-ten codes
- Single −35 Volt supply
- Word erasable
- 10 year data storage
- MOS compatible signal levels
- Word read time: 833μs
- Write/erase time: 16ms

PIN CONFIGURATIONS

Standard package

14 LEAD DUAL IN LINE



DESCRIPTION

The ER1400 is a serial input/output 1400 bit electrically erasable and reprogrammable ROM, organized as 100 words of 14 bits each. Data and address are communicated in serial form via a one-pin bidirectional bus.

Mode selection is by a 3 bit code applied to C1, C2 and C3.

Data is stored by internal negative writing pulses that selectively tunnel charge into the oxide-nitride interface of the gate insulator of the 1400 MNOS memory transistors. When the writing voltage is removed the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

PRIMARY SOURCES:

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs
(except V_{GG}) with respect to V_{SS} ..... −20V to +0.3V
V_{GG} with respect to V_{SS} ..... −40V
Storage temperature (No Data Retention) ..... −65°C to +150°C
Storage temperature (with Data Retention)
Operating ..... −25°C to +75°C
Unpowered ..... −65°C to +80°C

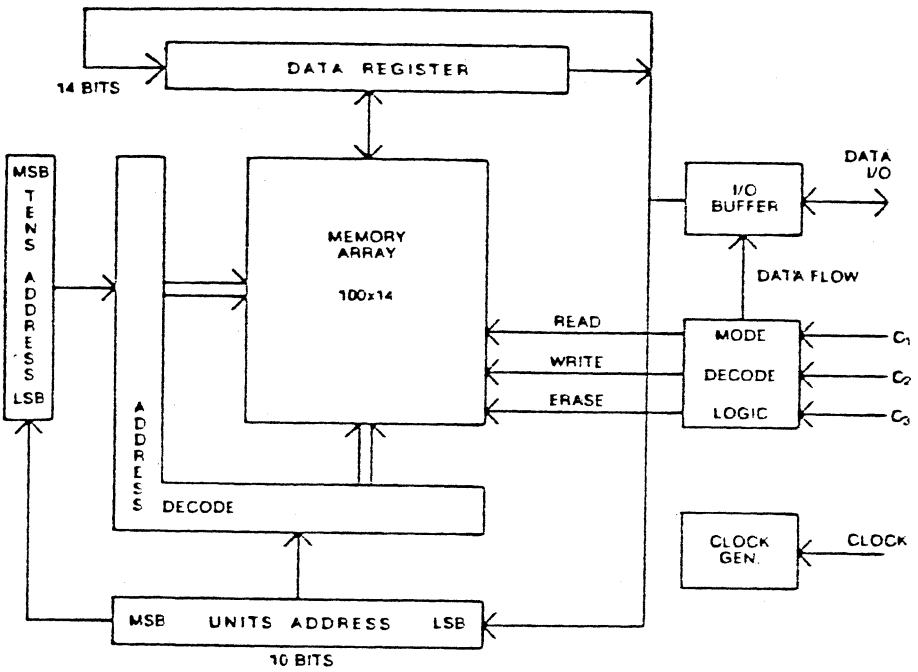
*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)
V_{SS} = GND
V_{GG} = −35V ± 8%
Operating Temperature (T_A) = 0°C to +70°C

Characteristics	Symbol	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Input logic "1"	V_{IL}	V_{SS}−15.0	—	V_{SS}−8.0	Volts	
Input logic "0"	V_{IH}	V_{SS}−1.0	—	V_{SS}+0.3	Volts	
Input leakage	I_L	—	—	10	μA	V_{IN} = −15V
Output logic "1"	V_{OL}	—	—	V_{SS}−12.0	Volts	Load = 1.5 Meg, 100pF
Output logic "0"	V_{OH}	V_{SS}−1.0	—	V_{SS}+0.3	Volts	I_{SOURCE} = 200μA
Power consumption	P_{GG}	—	—	300	mW	
Power supply current	I_{GG}	—	—	8.0	mA	
AC CHARACTERISTICS						
Clock Frequency	fϕ	11.2	14.0	16.8	kHz	
Clock duty cycle	Dϕ	45	50	55	%	
Write time	tw	16.0	20.0	24.0	ms	
Erase time	te	16.0	20.0	24.0	ms	
Rise, fall time	tr, tf	—	—	1.0	μs	
Control, Data set up time	t_{CS}	1	—	—	μs	
Control, Data hold time	t_{CH}	0	—	—	ns	
Propagation delay	tpw	—	—	20.0	μs	Load = 1 Meg, 100pF
Unpowered non-volatile data storage	T_S	10	—	—	Years	
Number of erase/write cycles	N_W	—	—	10^5	—	Per word
Number of read accesses between writes	N_{RA}	10^9	—	—	—	Per word

** Typical values are at +25°C and nominal voltages.

BLOCK DIAGRAM



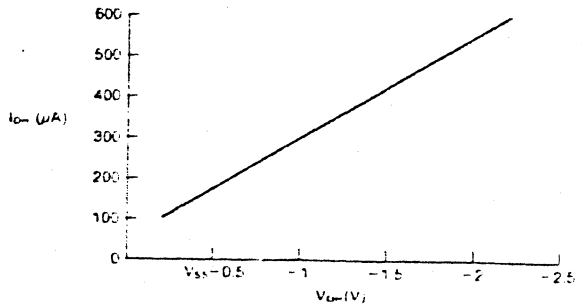


Fig.8 TYPICAL OUTPUT SOURCE CURRENT vs OUTPUT VOLTAGE

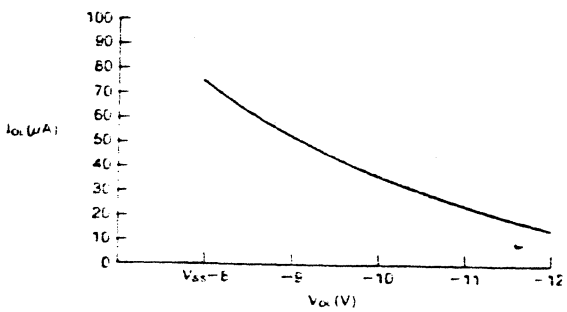
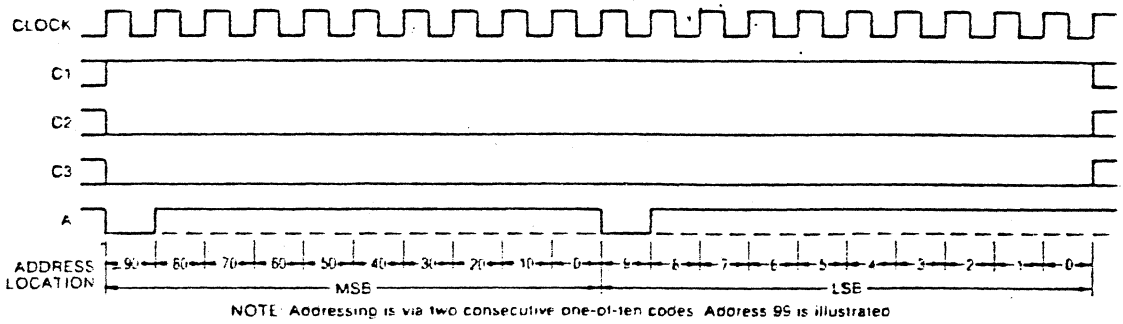


Fig.9 TYPICAL OUTPUT SINK CURRENT vs OUTPUT VOLTAGE

TIMING DIAGRAMS



NOTE: Addressing is via two consecutive one-of-ten codes. Address 99 is illustrated.

Fig.1 ACCEPT ADDRESS

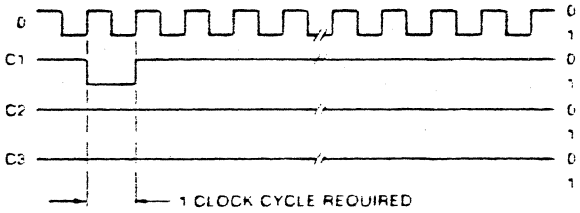
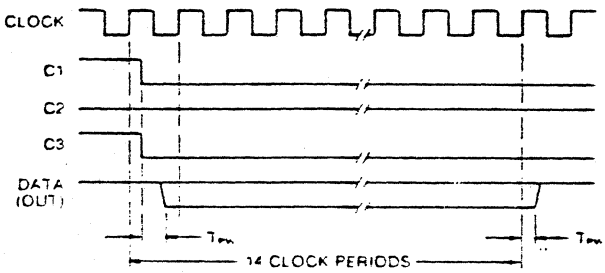


Fig.2 READ



T_{DA} measured initially from control line transition to data out, then measured from the positive clock edges to data changes. Timing measurements are made at V_{SS} - 2 and -10 volt points.

Fig.3 SHIFT DATA OUT

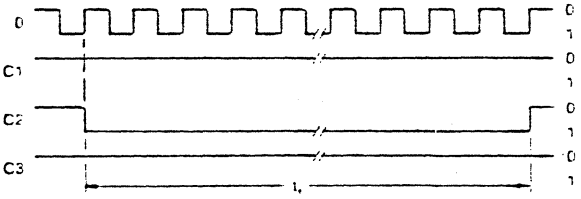


Fig.4 ERASE

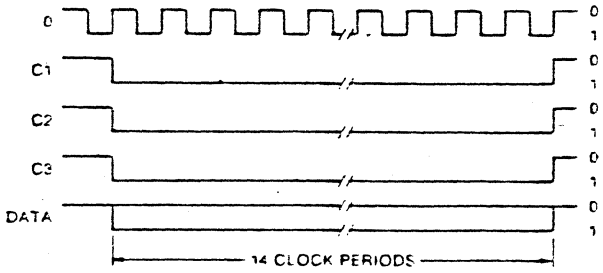


Fig.5 ACCEPT DATA

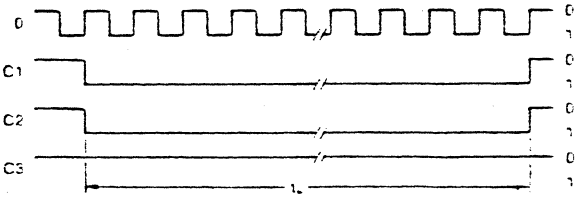


Fig.6 WRITE

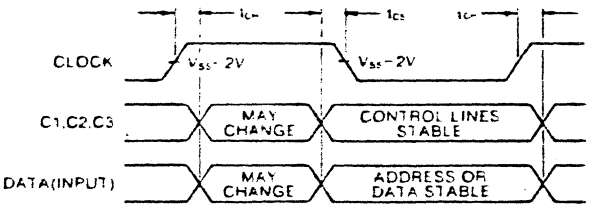
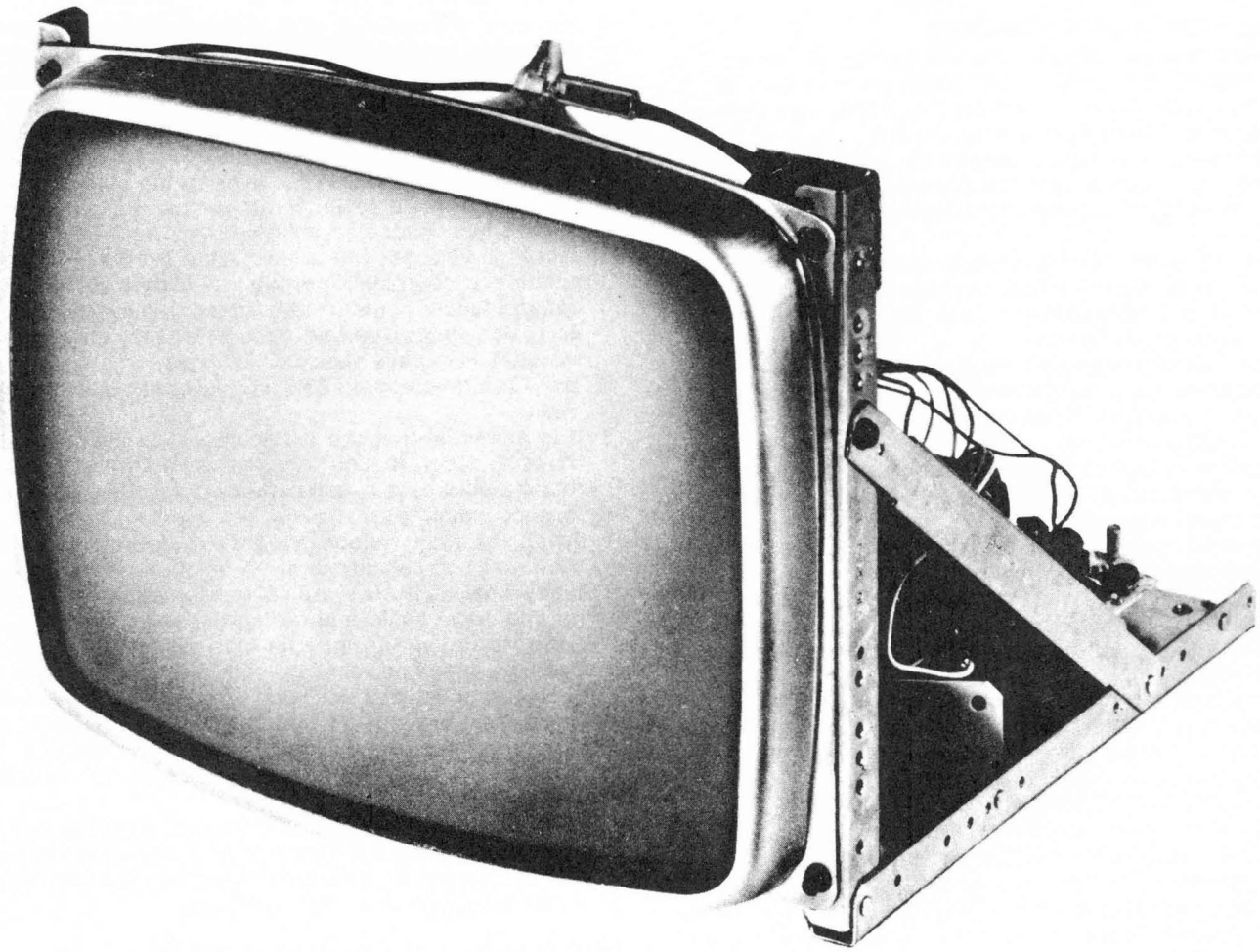


Fig.7 INPUT TIMING

7.0 TV MONITOR

SERVICE MANUAL



DT2

D12 SERIES DATA DISPLAY TERMINALS

ZENITH RADIO CORPORATION

1000 MILWAUKEE AVENUE, GLENVIEW, ILLINOIS 60025

DT2
2MRR

PRINTED IN U. S. A.
AUG, 1979

$2.00
923-951

PRODUCT SAFETY SERVICING GUIDELINES FOR ZENITH DATA DISPLAY TERMINALS

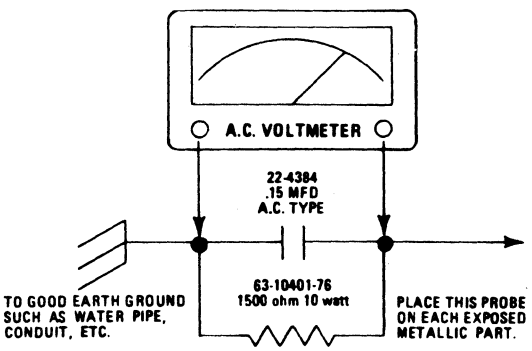
CAUTION: No modification of any circuit should be attempted. Service work should be performed only after you are thoroughly familiar with all of the following safety checks and servicing guidelines. To do otherwise increases the risk of potential hazards and injury to the user.

SAFETY CHECKS

After the original service problem has been corrected, a check should be made of the following:

SUBJECT: FIRE & SHOCK HAZARD

1. Be sure that all components are positioned in such a way to avoid possibility of adjacent component shorts. This is especially important on those chassis which are transported to and from the repair shop.
2. Never release a repair unless all protective devices such as insulators, barriers, covers, shields, strain reliefs, and other hardware have been reinstalled per original design.
3. Soldering must be inspected to uncover possible cold solder joints, frayed leads, damaged insulation, solder splashes or sharp solder points. Be certain to remove all loose foreign material.
4. Check "across-the-line" capacitor (if used) and other components for physical evidence of damage or deterioration and replace if necessary. Follow original layout, lead length and dress.
5. No lead or component should touch a resistor rated at 1 watt or more. Lead tension around protruding metal surfaces must be avoided.
6. All critical components (shaded on the schematic diagram and parts lists) such as: fuses, flameproof resistors, capacitors, etc., must be replaced with exact Zenith types. Do not use replacement components other than those specified or make unrecommended circuit modifications.
7. After re-assembly of the terminal always perform an AC leakage test on all exposed metallic parts of the cabinet and screws to be sure the terminal is safe to operate without danger of electrical shock. DO NOT USE A LINE ISOLATION TRANSFORMER DURING THIS TEST. Use an AC voltmeter having 5000 ohms per volt or more sensitivity in the following manner: Connect a 1500 ohm 10 watt resistor (63-10401-76), paralleled by a 0.15 mfd., 150V AC type capacitor (22-4384) between a known good earth ground (water pipe, conduit, etc.) and the exposed metallic parts, one at a time. Measure the AC voltage across the combination 1500 ohm resistor and 0.15 mfd. capacitor. Reverse the AC plug and repeat AC voltage measurements for each exposed metallic part. Voltage measured must not exceed 0.75 volts RMS. This corresponds to 0.5 milliamp AC. Any value exceeding this limit constitutes a potential shock hazard and must be corrected immediately.



SUBJECT: IMPLOSION PROTECTION

1. All Zenith picture tubes are equipped with an integral implosion protection system, but care should be taken to avoid damage during installation. Avoid scratching the tube.
2. Use only Zenith replacement tubes.

SUBJECT: X-RADIATION

1. Be sure procedures and instructions to all service personnel cover the subject of X-radiation. The only potential source of X-rays is the picture tube. However, this tube does not emit X-rays when the HV is at the factory-specified level. It is only when the HV is excessive that X-radiation can be generated. The basic precaution which must be exercised is to keep the HV at the factory-recommended level. Refer to the X-ray Precaution Label which is located inside each terminal for the correct high voltage. The proper value is also given in the schematic diagram. Operation at higher voltages may cause a failure of the picture tube or high voltage supply and, also, under certain circumstances, may produce radiation in excess of desirable levels.
2. Only Zenith-specified CRT anode connectors must be used.
3. It is essential that the serviceman has available at all times an accurate high voltage meter. The calibration of this meter should be checked periodically against a reference standard.
4. When the high voltage circuitry is operating properly there is no possibility of an X-radiation problem. Every time a chassis is serviced, the brightness should be run up and down while monitoring the high voltage with a meter to be certain that the high voltage does not exceed the specified value and that it is regulating correctly. We suggest that you and your service organization review test procedures so that voltage regulation is always checked as a standard servicing procedure, and that the reason for this prudent routine be clearly understood by everyone.
5. When trouble shooting and making test measurements in a terminal with a problem of excessive high voltage, do not operate the chassis longer than is necessary to locate the cause of excessive voltage.

IMPORTANT NOTE: DAG GROUNDING.

Each unit provides for grounding of the main P.C. Board and CRT socket board to the dag of the CRT through the dag grounding spring.

The ground wires are connected to the shell bond or T-band through a terminal lug. Upon installing the Video Display in a terminal, this grounding procedure should be followed to provide adequate high voltage filtering and arc protection. This especially pertains to mounting the video display as a kit version.

CAUTION

NO WORK SHOULD BE ATTEMPTED ON ANY EXPOSED MONITOR CHASSIS BY ANYONE NOT FAMILIAR WITH SERVICING PROCEDURES AND PRECAUTIONS.

GENERAL INFORMATION

This service manual introduces the Zenith D12 series of Video Displays. The series includes three basic forms: the D12-PF which is complete with power supply and frame, the D12-NF without power supply, the D12-NK in kit form which comes without frame or power supply.

The D12 series incorporate precision CRT's which provide uniformity of display and controlled spot size and geometry. The display may be operated from a standard 15 volt D.C. supply (or optional 12 V.D.C.) or from 120 volts A.C.

Input and output connections for the displays are made through a 10 pin edge connector on the main circuit board. Provision has been made for an optional remote brightness control. Schematic reference numbers are printed on the circuit board to aid in the location and identification of components for servicing.

Vertical and horizontal linearity is maintained within specifications without the use of linearity controls or adjustable devices. Excellent vertical linearity is assured by the extensive use of current feedback and horizontal linearity is achieved with a fixed saturable reactor.

Vertical and horizontal deflection systems sustain scan even in the absence or interruption of synchronizing signals. Vertical and horizontal synchronization is automatic and stable throughout the entire specified operating frequency range.

SPECIFICATIONS

CATHODE RAY TUBE

12″ diagonal measure, 90° deflection, 12.5KV nominal high voltage at 50μ A. beam current. Available with bonded anti-reflective face plate option. P4 phosphor is standard and other EIA phosphors are available.

NOMINAL DISPLAY AREA

51 sq. in. defined by a rectangle 8 1/2″ × 6″ centered on the CRT. (Other display dimensions optional.)

INPUT SIGNALS (TTL LEVEL)

HORIZONTAL
4 to 40μ sec. duration (positive going standard).
VERTICAL
50 to 2500μ sec. duration (negative going standard).
VIDEO
1.0V to 2.5V P-P (internal or customer supplied 500Ω contast control for higher input levels).
Positive polarity for white characters. (Other polarities are available for horizontal and vertical sync.)

POWER SUPPLY

120V ± 10% or 240V ± 10%
(customer strappable) 47 to 63 Hz., or
15V DC at 800 ma. max., or
12V DC at 1100 ma. max.

BRIGHTNESS CONTROL

Internal or Customer supplied 100 KΩ potentiometer (accessible at pins 2, 3 and 4 of edge connector).

INTERCONNECT TO CUSTOMER SYSTEM

Via standard 10-pin edge connector.
VIKING #25V10S/1-2
AMP #225-21031-101
CINCH #250-10-30-170

RESOLUTION

900 vertical lines minimum at center of display and 700 vertical lines at the corners. Pulse rise time less than 20 nanoseconds, for 30V rise at CRT. Bandwidth is within 3db from 10 Hz. to 18 MHz.

GEOMETRY

NOTE: Measurements made with an input of 1.0-2.5V P-P and with the display adjusted to 6″ highx8½″ wide.

VERTICAL

a. Height of display at left side shall be within ± 2.0 percent of height at right side.
b. Top and bottom pincushion or barrel shall be within ±1.25% of the average height.

HORIZONTAL

a. Width of display at top shall be within ±2.5% of the width at bottom.
b. Side pincushion or barrel shall be within ± 1.0% of the average width.

LINEARITY

No character shall vary in width or height by more than ±10% of the average width or height of all the characters in a row or column respectively.No specific character shall vary in width or height more than ±10% of an adjacent character.

SYNCHRONIZATION

HORIZONTAL
15.75 ± 0.5KHz.
18.60 ± 0.5KHz. (Optional)
Horizontal Blanking
9.0μ sec. min.
Horizontal Phasing Control
11.0 μ sec. nominal range
VERTICAL
47 to 63 Hz.
VERTICAL RETRACE TIME
850μsec. max.

STORAGE

55° C. max. with bonded anti-reflective faceplate.
65° C. max. for plain faced CRT's.

ENVIRONMENT

Operating temperature
55° max. (free air temperature of display electronics).
Altitude
40,000 ft. + storage & shipment.
10,000 ft. max. operating.

WEIGHT

11.5 lbs. max. without optional power supply.
13.5 lbs. max. with optional power supply.
9.0 lbs. max. without frame.

THEORY OF OPERATION

POWER SUPPLY

Power Transformer TX201 is designed for use with 120V or 240V A.C. source. The secondary provides power to bridge rectifier (CR501, CR502, CR503 and CR504). The positive output of the bridge rectifier (junction of CR503 and CR504), forms the raw B+ supply (~ 20VDC).

Voltage regulation is accomplished in the negative leg of the power supply through a feedback network consisting of transistors QX501 and QX502 and their associated circuitry. The emitter voltage of QX501 is maintained by diodes CR505, CR506 and CR507. The base voltage is provided by potentiometer RX506.

If B+ increases, diodes CR505, CR506 and CR507 will draw more current to maintain the emitter voltage of QX501. Additionally, the voltage developed across RX506 will increase, resulting in a higher positive voltage at the base of QX501 which will result in less conduction. This reduces the base current of QX502 since QX501 provides the emitter/base current path for QX502. When QX502 conducts less, the voltage drop across Q502 is increased thus lowering B+.

If B+ decreases, diodes CR505, CR506 and CR507 will reduce conduction to maintain the emitter voltage of QX501. Additionally, the base voltage provided by RX506 will decrease. Less voltage on the base of QX501 will cause it to increase conduction, resulting in a greater emitter/base current flow in QX502. With this condition the voltage drop for Q502 is less and B+ is increased.

HORIZONTAL

The low-level horizontal section, which consists of transistors Q101 and Q102 (and associated circuitry), functions as a variable time delay monostable multivibrator. The input trigger for this circuit is provided by the horizontal drive pulse. The pulse is injected into the base or emitter (for either positive or negative pulse respectively) of Q101 through injection network C101, C111, R101, R110 and CR101. By varying the recovery time of the multivibrator, potentiometer R104 adjusts video information position (with respect to raster scan). Output of the monostable multivibrator, derived at the collector of Q102, is injected through a coupling network consisting of C110 and CR103. The resulting "Lock" signal is rereceived by one side of a precision astable multivibrator at the emitter of Q103. The astable multivibrator circuit is completed through Q104 and associated circuitry. This circuit will act as a free running oscillator until the "Lock" signal is received from the previous stage. Once locked, an output pulse is formed at the emitter of Q104 which is then D.C. coupled to the base of the horizontal driver transistor, Q105.

Remainder of the horizontal circuit is straightforward. Features to be noted are: Width and Linearity Coils LX102 and LX101 in series with the yoke (TX202). Linearity is fixed and an adjustable coil is provided for width. The linearity coil has a magnetically biased core which makes the inductance of the coil dependent upon its current. Pincushion and geometric corrections are made at the factory by the addition of rubber magnets around the plastic ring of the yoke. D.C. operation of 12 volts is accomplished by the (optional) addition of a boost circuit at the horizontal sweep transformer.

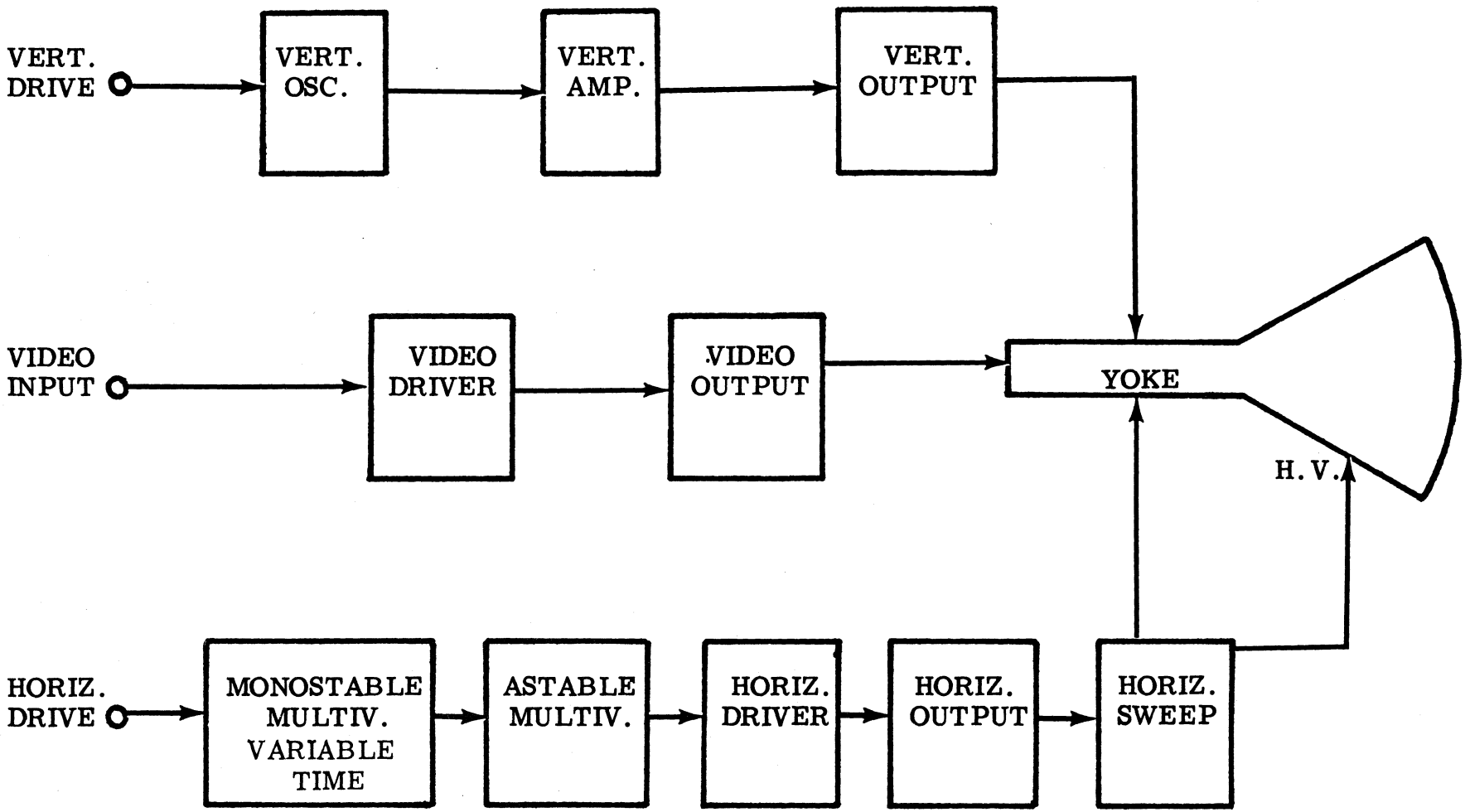
VERTICAL

The vertical circuit includes an oscillator consisting of transistors Q301 and Q302 and associated circuitry. Amplification is provided by transistors Q303 and Q304 with the emitter of Q304 feeding the base of the vertical driver Q305. The vertical output transistors, Q306 and Q307 are wired in the standard push-pull configuration. Transistor Q308 doubles B+ during retrace, maintaining less than 800 μ sec. of retrace time.

VIDEO

The video amplifier circuit consists of transistors Q401 and Q402 and associated circuitry. The circuit comprises a cascode amplifier which is triggered by a positive pulse at pin 8 of the edge connector. Upon receiving the input pulse, conduction is initiated and the collector voltage of Q402 is lowered. Amplification of low frequency voltage gain is fixed by the ratio of R407 and R408. Gain is maintained to 18 MHz by the bandwidth enhancing components R406, C403, and L401. Resistors R402 and R403 provide bias for the amplifier.

The collector output of Q401 is D.C. coupled to the cathode of the C.R.T. through resistor R201. Raster cut-off is adjusted with the brightness control R114 which is connected to G1 of the C.R.T.

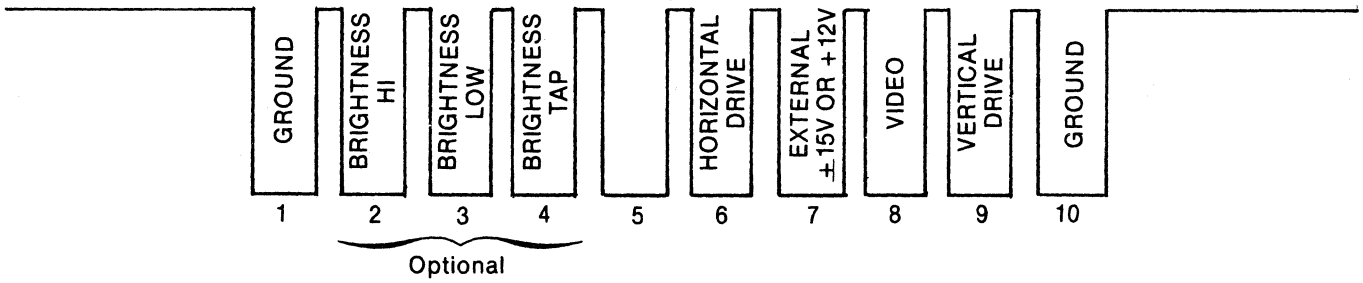

VERT.
DRIVE
VERT.
OSC.
VERT.
AMP.
VERT.
OUTPUT
VIDEO
INPUT
VIDEO
DRIVER
VIDEO
OUTPUT
YOKE
H.V.
HORIZ.
DRIVE
MONOSTABLE
MULTIV.
VARIABLE
TIME
ASTABLE
MULTIV.
HORIZ.
DRIVER
HORIZ.
OUTPUT
HORIZ.
SWEEP

ADJUSTMENT PROCEDURES FOR D12 VIDEO DISPLAY

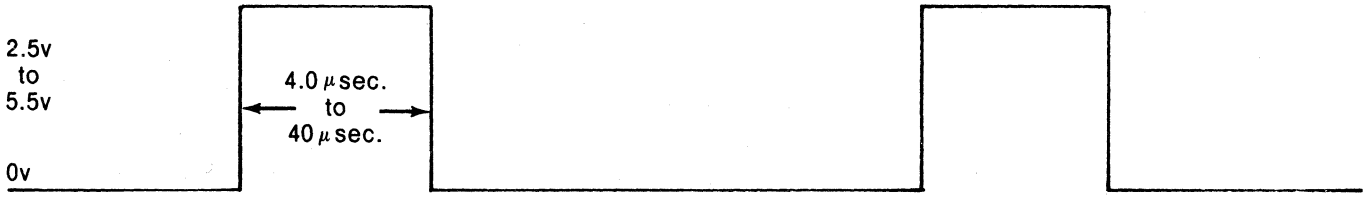
1. External power is applied to the monitor through an AC line cord or a 4 pin molex connector. The unit is wired for 120 VAC 50/60 Hz operation. (240 VAC 50/60 Hz optional)

2. INPUT SIGNALS: Input signals are connected to the display board through a 10 pin edge connector.

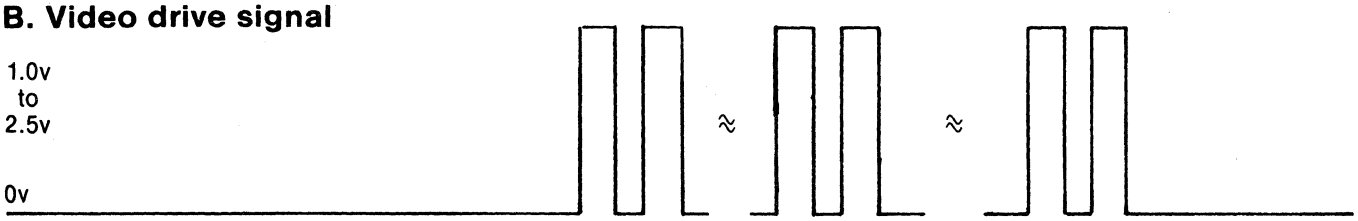
Component Side of Display Board



A. Horizontal drive signal — 15750Hz ± 500Hz, 18,600Hz ± 500Hz

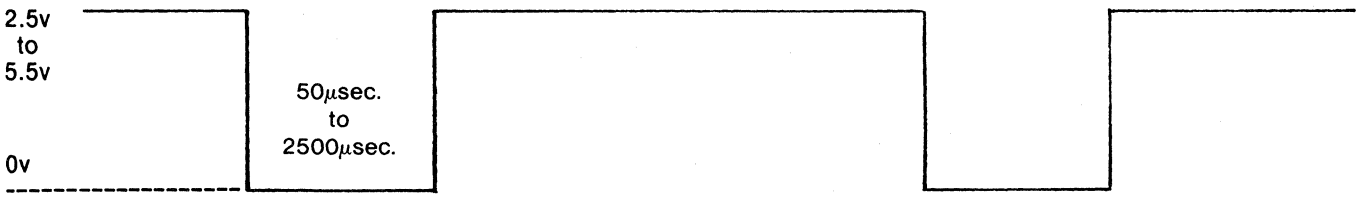


B. Video drive signal

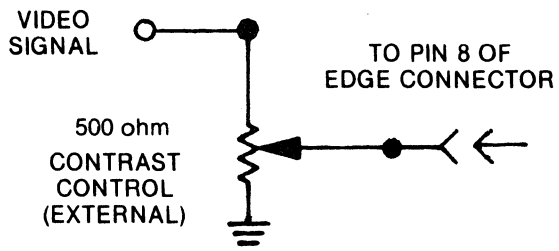


At a horizontal frequency of 15.7KHZ the video drive signal should start 11 microseconds ±5μ sec. after the leading edge of horizontal sync, and 900 microseconds or greater after the leading edge of vertical sync.

C. Vertical drive signal - 47Hz to 63Hz



Should the video drive level exceed the 2.5 volts specified, an external contrast control must be provided. The video drive signal is connected to the top end of the 500Ω pot, the bottom end is grounded and the wiper arm connects to the video input of the edge connector as shown.



3. Once power is applied to the display and the input signals connected, adjust the brightness control until the edges of the raster are visible.

4. Depending on the requirements for height and width of the video presentation, the vertical size control and width coil should be adjusted accordingly.

5. The power supply board also has a control to adjust the regulated B+ of the monitor to +15V. Check for proper adjustment.

6. Adjust the phase control to center the video information within the raster. (The contrast control may have to be adjusted to obtain a display of the video information.)

7. Adjust brightness control for visual cutoff of the raster.

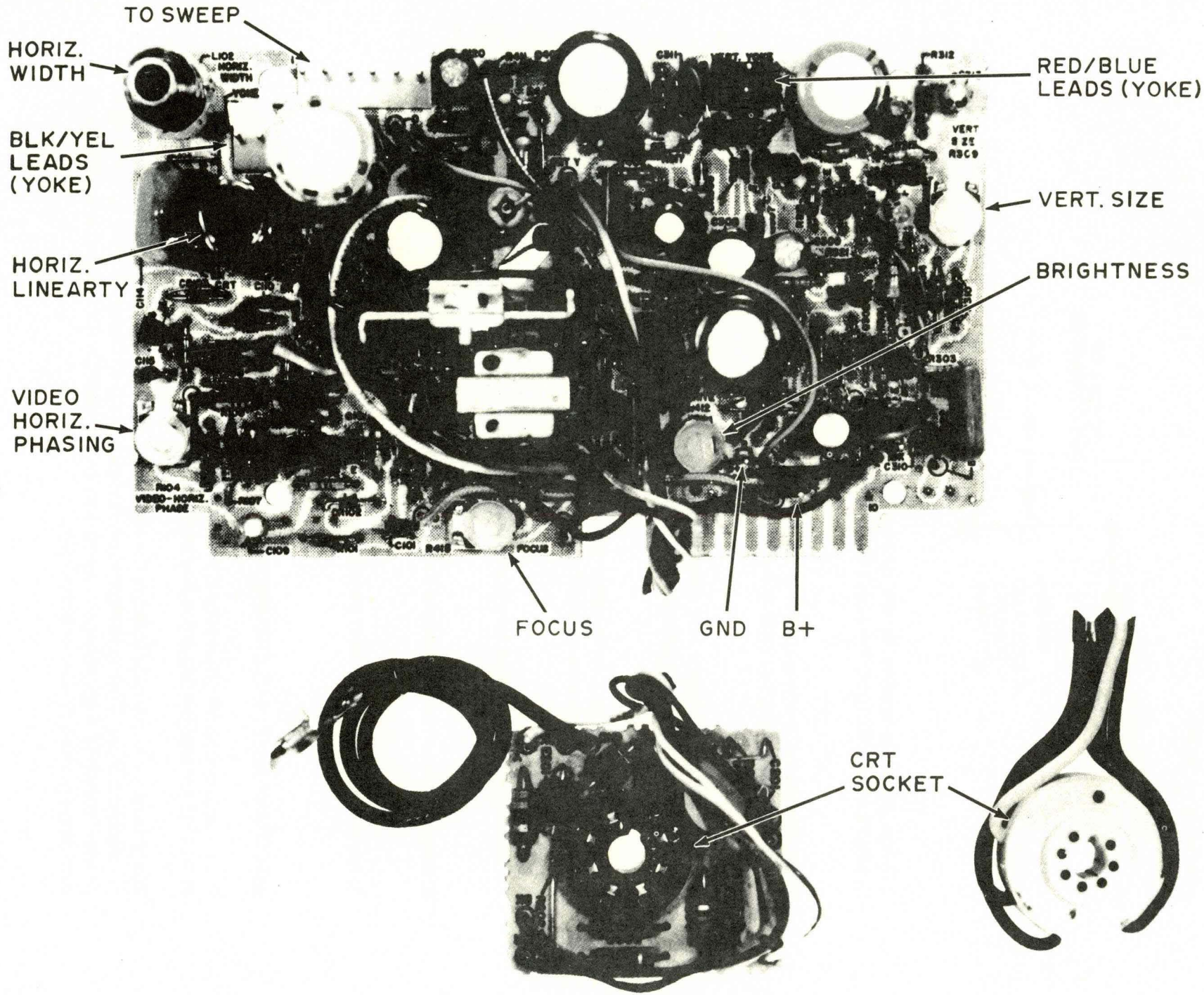
8. Adjust external contrast control for desired luminance.

9. Adjust focus control for best possible overall focus.

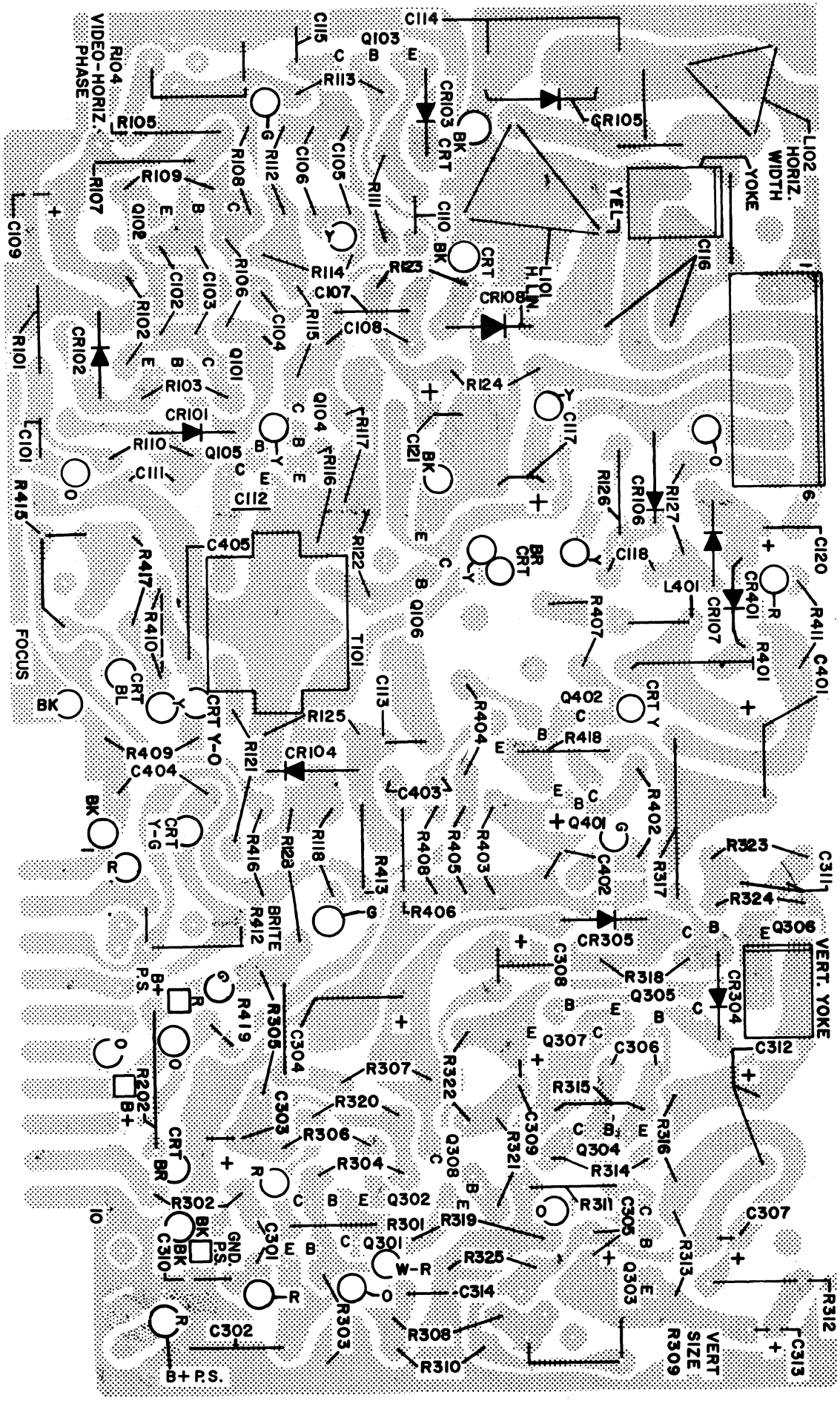
IMPORTANT NOTE: DAG GROUNDING.

Each unit provides for grounding of the main P.C. Board and CRT socket board to the dag of the CRT through the dag grounding spring.

The ground wires are connected to the shell bond or T-band through a terminal lug. Upon installing the Video Display in a terminal, this grounding procedure should be followed to provide adequate high voltage filtering and arc protection. This especially pertains to mounting the video display as a kit version.



VIDEO BOARD & CRT SOCKET

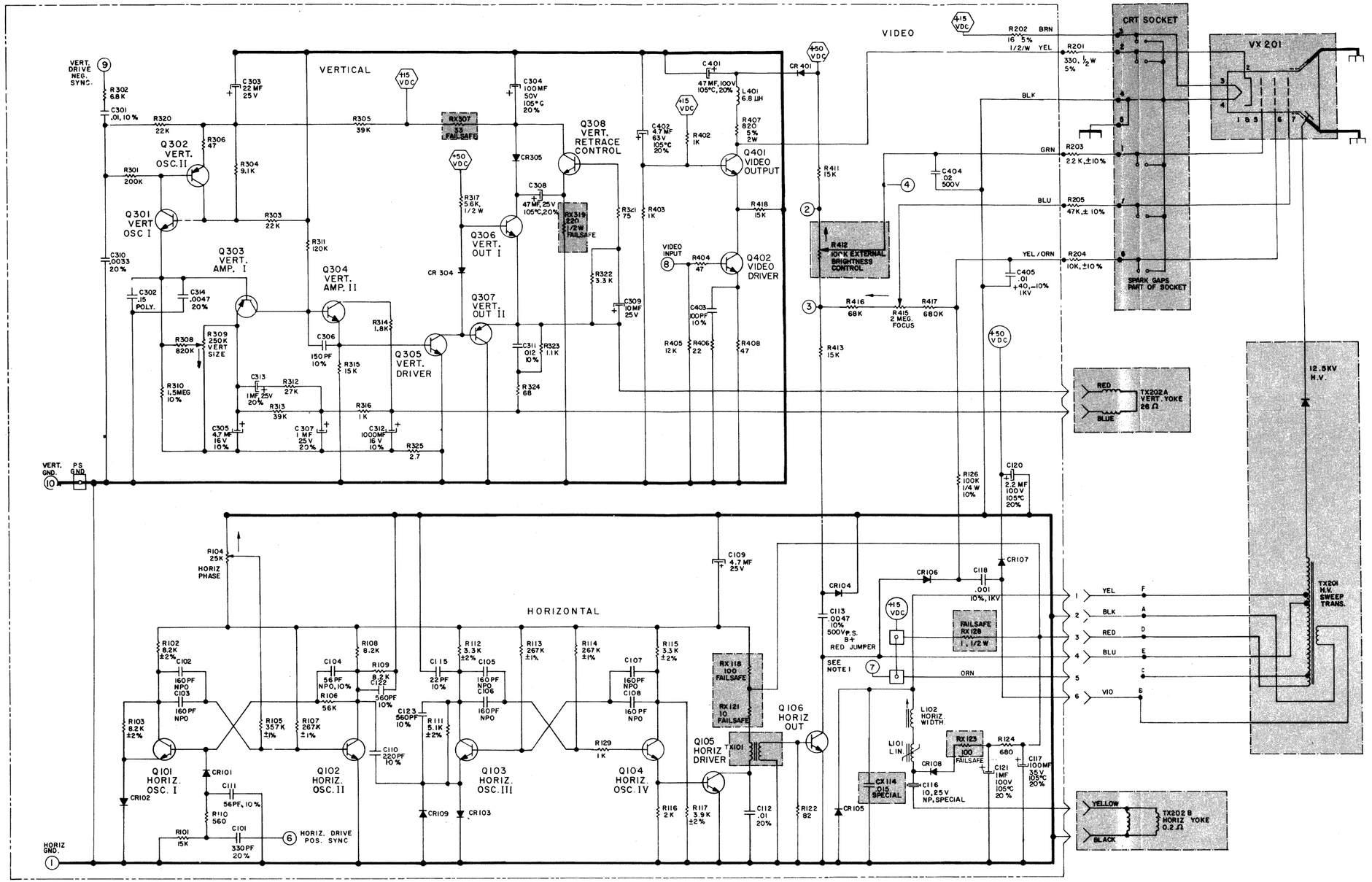

VIDEO-HORIZ. PHASE
R104
R105
R107
C109
R101
CR102
R102
Q102
C102
C103
R106
R108
R109
C105
C106
R112
C115
Q103
R113
C114
CR103
CRT
BK
CR105
LI02
HORIZ. WIDTH
YOKE
YEL
C116
R111
C110
R114
R123
C107
CR108
LI01
H LIN
C108
R115
C104
Q101
R103
CR101
R110
Q105
C111
C112
C101
R415
FOCUS
R124
C117
C121
R126
CR106
R127
C118
L401
C120
R411
C401
R401
CR401
CR107
R407
Q106
BR CRT
C405
R417
R410
T101
R122
R117
R116
C113
R404
Q402
R418
CRT BL
CRT Y-O
R125
R121
CR104
R409
C404
R416
R412
BRITE
R123
R118
R413
C403
R408
R405
R406
R403
R402
R317
CRT Y
CRT Y-G
R323
C311
R324
Q306
VERT. YOKE
CR305
R318
C308
Q305
CR304
C312
R419
B+ P.S.
R305
C304
R307
R320
R306
R304
R322
Q308
C309
R321
Q307
C306
R315
R316
Q304
R314
R202
B+
CRT BR
R302
BK
C310
GND. P.S.
C303
Q302
R301
R319
C301
Q301
W-R
R325
C314
R303
R308
R310
C302
B+ P.S.
C305
Q303
R313
C307
R312
C313
VERT SIZE
R309

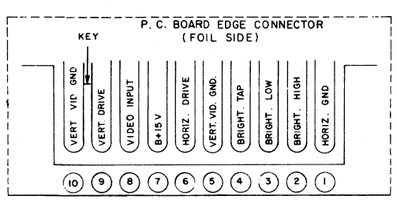
LEGEND

ITEM NO.	PART NO.	DESCRIPTION	
C101	22-7614-06A	330 PFD. CAPACITOR ±20% DISC.	50V
C102	22-7619-39A	160 PFD CAPACITOR ±5% DISC. NPO	50V
C103	22-7619-39A	160 PFD. CAPACITOR ±5% DISC. NPO	50V
C104	22-7622-28A	56 PFD CAPACITOR ±10% DISC NPO	50V
C105	22-7619-39A	160 PFD CAPACITOR ±5% DISC NPO	50V
C106	22-7619-39A	160 PFD CAPACITOR ±5% DISC NPO	50V
C107	22-7619-39A	160 PFD CAPACITOR ±5% DISC NPO	50V
C108	22-7619-39A	160 PFD CAPACITOR ±5% DISC NPO	50V
C109	22-7152-03	4.7 MFD CAPACITOR ELEC. +100%-10%	25V
C110	22-7613-04A	220 PFD CAPACITOR ±10% DISC	50V
C111	22-7622-28A	56 PFD CAPACITOR ±10% DISC	50V
C112	22-7614-24A	.01 MFD CAPACITOR ±20% DISC	50V
C113	22-7440	.0047 MFD CAPACITOR ±10% DISC	500V
CX114	22-7530-07	.015 MFD CAPACITOR SPECIAL..	
C115	22-7656-13A	22 PFD CAPACITOR ±10% DISC	50V
C116	22-7313	10 MFD CAPACITOF SPECIAL	
C117	22-7719-09	100 MFD CAPACITOR ±20% ELEC.	35V
C118	22-3748	.001 MFD CAPACITOR ±10% DISC	1KV
C120	22-7722-02	2.2 MFD CAPACITOR, ±20% ELEC.	100V
C121	22-7722-01	1 MFD CAPACITOR, ±20% ELEC.	100V
C122	22-7613-09	560 PFD CAPACITOR ±10% DISC.	50V
C123	22-7613-09	560 PFD CAPACITOR ±10% DISC.	50V
C301	22-7613-24A	.01 MFD CAPACITOR ±10% DISC	50V
C302	22-7548	.15 MFD CAPACITOR ±10% POLYESTER	50V
C303	22-7152-05	22 MFD CAPACITOR +100-10% ELEC.	25V
C304	22-7720-09	100 MFD CAPACITOR ±20% ELEC. 105°C	50V
C305	22-7579-03	4.7 MFD CAPACITOR ELEC. ±10%	16V
C306	22-7613-02A	150 PFD CAPACITOR ±10% DISC	50V
C307	22-7389-02	1MFD CAPACITOR ±20% ELEC.	25V
C308	22-7718-08	47 MFD CAPACITOR ±20% ELEC.	25V
C309	22-7152-04	10 MFD CAPACITOR ±100-10% ELEC 105°C	25V
C310	22-7614-18A	.0033 MFD CAPACITOR ±20% DISC	50V
C311	22-7613-25A	.012 MFD CAPACITOR ±10% DISC	50V
C312	22-7579-04	1000 MFD CAPACITOR ±10% ELEC.	16V
C313	22-7389-02	1 MFD CAPACITOR ±20% ELEC.	25V
C314	22-7614-20A	.0047 MFD CAPACITOR ±20% DISC	50V
C401	22-7722-08	47 MFD CAPACITOR ±20% ELEC. 105°C	100V
C402	22-7721-04	4.7 MFD CAPACITOR ±20% ELEC. 105°C	63V
C403	22-7613A	100 PFD CAPACITOR ±10% DISC	50V
C404	22-7724	.02 MFD. CAPACITOR +80-20% DISC.	500V
C405	22-3512	.01 MFD CAPACITOR +40-10% DISC	1KV
R101	63-9922	15K OHM RESISTOR ±5% FILM	1/4W
R102	63-9919-94	8.2K OHM RESISTOR ±2% FILM	1/4W
R103	63-9919-94	8.2K OHM RESISTOR ±2% FILM	1/4W
R104	63-10651-11	CONTROL 25K OHM (HORIZ. PHASE)	
R105	63-10533-05	357K OHM RESISTOR ±1% METAL FILM	1/4W
R106	63-9922-14	56K OHM RESISTOR ±5% FILM	1/4W
R107	63-10533-04	267K OHM RESISTOR ±1% METAL FILM	1/4W
R108	63-9921-94	8.2K OHM RESISTOR ±5% FILM	1/4W
R109	63-9921-94	8.2K OHM RESISTOR ± 5% FILM	1/4W
R110	63-9921-66	560 OHM RESISTOR ±5% FILM	1/4W
R111	63+0351-89	5.1KOHM RESISTOR ±2% FILM	1/4W
R112	63-9919-84	3.3KOHM RESISTOR ± 2%FILM	1/4W
R113	63-10533-04	267K OHM RESISTOR ± 1% METAL FILM	1/4W
R114	63-10533-04	267K OHM RESISTOR ± 1% METAL FILM	1/4W
R115	63-9919-84	3.3K OHM RESISTOR ±2% FILM	1/4W
R116	63-9921-79	2K OHM RESISTOR ±5% FILM	1/4W
R117	63-9919-86	3.9K OHM RESISTOR ±2% FILM	1/4W
▮RX118	63-10559-48	100 OHM RESISTOR ± 5% FAILSAFE	1/4W
▮RX121	63-10559-24	10 OHM RESISTOR ± 5% FAILSAFE	1/4W
R122	63-9921-46	82 OHM RESISTOR ± 5% FILM	1/4W
▮RX123	63-10559-48	100 OHM RESISTOR ± 5% FAILSAFE	1/4W
▮RX124	63-10559-66	680 OHM RESISTOR ± 5% FAILSAFE	1/4 W 1/4W
R126	63-10184-20	100K OHM RESISTOR ±10% CARBON COMP	1/4W
▮RX128	63-10565	1 OHM RESISTOR ± 5% FAILSAFE	1/2W
R129	63-8797	1K OHM RESISTOR ±5% FILM	1/4W
R201		330 OHM RESISTOR ±5% CARBON COMP	1/2W
R202		16 OHM RESISTOR ± 5% CARBON COMP	1/2W
R203	REFERENCE	2.2KOHM RESISTOR ±10% CARBON COMP	1/2W
R204	ONLY	10 K OHM RESISTOR ±10% CARBON COMP	1/2W

ITEM NO.	PART NO.	DESCRIPTION	
R205		47K OHM RESISTOR ±10% CARBON COMP	1/2W
R301	63-9922-27	200 K OHM RESISTOR ±5% FILM	1/4W
R302	63-9921-92	6.8 K OHM RESISTOR ± 5% FILM	1/4W
R303	63-9922-04	22K OHM RESISTOR ± 5% FILM	1/4W
R304	63-9921-95	9.1 K OHM RESISTOR ±5% FILM	1/4W
R305	63-9922-10	39K OHM RESISTOR ± 5% FILM	1/4W
R306	63-9921-40	47 OHM RESISTOR ± 5% FILM	1/4W
▮RX307	63-10559-36	33 OHM RESISTOR ± 5% FAILSAFE	1/4W
R308	63-9922-42	820K OHM RESISTOR ± 5% FILM	1/4W
R309	63-10651-13	CONTROL 250K OHM VERT. SIZE	
R310	63-9924-48	1.5 MEG OHM RESISTOR ± 10% FILM	1/4W
R311	63-9922-22	120 K OHM RESISTOR ± 5% FILM	1/4W
R312	63-9922-06	27K OHM RESISTOR ± 5% FILM	1/4W
R313	63-9922-10	39K OHM RESISTOR ± 5% FILM	1/4W
R314	63-9921-78	1.8 K OHM RESISTOR ± 5% FILM	1/4W
R315	63-9922	15 K OHM RESISTOR ± 5% FILM	1/4W
R316	63-9921-72	1K OHM RESISTOR ±5% FILM	1/4W
R317	63-7816	5.6 K OHM RESISTOR ± 5% CARBON COMP	1/2W
R318			
▮RX319	63-10565-56	220 OHM RESISTOR ± 5% FAILSAFE	1/2W
R320	63-9922-04	22K OHM RESISTOR ± 5% FILM	1/4W
R321	63-9921-45	75 OHM RESISTOR ± 5% FILM	1/4W
R322	63-9921-84	3.3K OHM RESISTOR ± 5% FILM	1/4W
R323	63-9921-73	1.1K OHM RESISTOR ±5% FILM	1/4W
R324	63-9921-44	68 OHM RESISTOR ±5%FILM	1/4W
R325	63-9921-10	2.7 OHM RESISTOR ±5% FILM	1/4W
R402	63-9921-72	1K OHM RESISTOR ±5% FILM	1/4W
R403	63-9921-72	1K OHM RESISTOR ± 5% FILM	1/4W
R404	63-9921-40	47 OHM RESISTOR ± 5% FILM	1/4 W
R405	63-8821	12K OHM RESISTOR ± 5% FILM	1/4W
R406	63-9921-32	22 OHM RESISTOR ± 5% FILM	1/4W
R407	63-10371-70	820 OHM RESISTOR ± 5% FILM	2W
R408	63-9921-40	47 OHM RESISTOR ± 5% FILM	1/4W
R411	63-9922-	15K OHM RESISTOR ±5% FILM	1/4W
R412			
R413	63-9922-04	15K OHM RESISTOR ±5% FILM	1/4W
R415	63-10812-01	CONTROL 2 MEG OHM FOCUS	
R416	63-9922-16	68K OHM RESISTOR ±5% FILM	1/4W
R417	63-9922-40	680K OHM RESISTOR ±5% FILM	1/4W
R418	63-9922	15K OHM RESISTOR ±5% FILM	1/4W
L101	20-3906	COIL,RCF LINEARITY	
L102	20-3882	COIL, RCF TUNABLE WIDTH	
L401	20-3887-10C	COIL, RCF 6.8 uh	
▮TX101	95-3138-03	TRANSFORMER HORIZ DRIVER	
▮TX201	95-3395-01	H.V. SWEEP TRANSFORMER	
▮TX202	95-3397-02	DEFLECTION YOKE	
CR101	103-142-01	DIODE	
CR102	103-142-01	DIODE	
CR103	103-142-01	DIODE	
CR104	103-295-03 A	DIODE	
CR105	103-284	DIODE	
CR106	212-76 -02	DIODE	
CR107	103-296-05A	DIODE	
CR108	212-76	DIODE	
CR109	103-142-01	DIODE	
CR304	103-142-01	DIODE	
CR305	212-76	DIODE	
CR401	212-76	DIODE	
Q101	121-975	TRANSISTOR	HORIZ. OSC.I
Q102	121-975	TRANSISTOR	HORIZ. OSC II
Q103	121-975	TRANSISTOR	HORIZ. OSC.III
Q104	121-975	TRANSISTOR	HORIZ. OSC.IV
Q105	121-819	TRANSISTOR	HORIZ DRIVER
Q106	121-1039	TRANSISTOR	HORIZ. OUTPUT
Q301	121-975	TRANSISTOR	VERT. OSC. I
Q302	121-699	TRANSISTOR	VERT. OSC. II
Q303	121-699	TRANSISTOR	VERT. AMP. I
Q304	121-975	TRANSISTOR	VERT. AMP. II
Q305	121-972	TRANSISTOR	VERT. DRIVER
Q306	121-819	TRANSISTOR	VERT. OUTPUT I
Q307	121-973	TRANSISTOR	VERT. OUTPUT II
Q308	121-819	TRANSISTOR	VERT. RETRACE
Q401	121-1058	TRANSISTOR 121-1034 ALT.	VIDEO OUTPUT
Q402	121-895	TRANSISTOR	VIDEO DRIVER
VX201	100-884	12" CRT	
OR	100-884-02	12" CRT	

D12 VIDEO DISPLAY 15.7KHz





= DC VOLTAGE SOURCE

= DC VOLTAGE APPLIED

NOTE 1. CUSTOMER SUPPLIED EXTERNAL DC SOURCE ON PIN 7 EDGE CONNECTOR

IMPORTANT SAFETY NOTICE

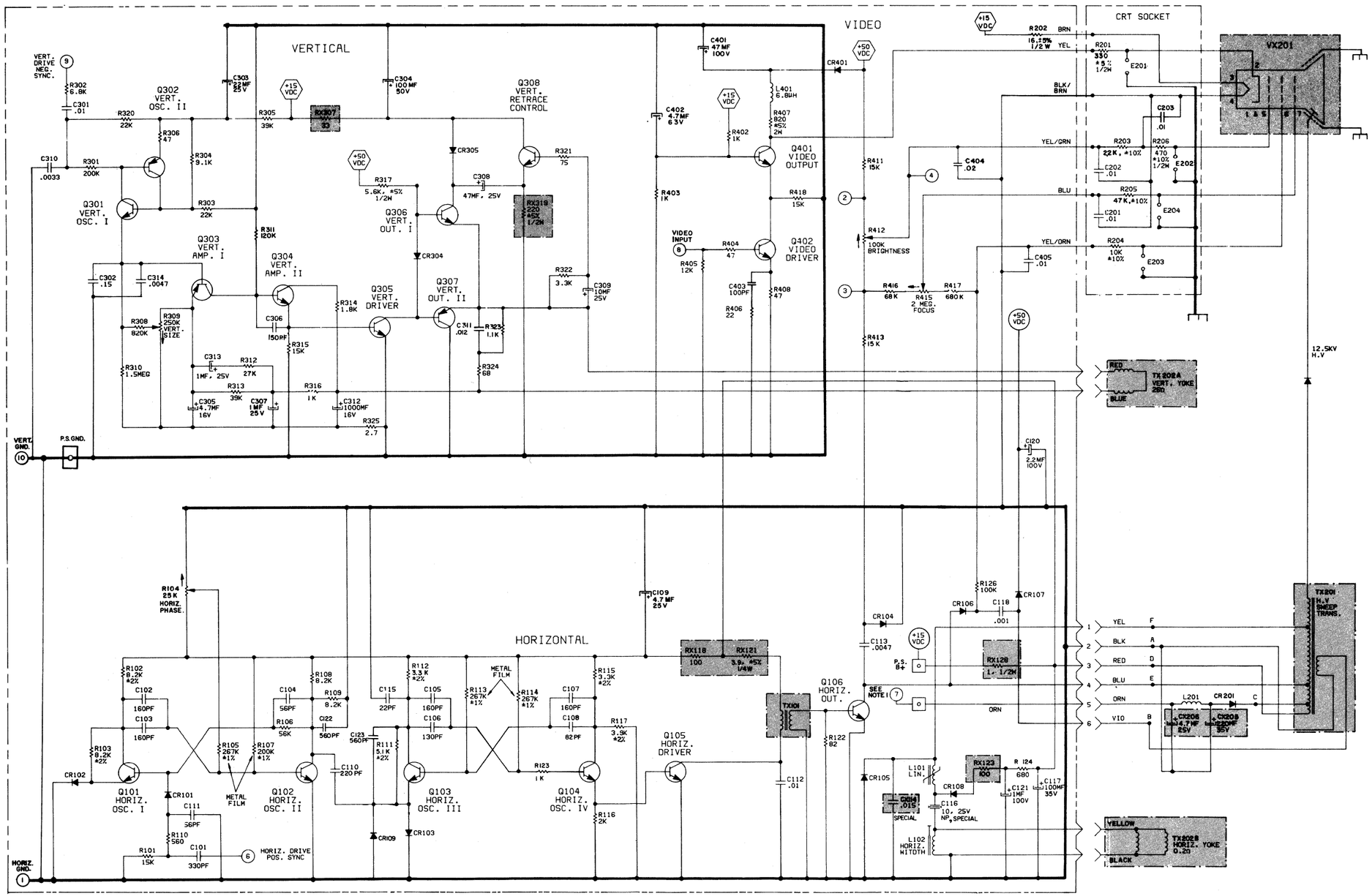
When servicing this chassis, under no circumstances should the original design be modified or altered without permission from the Zenith Radio Corporation. All components should be replaced only with types identical to those in the original circuit. Special components are used to prevent shock and fire hazard. These critical components are shaded on the schematic and parts list for easy identification.

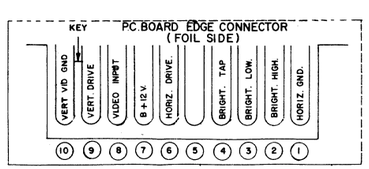
This circuit diagram may occasionally differ from the actual circuit used. This way, implementation of the latest safety and performance improvement changes into the set is not delayed until the new service literature is printed.

IMPORTANT SAFETY NOTICE

FOR X-RADIATION, FIRE OR SHOCK HAZARD PREVENTION, CERTAIN SPECIAL OR REDUNDANT PARTS ARE USED. USE ONLY EXACT REPLACEMENTS. DO NOT ALTER THE CIRCUIT OR DEFEAT THE FUSES. FAILURE TO COMPLY MAY BE UNLAWFUL.

D12 VIDEO DISPLAY 18.6KHz





= DC VOLTAGE SOURCE

= DC VOLTAGE APPLIED

NOTE L CUSTOMER SUPPLID EXTERNAL DC SOURCE ON PIN 7 EDGE CONNECTOR

IMPORTANT SAFETY NOTICE

When servicing this chassis, under no circumstances should the original design be modified or altered without permission from the Zenith Radio Corporation. All components should be replaced only with types identical to those in the original circuit. Special components are used to prevent shock and fire hazard. These critical components are shaded on the schematic and parts list for easy identification.

This circuit diagram may occasionally differ from the actual circuit used. This way, implementation of the latest safety and performance improvement changes into the set is not delayed until the new service literature is printed.

IMPORTANT SAFETY NOTICE

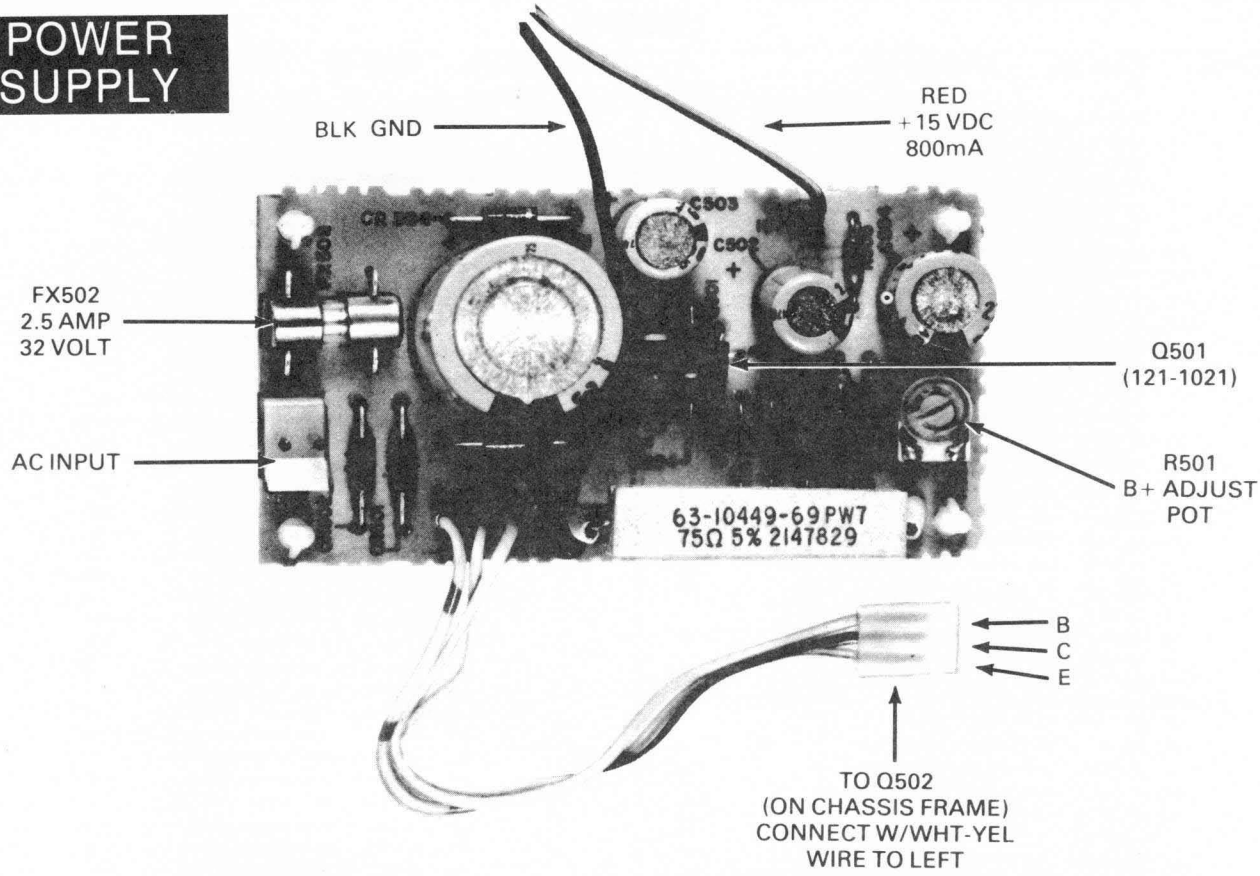
FOR X-RADIATION, FIRE OR SHOCK HAZARD PREVENTION, CERTAIN SPECIAL OR REDUNDANT PARTS ARE USED. USE ONLY EXACT REPLACEMENTS. DO NOT ALTER THE CIRCUIT OR DEFEAT THE FUSES. FAILURE TO COMPLY MAY BE UNLAWFUL.

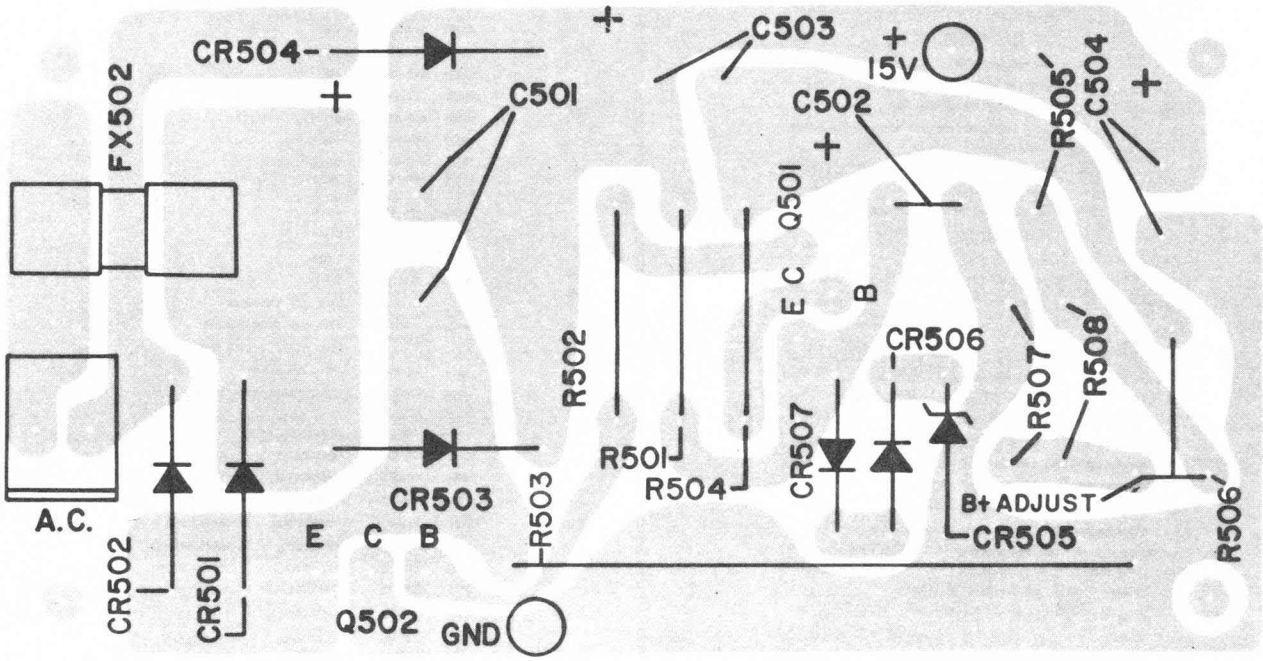
LEGEND

ITEM NO.	PART NO.	DESCRIPTION	
C101	22-7614-06A	330 PFD. CAPACITOR ±20% DISC.	50V
C102	22-7619-39A	180 PFD. CAPACITOR ±5% DISC. NPO	50V
C103	22-7619-39A	180 PFD. CAPACITOR ±5% DISC NPO	50V
C104	22-7622-28A	56 PFD CAPACITOR ±10% DISC	50V
C105	22-7619-39A	180 PFD CAPACITOR ±5% DISC NPO	50V
C106	22-7619-37A	130 PFD CAPACITOR ±5% DISC NPO	50V
C107	22-7619-39A	160 PFD CAPACITOR ±5% DISC NPO	50V
C108	22-7619-32A	82 PFD CAPACITOR ±5% DISC NPO	50V
C109	22-7152-03	4.7 MFD CAPACITOR +100%-10% ELEC.	25V
C110	22-7613-04A	220 PFD CAPACITOR ±10% DISC	50V
C111	22-7622-28A	56 PFD CAPACITOR ±10% DISC	50V
C112	22-7614-24A	.01 MFD CAPACITOR ± 20% DISC	50V
C113	22-7440	.0047 MFD CAPACITOR ±10% DISC	500V
C114	22-7530-07	.015 MFD CAPACITOR SPECIAL	
C115	22-7656-13A	22 PFD CAPACITOR ±10% DISC	50V
C116	22-7313	10 MFD CAPACITOR SPECIAL	
C117	22-7719-09	100 MFD CAPACITOR ± 20% ELEC. 105°C	35V
C118	22-3748	.001 MFD CAPACITOR ±10% DISC	1KV
C120	22-7722-02	2.2 MFD CAPACITOR ±20% ELEC. 105°C	100V
C121	22-7722-01	1 MFD CAPACITOR ±20% ELEC. 105°C	100V
C122	22-7613-09	560 PFD CAPACITOR ±10% DISC	50V
C123	22-7613-09	560 PFD CAPACITOR ±10% DISC	50V
C201	22-4905-01	.01 MFD CAPACITOR +80-20% DISC.	500V
C202	22-4905-01	.01 MFD CAPACITOR +80-20% DISC.	500V
C203	22-4905-01	.01 MFD CAPACITOR +80-20%DISC.	500V
▮CX205	22-7144-09	220 MFD CAPACITOR +100%-10% ELEC.	35V
▮CX206	22-7142-03	4.7 MFD CAPACITOR +100%-10% ELEC.	25V
C301	22-7613-24A	.01 MFD CAPACITOR ±10% DISC	50V
C302	22-7548	.15 MFD.CAPACITOR ±10% POLYESTER	50V
C303	22-7152-05	22 MFD CAPACITOR +100-10% ELEC.	25V
C304	22-7720-09	100 MFD CAPACITOR ±20% ELEC. 105°C	50V
C305	22-7579-03	4.7 MFD CAPACITOR ±10% ELEC.	16V
C306	22-7613-02A	150 PFD CAPACITOR ±10% DISC	50V
C307	22-7389-02	1 MFD CAPACITOR ±20% ELEC.	25V
C308	22-7718-08	47 MFD CAPACITOR ±20% ELEC. 105°C	25V
C309	22-7152-04	10 MFD CAPACITOR +100-10% ELEC.	25V
C310	22-7614-18A	.0033 MFD CAPACITOR ±20% DISC	50V
C311	22-7613-23A	.012 MFD CAPACITOR ±10% DISC.	50V
C312	22-7579-04	1000 MFD CAPACITOR ±10% ELEC.	16V
C313	22-7389-02	1 MFD CAPACITOR ±20% ELEC.	25V
C314	22-7614-20A	.0047 MFD CAPACITOR ±20% DISC	50V
C401	22-7722-08	47 MFD CAPACITOR ±20% ELEC. 105°C	100V
C402	22-7721-04	4.7 MFD CAPACITOR ±20% ELEC. 105°C	63V
C403	22-7613A	100 PFD CAPACITOR ±10% DISC	50V
C404	22-7724	.02 MFD CAPACITOR +80%-20% DISC.	500V
C405	22-3512	.01 MFD CAPACITOR +40-10% DISC	1KV
R101	63-9922	15K OHM RESISTOR ± 5% FILM	1/4W
R102	63-9919-94	8.2K OHM RESISTOR ±2% FILM	1/4W
R103	63-9919-94	8.2K OHM RESISTOR ± 2% FILM	1/4W
R104	63-10651-11	CONTROL 25K OHM (HORIZ. PHASE)	
R105	63-10533-04	267K OHM RESISTOR ± 1% (METAL FILM)	1/4W
R106	63-9922-14	56K OHM RESISTOR ± 5% FILM	1/4W
R107	63-10533-11	200K OHM RESISTOR ± 1% METAL FILM	1/4W
R108	63-9921-94	8.2K OHM RESISTOR ±5% FILM	1/4W
R109	63-9921-94	8.2K OHM RESISTOR ±5% FILM	1/4W
R110	63-9921-66	560 OHM RESISTOR ± 5%	1/4W
R111	63-10351-89	5.1KOHM RESISTOR ± 2% FILM	1/4W
R112	63-9919-84	3.3KK OHM RESISTOR ±2% FILM	1/4W
R113	63-10533-04	267K OHM RESISTOR 1% METAL FILM	1/4W
R114	63-10533-04	267K OHM RESISTOR ± 1% METAL FILM	1/4W
R115	63-9919-84	3.3K OHM RESISTOR ±2%	1/4W
R116	63-9921-79	2K OHM RESISTOR 5% FILM	1/4W
R117	63-9919-86	3.9K OHM RESISTOR ± 2% FILM	1/4W
▮RX118	63-10559-48	100 OHM RESISTOR ±5% FAILSAFE	1/4W
▮RX121	63-10559-14	3.9 OHM RESISTOR ± 5% FAILSAFE	1/4W
R122	63-9921-46	82 OHM RESISTOR ± 5%	1/4W
▮RX123	63-10559-48	100 OHM RESISTOR ± 5% FAILSAFE	1/4W
R 124	63-9321-68	680 OHM RESISTOR ±5% FILM	1/4W
R126	63-10814-20	100K OHM RESISTOR ± 5% CARBON COMP.	1/4W
▮RX128	63-10565-	1 OHM RESISTOR ±5% FAILSAFE	1/2W
R201	63-7763	330 OHM RESISTOR ±5% CARBON COMP.	1/2W
R202	63-7710	18 OHM RESISTOR ±5% CARBON COMP.	1/2W
R203	63-7799	2.2KOHM RESISTOR ±10% CARBON COMP.	1/2W
R204	63-7827	10K OHM RESISTOR ±10% CARBON COMP.	1/2W
R205	63-7855	47K OHM RESISTOR ±10% CARBON COMP.	1/2W
R206	63-7771	470 OHM RESISTOR ±10% CARBON COMP.	1/2W
R301	63-9922-27	200 K OHM RESISTOR ±5% FILM	1/4W
R302	63-9921-92	6.8 K OHM RESISTOR ±5% FILM	1/4W
R303	63-9922-04	22K OHM RESISTOR ±5% FILM	1/4W

ITEM NO.	PART NO.	DESCRIPTION	
R304	63-9921-95	9.1 K OHM RESISTOR ±5% FILM	1/4W
R305	63-9922-10	39K OHM RESISTOR ± 5% FILM	1/4W
R306	63-9921-40	47 OHM RESISTOR ±5% FILM	1/4W
▮RX307	63-10559-36	33 OHM RESISTOR ± 5% FAILSAFE	1/4W
R308	63-9922-42	820K OHM RESISTOR ± 5% FILM	1/4W
R309	63-10651-13	CONTROL 250K OHM VERT. SIZE	1/4W
R310	63-9924-48	1.5 MEG OHM RESISTOR ±10% FILM	1/4W
R311	63-9922-22	120K OHM RESISTOR ±5% FILM	1/4W
R312	63-9922-06	27K OHM RESISTOR ± 5% FILM	1/4W
R313	63-9922-10	39K OHM RESISTOR ± 5% FILM	1/4W
R314	63-9921-78	1.8K OHM RESISTOR ± 5% FILM	1/4W
R315	63-9922	15K OHM RESISTOR ± 5% FILM	1/4W
R316	63-9921-72	.1000 OHM RESISTOR ±5% FILM	1/4W
R317	63-7816	5.6K OHM RESISTOR ± 5% CARBON COMP.	1/2W
▮RX318	63-10565-36	220 OHM RESISTOR ± 5% FAILSAFE	1/2W
R320	63-9922-04	22K OHM RESISTOR ± 5% FILM	1/4W
R321	63-9921-45	75 OHM RESISTOR ± 5% FILM	1/4W
R322	63-9921-84	3.3K OHM RESISTOR ± 5% FILM	1/4W
R323	63-9921-73	1100 OHM RESISTOR ±5% FILM	1/4W
R324	63-9921-44	68 OHM RESISTOR ±5% FILM	1/4W
R325	63-9921-10	2.7 OHM RESISTOR ± 5% FILM	1/4W
R402	63-9921-72	1K OHM RESISTOR ± 5% FILM	1/4W
R403	63-9921-72	1K OHM RESISTOR ± 5% FILM	1/4W
R404	63-9921-40	47 OHM RESISTOR ± 5% FILM	1/4W
R405	63-8821	12K OHM RESISTOR ± 5% FILM	1/4W
R406	63-9921-32	22 OHM RESISTOR ± 5% FILM	1/4W
R407	63-10371-70	820 OHM RESISTOR ± 5% FILM	2W
R408	63-9921-40	47 OHM RESISTOR ±5% FILM	1/4W
R411	63-9922	15K OHM RESISTOR ±5% FILM	1/4W
R412	63-10651-12	CONTROL 100 K OHM BRIGHTNESS	
R413	63-9922	15K OHM RESISTOR ±5% FILM	1/4W
R415	63-10812-01	CONTROL 2 MEG OHM FOCUS	
R416	63-9922-16	68K OHM RESISTOR ±5% FILM	1/4W
R417	63-9922-40	680K OHM RESISTOR ±5% FILM	1/4W
R418	63-9922	15K OHM RESISTOR ±5% FILM	1/4W
CR101	103-142-01	DIODE	
CR102	103-142-01	DIODE	
CR103	103-142-01	DIODE	
CR104	103-295-03A	DIODE	
CR105	103-284	DIODE	
CR106	212-76-02	DIODE	
CR107	103-298-05A	DIODE	
CR108	212-76-02	DIODE	
CR109	103-142-01	DIODE	
CR201A	103-280-04	DIODE	
CR304	103-142-01	DIODE	
CR305	212-76-02	DIODE	
CR401	212-76-02	DIODE	
L101	20-3906-02	COIL, RCF LINEARITY	
L102	20-3905	COIL, RCF TUNABLE WIDTH	
L201	20-3824	COIL, HORIZ. FILTER CHOKE	
L401	20-3887-10C	COIL, RCF 6.8 Uh	
TX101	95-3136-03	TRANSFORMER HORIZ. DRIVER	
TX201	95-3305-01	H.V. SWEEP TRANSFORMER	
TX202	95-3307-02	DEFLECTION YOKE	
Q101	121-975	TRANSISTOR HORIZ OSC. I	
Q102	121-975	TRANSISTOR HORIZ. OSC. II	
Q103	121-975	TRANSISTOR HORIZ OSC. III	
Q104	121-975	TRANSISTOR HORIZ. OSC. IV	
Q105	121-819	TRANSISTOR HORIZ. DRIVER	
Q106	121-1039	TRANSISTOR HORIZ. OUTPUT	
Q301	121-975	TRANSISTOR VERT. OSC. I	
Q302	121-699	TRANSISTOR VERT. OSC. II	
Q303	121-699	TRANSISTOR VERT. AMP. I	
Q304	121-975	TRANSISTOR VERT. AMP II	
Q305	121-972	TRANSISTOR VERT. DRIVER	
Q306	121-819	TRANSISTOR VERT. OUTPUT I	
Q307	121-973	TRANSISTOR VERT. OUTPUT II	
Q308	121-819	TRANSISTOR VERT. RETRACE CONTROL	
Q401	121-1058	TRANSISTOR VIDEO OUTPUT 121-1034 ALT.	
Q402	121-895	TRANSISTOR VIDEO DRIVER	
E201	52-2240-01	SPARK GAP (PART OF CRT SOCKET ASSY)	
E202	52-2240-01	SPARK GAP (PART OF CRT SOCKET ASSY)	
E203	52-2240-01	SPARK GAP (PART OF CRT SOCKET ASSY)	
E204	52-2240-01	SPARK GAP (PART OF CRT SOCKET ASSY)	
YX201	100-884	12" CRT	
	OR		
	100-884-02	12" CRT	

POWER SUPPLY

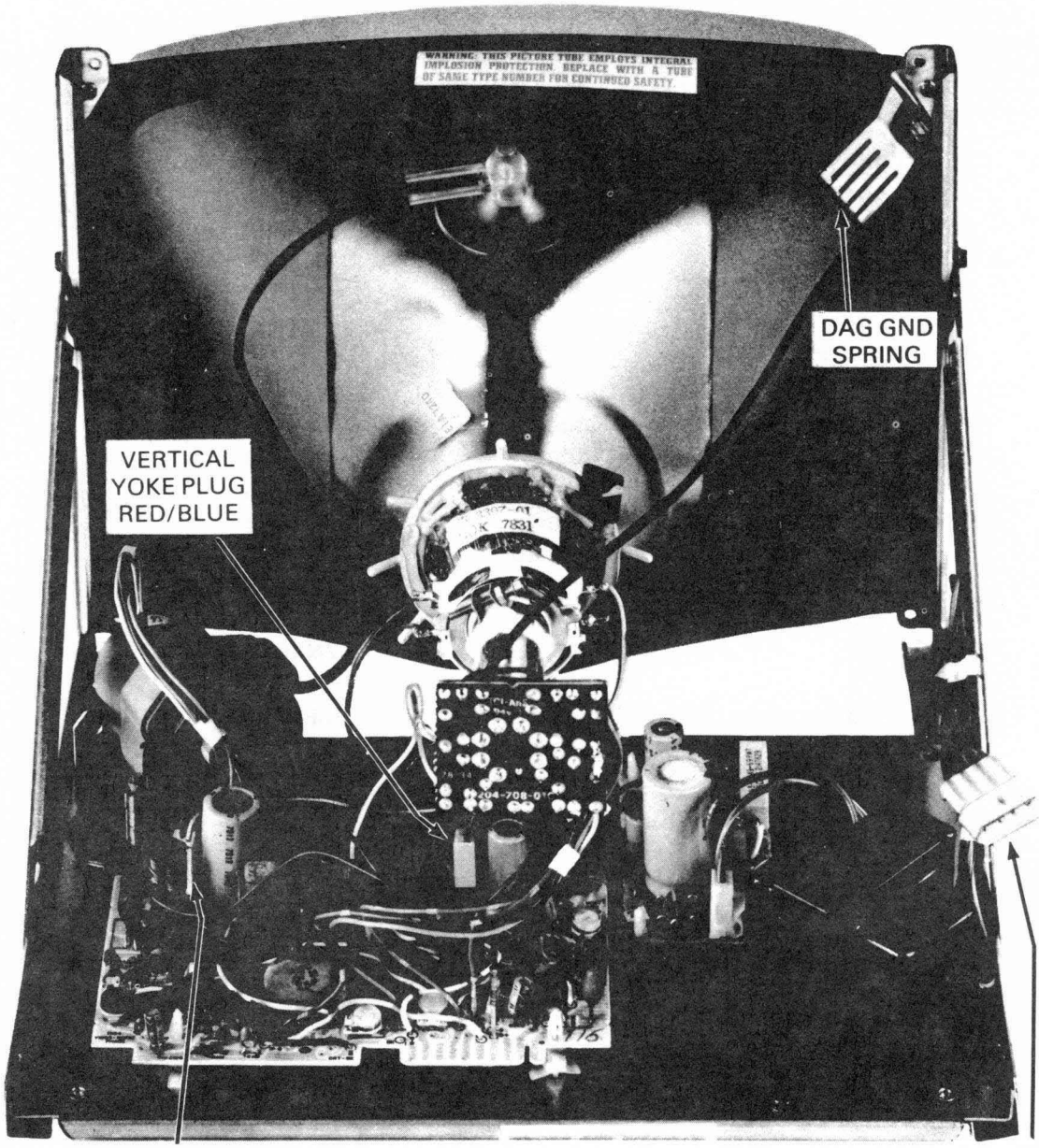


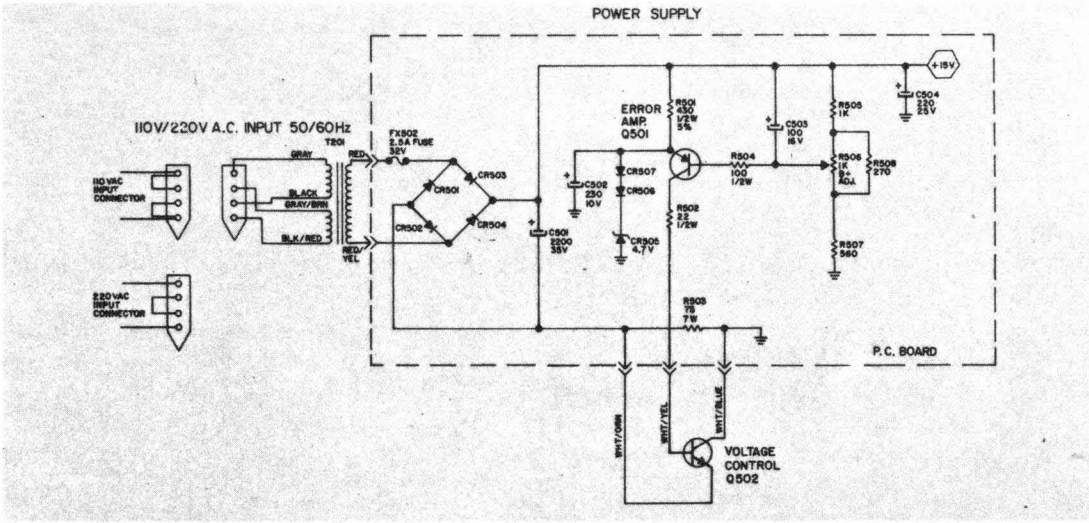


LEGEND

REF NO	PART NO	DESCRIPTION
C501	22-7154-13	2200 MFD CAP ELECT « 100% –10% 35V
C502	22-7152-08	100 μF CAP ELECT « 100% – 10% 25V
C503	22-7717-09	100 μF CAP ELECT 20% 16V
C504	22-7154-08	100μF CAP ELECT ±100% –10% 35V
R501	63-7769	430Ω RESISTOR 5% CARBON 1/2W
R502	63-7715	22Ω RESISTOR 10% CARB COMP 1/2W
R503	63-10449-69	75Ω RESISTOR WW 5% 7W
R504	63-7743	100Ω RESISTOR 10% CARB COMP 1/2W
RX505	**63-9921-72**	**1K Ω RESISTOR 5% FILM 1/4W**
RX506	**63-10651-01**	**CONTROL 1K Ω (B ± ADJ)**
RX507	63-9921-66	560 Ω RESISTOR 5% FILM 1/4W

REF NO	PART NO	DESCRIPTION
RX508	**63-9921-58**	**270 Ω RESISTOR 5% FILM 1/4W**
T201	95-3396	TRANSFORMER, POWER 110/220V
CR501	212-76	DIODE
CR502	212-76	DIODE
CR503	212-76	DIODE
CR504	212-76	DIODE
CR505	103-279-09A	DIODE ZENER 4.7V
CR506	103-142-01	DIODE
CR507	103-142-01	DIODE
Q501	121-1021	TRANSISTOR ERROR AMP
QX502	**121-9992-01**	**TRANSISTOR VOLTAGE CONTROL**
FX502	**136-120-06**	**FUSE 2.5 AMP 32V**


WARNING: THIS PICTURE TUBE EMPLOYS INTEGRAL IMPLOSION PROTECTION. REPLACE WITH A TUBE OF SAME TYPE NUMBER FOR CONTINUED SAFETY.
DAG GND SPRING
VERTICAL YOKE PLUG RED/BLUE
HORIZONTAL YOKE PLUG BLK/YEL
AC INPUT

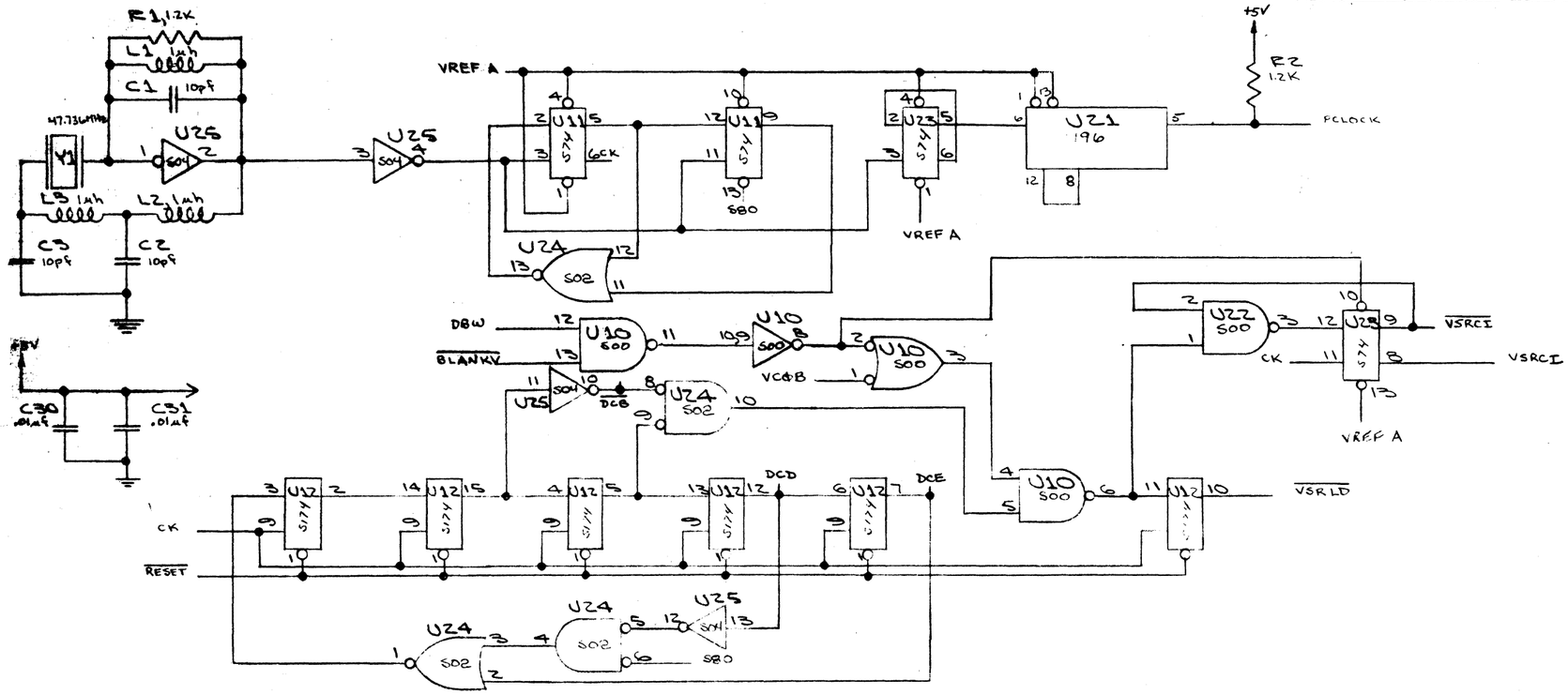

POWER SUPPLY
110W/220V A.C. INPUT 50/60Hz
110 VAC INPUT CONNECTOR
220 VAC INPUT CONNECTOR
T201
GRAY
BLACK
GRAY/BRN
BLK/RED
RED
RED/YEL
FX502 2.5A FUSE 32V
CR501
CR502
CR503
CR504
C501 2200 35V
C502 250 10V
CR507
CR506
CR505 4.7V
ERROR AMP Q501
R501 430 1/2W 5%
R502 22 1/2W
R503 75 7W
R504 100 1/2W
C503 100 16V
R505 1K
R506 1K 2% ADJ.
R508 270
R507 560
+15V
C504 220 25V
P.C. BOARD
WHT/BRN
WHT/YEL
WHT/BLUE
VOLTAGE CONTROL Q502

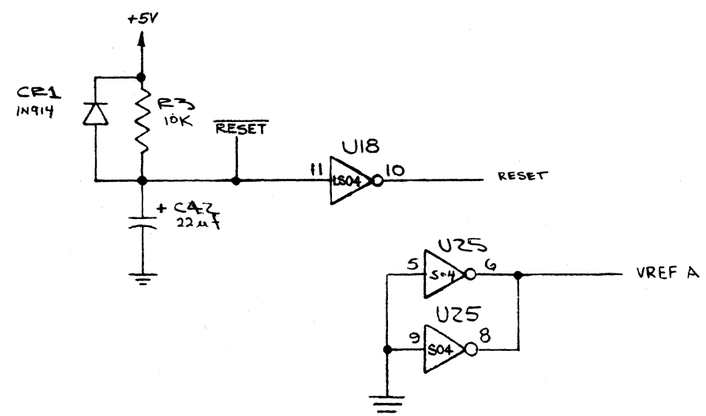
COMPONENT EQUIVALENTS

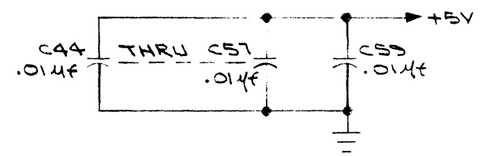
Zenith No.	Description	Equivalent
103-142-01	Diode	1N4148
103-261-02A	Diode	1N7000
103-261-04A	Diode	1N7000
103-263A	Diode	1N4007
103-280-02	Diode	(2)1N4007's in parallel
103-284	Diode	1N4820
103-295-02A	Diode	BA245
103-295-03A	Diode	1N4148
103-298-04	Diode	1N4822
103-298-05A	Diode	1N5398
212-76	Diode	1N4005
212-76-02	Diode	1N5061
121-699	Transistor	MPSA 70
121-819	Transistor	MPSA 05
121-895	Transistor	2N5210
121-972	Transistor	2N4048 or 2N3700
121-973	Transistor	MPSA 70
121-975	Transistor	MPSA 20
121-1034	Transistor	2N1893 or 2N2854
121-1039	Transistor	BU409 or 2SD724
121-1058	Transistor	2N1893 or 2N2854

8.0 SCHEMATIC DIAGRAMS

REVISION STATUS				
REV	ZONE	DESCRIPTION	DATE	APPRO.
EA	—	RELEASE TO PROD.	—	—
EB	—	REV PER 00117	1/29/80	KB







VISUAL TECHNOLOGY INC.
DUNDEE PARK RAILROAD AVE. ANDOVER, N.J. 07821

SCALE: NONE	APPROVED BY: K Barker 12/17/79
DATE: 12/12/79	

SCHEMATIC 7100

SHEET NUMBER: 1 OF 10

REVISION STATUS				
REV	ZONE	DESCRIPTION	DATE	APP'D
E.O.	–	SEE SHEET 1		

VISUAL TECHNOLOGY INC.
DUNDEE PARK, RAILROAD AVE., ANDOVER, MA. 01810

SCALE: NONE	APPROVED BY:	DRAWN BY:	
DATE: 12/12/79			

SCHEMATIC V100

SHEET NUMBER: 2 OF 10

REVISION HISTORY		
NO.	DATE	DESCRIPTION
		SEE SHEET 1

VSFLD
DBΦ
DB1
DB2
DB3
DB4
DB5
DB6
DB7
DBAK
U31 LS374
RB0
RB1
RB2
RB3
RB4
RB5
RB6
RB7
ATΦ
AT1
AT2
AT3
U38 LS257
U43 S4P2111A-2
U42 S4P2111A-2
U41 S4P2111A-2
GND PIN 8
U1 LS00
DCB
VCΦ
VC1
VC2
VC3
VC4
VC5
VC6
VC7
VDΦ
VD1
VD2
VD3
VD4
VD5
VD6
ACGR
U39 LS257
VREF A
VSRLD
U40 LS257
BLINK
U/L
RVID
BOLD
BOLD
LBLANK
VSRLD
+5V
C32 1μf
C41 22μf 16V
PIN 18 OF 2111
PIN 24 OF 2716
U29 2716
U28 2716 (OPT.)
U37 166
U43 S74
BLANKV
U48 S175
U46 LS00
VSRO
CK
VIDEOB
VSRCI
U26 LS00
+5V

VISUAL TECHNOLOGY, INC.
DUNDEE PARK, RAILROAD AVE., ANDOVER, MA. 01810

SCALE: NONE	APPROVED BY:	DRAWN BY:
DATE: 12/12/79		

SCHEMATIC V-100

SHEET NUMBER: 3 OF 10		DRAWING NUMBER: PS002-001

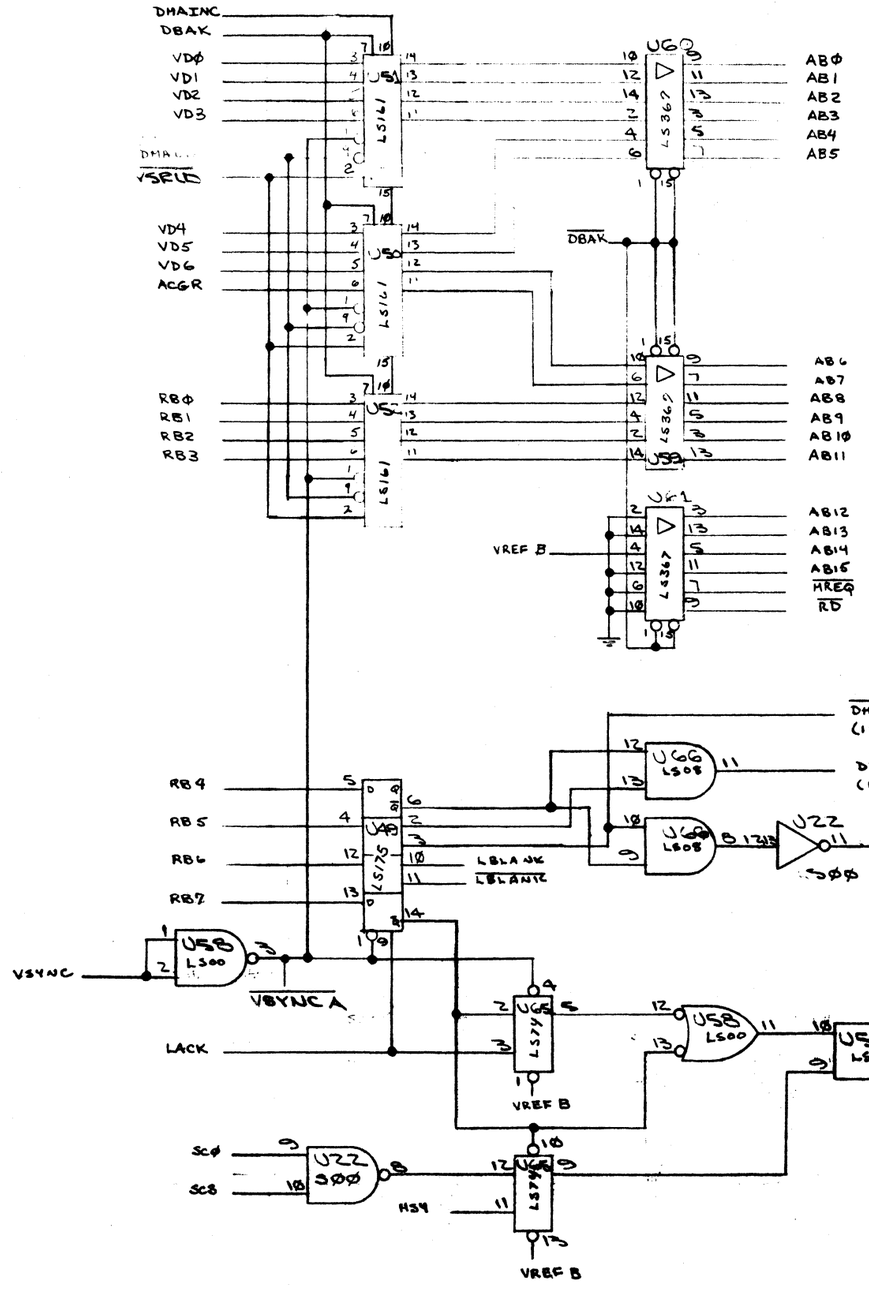
REVISION STATUS				
REV.	ZONE	DESCRIPTION	DATE	APPR.
	—	SEE SHEET 1		

SCB
BCRCUR
CURBF
U/L
VSRO
LBLANK
U56 S64
U57 S86
BLANKV
U36 S10
U48 S175 OW
CK
CSYNC
U37 26
R8 1.1K
R13 1.8K
R14 1.1K
+12V
R16 220Ω
R15 180Ω
Q1 PN3644
R18 75Ω
J9 COMP. VIDEO
U57 S86
U36 S10
U48 S175
+5V
RP2,2
R4 4.7K
VREF B
VIDENB
DCURF
PREV
RVID
U51 S86
U76 S00
BLINK
BTIME
U36 S10
U76 S00
BOLD
U57 S86
U51 S86
U37 26
R12 680Ω
R11 4.7K
R10 360Ω
R17 390Ω
R9 1KΩ
R25 2.2K
C8 1μf
C9 22μf 16V
Q2 PN3644
J1
DIR VID B
CR2 1N914
C5 .01μf
U107
DTAØ
DTA1
DTA2
DTA3
DTA4
R19 620Ω
R20 300Ω
R21 150Ω
R22 75Ω
R23 36Ω
R24 75Ω
+15V
C6 1μf
C7 22μf 35V
VSYNC
HSYNC
DIR VID GND.

VISUAL TECHNOLOGY INC.
DUNDEE PARK, RAILROAD AVE., ANDOVER, MA. 01810

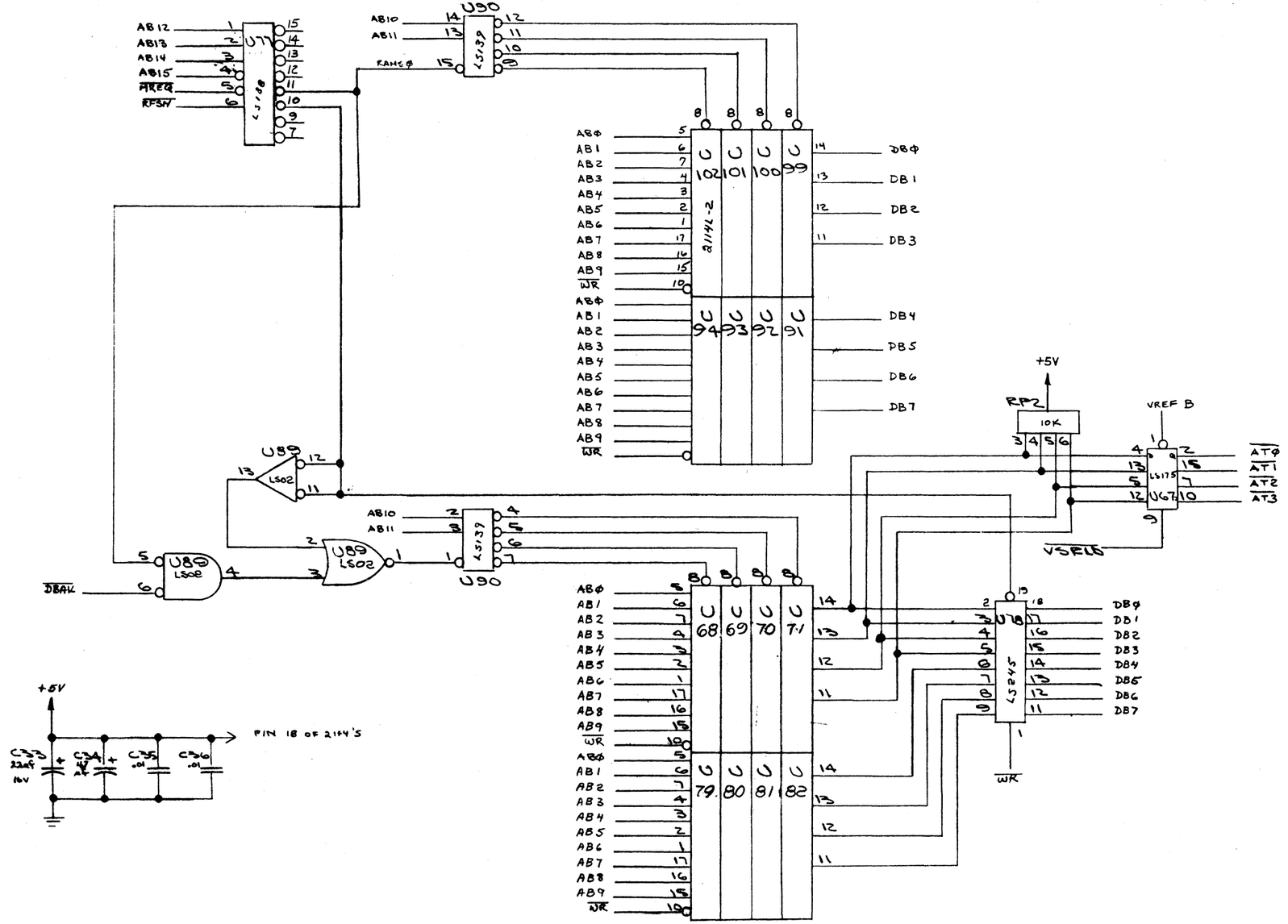
SCALE: NONE	APPROVED BY	DRAWING NO.
DATE	SCHEMATIC, V100	
SHEET NUMBER: 4 OF 10		

REVISION STATUS				
REV.	ZONE	DESCRIPTION	DATE	APPR.
	—	SEE SHEET 1		

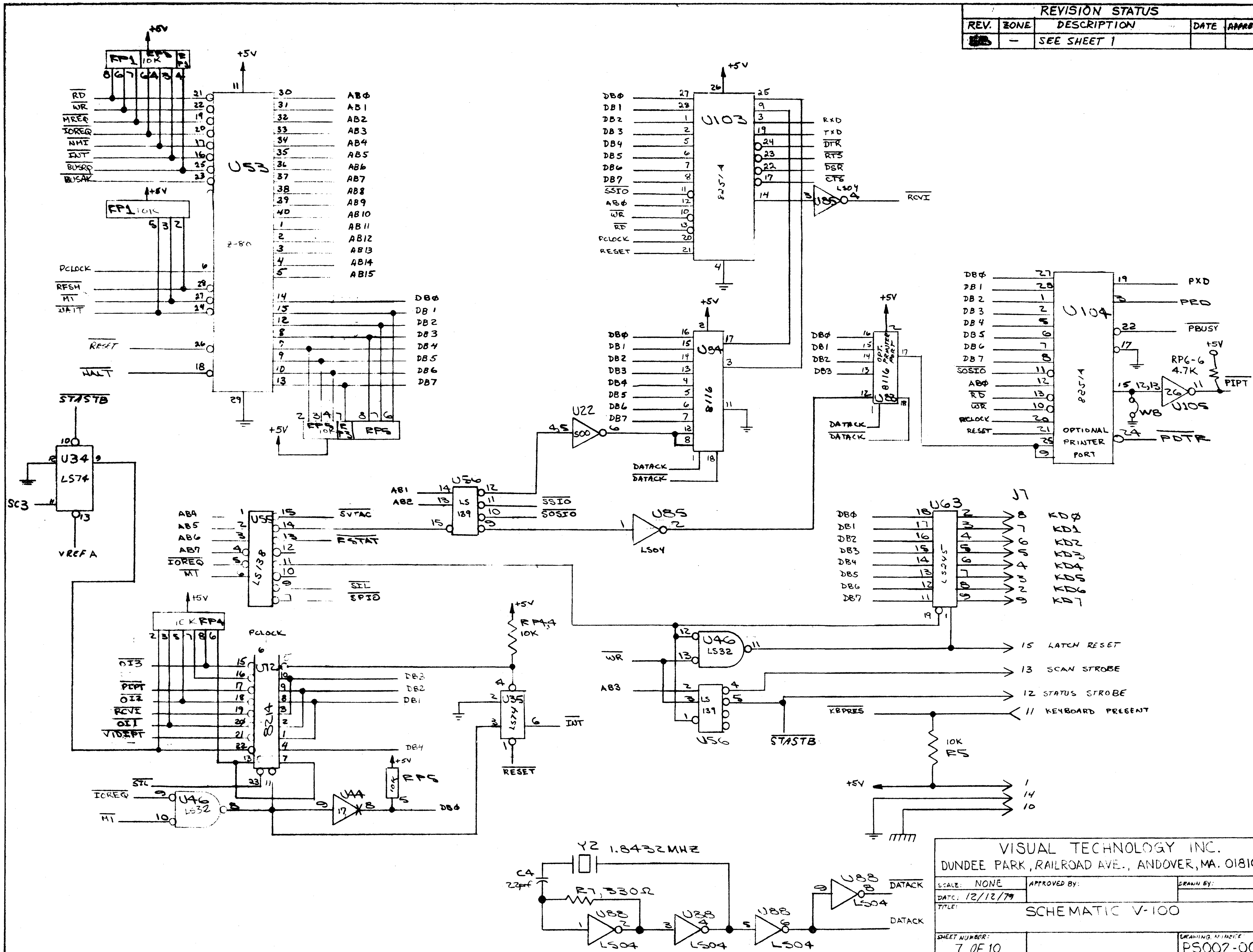


VISUAL TECHNOLOGY INC.	
DUNDEE PARK, RAILROAD AVE., ANDOVER, MA. 01810	
SCALE: NONE	APPROVED BY:
DATE: 12/12/79	
SCHEMATIC V-100	
SHEET NUMBER: 5 OF 10	

REVISION STATUS				
REV.	ZONE	DESCRIPTION	DATE	APPRV.
EB	–	SEE SHEET 1		

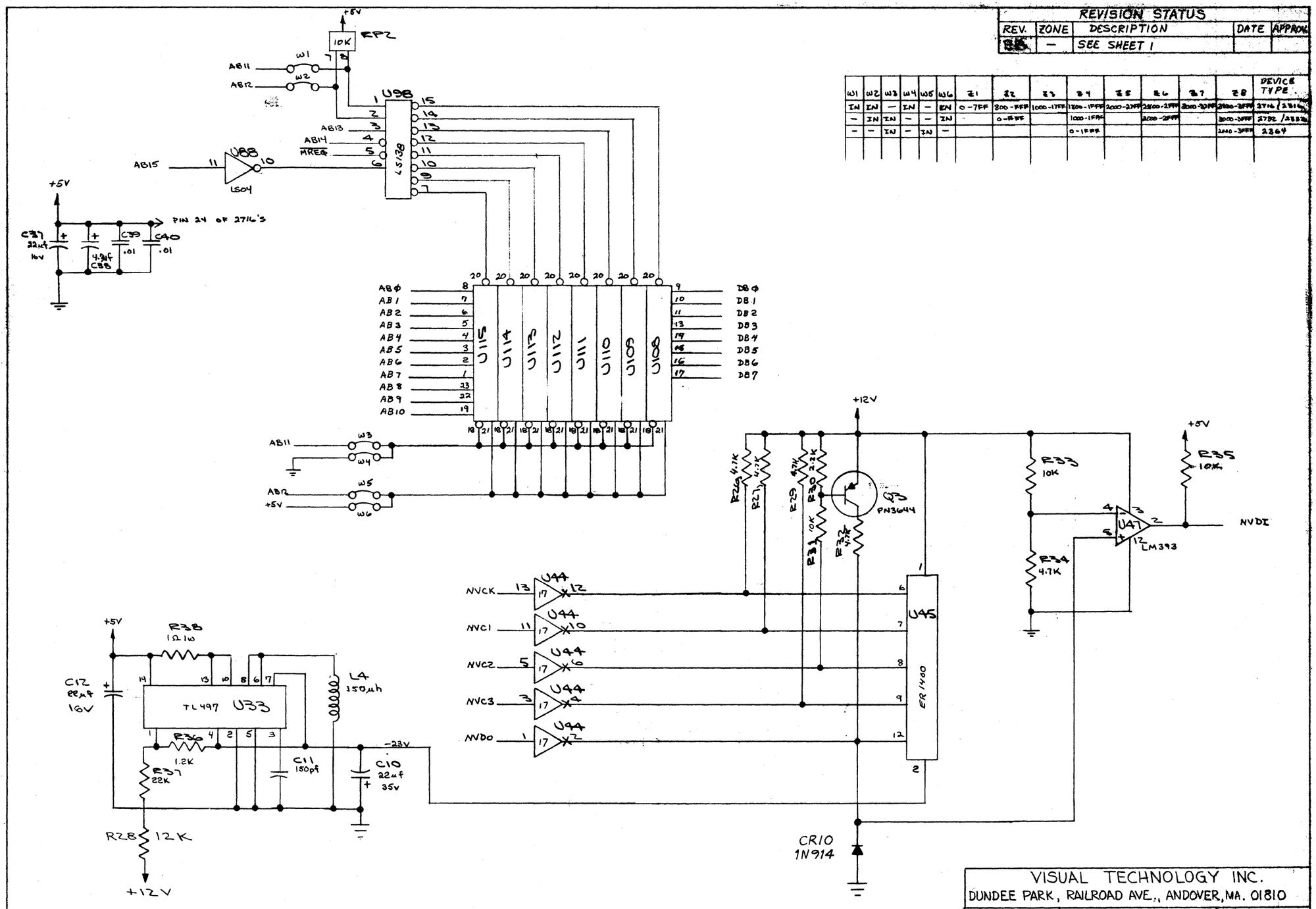


VISUAL TECHNOLOGY INC.		
DUNDEE PARK, RAILROAD AVE., ANDOVER, MA. 01810		
SCALE: NONE	APPROVED BY:	DRAWN BY:
DATE: 12/12/79		
SCHEMATIC V-100		
SHEET NUMBER: 6 OF 10		DRAWING NUMBER: PS002-001


REVISION STATUS
REV. ZONE DESCRIPTION DATE APPROV.
— SEE SHEET 1
U53
Z-80
RD
WR
MREQ
IOREQ
NMI
INT
BUSRQ
BUSAK
PCLOCK
RFSH
M1
WAIT
RESET
HALT
AB0 AB1 AB2 AB3 AB4 AB5 AB6 AB7 AB8 AB9 AB10 AB11 AB12 AB13 AB14 AB15
DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7
RP1 10K
RP3
+5V
STASTB
U34
LS74
SC3
VREF A
U103
8251A
RXD
TXD
DTR
RTS
DSR
CTS
U85
LS04
RCVI
SSIO
SOSIO
U84
8116
U22
S00
DATACK
U104
8251A
PXD
PRD
PBUSY
PIPT
PDTR
RP6-6
4.7K
U105
W8
OPTIONAL PRINTER PORT
U55
LS138
SVTAC
ESTAT
SIL
SPIO
U36
LS139
U63
LS245
J7
KD0 KD1 KD2 KD3 KD4 KD5 KD6 KD7
U46
LS32
15 LATCH RESET
13 SCAN STROBE
12 STATUS STROBE
11 KEYBOARD PRESENT
KBPRES
10K
R5
U56
LS139
U12
8214
OI3
PIPT
OI2
RCVI
OI1
VIDEPT
U35
LS74
INT
RESET
RP4-4
10K
RP5
U44
STL
Y2 1.8432MHZ
C4
22pf
R7, 330Ω
U88
LS04
DATACK
VISUAL TECHNOLOGY INC.
DUNDEE PARK, RAILROAD AVE., ANDOVER, MA. 01810
SCALE: NONE
APPROVED BY:
DRAWN BY:
DATE: 12/12/79
TITLE: SCHEMATIC V-100
SHEET NUMBER: 7 OF 10
DRAWING NUMBER PS002-001

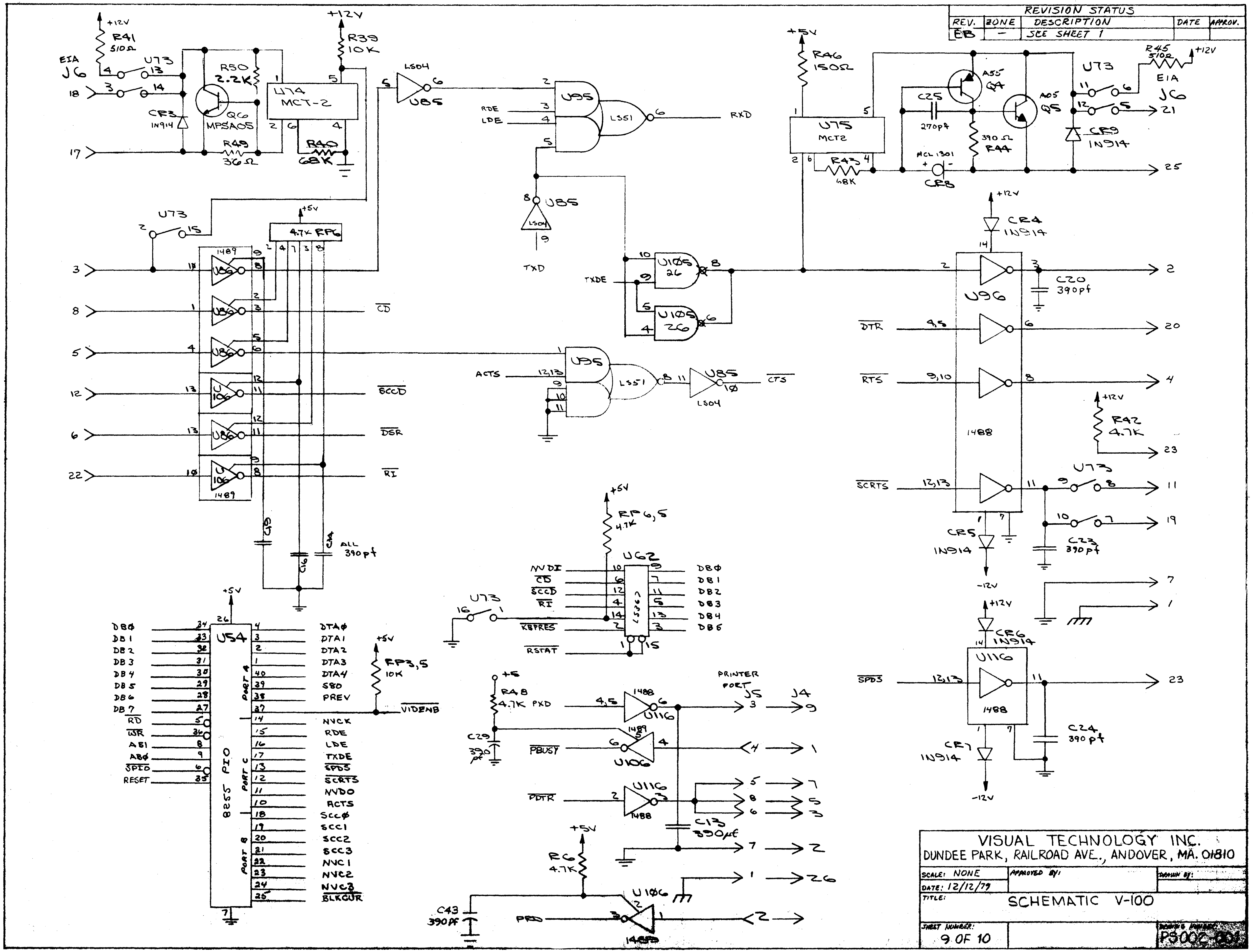
REVISION STATUS				
REV.	ZONE	DESCRIPTION	DATE	APPROVAL
[illegible]	—	SEE SHEET 1		

W1	W2	W3	W4	W5	W6	Z1	Z2	Z3	Z4	Z5	Z6	Z7	Z8	DEVICE TYPE
IN	IN	—	IN	—	EN	0-7FF	800-FFF	1000-17FF	1800-1FFF	2000-27FF	2800-2FFF	3000-37FF	3800-3FFF	2716 / 2316
—	IN	IN	—	IN	—		0-FFF		1000-1FFF		2000-2FFF		3000-3FFF	2732 / 2332
—	—	IN	—	IN	—				0-1FFF				2000-3FFF	2364



VISUAL TECHNOLOGY INC.
DUNDEE PARK, RAILROAD AVE., ANDOVER, MA. 01810

SCALE: NONE	APPROVED BY:	DRAWN BY
DATE: 12/12/79		
TITLE: SCHEMATIC V-100		
SHEET NUMBER: 8 OF 10		DRAWING NUMBER: PS002-001



REVISION STATUS				
REV.	ZONE	DESCRIPTION	DATE	APPROV.
EB	–	SEE SHEET 1		

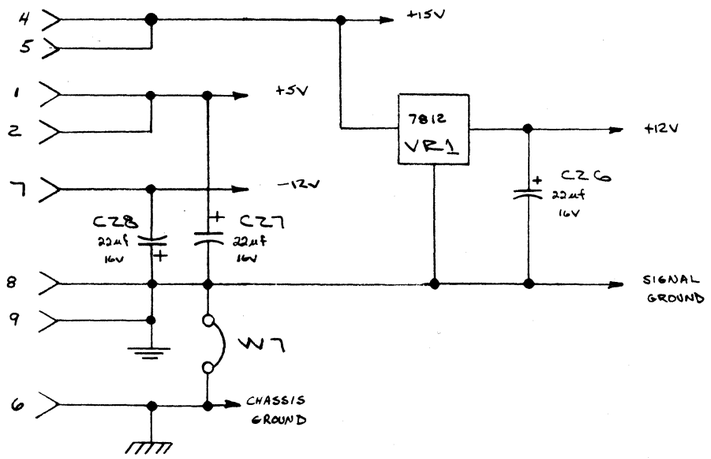
VISUAL TECHNOLOGY INC.
DUNDEE PARK, RAILROAD AVE., ANDOVER, MA. 01810

SCALE: NONE
APPROVED BY:
DRAWN BY:
DATE: 12/12/79
TITLE: SCHEMATIC V-100
SHEET NUMBER: 9 OF 10
DRAWING NUMBER: P300C-001

REVISION STATUS				
REV.	ZONE	DESCRIPTION	DATE	APPROV.
EB	—	SEE SHEET 1		

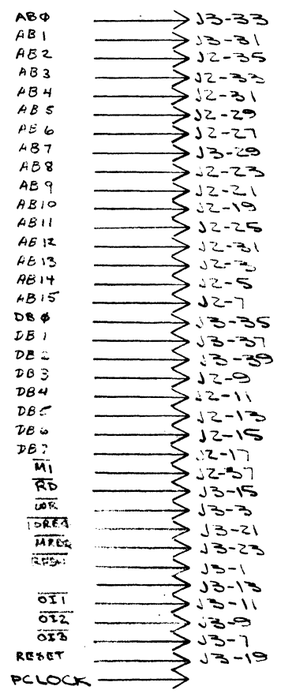
POWER CONNECTOR

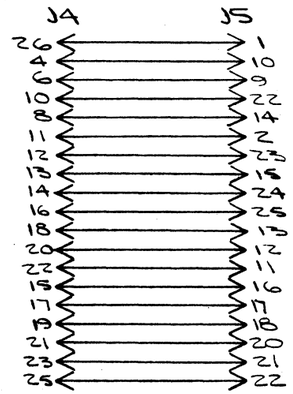
J8



OPTION CONNECTORS

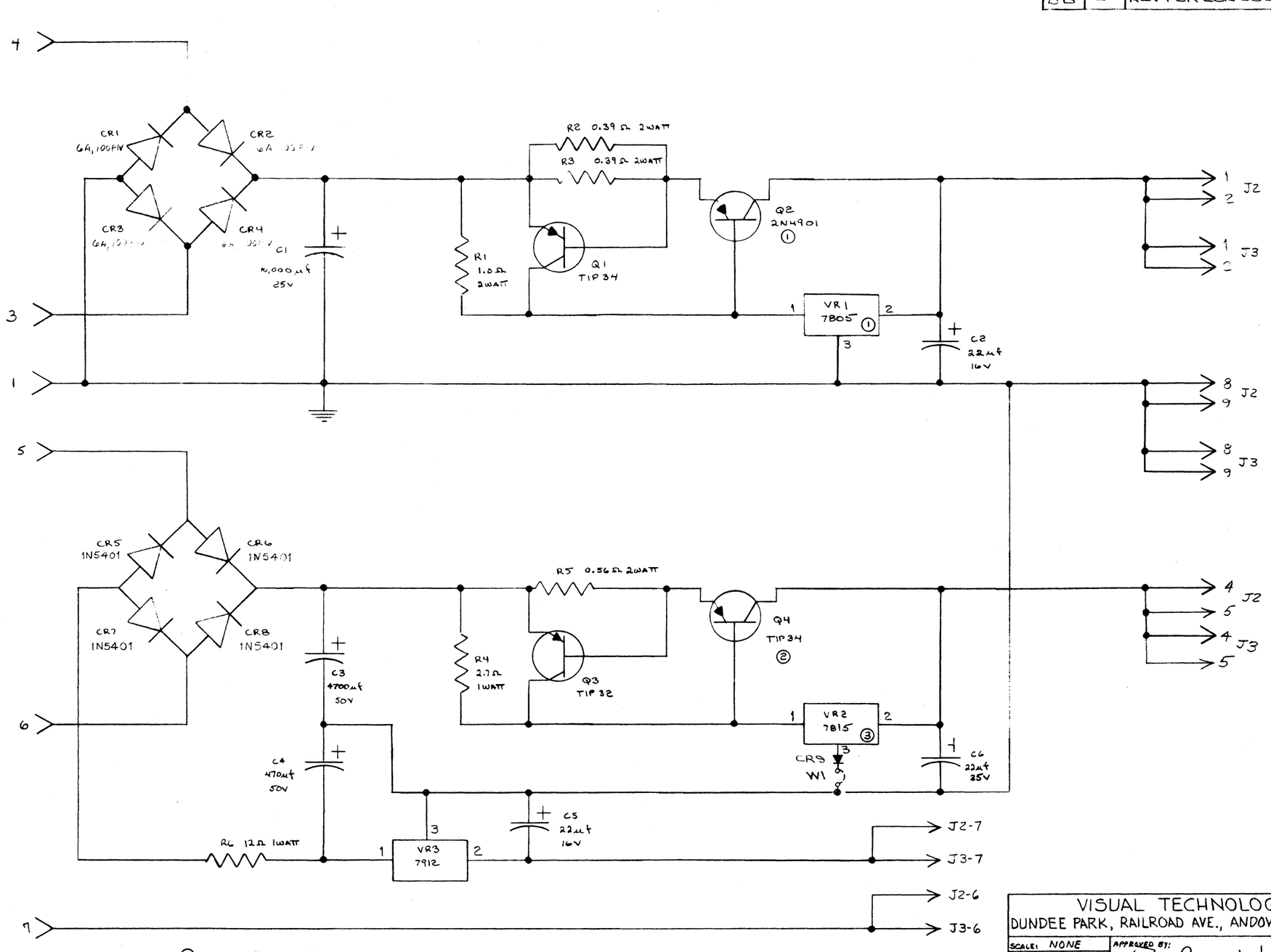
GROUND ALT PINS





VISUAL TECHNOLOGY INC. DUNDEE PARK, RAILROAD AVE., ANDOVER, MA. 01810		
SCALE: NONE	APPROVED BY:	DRAWN BY:
DATE: 12/12/79		
TITLE: SCHEMATIC V-100		
SHEET NUMBER: 10 OF 10		DRAWING NUMBER: PS002-001

REVISION STATUS				
REV.	ZONE	DESCRIPTION	DATE	APPROV.
B A	–	RELEAS TO PRODUCTION	–	–
B B	–	REV PER ECN 00065	6/10/80	KB



① USE SA004-001 HEATSINK

② USE 2 SA003-001 HEATSINKS

③ USE SA000-001 AND SA001-001 HEAT SINK

REV. BB

VISUAL TECHNOLOGY INC.
DUNDEE PARK, RAILROAD AVE., ANDOVER, MA. 01810

SCALE: NONE	APPROVED BY: K Bailey 12/17/79	DRAWN BY:
DATE: 12/12/79		
TITLE: SCHEMATIC V-100 (POWER SUPPLY)		
SHEET NUMBER: 1 OF 1		DRAWING NUMBER: PS003-001

REVISION STATUS				
REV	ZONE	DESCRIPTION	DATE	APPRO.
GA	—	RELEASE TO PROD.	5/29/80	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

R1, 1.2K
L1 1μh
C1 10pf
47.736MHz
Y1
U25 S04
L3 1μh
L2 1μh
C3 10pf
C2 10pf
+5V
C30 .01μf
C31 .01μf
VREF A
U25 S04
U11 LS74
6CK
U12 LS74
11
13 SBO
U24 S02
U23 LS74
U21 196
+5V
R2 1.2K
PCLOCK
VREF A
DBW
BLANKV
U10 S00
U25 S04
DCB
U24 S02
U10 S00
VCΦB
U10 S00
U22 S00
U22 LS74
CK
VSRCI
VSRCI
VREF A
U10 S00
VSRLD
U12 LS74
CK
RESET
DCD
DCE
U24 S02
U24 S02
U25 S04
SBO
C64 4.7μf
C44 4.7μf
C57 4.7μf
C72 4.7μf
C73 4.7μf
+5V
CR1 IN914
R3 10K
RESET
U18 LS04
RESET
+ C42 22μf
C45 .01μf THRU C56 .01μf
+5V
C59 .01μf
U25 S04
VREF A
U25 S04
+5V
C61 1μf
C65 1μf
+5V
C63 .01μf
C62 .01μf
C69 .01μf
C60 .01μf
C67 .01μf
C66 .01μf
C68 .01μf
C71 .01μf

VISUAL TECHNOLOGY INC.
DUNDEE PARK, RAILROAD AVE., ANDOVER, MA. 01810

SCALE: NONE	APPROVED BY: K Barlow 12/17/79	DRAWN BY:
DATE: 12/12/79		

SCHEMATIC V-100

SHEET NUMBER:		DRAWING NUMBER:
1 OF 10		PS002-001

REVISION STATUS				
REV	ZONE	DESCRIPTION	DATE	APPROV
GA	–	SEE SHEET 1		

VISUAL TECHNOLOGY INC. DUNDEE PARK, RAILROAD AVE., ANDOVER, MA. 01810			
SCALE: NONE	APPROVED BY:		DRAWN BY:
DATE: 12/12/79			
SCHEMATIC V-100			
SHEET NUMBER: 2 OF 10			DRAWING NUMBER: PS002-001

REVISION STATUS				
REV	ZONE	DESCRIPTION	DATE	APPROV.
GA	—	SEE SHEET 1		

VSRLD
DBØ
DB1
DB2
DB3
DB4
DB5
DB6
DB7
DBAK
U31 LS374
RBØ
RB1
RB2
RB3
RB4
RB5
RB6
RB7
ATØ
AT1
AT2
AT3
U38 LS244
DBAK
U43 S4P2111A-2 GND PIN 8
U42 S4P2111A-2 GND PIN 8
U41 S4P2111A-2 GND PIN 8 *
DBAK
DCB
U1 LS00
DBAK
VCØ
VC1
VC2
VC3
VC4
VC5
VC6
VC7
VSRLD
VDØ
VD1
VD2
VD3
VD4
VD5
VD6
ACGR
U39 LS273
VREF A
U39 *
BLINK
ULE
RVID
BOLD
BOLD
LBLANK
VSRLD
U36A S175
VSRLD
U/L
VREFA
+5V
C32 1µf
C41 22µf 16v
PIN 18 OF 2111
PIN 24 OF 2716
VSØ
VS1
VS2
VS3
VDØ
VD1
VD2
VD3
VD4
VD5
VD6
U29 2716
U28 2716 (OPT.)
ACGR
U26 LS00
+5V
VREF A
U36 S74
VSRLD
REXT
U37 166
VSRLD
VSRCI
CK
U87 S175
CK
VSROD
U87 S175
CK
VSRO

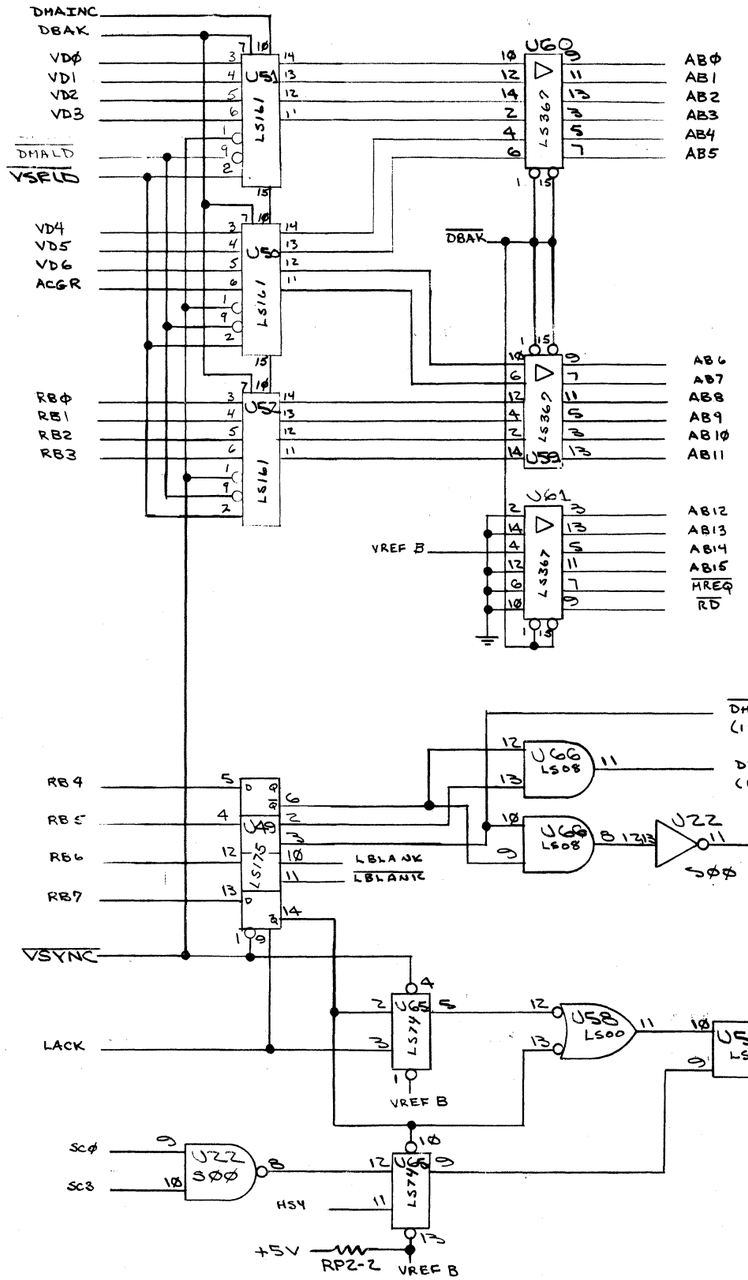
VISUAL TECHNOLOGY INC.		
DUNDEE PARK, RAILROAD AVE., ANDOVER, MA. 01810		
SCALE: NONE	APPROVED BY:	DRAWN BY:
DATE: 12/12/79		
SCHEMATIC V-100		
SHEET NUMBER: 3 OF 10		DRAWING NUMBER: PS002-001

REVISION STATUS				
REV.	ZONE	DESCRIPTION	DATE	APPROV.
GA	–	SEE SHEET 1		

SC8
BLKCUR
CURF
U/L
VSRO
LBLANK
VSROD
U64 S64
U76 S86
BLANKV
U57 S10
U87 S175 (U4)
CSYN
U97 26
R8 1.1K
R13 1.8K
R14 1.1K
+12V
R16 220Ω
R15 180Ω
Q1 PN3644
R18 75Ω
J9 COMP. VIDEO
U36A S175
VSRLD
U57 S10
U87 S175 (U4)
+5V
R4 4.7K
VIDENB
DCVR
RVID
U36 LS86
PREV
U36 LS86
U48 LS00
BLINK
BTIME
U48 LS00
U48 LS00
BOLD
U48 LS00
U36A S175
BOLD
U36 LS86
U36A S175
VSRLD
U36 LS86
VREFA
VIDENB
+12V
R17 270Ω
R9 68Ω
R25 22K
C8 1mf
C9 22mf 16V
R12 680Ω
R11 1.1K
R10 360Ω
Q2 PN3644
J1
DIR VID 2
CR2 1N914
C5 .01mf
DTAØ
DTA1
DTA2
DTA3
DTA4
U107
R19 680Ω
R20 300Ω
R21 150Ω
R22 75Ω
R23 36Ω
R24 75Ω
7 DIR VID GND.
+15V
C6 1mf
C7 22mf 35V
5
1
74LS04
VSYNC
HSYNC
3
4

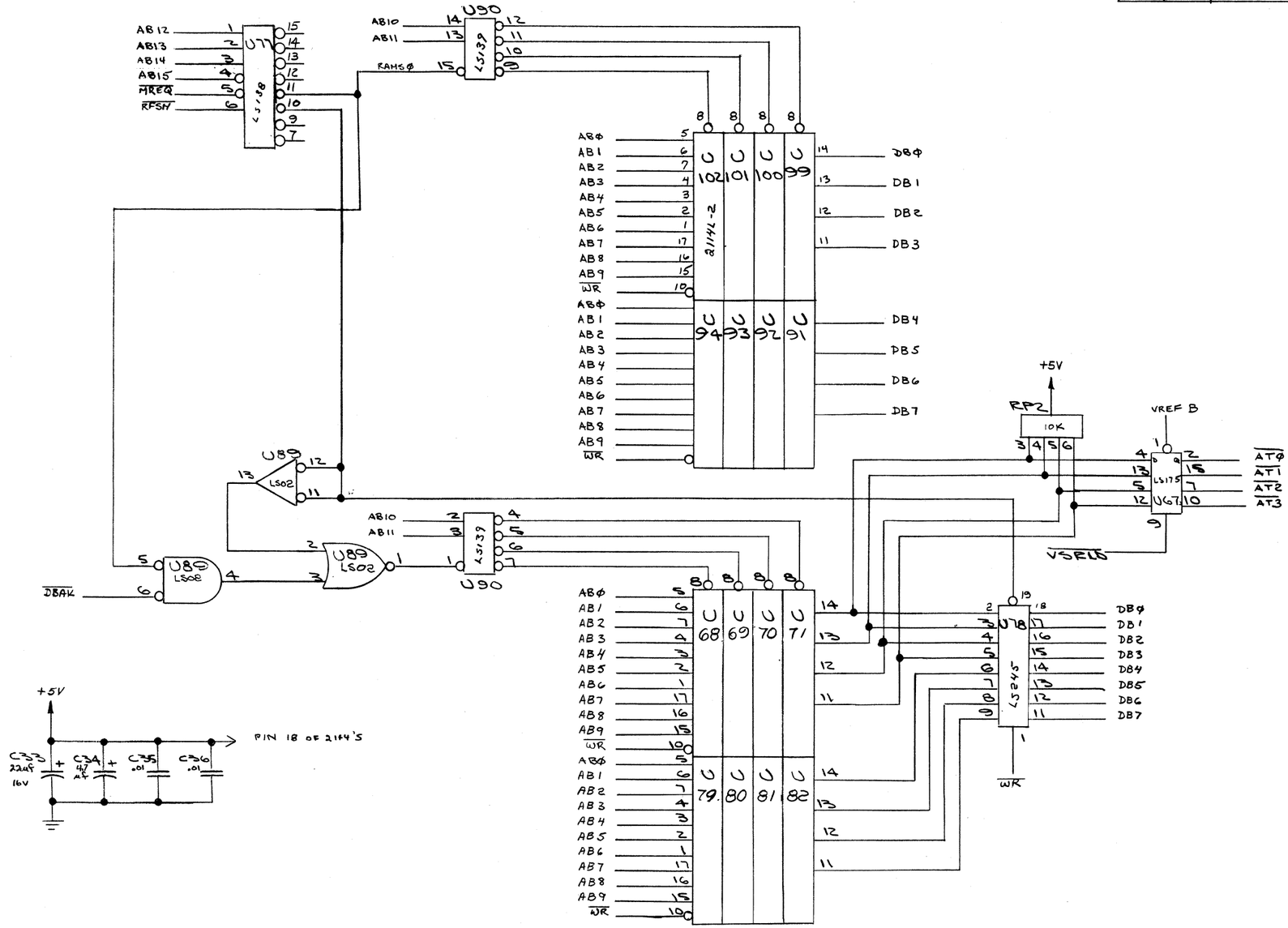
VISUAL TECHNOLOGY INC. DUNDEE PARK, RAILROAD AVE., ANDOVER, MA. 01810		
SCALE: NONE	APPROVED BY:	DRAWN BY:
DATE		
SCHEMATIC V-100		
SHEET NUMBER: 4 OF 10		DRAWING NUMBER: PS002-001

REVISION STATUS				
REV.	ZONE	DESCRIPTION	DATE	APPROV.
GA	—	SEE SHEET1		



VISUAL TECHNOLOGY INC. DUNDEE PARK, RAILROAD AVE., ANDOVER, MA. 01810		
SCALE: NONE	APPROVED BY:	DRAWN BY:
DATE: 12/12/79		
SCHEMATIC V-100		
SHEET NUMBER: 5 OF 10		DRAWING NUMBER: PS002-001

REVISION STATUS				
REV.	ZONE	DESCRIPTION	DATE	APPROV.
GA	–	SEE SHEET 1		



VISUAL TECHNOLOGY INC.		
DUNDEE PARK, RAILROAD AVE., ANDOVER, MA. 01810		
SCALE: NONE	APPROVED BY:	DRAWN BY:
DATE: 12/12/79		
SCHEMATIC V-100		
SHEET NUMBER: 6 OF 10		DRAWING NUMBER: PS002-001

REVISION STATUS				
REV.	ZONE	DESCRIPTION	DATE	APPROVED
A	—	SEE SHEET 1		

VISUAL TECHNOLOGY INC.
DUNDEE PARK, RAILROAD AVE., ANDOVER, MA. 01810

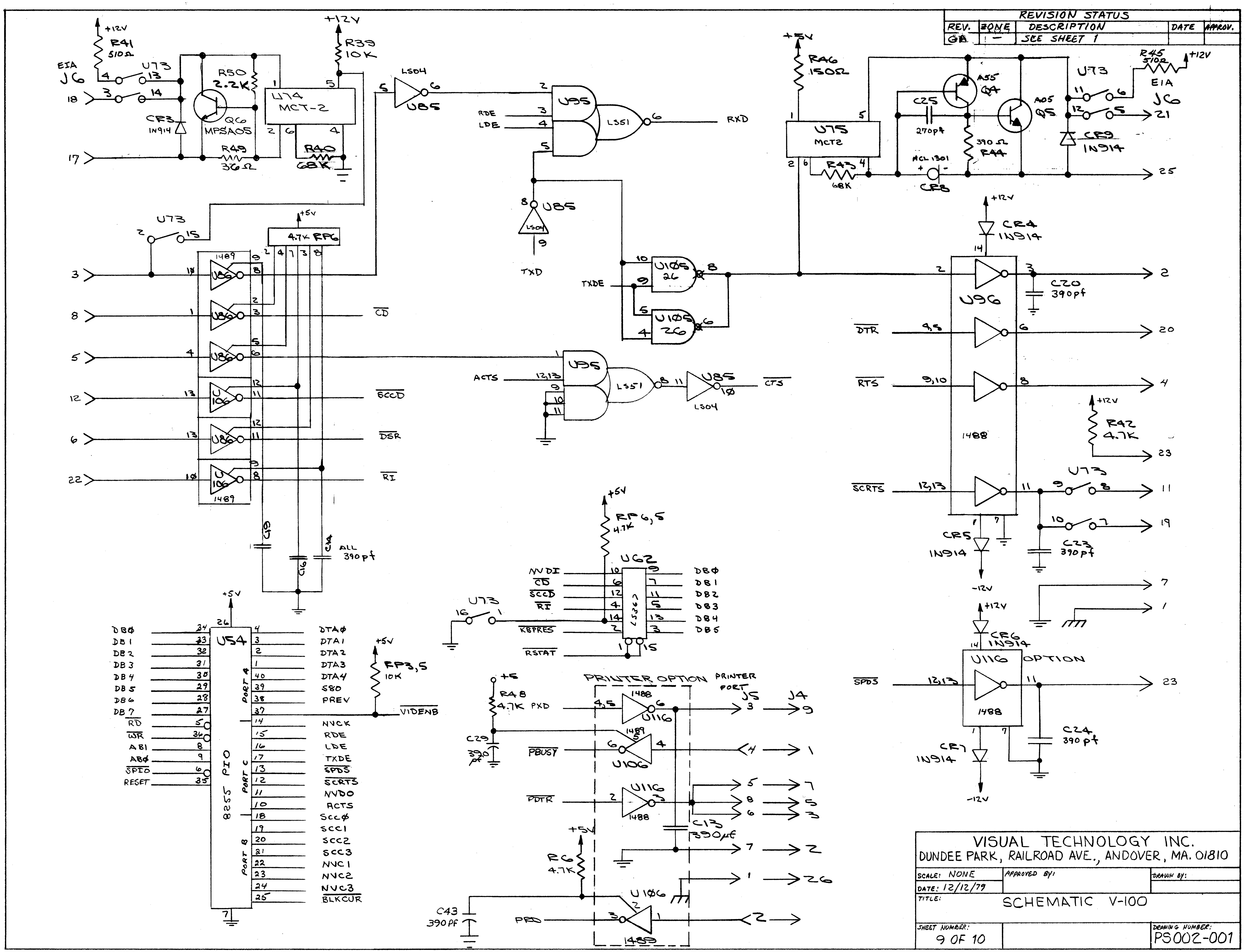
SCALE: NONE	APPROVED BY:	DRAWN BY:	
DATE: 12/12/79			
TITLE: SCHEMATIC V-100			
SHEET NUMBER: 7 OF 10		DRAWING NUMBER: PS002-001	

REVISION STATUS				
REV.	ZONE	DESCRIPTION	DATE	APPROV.
GA	—	SEE SHEET 1		

W1	W2	W3	W4	W5	W6	Z1	Z2	Z3	Z4	Z5	Z6	Z7	Z8	DEVICE TYPE
IN	IN	—	IN	—	EN	0-7FF	800-FFF	1000-17FF	1800-1FFF	2000-27FF	2800-2FFF	3000-37FF	3800-3FFF	2716/2816
—	IN	IN	—	—	IN		0-FFF		1000-1FFF		2000-2FFF		3000-3FFF	2732/2332
—	—	IN	—	IN	—				0-1FFF				2000-3FFF	2364

+5V
EP2
10K
W1
W2
AB11
AB12
AB13
AB14
MREQ
AB15
U98
LS138
U88
LS04
+5V
C37 22uf 16V
C39 .01
C38 4.99K
C40 .01
PIN 24 OF 2716'S
AB0
AB1
AB2
AB3
AB4
AB5
AB6
AB7
AB8
AB9
AB10
U115
U114
U113
U112
U111
U110
U109
U108
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
W3
W4
W5
W6
AB11
AB12
+5V
+12V
R29 4.7K
R27 4.7K
R29 4.7K
R30 4.7K
R31 10K
R32 4.7K
Q3 PN3644
R33 10K
R35 10K
U47 LM393
R34 4.7K
NVDI
NVCK
NVC1
NVC2
NVC3
NVDO
U44
U45 ER1400
CR10 1N914
+5V
R38 1Ω 2W
C12 22uF 16V
U33 TL497
L4 150μh
R36 1.2K
R37 22K
C11 150pf
C10 22uf 35v
-23V
R28 12K
+12V

VISUAL TECHNOLOGY INC.	
DUNDEE PARK, RAILROAD AVE., ANDOVER, MA. 01810	
SCALE: NONE	APPROVED BY:
DATE: 12/12/79	DRAWN BY
TITLE: SCHEMATIC V-100	
SHEET NUMBER: 8 OF 10	DRAWING NUMBER: P5002-001



REV.	ZONE	DESCRIPTION	DATE	APPROV.
GB	—	SEE SHEET 1		

VISUAL TECHNOLOGY INC.
DUNDEE PARK, RAILROAD AVE., ANDOVER, MA. 01810

SCALE: NONE
APPROVED BY:
DRAWN BY:
DATE: 12/12/79
TITLE: SCHEMATIC V-100
SHEET NUMBER: 9 OF 10
DRAWING NUMBER: PS002-001

REVISION STATUS				
REV.	ZONE	DESCRIPTION	DATE	APPROV.
G A	—	SEE SHEET 1		

POWER CONNECTOR

J8

4
5
1
2
7
8
9
6

+15V
+5V
-12V
7812 VR1
+12V
C26 22uf 16V
C28 22uf 16V
C27 22uf 16V
SIGNAL GROUND
W7 *OPTIONAL
CHASSIS GROUND

OPTION CONNECTORS GROUND ALT PINS

AB0	J3-33
AB1	J3-31
AB2	J2-35
AB3	J2-33
AB4	J2-31
AB5	J2-29
AB6	J2-27
AB7	J3-29
AB8	J2-23
AB9	J2-21
AB10	J2-19
AB11	J2-25
AB12	J2-31
AB13	J2-3
AB14	J2-5
AB15	J2-7
DB0	J3-35
DB1	J3-37
DB2	J3-39
DB3	J2-9
DB4	J2-11
DB5	J2-13
DB6	J2-15
DB7	J2-17
$\overline{M1}$	J2-37
$\overline{RD}$	J3-15
$\overline{WR}$	J3-3
$\overline{IOREQ}$	J3-21
$\overline{MREQ}$	J3-23
$\overline{RFSH}$	J3-1
$\overline{OI1}$	J3-11
$\overline{OI2}$	J3-9
$\overline{OI3}$	J3-7
RESET	J3-19
PCLOCK	

J4 J5

26	1
4	10
6	9
10	22
8	14
11	2
12	23
13	15
14	24
16	25
18	13
20	12
22	11
15	16
17	17
19	18
21	20
23	21
25	22

VISUAL TECHNOLOGY INC.
DUNDEE PARK, RAILROAD AVE., ANDOVER, MA. 01810

SCALE: NONE	APPROVED BY:	DRAWN BY:
DATE: 12/12/79		
TITLE: SCHEMATIC V-100		
SHEET NUMBER: 10 OF 10		DRAWING NUMBER: PS002-001

REVISION STATUS				
REV.	ZONE	DESCRIPTION	DATE	APPROVED
AA		REL. PER 00105	7/7/80	KB

J1

4

3

1

5

6

7

CR1 6A, 100PIV

CR2 6A, 100PIV

CR3 6A, 100PIV

CR4 6A, 100PIV

C1 10,000mf 25V

R2 .36Ω, 2WATT

Q6 TIP34

Q5 2N4901 ①

R3 .36Ω, 2 WATT

R1 1.8Ω 2 WATT

Q1 TIP34

Q2 2N4901 ①

VR1 7805 ①

C2 22mf 16V

CR5 1N5401

CR6 1N5401

CR7 1N5401

CR8 1N5401

C3 4700mf 50V

C4 470mf 50V

R5 0.56Ω 2WATT

R4 2.7Ω 2WATT

Q3 TIP 32

Q4 TIP34 ②

VR2 7815 ③

CR9 1N914

C6 22mf 25V

VR3 7912

C5 22mf 16V

R7 1K 1/4W

R8 1K, 1/4W

RC 100Ω, 2W.

J2 1 2

J3 1 2

J2 8 9

J3 8 9

J2 4 5

J3 4 5

J2-7

J3-7

J2-6

J3-6

① USE SA004-001 HEATSINK

② USE 2 SA003-001 HEATSINKS

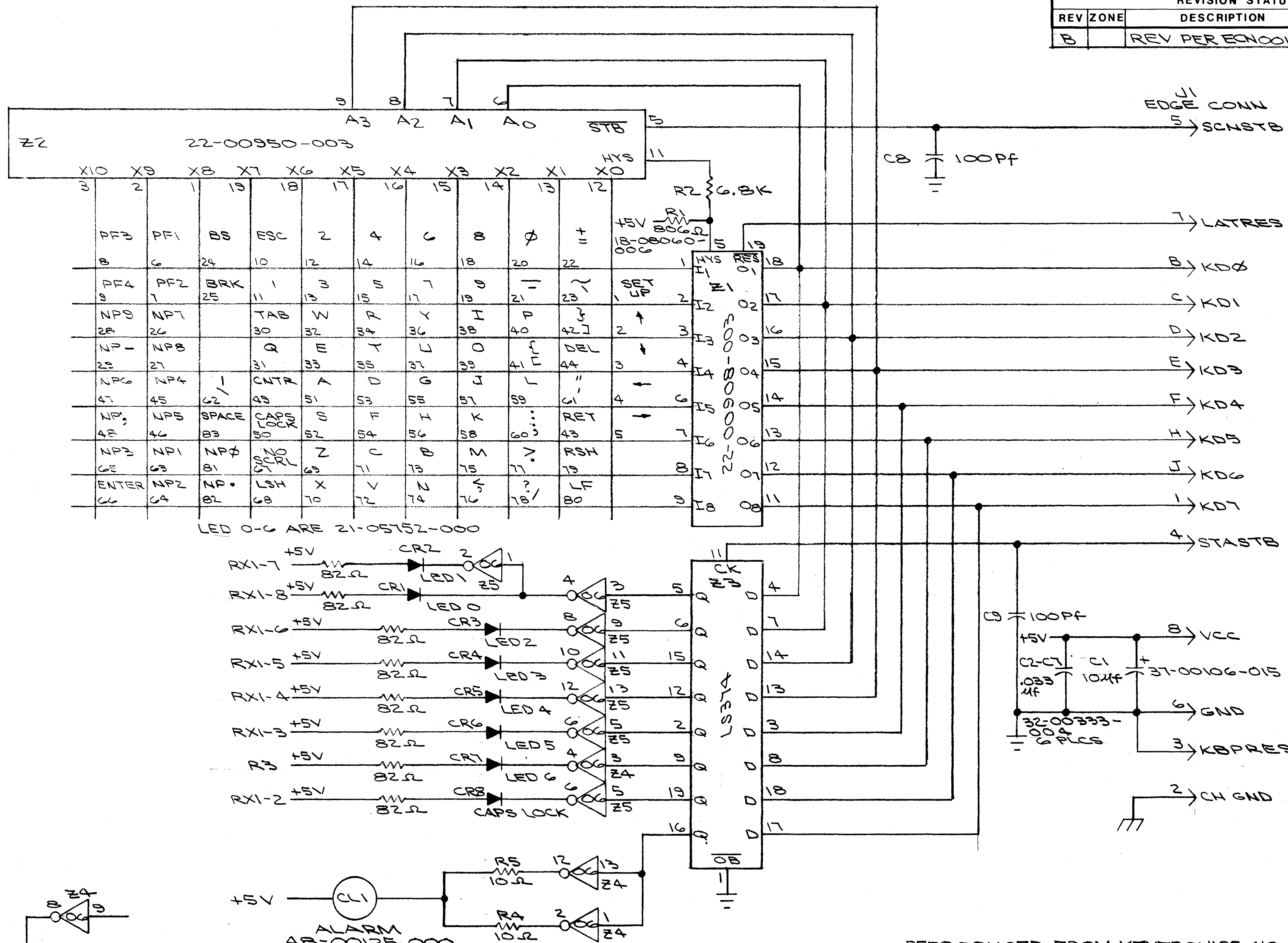
③ USE SA000-001 AND SA004-001 HEAT SINK

REV. AA

VISUAL TECHNOLOGY INC.
DUNDEE PARK, RAILROAD AVE., ANDOVER, MA. 01810

SCALE: NONE	APPROVED BY: CAD 5/15/80 KB 6/18/80	DRAWN BY: W. F. Barnes
DATE: 5/14/80		
TITLE: SCHEMATIC V-100 (POWER SUPPLY)		
SHEET NUMBER: 1 OF 1		DRAWING NUMBER: PS005-001

REVISION STATUS				
REV	ZONE	DESCRIPTION	DATE	APPR
B		REV PER ECN00128		



REPRODUCED FROM KEYTRONICS NO. 35-02131

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Material:	INCHES/MM .X = / .XX = / .XXX = /	CHECKED	9/5/80	TITLE: SCHEMATIC KEYBOARD	SIZE: C SCALE: NONE
Finish:	FRACT. = ANGLE =	APPR.	9/8/80		UNIT NO. KS002-001
		APPR.		Model No. V-100	Next Assy. KB002-001
		SIGNATURE	DATE		SHEET 1 OF 1

VISUAL FORM VF001-013

REVISION STATUS				
REV	ZONE	DESCRIPTION	DATE	APPR
A		RELEASED		

Z5 22-00950-003

X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0
3	2	1	19	18	17	16	15	14	13	12
PRINT 85	PF3 8	PF1 6	BS 24	ESC 10	2 12	4 14	6 16	8 18	Ø 20	= + 22
XMIT 86	PF4 9	PF2 7	BRK 25	! 1 11	3 13	5 15	7 17	9 19	— 21	~ ^ 23
PF9 87	NP9 28	NP7 26	HOME 95	TAB 30	W 32	R 34	Y 36	I 38	P 40	{ [42
PF10 88	NP- 29	NP8 27	PF5 91	Q 31	E 33	T 35	U 37	O 39	}] 41	DEL 44
PF11 89	NP0 47	NP4 45	| 62	CNTR 93	A 51	D 53	G 55	J 57	L 59	" ' 61
PF12 90	NP, 48	NP5 46	SPACE 83	CAPS LOCK 50	S 52	F 54	H 56	K 58	: ; 60	RET 43
PF6 92	NP3 65	NP1 63	NP0 81	CTRL 49	Z 69	C 71	B 73	M 75	> . 77	RSH 79
PF7 93	ENTER 66	NP2 64	NP. 82	LSH 68	X 70	V 72	N 74	< , 76	? / 78	LF 80

PF8 94 8 — FUNC 84 9

LED 0-6 ARE 21-05752-000

A3 A2 A1 A0 STB HYS

R2 6.8K

+5V R1 806Ω 18-00060-006

C8 100pf

J1 EDGE CONN

5 SCNSTB
7 LATRES
B KD0
C KD1
D KD2
E KD3
F KD4
H KD5
J KD6
1 KD7
4 STASTB
8 VCC
6 GND
3 KBPRES
2 CH GND

Z1 500-80600-22

Z2 LS374

Z3 LS04

Z4 LS04

RX1-7 +5V 82Ω CR2 LED1
RX1-8 +5V 82Ω CR1 LED0
RX1-6 +5V 82Ω CR3 LED2
RX1-5 +5V 82Ω CR4 LED3
RX1-4 +5V 82Ω CR5 LED4
RX1-3 +5V 82Ω CR6 LED5
R3 +5V 82Ω CR7 LED6
RX1-2 +5V 82Ω CR8 CAPS LOCK

CR8 IN4148

+5V C11 ALARM 48-00125-000

R5 10Ω
R4 10Ω

C9 100pf
C2-C7 .033 µf
C1 10µf
32-00333-004 6 PLCS
31-00106-015

UNUSED GATES

REPRODUCED FROM KEYTRONICS NO. 35-02220

TOLERANCES: Except as noted
INCHES/MM
.X = /
.XX = /
.XXX = /
FRACT. =
ANGLE =

Material:
Finish:

DRAWN	W. L. Barnes	9/5/80
CHECKED	D. Babcock	9/5/80
APPR.	D. Babcock	9/5/80
APPR.		
SIGNATURE		DATE

VISUAL
Visual Technology Incorporated
Railroad Avenue, Dundee Park, Andover, Ma. 01810

REV. A

TITLE: SCHEMATIC KEYBOARD
SIZE C | SCALE: NONE
UNIT NO. KS003-001
Model No. V-400 | Next Assy. KB003-001 | SHEET 1 OF 1

VISUAL FORM VF001-013

MM-100-001-0A
September, 1980