VISUAL 200

VIDEO DISPLAY TERMINAL
MAINTENANCE MANUAL

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VISUAL TECHNOLOGY INCORPORATED, RAILROAD AVENUE, DUNDEE PARK, ANDOVER, MA 01810

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SAFETY WARNING

Hazardous voltages 115, 220 VAC and 15 KV DC are present when the terminal is on, and may remain after power is removed. Use caution when working on internal circuits, and do not work alone.

When handling the cathode ray tube caution is required as the internal phosphor is toxic. Safety goggles and gloves must be used whenever the CRT tube is handled. Should the tube break, skin or eyes exposed to the phosphor, rinse the affected area with cold water and consult a physician.

This terminal is supplied with a cord set which includes a safety ground. Do not use this terminal with an ungrounded outlet, missing ground pin, or use any adaptor which will defeat the safety ground.

Insure that power is turned off before connecting or disconnecting the keyboard cable.

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1. ARCHITECTURE

The Visual 200 is a microprocessor (Z80) based terminal composed of SSI and MSI logic elements. The communications receiver and transmitter (USART) and the video refresh are interrupt driven. The video refresh utilizes a DMA cycle in order to minimize processor overhead.

Program memory consists of PROM or ROM in two 24 pin sockets for a total of up to 12288 Bytes.

Data memory consists of 4096 Bytes of dynamic RAM with 1920 words used as display memory (80 characters per line and 24 lines). Additional RAM of 128 Bytes is used as a DMA buffer.

All timing is derived from a single crystal controlled oscillator operating at 33.48 MHz. Each frame is refreshed at 60 Hz. (50 Hz.) rate in an overlapped manner rather than using an interlaced scan. This provides all of the video information required and allows refresh to occur twice as often as compared with television, resulting in reduced flicker while allowing the use of faster, brighter phosphor.

Each character is made up from a 7 x 9 dot matrix in a 9 x 12 field. Lower case characters are formed in a 7 x 11 matrix. While 80 characters are displayed on each line, the timing allows 100 character times per line including Horizontal Sync. timing, resulting in the display being centered horizontally on the screen.

Vertically, each frame consists of 24 character lines, each 12 raster lines tall. While this requires 288 raster lines, the Visual 200 generates 310 lines (60 Hz.) or 372 lines (50 Hz.) to center the display vertically and to provide proper synchronizing with the power line frequency. The following calculations describe the above relationships. (60 Hz.) (9 dots width per character) (100 characters per line) (310 raster lines per frame) (2) = 33.48 MHz. (50 Hz.) (9 dots width per character) (100 characters per line) (372 raster lines per frame) (2) = 33.48 MHz.

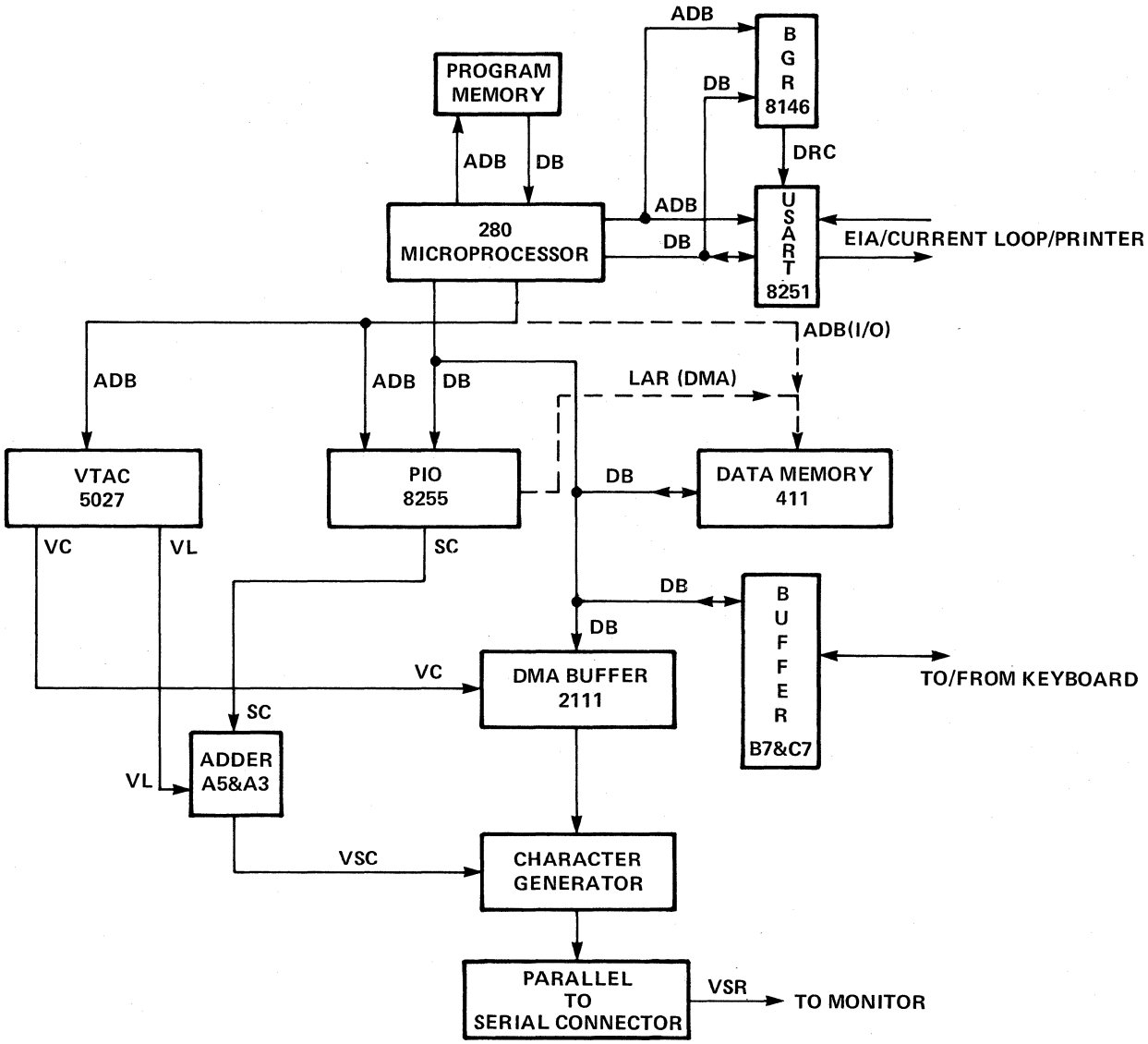

Figure 1-1. Block Diagram

2. THEORY OF OPERATION

The Visual 200 printed circuit board contains all logic components and power supply components except for the transformer. The printed circuit board is laid out in a geographic manner allowing the schematic diagrams to serve as the assembly drawing normally required to locate various parts. The PCB is organized in 9 rows lettered from the bottom from A to K, and in 11 columns numbered from left to right from 1 to 11.

2.1 MASTER TIMING AND VIDEO REFRESH TIMING

Sheet 5 of the schematics contains the crystal oscillator operating at 33.48 MHz. This clock signal is divided by 2 (A1) forming Data Rate Clock (DRC) at 16.74 MHz. DRC is divided by 8 (C1) to form the processor clock (PCLK) at 2.09 MHz. DRC also feeds the 5 stage ring counter performing a divide by 9, and providing the resulting 1.86 MHz. rate in five phases (DCA, DCB, DCC, DCD, DCE). DCD and DCE are combined to create VMREQ (Video Memory Request) which clocks the data transfer from Data Memory to DMA buffer during a DMA cycle. VMREQ will occur at a rate of 537 ns. per character. The rest of the video timing is generated by the VTAC (Video Timing and Control Chip). The VTAC provides the following outputs: CSYN (Composite Sync), CRV (Cursor Video), VBLANK (Vertical Blanking), HSYN (Horizontal Sync), VSYN (Vertical Sync), LC0 thru LC3 (Raster Line output each character line), VC0 thru VC6 (Video Character Count per line) and VL0 thru VL4 (Video Line Count).

2.2 VIDEO REFRESH (DATA TRANSFER)

Each time the twelfth line of each character line is displayed, a DMA cycle is enabled. Sheet 7 shows the BUSRQ flop (K3) which is set at the end of the twelfth scan line. ELC (End of Line Count e.g. scan 12) enables this flop. It is set by HSYNC (Horizontal Sync) which occurs at the end of each scan line. This flop requests a DMA cycle of the Z80 which will be acknowledged at the end of the current instruction. When the Z80 releases the I/O bus to the DMA it will respond with a bus acknowledge ($\overline{\text{BUSAK}}$). Note that a DMA cycle is inhibited during vertical retrace time by the signal VSYN which inhibits ELC from enabling the BUSRQ flop. Once the Z80 releases the bus to the DMA, Data Memory address is established by flop H3 on sheet 5. $\overline{\text{DBAK}}$ (Data Bus Acknowledge) gates the LAR bits (Line Address Register) on the high order address bus and the VC bits (Video Character) from the VTAC on the low order address bus. The BUSRQ flop is reset by the next HSYNC pulse (one line later), which forces the $\overline{\text{DBAK}}$ flop reset and returns the bus to the Z80. During the DMA cycle at each character time VMREQ sheet 5 is generated. VMREQ generates $\overline{\text{MREQ}}$ (Memory Request) on sheet 1 which forces $\overline{\text{RAMSEL}}$ (Ram Select) also on sheet 1, and allows the address bus to select the Data Memory shown on sheet 4. Data read from Data Memory is placed on the data bus and loaded into the 128 character DMA buffers shown on sheet 6 (D5 and E5). At each character time, DCE strobes memory data into the latch D6. Present configurations of the V200 do not utilize attributes (W8 installed), resulting in all 8 bits of the memory word being transfered into the DMA buffer. Video Character Count (VC0-VC6) provide the actual location within the DMA buffer.

The LAR (Line Address Register) generated by firmware and output by the PIO (F7 & F8) sheet 1, point to the first character of a group of 128 characters in data memory. The first 80 locations of each block is the data displayed on that particular line of the screen. The remaining 48 locations are used as function key data on the Block Mode version.

During each DMA cycle a non-maskable interrupt ($\overline{NMI}$) is generated. This is shown on sheet 1 in the center of the page. $\overline{NMI}$ is serviced by the Z80 immediately upon exiting the DMA cycle and is used to update the LAR, so that the LAR will point to the next line to be loaded into the DMA buffer on the next DMA cycle.

Once the DMA cycle has ended and the new line to be displayed on the screen is in the DMA buffer, see sheet 6, no further data can enter the buffer as D4 is now disabled. Video character counts (VC0-VC6) continue to be generated, and cause current DMA data to be presented on the output of the DMA buffer (D5 & E5). Each character time these character codes, in ASCII, are latched into L5. The seven low order bits are presented to the character generator ROM/PROM together with the Video Slice counter (VSC0-VSC3). This character generator address provides the horizontal dots for each character on each of the twelve raster lines (slices) to the video shift register K5. The Video Shift Register converts the parallel dot information into a serial dot stream (VSR). The high order bit from the DMA buffer is stored in flop E2 for future use as half intensity display ($\overline{HLF}$).

At the bottom of sheet 6, the flop A1 generates the signal DOT. Because attributes are not presently supported, chips E6, F5, F3, D1 and D2 are not present. As a result, only the top two gate inputs to F2 are functional. Video data from the video shift register (VSR) is allowed through the gate F2 except when the video shift register is being loaded ($\overline{LVSR}$ = 0). The second gate input section of F2 allows VB8 through while the video shift register is being loaded. VB8 is generated only by graphics symbols and is the right most dot of horizontal segments which require continuous lines on the screen. On the right side of sheet 7, DOT with the reverse video switch off ($\overline{RVID}$) generate straight dots ($\overline{SDOT}$) which are white dots. If the reverse video switch is on (RVID) then DOT becomes $\overline{RDOT}$ (reverse Dots) which are black dots. These are presented to the video input of the internal monitor via connector J6 pin 2. RVID is generated above this logic and is the reverse video switch ($\overline{RVIDS}$) which is exclusive or'd with the cursor block and delayed by flop K1. The delay by flop K1 matches the internal delay of the character generator PROM. $\overline{REV}$ (Reverse Attribute is also gated with $\overline{RVIDS}$, but because attributes are not presently supported $\overline{REV}$ will always be false. Horizontal and Vertical Syncs. (HSYNC & VSYNC), together with half intensity ($\overline{HLF}$) and power are presented to the monitor. Refer to the Video Cable Drawing located at the rear of this manual for the schematic which shows that the half intensity signal ($\overline{HLF}$) and the Half Intensity Potentiometer form a voltage divider for video. Composite Sync (CSYN) and both straight and reversed dots are mixed on sheet 7 to provide the external video.

External video will drive an RS170 monitor provided that the monitor has a video bandwidth in the 18 MHz. range, and provided it will synchronize at 18.6 KHz. horizontal rate.

2.2.1 Smooth Scroll Video Refresh

The scroll counter (SC0-SC3) on sheet 1 (PIO) F7 & F8, is intitalized to a count of 4. On sheet 7 the scroll count is added to the scan line count by adders A5 and A3 generating video slice counts (VSC0-VSC3). With this initialization, scan lines 0 through 11 will result in video slice counts 0 through 11. This results in the dots being painted on the

screen in their proper orientation vertically. Once scroll is enabled the scroll counter will be advanced from 4 to 5. On the next frame each character line will be displayed with slice 1 at the top of each line area followed by slices 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 0. This is performed for the entire frame. At the end of the frame the scroll counter is again advanced (to 6) and now causes each character line to be displayed with slice 2 at the top followed by 3, 4, , , , 11, 0, 1. This sequence continues until twelve frames have been completed, at which time the screen has been scrolled up one character line. Each time ELC is decoded (VSC=11) a DMA cycle is initiated and the next line of data is extracted from memory. This results in the next line of data being painted on the screen beginning at VSC=0.

Once the scroll counter advances from 4 to 15 it is reset to 4.

Example:

Scroll Count		Line Count		A5		A3 Input		VSC		
4	+	0		4	+	12	=	16	=	0
		1		5		12		17		1
		2		6		12		18		2
		3		7		12		19		3
		4		8		12		20		4
		5		9		12		21		5
		6		10		12		22		6
		7		11		12		23		7
		8		12		12		24		8
		9		13		12		25		9
		10		14		12		26		10
		11		15		12		27		11
5	+	0	=	5	+	12	=	17	=	1
		1		6		12		18		2
		2		7		12		19		3
		3		8		12		20		4
		4		9		12		21		5
		5		10		12		22		6
		6		11		12		23		7
		7		12		12		24		8
		8		13		12		25		9
		9		14		12		26		10
		10		15		12		27		11
		11		0+ Carry		0		0		0 ← (Next Data Line)

2.3 MICROPROCESSOR ADDRESSING

2.3.1 Program Memory Addressing

Two PROM/ROM sockets are provided which allow for use of 2K, 4K, or 8K PROMS or ROMS. The following chart provides the addresses in hex for the indicated device sizes and assumes that the jumpers W12 through W18 are installed according to notes on schematic sheet 1.

Device Size	Socket G10	Socket E10
2K	0000-07FF	0800-0FFF
4K	0000-0FFF	1000-1FFF
8K	0000-1FFF	2000-2FFF

2.3.2 Data Memory Addressing

The data memory 4096 X 8 is addressed from 4000 to 4FFF hex ($\overline{\text{RAMSEL}}$).

2.3.3 Device Addressing

The following device address decoding is shown on sheet 1 of the schematic.

Signal	Hex Address	Description
$\overline{\text{KBSTB}}$	00	Read and Write the Keyboard
$\overline{\text{SSREG}}$	01	Read Status Register and Write the Baud Rate Generator
$\overline{\text{SSIO}}$	1X	Read and Write the USART
$\overline{\text{SPIO}}$	2X	Write the PIO
$\overline{\text{SVLINE}}$	3X	Read Current Video Line Count
$\overline{\text{RDMAI}}$	4X	Reset DMA Inhibit
$\overline{\text{SVTAC}}$	5X	Read and Write the VTAC
$\overline{\text{RVATE}}$	6X	Reset Video Attributes

2.3.3.1 Keyboard Operation

The microprocessor reads the keyboard by generating a 4 Bit address indicating which of 16 columns within the keyboard is to be selected. $\overline{\text{KBSTB}}$ (Address 00, 02, 04, 06, 08, 0A, 0C, or 0E) is used on sheet 3 to gate the low order four bits of the data bus to the keyboard. While the $\overline{\text{KBSTB}}$ is low (see keyboard schematic) the four bits are loaded into the 22-00950 IC and select one of the vertical axis X0-X11. $\overline{\text{KBSTB}}$ when low also inhibits the detector chip, 22-00908. When $\overline{\text{KBSTB}}$ returns high the address remains latched in the 950 IC, however the detector chip is now enabled and will present, on its output, eight bits which represent all or any of the eight keys on that vertical axis which are presently depressed. On sheet 3 of the schematics $\overline{\text{RDKBD}}$ is required in order for the keyboard data to be read by the Z80. $\overline{\text{RDKBD}}$ is activated by addresses 00, 02, 04, 06, 08, 0A, 0C, or 0E which are the same as $\overline{\text{KBSTB}}$. $\overline{\text{KBSTB}}$ is generated at these addresses during an I/O write. $\overline{\text{RDKBD}}$ is generated at these addresses during an I/O read. The keyboard row and column assignments do not represent any particular coding and are represented on the keyboard schematic by the numeric location of the key. This number is marked on the underside of each keyboard. In addition to this numeric location code the schematic also has the key top legend of the standard U.S. version.

2.3.3.2 Status Register and Baud Rate Generator

Device addresses 01, 03, 05, 07, 09, 0B, 0D, and 0F are used to read the Status Register and to write to the Baud Rate Generator. On sheet 3 of the schematics all switches which are accessible at the rear of the terminal, are read by the two multiplexers A4 and B4, except for the reverse video switch. During normal operation these switches are not read continuously, see paragraphs 3.1.1 and 3.1.2.5 of the Reference Manual.

After the Z80 reads these switches, four of which are Data Rate, it sets the Data Rate by writing to the Baud Rate Generator. The output of the Baud Rate Generator is 16 times the data rate selected (110 baud is 1.76 KHz.).

2.3.3.3 USART

The USART (Universal Synchronous, Asynchronous Receiver Transmitter) IC located at E7 and E8 is operated in the asynchronous mode. It is used to serialize transmit and printer data and to convert receive serial data to parallel. Device addresses 10, 12, 14, 16, 18, 1A, 1C, and 1E are used to write, transmit/print, data to the USART and are used to read received data. Addresses 11, 13, 15, 17, 19, 1B, 1D and 1F are used to set (write) the mode (asynch./sync.), parity, and interface lines (RTS, DTR, DSR, and GCTS) and to read status of the USART (overrun, parity error, etc.). See the IC section of this manual for detailed specifications and operation.

2.3.3.4 PIO

The parallel I/O IC is used to enable transmit data, as a Line Address Register and Scroll counter. It contains three channels which are all set to output mode during initialize. Device addresses 20, 24, 28, and 2C are used to write to channel A. Device addresses 21, 25, 29 and 2D are used to write to channel B (LAR and keyboard lights). Device addresses 22, 26, 2A and 2E are used to write to channel C (Scroll Count, Bell, etc.). Device addresses 23, 27, 2B and 2F are used to set the mode of all channels. See the IC section of this manual for complete specification.

2.3.3.5 Select Video Line ($\overline{\text{SVLINE}}$)

Device addresses 30 through 3F are used to read the current video line count from the VTAC, sheet 5, in order for the Z80 to update the LAR. This command also resets the non-maskable interrupt generated by the last DMA cycle. This function is performed as part of the DMA interrupt cycle which immediately follows each DMA cycle.

2.3.3.6 Reset DMA Inhibit ($\overline{\text{RDMAI}}$)

Device addresses 40 through 4F are used to reset the DMA inhibit which is set after the last line is refreshed on the screen each frame. This prevents DMA cycles from occurring during vertical retrace.

2.3.3.7 VTAC

The VTAC establishes the refresh timing, and addressing, along with establishing the position of the cursor. The following addresses are used to control the VTAC:

Address	Function	
50	Load Register 0	Initialize Parameters
51	Load Register 1	
52	Load Register 2	
53	Load Register 3	
54	Load Register 4	
55	Load Register 5	
56	Load Register 6	
57	Initialize Start Command	
58	Read Cursor Line Address	
59	Read Cursor Character Address	
5A	Reset VTAC	
5B	Scroll Up Command	
5C	Load Cursor Character Address	
5D	Load Cursor Line Address	
5E	Start VTAC Command	
5F	Not Used	

During initialize, registers 0 through 6 are loaded to set the operating parameters as follows:

Register	60 Hz. Value	50 Hz. Value	Description
0	63	63	Horizontal Line Count 99 Characters
1	43	43	Non Interlace, Hsync. Width = 8 Characters
2	5D	5D	12 Scans/Row, 80 Characters/Row
3	97	97	24 Rows/Frame, 1 Character Sync. Blank Delay, 0 Cursor Delay
4	1B	3A	310 Lines (60 Hz.), 372 Lines (50 Hz.)
5	11	30	Data Starts After Vsync. 17 Lines (60 Hz.), 48 Lines (50 Hz.)
6	17	17	Last Line Displayed = 23 (24 Lines)

2.3.3.8 Reset Video Attributes ($\overline{\text{RVATE}}$)

Device addresses 60 through 6F are used to reset any attributes set. Because the present version of the V200 does not support attributes, and attribute logic is not present, this command is not presently used.

2.4 INTERFACE OPERATION

On sheet 2 of the schematics, all receivers, both EIA and Current Loop, are shown on the left side of the page. The MCT2, A9A, converts received current loop data to TTL. The 1489 IC's, B8 and B11, convert EIA signals to TTL levels. Note that each of the EIA

receivers has a pullup resistor attached to its node. This allows the receiver to detect a true condition when its input is not connected. Secondary Request-to-Send signal is attached to two output pins, 11 and 19, through jumpers W3 and W4. Both jumpers are installed at the factory and normally present no problems. Check the modem in use to insure that the extra pin is not used. Remove the incorrect jumper when required. The and-or-invert gate, B9, allows received EIA data, Current Loop received data and transmit data (when enabled) to the USART($\overline{RXD}$).

At the top right of sheet 2 received Clear-to-Send($\overline{CTS}$) causes $\overline{GCTS}$ to enable the USART transmitter. $\overline{FCTS}$ (Force Clear-to-Send) forces the USART transmitter on when $\overline{CTS}$ is false and when printer output is required. $\overline{FCTS}$ is generated by the PIO.

Transmit data from the USART ($\overline{TXD}$) is converted from TTL levels to EIA levels by the 1488 IC, C10, and is converted to current loop levels by the MCT2, A9B. $\overline{DTR}$ and $\overline{RTS}$ from the USART are converted to EIA levels by C10. Received data($\overline{RXD}$) is allowed to the printer port when copy mode is enabled($\overline{COPY}$). Transmit data is sent to the printer port when print page mode is enabled($\overline{PPAGE}$).

2.5 SELF TEST

Each time the V200 is powered on, the following sequence is executed:

Caps Only and Line LEDs Illuminated
Checksum on Program Memory Calculated and Checked
Pattern Test on Data Memory
Caps Only LED Extinguished
VTAC Initialized
Terminal Set to Normal Mode and On Line

When the program memory self test and data memory pattern test is being executed, a continuous check for erroneous data is performed. Whenever incorrect data is found, the test sequence is halted just prior to extinguishing the Caps Only LED. Power must be turned off and back on in order to repeat the test. All terminal operation halts at this point when a self test error is found.

2.6 JUMPER ASSIGNMENTS

Each terminal's Main PCB contains up to 19 jumpers which are used to alter features and to adapt to various Modems.

	Description		
Jumper	Installed	Removed	Status
W1	Printer Busy Pin 2 (Note 1)	Disconnected	OUT
W2	Printer Busy Pin 4 (Note 1)	Disconnected	OUT
W3	SRTS Pin 19 (Note 4)	Disconnected	IN
W4	SRTS Pin 11 (Note 4)	Disconnected	IN
W5	Current Loop RCVR Connected (Note 2)	Disconnected	IN

Jumper	Description: Installed	Description: Removed	Status
W6	Current Loop XMTR Connected (Note 3)	Disconnected	IN
W7	Printer Busy Connected (Note 1)	Disconnected	OUT
W8	Disable Attributes	Enable Attributes	IN
W9	ASCII XMIT Data (Note 1)	Scrambled Xmit Data	IN } Note 5
W10	# (Note 1)	£	IN } Note 5
W11	60 Hz. (Note 1)	50 Hz.	IN } Note 5
W12	Largest PROM = 2K X 8	Largest PROM = $\overline{2K \times 8}$	
W13	Largest PROM = 4K X 8	Largest PROM = $\overline{4K \times 8}$	
W14	G10 = 2K or 4K	G10 = 8K	
W15	G10 = 8K	G10 = 2K or 4K	
W16	E10 = 2K	E10 = 4K	
W17	E10 = 4K	E10 = 2K	
W18	Largest PROM = 8K X 8	Largest PROM = $\overline{8K \times 8}$	
W19	External 16X Clock Connected to Pin 13	Disconnected	IN

Note 1: Used only on model 200-1

Note 2: Current Loop Receiver uses EIA pin 17. Some V24 Modems use 17 as signal pin, in which case W5 must be removed.

Note 3: Current Loop Transmitter uses EIA pin 25. Some V24 Modems use 25 as a signal pin, in which case W6 must be removed.

Note 4: Secondary Request-to-Send uses pin 11 on Bell 202 series modems and pin 19 on EIA and V24 modems. When a modem with secondary channel is used remove whichever jumper is not used.

Note 5: Installed for model 200-1. Nonexistant on all other models.

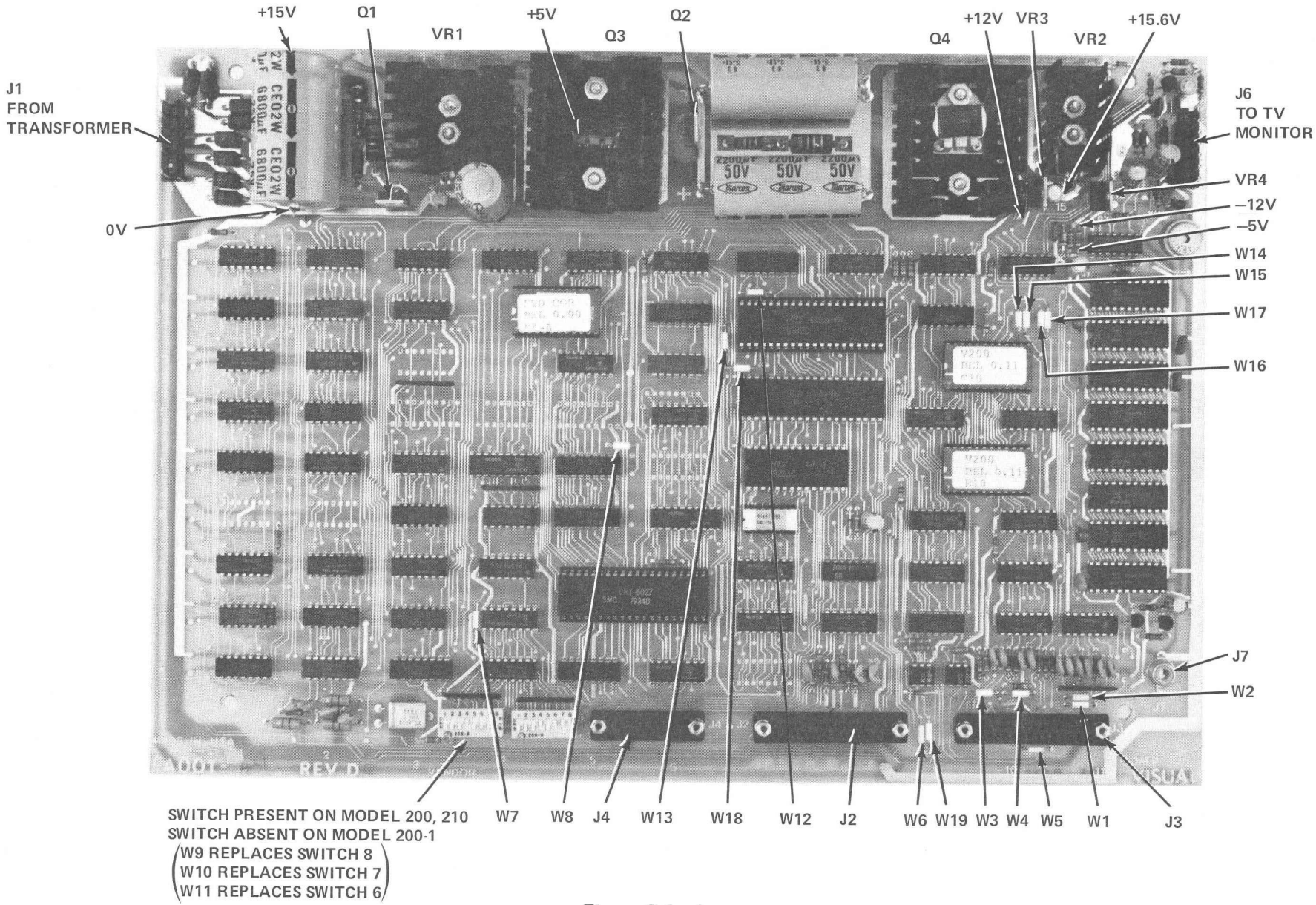

Figure 2-1. Jumpers

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3. SPARE PARTS AND TOOLS

3.1 SPARE PARTS

Each Visual 200 terminal is composed of three major subassemblies and is designed to be serviced on site by replacing subassemblies only.

3.1.1 TV Monitor Subassembly

The Zenith model D 12-NK-12 monitor consists of three assemblies as follows:

Description	Zenith Part No.	Visual Part No.
Monitor (total)	D 12-NK-12	MN 001-000
PCB	A8437	MN 001-002
Flyback Transformer	A8438	MN 001-001
CRT & Yoke (CRT is Panasonic 310JLB4N)	F6348	MN 001-003

3.1.2 Keyboard Assembly

Three keyboards are utilized within the product as follows:

Description	Model	KTC Part No.	Visual Part No.
Standard KBD	200	65-2006-02	KB 001-002
KBD with Function Keys	200	65-2006-03	KB 001-003
Block Mode KBD with with Function Keys	210	65-2006-04	KB 001-004

3.1.3 Main PCB

The main PCB (PA 001-A01) is used on both the model 200 and the model 210. The model implies firmware when ordered as a total terminal. When ordering the PCB as a spare, the firmware and character set must be additionally specified. Section 3.1.4 defines the firmware and character generator variations.

3.1.4 PROM/ROM Assignments

PCB Location	PROM No.	ROM No.	Description
H4	STDCGR	IC 240-001	Standard Character Generator used on all U.S. Models
H4	CGR 52		Optional VT52 Graphics Character Generator Models 200, 210
G10	V200	IC 240-002	Firmware Used on Model 200
E10	V200	IC 240-003	
G10	V210	IC 243-001	Firmware Used on Model 210
E10	V210	Not Used	

3.2 SPARE SUBASSEMBLY RECOMMENDATIONS

To service 100 terminals by subassembly exchange, the following subassemblies should be stocked at the quantities indicated.

Quantity	Description	Part No.
5	Main PCB	PA 001-A01
5	Keyboards	KB 001-002, 003, or 004
3	TV Monitor PCB	MN 001-002

3.2.1 Active Component Recommendations

The following list contains all active components found on the Main PCB and on the Keyboard. Total quantities per terminal and recommended stocking levels are indicated. The recommendations are based on one depot repairing subassemblies from approximately 100 terminals. See Section 7 for TV monitor components.

Part	Visual P.N.	Qty./Terminal	Recommended Spares
74S04	IC 020-004	1	10
74S08	IC 020-008	1	10
74S10	IC 020-010	1	10
74S38	IC 020-038	2	15
74S64	IC 020-064	1	10
74S74	IC 020-074	1	10
74S174	IC 020-174	1	10
7416	IC 010-016	1	10
74166	IC 010-166	1	10
74LS00	IC 000-000	2	15
74LS04	IC 000-004	4	20
74LS08	IC 000-008	6	20
74LS32	IC 000-032	4	20
74LS54	IC 000-054	1	10
74LS74	IC 000-074	4	20
74LS75	IC 000-075	1	10
74LS83	IC 000-083	2	15
74LS86	IC 000-086	1	10
74LS93	IC 000-093	1	10
74LS138	IC 000-138	1	10
74LS139	IC 000-139	1	10
74LS175	IC 000-175	1	10
74LS253	IC 000-253	2	15
74LS273	IC 000-273	2	15
74LS367	IC 000-367	5	30
74LS368	IC 000-368	5	30
1488	IC 340-001	2	15

Part	Visual P.N.	Qty./Terminal	Recommended Spares
1489	IC 340-002	2	15
μPD 411	IC 140-001	8	15
2111	IC 140-002	2	10
Z80(μPD 780)	IC 440-001	1	10
P10(μPD 8255)	IC 440-002	1	10
USART(μPD 8251)	IC 440-003	1	10
VTAC(CRT 5027)	IC 440-004	1	10
BRG(8146T-002)	IC 340-003	1*	10
MCT-2	IC 340-004	2	15
PN3644	TR 000-001	2	10
PN3643	TR 100-001	2	15
TIP32	TR 020-001	2	15
TIP34	TR 020-002	2	15
7805	VR 000-005	1	10
7812	VR 000-012	1	10
7815	VR 000-015	1	10
7912	VR 010-012	1	10
1N914	DA 000-001	5	10
1N5401	DA 320-001	8	15
1N4733A	DA 230-051	1	10
Firmware	See Sec. 3.1.4	1 set*	2 sets
Character Gen.	See Sec. 3.1.4	1*	2
22-00950-003	Keytronic	1*	15
22-00908-003	Keytronic	1*	15

*denotes custom part

3.3 TOOLS

In order to gain access to the Visual 200 and to replace any subassembly, only a cross-head and common blade screwdriver are required. The following listed tools, or their equivalent, are recommended for depot level where subassemblies are repaired.

Qty.	Description	Manufacturer	Part No.
1	Oscilloscope, 10 MHz.	Tektronix	335, 465
1	Romaid 2700 ROM Simulator with 716 Personality Module	Microlink	2700-716
1	V200 TEST PROM	Visual	V200TEST

4. TEST METHODS

Test procedures for use of the Romaid ROM Simulator and the V200 TEST PROM are included with the test PROM. This combination allows the depot to exercise the Z80, PIO, VTAC, USART, and memory.

5. MNEMONIC LIST

MNEMONIC LIST

Mnemonic	Source Schematic Sheet	I.C.	Description
+5	8	Q3	+5 Volts
–5	4	CR9	–5 Volts
+12	8	VR3	+12 Volts
+15	8	Q4	+15 Volts
–12	8	VR4	–12 Volts
AB0	1	H7	Address Bit 0 (Non DMA Cycle)
AB0	5	G5	Address Bit 0 (DMA Cycle)
ATT	6	D3	Attribute Character
ATTE	6	E3	Attribute Enable
BELL	1	F7	Bell
BLANK	6	F3	Video Blank (Attribute)
BLINK	6	F3	Video Blink (Attribute)
BLOCK	1	F7	Block LED Drive (210)
BR0	3	SWITCH A	Baud Rate Selector Bit 0
BUFWR	6	C3	Buffer Memory Write (DMA Cycle)
BUSAK	1	H7	Bus Acknowledge (DMA Cycle)
BUSRQ	7	K3	Bus Request (DMA Cycle Request)
CAPS	1	F7	CAPS LED Drive
CD	2	B8	Primary Channel Carrier Detect
COPY	1	F7	Copy Mode
CRV	5	C5	Cursor Video
CSYN	5	C5	Composite Sync (H, & V,)
CTS	2	B11	Clear to Send
CURBL	6	E2	Cursor Block
DB0	SEVERAL		Data Bus Bit 0
DBAK	5	H3	Decoded Bus Acknowledge (DMA Cycle)
DCB	5	B1	Decoded Character Clock B (1.86 MHz)
DCC	5	B1	Decoded Character Clock C (1.86 MHz)
DCD	5	B1	Decoded Character Clock D (1.86 MHz)
DCE	5	B1	Decoded Character Clock E (1.86 MHz)

MNEMONIC LIST (Continued)

Mnemonic	Source Schematic Sheet	I.C.	Description
DDBL	7	C2	Double Delayed Blank
DOT	6	A1	Blanked Dots
DRC	5	A1	Data Rate Clock (16.7 MHz)
DRD	1	K1	Delayed Read
DS10	7	B3	Display Slice 10
DSR	2	B11	Data Set Ready
DTR	1	E7	Data Terminal Ready
ELC	7	B3	End of Line Count (Slice 11)
FCTS	1	F7	Force Clear to Send (Printer Operation)
GCTS	2	H9	Gated Clear to Send
HSYN	5	C5	Horizontal Sync
INT	1	G6	Maskable Interrupt
IOREQ	1	H7	I/O Request
KB0	3	KEYBOARD (J4)	Keyboard Bit 0
KSTB	1	K6	Keyboard Strobe
LAR0	1	F7	Line Address Register Bit 0
LC0	5	C5	Line Count Bit 0
LINE	1	F7	On Line LED Drive
LVSR	5	A2	Load Video Shift Register
M1	1	H7	M 1 Cycle (OP Code Fetch)
MREQ	1	H7	Memory Request Cycle
NMI	1	K3	Nonmaskable Interrupt
PBUSY	2	B11 (200-1)	Printer Busy
PBUSY	3	DIP SWITCH B (200)	Auto New Line Switch
PCLK	5	C1	Processor Clock (2.09 MHz)
PPAGE	1	F7	Print Page
RAMRD	1	K9	RAM Read
RAMSEL	1	H9	RAM Select
RB0	4	U1	RAM Bit 0
RD	1	H7	Read Cycle
RDE	1	F7	Receive Data Enable
RDKBD	1	K6	Read Keyboard
RDMAI	1	H6	Reset DMA Inhibit
RDOT	7	K2	Reverse Dots
RESET	1	D9	Reset (Power On)
REV	6	F3	Reverse (Attribute)

MNEMONIC LIST (Continued)

Mnemonic	Source Schematic Sheet	I.C.	Description
RFSH	1	H7	Refresh RAM Cycle
ROW	1	H9	Read or Write Cycle
RS0	1	K6	ROM Select 0
RTS	1	E7	Request to Send
RVATE	1	H6	Reset Video Attributes
RVID	7	K4	Reverse Video
RVIDS	3	SWITCH A	Reverse Video Switch
RXD	2	D9	Receive & Xmit Serial Data
SBRG	1	K6	Set Baud Rate Generator
SC0	1	F7	Scroll Count 0
SCCD	2	B8	Secondary Carrier Detect
SCRTS	1	F7	Secondary Channel Request-to-Send
SDOT	7	K2	Straight Dots
SPDE	1	F7	Serial Print Data Enable
SPIO	1	H6	Select Parallel I/O (PIO)
SS0	3	SWITCH A	Selection Switch Bit 0
SSIO	1	H6	Select Serial I/O (USART)
SSREG	1	K6	Select Status Register
SVLINE	1	H6	Select Video Line
SVTAC	1	G6	Select VTAC
TDE	1	F7	Transmit Data Enable
TXC	3	D7	Transmit/Receive Clock
TXD	1	E7	Transmit Data
UL	6	F3	Underline (Attribute)
VB8	6	K4	Video Bit 8
VBLANK	5	C5	Vertical Blank
VC0	5	C5	Video Character Counter Bit 0
VD0	6	D6	Video Data Bit 0
VIDINH	1	F7	Video Inhibit
VL0	5	C5	Video Line Counter Bit 0
VMREQ	5	A2	Video Memory Request (DMA Cycle Request)
VSC0	7	A3	Video Slice Count 0
VSR	6	K5	Video Shift Register (Serial Video)
VSYN	5	C5	Vertical Sync
WR	1	H7	Write Cycle

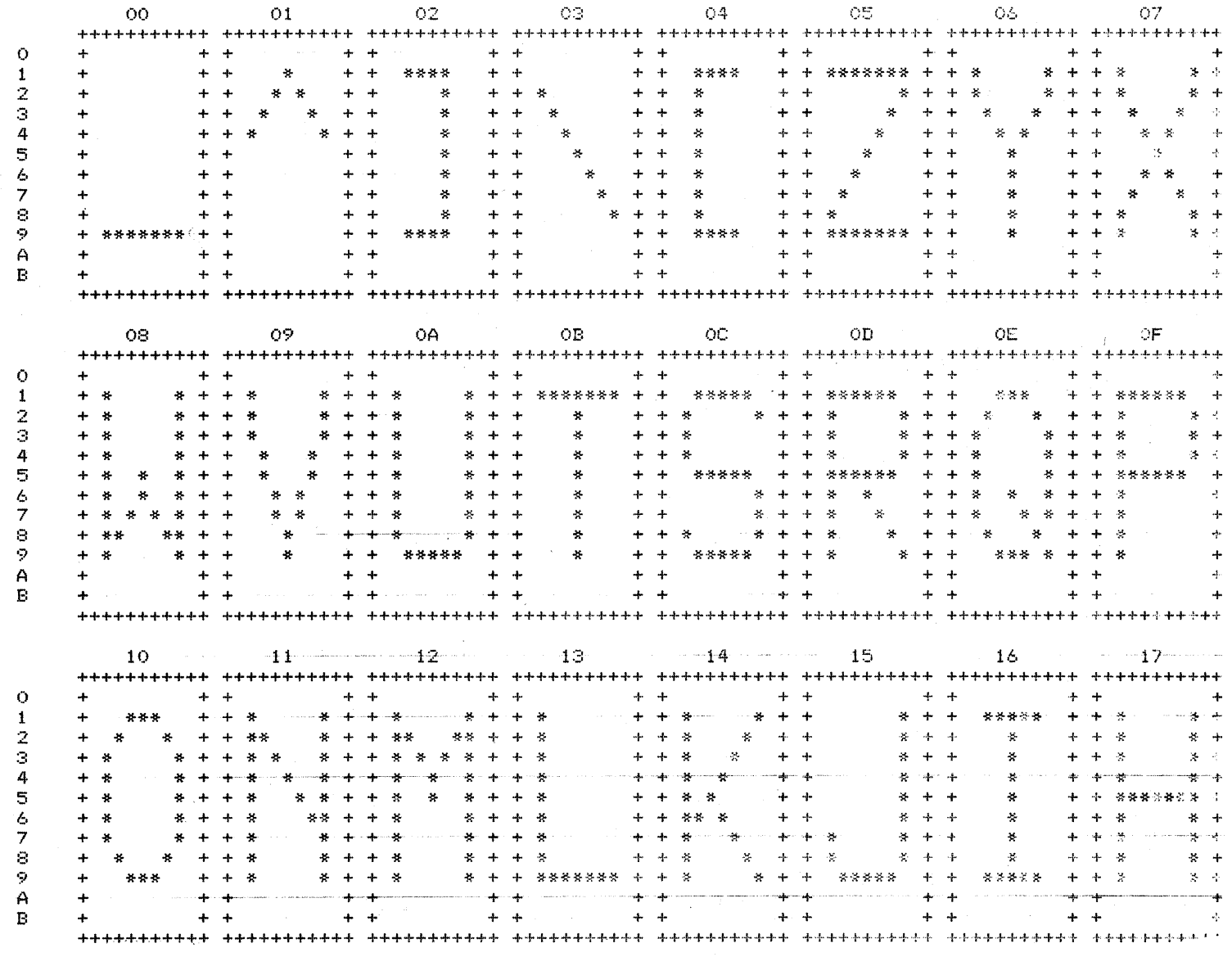
6. I.C. DATA SHEETS

Included in this section are specifications for the following I.C.'s.

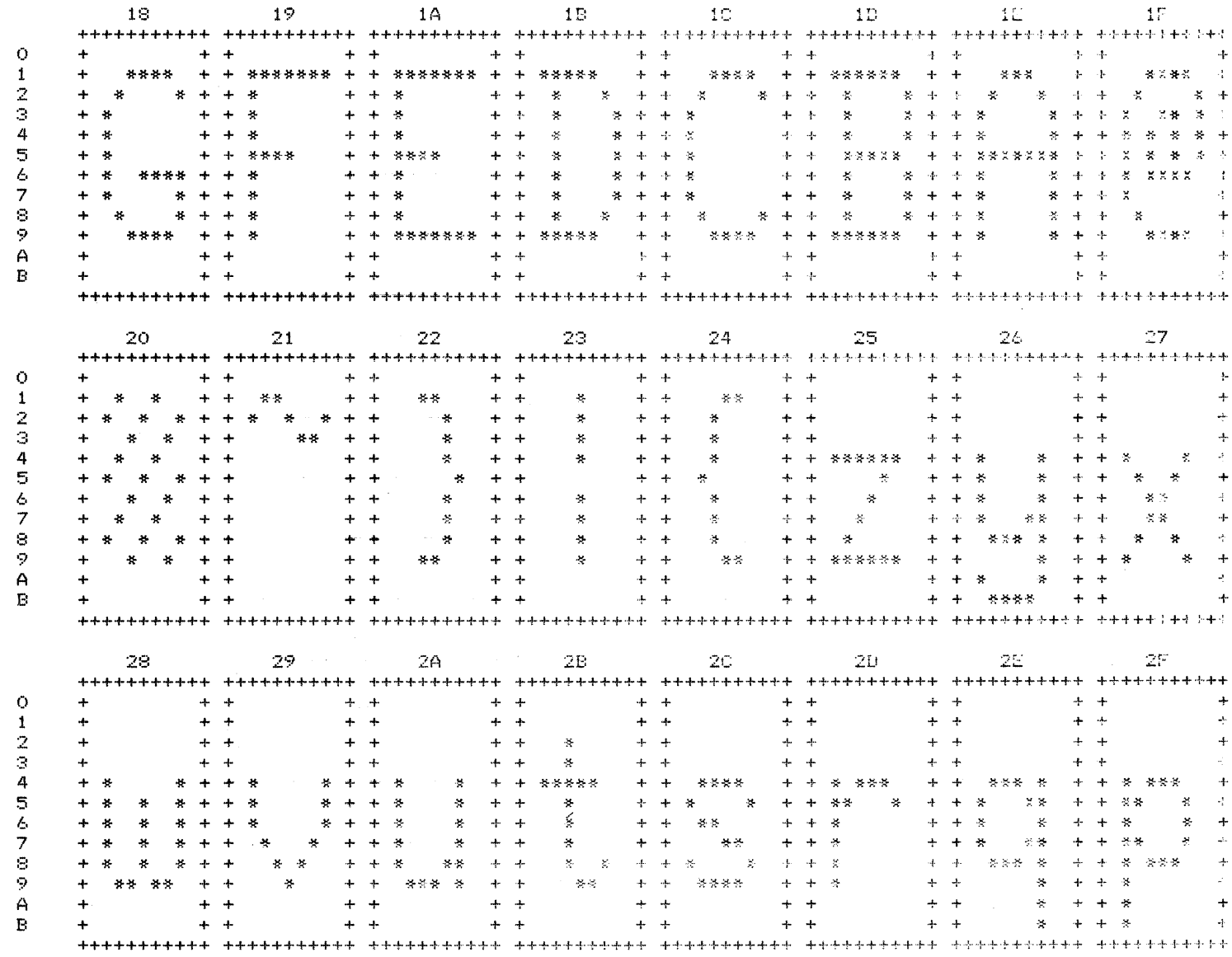
Standard Character Generator

μPD 780	Z80 CPU
μPD 411	4K RAM
2111	256X4 RAM
μPD 8251	USART
μPD 8255	PIO
8146T-002	Baud Rate Generator
CRT 5027	VTAC

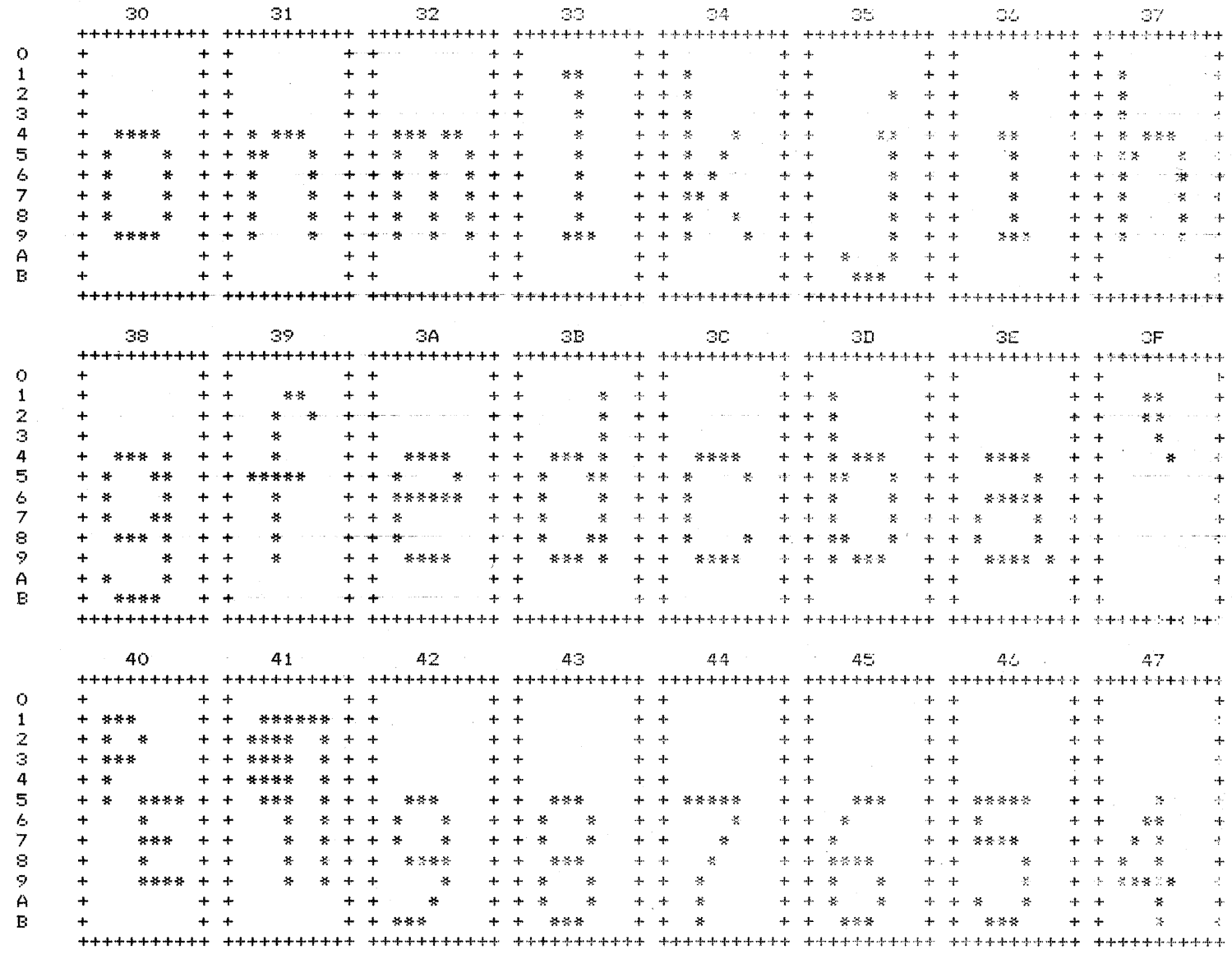
STDCGR-OBJ



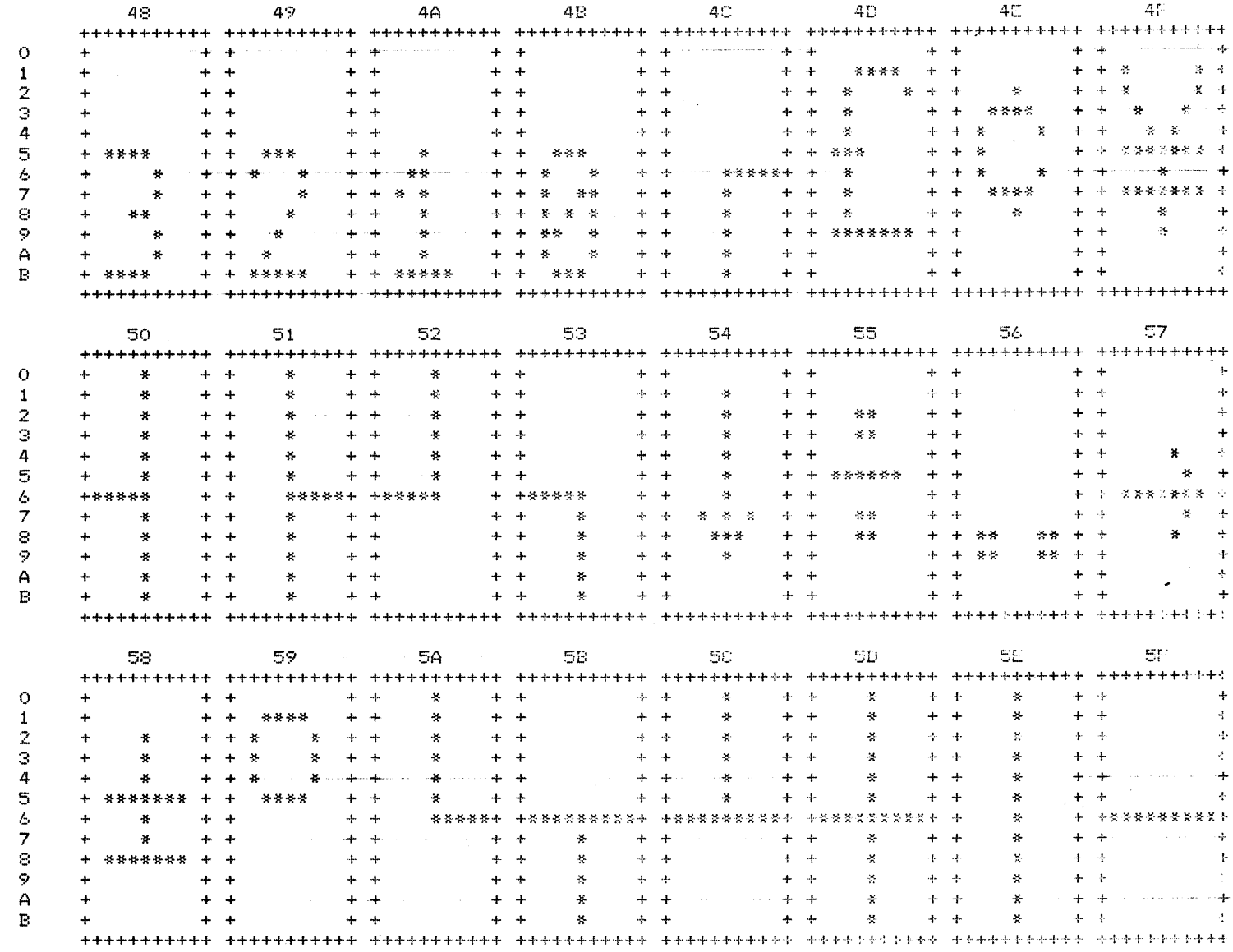
STDCGR-OBJ


18 19 1A 1B 1C 1D 1E 1F
0 1 2 3 4 5 6 7 8 9 A B
20 21 22 23 24 25 26 27
0 1 2 3 4 5 6 7 8 9 A B
28 29 2A 2B 2C 2D 2E 2F
0 1 2 3 4 5 6 7 8 9 A B

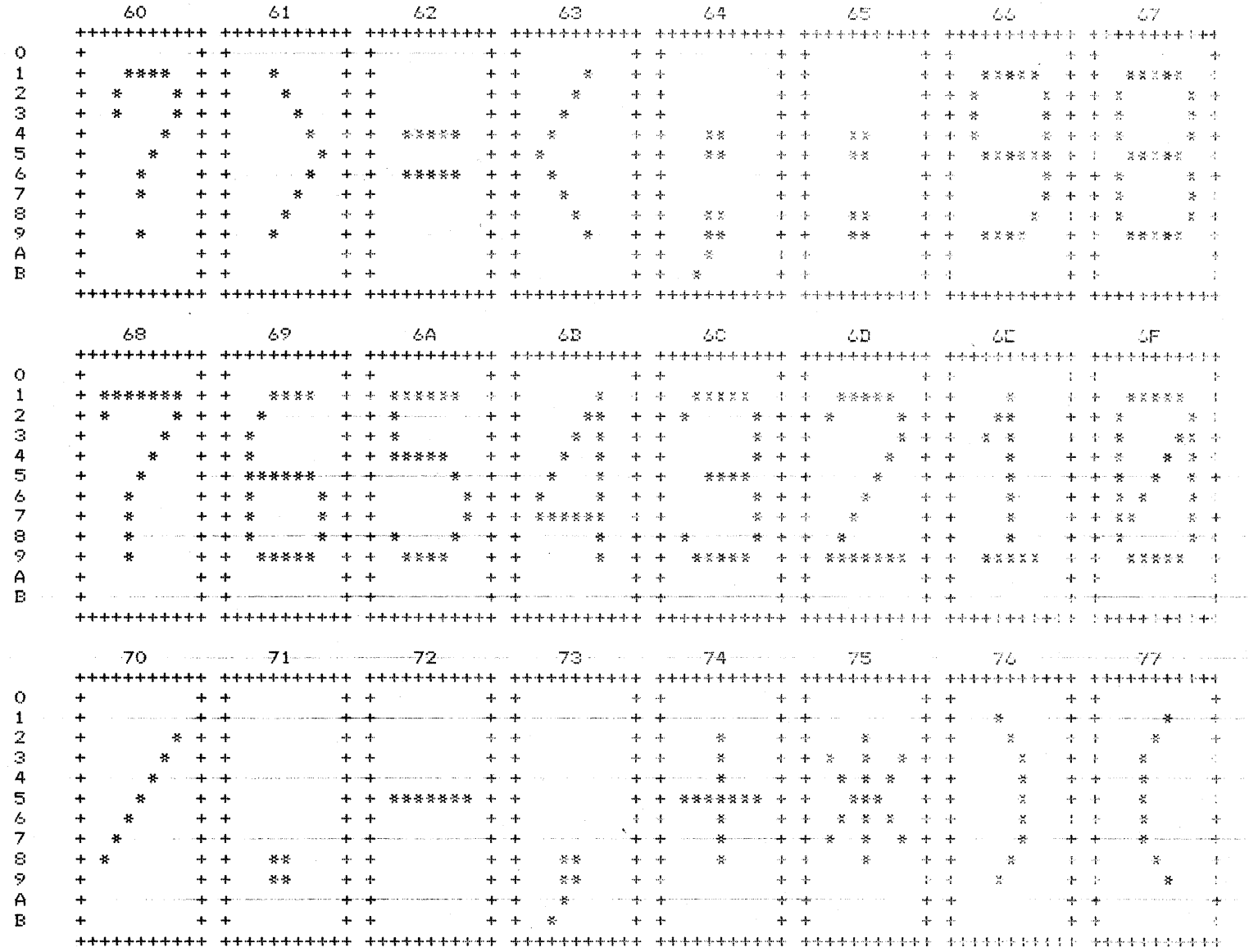
STDCGR-OBJ



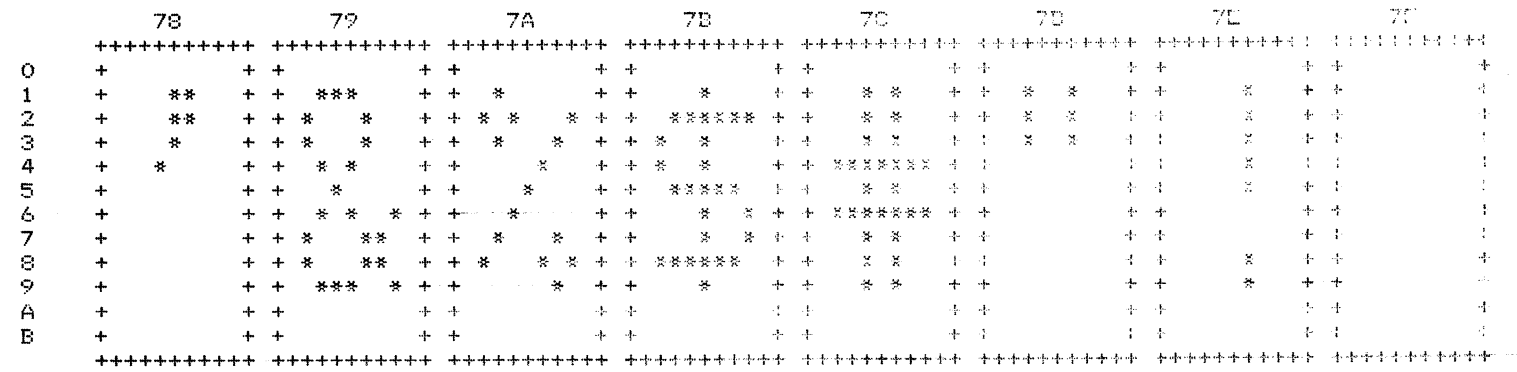
STDCGR-OBJ


48
49
4A
4B
4C
4D
4E
4F
50
51
52
53
54
55
56
57
58
59
5A
5B
5C
5D
5E
5F
0
1
2
3
4
5
6
7
8
9
A
B

STDCGR-OBJ


60 61 62 63 64 65 66 67
68 69 6A 6B 6C 6D 6E 6F
70 71 72 73 74 75 76 77
0 1 2 3 4 5 6 7 8 9 A B

STDCGR-OBJ



8-BIT N-CHANNEL MICROPROCESSOR COMPLETELY Z80™ COMPATIBLE

DESCRIPTION

The μPD780 and μPD780-1 processors are single chip microprocessors developed from third generation technology. Their increased computational power produces higher system through-put and more efficient memory utilization, surpassing that of any second generation microprocessor. The single voltage requirement of the μPD780 and μPD780-1 processors makes it easy to implement them into a system. All output signals are fully decoded and timed to either standard memory or peripheral circuits. An N-channel, ion implanted, silicon gate MOS process is utilized in implementing the circuit.

The block diagram shows the functions of the processor and details the internal register structure. The structure contains 26 bytes of Read/Write (R/W) memory available to the programmer. Included in the registers are two sets of six general purpose registers, which may be used as 8-bit registers individually, or as 16-bit register pairs. Also included are two sets of accumulator and flag registers.

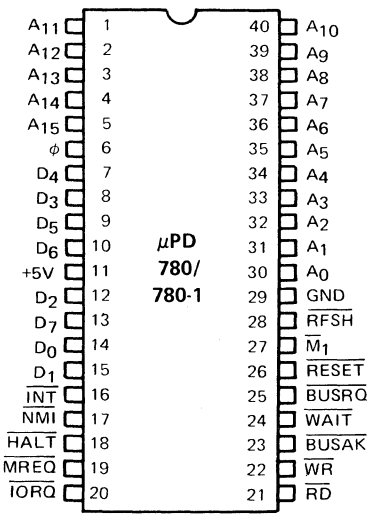
Through a group of exchange instructions the programmer has access to either set of main or alternate registers. The alternate register permits foreground/background mode of operation, or may be used for fast interrupt response. A 16-bit stack pointer is also included in each processor, simplifying implementation of multiple level interrupts, permitting unlimited subroutine nesting, and simplifying many types of data handling.

The two 16-bit index registers simplify implementation of relocatable code and manipulation of tabular data. The Refresh register will automatically refresh external dynamic memories. A powerful interrupt response mode will use the I register to form the upper 8-bits of a pointer to an interrupt service address table, while the interrupting apparatus supplies the lower 8-bits of the pointer. An indirect call will then be made to service this address.

FEATURES

- Single Chip, N-Channel Silicon Gate Processor
- 158 Instructions — Including all 78 of the 8080A Instructions, Permitting Total Software Compatibility
- New 4-, 8-, and 16-Bit Operations Featuring Useful Addressing Modes such as Indexed, Bit and Relative
- 17 Internal Registers
- Three Modes of Rapid Interrupt Response, and One Non-Maskable Interrupt
- Directly Connects Standard Speed Dynamic or Static Memories, with Minimum Support Circuitry
- Single-Phase +5 Volt Clock and 5 VDC Supply
- TTL Compatibility
- Automatic Dynamic RAM Refresh Circuitry
- Available in Plastic Package

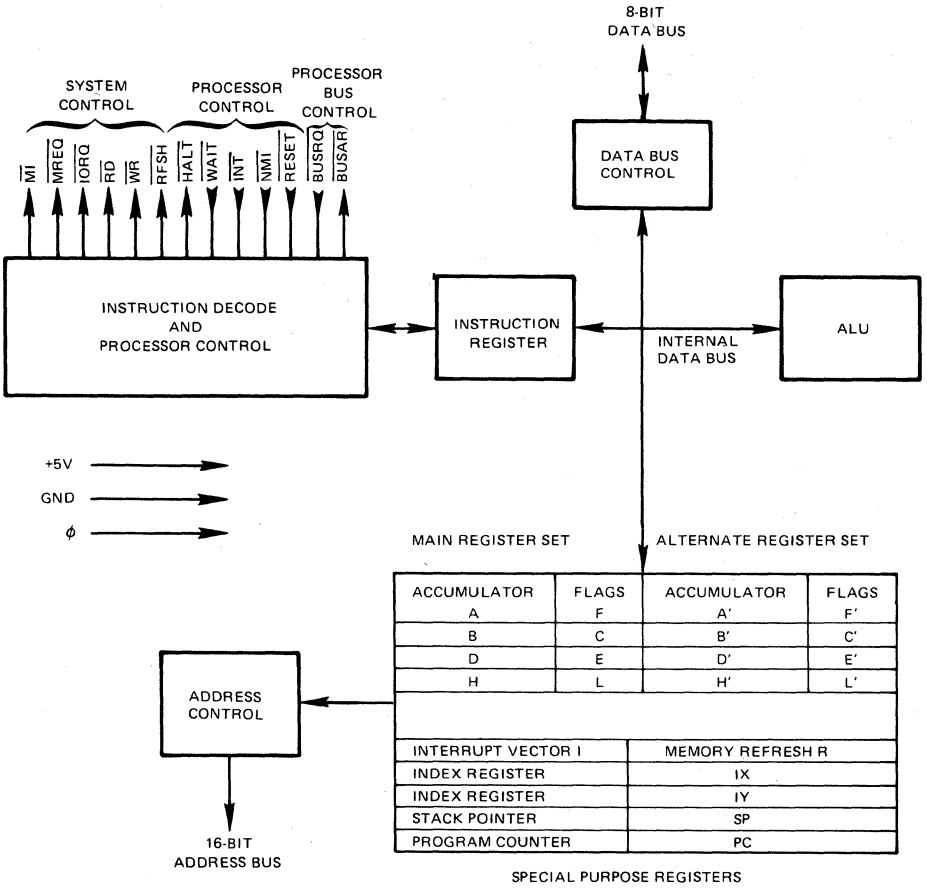
PIN CONFIGURATION



TM:Z80 is a registered trademark of Zilog, Inc.

173 Worcester Street/Wellesley, Massachusetts 02181 Telephone 617/237-1910 TWX: 710-383-1745

BLOCK DIAGRAM



PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
1-5, 30-40	A_0-A_{15}	Address Bus	3-State Output, active high. Pins A_0-A_{15} constitute a 16-bit address bus, which provides the address for memory and I/O device data exchanges. Memory capacity 65,536 bytes. A_0-A_7 is also needed as refresh cycle.
7-10, 12-15	D_0-D_7	Data Bus	3-State input/output, active high. Pins D_0-D_7 compose an 8-bit, bidirectional data bus, used for data exchanges with memory and I/O devices.
27	$\overline{M_1}$	Machine Cycle One	Output, active low. $\overline{M_1}$ indicates that the machine cycle in operation is the op code fetch cycle of an instruction execution.
19	$\overline{MREQ}$	Memory Request	3-State output, active low. $\overline{MREQ}$ indicates that a valid address for a memory read or write operation is held in the address.
20	$\overline{IORQ}$	Input/Output Request	3-State output, active low. The I/O request signal indicates that the lower half of the address bus holds a valid address for an I/O read or write operation. The $\overline{IORQ}$ signal is also used to acknowledge an interrupt command, indicating that an interrupt response vector can be placed on the data bus.
21	$\overline{RD}$	Memory Read	3-State output, active low. $\overline{RD}$ indicates that the processor is requesting data from memory or an I/O device. The memory or I/O device being addressed should use this signal to gate data onto the data bus.

PIN IDENTIFICATION (CONT.)

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
22	$\overline{WR}$	Memory Write	3-State output, active low. The memory write signal indicates that the processor data bus is holding valid data to be stored in the addressed, memory or I/O device.
28	$\overline{RFSH}$	Refresh	Output, active low. $\overline{RFSH}$ indicates that a refresh address for dynamic memories is being held in the lower 7-bits of the address bus. The $\overline{MREQ}$ signal should be used to implement a refresh read to all dynamic memories.
18	$\overline{HALT}$	Halt State	Output, active low. $\overline{HALT}$ indicates that the processor has executed a HALT software instruction, and will not resume operation until either a non-maskable or a maskable (with mask enabled) interrupt has been implemented. The processor will execute NOP's while halted, to maintain memory refresh activity.
24	$\overline{WAIT}$	Wait	Input, active low. $\overline{WAIT}$ indicates to the processor that the memory or I/O devices being addressed are not ready for a data transfer. As long as this signal is active, the processor will reenter wait states.
16	$\overline{INT}$	Interrupt Request	Input, active low. The $\overline{INT}$ signal is produced by I/O devices. The request will be honored upon completion of the current instruction, if the interrupt enable flip-flop (IFF) is enabled by the internal software. There are three modes of interrupt response. Mode 0 is identical to 8080 interrupt response mode. The Mode 1 response is a restart location at 0038_H. Mode 2 is for simple vectoring to an interrupt service routine anywhere in memory.
17	$\overline{NMI}$	Non-Maskable Interrupt	Input, active low. The non-maskable interrupt has a higher priority than $\overline{INT}$. It is always acknowledged at the end of the current instruction, regardless of the status of the interrupt enable flip-flop. When the $\overline{NMI}$ signal is given, the μPD780 processor automatically restarts to location 0066_H.
26	$\overline{RESET}$	Reset	Input, active low. The $\overline{RESET}$ signal causes the processor to reset the interrupt enable flip-flop (IFF), clear PC and I and R registers, and set interrupt to 8080A mode. During the reset time, the address bus and data bus go to a state of high impedance, and all control output signals become inactive, after which processing continues at 0000H.
25	$\overline{BUSRQ}$	Bus Request	Input, active low. $\overline{BUSRQ}$ has a higher priority than $\overline{NMI}$, and is always honored at the end of the current machine cycle. It is used to allow other devices to take control over the processor address bus, data bus signals; by requesting that they go to a state of high impedance.
23	$\overline{BUSAK}$	Bus Acknowledge	Output, active low. $\overline{BUSAK}$ is used to inform the requesting device that the processor address bus, data bus and 3-state control bus signals have entered a state of high impedance, and the external device can now take control of these signals.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Voltage on any Pin	−0.3 to +7 Volts ①
Power Dissipation	1.5W

Note: ① With Respect to Ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 5% unless otherwise specified.

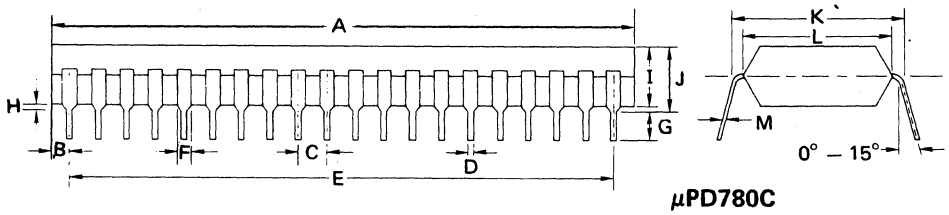
PARAMETER		SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Input Low Voltage		V_{ILC}	−0.3		0.45	V	
Clock Input High Voltage		V_{IHC}	V_{CC}−0.2		V_{CC}	V	
Input Low Voltage		V_{IL}	−0.3		0.8	V	
Input High Voltage		V_{IH}	2.0		V_{CC}	V	
Output Low Voltage		V_{OL}			0.4	V	I_{OL} = 1.8 mA
Output High Voltage		V_{OH}	2.4			V	I_{OH} = −250 μA
Power Supply Current	μPD780	I_{CC}			150	mA	t_c = 400 ns
	μPD780-1	I_{CC}		90	200	mA	t_c = 250 ns
Input Leakage Current		I_{LI}			10	μA	V_{IN} = 0 to V_{CC}
Tri-State Output Leakage Current in Float		I_{LOH}			10	μA	V_{OUT} = 2.4 to V_{CC}
Tri-State Output Leakage Current in Float		I_{LOL}			−10	μA	V_{OUT} = 0.4 V
Data Bus Leakage Current in Input Mode		I_{LD}			±10	μA	$0 \leqslant V_{IN} \leqslant V_{CC}$

CAPACITANCE

T_a = 25°C

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Capacitance	C_ϕ			35	pF	f_c = 1 MHz
Input Capacitance	C_{IN}			5	pF	Unmeasured Pins
Output Capacitance	C_{OUT}			10	pF	Returned to Ground

PACKAGE OUTLINES
μPD780C/D



μPD780C
μPD780C-1
(Plastic)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

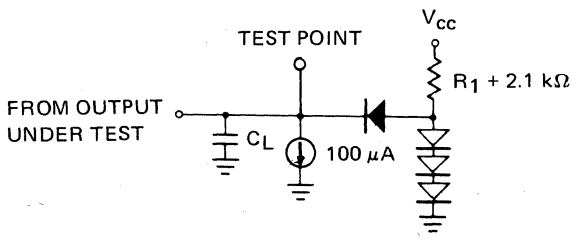
AC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 5%, unless otherwise specified.

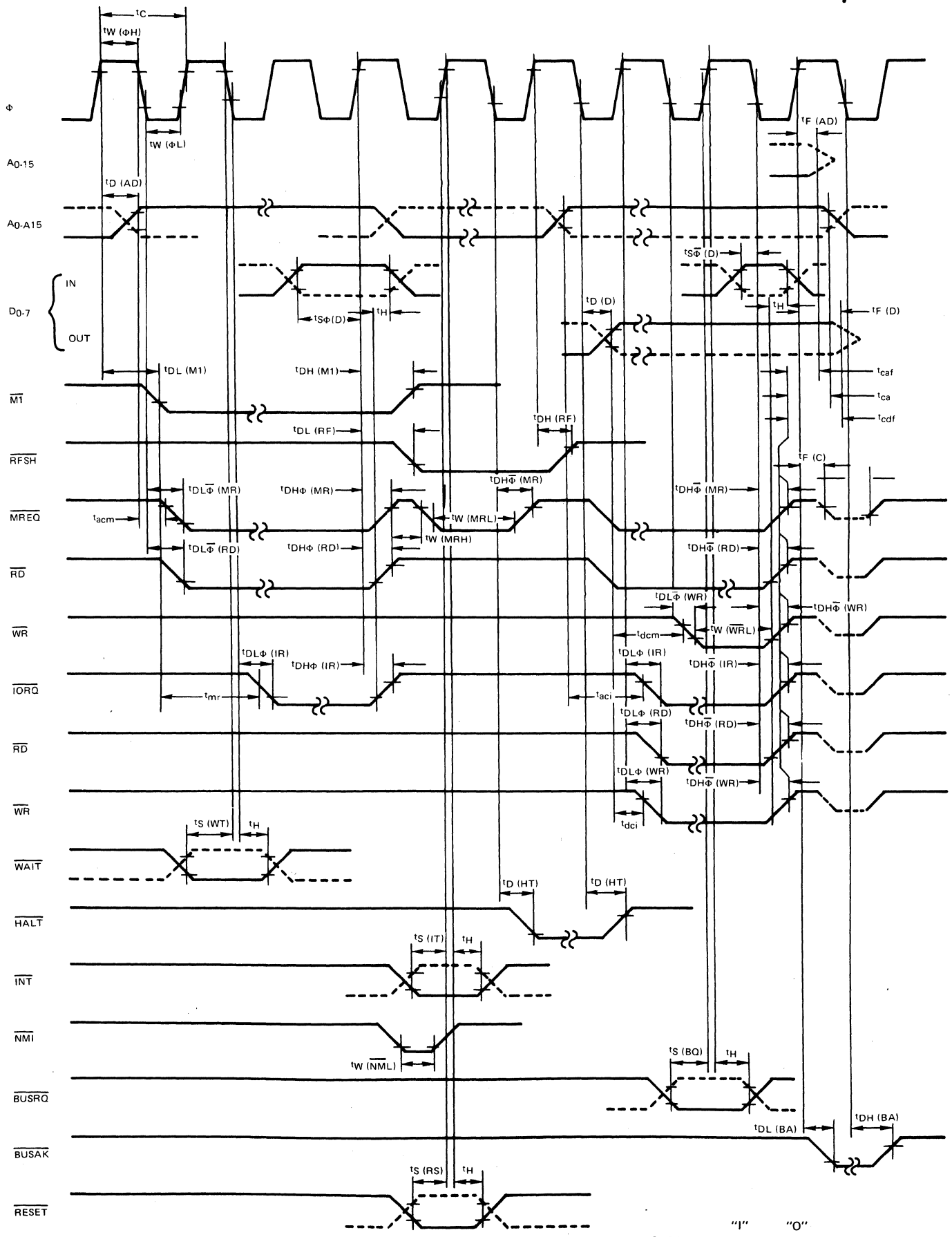
PARAMETER	SYMBOL	LIMITS μPD780 MIN	LIMITS μPD780 MAX	LIMITS μPD780-1 MIN	LIMITS μPD780-1 MAX	UNIT	TEST CONDITIONS
Clock Period	t_c	0.4	⑫	0.25	⑫	μs	
Clock Pulse Width, Clock High	$t_{w(\Phi H)}$	180		110		ns	
Clock Pulse Width, Clock Low	$t_{w(\Phi L)}$	180	2000	110	2000	ns	
Clock Rise and Fall Time	$t_{r,f}$		30		30	ns	
Address Output Delay	$t_{D(AD)}$		145		110	ns	
Delay to Float	$t_{F(AD)}$		110		90	ns	
Address Stable Prior to $\overline{MREQ}$ (Memory Cycle)	t_{acm}	①		①		ns	C_L = 50 pF
Address Stable Prior to $\overline{IORQ}$, $\overline{RD}$ or $\overline{WR}$ (I/O Cycle)	t_{aci}	②		②		ns	
Address Stable from $\overline{RD}$ or $\overline{WR}$	t_{ca}	③		③		ns	
Address Stable from $\overline{RD}$ or $\overline{WR}$ During Float	t_{caf}	④		④		ns	
Data Output Delay	$t_{D(D)}$		230		150	ns	
Delay to Float During Write Cycle	$t_{F(D)}$		90		90	ns	
Data Setup Time to Rising Edge of Clock During M1 Cycle	$t_{S\Phi(D)}$	50		35		ns	
Data Setup Time to Falling Edge of Clock During M2 to M5 Cycles	$t_{S\overline{\Phi}(D)}$	60		50		ns	C_L = 200 pF
Data Stable Prior to $\overline{WR}$ (Memory Cycle)	t_{dcm}	⑤		⑤		ns	
Data Stable Prior to $\overline{WR}$ (I/O Cycle)	t_{dci}	⑥		⑥		ns	
Data Stable from $\overline{WR}$	t_{cdf}	⑦		⑦		ns	
Any Hold Time for Setup Time	t_H	0			0	ns	
$\overline{MREQ}$ Delay from Falling Edge of Clock to $\overline{MREQ}$ Low	$t_{DL\overline{\Phi}(MR)}$		100		85	ns	
$\overline{MREQ}$ Delay from Rising Edge of Clock to $\overline{MREQ}$ High	$t_{DH\Phi(MR)}$		100		85	ns	
$\overline{MREQ}$ Delay from Falling Edge of Clock to $\overline{MREQ}$ High	$t_{DH\overline{\Phi}(MR)}$		100		85	ns	
Pulse Width, $\overline{MREQ}$ Low	$t_{w(\overline{MRL})}$	⑧		⑧		ns	
Pulse Width, $\overline{MREQ}$ High	$t_{w(\overline{MRH})}$	⑨		⑨		ns	
$\overline{IORQ}$ Delay from Rising Edge of Clock to $\overline{IORQ}$ Low	$t_{DL\Phi(IR)}$		90		75	ns	
$\overline{IORQ}$ Delay from Falling Edge of Clock to $\overline{IORQ}$ Low	$t_{DL\overline{\Phi}(IR)}$		110		85	ns	
$\overline{IORQ}$ Delay from Rising Edge of Clock to $\overline{IORQ}$ High	$t_{DH\Phi(IR)}$		100		85	ns	
$\overline{IORQ}$ Delay from Falling Edge of Clock to $\overline{IORQ}$ High	$t_{DH\overline{\Phi}(IR)}$		110		85	ns	C_L = 50 pF
$\overline{RD}$ Delay from Rising Edge of Clock to $\overline{RD}$ Low	$t_{DL\Phi(RD)}$		100		85	ns	
$\overline{RD}$ Delay from Falling Edge of Clock to $\overline{RD}$ Low	$t_{DL\overline{\Phi}(RD)}$		130		95	ns	
$\overline{RD}$ Delay from Rising Edge of Clock to $\overline{RD}$ High	$t_{DH\Phi(RD)}$		100		85	ns	
$\overline{RD}$ Delay from Falling Edge of Clock to $\overline{RD}$ High	$t_{DH\overline{\Phi}(RD)}$		110		85	ns	
$\overline{WR}$ Delay from Rising Edge of Clock to $\overline{WR}$ Low	$t_{DL\Phi(WR)}$		80		65	ns	
$\overline{WR}$ Delay from Falling Edge of Clock to $\overline{WR}$ Low	$t_{DL\overline{\Phi}(WR)}$		90		80	ns	
$\overline{WR}$ Delay from Falling Edge of Clock to $\overline{WR}$ High	$t_{DH\Phi(WR)}$		100		80	ns	
Pulse Width to $\overline{WR}$ Low	$t_{w(\overline{WRL})}$	⑩		⑩		ns	
$\overline{M1}$ Delay from Rising Edge of Clock to $\overline{M1}$ Low	$t_{DL(M1)}$		130		100	ns	C_L = 30 pF
$\overline{M1}$ Delay from Rising Edge of Clock to $\overline{M1}$ High	$t_{DH(M1)}$		130		100	ns	
$\overline{RFSH}$ Delay from Rising Edge of Clock to $\overline{RFSH}$ Low	$t_{DL(RF)}$		180		130	ns	
$\overline{RFSH}$ Delay from Rising Edge of Clock to $\overline{RFSH}$ High	$t_{DH(RF)}$		150		120	ns	
$\overline{WAIT}$ Setup Time to Falling Edge of Clock	$t_{s(WT)}$	70		70		ns	
$\overline{HALT}$ Delay Time from Falling Edge of Clock	$t_{D(HT)}$		300		300	ns	C_L = 50 pF
$\overline{INT}$ Setup Time to Rising Edge of Clock	$t_{s(IT)}$	80		80		ns	
Pulse Width, $\overline{NMI}$ Low	$t_{w(\overline{NML})}$	80		80		ns	
$\overline{BUSRQ}$ Setup Time to Rising Edge of Clock	$t_{s(BQ)}$	80		50		ns	
$\overline{BUSAK}$ Delay from Rising Edge of Clock to $\overline{BUSAK}$ Low	$t_{DL(BA)}$		120		100	ns	C_L = 50 pF
$\overline{BUSAK}$ Delay from Falling Edge of Clock to $\overline{BUSAK}$ High	$t_{DH(BA)}$		110		100	ns	
$\overline{RESET}$ Setup Time to Rising Edge of Clock	$t_{s(RS)}$	90		60		ns	
Delay to Float ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$ and $\overline{WR}$)	$t_{F(C)}$		100		80	ns	
$\overline{M1}$ Stable Prior to $\overline{IORQ}$ (Interrupt Ack.)	t_{mr}	⑪		⑪		ns	

Notes:
① $t_{acm} = t_{w(\Phi H)} + t_f - 65$ (75)*
② $t_{aci} = t_c - 70$ (80)*
③ $t_{ca} = t_{w(\Phi L)} + t_r - 50$ (40)*
④ $t_{caf} = t_{w(\Phi L)} + t_r - 45$ (60)*
⑤ $t_{dcm} = t_c - 170$ (210)*
⑥ $t_{dci} = t_{w(\Phi L)} + t_r - 170$ (210)*
⑦ $t_{cdf} = t_{w(\Phi L)} + t_r - 70$ (80)*
⑧ $t_{w(\overline{MRL})} = t_c - 30$ (40)*
⑨ $t_{w(\overline{MRH})} = t_{w(\Phi H)} + t_f - 20$ (30)*
⑩ $t_{w(\overline{WR})} = t_c - 30$ (40)*
⑪ $t_{mr} = 2t_c + t_{w(\Phi H)} + t_f - 65$ (80)*
⑫ $t_c = t_{w(\Phi H)} + t_{w(\Phi L)} + t_r + t_f$

*These values apply to the μPD780.



LOAD CIRCUIT FOR OUTPUT

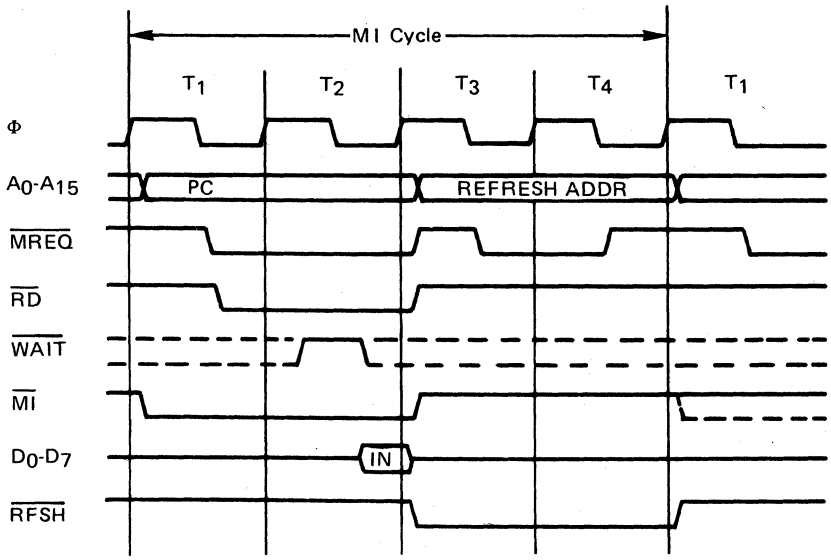


	"I"	"O"
CLOCK	4.2V	0.8V
OUTPUT	2.0V	0.8V
INPUT	2.0V	0.8V
FLOAT	ΔV	±0.5V

Note: ① Timing measurements are made at the following voltages unless otherwise specified:

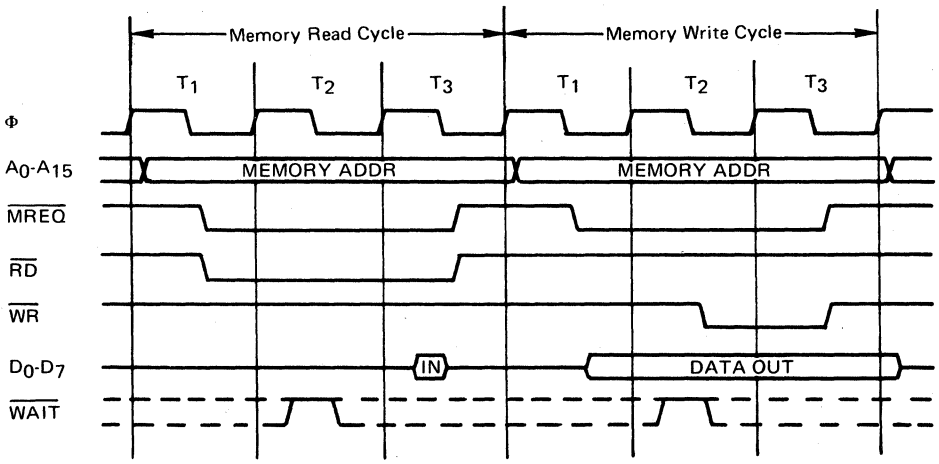
Instruction Op Code Fetch

The contents of the program counter (PC) are placed on the address bus at the start of the cycle. $\overline{MREQ}$ goes active one-half clock cycle later, and the falling edge of this signal can be used directly as a chip enable to dynamic memories. The memory data should be enabled onto the processor data bus when $\overline{RD}$ goes active. The processor takes data with the rising edge of the clock state T_3. The processor internally decodes and executes the instruction, while clock states T_3 and T_4 of the fetch cycle are used to refresh dynamic memories. The refresh control signal $\overline{RFSH}$ indicates that a refresh read should be done to all dynamic memories.



Memory Read or Write Cycles

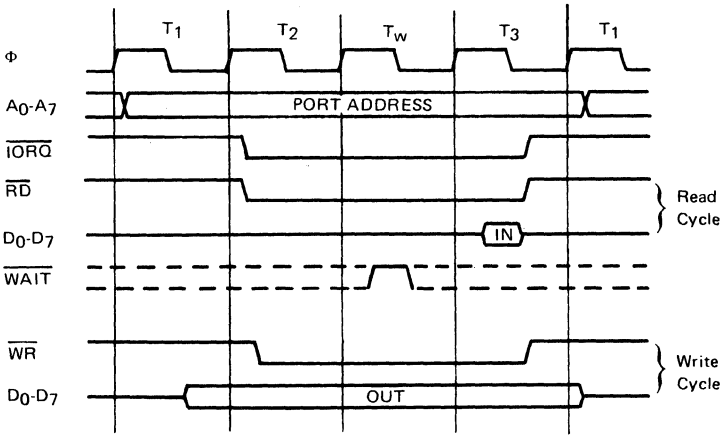
This diagram illustrates the timing of memory read or write cycles other than an op code fetch (M_1 cycle). The function of the $\overline{MREQ}$ and $\overline{RD}$ signals is exactly the same as in the op code fetch cycle. When a memory write cycle is implemented, the $\overline{MREQ}$ becomes active and is used directly as a chip enable for dynamic memories, when the address bus is stable. The $\overline{WR}$ line is used directly as a R/W pulse to any type of semiconductor memory, and is active when data on the data bus is stable.



TIMING WAVEFORMS (CONT.)

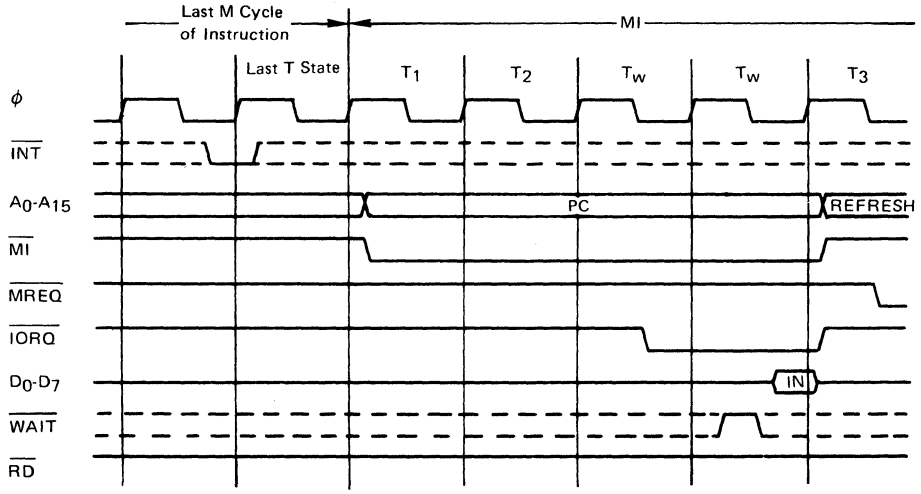
Input or Output Cycles

This illustrates the timing for an I/O read or I/O write operation. A single wait state (T_W) is automatically inserted in I/O operations to allow sufficient time for an I/O port to decode its address and activate the $\overline{WAIT}$ line, if necessary.



Interrupt Request/Acknowledge Cycle

The processor samples the interrupt signal with the rising edge of the last clock at the end of any instruction. A special M_1 cycle is started when an interrupt is accepted. During the M_1 cycle, the $\overline{IORQ}$ (instead of $\overline{MREQ}$) signal becomes active, indicating that the interrupting device can put an 8-bit vector on the data bus. Two wait states (T_W) are automatically added to this cycle. This makes it easy to implement a ripple priority interrupt scheme.



INSTRUCTION SET

The following summary shows the assembly language mnemonic and the symbolic operation performed by the instructions of the μPD780 and μPD780-1 processors. The instructions are divided into 16 categories:

Miscellaneous Group	8-Bit Loads
Rotates and Shifts	16-Bit Loads
Bit Set, Reset and Test	Exchanges
Input and Output	Memory Block Moves
Jumps	Memory Block Searches
Calls	8-Bit Arithmetic and Logic
Restarts	16-Bit Arithmetic
Returns	General Purpose Accumulator and Flag Operations

The addressing Modes include combinations of the following:

Indexed	Immediate
Register	Immediate Extended
Implied	Modified Page Zero
Register Indirect	Relative
Bit	Extended

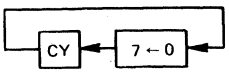
INSTRUCTION SET TABLE

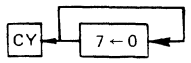
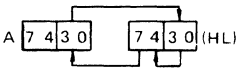
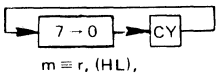
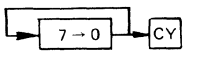
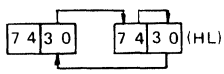
MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
ADC HL, ss	HL ← HL + ss + CY	Add with carry reg. pair ss to HL	1	11	↕	↕	V	↕	0	X	11 101 101 Ⓐ 01 ss1 010
ADC A, r	A ← A + r + CY	Add with carry Reg. r to ACC	1	4	↕	↕	V	↕	0	↕	10 001 rrr Ⓑ
ADC A,n	A ← A + n + CY	Add with carry value n to ACC		7	↕	↕	V	↕	0	↕	11 001 110 nn nnn nnn
ADC A, (HL)	A ← A + (HL) + CY	Add with carry loc. (HL) to ACC		7	↕	↕	V	↕	0	↕	10 001 110
ADC A, (IX + d)	A ← A + (IX + d) + CY	Add with carry loc. (IX + d) to ACC		19	↕	↕	V	↕	0	↕	11 011 101 10 001 110 dd ddd ddd
ADC A, (IY + d)	A ← A + (IY + d) + CY	Add with carry loc. (IY + d) to ACC		19	↕	↕	V	↕	0	↕	11 111 101 10 001 110 dd ddd ddd
ADD A, n	A ← A + n	Add value n to ACC	2	7	↕	↕	V	↕	0	↕	11 000 110 nn nnn nnn
ADD A, r	A ← A + r	Add Reg. r to ACC	1	4	↕	↕	V	↕	0	↕	10 000 rrr Ⓑ
ADD A, (HL)	A ← A + (HL)	Add location (HL) to ACC	1	7	↕	↕	V	↕	0	↕	10 000 110
ADD A, (IX + d)	A ← A + (IX + d)	Add location (IX + d) to ACC	3	19	↕	↕	V	↕	0	↕	11 011 101 10 000 110 dd ddd ddd
ADD A, (IY + d)	A ← A + (IY + d)	Add location (IY + d) to ACC	3	19	↕	↕	V	↕	0	↕	11 111 101 10 000 110 dd ddd ddd
ADD HL, ss	HL ← HL + ss	Add Reg. pair ss to HL	1	11	↕	•	•	•	0	X	00 ss1 001 Ⓐ
ADD IX, pp	IX ← IX + pp	Add Reg. pair pp to IX	2	15	↕	•	•	•	0	X	11 011 101 Ⓒ 00 pp1 001
ADD IY, rr	IY ← IY + rr	Add Reg. pair rr to IY	2	15	↕	•	•	•	0	X	11 111 101 Ⓓ 00 rr1 001
AND r	A ← AΛr	Logical 'AND' of Reg. r Λ ACC		4	0	↕	P	↕	0	↕	10 100 rrr Ⓑ
AND n	A ← AΛn	Logical 'AND' of value n Λ ACC		7	0	↕	P	↕	0	↕	11 100 110 nn nnn nnn
AND (HL)	A ← AΛ(HL)	Logical 'AND' of loc. (HL) Λ ACC		7	0	↕	P	↕	0	↕	10 100 110
AND (IX + d)	A ←AΛ(IX + d)	Logical 'AND' of loc. (IX + d) Λ ACC		19	0	↕	P	↕	0	↕	11 011 101 10 100 110 dd ddd ddd
AND (IY + d)	A ←AΛ(IY + d)	Logical 'AND' of loc. (IY + d) Λ ACC		19	0	↕	P	↕	0	↕	11 111 101 10 100 110 dd ddd ddd
BIT b, (HL)	Z ← $\overline{(HL)}_b$	Test BIT b of location (HL)	2	12	•	↕	X	X	0	1	11 001 011 Ⓔ 01 bbb 110
BIT b, (IX + d)	Z ← $\overline{(IX + d)}_b$	Test BIT b at location (IX + d)	4	20	•	↕	X	X	0	1	11 011 101 Ⓔ 11 001 011 dd ddd ddd 01 bbb 110
BIT b, (IY + d)	Z ← $\overline{(IY + d)}_b$	Test BIT b at location (IY + d)	4	20	•	↕	X	X	0	1	11 111 101 Ⓔ 11 001 011 dd ddd ddd 01 bbb 110
BIT b, r	Z ← $\overline{r}_b$	Test BIT of Reg. r	2	8	•	↕	X	X	0	1	11 001 011 ⒷⒺ 01 bbb rrr
CALL cc, nn	If condition cc false continue, else same as CALL nn	Call subroutine at location nn if condition cc is true	3	10	•	•	○	•	•	•	11 ←cc→ 100 Ⓗ nn nnn nnn nn nnn nnn
CALL nn	(SP − 1) ← PC_H (SP − 2) ← PC_L PC ← nn	Unconditional call subroutine at location nn	3	17	•	•	•	•	•	•	11 001 101 nn nnn nnn nn nnn nnn
CCF	CY ← CY	Complement carry flag	1	4	↕	•	•	•	0	X	00 111 111
CP r	A − r	Compare Reg. r with ACC		4	↕	↕	V	↕	1	↕	10 111 rrr Ⓑ
CP n	A − n	Compare value n with ACC		7	↕	↕	V	↕	1	↕	11 111 110 nn nnn nnn
CP (HL)	A − (HL)	Compare loc. (HL) with ACC		7	↕	↕	V	↕	1	↕	10 111 110
CP (IX + d)	A − (IX + d)	Compare loc. (IX + d) with ACC		19	↕	↕	V	↕	1	↕	11 011 101 10 111 110 dd ddd ddd
CP (IY + d)		Compare loc. (IY + d) with ACC		19	↕	↕	V	↕	1	↕	11 111 101 10 111 110 dd ddd ddd
CPD	A − (HL) HL ← HL −1 BC ← BC − 1	Compare location (HL) and ACC, decrement HL and BC	2	16	•	↕②	↕①	↕	1	↕	11 101 101 10 101 001
CPDR	A − (HL) HL ← HL − 1 BC ← BC − 1 until A = (HL) or BC = 0	Compare location (HL) and ACC, decrement HL and BC, repeat until BC = 0	2	21 if BC = 0 and A ≠ (HL) 16 if BC = 0 or A = (HL)	•	↕②	↕①	↕	1	↕	11 101 101 10 111 001

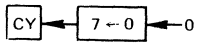
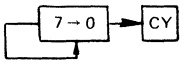
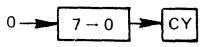
MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
CPI	A – (HL) HL ← HL + 1 BC ← BC – 1	Compare location (HL) and ACC, increment HL and decrement BC	2	16	•	‡②	‡①	‡	1	‡	11 101 101 10 100 001
CPIR	A – (HL) HL ← HL + 1 BC ← BC – 1 until A = (HL) or BC = 0	Compare location (HL) and ACC, increment HL, decrement BC Repeat until BC = C	2	21 if BC = 0 and A ≠ (HL) 16 if BC = 0 or A = (HL)	•	‡②	‡①	‡	1	‡	11 101 101 10 110 001
CPL	A ← A	Complement ACC (1's comp.)	1	4	•	•	•	•	1	1	00 101 111
DAA		Decimal adjust ACC	1	4	‡	‡	P	‡	•	‡	00 100 111
DEC r	r ← r – 1	Decrement Reg. r		4	•	‡	V	‡	1	‡	00 rrr 101Ⓑ
DEC (HL)	(HL) ← (HL) – 1	Decrement loc. (HL)		11	•	‡	V	‡	1	‡	00 110 101
DEC (IX + d)	(IX + d) ← (IX + d) – 1	Decrement loc. (IX + d)		23	•	‡	V	‡	1	‡	11 011 101 00 110 101 dd ddd ddd
DEC (IY + d)	(IY + d) ← (IY + d) – 1	Decrement loc. (IY + d)		23	•	‡	V	‡	1	‡	11 111 101 00 110 101 dd ddd ddd
DEC IX	IX ← IX – 1	Decrement IX	2	10	•	•	•	•	•	•	11 011 101 00 101 011
DEC IY	IY ← IY – 1	Decrement IY	2	10	•	•	•	•	•	•	11 111 101 00 101 011
DEC ss	ss ← ss – 1	Decrement Reg. pair ss	1	6	•	•	•	•	•	•	00 ss1 011Ⓐ
DI	IFF ← 0	Disable interrupts	1	4	•	•	•	•	•	•	11 110 011
DJNZ, e	B ← B – 1 if B = 0 continue if B ≠ 0 PC ← PC + e	Decrement B and jump relative if B = 0	2	8	•	•	•	•	•	•	00 010 000 ◄—e-2—►
EI	IFF ← 1	Enable interrupts	1	4	•	•	•	•	•	•	11 111 011
EX (SP), HL	H ↔ (SP + 1) L ↔ (SP)	Exchange the location (SP) and HL	1	19	•	•	•	•	•	•	11 100 011
EX (SP), IX	IX_H ↔ (SP + 1) IX_L ↔ (SP)	Exchange the location (SP) and IX	2	23	•	•	•	•	•	•	11 011 101 11 100 011
EX (SP), IY	IY_H ↔ (SP + 1) IY_L ↔ (SP)	Exchange the location (SP) and IY	2	23	•	•	•	•	•	•	11 111 101 11 100 011
EX AF, AF'	AF ↔ AF'	Exchange the contents of AF AF	1	4	•	•	•	•	•	•	00 001 000
EX DE, HL	DE ↔ HL	Exchange the contents of DE and HL	1	4	•	•	•	•	•	•	11 101 011
EXX	BC ↔ BC' DE ↔ DE' HL ↔ HL'	Exchange the contents of BC, DE, HL with contents of BC', DE', HL', respectively	1	4	•	•	•	•	•	•	11 011 001
HALT	Processor Halted	HALT (wait for interrupt or reset)	1	4	•	•	•	•	•	•	01 110 110
IM 0		Set Interrupt mode 0	2	8	•	•	•	•	•	•	11 101 101 01 000 110
IM 1		Set Interrupt mode 1	2	8	•	•	•	•	•	•	11 101 101 01 010 110
IM 2		Set Interrupt mode 2	2	8	•	•	•	•	•	•	11 101 101 01 011 110
IN A, (n)	A ← (n)	Load ACC with input from device n	2	11	•	•	•	•	•	•	11 011 011 nn nnn nnn
IN r, (C)	r ← (C)	Load Reg. r with input from device (C)	2	12	•	‡	P	‡	0	‡	11 101 101Ⓘ 01 rrr 000
INC (HL)	(HL) ← (HL) + 1	Increment location (HL)	1	11	•	‡	V	‡	0	‡	00 110 100
INC IX	IX ← IX + 1	Increment IX	2	10	•	•	•	•	•	•	11 011 101 00 100 011
INC (IX + d)	(IX + d) ← (IX + d) + 1	Increment location (IX + d)	3	23	•	‡	V	‡	0	‡	11 011 101 00 110 100 dd ddd ddd
INC IY	IY ← IY + 1	Increment IY	2	10	•	•	•	•	•	•	11 111 101 00 100 011
INC (IY + d)	(IY + d) ← (IY + d) + 1	Increment location (IY + d)	3	23	•	‡	V	‡	0	‡	11 111 101 00 110 100 dd ddd ddd
INC r	r ← r + 1	Increment Reg. r	1	4	•	‡	V	‡	0	‡	00 rrr 100Ⓑ
INC ss	ss ← ss + 1	Increment Reg. pair ss	1	6	•	•	•	•	•	•	00 ss0 011Ⓐ
IND	(HL) ← (C) B ← B – 1 HL ← HL – 1	Load location (HL) with input from port (C), decrement HL and B	2	16	•	‡③	X	X	1	X	11 101 101 10 101 010

MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
INDR	(HL) ← (C) B ← B – 1 HL ← HL – 1 until B = 0	Load location (HL) with input from port (C), decrement HL and decrement B, repeat until B = 0	2	21	•	1	X	X	1	X	11 101 101 10 111 010
INI	(HL) ← (C) B ← B – 1 HL ← HL + 1	Load location (HL) with input from port (C); and increment HL and decrement B	2	16	•	↕③	X	X	1	X	11 101 101 10 100 010
INIR	(HL) ← (C) B ← B – 1 HL ← HL + 1 until B = 0	Load location (HL) with input from port (C), increment HL and decrement B, repeat until B = 0	2	21	•	1	X	X	1	X	11 101 101 10 110 010
JP (HL)	PC ← HL	Unconditional jump to (HL)	1	4	•	•	•	•	•	•	11 101 001
JP (IX)	PC ← IX	Unconditional jump to (IX)	2	8	•	•	•	•	•	•	11 011 101 11 101 001
JP (IY)	PC ← IY	Unconditional jump to (IY)	2	8	•	•	•	•	•	•	11 111 101 11 101 001
JP cc, nn	If cc true PC ← nn else continue	Jump to location nn if condition cc is true	3	10	•	•	•	•	•	•	11 ←cc→ 010Ⓗ nn nnn nnn nn nnn nnn
JP nn	PC ← nn	Unconditional jump to location nn	3	10	•	•	•	•	•	•	11 000 011 nn nnn nnn nn nnn nnn
JR C, e	If C = 0 continue If C = 1 PC ← PC + e	Jump relative to PC + e, if carry = 1	2	7 if condition met. 12, if not	•	•	•	•	•	•	00 111 000 ◄— e-2 —►
JR e	PC ← PC + e	Unconditional jump relative to PC + e	2	12	•	•	•	•	•	•	00 011 000 ◄— e-2 —►
JR NC, e	If C = 1 continue If C = 0 PC ← PC + e	Jump relative to PC + e if carry = 0	2	7	•	•	•	•	•	•	00 110 000 ◄— e-2 —►
JR NZ, e	If Z = 1 continue	Jump relative to PC + e if non-zero (Z = 0)	2	7	•	•	•	•	•	•	00 100 000 ◄— e-2 —►
JR Z, e	If Z = 0 continue	Jump relative to PC + e if zero (Z = 1)	2	7	•	•	•	•	•	•	00 101 000 ◄— e-2 —►
LD A, (BC)	A ← (BC)	Load ACC with location (BC)	1	7	•	•	•	•	•	•	00 001 010
LD A, (DE)	A ← (DE)	Load ACC with location (DE)	1	7	•	•	•	•	•	•	00 011 010
LD A, I	A ← I	Load ACC with I	2	9	•	↕	IFF	↕	0	0	11 101 101 01 010 111
LD A, (nn)	A ← (nn)	Load ACC with location nn	3	13	•	•	•	•	•	•	00 111 010 nn nnn nnn nn nnn nnn
LD A, R	A ← R	Load ACC with Reg. R	2	9	•	↕	IFF	↕	0	0	11 101 101 01 011 111
LD (BC), A	(BC) ← A	Load location (BC) with ACC	1	7	•	•	•	•	•	•	00 000 010
LD (DE), A	(DE) ← A	Load location (DE) with ACC	1	7	•	•	•	•	•	•	00 010 010
LD (HL), n	(HL) ← n	Load location (HL) with value n	2	10	•	•	•	•	•	•	00 110 110 nn nnn nnn
LD ss, nn	ss ← nn	Load Reg. pair ss with value nn	4	20	•	•	•	•	•	•	00 ss0 001Ⓐ nn nnn nnn nn nnn nnn
LD HL, (nn)	H ← (nn + 1) L ← (nn)	Load HL with location (nn)	3	16	•	•	•	•	•	•	00 101 010 nn nnn nnn nn nnn nnn
LD (HL), r	(HL) ← r	Load location (HL) with Reg. r	1	7	•	•	•	•	•	•	01 110 rrrⒷ
LD I, A	I ← A	Load I with ACC	2	9	•	•	•	•	•	•	11 101 101 01 000 111
LD IX, nn	IX ← nn	Load IX with value nn	4	19	•	•	•	•	•	•	11 011 101 00 100 001 nn nnn nnn nn nnn nnn
LD IX, (nn)	IX_H ← (nn + 1) IX_L ← (nn)	Load IX with location (nn)	4	20	•	•	•	•	•	•	11 011 101 00 101 010 nn nnn nnn nn nnn nnn
LD (IX + d), n	(IX + d) ← n	Load location (IX + d) with value n	4	19	•	•	•	•	•	•	11 011 101 00 110 110 dd ddd ddd nn nnn nnn
LD (IX + d), r	(IX + d) ← r	Load location (IX + d) with Reg. r	3	19	•	•	•	•	•	•	11 011 101Ⓑ 01 110 rrr dd ddd ddd

MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
LD IY, nn	$IY \leftarrow nn$	Load IY with value nn	4	14	•	•	•	•	•	•	11 111 101 00 100 001 nn nnn nnn nn nnn nnn
LD IY, (nn)	$IY_H \leftarrow (nn + 1)$ $IY_L \leftarrow (nn)$	Load IY with location (nn)	4	20	•	•	•	•	•	•	11 111 101 00 101 010 nn nnn nnn nn nnn nnn
LD ss, (nn)	$ss_H \leftarrow (nn + 1)$ $ss_L \leftarrow (nn)$	Load Reg. pair dd with location (nn)	4	20	•	•	•	•	•	•	11 101 101 Ⓐ 01 ss1 011 nn nnn nnn nn nnn nnn
LD (IY + d), n	$(IY + d) \leftarrow n$	Load (IY + d) with value n	4	19	•	•	•	•	•	•	11 111 101 00 110 110 dd ddd ddd nn nnn nnn
LD (IY + d), r	$(IY + d) \leftarrow r$	Load location (IY + d) with Reg. r	3	19	•	•	•	•	•	•	11 111 101 Ⓑ 01 110 rrr dd ddd ddd
LD (nn), A	$(nn) \leftarrow A$	Load location (nn) with ACC	3	13	•	•	•	•	•	•	00 110 010 nn nnn nnn nn nnn nnn
LD (nn), ss	$(nn + 1) \leftarrow ss_H$ $(nn) \leftarrow ss_L$	Load location (nn) with Reg. pair dd	4	20	•	•	•	•	•	•	11 101 101 Ⓐ 01 ss0 011 nn nnn nnn nn nnn nnn
LD (nn), HL	$(nn + 1) \leftarrow H$ $(nn) \leftarrow L$	Load location (nn) with HL	3	16	•	•	•	•	•	•	00 100 010 nn nnn nnn nn nnn nnn
LD (nn), IX	$(nn + 1) \leftarrow IX_H$ $(nn) \leftarrow IX_L$	Load location (nn) with IX	4	20	•	•	•	•	•	•	11 011 101 00 100 010 nn nnn nnn nn nnn nnn
LD (nn), IY	$(nn + 1) \leftarrow IY_H$ $(nn) \leftarrow IY_L$	Load location (nn) with IY	4	20	•	•	•	•	•	•	11 111 101 00 100 010 nn nnn nnn nn nnn nnn
LD R, A	$R \leftarrow A$	Load R with ACC	2	9	•	•	•	•	•	•	11 101 101 01 001 111
LD r, (HL)	$r \leftarrow (HL)$	Load Reg. r with location (HL)	1	7	•	•	•	•	•	•	01 rrr 110 Ⓑ
LD r, (IX + d)	$r \leftarrow (IX + d)$	Load Reg. r with location (IX + d)	3	19	•	•	•	•	•	•	11 011 101 Ⓑ 01 rrr 110 dd ddd ddd
LD r, (IY + d)	$r \leftarrow (IY + d)$	Load Reg. r with location (IY + d)	3	19	•	•	•	•	•	•	11 111 101 Ⓑ 01 rrr 110 dd ddd ddd
LD r, n	$r \leftarrow n$	Load Reg. r with value n	2	7	•	•	•	•	•	•	00 rrr 110 Ⓑ nn nnn nnn
LD, r, r'	$r \leftarrow r'$	Load Reg. r with Reg. r	1	4	•	•	•	•	•	•	01 rrr r'r'r' Ⓕ
LD SP, HL	$SP \leftarrow HL$	Load SP with HL	1	6	•	•	•	•	•	•	11 111 001
LD SP, IX	$SP \leftarrow IX$	Load SP with IX	2	10	•	•	•	•	•	•	11 011 101 11 111 001
LD SP, IY	$SP \leftarrow IY$	Load SP with IY	2	10	•	•	•	•	•	•	11 111 101 11 111 001
LDD	$(DE) \leftarrow (HL)$ $DE \leftarrow DE - 1$ $HL \leftarrow HL - 1$ $BC \leftarrow BC - 1$	Load location (DE) with location (HL), decrement DE, HL and BC	2	16	•	•	↕	•	0	0	11 101 101 10 101 000
LDDR	$(DE) \leftarrow (HL)$ $DE \leftarrow DE - 1$ $HL \leftarrow HL - 1$ $BC \leftarrow BC - 1$ until $BC = 0$	Load location (DE) with location (HL)	2	21	•	•	0	•	0	0	11 101 101 10 111 000
LDI	$(DE) \leftarrow (HL)$ $DE \leftarrow DE + 1$ $HL \leftarrow HL + 1$ $BC \leftarrow BC - 1$	Load location (DE) with location (HL), increment DE, HL; decrement BC	2	16	•	•	↕①	•	0	0	11 101 101 10 100 000
LDIR	$(DE) \leftarrow (HL)$ $DE \leftarrow DE + 1$ $HL \leftarrow HL + 1$ $BC \leftarrow BC - 1$ until $BC = 0$	Load location (DE) with location (HL), increment DE, HL; decrement BC and repeat until BC = 0	2	21 if $BC \neq 0$ 16 if $BC = 0$	•	•	0	•	0	0	11 101 101 10 110 000
NEG	$A \leftarrow 0 - A$	Negate ACC (2's complement)	2	8	↕	↕	V	↕	1	↕	11 101 101 01 000 100

MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
NOP		No operation	1	4	•	•	•	•	•	•	00 000 000
OR r	A ← AV r	Logical 'OR' of Reg. r and ACC		4	0	↕	P	↕	0	↕	10 110 rrr Ⓑ
OR n	A ← AV n	Logical 'OR' of value n and ACC		7	•	↕	P	↕	0	↕	11 110 110 nn nnn nnn
OR (HL)	A ← AV (HL)	Logical 'OR' of loc. (HL) and ACC		7	•	↕	P	↕	0	↕	10 110 110
OR (IX + d)	A ← (IX + d)	Logical 'OR' of loc. (IX + d) ∧ ACC		19	•	↕	P	↕	0	↕	11 011 101 10 110 110 dd ddd ddd
OR (IY + d)	A ← AV (IY + d)	Logical 'OR' of loc. (IY + d) ∧ ACC		19	•	↕	P	↕	0	↕	11 111 101 10 110 110 dd ddd ddd
OTDR	(C) ← (HL) B ← B − 1 HL ← HL − 1 until B = 0	Load output port (C) with contents of location (HL), decrement HL and B, repeat until B = 0	2	21 if B ≠ 0 16 if B = C	•	1	X	X	1	X	11 101 101 10 111 011
OTIR	(C) ← (HL) B ← B − 1 HL ← HL + 1 until B = 0	Load output port (C) with location (HL), increment HL, decrement B, repeat until B = 0	2	21 if B ≠ 0 16 if B = C	•	1	X	X	1	X	11 101 101 10 110 011
OUT (C), r	(C) ← r	Load output port (C) with Reg. r	2	12	•	•	•	•	•	•	11 101 101 Ⓑ 01 rrr 001
OUT (n), A	(n) ← A	Load output port (n) with ACC	2	11	•	•	•	•	•	•	11 010 011 nn nnn nnn
OUTD	(C) ← (HL) B ← B − 1 HL ← HL − 1	Load output port (C) with location (HL), increment HL and decrement B	2	16	•	↕③	X	X	1	X	11 101 101 10 101 011
OUTI	(C) ← (HL) B ← B − 1 HL ← HL + 1	Load output port (C) with location (HL), increment HL and decrement B	2	16	•	↕③	X	X	1	X	11 101 101 10 100 011
POP IX	IX_H ← (SP + 1) IX_L ← (SP)	Load IX with top of stack	2	14	•	•	•	•	•	•	11 011 101 11 100 001
POP IY	IY_H ← (SP + 1) IY_L ← (SP)	Load IY with top of stack	2	14	•	•	•	•	•	•	11 111 101 11 100 001
POP qq	qq_H ← (SP + 1) qq_L ← (SP)	Load Reg. pair qq with top of stack	1	10	•	•	•	•	•	•	11 qq0 001 Ⓖ
PUSH IX	(SP − 2) ← IX_L (SP − 1) ← IX_H	Load IX onto stack	2	15	•	•	•	•	•	•	11 011 101 11 100 101
PUSH IY	(SP − 2) ← IY_L (SP − 1) ← IY_H	Load IY onto stack	2	15	•	•	•	•	•	•	11 111 101 11 100 101
PUSH qq	(SP − 2) ← qq_L (SP − 1) ← qq_H	Load Reg. pair qq onto stack	1	11	•	•	•	•	•	•	11 qq0 101 Ⓖ
RES b, r	S_b ← 0	Reset Bit b of Reg. r		8	•	•	•	•	•	•	11 001 011 Ⓑ 10 bbb rrr Ⓔ
RES b, (HL)	S_b ← 0, (HL)	Reset Bit b of loc. (HL)		15	•	•	•	•	•	•	11 001 011 10 bbb 110
RES b, (IX + d)	S_b ← 0, (IX + d)	Reset Bit b of loc. (IX + d)		23	•	•	•	•	•	•	11 011 101 11 001 011 dd ddd ddd 10 bbb 110
RES b, (IY + d)	S_b ← 0, (IY + d)	Reset Bit b of loc. (IY + d)		23	•	•	•	•	•	•	11 111 101 11 001 011 dd ddd ddd 10 bbb 110
RET	PC_L ← (SP) PC_H ← (SP + 1)	Return from subroutine	1	10	•	•	•	•	•	•	11 001 001
RET cc	If condition cc is false cont. else (PC_L ← (SP) PC_H ← (SP + 1)	Return from subroutine if condition cc is true	1	5 if CC false 11 if CC true	•	•	•	•	•	•	11 ←cc→ 000 Ⓗ
RETI		Return from interrupt	2	14	•	•	•	•	•	•	11 101 101 01 001 101
RETN		Return from non-maskable interrupt	2	14	•	•	•	•	•	•	11 101 101 01 000 101
RL r		Rotate left through carry Reg. r		2	↕	↕	P	↕	0	0	11 001 011 Ⓑ 00 010 rrr
RL (HL)		Rotate left through carry loc. (HL)		4	↕	↕	P	↕	0	0	11 001 011 00 010 110
RL (IX + d)	 m ≡ r, (HL), (IX + d), (IY + d), A	Rotate left through carry loc. (IX + d)		6	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 010 110
RL (IY + d)		Rotate left through carry loc. (IY + d)		6	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 010 110
RLA		Rotate left ACC through carry	1	4	↕	•	•	•	0	0	00 010 111

MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
RLC (HL)		Rotate location (HL) left circular	2	15	↕	↕	P	↕	0	0	11 001 011 00 000 110
RLC (IX + d)		Rotate location (IX + d) left circular	4	23	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 000 110
RLC (IY + d)	 m ≡ r, (HL), (IX + d), (IY + d), A	Rotate location (IY + d) left circular	4	23	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 000 110
RLC r		Rotate Reg. r left circular	2	8	↕	↕	P	↕	0	0	11 001 011 (B) 00 000 r r r
RLCA		Rotate left circular ACC	1	4	↕	•	•	•	0	0	00 000 111
RLD		Rotate digit left and right between ACC and location (HL)	2	18	•	↕	P	↕	0	0	11 101 101 01 101 111
RR r		Rotate right through carry Reg. r		2	↕	↕	P	↕	0	0	11 001 011 (B) 00 011 r r r
RR (HL)		Rotate right through carry loc. (HL)		4	↕	↕	P	↕	0	0	11 001 011 00 011 110
RR (IX + d)		Rotate right through carry loc. (IX + d)		6	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 011 110
RR (IY + d)	 m ≡ r, (HL), (IX + d), (IY + d), A	Rotate right through carry loc. (IY + d)		6	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 011 110
RRA		Rotate right ACC through carry	1	4	↕	•	•	•	0	0	00 011 111
RRC r		Rotate Reg. r right circular		2	↕	↕	P	↕	0	0	11 001 011 (B) 00 001 r r r
RRC (HL)		Rotate loc. (HL) right circular		4	↕	↕	P	↕	0	0	11 001 011 00 001 110
RRC (IX + d)		Rotate loc. (IX + d) right circular		6	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 001 110
RRC (IY + d)	 m ≡ r, (HL), (IX + d), (IY + d), A	Rotate loc. (IY + d) right circular		6	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 001 110
RRCA		Rotate right circular ACC	1	4	↕	•	•	•	0	0	00 001 111
RRD		Rotate digit right and left between ACC and location (HL)	2	18	•	↕	P	↕	0	0	11 101 101 01 100 111
RST_t	(SP − 1) ← PC_H (SP − 2) ← PC_L PC_H ← 0, PC_L ← T	Restart to location T	1	11	•	•	•	•	•	•	11 t t t 111
SBC A, r	A ← A − r − CY	Subtract Reg. r from ACC w/carry	1	4	↕	↕	V	↕	1	↕	10 011 r r r (B)
SBC A, n	A ← A − n − CY	Subtract value n from ACC with carry		7	↕	↕	V	↕	1	↕	11 011 110 n n n nnn
SBC A, (HL)	A ← A − (HL) − CY	Sub. loc. (HL) from ACC w/carry		7	↕	↕	V	↕	1	↕	10 011 110
SBC A, (IX + d)	A ← A − (IX + d) − CY	Subtract loc. (IX + d) from ACC with carry		19	↕	↕	V	↕	1	↕	11 011 101 10 011 110 dd ddd ddd
SBC A, (IY + d)	A ← A − (IY + d) − CY	Subtract loc. (IY + d) from ACC with carry		19	↕	↕	V	↕	1	↕	11 111 101 10 011 110 dd ddd ddd
SBC HL, ss	HL ← HL − ss − CY	Subtract Reg. pair ss from HL with carry	2	15	↕	↕	V	↕	1	X	11 101 101 (A) 01 s s 0 010
SCF	CY ← 1	Set carry flag (C = 1)	1	4	1	•	•	•	0	0	00 110 111
SET b, (HL)	$(HL)_b$ ← 1	Set Bit b of location (HL)	2	15	•	•	•	•	•	•	11 001 011 (E) 11 b b b 110
SET b, (IX + d)	$(IX + d)_b$ ← 1	Set Bit b of location (IX + d)	4	23	•	•	•	•	•	•	11 011 101 (E) 11 001 011 dd ddd ddd 11 b b b 110

MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
SET b, (IY + d)	$(IY + d)_b \leftarrow 1$	Set Bit b of location (IY + d)	4	23	•	•	•	•	•	•	11 111 101 Ⓔ 11 001 011 dd ddd ddd 11 bbb 110
SET b, r	$r_b \leftarrow 1$	Set Bit b of Reg. r	2	8	•	•	•	•	•	•	11 001 011 Ⓑ 11 bbb rrr
SLA r		Shift Reg. r left arithmetic		8	↕	↕	P	↕	0	0	11 001 011 Ⓑ 00 100 rrr
SLA (HL)		Shift loc. (HL) left arithmetic		15	↕	↕	P	↕	0	0	11 001 011 00 100 110
SLA (IX + d)		Shift loc. (IX + d) left arithmetic		23	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 100 110
SLA (IY + d)	m ≡ r, (HL), (IX + d), (IY + d)	Shift loc. (IY + d) left arithmetic		23	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 100 110
SRA r		Shift Reg. r right arithmetic		8	↕	↕	P	↕	0	0	11 001 011 Ⓑ 00 101 rrr
SRA (HL)		Shift loc. (HL) right arithmetic		15	↕	↕	P	↕	0	0	11 001 011 00 101 110
SRA (IX + d)		Shift loc. (IX + d) right arithmetic		23	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 101 110
SRA (IY + d)	m ≡ r, (HL), (IX + d), (IY + d)	Shift loc. (IY + d) right arithmetic		23	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 101 110
SRL r		Shift Reg. r right logical		8	↕	↕	P	↕	0	0	11 001 011 Ⓑ 00 111 rrr
SRL (HL)		Shift loc. (HL) right logical		15	↕	↕	P	↕	0	0	11 001 011 00 111 110
SRL (IX + d)		Shift loc. (IX + d) right logical		23	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 111 110
SRL (IY + d)	m ≡ r, (HL), (IX + d), (IY + d)	Shift loc. (IY + d) right logical		23	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 111 110
SUB r	A ← A − r	Subtract Reg. r from ACC		4	↕	↕	V	↕	1	↕	10 010 rrr Ⓑ
SUB n	A ← A − n	Subtract value n from ACC		7	↕	↕	V	↕	1	↕	11 010 110 nn nnn nnn
SUB (HL)	A ← A − (HL)	Subtract loc. (HL) from ACC		7	↕	↕	V	↕	1	↕	10 010 110
SUB (IX + d)	A ← A − (IX + d)	Subtract loc. (IX + d) from ACC		19	↕	↕	V	↕	1	↕	11 011 101 10 010 110 dd ddd ddd
SUB (IY + d)	A ← A − (IY + d)	Subtract loc. (IY + d) from ACC		19	↕	↕	V	↕	1	↕	11 111 101 10 010 110 dd ddd ddd
XOR r	$A \leftarrow A \veebar r$	Exclusive 'OR' Reg. r and ACC		4	↕	↕	P	↕	1	↕	10 101 rrr Ⓑ
XOR n	$A \leftarrow A \veebar n$	Exclusive 'OR' value n and ACC		7	↕	↕	P	↕	1	↕	11 101 110 nn nnn nnn
XOR (HL)	$A \leftarrow A \veebar$ (HL)	Exclusive 'OR' loc. (HL) and ACC		7	↕	↕	P	↕	1	↕	10 101 110
XOR (IX + d)	$A \leftarrow A \veebar$ (IX + d)	Exclusive 'OR' loc. (IX + d) and ACC		19	↕	↕	P	↕	1	↕	11 011 101 10 101 110 dd ddd ddd
XOR (IY + d)	$A \leftarrow A \veebar$ (IY + d)	Exclusive 'OR' loc. (IY + d) and ACC		19	↕	↕	P	↕	1	↕	11 111 101 10 101 110 dd ddd ddd

FLAG NOTES:

① P/V flag is 0 if B-1=0, else P/V=1

② Z=1 if A=(HL), else Z=0

③ If B-1=0, Z flag set, else reset

FLAG DEFINITIONS:

• = Flag not affected

0 = Flag reset

1 = Flag set

X = Flag unknown

↕ = Flag affected according to result of operation

V = Overflow set

P = Parity set

IFF = Interrupt flip-flop set

Ⓐ

Reg	s s
BC	00
DE	01
HL	10
SP	11

Ⓑ

Reg	r
A	111
B	000
C	001
D	010
E	011
H	100
L	101

Ⓒ

Reg	pp
BC	00
DE	01
IX	10
SP	11

Ⓓ

Reg	r r
BC	00
DE	01
IY	10
SP	11

Ⓔ

Bit	b
0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

Ⓕ

Reg	r,r'
A	111
B	000
C	001
D	010
E	011
H	100
L	101

Ⓖ

Reg	qq
BC	00
DE	01
HL	10
AF	11

Ⓗ

CC	Condition		Relevant Flag
000	NZ	Non Zero	Z
001	Z	Zero	Z
010	NC	Non Carry	C
011	C	Carry	C
100	PO	Parity Odd	P/V
101	PE	Parity Even	P/V
110	P	Sign Positive	S
111	M	Sign Negative	S

Ⓘ

Reg	r
B	000
C	001
D	010
E	011
H	100
L	101
F	110
A	111

FLAG DESCRIPTION:

C = Carry/Link
Z = Zero
P/V = Parity/Overflow
S = Sign
N = Add/Subtract
H = Half Carry

PRINTED IN USA

SP780-7-78-3K-GN

μPD411A-E
μPD411A
μPD411A-1
μPD411A-2

4096 BIT DYNAMIC RAMS

DESCRIPTION

The μPD411A Family consists of four 4096 words by 1 bit dynamic N-channel MOS RAMs. They are designed for memory applications where very low cost and large bit storage are important design objectives. The μPD411A Family is designed using dynamic circuitry which reduces the standby power dissipation.

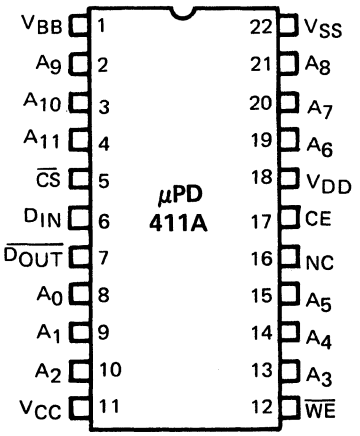
Reading information from the memory is non-destructive. Refreshing is easily accomplished by performing one read cycle on each of the 64 row addresses. Each row address must be refreshed every two milliseconds. The memory is refreshed whether Chip Select is a logic high or a logic low.

FEATURES

- Low Standby Power
- 4096 words x 1 bit Organization
- A single low-capacitance high level clock input with solid ±1 volt margins.
- Inactive Power 0.3 mW (Typ.)
- Power Supply +12, +5, −5V
- Easy System Interface
- TTL Compatible (Except CE)
- Address Registers on the Chip
- Simple Memory Expansion by Chip Select
- Three State Output and TTL Compatible
- 22 pin Plastic or Cerdip Dual-in-Line Package
- Replacement for INTEL's 2107B, TI's 4060 and Equivalent Devices.
- 4 Performance Ranges:

	ACCESS TIME	R/W CYCLE	RMW CYCLE	REFRESH TIME
μPD411A-E	350 ns	800 ns	960 ns	1 ms
μPD411A	300 ns	470 ns	650 ns	2 ms
μPD411A-1	250 ns	430 ns	600 ns	2 ms
μPD411A-2	200 ns	400 ns	520 ns	2 ms

PIN CONFIGURATION



PIN NAMES

A_0 - A_{11}	Address Inputs
A_0 - A_5	Refresh Addresses
CE	Chip Enable
$\overline{CS}$	Chip Select
D_{IN}	Data Input
$\overline{D_{OUT}}$	Data Output
$\overline{WE}$	Write Enable
V_{DD}	Power (+12V)
V_{CC}	Power (+5V)
V_{SS}	Ground
V_{BB}	(Power −5V)
NC	No Connection

Five Militia Drive/Lexington, Massachusetts 02173 Telephone 617/862-6410 Telex 92-3434

FUNCTIONAL DESCRIPTION

CE Chip Enable

A single external clock input is required. All read, write, refresh and read-modify-write operations take place when chip enable input is high. When the chip enable is low, the memory is in the low power standby mode. No read/write operations can take place because the chip is automatically precharging.

$\overline{CS}$ Chip Select

The chip select terminal affects the data in, data out and read/write inputs. The data input and data output terminals are enabled when chip select is low. The chip select input must be low on or before the rising edge of the chip enable and can be driven from standard TTL circuits. A register for the chip select input is provided on the chip to reduce overhead and simplify system design.

$\overline{WE}$ Write Enable

The read or write mode is selected through the write enable input. A logic high on the $\overline{WE}$ input selects the read mode and a logic low selects the write mode. The $\overline{WE}$ terminal can be driven from standard TTL circuits. The data input is disabled when the read mode is selected.

A_0–A_{11} Addresses

All addresses must be stable on or before the rising edge of the chip enable pulse. All address inputs can be driven from standard TTL circuits. Address registers are provided on the chip to reduce overhead and simplify system design.

D_{IN} Data Input

Data is written during a write or read-modify-write cycle while the chip enable is high. The data in terminal can be driven from standard TTL circuits. There is no register on the data in terminal.

$\overline{D_{OUT}}$ Data Output

The three state output buffer provides direct TTL compatibility with a fan-out of two TTL gates. The output is in the high-impedance (floating) state when the chip enable is low or when the Chip Select input is high. Data output is inverted from data in.

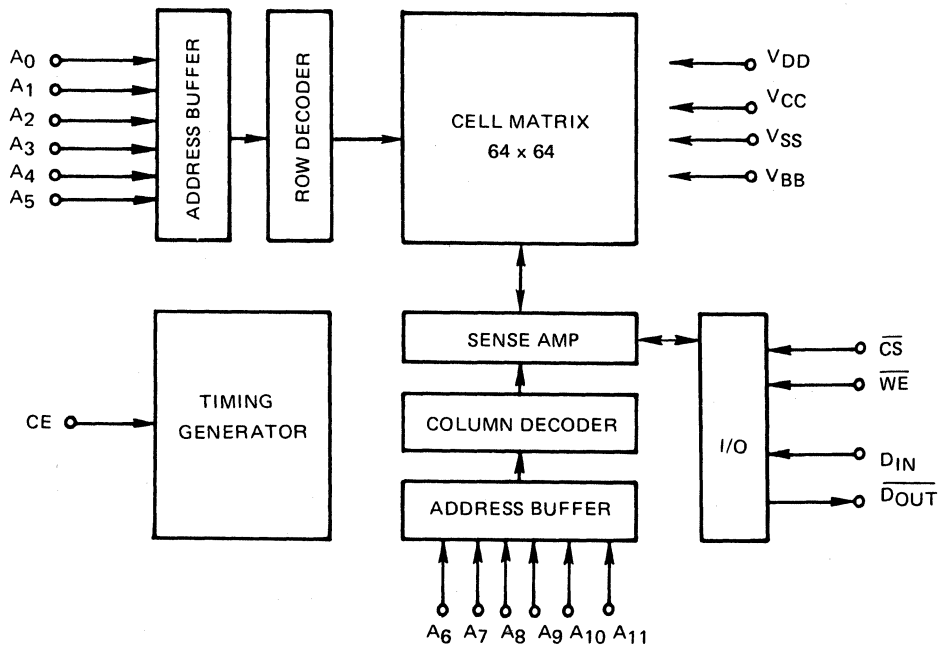
Refresh

Refresh must be performed every two milliseconds by cycling through the 64 addresses of the lower-order-address inputs A_0 through A_5 or by addressing every row within any 2*-millisecond period. Addressing any row refreshes all 64 bits in that row.

The chip does not need to be selected during the refresh. If the chip is refreshed during a write mode, the chip select must be high.

*μPD411A-E = 1 millisecond refresh period.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −55°C to +150°C
Output Voltage ① ..... +20 to −0.3 Volts
All Input Voltages ① ..... +20 to −0.3 Volts
Supply Voltage V_{DD} ① ..... +20 to −0.3 Volts
Supply Voltage V_{CC} ① ..... +20 to −0.3 Volts
Supply Voltage V_{SS} ① ..... +20 to −0.3 Volts
Power Dissipation 1.0W

Note: ① Relative to V_{BB}.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to 70°C, V_{DD} = +12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP. ①	LIMITS MAX.	UNIT	TEST CONDITIONS
Input Load Current	I_{LI}		0.01	10	μA	V_{IN} = V_{IL} MIN to V_{IH} MAX
CE Input Load Current	I_{LC}		0.01	10	μA	V_{IN} = V_{ILC} MIN to V_{IHC} MAX
Output Leakage Current for High Impedance State	I_{LO}		0.01	±10	μA	CE = V_{ILC} or $\overline{CS}$ = V_{IH} V_O = 0V to 5.25V
V_{DD} Supply Current during CE off	I_{DD} OFF		50	200	μA	CE = −1.0V to 0.6V
V_{DD} Supply Current during CE on	I_{DD} ON		35	50	mA	CE = V_{IHC}, T_a = 25°C
Average V_{DD} Current						T_a = 25°C
μPD411A-E	I_{DD} AV		25	40	mA	Cycle Time = 800 ns
μPD411A	I_{DD} AV		38	55	mA	Cycle Time = 470 ns
μPD411A-1	I_{DD} AV		38	55	mA	Cycle Time = 430 ns
μPD411A-2	I_{DD} AV		38	55	mA	Cycle Time = 400 ns
V_{BB} Supply Current ②	I_{BB}		5	100	μA	
V_{CC} Supply Current during CE off ③	I_{CC} OFF		0.01	10	μA	CE = V_{ILC} or $\overline{CS}$ = V_{IH}
Input Low Voltage	V_{IL}	−1.0		0.6	V	
Input High Voltage	V_{IH}	2.4		V_{CC} + 1	V	
CE Input Low Voltage	V_{ILC}	−1.0		0.6	V	
CE Input High Voltage	V_{IHC}	V_{DD} − 1	V_{DD}	V_{DD} + 1	V	
Output Low Voltage	V_{OL}	0		0.40	V	I_{OL} = 3.2 mA
Output High Voltage	V_{OH}	2.4		V_{CC}	V	I_{OH} = −2.0 mA

Notes: ① Typical values are for T_a = 25°C and nominal power supply voltages.
② The I_{BB} current is the sum of all leakage currents.
③ During CE on V_{CC} supply current is dependent on output loading.

CAPACITANCE

T_a = 0°C to 70°C, V_{DD} = +12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
Address Capacitance	C_{AD}			6	pF	V_{IN} = V_{SS}
$\overline{CS}$ Capacitance	C_{CS}			6	pF	V_{IN} = V_{SS}
D_{IN} Capacitance	C_{IN}			6	pF	V_{IN} = V_{SS}
$\overline{D_{OUT}}$ Capacitance	C_{OUT}			7	pF	V_{OUT} = V_{SS}
$\overline{WE}$ Capacitance	C_{WE}			7	pF	V_{IN} = V_{SS}
CE Capacitance	C_{CE1}			27	pF	V_{IN} = V_{SS}
	C_{CE2}			22	pF	V_{IN} = V_{DD}

READ CYCLE

T_a = 0°C to 70°C, V_{DD} = 12V ± 10%, V_{CC} = 5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V, unless otherwise noted.

PARAMETER	SYMBOL	LIMITS μPD411A-E MIN	μPD411A-E MAX	μPD411A MIN	μPD411A MAX	μPD411A-1 MIN	μPD411A-1 MAX	μPD411A-2 MIN	μPD411A-2 MAX	UNIT	TEST CONDITIONS
Time Between Refresh	t_{REF}		1		2		2		2	ms	$t_T = t_r = t_f$ = 20 ns C_L = 50 pF Load = 1TTL Gate V_{ref} = 2.0 or 0.8 Volts
Address to CE Set Up Time	t_{AC}	0		0		0		0		ns	
Address Hold Time	t_{AH}	150		150		150		150		ns	
CE Off Time	t_{CC}	380		130		130		130		ns	
CE Transition Time	t_T	0	40	0	40	0	40	0	40	ns	
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	0	130	ns	
Cycle Time	t_{CY}	800		470		430		400		ns	
CE on Time	t_{CE}	380	3000	300	3000	260	3000	230	3000	ns	
CE Output Delay	t_{CO}		330		280		230		180	ns	
Access Time	t_{ACC}		350		300		250		200	ns	
CE to $\overline{WE}$	t_{WL}	40		40		40		40		ns	
$\overline{WE}$ to CE on	t_{WC}	0		0		0		0		ns	

WRITE CYCLE

T_a = 0°C to 70°C, V_{DD} = 12V ±10%, V_{CC} = 5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V, unless otherwise noted.

PARAMETER	SYMBOL	LIMITS μPD411A-E MIN	μPD411A-E MAX	μPD411A MIN	μPD411A MAX	μPD411A-1 MIN	μPD411A-1 MAX	μPD411A-2 MIN	μPD411A-2 MAX	UNIT	TEST CONDITIONS
Cycle Time	t_{CY}	800		470		430		400		ns	$t_T = t_r = t_f$ = 20 ns C_L = 50 pF Load = 1TTL Gate V_{ref} = 2.0 or 0.8 Volts
Time Between Refresh	t_{REF}		1		2		2		2	ms	
Address to CE Set Up Time	t_{AC}	0		0		0		0		ns	
Address Hold Time	t_{AH}	150		150		150		150		ns	
CE Off Time	t_{CC}	380		130		130		130		ns	
CE Transition Time	t_T	0	40	0	40	0	40	0	40	ns	
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	0	130	ns	
CE on Time	t_{CE}	380	3000	300	3000	260	3000	230	3000	ns	
$\overline{WE}$ to CE off	t_W	200		180		180		150		ns	
CE to $\overline{WE}$	t_{CW}	380		300		260		230		ns	
D_{IN} to $\overline{WE}$ Set Up ①	t_{DW}	0		0		0		0		ns	
D_{IN} Hold Time	t_{DH}	40		40		40		40		ns	
$\overline{WE}$ Pulse Width	t_{WP}	200		180		180		150		ns	

Note: ① If $\overline{WE}$ is low before CE goes high then D_{IN} must be valid when CE goes high.

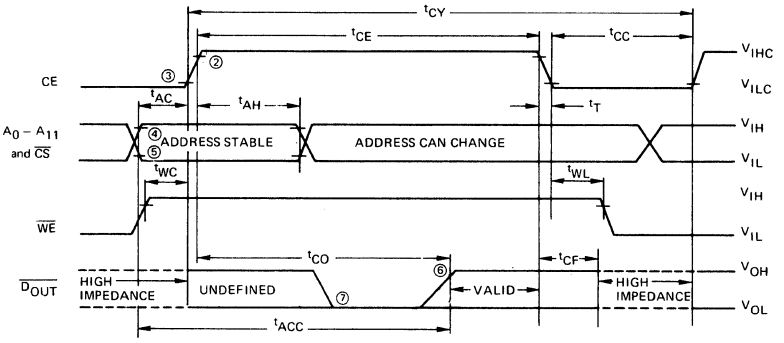
READ-MODIFY-WRITE CYCLE

T_a = 0°C to 70°C, V_{DD} = 12V ± 10%, V_{CC} = 5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V, unless otherwise noted.

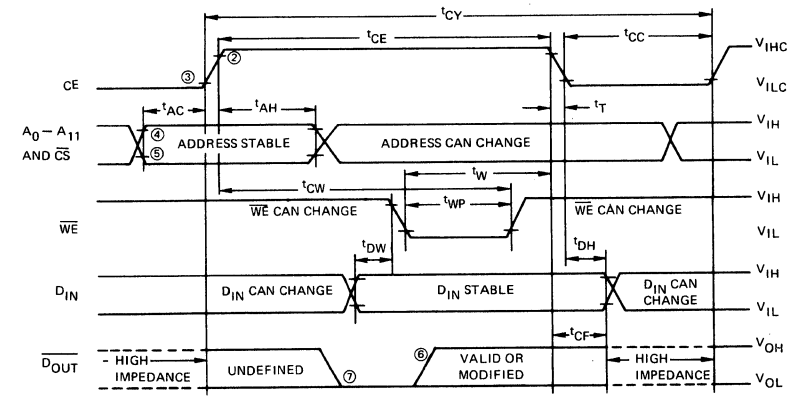
PARAMETER	SYMBOL	LIMITS μPD411A-E MIN	μPD411A-E MAX	μPD411A MIN	μPD411A MAX	μPD411A-1 MIN	μPD411A-1 MAX	μPD411A-2 MIN	μPD411A-2 MAX	UNIT	TEST CONDITIONS
Read-Modify-Write (RMW) Cycle Time	t_{RWC}	960		650		600		520		ns	$t_T = t_r = t_f$ = 20 ns C_L = 50 pF Load = 1TTL Gate V_{ref} = 2.0 or 0.8 Volts
Time Between Refresh	t_{REF}		1		2		2		2	ms	
Address to CE Set Up Time	t_{AC}	0		0		0		0		ns	
Address Hold Time	t_{AH}	150		150		150		150		ns	
CE Off Time	t_{CC}	380		130		130		130		ns	
CE Transition Time	t_T	0	40	0	40	0	40	0	40	ns	
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	0	130	ns	
CE Width During RMW	t_{CRW}	540	3000	480	3000	430	3000	350	3000	ns	
$\overline{WE}$ to CE on	t_{WC}	0		0		0		0		ns	
$\overline{WE}$ to CE off	t_W	200		180		180		150		ns	
$\overline{WE}$ Pulse Width	t_{WP}	200		180		180		150		ns	
D_{IN} to $\overline{WE}$ Set Up	t_{DW}	0		0		0		0		ns	
D_{IN} Hold Time	t_{DH}	40		40		40		40		ns	
CE to Output Delay	t_{CO}		330		280		230		180	ns	
Access Time	t_{ACC}		350		300		250		200	ns	

TIMING WAVEFORMS

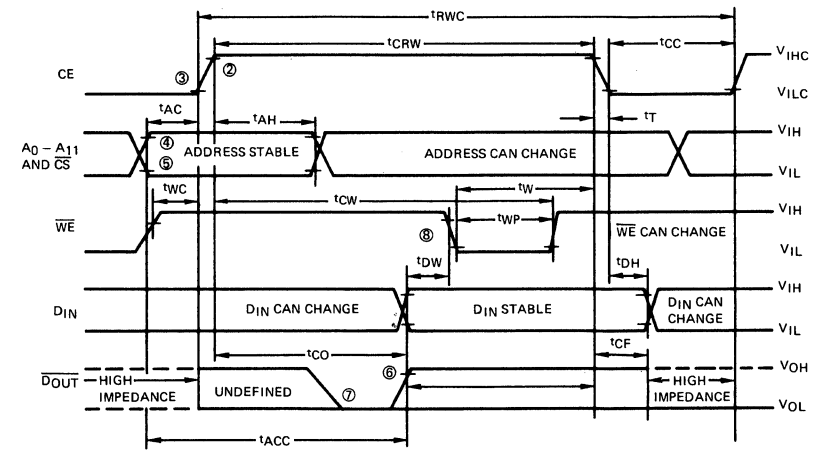
READ AND REFRESH CYCLE ①



WRITE CYCLE



READ-MODIFY-WRITE CYCLE



Notes:

① For refresh cycle, row and column addresses must be stable t_{AC} and remain stable for entire t_{AH} period.

② V_{DD} – 2V is the reference level for measuring timing of CE.

③ V_{SS} + 2V is the reference level for measuring timing of CE.

④ V_{IHMIN} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.

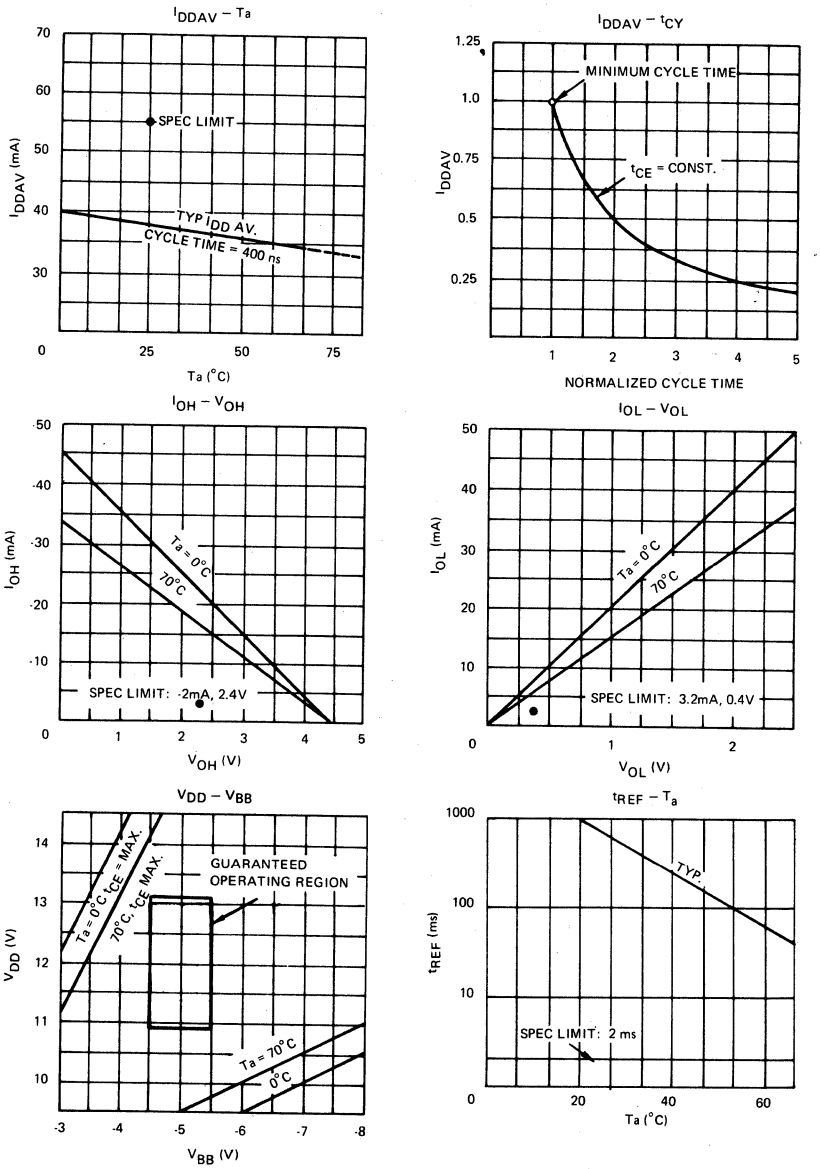
⑤ V_{ILMAX} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.

⑥ V_{SS} + 2.0V is the reference level for measuring timing of $\overline{D_{OUT}}$.

⑦ V_{SS} + 0.8V is the reference level for measuring timing of $\overline{D_{OUT}}$.

⑧ $\overline{WE}$ must be at V_{IH} until end of t_{CO}.

TYPICAL OPERATING CHARACTERISTICS



POWER CONSUMPTION

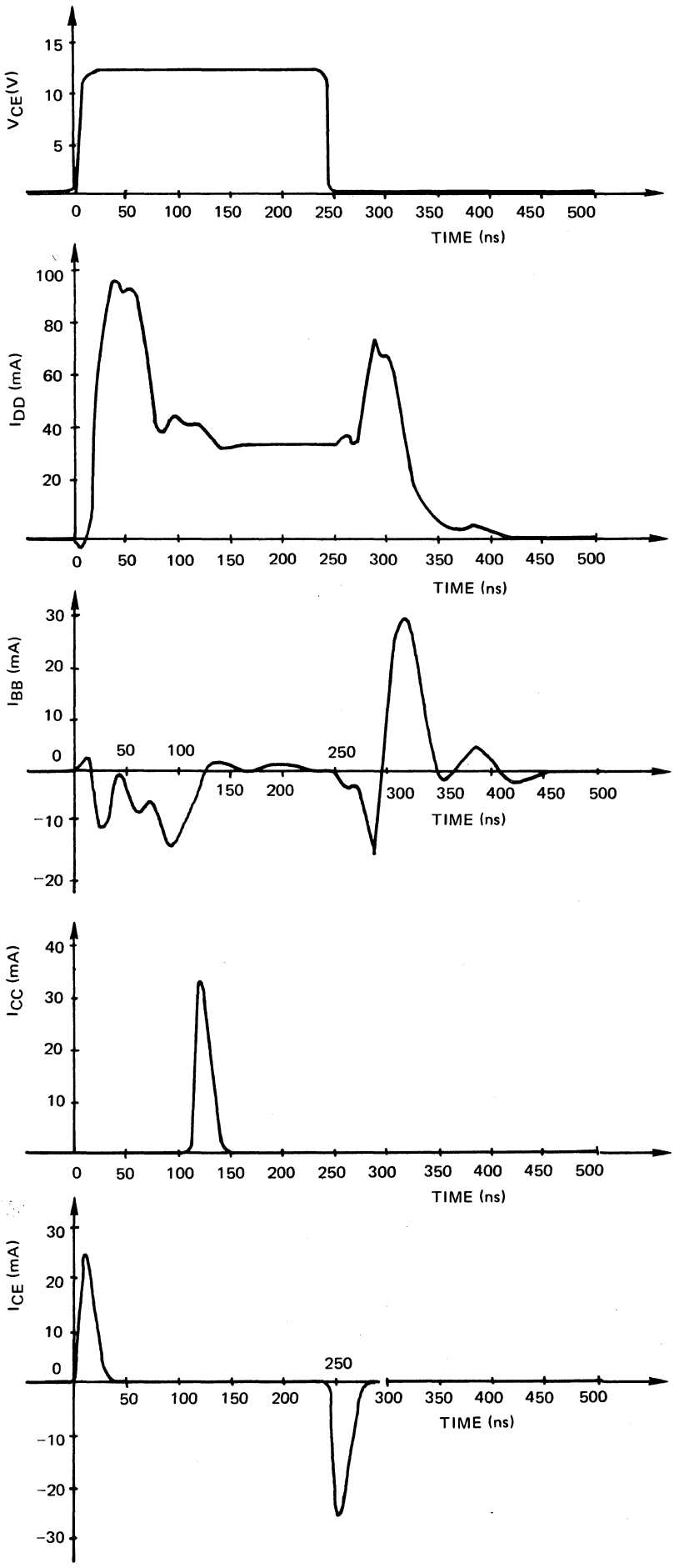
Power consumption = $V_{DD} \times I_{DDAV} + V_{BB} \times I_{BB}$

Typical power dissipation for each product is shown below.

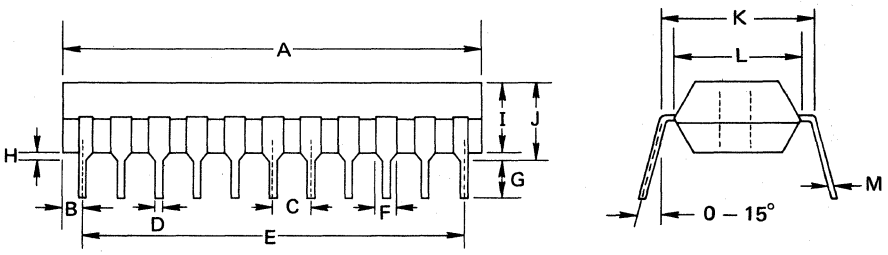
	mW (TYP.)	CONDITIONS
μPD411A-E	300 mW	$T_a = 25°C$, $t_{cy} = 800$ ns, $t_{CE} = 380$ ns
μPD411A	460 mW	$T_a = 25°C$, $t_{cy} = 470$ ns, $t_{CE} = 300$ ns
μPD411A-1	460 mW	$T_a = 25°C$, $t_{cy} = 430$ ns, $t_{CE} = 260$ ns
μPD411A-2	460 mW	$T_a = 25°C$, $t_{cy} = 400$ ns, $t_{CE} = 230$ ns

See curve above for power dissipation versus cycle time.

CURRENT WAVEFORMS ①

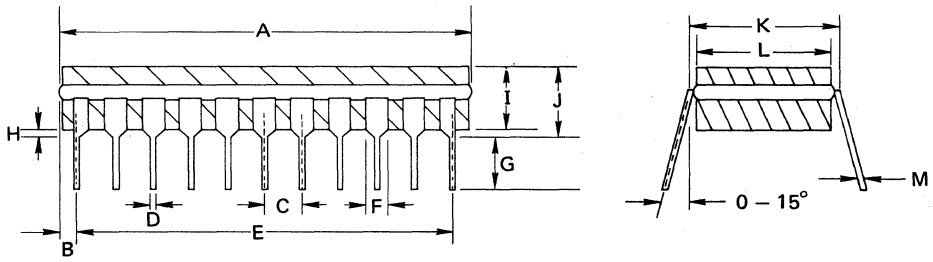


Note: ① V_{DD} = 12V, V_{BB} = −5.0V, V_{CC} = 5.0V



μPD411AC (Plastic)

ITEM	MILLIMETERS	INCHES
A	28.0 Max.	1.10 Max.
B	1.4 Max.	0.025 Max.
C	2.54	0.10
D	0.50	0.02
E	25.4	1.00
F	1.40	0.055
G	2.54 Min.	0.10 Min.
H	0.5 Min.	0.02 Min.
I	4.7 Max.	0.18 Max.
J	5.2 Max.	0.20 Max.
K	10.16	0.40
L	8.5	0.33
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$



μPD411AD (Cerdip)

ITEM	MILLIMETERS	INCHES
A	27.43 Max.	1.079 Max.
B	1.27 Max.	0.05 Max.
C	2.54 ± 0.1	0.10
D	0.42 ± 0.1	0.016
E	25.4 ± 0.3	1.0
F	1.5 ± 0.2	0.059
G	3.5 ± 0.3	0.138
H	3.7 ± 0.3	0.145
I	4.2 Max.	0.165 Max.
J	5.08 Max.	0.200 Max.
K	10.16 ± 0.15	0.400
L	9.1 ± 0.2	0.358
M	0.25 ± 0.05	0.009

μPD2111AL
μPD2111AL-2
μPD2111AL-4

1024 BIT (256 x 4) STATIC MOS RAM WITH COMMON I/O AND OUTPUT DISABLE

DESCRIPTION

The μPD2111AL is a 256 words by 4 bits static random access memory fabricated with N-channel MOS technology. It uses fully static circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

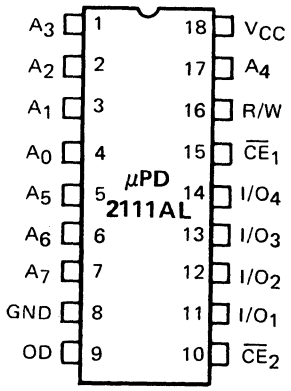
It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. Separate chip enable ($\overline{CE}$) leads allow easy selection of an individual package when outputs are OR-tied.

All members in the μPD2111AL family feature a low standby power mode with the supply voltage being reduced to +1.5V.

FEATURES

- 256 Words x 4 Bits Organization
- Common Data Input and Output
- Single +5V Supply Voltage
- Directly TTL Compatible – All Inputs and Outputs
- Static MOS – No Clocks or Refreshing Required
- Access Time – 250 ns to 450 ns max.
- Simple Memory Expansion – Chip Enable Inputs
- Fully Decoded – On Chip Address Decode
- Inputs Protected – All Inputs have Protection Against Static Charge
- Low Cost Packaging – 18 Pin Plastic Dual-In-Line Configuration
- Three-State Output – OR-Tie Capability
- Low Standby Power

PIN CONFIGURATION



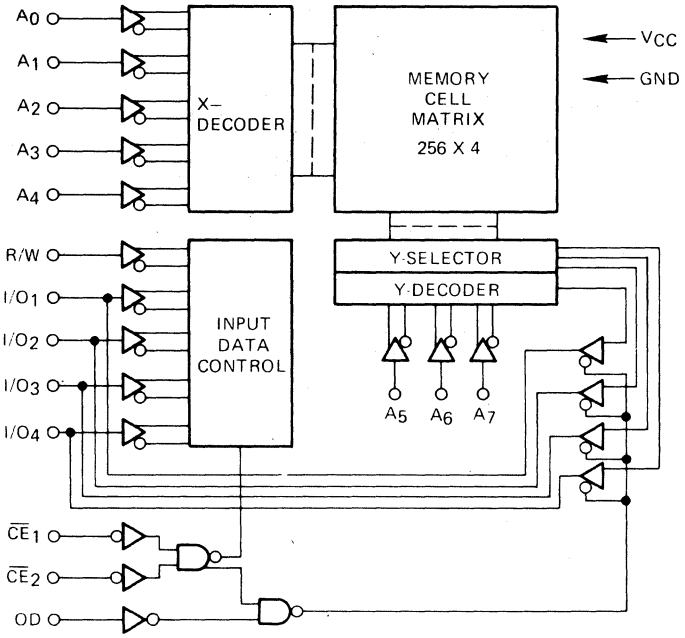
PIN NAMES

$A_0 - A_7$	Address Inputs
OD	Output Disable
R/W	Read/Write Input
$\overline{CE}_1$	Chip Enable 1
$\overline{CE}_2$	Chip Enable 2
$I/O_1 - I/O_4$	Data Input/Output

OPERATION MODES

CE_1	CE_2	OD	Chip Output Status	
0	1	0	Selected	Data Output
0	1	1		High Z
Others			Unselected	State

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−65°C to +125°C
All Output Voltages	−0.5 to +7 Volts
All Input Voltages	−0.5 to +7 Volts
Supply Voltage V_{CC}	−0.5 to +7 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = -10 to +70°C; V_{CC} = +5V ± 5%

PARAMETER		SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input High Voltage		V_{IH}	+2.0		V_{CC}	V	
Input Low Voltage		V_{IL}	−0.5		+0.8	V	
Output High Voltage	2111AL-4	V_{OH}	+2.4			V	I_{OH} = −150 μA
	2111AL 2111AL-2		+2.4			V	I_{OH} = −200 μA
Output Low Voltage		V_{OL}			+0.4	V	I_{OL} = +2.1 mA
Input Leakage Current High		I_{LIH}			+10	μA	$V_I = V_{CC}$
Input Leakage Current Low		I_{LIL}			−10	μA	V_I = OV
Output Leakage Current High		I_{LOH}			+5	μA	V_O = +2.4V to V_{CC} $\overline{CE}$ = +2.0V
Output Leakage Current Low		I_{LOL}			−10	μA	V_O = +0.4V $\overline{CE}$ = +2.0V
Power Supply Current	2111AL-4	I_{CC1}			50	mA	V_I = +5.25V
	2111AL 2111AL-2				55	mA	I_O = 0 mA T_a = +25°C
Power Supply Current	2111AL-4	I_{CC2}			60	mA	V_I = +5.25V
	2111AL 2111AL-2				65	mA	I_O = 0 mA T_a = −10 to +70°C

AC CHARACTERISTICS

READ CYCLE

T_a = −10°C to +70°C, V_{CC} = +5V ± 5%

PARAMETER	SYMBOL	LIMITS									UNIT
		2111AL-4			2111AL			2111AL-2			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Read Cycle Time	t_{RC}	450			350			250			ns
Access Time	t_A			450			350			250	ns
Chip Enable to Output	t_{CO}			310			240			180	ns
Output Disable to Output	t_{OD}			250			180			130	ns
Data Output to High Z State	t_{DF} ①	0		200	0		150	0		130	ns
Previous Read Data Valid After Change of Address	t_{OH}	40			40			40			ns

Note: ① t_{DF} is with respect to the trailing edge of $\overline{CE}_1$, $\overline{CE}_2$, or OD, whichever occurs first.

WRITE CYCLE

T_a = −10°C to +70°C, V_{CC} = +5V ± 5%

PARAMETER	SYMBOL	LIMITS									UNIT
		2111AL-4			2111AL			2111AL-2			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Write Cycle Time	t_{WC}	270			220			170			ns
Write Delay	t_{AW}	20			20			20			ns
Chip Enable to Write	t_{CW}	250			200			150			ns
Data Setup Time	t_{DW}	250			200			150			ns
Data Hold Time	t_{DH}	0			0			0			ns
Write Pulse Width	t_{WP}	250			200			150			ns
Write Recovery	t_{WR}	0			0			0			ns
Output Disable Setup	t_{DS}	20			20			20			ns

Note: OD is a logical 1 for common I/O and "don't care" for separate I/O operation.

AC CONDITIONS OF TEST

Input Pulse Levels . . . . . +0.8V to +2.0V
Input Pulse Rise and Fall Times . . . . . 20 ns
Timing Measurement Reference Level 1.5V
Output Load . . . . . 1 TTL + 100 pF

STANDBY CHARACTERISTICS

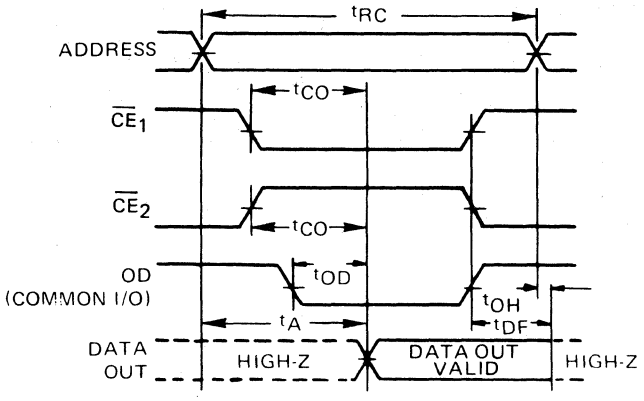
T_a = −10°C to +70°C

PARAMETER		SYMBOL	LIMITS			UNIT	TEST CONDITIONS
			MIN	TYP ①	MAX		
V_{CC} in Standby		V_{PD}	1.5			V	
$\overline{CE}_1$ Bias in Standby		V_{CES}	2.0			V	2.0V ≤ V_{PD} ≤ 5.25V
			V_{PD}			V	1.5V ≤ V_{PD} < 2.0V
Standby Current Drain	2111AL-4	I_{PD_1}			36	mA	All Inputs = V_{PD_1} = 1.5V
	2111AL/AL-2				38		
Standby Current Drain	2111AL-4	I_{PD_2}			45	mA	All Inputs = V_{PD_2} = 2.0V
	2111AL/AL-2				48		
Chip Deselect to Standby Time		t_{CP}	0			ns	
Standby Recovery		t_R	t_{RC} ②			ns	

Notes: ① Typical values are for T_a = 25°C and nominal supply voltage
② t_R = t_{RC} (Read Cycle Time)

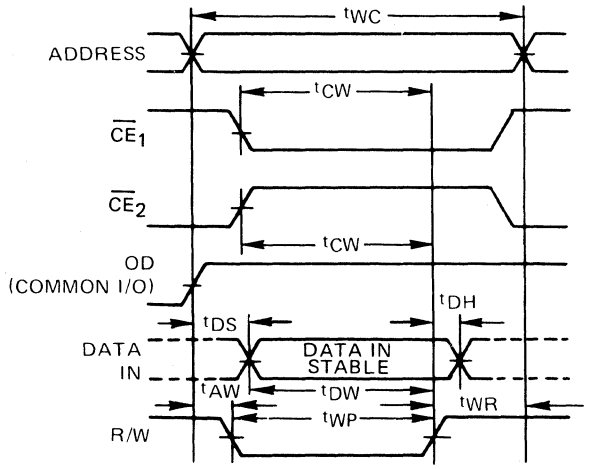
TIMING WAVEFORMS

READ CYCLE



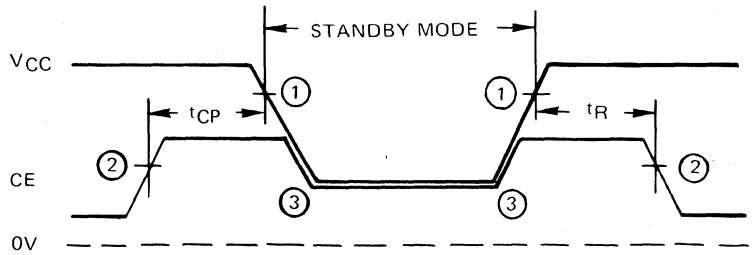
Notes: (1) OD should be tied low for separate I/O operation.
(2) R/W is high for read operation.

WRITE CYCLE



Note: OD is a logical 1 for common I/O and "don't care" for separate I/O operation.

STANDBY WAVEFORMS



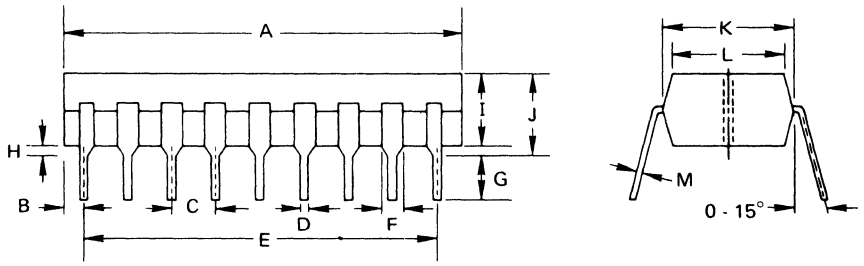
Notes: (1) 4.75V
(2) 2.0V
(3) 1.5V
(4) If the standby voltage (V_{PD}) is between 5.25V (V_{CC} Max) and 2.0V, then $\overline{CE}$ must be held at 2.0V Min (V_{IH}). If the standby voltage is less than 2.0V but greater than 1.5V (V_{PD} Min), then $\overline{CE}$ and standby voltage must be at least the same value or, if they are different, $\overline{CE}$ must be the more positive of the two. $\overline{CE}$ may be either of $\overline{CE_1}$ or $\overline{CE_2}$.

CAPACITANCE

T_a = 25°C; f = 1 MHz

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C_{IN}			8	pf	V_I = 0V
Output Capacitance	C_{OUT}			12	pf	V_O = 0V

PACKAGE OUTLINE μPD2111ALC



ITEM	MILLIMETERS	INCHES
A	22.5 MAX.	0.89
B	1.09	0.04
C	2.54	0.10
D	0.50 ± 0.10	0.02
E	20.32	0.80
F	1.2 MIN.	0.05
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.05 MAX.	0.16 MAX.
J	4.55 MAX.	0.18 MAX.
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	0.01

PROGRAMMABLE COMMUNICATION INTERFACE

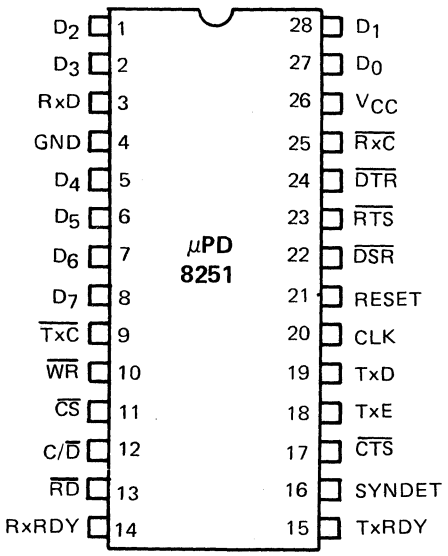
DESCRIPTION

The μPD8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART) is designed for microcomputer systems data communications. The USART is used as a peripheral and is programmed by the μPD8080 or other processor to communicate in commonly used serial data transmission techniques including IBM Bi-Sync. The USART receives serial data streams and converts them into parallel data characters for the processor. While receiving serial data, the USART will also accept data characters from the processor in parallel format, convert them to serial format and transmit. The USART will signal the processor when it has completely received or transmitted a character and requires service. Complete USART STATUS including data format errors and control signals such as TxE and SYNDET is available to the processor at any time.

FEATURES

- Asynchronous or Synchronous Operation
  - Asynchronous:
    - 5-8 Bit Characters
    - Clock Rate – 1, 16 or 64 x Baud Rate
    - Break Character Generation
    - Select 1, 1-1/2, or 2 Stop Bits
    - False Start Bit Detector
  - Synchronous:
    - 5-8 Bit Characters
    - Internal or External Character Synchronization
    - Automatic Sync Insertion
    - Single or Double Sync Characters
- Baud Rate – Synchronous – DC to 56K Baud
  – Asynchronous – DC to 9.6K Baud
- Full Duplex, Double Buffered Transmitter and Receiver
- Parity, Overrun and Framing Flags
- Fully Compatible with 8080
- All Inputs and Outputs are TTL Compatible
- Single +5 Volt Supply
- Separate Device, Receive and Transmit TTL Clocks
- 28 Pin Plastic DIP Package
- N-Channel MOS Technology

PIN CONFIGURATION



PIN NAMES

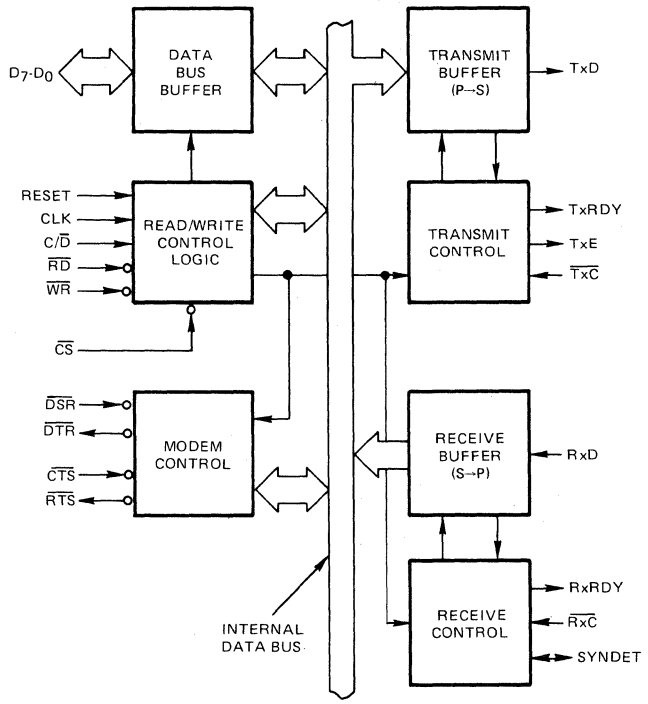
D_7-D_0	Data Bus (8 bits)
C/D	Control or Data is to be Written or Read
RD	Read Data Command
WR	Write Data or Control Command
CS	Chip Enable
CLK	Clock Pulse (TTL)
RESET	Reset
TxC	Transmitter Clock (TTL)
TxD	Transmitter Data
RxC	Receiver Clock (TTL)
RxD	Receiver Data
RxRDY	Receiver Ready (has character for 8080)
TxRDY	Transmitter Ready (ready for char. from 8080)
DSR	Data Set Ready
DTR	Data Terminal Ready
SYNDET	Sync Detect
RTS	Request to Send Data
CTS	Clear to Send Data
TxE	Transmitter Empty
V_{CC}	+5 Volt Supply
GND	Ground

FUNCTIONAL DESCRIPTION

The μPD8251 Universal Synchronous/Asynchronous Receiver/Transmitter is designed specifically for 8080 microcomputer systems but works with most 8-bit processors. Operation of the 8251, like other I/O devices in the 8080 family, is programmed by system software for maximum flexibility.

In the receive mode, a communication interface device must convert incoming serial format data into parallel data and make certain format checks on the data. And in the transmit mode, the device must format data into serial data. The device must also supply or remove characters or bits that are unique to the communication format in use. By performing conversion and formatting services automatically, the USART appears to the processor as a simple or "transparent" input or output of byte-oriented parallel data.

BLOCK DIAGRAM



BASIC OPERATION

C/D	RD	WR	CS	
0	0	1	0	8251 → Data Bus
0	1	0	0	Data Bus → 8251
1	0	1	0	Status → Data Bus
1	1	0	0	Data Bus → Control
X	X	X	1	Data Bus → 3-State
X	1	1	0	

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	-0°C to +70°C
Storage Temperature	-65°C to +125°C
All Output Voltages	-0.5 to +7 Volts
All Input Voltages	-0.5 to +7 Volts
Supply Voltages	-0.5 to +7 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

$T_a = 0°C$ to $70°C$; $V_{CC} = 5.0V \pm 5\%$; GND = 0V

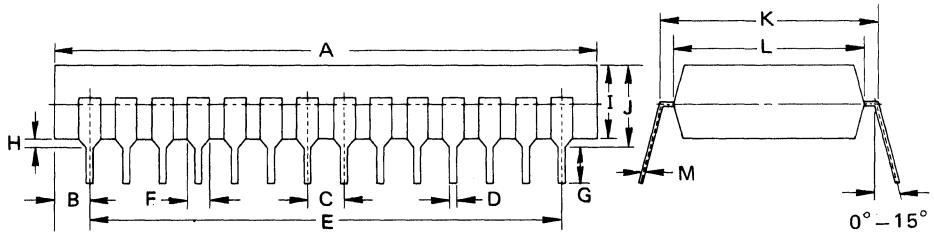
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	GND –.5		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC}	V	
Output Low Voltage	V_{OL}			0.45	V	$I_{OL} = 1.7$ mA
Output High Voltage	V_{OH}	2.4			V	$I_{OH} = -100\ \mu A$
Data Bus Leakage	I_{DL}			–50	μA	$V_{OUT} = 0.45V$
				10		$V_{OUT} = V_{CC}$
Input Load Current	I_{IL}			10	μA	@5.5V
Power Supply Current	I_{CC}		45	80	mA	

CAPACITANCE

$T_a = 25°C$; V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	fc = 1 MHz
I/O Capacitance	$C_{I/O}$			20	pF	Unmeasured pins returned to GND

PACKAGE OUTLINE μPD8251C



ITEM	MILLIMETERS	INCHES
A	38.0 MAX.	1.496 MAX.
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

BUS PARAMETERS: ①

T_a = 0°C to 70°C; V_{CC} = 5.0V ± 5%; GND = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
READ						
Address Stable before $\overline{READ}$, ($\overline{CS}$, C/$\overline{D}$)	t_{AR}	50			ns	
Address Hold Time for $\overline{READ}$, ($\overline{CS}$, $\overline{CD}$)	t_{RA}	5			ns	
$\overline{READ}$ Pulse Width	t_{RR}	430			ns	
Data Delay from $\overline{READ}$	t_{RD}			350	ns	C_L = 100 pF
$\overline{READ}$ to Data Floating	t_{DF}	25		200	ns	C_L = 100 pF C_L = 15 pF
Recovery Time Between WRITES ②	t_{RV}	6			t_{CY}	
WRITE						
Address Stable before $\overline{WRITE}$	t_{AW}	20			ns	
Address Hold Time for $\overline{WRITE}$	t_{WA}	20			ns	
$\overline{WRITE}$ Pulse Width	t_{WW}	400			ns	
Data Set-Up Time for $\overline{WRITE}$	t_{DW}	200			ns	
Data Hold Time for $\overline{WRITE}$	t_{WD}	40			ns	
OTHER TIMING						
Clock Period ③	t_{CY}	.420		1.35	μs	
Clock Pulse Width	$t_{\phi W}$	220		0.7t_{CY}	ns	
Clock Rise and Fall Time	t_R, t_F	0		50	ns	
TxD Delay from Falling Edge of $\overline{TxC}$	t_{DTx}			1	μs	C_L = 100 pF
Rx Data Set-Up Time to Sampling Pulse	t_{SRx}	2			μs	C_L = 100 pF
Rx Data Hold Time to Sampling Pulse	t_{HRx}	2			μs	C_L = 100 pF
Transmitter Input Clock Frequency 1X Baud Rate 16X and 64X Baud Rate	f_{Tx}	 DC DC		 56 520	 KHz KHz	
Transmitter Input Clock Pulse Width 1X Baud Rate 16X and 64X Baud Rate	t_{TPW}	 12 1			 t_{CY} t_{CY}	
Transmitter Input Clock Pulse Delay 1X Baud Rate 16X and 64X Baud Rate	t_{TPD}	 15 3			 t_{CY} t_{CY}	
Receiver Input Clock Frequency 1X Baud Rate 16X and 64X Baud Rate	f_{Rx}	 DC DC		 56 520	 KHz KHz	
Receiver Input Clock Pulse Width 1X Baud Rate 16X and 64X Baud Rate	t_{RPW}	 12 1			 t_{CY} t_{CY}	
Receiver Input Clock Pulse Delay 1X Baud Rate 16X and 64X Baud Rate	t_{RPD}	 15 3			 t_{CY} t_{CY}	
TxRDY Delay from Center of Data Bit	t_{Tx}			16	t_{CY}	C_L = 50 pF
RxRDY Delay from Center of Data Bit	t_{Rx}			20	t_{CY}	
Internal Syndet Delay from Center of Data Bit	t_{IS}			25	t_{CY}	
External Syndet Set-Up Time before Falling Edge of $\overline{RxC}$	t_{ES}	16		16	t_{CY}	
TxEMPTY Delay from Center of Data Bit	t_{TxE}			16	t_{CY}	C_L = 50 pF
Control Delay from Rising Edge of WRITE (TxE, $\overline{DTR}$, $\overline{RTS}$)	t_{WC}				t_{CY}	
Control to READ Set-Up Time ($\overline{DSR}$, $\overline{CTS}$)	t_{CR}	16			t_{CY}	

Notes:
① AC timings measured at V_{OH} = 2.0, V_{OL} = 0.8, and with load circuit of Figure 1.
② This recovery time is for initialization only, when MODE, SYNC1, SYNC2, COMMAND and first DATA BYTES are written into the USART. Subsequent writing of both COMMAND and DATA are only allowed when TxRDY = 1.
③ The TxC and RxC frequencies have the following limitations with respect to CLK.
For 1X Baud Rate, f_{Tx} or $f_{Rx} \leq 1/(30\ t_{CY})$
For 16X and 64X Baud Rate, f_{Tx} or $f_{Rx} \leq 1/(4.5\ t_{CY})$
④ Reset Pulse Width = 6 t_{CY} minimum.

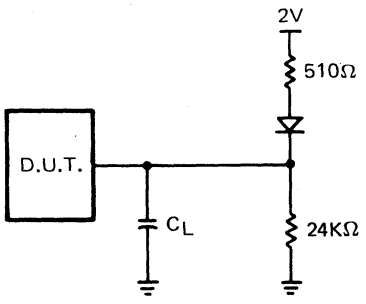
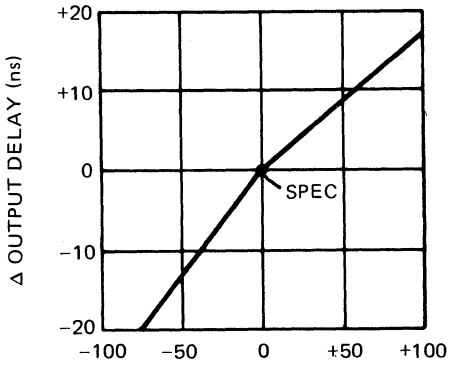


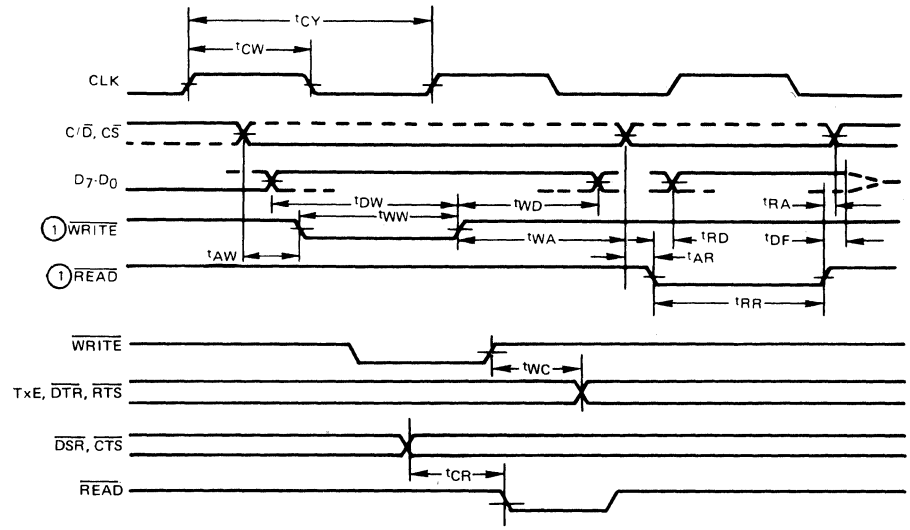
Figure 1.



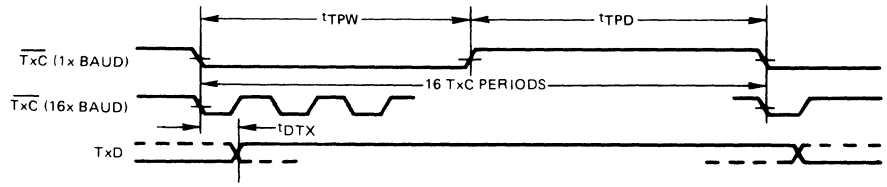
Typical Δ Output Delay Versus Δ Capacitance (pF)

TEST LOAD CIRCUIT

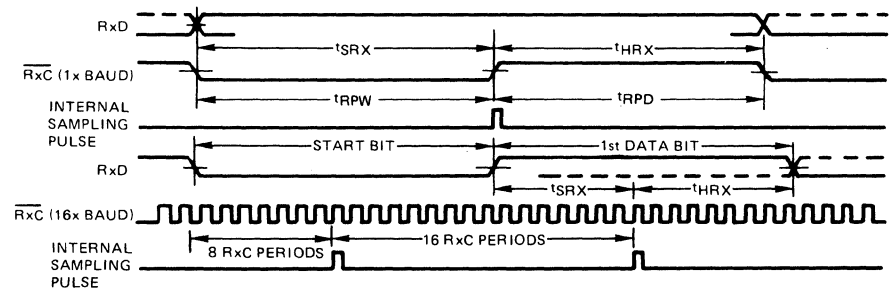
TIMING WAVEFORMS



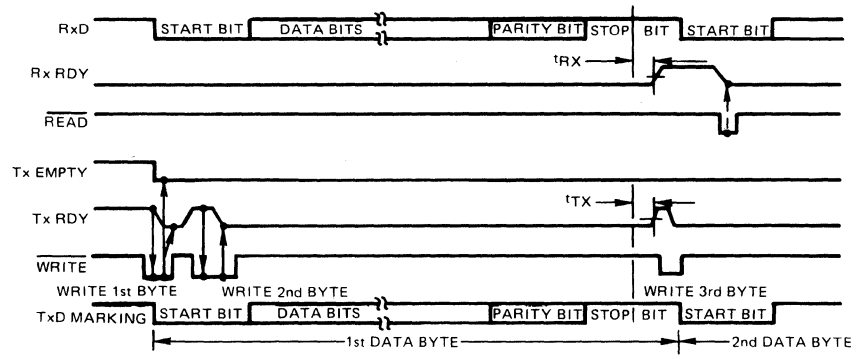
READ AND WRITE TIMING



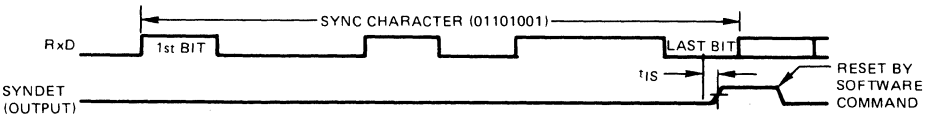
TRASNMITTER CLOCK AND DATA



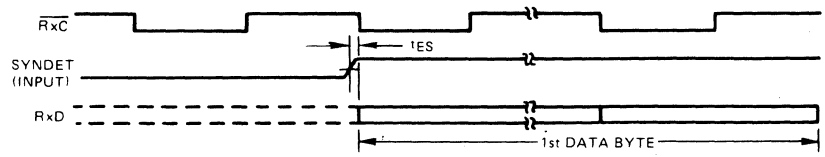
RECEIVER CLOCK AND DATA



TxRDY AND RxRDY TIMING (ASYNC MODE)



INTERNAL SYNC DETECT



EXTERNAL SYNC DETECT

Note: (1) Write and Read pulses have no timing limitation with respect to CLK.

PIN IDENTIFICATION

PIN			FUNCTION
NO.	SYMBOL	NAME	
1, 2, 27, 28 5 – 8	$D_7 - D_0$	Data Bus Buffer	An 8-bit, 3-state bi-directional buffer used to interface the 8251 to the processor data bus. Data is transmitted or received by the buffer in response to input/output or Read/Write instructions from the processor. The Data Bus Buffer also transfers Control words, Command words, and Status.
26	V_{CC}	V_{CC} Supply Voltage	+5 volt supply
4	GND	Ground	Ground
Read/Write Control Logic			This logic block accepts inputs from the processor Control Bus and generates control signals for overall USART operation. The Mode Instruction and Command Instruction registers that store the control formats for device functional definition are located in the Read/ Write Control Logic.
21	RESET	Reset	A "one" on this input forces the USART into the "Idle" mode where it will remain until reinitialized with a new set of control words. Minimum RESET pulse width is t_{CY}.
20	CLK	Clock Pulse	The CLK input provides for internal device timing and is usually connected to the Phase 2 (TTL) output of the μPB8224 Clock Generator. External inputs and outputs are not referenced to CLK, but the CLK frequency must be 30 times the Receiver or Transmitter clocks in the synchronous mode and 4.5 times for the asynchronous mode.
10	$\overline{WR}$	Write Data	A "zero" on this input instructs the μPD8251 to accept the data or control word which the processor is writing out to the USART via the data bus.
13	$\overline{RD}$	Read Data	A "zero" on this input instructs the μPD8251 to place the data or status information onto the Data Bus for the processor to read.
12	C/$\overline{D}$	Control/Data	The Control/Data input, in conjunction with the $\overline{WR}$ and $\overline{RD}$ inputs, informs USART to accept or provide either a data character, control word or status information via the Data Bus. 0 = Data; 1 = Control.
11	$\overline{CS}$	Chip Select	A "zero" on this input enables the USART for reading and writing to the processor.
Modem Control			The μPD8251 has a set of control inputs and outputs which may be used to simplify the interface to a Modem.
22	$\overline{DSR}$	Data Set Ready	The Data Set Ready input can be tested by the processor via Status information. The $\overline{DSR}$ input is normally used to test Modem Data Set Ready condition.
24	$\overline{DTR}$	Data Terminal Ready	The Data Terminal Ready output can be controlled via the Command word. The $\overline{DTR}$ output is normally used to drive Modem Data Terminal Ready or Rate Select lines.
23	$\overline{RTS}$	Request to Send	The Request to Send output can be controlled via the Command word. The $\overline{RTS}$ output is normally used to drive the Modem Request to Send line.
17	$\overline{CTS}$	Clear to Send	A "zero" on the Clear to Send input enables the USART to transmit serial data if the TxEN bit in the Command Instruction register is enabled (one).

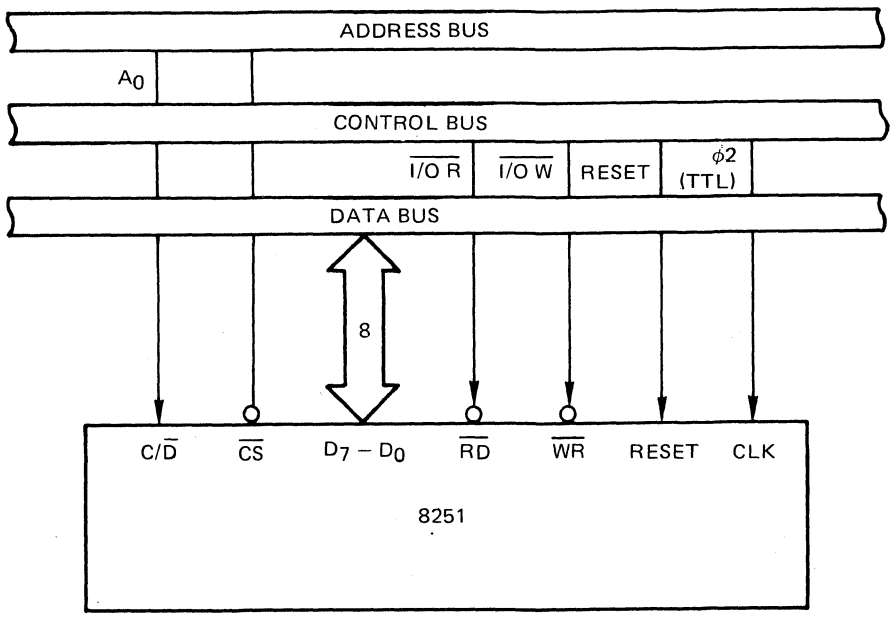
TRANSMIT BUFFER/ CONVERTER

The Transmit Buffer/Converter receives parallel data from the Data Bus Buffer via the internal data bus, converts parallel to serial data, inserts the necessary characters or bits needed for the programmed communication format and outputs composite serial data on the TxD output.

PIN IDENTIFICATION (CONT.)

PIN			FUNCTION
NO.	SYMBOL	NAME	
Transmit Control Logic			The Transmit Control Logic accepts and outputs all external and internal signals necessary for serial data transmission.
15	TxRDY	Transmitter Ready	Transmitter Ready signals the processor that the transmitter is ready to accept a data character. TxRDY can be used as an interrupt or may be tested through the Status information for Polled operation. Loading a character from the processor automatically resets TxRDY.
18	TxE	Transmitter Empty	The Transmitter Empty output signals the processor that the USART has no further characters to transmit. TxE is automatically reset upon receiving a data character from the processor. In half-duplex, TxE can be used to signal end of a transmission and request the processor to "turn the line around." The TxEn bit in the command instruction does not effect TxE. In the Synchronous mode, a "one" on this output indicates that a Sync character or characters are about to be automatically transmitted as "fillers" because the next data character has not been loaded.
9	$\overline{TxC}$	Transmitter Clock	The Transmitter Clock controls the serial character transmission rate. In the Asynchronous mode, the $\overline{TxC}$ frequency is a multiple of the actual Baud Rate. Two bits of the Mode Instruction select the multiple to be 1x, 16x, or 64x the Baud Rate. In the Synchronous mode, the $\overline{TxC}$ frequency is automatically selected to equal the actual Baud Rate. Note that for both Synchronous and Asynchronous modes, serial data is shifted out of the USART by the falling edge of $\overline{TxC}$.
19	TxD	Transmitter Data	The Transmit Control Logic outputs the composite serial data stream on this pin.

8251 INTERFACE TO 8080 STANDARD SYSTEM BUS



RECEIVER BUFFER

The Receiver Buffer accepts serial data input at the $\overline{RxD}$ pin and converts the data from serial to parallel format. Bits or characters required for the specific communication technique in use are checked and then an eight-bit "assembled" character is readied for the processor. For communication techniques which require less than eight bits, the μPD8251 sets the extra bits to "zero."

PIN IDENTIFICATION (CONT.)

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
Receiver Control Logic			This block manages all activities related to incoming data.
14	RxRDY	Receiver Ready	The Receiver Ready output indicates that the Receiver Buffer is ready with an "assembled" character for input to the processor. For Polled operation, the processor can check RxRDY using a Status Read or RxRDY can be connected to the processor interrupt structure. Note that reading the character to the processor automatically resets RxRDY.
25	$\overline{RxC}$	Receiver Clock	The Receiver Clock is the rate at which the incoming character is received. In the Asynchronous mode, the $\overline{RxC}$ frequency may be 1,16 or 64 times the actual Baud Rate but in the Synchronous mode the $\overline{RxC}$ frequency must equal the Baud Rate. Two bits in the mode instruction select Asynchronous at 1x, 16x or 64x or Synchronous operation at 1x the Baud Rate. Unlike $\overline{TxC}$, data is sampled by the μPD8251 on the rising edge of $\overline{RxC}$. (1)
3	RxD	Receiver Data	A composite serial data stream is received by the Receiver Control Logic on this pin.
16	SYNDET	Sync Detect	The SYNC Detect pin is only used in the Synchronous mode. The μPD8251 may be programmed through the Mode Instruction to operate in either the internal or external Sync mode and SYNDET then functions as an output or input respectively. In the internal Sync mode, the SYNDET output will go to a "one" when the μPD8251 has located the SYNC character in the Receive mode. If double SYNC character (bi-sync) operation has been programmed, SYNDET will go to "one" in the middle of the last bit of the second SYNC character. SYNDET is automatically reset to "zero" upon a Status Read or RESET. In the external SYNC mode, a "zero" to "one" transition on the SYNDET input will cause the μPD8251 to start assembling data character on the next falling edge of $\overline{RxC}$. The length of the SYNDET input should be at least one $\overline{RxC}$ period, but may be removed once the μPD8251 is in SYNC.

Note: (1) Since the μPD8251 will frequently be handling both the reception and transmission for a given link, the Receive and Transmit Baud Rates will be same. $\overline{RxC}$ and $\overline{TxC}$ then require the same frequency and may be tied together and connected to a single clock source or Baud Rate Generator.

Examples:

If the Baud Rate equals 110 (Async):
$\overline{RxC}$ or $\overline{TxC}$ equals 110 Hz (1x)
$\overline{RxC}$ or $\overline{TxC}$ equals 1.76 KHz (16x)
$\overline{RxC}$ or $\overline{TxC}$ equals 7.04 KHz (64x)

If the Baud Rate equals 300:
$\overline{RxC}$ or $\overline{TxC}$ equals 300 Hz (1x) A or S
$\overline{RxC}$ or $\overline{TxC}$ equals 4800 Hz (16x) A only
$\overline{RxC}$ or $\overline{TxC}$ equals 19.2 KHz (64x) A only

OPERATIONAL DESCRIPTION

A set of control words must be sent to the μPD8251 to define the desired mode and communications format. The control words will specify the BAUD RATE FACTOR (1x, 16x, 64x), CHARACTER LENGTH (5 to 8), NUMBER OF STOP BITS (1, 1-1/2, 2), ASYNCHRONOUS or SYNCHRONOUS MODE, SYNDET (IN or OUT), PARITY, etc.

After receiving the control words, the μPD8251 is ready to communicate. TxRDY is raised to signal the processor that the USART is ready to receive a character for transmission. When the processor writes a character to the USART, TxRDY is automatically reset.

Concurrently, the μPD8251 may receive serial data; and after receiving an entire character, the RxRDY output is raised to indicate a completed character is ready for the processor. The processor fetch will automatically reset RxRDY.

Note: The μPD8251 may provide faulty RxRDY for the first read after power-on or for the first read after receive is re-enabled by a command instruction (RxE). A dummy read is recommended to clear faulty RxRDY. But this is not the case for the first read after hardware or software reset after the device operation has once been established.

The μPD8251 cannot transmit until the TxEN (Transmitter Enable) bit has been set by a Command Instruction and until the $\overline{CTS}$ (Clear to Send) input is a "zero". TxD is held in the "marking" state after Reset awaiting new Command Words.

μPD8251 PROGRAMMING

The USART must be loaded with a group of two to four control words provided by the processor before data reception and transmission can begin. A Reset (internal or external) must immediately proceed the control words which are used to program the complete operational description of the communications interface. If an external RESET is not available, three successive 00 Hex or two successive 80 Hex command instructions ($C/\overline{D}$ = 1) followed by a software reset command instruction (40 Hex) can be used to initialize the 8251.

There are two control word formats:

1. Mode Instruction
2. Command Instruction

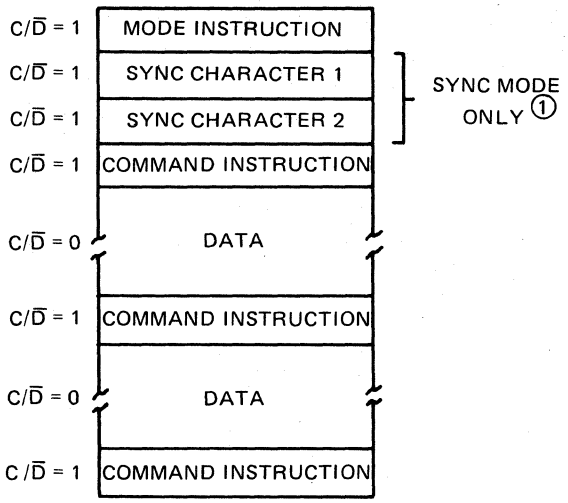
MODE INSTRUCTION

This control word specifies the general characteristics of the interface regarding the SYNCHRONOUS or ASYNCHRONOUS MODE, BAUD RATE FACTOR, CHARACTER LENGTH, PARITY, and NUMBER OF STOP BITS. Once the Mode Instruction has been received, SYNC characters or Command Instructions may be inserted depending on the Mode Instruction content.

COMMAND INSTRUCTION

This control word will be interpreted as a SYNC character definition if immediately preceded by a Mode Instruction which specified a Synchronous format. After the SYNC character(s) are specified or after an Asynchronous Mode Instruction, all subsequent control words will be interpreted as an update to the Command Instruction. Command Instruction updates may occur at any time during the data block. To modify the Mode Instruction, a bit may be set in the Command Instruction which causes an internal Reset which allows a new Mode Instruction to be accepted.

TYPICAL DATA BLOCK



NOTE ① The second SYNC character is skipped if MODE instruction has programmed the 8251 to single character Internal SYNC Mode. Both SYNC characters are skipped if MODE instruction has programmed the 8251 to ASYNC mode.

MODE INSTRUCTION DEFINITION

The μPD8251 can operate in either Asynchronous or Synchronous communication modes. Understanding how the Mode Instruction controls the functional operation of the USART is easiest when the device is considered to be two separate components, one asynchronous and the other synchronous, which share the same support circuits and package. Although the format definition can be changed at will or "on the fly", the two modes will be explained separately for clarity.

ASYNCHRONOUS TRANSMISSION

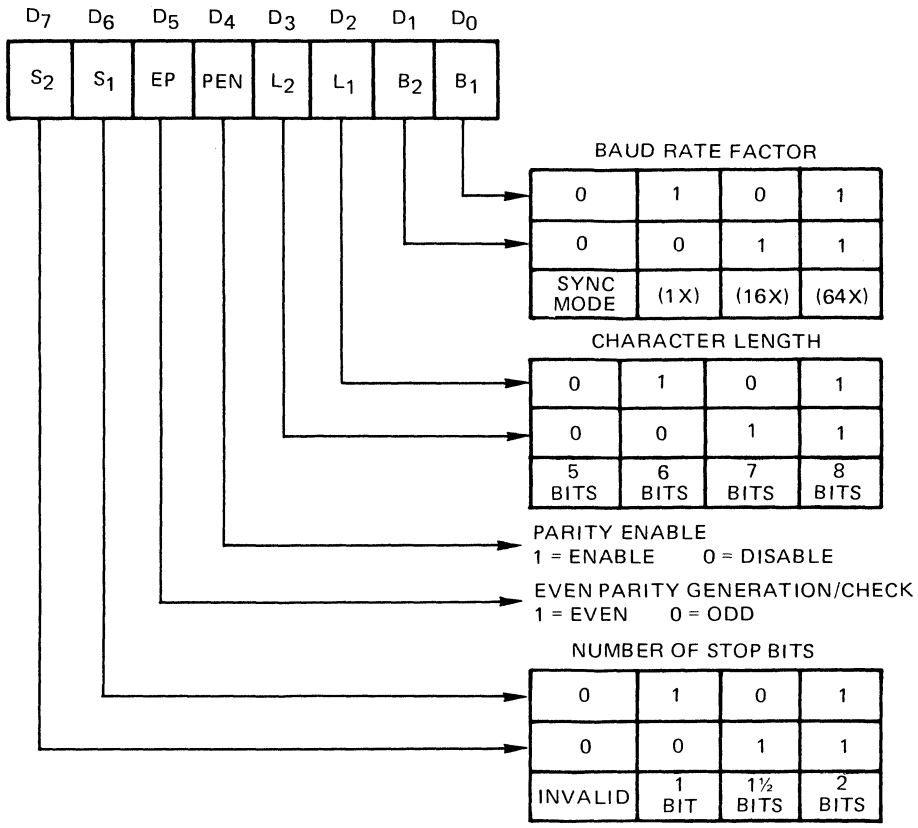
When a data character is written into the μPD8251, the USART automatically adds a START bit (low level or "space") and the number of STOP bits (high level or "mark") specified by the Mode Instruction. If Parity has been enabled, an odd or even Parity bit is inserted just before the STOP bits(s), as specified by the Mode Instruction. Then, depending on $\overline{CTS}$ and TxEN, the character may be transmitted as a serial data stream at the TxD output. Data is shifted out by the falling edge of $\overline{TxC}$ at $\overline{TxC}$, $\overline{TxC}$/16 or $\overline{TxC}$/64, as defined by the Mode Instruction.

If no data characters have been loaded into the μPD8251, or if all available characters have been transmitted, the TxD output remains "high" (marking) in preparation for sending the START bit of the next character provided by the processor. TxD may be forced to send a BREAK (continuously low) by setting the correct bit in the Command Instruction.

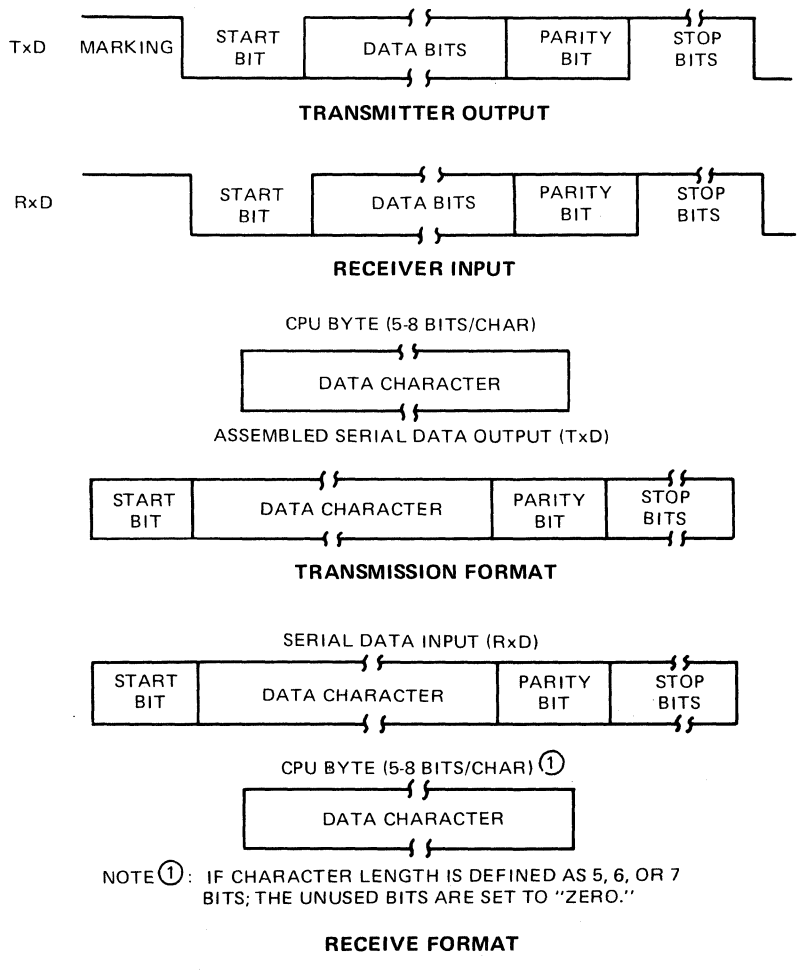
ASYNCHRONOUS RECEIVE

The RxD input line is normally held "high" (marking) by the transmitting device. A falling edge at RxD signals the possible beginning of a START bit and a new character. The START bit is checked by testing for a "low" at its nominal center as specified by the BAUD RATE. If a "low" is detected again, it is considered valid, and the bit assembling counter starts counting. The bit counter locates the approximate center of the data, parity (if specified), and STOP bits. The parity error flag (PE) is set, if a parity error occurs. Input bits are sampled at the RxD pin with the rising edge of $\overline{RxC}$. If a high is not detected for the STOP bit, which normally signals the end of an input character, a framing error (FE) will be set. After a valid STOP bit, the input character is loaded into the parallel Data Bus Buffer of the μPD8251 and the RxRDY signal is raised to indicate to the processor that a character is ready to be fetched. If the processor has failed to fetch the previous character, the new character replaces the old and the overrun flag (OE) is set. All the error flags can be reset by setting a bit in the Command Instruction. Error flag conditions will not stop subsequent USART operation.

MODE INSTRUCTION FORMAT ASYNCHRONOUS MODE



TRANSMIT/RECEIVE FORMAT ASYNCHRONOUS MODE



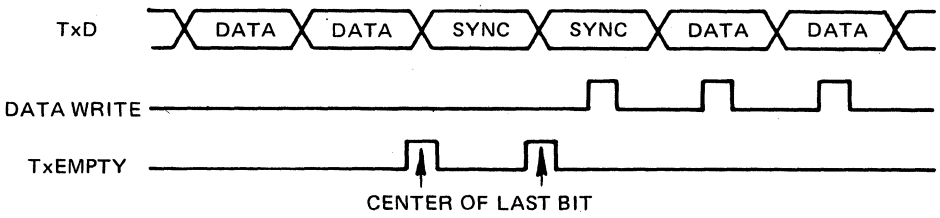
SYNCHRONOUS TRANSMISSION

As in Asynchronous transmission, the TxD output remains "high" (marking) until the μPD8251 receives the first character from the processor which is usually a SYNC character. After a Command Instruction has set TxEN and after Clear to Send ($\overline{CTS}$) goes low, the first character is serially transmitted. Data is shifted out on the falling edge of $\overline{TxC}$ and the same rate as $\overline{TxC}$.

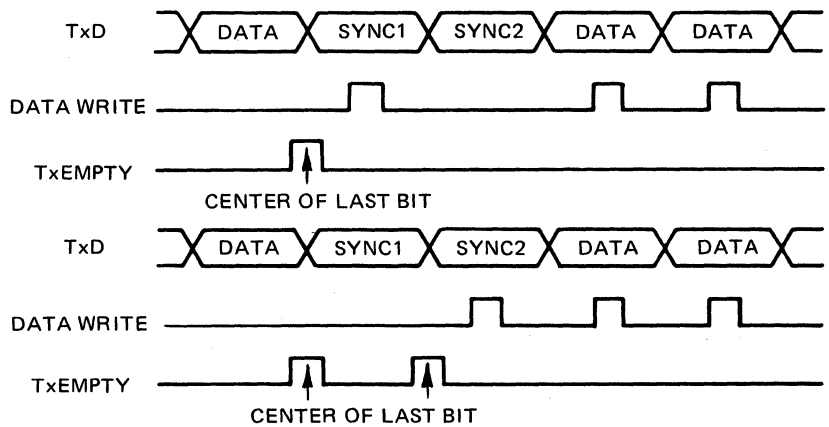
Once transmission has started, Synchronous Mode format requires that the serial data stream at TxD continue at the $\overline{TxC}$ rate or SYNC will be lost. If a data character is not provided by the processor before the μPD8251 Transmitter Buffer becomes empty, the SYNC character(s) loaded directly following the Mode Instruction will be automatically inserted in the TxD data stream. The SYNC character(s) are inserted to fill the line and maintain synchronization until new data characters are available for transmission. If the μPD8251 becomes empty, and must send the SYNC character(s), the TxEMPTY output is raised to signal the processor that the Transmitter Buffer is empty and SYNC characters are being transmitted. TxEMPTY is automatically reset by the next character from the processor.

TxEMPTY go high at the middle of the last data bit when the Transmit Register is EMPTY. TxEMPTY goes low again as sync characters are transmitted. See figure below.

FOR SINGLE SYNC CHARACTER OPERATION



FOR DOUBLE SYNC CHARACTER OPERATION (BISYNC)



SYNCHRONOUS RECEIVE

In Synchronous Receive, character synchronization can be either external or internal. If the internal SYNC mode has been selected, and the Enter HUNT (EH) bit has been set by a Command Instruction, the receiver goes into the HUNT mode.

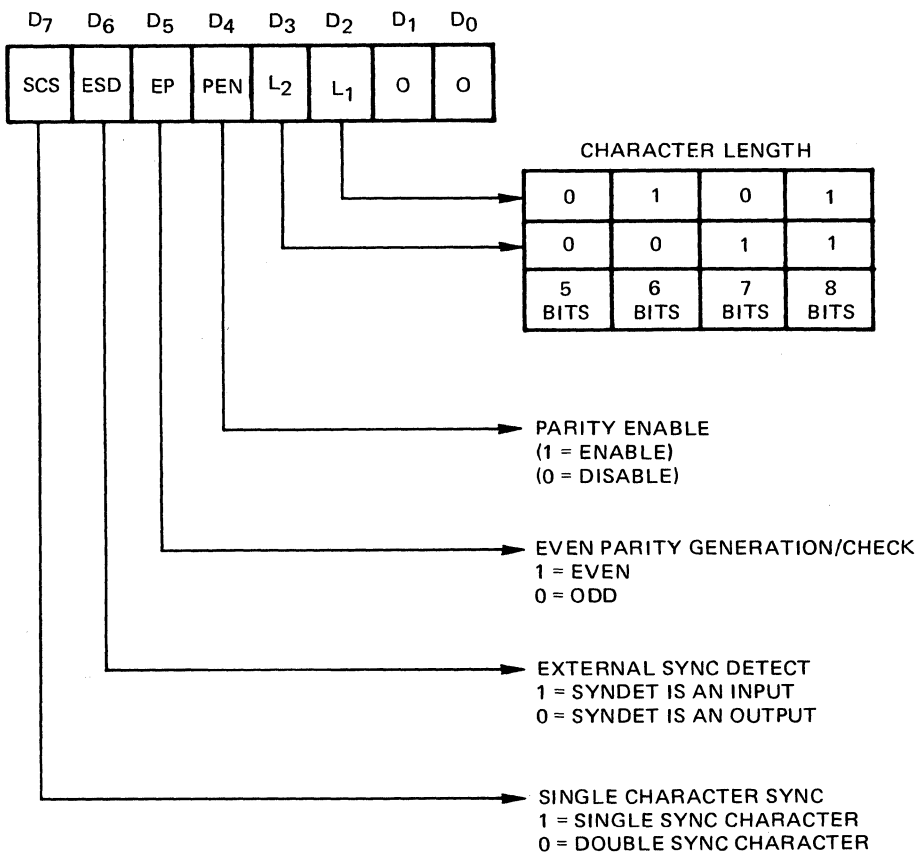
Incoming data on the RxD input is sampled on the rising edge of $\overline{RxC}$, and the Receiver Buffer is compared with the first SYNC character after each bit has been loaded until a match is found. If two SYNC characters have been programmed, the next received character is also compared. When the SYNC character(s) programmed have been detected, the μPD8251 leaves the HUNT mode and is in character synchronization. At this time, the SYNDET (output) is set high. SYNDET is automatically reset by a STATUS READ.

If external SYNC has been specified in the Mode Instruction, a "one" applied to the SYNDET (input) for at least one $\overline{RxC}$ cycle will synchronize the USART.

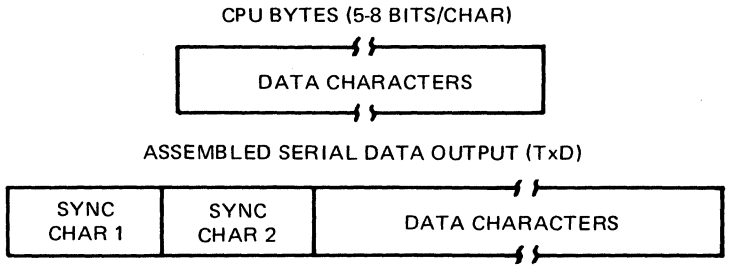
Parity and Overrun Errors are treated the same in the Synchronous as in the Asynchronous Mode. Framing errors do not apply in the Synchronous format.

The processor may command the receiver to enter the HUNT mode with a Command Instruction which sets Enter HUNT (EH) if synchronization is lost.

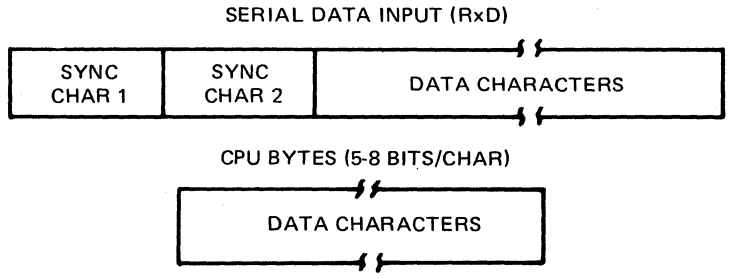
MODE INSTRUCTION FORMAT SYNCHRONOUS MODE



TRANSMIT/RECEIVE FORMAT SYNCHRONOUS MODE



TRANSMIT FORMAT



RECEIVE FORMAT

COMMAND INSTRUCTION FORMAT

After the functional definition of the μPD8251 has been specified by the Mode Instruction and the SYNC character(s) have been entered, if in SYNC mode, the USART is ready to receive Command Instructions and begin communication. A Command Instruction is used to control the specific operation of the format selected by the Mode Instruction. Enable Transmit, Enable Receive, Error Reset and Modem Controls are controlled by the Command Instruction.

After the Mode Instruction and the SYNC character(s), as needed, are loaded, all subsequent "control writes" ($C/\overline{D} = 1$) will load or overwrite the Command Instruction register. A Reset operation (internal via CMD IR or external via the RESET input) will cause the μPD8251 to interpret the next "control write", which must immediately follow the reset, as a Mode Instruction.

STATUS READ FORMAT

It is frequently necessary for the processor to examine the "status" of an active interface device to determine if errors have occurred or to notice other conditions which require a response from the processor. The μPD8251 has features which allow the processor to "read" the device status at any time. A data fetch is issued by the processor while holding the $C/\overline{D}$ input "high" to obtain device Status Information. Many of the bits in the status register are copies of external pins. This dual status arrangement allows the μPD8251 to be used in both Polled and interrupt driven environments. Status update can have a maximum delay of a 16 clock period.

PARITY ERROR

When a parity error is detected, the PE flag is set, and is cleared by setting the ER bit in a subsequent Command Instruction. PE being set does not inhibit USART operation.

OVERRUN ERROR

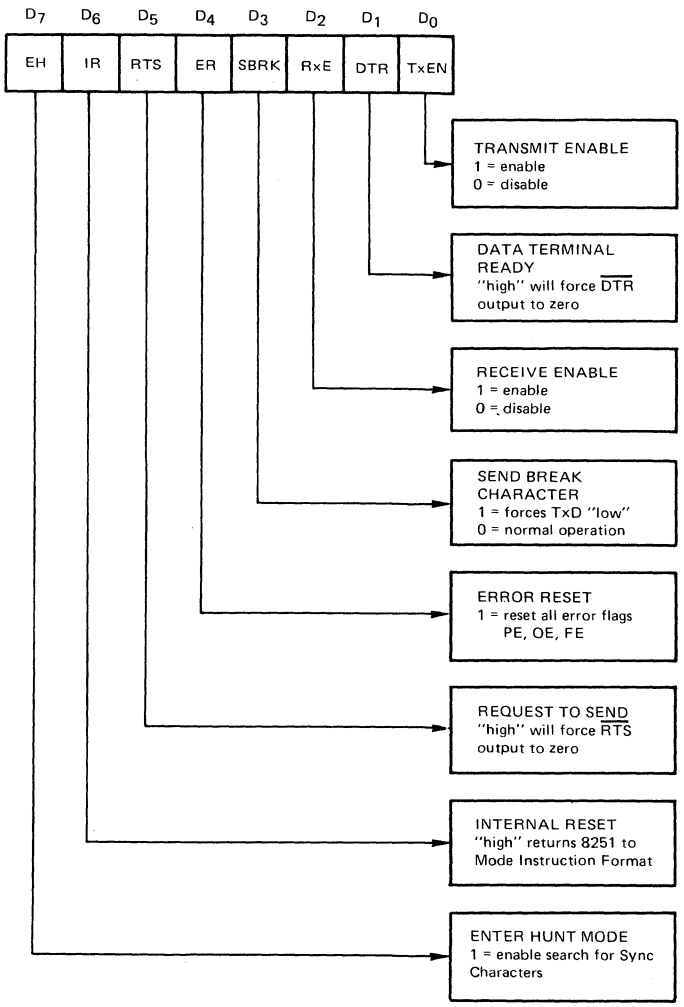
If the processor fails to read a data character before the one following is available, the OE flag is set, and is cleared by setting the ER bit in a subsequent Command Instruction. Although OE being set does not inhibit USART operation, the previously received character is overwritten and lost.

FRAMING ERROR ①

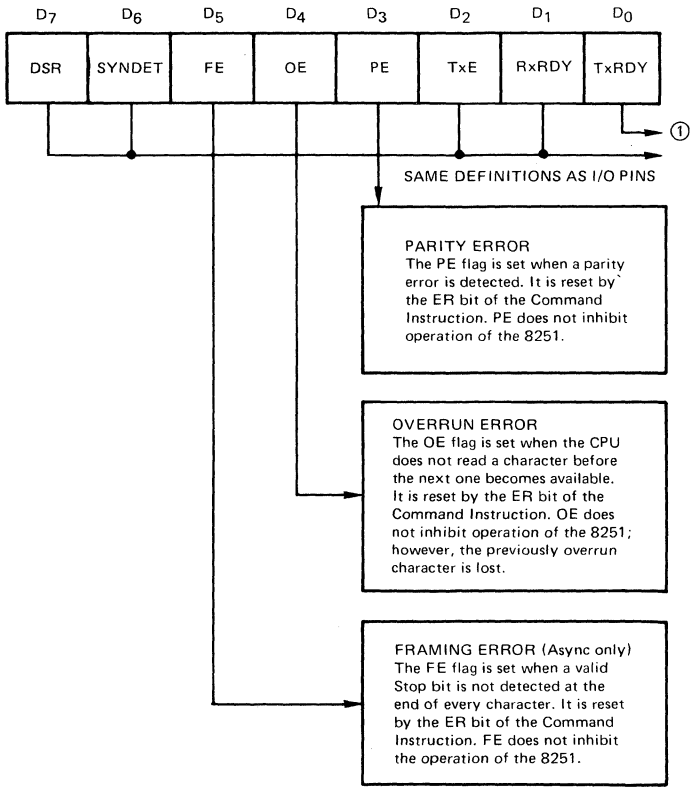
If a valid STOP bit is not detected at the end of a character, the FE flag is set, and is cleared by setting the ER bit in a subsequent Command Instruction. FE being set does not inhibit USART operation.

Note: ① ASYNC mode only.

COMMAND INSTRUCTION FORMAT



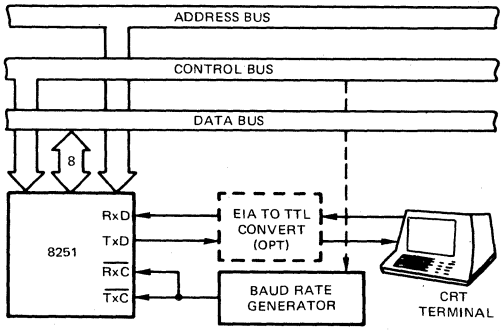
STATUS READ FORMAT



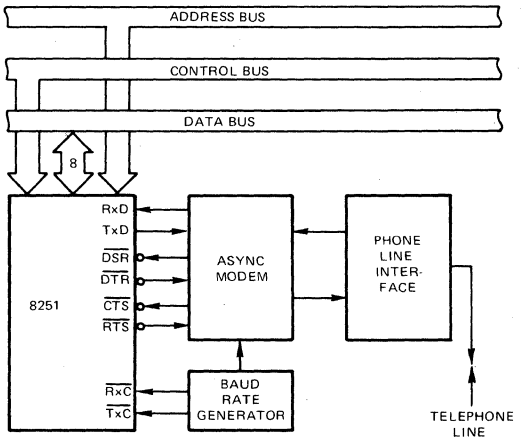
Note: ① TxRDY status bit is not totally equivalent to the TxRDY output pin, the relationship is as follows:

TxRDY status bit = DB Buffer Empty

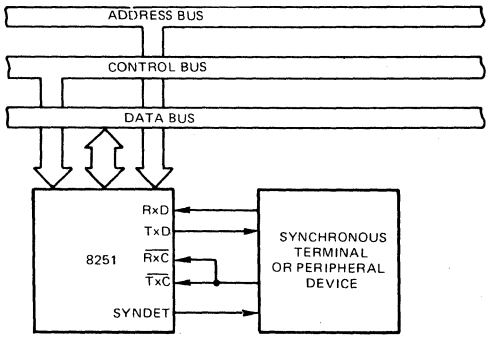
TxRDY (pin 15) = DB Buffer Empty • CTS • TxEn



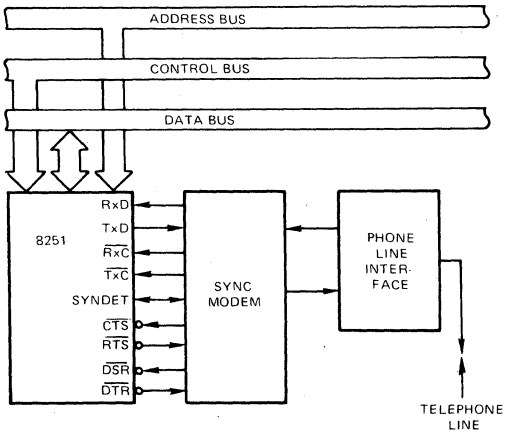
ASYNCHRONOUS SERIAL INTERFACE TO CRT TERMINAL, DC to 9600 BAUD



ASYNCHRONOUS INTERFACE TO TELEPHONE LINES



SYNCHRONOUS INTERFACE TO TERMINAL OR PERIPHERAL DEVICE



SYNCHRONOUS INTERFACE TO TELEPHONE LINES

PROGRAMMABLE PERIPHERAL INTERFACES

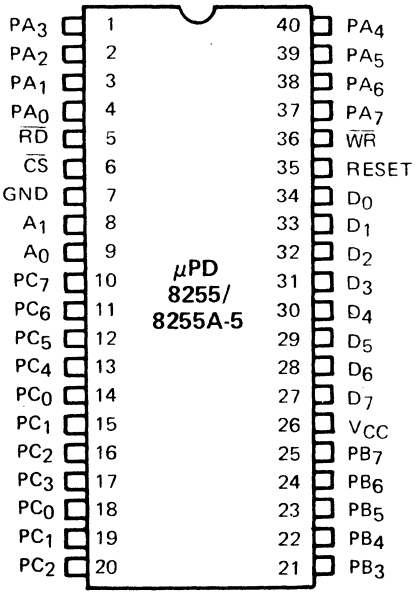
DESCRIPTION

The μPD8255 and μPD8255A-5 are general purpose programmable INPUT/OUTPUT devices designed for use with the 8080A/8085A microprocessors. Twenty-four (24) I/O lines may be programmed in two groups of twelve (group I and group II) and used in three modes of operation. In the Basic mode, (MODE 0), each group of twelve I/O pins may be programmed in sets of 4 to be input or output. In the Strobed mode, (MODE 1), each group may be programmed to have 8 lines of input or output. Three of the remaining four pins in each group are used for handshaking strobes and interrupt control signals. The Bidirectional Bus mode, (MODE 2), uses the 8 lines of Port A for a bidirectional bus, and five lines from Port C for bus control signals. The μPD8255 and μPD8255A-5 are packaged in 40 pin plastic dual-in-line packages.

FEATURES

- Fully Compatible with the 8080A/8085 Microprocessor Families
- All Inputs and Outputs TTL Compatible
- 24 Programmable I/O Pins
- Direct Bit SET/RESET Eases Control Application Interfaces
- 8 – 2 mA Darlington Drive Outputs for Printers and Displays (μPD8255)
- 8 – 4 mA Darlington Drive Outputs for Printers and Displays (μPD8255A-5)
- LSI Drastically Reduces System Package Count
- Standard 40 Pin Dual-In-Line Plastic Package

PIN CONFIGURATION



PIN NAMES

D_7-D_0	Data Bus (Bi-Directional)
RESET	Reset Input
$\overline{CS}$	Chip Select
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A_0, A_1	Port Address
PA_7-PA_0	Port A (Bit)
PB_7-PB_0	Port B (Bit)
PC_7-PC_0	Port C (Bit)
V_{CC}	+5 Volts
GND	0 Volts

*All data pertaining to the μPD8255A-5 is preliminary.

FUNCTIONAL DESCRIPTION

General

The μPD8255 and μPD8255A-5 Programmable Peripheral Interfaces (PPI) are designed for use in 8080A/8085A microprocessor systems. Peripheral equipment can be effectively and efficiently interfaced to the 8080A/8085A data and control busses with the μPD8255 and μPD8255A-5. The μPD8255 and μPD8255A-5 are functionally configured to be programmed by system software to avoid external logic for peripheral interfaces.

Data Bus Buffer

The 3-state, bidirectional, eight bit Data Bus Buffer (D_0-D_7) of the μPD8255 and μPD8255A-5 can be directly interfaced to the processor's system Data Bus (D_0-D_7). The Data Bus Buffer is controlled by execution of IN and OUT instructions by the processor. Control Words and Status information are also transmitted via the Data Bus Buffer.

Read/Write and Control Logic

This block manages all of the internal and external transfers of Data, Control and Status. Through this block, the processor Address and Control busses can control the peripheral interfaces.

Chip Select, $\overline{CS}$, pin 6

A Logic Low, V_{IL}, on this input enables the μPD8255 and μPD8255A-5 for communication with the 8080A/8085A.

Read, $\overline{RD}$, pin 5

A Logic Low, V_{IL}, on this input enables the μPD8255 and μPD8255A-5 to send Data or Status to the processor via the Data Bus Buffer.

Write, $\overline{WR}$, pin 36

A Logic Low, V_{IL}, on this input enables the Data Bus Buffer to receive Data or Control Words from the processor.

Port Select 0, A_0, pin 9
Port Select 1, A_1, pin 8

These two inputs are used in conjunction with $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ to control the selection of one of three ports on the Control Word Register. A_0 and A_1 are usually connected to A_0 and A_1 of the processor Address Bus.

Reset, pin 35

A Logic High, V_{IH}, on this input clears the Control Register and sets ports A, B, and C to the input mode. The input latches in ports A, B, and C are not cleared.

Group I and Group II Controls

Through an OUT instruction in System Software from the processor, a control word is transmitted to the μPD8255 and μPD8255A-5. Information such as "MODE," "Bit SET," and "Bit RESET" is used to initialize the functional configuration of each I/O port.

Each group (I and II) accepts "commands" from the Read/Write Control Logic and "control words" from the internal data bus and in turn controls its associated I/O ports.

Group I – Port A and upper Port C (PC_7-PC_4)
Group II – Port B and lower Port C (PC_3-PC_0)

While the Control Word Register can be written into, the contents cannot be read back to the processor.

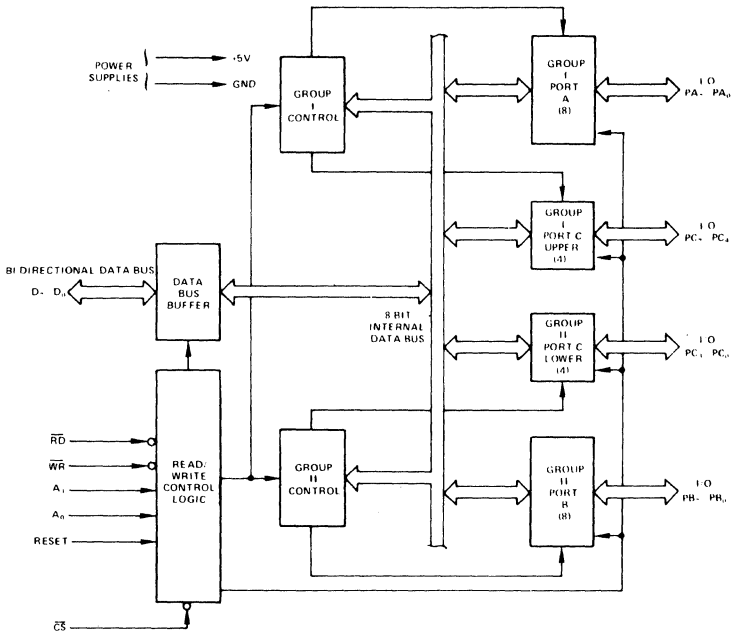
Ports A, B, and C

The three 8-bit I/O ports (A, B, and C) in the μPD8255 and μPD8255A-5 can all be configured to meet a wide variety of functional requirements through system software. The effectiveness and flexibility of the μPD8255 and μPD8255A-5 is further enhanced by special features unique to each of the ports.

Port A = An 8-bit data output latch/buffer and data input latch.
Port B = An 8-bit data input/output latch/buffer and an 8-bit data input buffer.
Port C = An 8-bit output latch/buffer and a data input buffer (input not latched).

Port C may be divided into two independent 4-bit control and status ports for use with Ports A and B.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +125°C
All Output Voltages ①	-0.5 to +7 Volts
All Input Voltages ①	-0.5 to +7 Volts
Supply Voltages ①	-0.5 to +7 Volts

Note: ① With respect to V_{SS}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = +5V ± 5%; V_{SS} = 0V.

PARAMETER	SYMBOL	LIMITS μPD8255 MIN	TYP	MAX	LIMITS μPD8255A-5 MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	V_{SS}-0.5		0.8	-0.5		0.8	V	
Input High Voltage	V_{IH}	2		V_{CC}	2		V_{CC}	V	
Output Low Voltage	V_{OL}			0.4			0.45	V	②
Output High Voltage	V_{OH}	2.4			2.4			V	③
Darlington Drive Current	I_{OH} ①	1	2	4	-1	-2	-4	mA	V_{OH} = 1.5V, R_{EXT} = 750Ω
Power Supply Current	I_{CC}		40	120		40	120	mA	V_{CC} = +5V, Output Open
Input Leakage Current	I_{LIH}			10			10	μA	V_{IN} = V_{CC}
Input Leakage Current	I_{LIL}			-10			-10	μA	V_{IN} = 0.4V
Output Leakage Current	I_{LOH}			10			10	μA	V_{OUT} = V_{CC}, $\overline{CS}$ = 2.0V
Output Leakage Current	I_{LOL}			-10			-10	μA	V_{OUT} = 0.4V, $\overline{CS}$ = 2.0V

Notes: ① Any set of eight (8) outputs from either Port A, B, or C can source 2 mA into 1.5V for μPD8255; or 4 mA into 1.5V for μPD8255A-5.
② For μPD8255: I_{OL} = 1.7 mA
For μPD8255A-5: I_{OL} = 2.5 mA for DB Port, 1.7 mA for Peripheral Ports.
③ For μPD8255: I_{OH} = -100 μs for DB Port, 50 μs for Peripheral Ports
For μPD8255A-5: I_{OH} = -400 μs for DB Port, -200 μs for Peripheral Ports.

CAPACITANCE

T_a = 25°C; V_{CC} = V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	f_c = 1 MHz
I/O Capacitance	$C_{I/O}$			20	pF	Unmeasured pins returned to V_{SS}

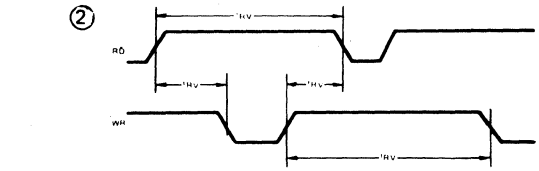
AC CHARACTERISTICS

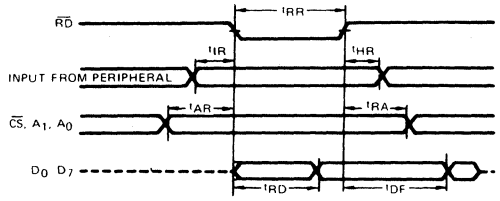
T_a = 0°C to +70°C; V_{CC} = +5V ± 5%; V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS μPD8255 MIN	LIMITS μPD8255 MAX	LIMITS μPD8255A-5 MIN	LIMITS μPD8255A-5 MAX	UNIT	TEST CONDITIONS
READ							
Address Stable Before $\overline{READ}$	t_{AR}	50		0		ns	
Address Stable After $\overline{READ}$	t_{RA}	0		0		ns	
$\overline{READ}$ Pulse Width	t_{RR}	405		300		ns	
Data Valid From $\overline{READ}$	t_{RD}		295		200	ns	8255: C_L = 100 pF 8255A-5: C_L = 150 pF
Data Float After $\overline{READ}$	t_{DF}	10	150	10	100	ns ns	C_L = 100 pF C_L = 15 pF
Time Between $\overline{READ}$s and/or $\overline{WRITE}$s	t_{RV}	850		850		ns	②
WRITE							
Address Stable Before $\overline{WRITE}$	t_{AW}	20		0		ns	
Address Stable After $\overline{WRITE}$	t_{WA}	20		20		ns	
$\overline{WRITE}$ Pulse Width	t_{WW}	400		300		ns	
Data Valid To $\overline{WRITE}$ (L.E.)	t_{DW}	10		100		ns	
Data Valid After $\overline{WRITE}$	t_{WD}	35		30		ns	
OTHER TIMING							
$\overline{WR}$ = 0 To Output	t_{WB}		500		350	ns	8255: C_L = 50 pF 8255A-5: C_L = 150 pF
Peripheral Data Before $\overline{RD}$	t_{IR}	0		0		ns	
Peripheral Data After $\overline{RD}$	t_{HR}	50		0		ns	
$\overline{ACK}$ Pulse Width	t_{AK}	500		300		ns	
$\overline{STB}$ Pulse Width	t_{ST}	350		500		ns	
Per. Data Before T.E. Of $\overline{STB}$	t_{PS}	60		0		ns	
Per. Data After T.E. Of $\overline{STB}$	t_{PH}	150		180		ns	
$\overline{ACK}$ = 0 To Output	t_{AD}		400		300	ns	8255: C_L = 50 pF 8255A-5: C_L = 150 pF
$\overline{ACK}$ = 0 To Output Float	t_{KD}	20	300	20	250	ns	8255 { C_L = 50 pF C_L = 15 pF
$\overline{WR}$ = 1 To $\overline{OBF}$ = 0	t_{WOB}		300		650	ns	
$\overline{ACK}$ = 0 To $\overline{OBF}$ = 1	t_{AOB}		450		350	ns	
$\overline{STB}$ = 0 To IBF = 1	t_{SIB}		450		300	ns	8255: C_L = 50 pF
$\overline{RD}$ = 1 To IBF = 0	t_{RIB}		360		300	ns	
$\overline{RD}$ = 0 To INTR = 0	t_{RIT}		450		400	ns	
$\overline{STB}$ = 1 To INTR = 1	t_{SIT}		400		300	ns	8255A-5: C_L = 150 pF
$\overline{ACK}$ = 1 To INTR = 1	t_{AIT}		400		350	ns	
$\overline{WR}$ = 0 To INTR = 0	t_{WIT}		850		850	ns	

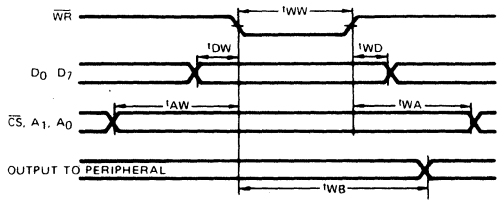
Notes: ① Period of Reset pulse must be at least 50 μs during or after power on. Subsequent Reset pulse can be 500 ns min.

TIMING WAVEFORMS
MODE 0

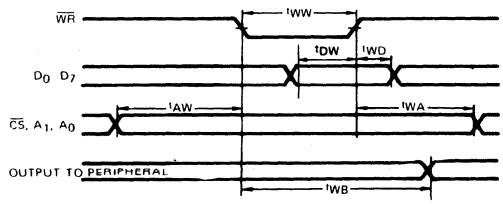




BASIC INPUT



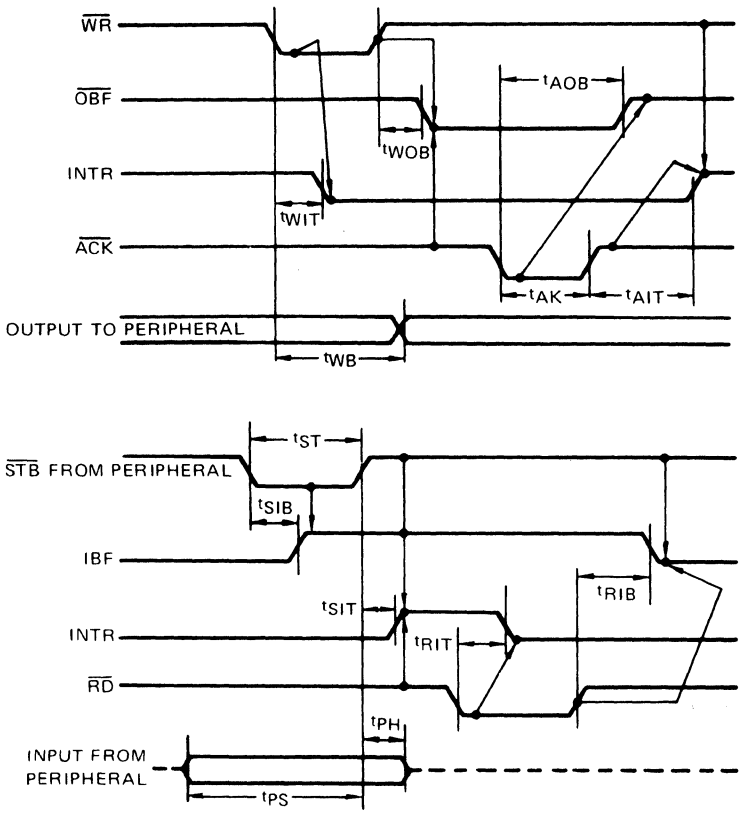
BASIC OUTPUT – μPD8255



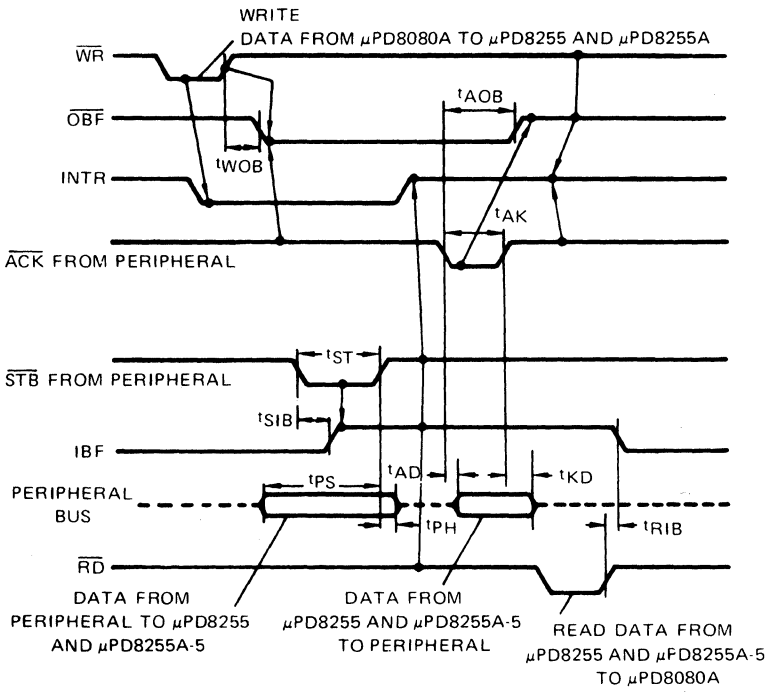
BASIC OUTPUT – μPD8255A-5

TIMING WAVEFORMS (CONT.)

MODE 1



MODE 2



Note: ① Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
(INTR = IBF · $\overline{MASK}$ · $\overline{STB}$ · $\overline{RD}$ + $\overline{OBF}$ · $\overline{MASK}$ · $\overline{ACK}$ · $\overline{WR}$)

② When the μPD8255A-5 is set to Mode 1 or 2, $\overline{OBF}$ is reset to be high (logic 1).

μPD8255/8255A-5

MODES

The μPD8255 and μPD8255A-5 can be operated in modes (0, 1 or 2) which are selected by appropriate control words and are detailed below.

MODE 0

- MODE 0 provides for basic Input and Output operations through each of the ports A, B, and C. Output data is latched and input data follows the peripheral. No "handshaking" strobes are needed.

  16 different configurations in MODE 0

  Two 8-bit ports and two 4-bit ports

  Inputs are not latched

  Outputs are latched

MODE 1

MODE 1 provides for Strobed Input and Output operations with data transferred through Port A or B and handshaking through Port C.

Two I/O Groups (I and II)

Both groups contain an 8-bit data port and a 4-bit control/data port

Both 8-bit data ports can be either Latched Input or Latched Output

MODE 2

MODE 2 provides for Strobed bidirectional operation using PA_{0-7} as the bidirectional latched data bus. PC_{3-7} is used for interrupts and "handshaking" bus flow controls similar to Mode 1. Note that PB_{0-7} and PC_{0-2} may be defined as Mode 0 or 1, input or output in conjunction with Port A in Mode 2.

An 8-bit latched bidirectional bus port (PA_{0-7}) and a 5-bit control port (PC_{3-7})

Both inputs and outputs are latched

An additional 8-bit input or output port with a 3-bit control port

BASIC OPERATION

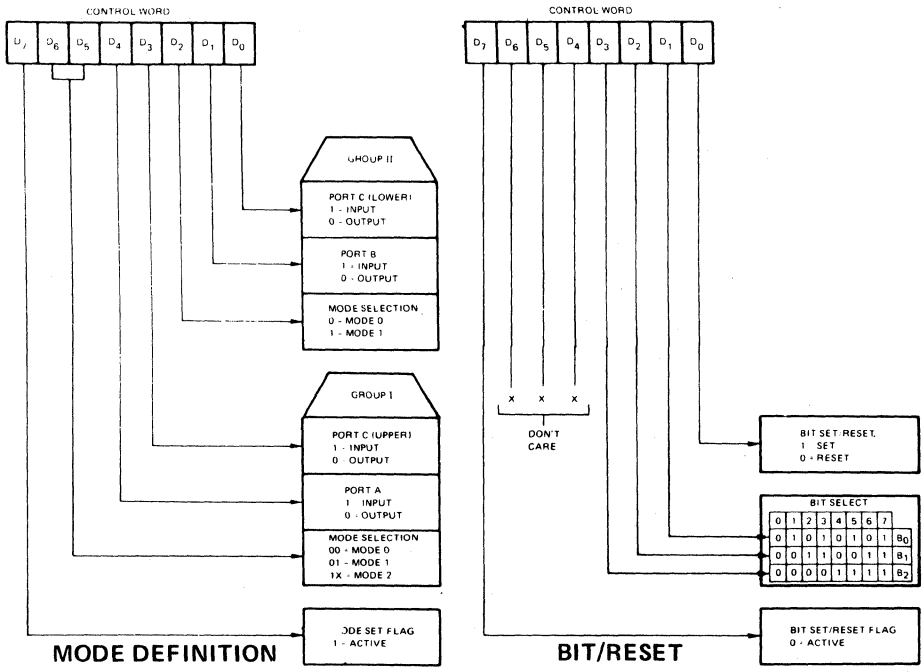
INPUT OPERATION (READ)					
A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	0	1	0	PORT A → DATA BUS
0	1	0	1	0	PORT B → DATA BUS
1	0	0	1	0	PORT C → DATA BUS

OUTPUT OPERATION (WRITE)					
A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	0	DATA BUS → PORT A
0	1	1	0	0	DATA BUS → PORT B
1	0	1	0	0	DATA BUS → PORT C
1	1	1	0	0	DATA BUS → CONTROL

DISABLE FUNCTION					
A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
X	X	X	X	1	DATA BUS → HIGH Z STATE
X	X	1	1	0	DATA BUS → HIGH Z STATE

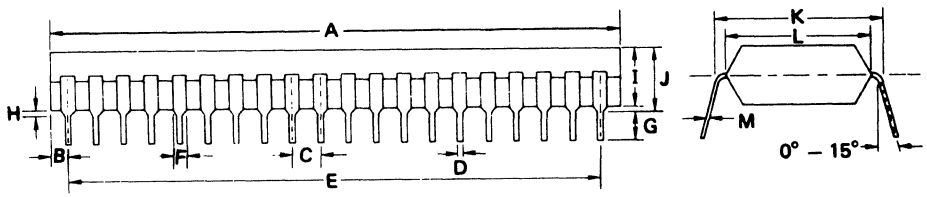
NOTES: ① X means "DO NOT CARE."
② All conditions not listed are illegal and should be avoided.

FORMATS



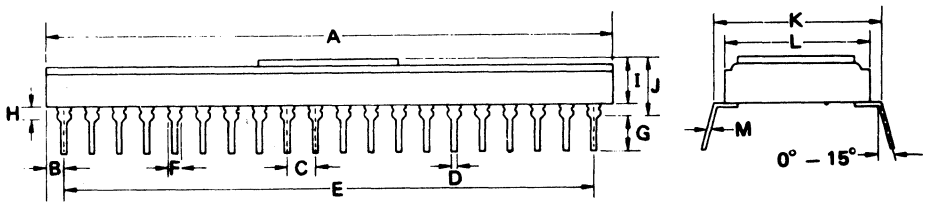
PACKAGE OUTLINE μPD8255C/D μPD8255AC/D-5

Members of the μPD8085 Family are housed in both plastic and ceramic 40 pin packages. The drawings and tables below apply to all five of the NEC Microcomputer parts covered in this data sheet.



Plastic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$



Ceramic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.100 ± 0.004
D	0.50 ± 0.1	0.0197 ± 0.004
E	48.26 ± 0.2	1.900 ± 0.008
F	1.27	0.050
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.17 MAX
J	5.2 MAX	0.205 MAX
K	15.24 ± 0.1	0.6 ± 0.004
L	$13.5^{+0.2}_{-0.25}$	$0.531^{+0.008}_{-0.010}$
M	0.30 ± 0.1	0.012 ± 0.004

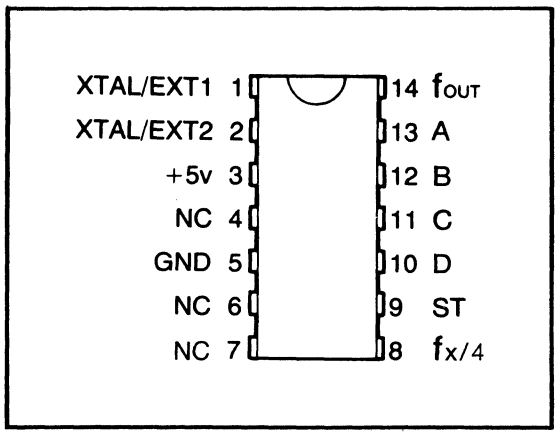
COM 8146
COM 8146T

Baud Rate Generator
Programmable Divider

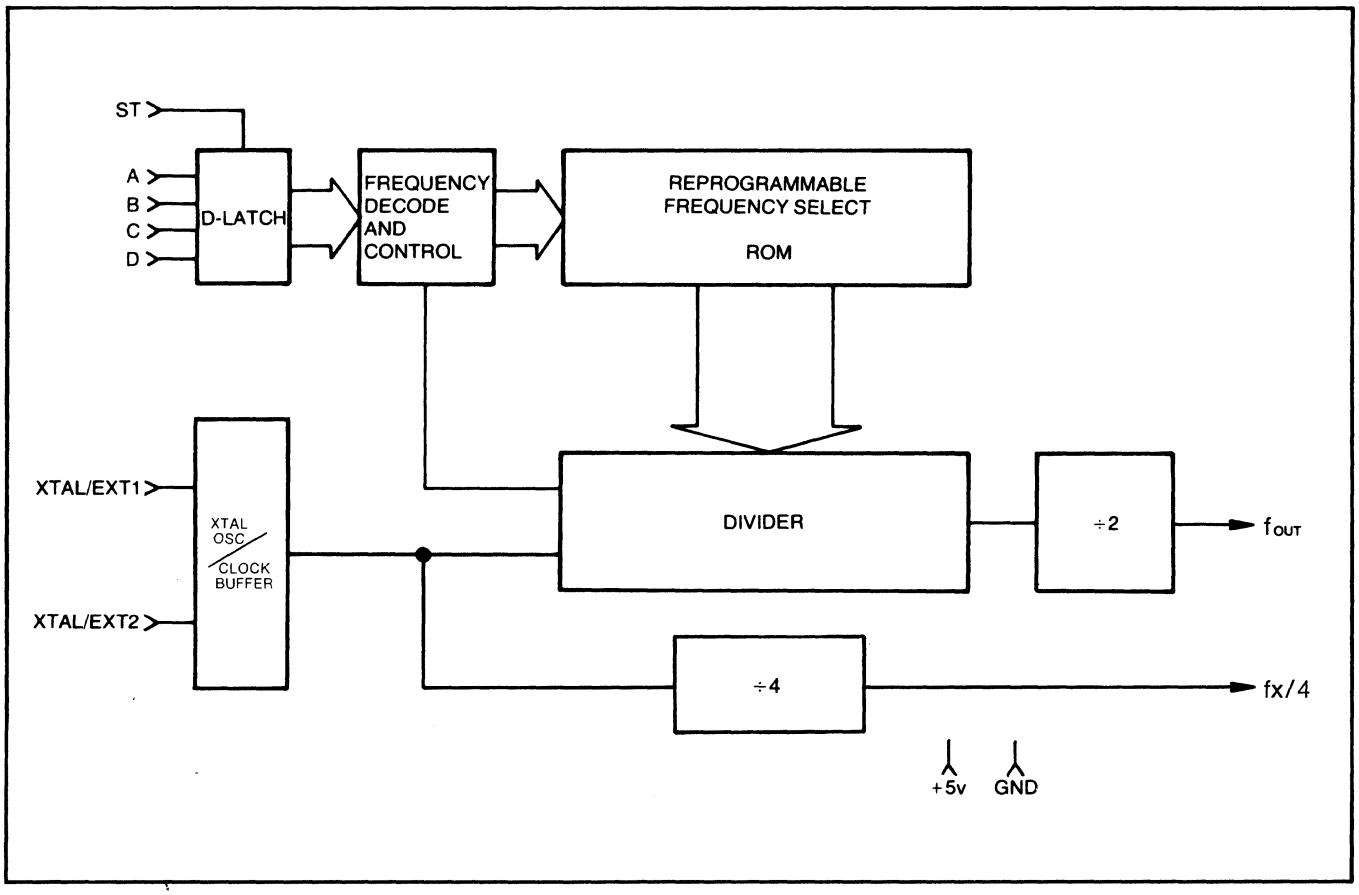
FEATURES

- ☐ On chip crystal oscillator or external frequency input
- ☐ Single +5v power supply
- ☐ Choice of 16 output frequencies
- ☐ 16 asynchronous/synchronous baud rates
- ☐ Direct UART/USRT/ASTRO/USYNRT compatibility
- ☐ High frequency reference output
- ☐ Re-programmable ROM via CLASP™ technology allows generation of other frequencies
- ☐ TTL, MOS compatibility
- ☐ Compatible with COM 5046

PIN CONFIGURATION



BLOCK DIAGRAM



General Description

The Standard Microsystem's COM 8146 is an enhanced version of the COM 5046 Baud Rate Generator. It is fabricated using SMC's patented COPLAMOS® and CLASP™ technologies and employs depletion mode loads, allowing operation from a single +5v supply.

The standard COM 8146 is specifically dedicated to generating the full spectrum of 16 asynchronous/synchronous data communication frequencies for 16X UART/USRT devices. A large number of the frequencies available are also useful for 1X and 32X ASTRO/USYNRT devices.

The COM 8146 features an internal crystal oscillator which may be used to provide the master reference frequency. Alternatively, an external reference may be supplied by applying complementary TTL level signals to pins 1 and 2. Parts suitable for use only with an external TTL reference are marked COM 8146T. TTL outputs used to drive the COM 8146 or COM 8146T XTAL/EXT inputs should not be used to drive other TTL inputs, as noise immunity may be compromised due to excessive loading.

The output of the oscillator/buffer is applied to the divider for generation of the output frequency. The divider is capable of dividing by any integer from 6 to $2^{19} + 1$, inclusive. If the divisor is even, the output will be square; otherwise the output will be high longer than it is low by one fx clock period.

The reference frequency (fx) is used to provide a high frequency output at fx/4.

The divisor ROM contains 16 divisors, each 19 bits wide, and is fabricated using SMC's unique CLASP™ technology. This process permits reduction of turnaround time for ROM patterns. The four divisor select bits are held in an externally strobed data latch. The strobe input is level sensitive: while the strobe is high, data is passed directly through to the ROM. Initiation of a new frequency is effected within 3.5μs of a change in any of the four divisor select bits (strobe activity is not required). This feature may be disabled through a CLASP™ programming option causing new frequency initiation to be delayed until the end of the current f_{OUT} half-cycle. The divisor select inputs have pull-up resistors; the strobe input does not.

Description of Pin Functions

Pin No.	Symbol	Name	Function
1	XTAL/EXT1	Crystal or External Input 1	This input is either one pin of the crystal package or one polarity of the external input.
2	XTAL/EXT2	Crystal or External Input 2	This input is either the other pin of the crystal package or the other polarity of the external input.
3	V_{CC}	Power Supply	+5 volt supply
4,6,7	NC	No Connection	
5	GND	Ground	Ground
8	$f_X/4$	$f_X/4$	¼ crystal/clock frequency reference output.
9	ST	Strobe	A high level strobe loads the input data (A, B, C, D) into the input divisor select register. This input may be strobed or hard-wired to a high level.
10-13	D,C,B,A	Divisor Select Data Bits	The logic level on these inputs as shown in Table 1, selects the output frequency.
14	f_{OUT}	Output Frequency	This output runs at a frequency selected by the divisor select data bits.

8116T
Fin = 1.8432 MHZ

T_D	T_C	T_B	T_A	R_D	R_C	R_B	R_A	BAUD RATE
0	0	0	0	0	0	0	0	50
0	0	0	1	0	0	0	1	75
0	0	1	0	0	0	1	0	110
0	0	1	1	0	0	1	1	134.5
0	1	0	0	0	1	0	0	150
0	1	0	1	0	1	0	1	200
0	1	1	0	0	1	1	0	300
0	1	1	1	0	1	1	1	600
1	0	0	0	1	0	0	0	1200
1	0	0	1	1	0	0	1	1800
1	0	1	0	1	0	1	0	2000
1	0	1	1	1	0	1	1	2400
1	1	0	0	1	1	0	0	3600
1	1	0	1	1	1	0	1	4800
1	1	1	0	1	1	1	0	9600
1	1	1	1	1	1	1	1	19200

Standard Microsystems Corporation
35 Marcus Boulevard
Hauppauge, New York 11787
(516) 273-3100
TWX: 510-227-8898

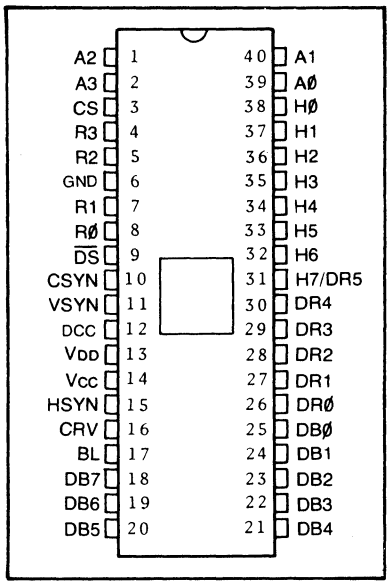
CRT 5027
CRT 5037
μPC FAMILY

CRT Video Timer-Controller VTAC®

FEATURES

- ☐ Fully Programmable Display Format
  - Characters per data row (1-200)
  - Data rows per frame (1-64)
  - Raster scans per data row (1-16)
- ☐ Programmable Monitor Sync Format
  - Raster Scans/Frame (256-1023)
  - "Front Porch"
  - Sync Width
  - "Back Porch"
  - Interlace/Non-Interlace
  - Vertical Blanking
- ☐ Direct Outputs to CRT Monitor
  - Horizontal Sync
  - Vertical Sync
  - Composite Sync
  - Blanking
  - Cursor coincidence
- ☐ Programmed via:
  - Processor data bus
  - External PROM
  - Mask Option ROM
- ☐ Standard or Non-Standard CRT Monitor Compatible
- ☐ Refresh Rate: 60Hz, 50Hz,...
- ☐ Scrolling
  - Single Line
  - Multi-Line
- ☐ Cursor Position Registers
- ☐ Character Format: 5x7, 7x9,...
- ☐ Programmable Vertical Data Positioning
- ☐ Balanced Beam Current Interlace (CRT 5037)

PIN CONFIGURATION



- ☐ Split-Screen Applications
  - Horizontal
  - Vertical
- ☐ Graphics Compatible
- ☐ Interlace or Non-Interlace operation
- ☐ TTL Compatibility
- ☐ BUS Oriented
- ☐ High Speed Operation
- ☐ COPLAMOS® N-Channel Silicon Gate Technology
- ☐ Compatible with CRT 8002 VDAC™
- ☐ Compatible with CRT 7004

General Description

The CRT Video Timer-Controller Chip (VTAC)® is a user programmable 40-pin COPLAMOS® n channel MOS/LSI device containing the logic functions required to generate all the timing signals for the presentation and formatting of interlaced and non-interlaced video data on a standard or non-standard CRT monitor.

With the exception of the dot counter, which may be clocked at a video frequency above 25 MHz and therefore not recommended for MOS implementation, all frame formatting, such as horizontal, vertical, and composite sync, characters per data row, data rows per frame, and raster scans per data row and per frame are totally user programmable. The data row counter has been designed to facilitate scrolling.

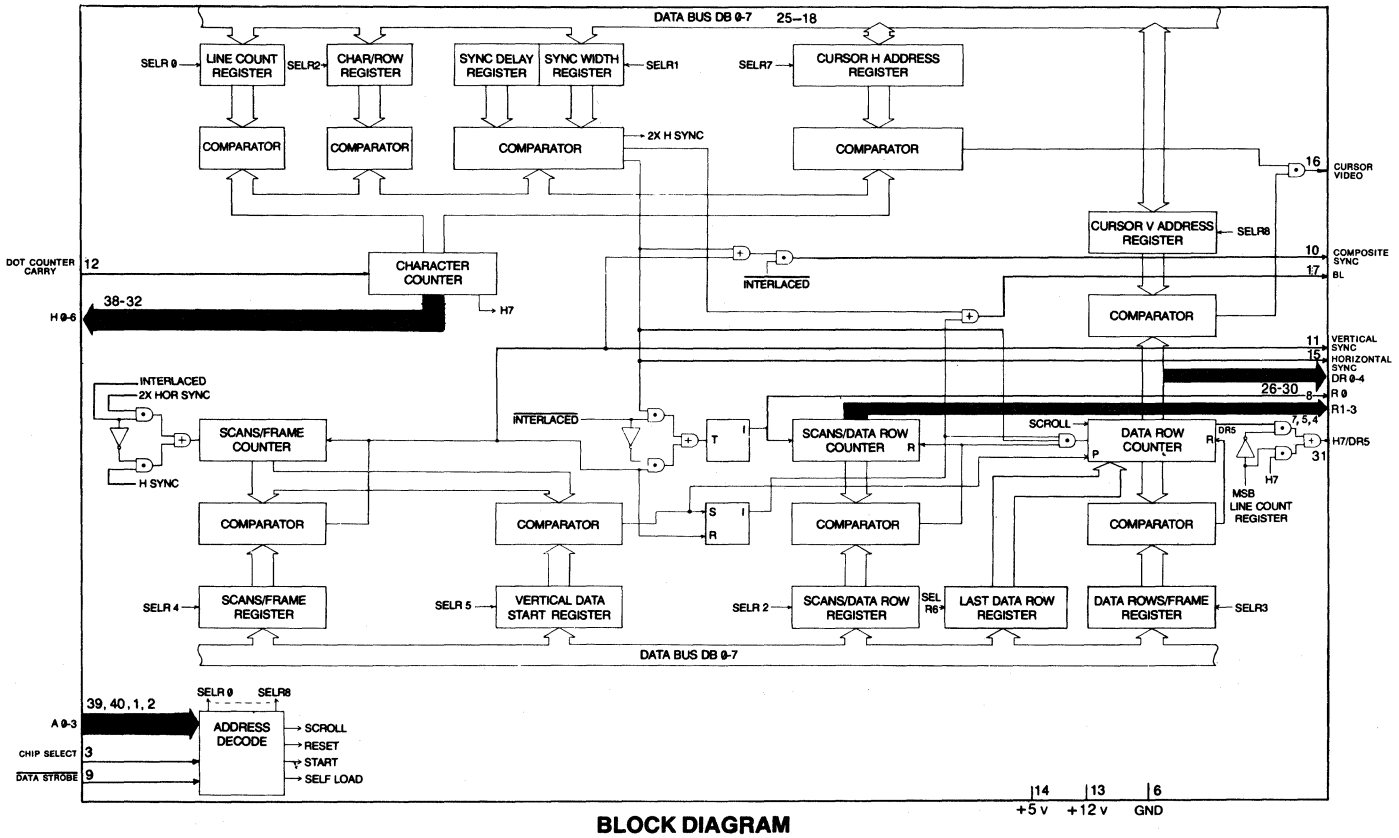
Programming is effected by loading seven 8 bit control registers directly off an 8 bit bidirectional data bus. Four register address lines and a chip select line provide complete microprocessor compatibility for program controlled set up. The device can be "self loaded" via an external PROM tied on the data bus as described in the OPERATION section. Formatting can also be programmed by a single mask option.

In addition to the seven control registers two additional registers are provided to store the cursor character and data row addresses for generation of the cursor video signal. The contents of these two registers can also be read out onto the bus for update by the program.

Two versions of the VTAC® are available. The CRT 5027 provides non-interlaced operation with an even or odd number of scan lines per data row, or interlaced operation with an even number of scan lines per data row. The CRT 5037 may be programmed for an odd or even number of scan lines per data row in both interlaced and non-interlaced modes. Programming the CRT 5037 for an odd number of scan lines per data row eliminates character distortion caused by the uneven beam current normally associated with odd field/even field interlacing of alphanumeric displays.

Description of Pin Functions

Pin No.	Symbol	Name	Input/ Output	Function
25-18	DBØ–7	Data Bus	I/O	Data bus. Input bus for control words from microprocessor or PROM. Bidirectional bus for cursor address.
3	CS	Chip Select	I	Signals chip that it is being addressed
39, 40, 1, 2	AØ-3	Register Address	I	Register address bits for selecting one of seven control registers or either of the cursor address registers
9	$\overline{DS}$	Data Strobe	I	Strobes DBØ-7 into the appropriate register or outputs the cursor character address or cursor line address onto the data bus
12	DCC	DOT Counter Carry	I	Carry from off chip dot counter establishing basic character clock rate. Character clock.
38-32	HØ-6	Character Counter Outputs	O	Character counter outputs.
7, 5, 4	R1-3	Scan Counter Outputs	O	Three most significant bits of the Scan Counter; row select inputs to character generator.
31	H7/DR5	H7/DR5	O	Pin definition is user programmable. Output is MSB of Character Counter if horizontal line count (REG.Ø) is ≧128; otherwise output is MSB of Data Row Counter.
8	RØ	Scan Counter LSB	O	Least significant bit of the scan counter. In the interlaced mode with an even number of scans per data row, RØ will toggle at the field rate; for an odd number of scans per data row in the interlaced mode, RØ will toggle at the data row rate.
26-30	DRØ-4	Data Row Counter Outputs	O	Data Row counter outputs.
17	BL	Blank	O	Defines non active portion of horizontal and vertical scans.
15	HSYN	Horizontal Sync	O	Initiates horizontal retrace.
11	VSYN	Vertical Sync	O	Initiates vertical retrace.
10	CSYN	Composite Sync	O	Active in non-interlaced mode only. Provides a true RS-170 composite sync waveform.
16	CRV	Cursor Video	O	Defines cursor location in data field.
14	V_{CC}	Power Supply	PS	+5 volt Power Supply
13	V_{DD}	Power Supply	PS	+12 volt Power Supply



BLOCK DIAGRAM

Operation

The design philosophy employed was to allow the device to interface effectively with either a microprocessor based or hardwire logic system. The device is programmed by the user in one of two ways; via the processor data bus as part of the system initialization routine, or during power up via a PROM tied on the data bus and addressed directly by the Row Select outputs of the chip. (See figure 4). Seven 8 bit words are required to fully program the chip. Bit assignments for these words are shown in Table 1. The information contained in these seven words consists of the following:

Horizontal Formatting:

Characters/Data Row	A 3 bit code providing 8 mask programmable character lengths from 20 to 132. The standard device will be masked for the following character lengths; 20, 32, 40, 64, 72, 80, 96, and 132.
Horizontal Sync Delay	3 bits assigned providing up to 8 character times for generation of "front porch".
Horizontal Sync Width	4 bits assigned providing up to 16 character times for generation of horizontal sync width.
Horizontal Line Count	8 bits assigned providing up to 256 character times for total horizontal formatting.
Skew Bits	A 2 bit code providing from a 0 to 2 character skew (delay) between the horizontal address counter and the blank and sync (horizontal, vertical, composite) signals to allow for retiming of video data prior to generation of composite video signal. The Cursor Video signal is also skewed as a function of this code.

Vertical Formatting:

Interlaced/Non-interlaced	This bit provides for data presentation with odd/even field formatting for interlaced systems. It modifies the vertical timing counters as described below. A logic 1 establishes the interlace mode.
Scans/Frame	8 bits assigned, defined according to the following equations: Let X = value of 8 assigned bits. 1) in interlaced mode—scans/frame = 2X + 513. Therefore for 525 scans, program X = 6 (00000110). Vertical sync will occur precisely every 262.5 scans, thereby producing two interlaced fields. Range = 513 to 1023 scans/frame, odd counts only. 2) in non-interlaced mode—scans/frame = 2X + 256. Therefore for 262 scans, program X = 3 (00000011). Range = 256 to 766 scans/frame, even counts only. In either mode, vertical sync width is fixed at three horizontal scans (≡ 3H).
Vertical Data Start	8 bits defining the number of raster scans from the leading edge of vertical sync until the start of display data. At this raster scan the data row counter is set to the data row address at the top of the page.
Data Rows/Frame	6 bits assigned providing up to 64 data rows per frame.
Last Data Row	6 bits to allow up or down scrolling via a preload defining the count of the last displayed data row.
Scans/Data Row	4 bits assigned providing up to 16 scan lines per data row.

Additional Features

Device Initialization:

Under microprocessor control—The device can be reset under system or program control by presenting a 1Ø1Ø address on A3-Ø. The device will remain reset at the top of the even field page until a start command is executed by presenting a 111Ø address on A3-Ø.

Via "Self Loading"—In a non-processor environment, the self loading sequence is effected by presenting and holding the 1111 address on A3-Ø, and is initiated by the receipt of the strobe pulse ($\overline{DS}$). The 1111 address should be maintained long enough to insure that all seven registers have been loaded (in most applications under one millisecond). The timing sequence will begin one line scan after the 1111 address is removed. In processor based systems, self loading is initiated by presenting the Ø111 address to the device. Self loading is terminated by presenting the start command to the device which also initiates the timing chain.

Scrolling—In addition to the Register 6 storage of the last displayed data row a "scroll" command (address 1Ø11) presented to the device will increment the first displayed data row count to facilitate up scrolling in certain applications.

Control Registers Programming Chart

Horizontal Line Count: Total Characters/Line = N+1, N=0 to 255 (DBØ=LSB)

Characters/Data Row:

DB2	DB1	DBØ		
0	0	0	= 20	Active Characters/Data Row
0	0	1	= 32	
0	1	0	= 40	
0	1	1	= 64	
1	0	0	= 72	
1	0	1	= 80	
1	1	0	= 96	
1	1	1	= 132	

Horizontal Sync Delay: =N, from 1 to 7 character times (DBØ=LSB) (N=0 Disallowed)

Horizontal Sync Width: =N, from 1 to 15 character times (DB3=LSB) (N=0 Disallowed)

Skew Bits

DB7	DB6	Sync/Blank Delay (Character Times)	Cursor Delay
0	0	0	0
1	0	1	0
0	1	2	1
1	1	2	2

Scans/Frame

8 bits assigned, defined according to the following equations: Let X = value of 8 assigned bits. (DBØ=LSB)

1) in interlaced mode—scans/frame = 2X + 513. Therefore for 525 scans, program X = 6 (00000110). Vertical sync will occur precisely every 262.5 scans, thereby producing two interlaced fields.
Range = 513 to 1023 scans/frame, odd counts only.

2) in non-interlaced mode—scans/frame = 2X + 256. Therefore for 262 scans, program X = 3 (00000011).
Range = 256 to 766 scans/frame, even counts only.

In either mode, vertical sync width is fixed at three horizontal scans (≡3H).

Vertical Data Start: N= number of raster lines delay after leading edge of vertical sync of vertical start position. (DBØ=LSB)

Data Rows/Frame: Number of data rows = N+1, N=0 to 63 (DBØ=LSB)

Last Data Row: N= Address of last displayed data row, N=0 to 63, ie; for 24 data rows, program N=23. (DBØ=LSB)

Mode: Register 1, DB7=1 establishes Interlace.

Scans/Data Row:

Interlace Mode

CRT 5027: Scans per Data Row=N+1 where N=programmed number of data rows. N=0 to 15. Scans per data row must be even counts only.

CRT 5037: Scans per data Row=N+2. N=0 to 14, odd or even counts.

Non-Interlace Mode

CRT 5027, CRT 5037: Scans per Data Row=N+1 odd or even count. N=0 to 15.

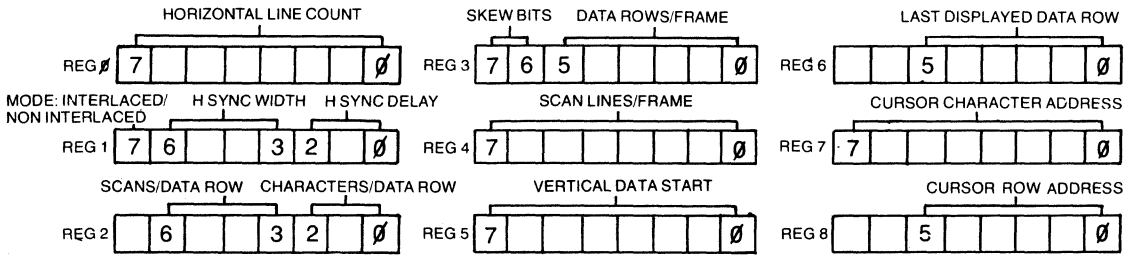
Register Selects/Command Codes

A3	A2	A1	AØ	Select/Command	Description
0	0	0	0	Load Control Register Ø	See Table 1
0	0	0	1	Load Control Register 1	
0	0	1	0	Load Control Register 2	
0	0	1	1	Load Control Register 3	
0	1	0	0	Load Control Register 4	
0	1	0	1	Load Control Register 5	
0	1	1	0	Load Control Register 6	
0	1	1	1	Processor Initiated Self Load	Command from processor instructing VTAC® to enter Self Load Mode (via external PROM)
1	0	0	0	Read Cursor Line Address	
1	0	0	1	Read Cursor Character Address	
1	0	1	0	Reset	Resets timing chain to top left of page. Reset is latched on chip by $\overline{DS}$ and counters are held until released by start command.
1	0	1	1	Up Scroll	Increments address of first displayed data row on page. ie; prior to receipt of scroll command—top line = 0, bottom line = 23. After receipt of Scroll Command—top line = 1, bottom line = 0.
1	1	0	0	Load Cursor Character Address*	
1	1	0	1	Load Cursor Line Address*	
1	1	1	0	Start Timing Chain	Receipt of this command after a Reset or Processor Self Load command will release the timing chain approximately one scan line later. In applications requiring synchronous operation of more than one CRT 5027 the dot counter carry should be held low during the $\overline{DS}$ for this command.
1	1	1	1	Non-Processor Self Load	Device will begin self load via PROM when $\overline{DS}$ goes low. The 1111 command should be maintained on A3-Ø long enough to guarantee self load. (Scan counter should cycle through at least once). Self load is automatically terminated and timing chain initiated when the all "1's" condition is removed, independent of $\overline{DS}$. For synchronous operation of more than one VTAC®, the Dot Counter Carry should be held low when the command is removed.

*NOTE: During Self-Load, the Cursor Character Address Register (REG 7) and the Cursor Row Address Register (REG 8) are enabled during states Ø111 and 1ØØØ of the R3-RØ Scan Counter outputs respectively. Therefore, Cursor data in the PROM should be stored at these addresses.

TABLE 1

BIT ASSIGNMENT CHART



AC TIMING DIAGRAMS

FIGURE 1 VIDEO TIMING

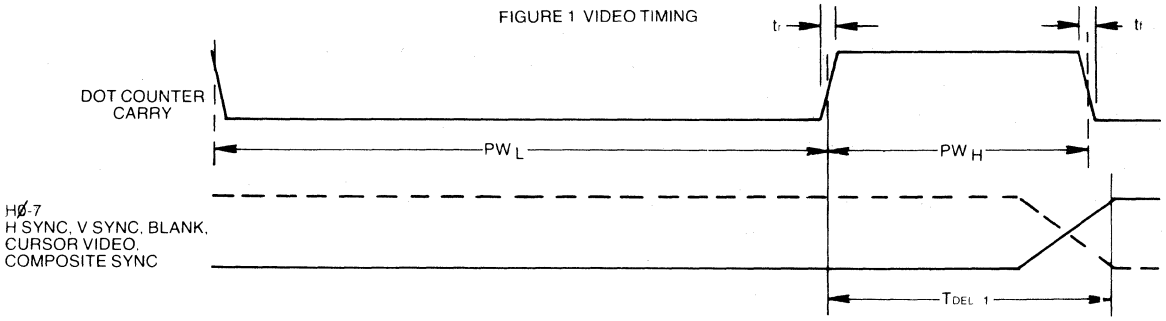


FIGURE 2 LOAD/READ TIMING

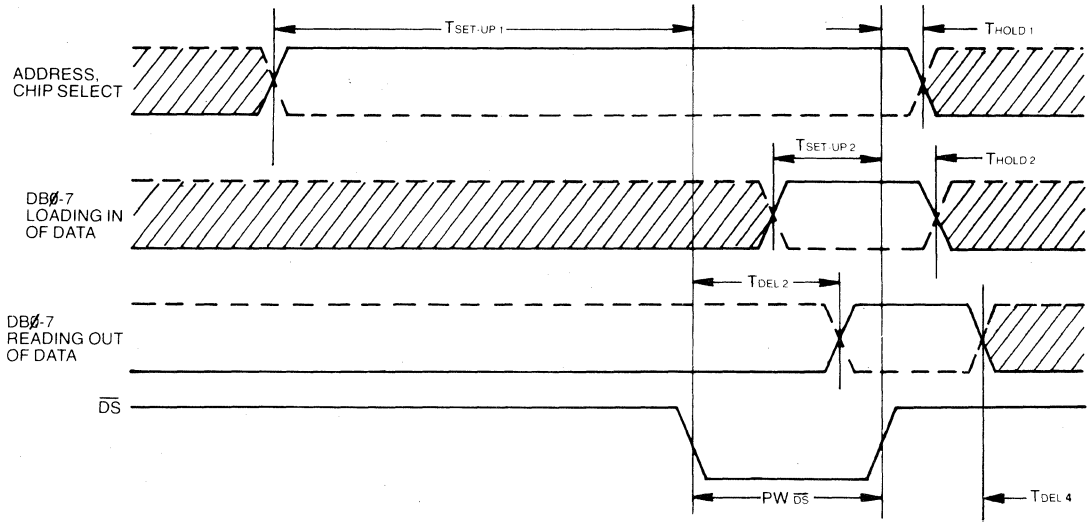
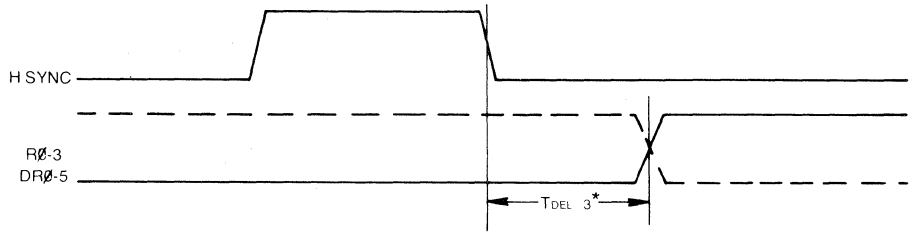
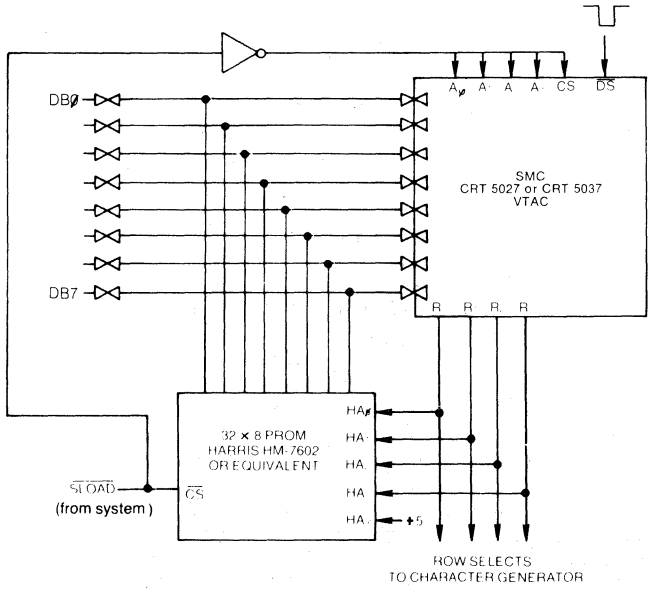


FIGURE 3 SCAN AND DATA ROW COUNTER TIMING



*RØ-3 and DRØ-5 may change prior to the falling edge of H sync

Figure 4. SELF LOADING SCHEME FOR VTAC SET-UP



MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +18.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. For example, the bench power supply programmed to deliver +12 volts may have large voltage transients when the AC power is switched on and off. If this possibility exists it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C, V_{CC}=+5V±5%, V_{DD}=+12V±5%, unless otherwise noted)

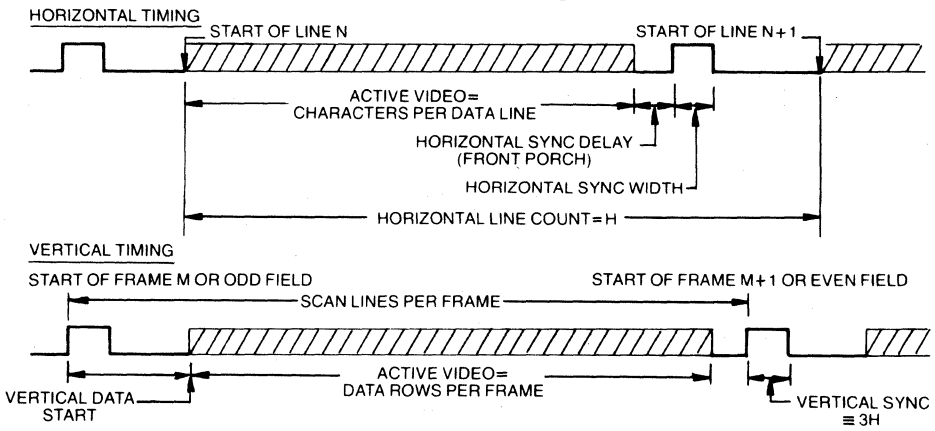
Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low Level, V_{IL}			0.8	V	
High Level, V_{IH}	V_{CC}−1.5		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low Level—V_{OL} for RØ-3			0.4	V	I_{OL}=3.2ma
Low Level—V_{OL} all others			0.4	V	I_{OL}=1.6ma
High Level—V_{OH} for RØ-3, DBØ-7	2.4				I_{OH}=80μa
High Level—V_{OH} all others	2.4				I_{OH}=40μa
INPUT CURRENT					
Low Level, I_{IL}			250	μA	V_{IN}=0.4V
High Level, I_{IH}			10	μA	$V_{IN}=V_{CC}$
INPUT CAPACITANCE					
Data Bus, C_{IN}		10	15	pF	
$\overline{DS}$, Clock, C_{IN}		25	40	pF	
All other, C_{IN}		10	15	pF	
DATA BUS LEAKAGE in INPUT MODE					
I_{DB}			10	μA	$0.4V \leq V_{IN} \leq 5.25V$
POWER SUPPLY CURRENT					
I_{CC}		80	100	mA	
I_{DD}		40	60	mA	
A.C. CHARACTERISTICS					T_A = 25°C
DOT COUNTER CARRY					
frequency	0.2		4.0	MHz	Figure 1
PW_H	35			ns	Figure 1
PW_L	215			ns	Figure 1
tr, tf		10	50	ns	Figure 1
DATA STROBE					
$PW_{\overline{DS}}$	150ns		10μs		Figure 2
ADDRESS, CHIP SELECT					
Set-up time	125			ns	Figure 2
Hold time	50			ns	Figure 2
DATA BUS—LOADING					
Set-up time	125			ns	Figure 2
Hold time	75			ns	Figure 2
DATA BUS—READING					
T_{DEL2}			125	ns	Figure 2, CL=50pF
T_{DEL4}	5		60	ns	Figure 2, CL=50pF
OUTPUTS: HØ-7, HS, VS, BL, CRV, CS-T_{DEL1}			125	ns	Figure 1, CL=20pF
OUTPUTS: RØ-3, DRØ-5					
T_{DEL3}	*		500	ns	Figure 3, CL=20pF

*RØ-3 and DRØ-5 may change prior to the falling edge of H sync

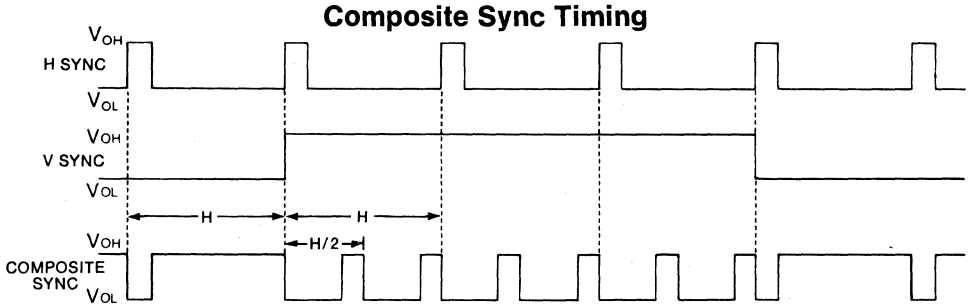
Restrictions

1. Only one pin is available for strobing data into the device via the data bus. The cursor X and Y coordinates are therefore loaded into the chip by presenting one set of addresses and outputed by presenting a different set of addresses. Therefore the standard WRITE and READ control signals from most microprocessors must be "NORed" externally to present a single strobe ($\overline{DS}$) signal to the device.
2. In interlaced mode the total number of character slots assigned to the horizontal scan must be even to insure that vertical sync occurs precisely between horizontal sync pulses.

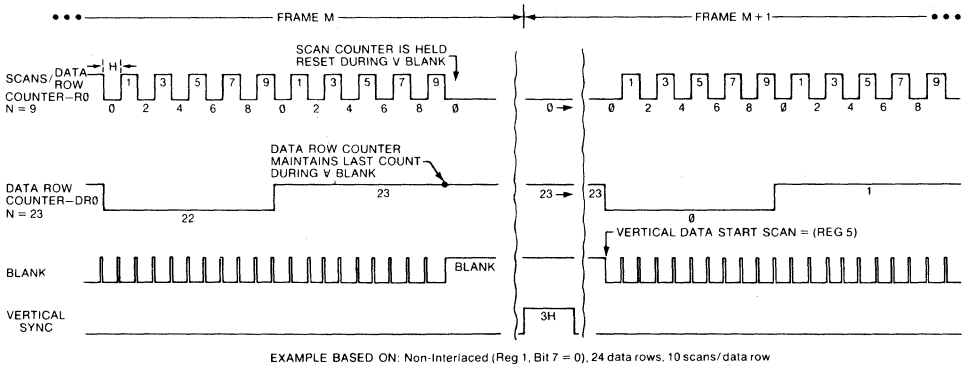
General Timing



Composite Sync Timing



Vertical Sync Timing



EXAMPLE BASED ON: Non-Interlaced (Reg 1, Bit 7 = 0), 24 data rows, 10 scans/data row

Start-up, CRT 5027

When employing microprocessor controlled loading of the CRT 5027's registers, the following sequence of instructions is necessary:

ADDRESS	COMMAND
1 1 1 0	Start Timing Chain
1 0 1 0	Reset
0 0 0 0	Load Register 0
.	.
.	.
.	.
0 1 1 0	Load Register 6
1 1 1 0	Start Timing Chain

The sequence of START RESET LOAD START is necessary to insure proper initialization of the registers.

This sequence is not required if register loading is via either of the Self Load modes. This sequence is optional with the CRT 5037.

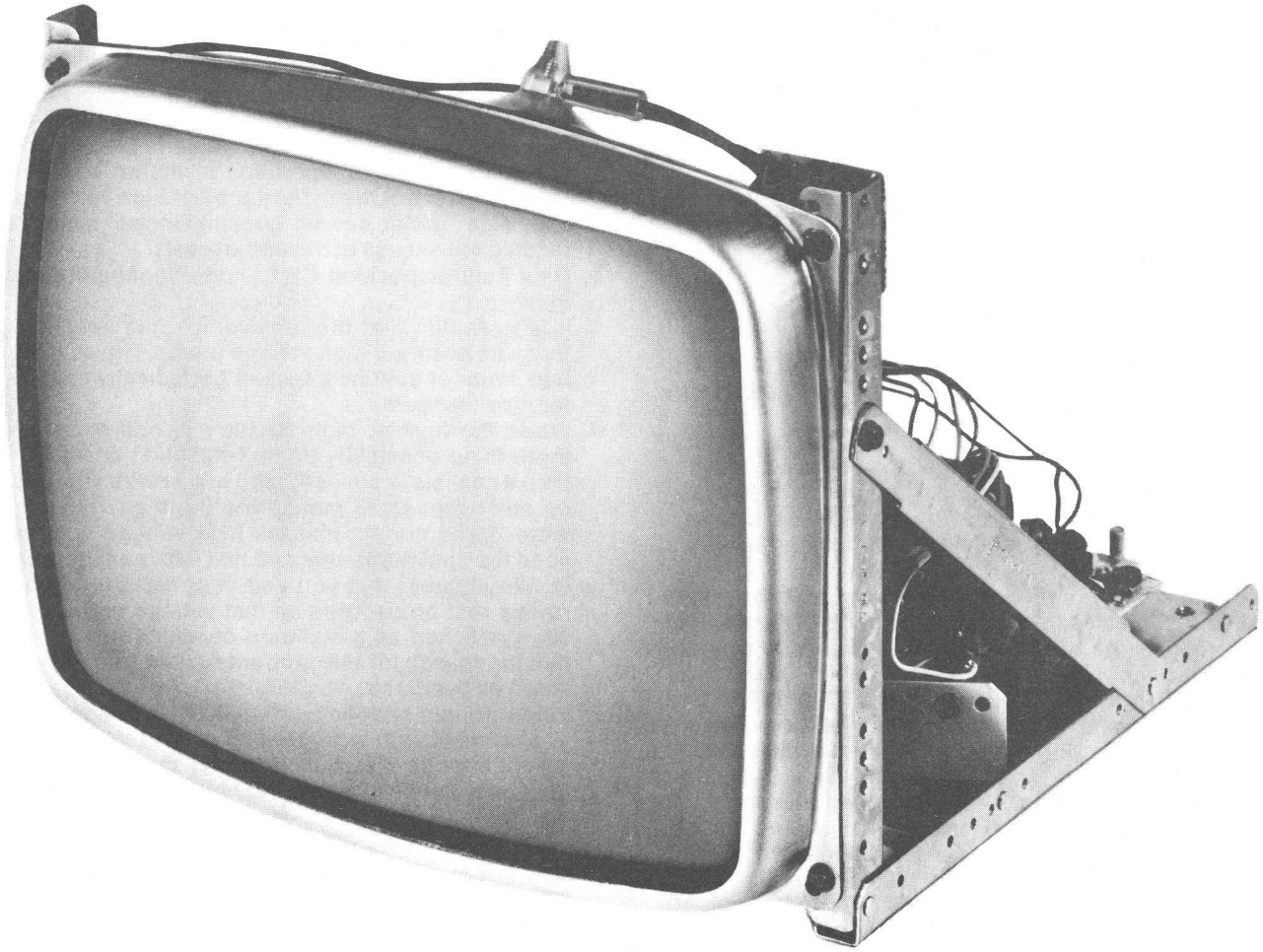
Standard Microsystems Corporation
35 Marcus Blvd., Hauppauge, N.Y. 11787 Phone (516) 273-3100 TWX 510-227-8898

7.0 TV MONITOR

DT2

DT2

SERVICE MANUAL



DT2

D12 SERIES DATA DISPLAY TERMINALS

ZENITH RADIO CORPORATION

1000 MILWAUKEE AVENUE, GLENVIEW, ILLINOIS 60025

DT2
2MRR

PRINTED IN U. S. A.
AUG, 1979

$2.00
923-951

PRODUCT SAFETY SERVICING GUIDELINES FOR ZENITH DATA DISPLAY TERMINALS

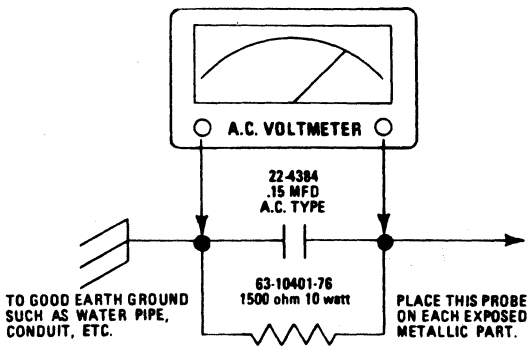
CAUTION: No modification of any circuit should be attempted. Service work should be performed only after you are thoroughly familiar with all of the following safety checks and servicing guidelines. To do otherwise increases the risk of potential hazards and injury to the user.

SAFETY CHECKS

After the original service problem has been corrected, a check should be made of the following:

SUBJECT: FIRE & SHOCK HAZARD

1. Be sure that all components are positioned in such a way to avoid possibility of adjacent component shorts. This is especially important on those chassis which are transported to and from the repair shop.
2. Never release a repair unless all protective devices such as insulators, barriers, covers, shields, strain reliefs, and other hardware have been reinstalled per original design.
3. Soldering must be inspected to uncover possible cold solder joints, frayed leads, damaged insulation, solder splashes or sharp solder points. Be certain to remove all loose foreign material.
4. Check "across-the-line" capacitor (if used) and other components for physical evidence of damage or deterioration and replace if necessary. Follow original layout, lead length and dress.
5. No lead or component should touch a resistor rated at 1 watt or more. Lead tension around protruding metal surfaces must be avoided.
6. All critical components (shaded on the schematic diagram and parts lists) such as: fuses, flameproof resistors, capacitors, etc., must be replaced with exact Zenith types. Do not use replacement components other than those specified or make unrecommended circuit modifications.
7. After re-assembly of the terminal always perform an AC leakage test on all exposed metallic parts of the cabinet and screws to be sure the terminal is safe to operate without danger of electrical shock. DO NOT USE A LINE ISOLATION TRANSFORMER DURING THIS TEST. Use an AC voltmeter having 5000 ohms per volt or more sensitivity in the following manner: Connect a 1500 ohm 10 watt resistor (63-10401-76), paralleled by a 0.15 mfd., 150V AC type capacitor (22-4384) between a known good earth ground (water pipe, conduit, etc.) and the exposed metallic parts, one at a time. Measure the AC voltage across the combination 1500 ohm resistor and 0.15 mfd. capacitor. Reverse the AC plug and repeat AC voltage measurements for each exposed metallic part. Voltage measured must not exceed 0.75 volts RMS. This corresponds to 0.5 milliamp AC. Any value exceeding this limit constitutes a potential shock hazard and must be corrected immediately.



SUBJECT: IMPLOSION PROTECTION

1. All Zenith picture tubes are equipped with an integral implosion protection system, but care should be taken to avoid damage during installation. Avoid scratching the tube.
2. Use only Zenith replacement tubes.

SUBJECT: X-RADIATION

1. Be sure procedures and instructions to all service personnel cover the subject of X-radiation. The only potential source of X-rays is the picture tube. However, this tube does not emit X-rays when the HV is at the factory-specified level. It is only when the HV is excessive that X-radiation can be generated. The basic precaution which must be exercised is to keep the HV at the factory-recommended level. Refer to the X-ray Precaution Label which is located inside each terminal for the correct high voltage. The proper value is also given in the schematic diagram. Operation at higher voltages may cause a failure of the picture tube or high voltage supply and, also, under certain circumstances, may produce radiation in excess of desirable levels.
2. Only Zenith-specified CRT anode connectors must be used.
3. It is essential that the serviceman has available at all times an accurate high voltage meter. The calibration of this meter should be checked periodically against a reference standard.
4. When the high voltage circuitry is operating properly there is no possibility of an X-radiation problem. Every time a chassis is serviced, the brightness should be run up and down while monitoring the high voltage with a meter to be certain that the high voltage does not exceed the specified value and that it is regulating correctly. We suggest that you and your service organization review test procedures so that voltage regulation is always checked as a standard servicing procedure, and that the reason for this prudent routine be clearly understood by everyone.
5. When trouble shooting and making test measurements in a terminal with a problem of excessive high voltage, do not operate the chassis longer than is necessary to locate the cause of excessive voltage.

IMPORTANT NOTE: DAG GROUNDING.

Each unit provides for grounding of the main P.C. Board and CRT socket board to the dag of the CRT through the dag grounding spring.

The ground wires are connected to the shell bond or T-band through a terminal lug. Upon installing the Video Display in a terminal, this grounding procedure should be followed to provide adequate high voltage filtering and arc protection. This especially pertains to mounting the video display as a kit version.

CAUTION

NO WORK SHOULD BE ATTEMPTED ON ANY EXPOSED MONITOR CHASSIS BY ANYONE NOT FAMILIAR WITH SERVICING PROCEDURES AND PRECAUTIONS.

GENERAL INFORMATION

This service manual introduces the Zenith D12 series of Video Displays. The series includes three basic forms: the D12-PF which is complete with power supply and frame, the D12-NF without power supply, the D12-NK in kit form which comes without frame or power supply.

The D12 series incorporate precision CRT's which provide uniformity of display and controlled spot size and geometry. The display may be operated from a standard 15 volt D.C. supply (or optional 12 V.D.C.) or from 120 volts A.C.

Input and output connections for the displays are made through a 10 pin edge connector on the main circuit board. Provision has been made for an optional remote brightness control. Schematic reference numbers are printed on the circuit board to aid in the location and identification of components for servicing.

Vertical and horizontal linearity is maintained within specifications without the use of linearity controls or adjustable devices. Excellent vertical linearity is assured by the extensive use of current feedback and horizontal linearity is achieved with a fixed saturable reactor.

Vertical and horizontal deflection systems sustain scan even in the absence or interruption of synchronizing signals. Vertical and horizontal synchronization is automatic and stable throughout the entire specified operating frequency range.

SPECIFICATIONS

CATHODE RAY TUBE

12" diagonal measure, 90° deflection, I2.5KV nominal high voltage at 50μ A. beam current. Available with bonded anti-reflective face plate option. P4 phosphor is standard and other EIA phosphors are available.

NOMINAL DISPLAY AREA

5I sq. in. defined by a rectangle 8 1/2" × 6" centered on the CRT. (Other display dimensions optional.)

INPUT SIGNALS (TTL LEVEL)

HORIZONTAL
4 to 40μ sec. duration (positive going standard).
VERTICAL
50 to 2500μ sec. duration (negative going standard).
VIDEO
1.0V to 2.5V P-P (internal or customer supplied 500Ω contast control for higher input levels).
Positive polarity for white characters. (Other polarities are available for horizontal and vertical sync.)

POWER SUPPLY

120V ± 10% or 240V ± 10%
(customer strappable) 47 to 63 Hz., or
15V DC at 800 ma. max., or
12V DC at 1100 ma. max.

BRIGHTNESS CONTROL

Internal or Customer supplied 100 KΩ potentiometer (accessible at pins 2, 3 and 4 of edge connector).

INTERCONNECT TO CUSTOMER SYSTEM

Via standard 10-pin edge connector.
VIKING #25V10S/1-2
AMP #225-21031-101
CINCH #250-10-30-170

RESOLUTION

900 vertical lines minimum at center of display and 700 vertical lines at the corners. Pulse rise time less than 20 nanoseconds, for 30V rise at CRT. Bandwidth is within 3db from 10 Hz. to 18 MHz.

GEOMETRY

NOTE: Measurements made with an input of 1.0-2.5V P-P and with the display adjusted to 6" highx8½" wide.

VERTICAL

a. Height of display at left side shall be within ± 2.0 percent of height at right side.
b. Top and bottom pincushion or barrel shall be within ±1.25% of the average height.

HORIZONTAL

a. Width of display at top shall be within ±2.5% of the width at bottom.
b. Side pincushion or barrel shall be within ± 1.0% of the average width.

LINEARITY

No character shall vary in width or height by more than ±10% of the average width or height of all the characters in a row or column respectively.No specific character shall vary in width or height more than ±10% of an adjacent character.

SYNCHRONIZATION

HORIZONTAL
15.75 ± 0.5KHz.
18.60 ± 0.5KHz. (Optional)
Horizontal Blanking
9.0μ sec. min.
Horizontal Phasing Control
11.0 μ sec. nominal range
VERTICAL
47 to 63 Hz.
VERTICAL RETRACE TIME
850μsec. max.

STORAGE

55° C. max. with bonded anti-reflective faceplate.
65° C. max. for plain faced CRT's.

ENVIRONMENT

Operating temperature
55° max. (free air temperature of display electronics).
Altitude
40,000 ft. + storage & shipment.
10,000 ft. max. operating.

WEIGHT

11.5 lbs. max. without optional power supply.
13.5 lbs. max. with optional power supply.
9.0 lbs. max. without frame.

THEORY OF OPERATION

POWER SUPPLY

Power Transformer TX201 is designed for use with 120V or 240V A.C. source. The secondary provides power to bridge rectifier (CR501, CR502, CR503 and CR504). The positive output of the bridge rectifier (junction of CR503 and CR504), forms the raw B+ supply (~ 20VDC).

Voltage regulation is accomplished in the negative leg of the power supply through a feedback network consisting of transistors QX501 and QX502 and their associated circuitry. The emitter voltage of QX501 is maintained by diodes CR505, CR506 and CR507. The base voltage is provided by potentiometer RX506.

If B+ increases, diodes CR505, CR506 and CR507 will draw more current to maintain the emitter voltage of QX501. Additionally, the voltage developed across RX506 will increase, resulting in a higher positive voltage at the base of QX501 which will result in less conduction. This reduces the base current of QX502 since QX501 provides the emitter/base current path for QX502. When QX502 conducts less, the voltage drop across Q502 is increased thus lowering B+.

If B+ decreases, diodes CR505, CR506 and CR507 will reduce conduction to maintain the emitter voltage of QX501. Additionally, the base voltage provided by RX506 will decrease. Less voltage on the base of QX501 will cause it to increase conduction, resulting in a greater emitter/base current flow in QX502. With this condition the voltage drop for Q502 is less and B+ is increased.

HORIZONTAL

The low-level horizontal section, which consists of transistors Q101 and Q102 (and associated circuitry), functions as a variable time delay monostable multivibrator. The input trigger for this circuit is provided by the horizontal drive pulse. The pulse is injected into the base or emitter (for either positive or negative pulse respectively) of Q101 through injection network C101, C111, R101, R110 and CR101. By varying the recovery time of the multivibrator, potentiometer R104 adjusts video information position (with respect to raster scan). Output of the monostable multivibrator, derived at the collector of Q102, is injected through a coupling network consisting of C110 and CR103. The resulting "Lock" signal is rereceived by one side of a precision astable multivibrator at the emitter of Q103. The astable multivibrator circuit is completed through Q104 and associated circuitry. This circuit will act as a free running oscillator until the "Lock" signal is received from the previous stage. Once locked, an output pulse is formed at the emitter of Q104 which is then D.C. coupled to the base of the horizontal driver transistor, Q105.

Remainder of the horizontal circuit is straightforward. Features to be noted are: Width and Linearity Coils LX102 and LX101 in series with the yoke (TX202). Linearity is fixed and an adjustable coil is provided for width. The linearity coil has a magnetically biased core which makes the inductance of the coil dependent upon its current. Pincushion and geometric corrections are made at the factory by the addition of rubber magnets around the plastic ring of the yoke. D.C. operation of 12 volts is accomplished by the (optional) addition of a boost circuit at the horizontal sweep transformer.

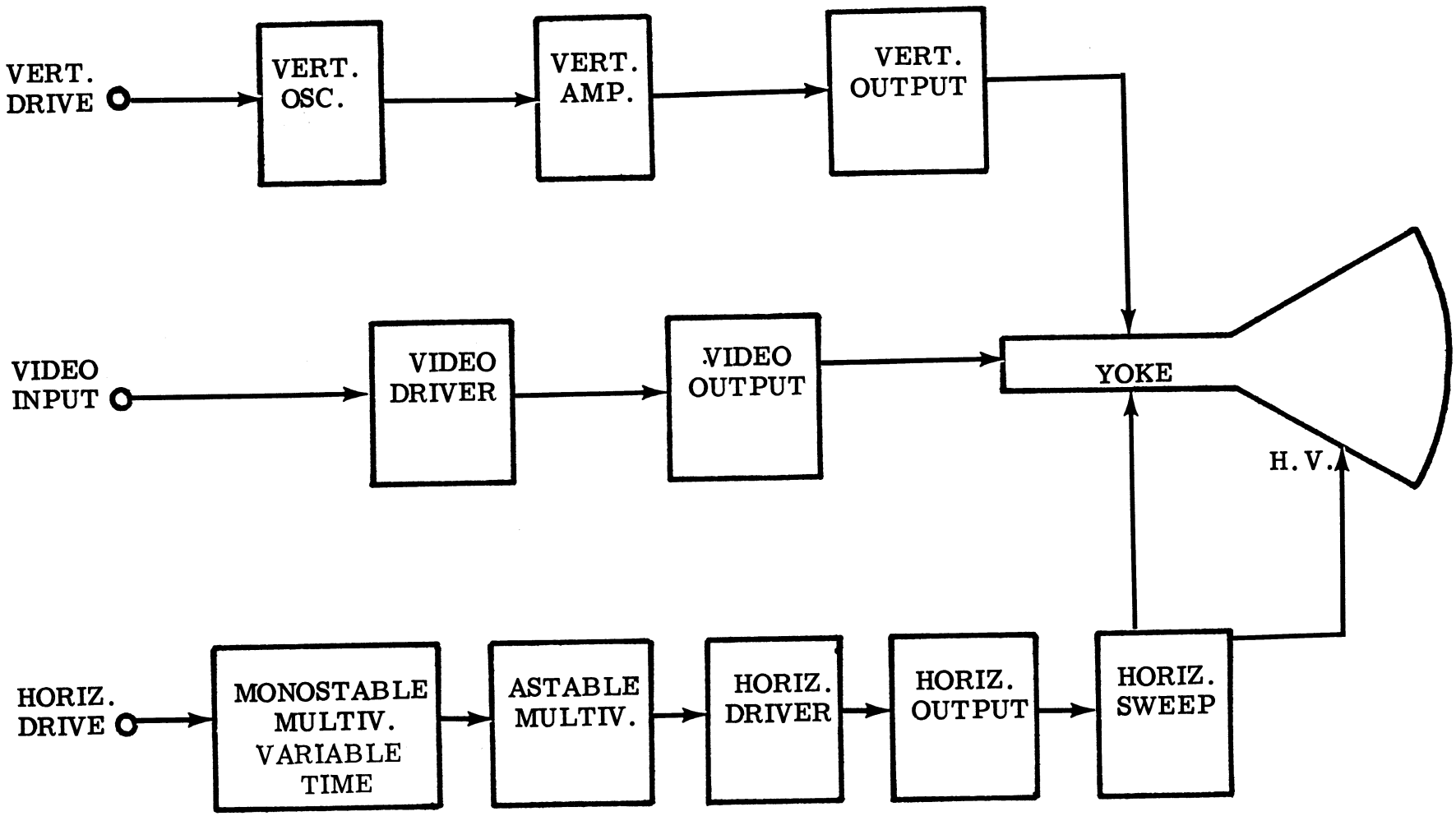
VERTICAL

The vertical circuit includes an oscillator consisting of transistors Q301 and Q302 and associated circuitry. Amplification is provided by transistors Q303 and Q304 with the emitter of Q304 feeding the base of the vertical driver Q305. The vertical output transistors, Q306 and Q307 are wired in the standard push-pull configuration. Transistor Q308 doubles B+ during retrace, maintaining less than 800 μ sec. of retrace time.

VIDEO

The video amplifier circuit consists of transistors Q401 and Q402 and associated circuitry. The circuit comprises a cascode amplifier which is triggered by a positive pulse at pin 8 of the edge connector. Upon receiving the input pulse, conduction is initiated and the collector voltage of Q402 is lowered. Amplification of low frequency voltage gain is fixed by the ratio of R407 and R408. Gain is maintained to 18 MHz by the bandwidth enhancing components R406, C403, and L401. Resistors R402 and R403 provide bias for the amplifier.

The collector output of Q401 is D.C. coupled to the cathode of the C.R.T. through resistor R201. Raster cut-off is adjusted with the brightness control R114 which is connected to G1 of the C.R.T.

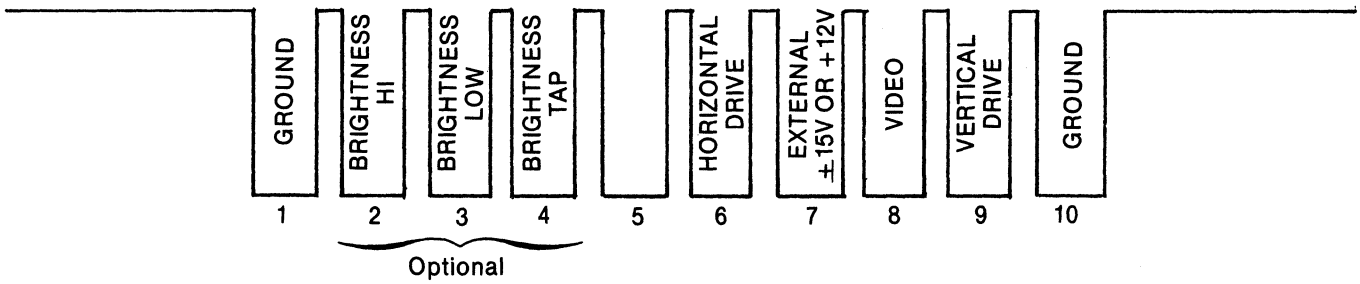

VERT.
DRIVE
VERT.
OSC.
VERT.
AMP.
VERT.
OUTPUT
VIDEO
INPUT
VIDEO
DRIVER
VIDEO
OUTPUT
YOKE
H.V.
HORIZ.
DRIVE
MONOSTABLE
MULTIV.
VARIABLE
TIME
ASTABLE
MULTIV.
HORIZ.
DRIVER
HORIZ.
OUTPUT
HORIZ.
SWEEP

ADJUSTMENT PROCEDURES FOR D12 VIDEO DISPLAY

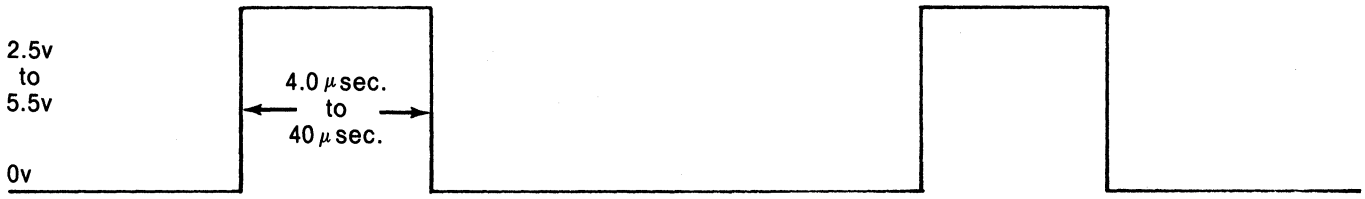
1. External power is applied to the monitor through an AC line cord or a 4 pin molex connector. The unit is wired for 120 VAC 50/60 Hz operation. (240 VAC 50/60 Hz optional)

2. INPUT SIGNALS: Input signals are connected to the display board through a 10 pin edge connector.

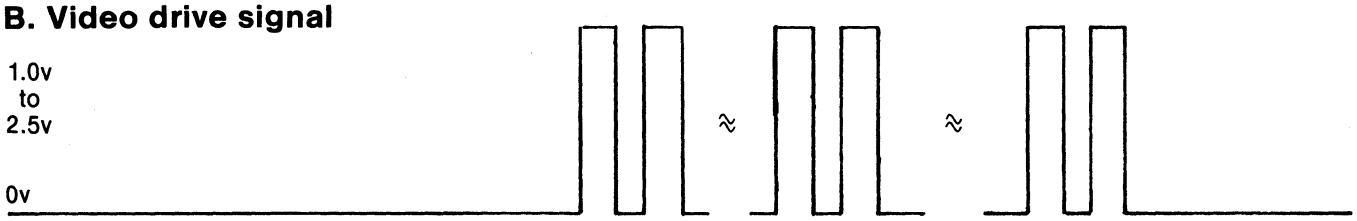
Component Side of Display Board



A. Horizontal drive signal — 15750Hz ± 500Hz, 18,600Hz ± 500Hz

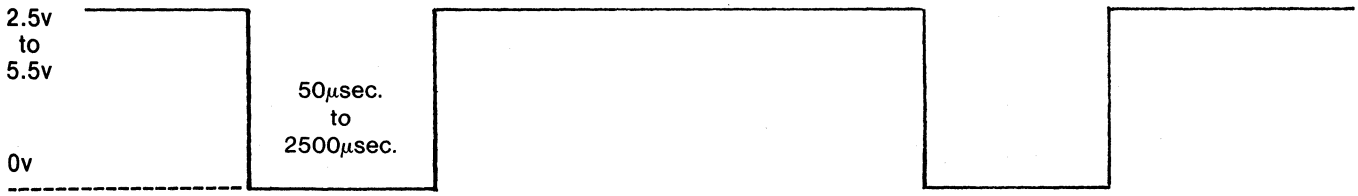


B. Video drive signal

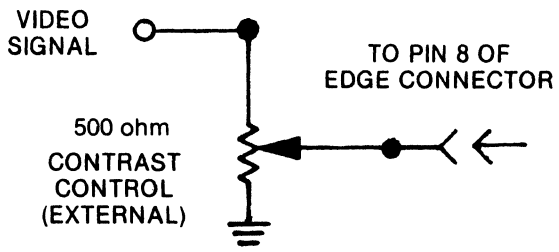


At a horizontal frequency of 15.7KHZ the video drive signal should start 11 microseconds ±5 μ sec. after the leading edge of horizontal sync, and 900 microseconds or greater after the leading edge of vertical sync.

C. Vertical drive signal - 47Hz to 63Hz



Should the video drive level exceed the 2.5 volts specified, an external contrast control must be provided. The video drive signal is connected to the top end of the 500Ω pot, the bottom end is grounded and the wiper arm connects to the video input of the edge connector as shown.



3. Once power is applied to the display and the input signals connected, adjust the brightness control until the edges of the raster are visible.

4. Depending on the requirements for height and width of the video presentation, the vertical size control and width coil should be adjusted accordingly.

5. The power supply board also has a control to adjust the regulated B+ of the monitor to +15V. Check for proper adjustment.

6. Adjust the phase control to center the video information within the raster. (The contrast control may have to be adjusted to obtain a display of the video information.)

7. Adjust brightness control for visual cutoff of the raster.

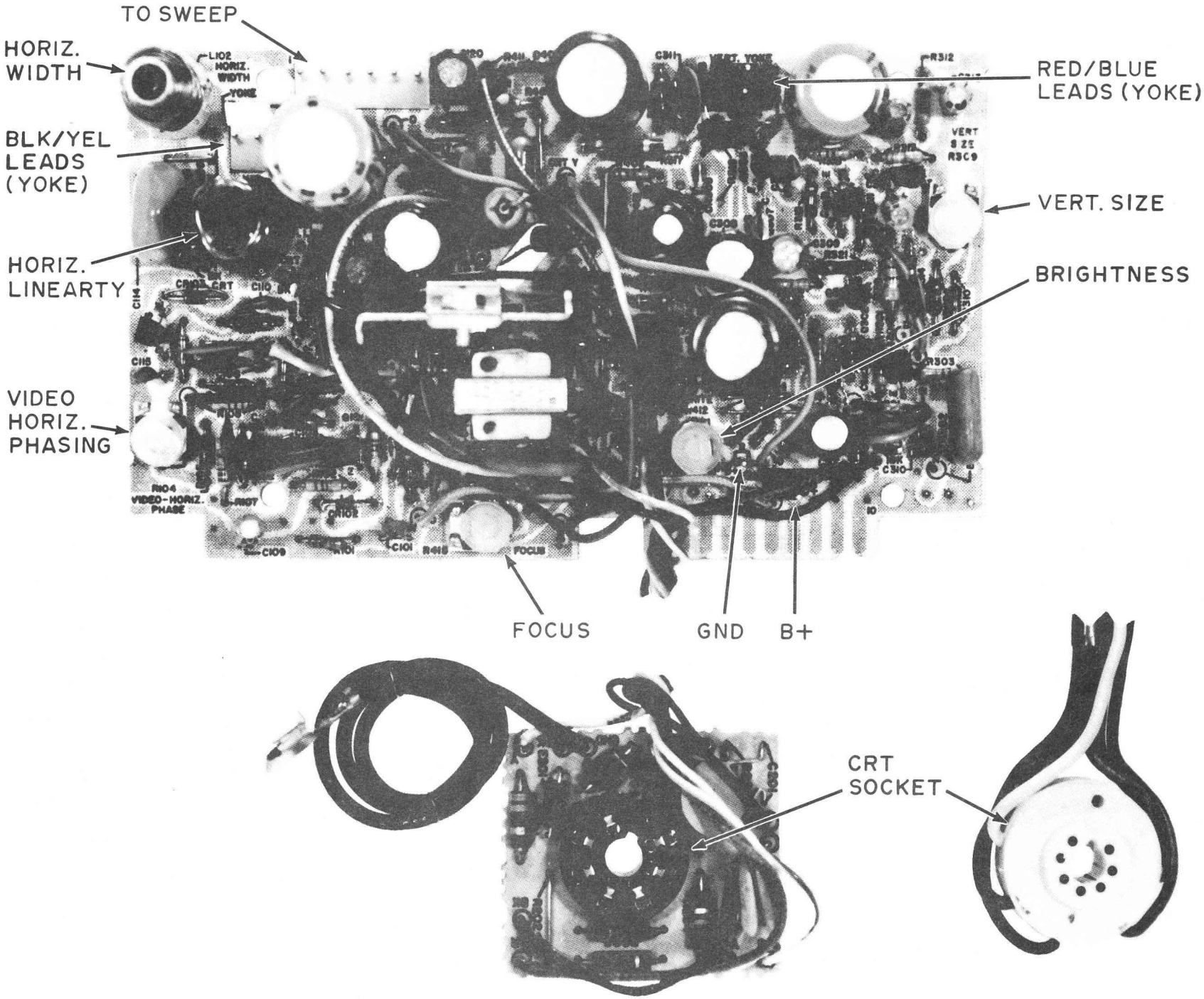
8. Adjust external contrast control for desired luminance.

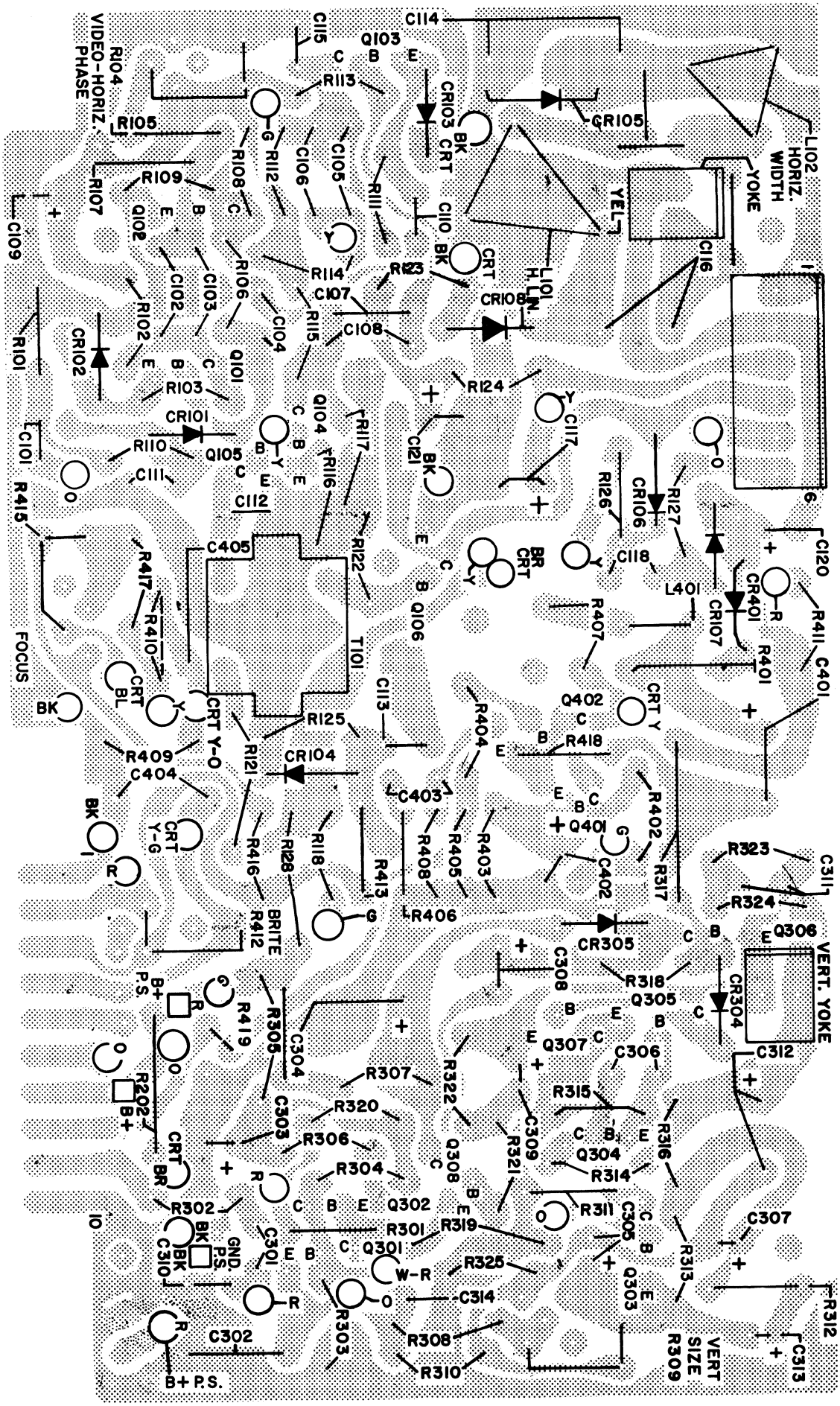
9. Adjust focus control for best possible overall focus.

IMPORTANT NOTE: DAG GROUNDING.

Each unit provides for grounding of the main P.C. Board and CRT socket board to the dag of the CRT through the dag grounding spring.

The ground wires are connected to the shell bond or T-band through a terminal lug. Upon installing the Video Display in a terminal, this grounding procedure should be followed to provide adequate high voltage filtering and arc protection. This especially pertains to mounting the video display as a kit version.


TO SWEEP
HORIZ. WIDTH
BLK/YEL LEADS (YOKE)
HORIZ. LINEARTY
VIDEO HORIZ. PHASING
RED/BLUE LEADS (YOKE)
VERT. SIZE
BRIGHTNESS
FOCUS
GND
B+
CRT SOCKET

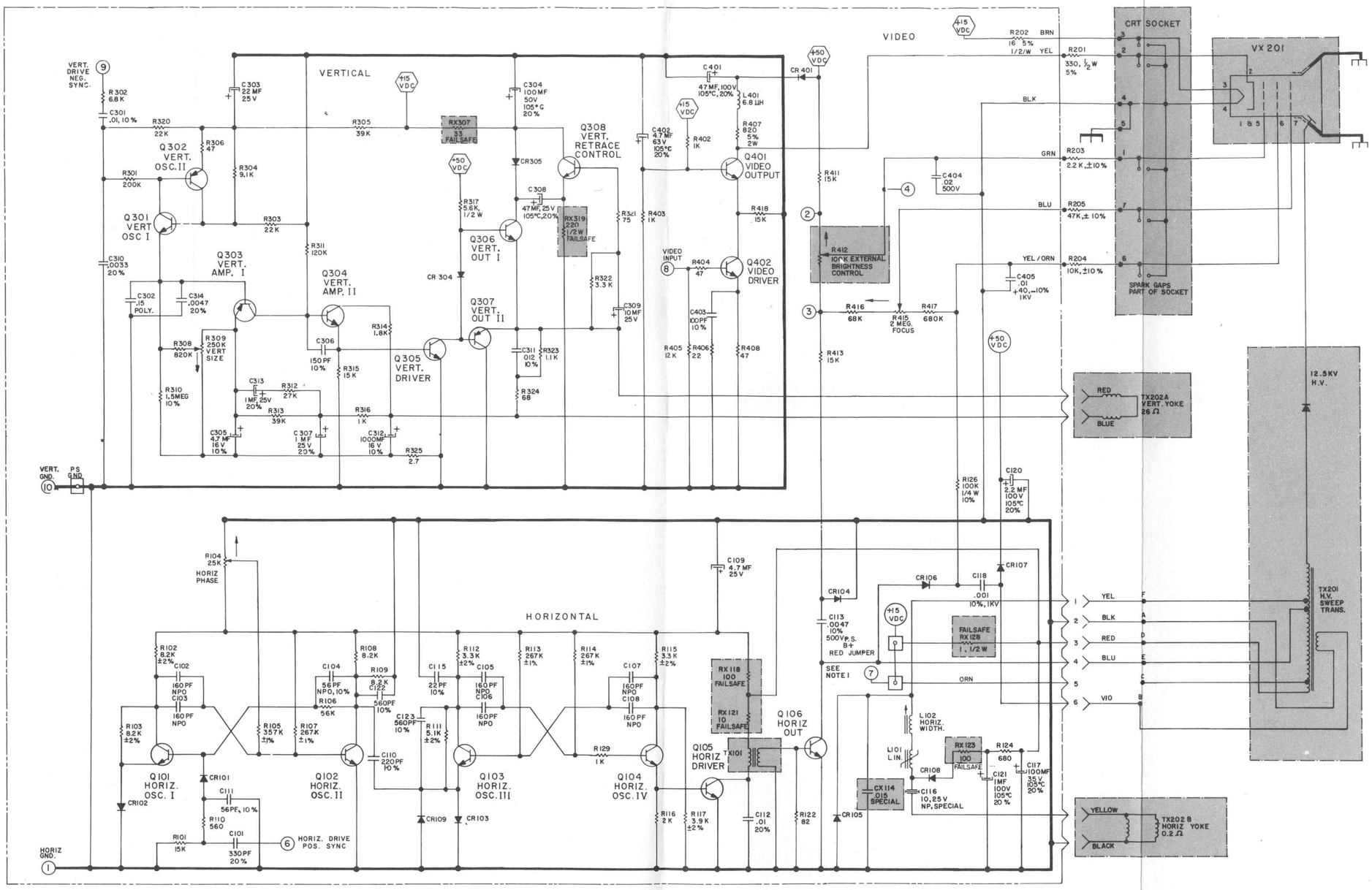

C114
C115
Q103
C
B
E
R113
CR103
BK
CRT
CR105
L102
HORIZ.
WIDTH
YOKE
YEL
C116
R104
VIDEO-HORIZ.
PHASE
R105
R109
R107
C109
R108
R112
C106
C105
R111
C110
BK
CRT
R123
L101
H. LIN.
CR108
R114
C107
C108
R115
C104
R106
C103
C102
R102
CR102
R101
Q102
Q101
R103
CR101
R110
Q105
C111
C112
C101
R415
FOCUS
BK
R124
C121
C117
R126
CR106
R127
C118
BR
CRT
Q106
R122
R117
R116
C405
R417
R410
T101
CRT
BL
CRT Y
CRT Y-O
R125
R121
CR104
C113
R404
C403
R409
C404
BK
CRT
Y-G
R416
R128
R118
R413
R408
R406
R405
R403
Q402
R418
Q401
R402
R317
C402
CRT Y
C120
R411
C401
L401
CR107
CR401
R407
R401
R323
C311
R324
Q306
VERT. YOKE
CR305
C308
R318
Q305
CR304
C312
R412
BRITE
B+
P.S.
R419
R305
C304
R307
R322
R315
C309
Q307
C306
R202
B+
R320
R303
C303
R306
R304
Q308
R321
R316
Q304
R314
R311
C305
R313
C307
CRT
BR
R302
Q302
R301
R319
Q301
W-R
R325
C314
R303
R308
R310
C302
B+ P.S.
GND.
P.S.
BK
C310
C301
R312
C313
VERT
SIZE
R309

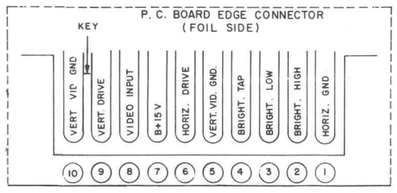
LEGEND

ITEM NO.	PART NO.	DESCRIPTION	
C101	22-7614-06A	330 PFD. CAPACITOR ±20% DISC.	50V
C102	22-7619-39A	160 PFD CAPACITOR ±5% DISC. NPO	50V
C103	22-7619-39A	160 PFD. CAPACITOR ±5% DISC. NPO	50V
C104	22-7622-28A	56 PFD CAPACITOR ±10% DISC NPO	50V
C105	22-7619-39A	160 PFD CAPACITOR ±5% DISC NPO	50V
C106	22-7619-39A	160 PFD CAPACITOR ±5% DISC NPO	50V
C107	22-7619-39A	160 PFD CAPACITOR ±5% DISC NPO	50V
C108	22-7619-39A	160 PFD CAPACITOR ±5% DISC NPO	50V
C109	22-7152-03	4.7 MFD CAPACITOR ELEC. +100%-10%	25V
C110	22-7613-04A	220 PFD CAPACITOR ±10% DISC	50V
C111	22-7622-28A	56 PFD CAPACITOR ±10% DISC	50V
C112	22-7614-24A	.01 MFD CAPACITOR ±20% DISC	50V
C113	22-7440	.0047 MFD CAPACITOR ±10% DISC	500V
CX114	22-7530-07	.015 MFD CAPACITOR SPECIAL..	
C115	22-7656-13A	22 PFD CAPACITOR ±10% DISC	50V
C116	22-7313	10 MFD CAPACITOR SPECIAL	
C117	22-7719-09	100 MFD CAPACITOR ±20% ELEC.	35V
C118	22-3748	.001 MFD CAPACITOR ±10% DISC	1KV
C120	22-7722-02	2.2 MFD CAPACITOR, ±20% ELEC.	100V
C121	22-7722-01	1 MFD CAPACITOR, ±20% ELEC.	100V
C122	22-7613-09	560 PFD CAPACITOR ±10% DISC.	50V
C123	22-7613-09	560 PFD CAPACITOR ±10% DISC.	50V
C301	22-7613-24A	.01 MFD CAPACITOR ±10% DISC	50V
C302	22-7548	.15 MFD CAPACITOR ±10% POLYESTER	50V
C303	22-7152-05	22 MFD CAPACITOR +100-10% ELEC.	25V
C304	22-7720-09	100 MFD CAPACITOR ±20% ELEC. 105°C	50V
C305	22-7579-03	4.7 MFD CAPACITOR ELEC. ± 10%	16V
C306	22-7613-02A	150 PFD CAPACITOR ±10% DISC	50V
C307	22-7389-02	1MFD CAPACITOR ±20% ELEC.	25V
C308	22-7718-08	47 MFD CAPACITOR ±20% ELEC.	25V
C309	22-7152-04	10 MFD CAPACITOR ±100-10% ELEC 105°C	25V
C310	22-7614-18A	.0033 MFD CAPACITOR ±20% DISC	50V
C311	22-7613-25A	.012 MFD CAPACITOR ±10% DISC	50V
C312	22-7579-04	1000 MFD CAPACITOR ±10% ELEC.	16V
C313	22-7389-02	1 MFD CAPACITOR ±20% ELEC.	25V
C314	22-7614-20A	.0047 MFD CAPACITOR ±20% DISC	50V
C401	22-7722-08	47 MFD CAPACITOR ±20% ELEC. 105°C	100V
C402	22-7721-04	4.7 MFD CAPACITOR ±20% ELEC. 105°C	63V
C403	22-7613A	100 PFD CAPACITOR ±10% DISC	50V
C404	22-7724	.02 MFD. CAPACITOR +80-20% DISC.	500V
C405	22-3512	.01 MFD CAPACITOR +40-10% DISC	1KV
R101	63-9922	15K OHM RESISTOR ±5% FILM	1/4W
R102	63-9919-94	8.2K OHM RESISTOR ±2% FILM	1/4W
R103	63-9919-94	8.2K OHM RESISTOR ±2% FILM	1/4W
R104	63-10651-11	CONTROL 25K OHM (HORIZ. PHASE)	
R105	63-10533-05	357K OHM RESISTOR ±1% METAL FILM	1/4W
R106	63-9922-14	56K OHM RESISTOR ±5% FILM	1/4W
R107	63-10533-04	267K OHM RESISTOR ±1% METAL FILM	1/4W
R108	63-9921-94	8.2K OHM RESISTOR ±5% FILM	1/4W
R109	63-9921-94	8.2K OHM RESISTOR ± 5% FILM	1/4W
R110	63-9921-66	560 OHM RESISTOR ±5% FILM	1/4W
R111	63+0351-89	5.1KOHM RESISTOR ±2% FILM	1/4W
R112	63-9919-84	3.3KOHM RESISTOR ± 2%FILM	1/4W
R113	63-10533-04	267K OHM RESISTOR ± 1% METAL FILM	1/4W
R114	63-10533-04	267K OHM RESISTOR ± 1% METAL FILM	1/4W
R115	63-9919-84	3.3K OHM RESISTOR ±2% FILM	1/4W
R116	63-9921-79	2K OHM RESISTOR ±5% FILM	1/4W
R117	63-9919-86	3.9K OHM RESISTOR ±2% FILM	1/4W
▮RX118	63-10559-48	100 OHM RESISTOR ± 5% FAILSAFE	1/4W
▮RX121	63-10559-24	10 OHM RESISTOR ± 5% FAILSAFE	1/4W
R122	63-9921-46	82 OHM RESISTOR ± 5% FILM	1/4W
▮RX123	63-10559-48	100 OHM RESISTOR ± 5% FAILSAFE	1/4W
▮RX124	63-10559-68	680 OHM RESISTOR ± 5% FAILSAFE	1/4 W
			1/4W
R126	63-10184-20	100K OHM RESISTOR ±10% CARBON COMP	1/4W
▮RX128	63-10565	1 OHM RESISTOR ± 5% FAILSAFE	1/2W
R129	63-8797	1K OHM RESISTOR ±5% FILM	1/4W
R201		330 OHM RESISTOR ±5% CARBON COMP	1/2W
R202		16 OHM RESISTOR ± 5% CARBON COMP	1/2W
R203	REFERENCE ONLY	2.2KOHM RESISTOR ±10% CARBON COMP	1/2W
R204		10 K OHM RESISTOR ±10% CARBON COMP	1/2W

ITEM NO.	PART NO.	DESCRIPTION	
R205		47K OHM RESISTOR ±10% CARBON COMP	1/2W
R301	63-9922-27	200 K OHM RESISTOR ±5% FILM	1/4W
R302	63-9921-92	6.8 K OHM RESISTOR ± 5% FILM	1/4W
R303	63-9922-04	22K OHM RESISTOR ± 5% FILM	1/4W
R304	63-9921-95	9.1 K OHM RESISTOR ±5% FILM	1/4W
R305	63-9922-10	39K OHM RESISTOR ± 5% FILM	1/4W
R306	63-9921-40	47 OHM RESISTOR ± 5% FILM	1/4W
▮RX307	63-10559-36	33 OHM RESISTOR ± 5% FAILSAFE	1/4W
R308	63-9922-42	820K OHM RESISTOR ± 5% FILM	1/4W
R309	63-10651-13	CONTROL 250K OHM VERT. SIZE	
R310	63-9924-48	1.5 MEG OHM RESISTOR ± 10% FILM	1/4W
R311	63-9922-22	120 K OHM RESISTOR ± 5% FILM	1/4W
R312	63-9922-06	27K OHM RESISTOR ± 5% FILM	1/4W
R313	63-9922-10	39K OHM RESISTOR ± 5% FILM	1/4W
R314	63-9921-78	1.8 K OHM RESISTOR ± 5% FILM	1/4W
R315	63-9922	15 K OHM RESISTOR ± 5% FILM	1/4W
R316	63-9921-72	1K OHM RESISTOR ±5% FILM	1/4W
R317	63-7816	5.6 K OHM RESISTOR ± 5% CARBON COMP	1/2W
R318			
▮RX319	63-10565-56	220 OHM RESISTOR ± 5% FAILSAFE	1/2W
R320	63-9922-04	22K OHM RESISTOR ± 5% FILM	1/4W
R321	63-9921-45	75 OHM RESISTOR± 5% FILM	1/4W
R322	63-9921-84	3.3K OHM RESISTOR ± 5% FILM	1/4W
R323	63-9921-73	1.1K OHM RESISTOR ±5% FILM	1/4W
R324	63-9921-44	68 OHM RESISTOR ±5%FILM	1/4W
R325	63-9921-10	2.7 OHM RESISTOR ±5% FILM	1/4W
R402	63-9921-72	1K OHM RESISTOR ±5% FILM	1/4W
R403	63-9921-72	1K OHM RESISTOR ± 5% FILM	1/4W
R404	63-9921-40	47 OHM RESISTOR± 5% FILM	1/4 W
R405	63-8821	12K OHM RESISTOR ± 5% FILM	1/4W
R406	63-9921-32	22 OHM RESISTOR ± 5% FILM	1/4W
R407	63=10371-70	820 OHM RESISTOR ± 5% FILM	2W
R408	63-9921-40	47 OHM RESISTOR ± 5% FILM	1/4W
R411	63-9922-	15K OHM RESISTOR ±5% FILM	1/4W
R412			
R413	63-9922-04	15K OHM RESISTOR ±5% FILM	1/4W
R415	63-10812-01	CONTROL 2 MEG OHM FOCUS	
R416	63-9922-16	68K OHM RESISTOR ±5% FILM	1/4W
R417	63-9922-40	680K OHM RESISTOR ±5% FILM	1/4W
R418	63-9922	15K OHM RESISTOR ±5% FILM	1/4W
L101	20-3906	COIL,RCF LINEARITY	
L102	20-3882	COIL, RCF TUNABLE WIDTH	
L401	20-3887-10C	COIL, RCF 6.8 uh	
▮TX101	95-3138-03	TRANSFORMER HORIZ DRIVER	
▮TX201	95-3395-01	H.V. SWEEP TRANSFORMER	
▮TX202	95-3397-02	DEFLECTION YOKE	
CR101	103-142-01	DIODE	
CR102	103-142-01	DIODE	
CR103	103-142-01	DIODE	
CR104	103-295-03 A	DIODE	
CR105	103-284	DIODE	
CR106	212-76 -02	DIODE	
CR107	103-298-05A	DIODE	
CR108	212-76	DIODE	
CR109	103-142-01	DIODE	
CR304	103-142-01	DIODE	
CR305	212-76	DIODE	
CR401	212-76	DIODE	
Q101	121-975	TRANSISTOR	HORIZ. OSC.I
Q102	121-975	TRANSISTOR	HORIZ. OSC II
Q103	121-975	TRANSISTOR	HORIZ. OSC.III
Q104	121-975	TRANSISTOR	HORIZ. OSC.IV
Q105	121-819	TRANSISTOR	HORIZ DRIVER
Q106	121-1039	TRANSISTOR	HORIZ. OUTPUT
Q301	121-975	TRANSISTOR	VERT. OSC. I
Q302	121-699	TRANSISTOR	VERT. OSC. II
Q303	121-699	TRANSISTOR	VERT. AMP. I
Q304	121-975	TRANSISTOR	VERT. AMP. II
Q305	121-972	TRANSISTOR	VERT. DRIVER
Q306	121-819	TRANSISTOR	VERT. OUTPUT I
Q307	121-973	TRANSISTOR	VERT. OUTPUT II
Q308	121-819	TRANSISTOR	VERT. RETRACE
Q401	121-1058	TRANSISTOR 121-1034 ALT.	VIDEO OUTPUT
Q402	121-895	TRANSISTOR	VIDEO DRIVER
VX201 OR	100-684 100-684-02	12" CRT 12" CRT	

D12 VIDEO DISPLAY 15.7KHz





= DC VOLTAGE SOURCE

= DC VOLTAGE APPLIED

NOTE 1. CUSTOMER SUPPLIED EXTERNAL DC SOURCE ON PIN 7 EDGE CONNECTOR

IMPORTANT SAFETY NOTICE

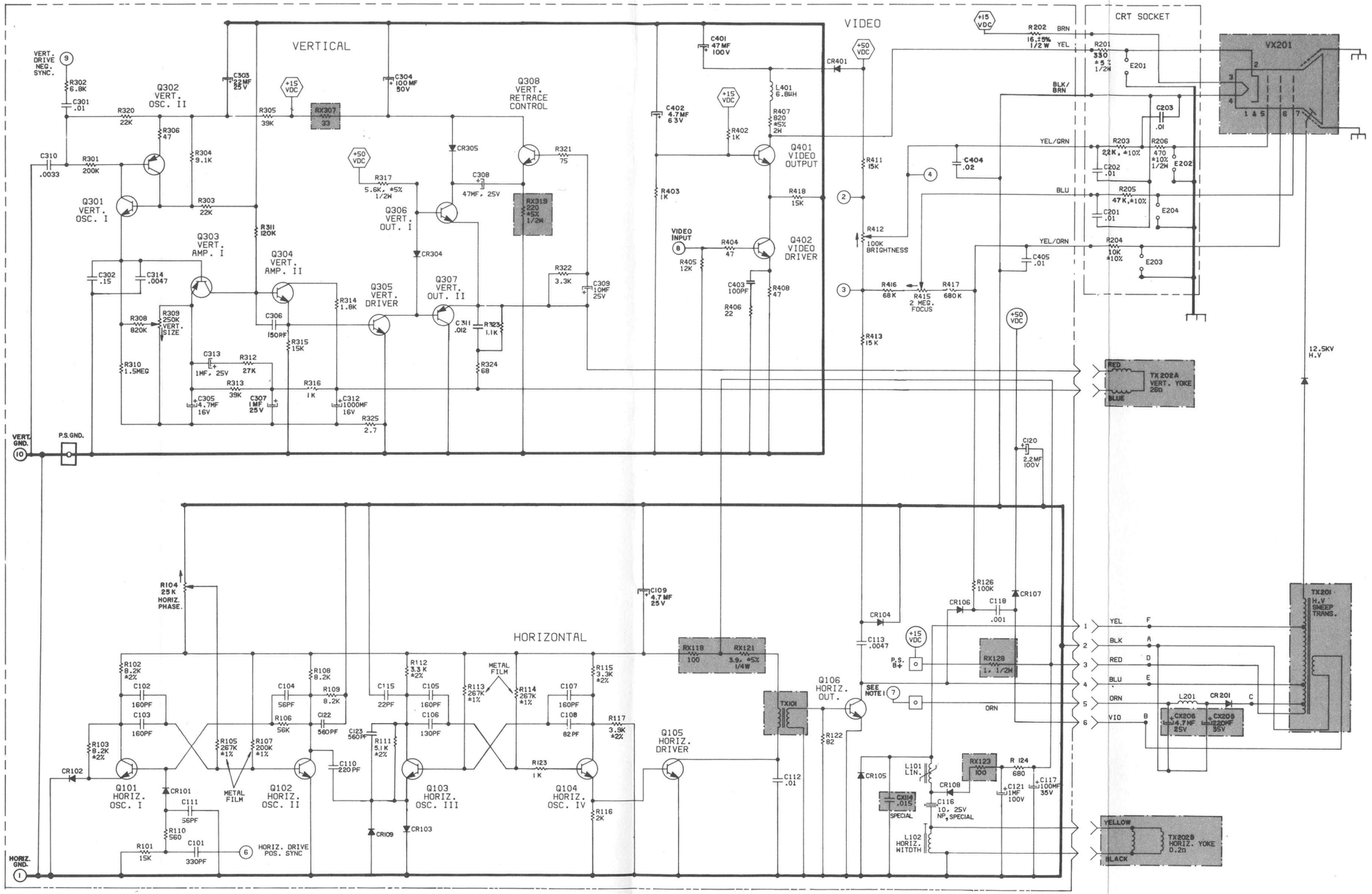
When servicing this chassis, under no circumstances should the original design be modified or altered without permission from the Zenith Radio Corporation. All components should be replaced only with types identical to those in the original circuit. Special components are used to prevent shock and fire hazard. These critical components are shaded on the schematic and parts list for easy identification.

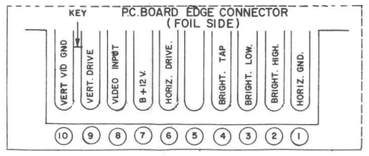
This circuit diagram may occasionally differ from the actual circuit used. This way, implementation of the latest safety and performance improvement changes into the set is not delayed until the new service literature is printed.

IMPORTANT SAFETY NOTICE

FOR X-RADIATION, FIRE OR SHOCK HAZARD PREVENTION, CERTAIN SPECIAL OR REDUNDANT PARTS ARE USED. USE ONLY EXACT REPLACEMENTS. DO NOT ALTER THE CIRCUIT OR DEFEAT THE FUSES. FAILURE TO COMPLY MAY BE UNLAWFUL.

D12 VIDEO DISPLAY 18.6KHz





= DC VOLTAGE SOURCE

= DC VOLTAGE APPLIED

NOTE L CUSTOMER SUPPLID EXTERNAL DC SOURCE ON PIN 7 EDGE CONNECTOR

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IMPORTANT SAFETY NOTICE

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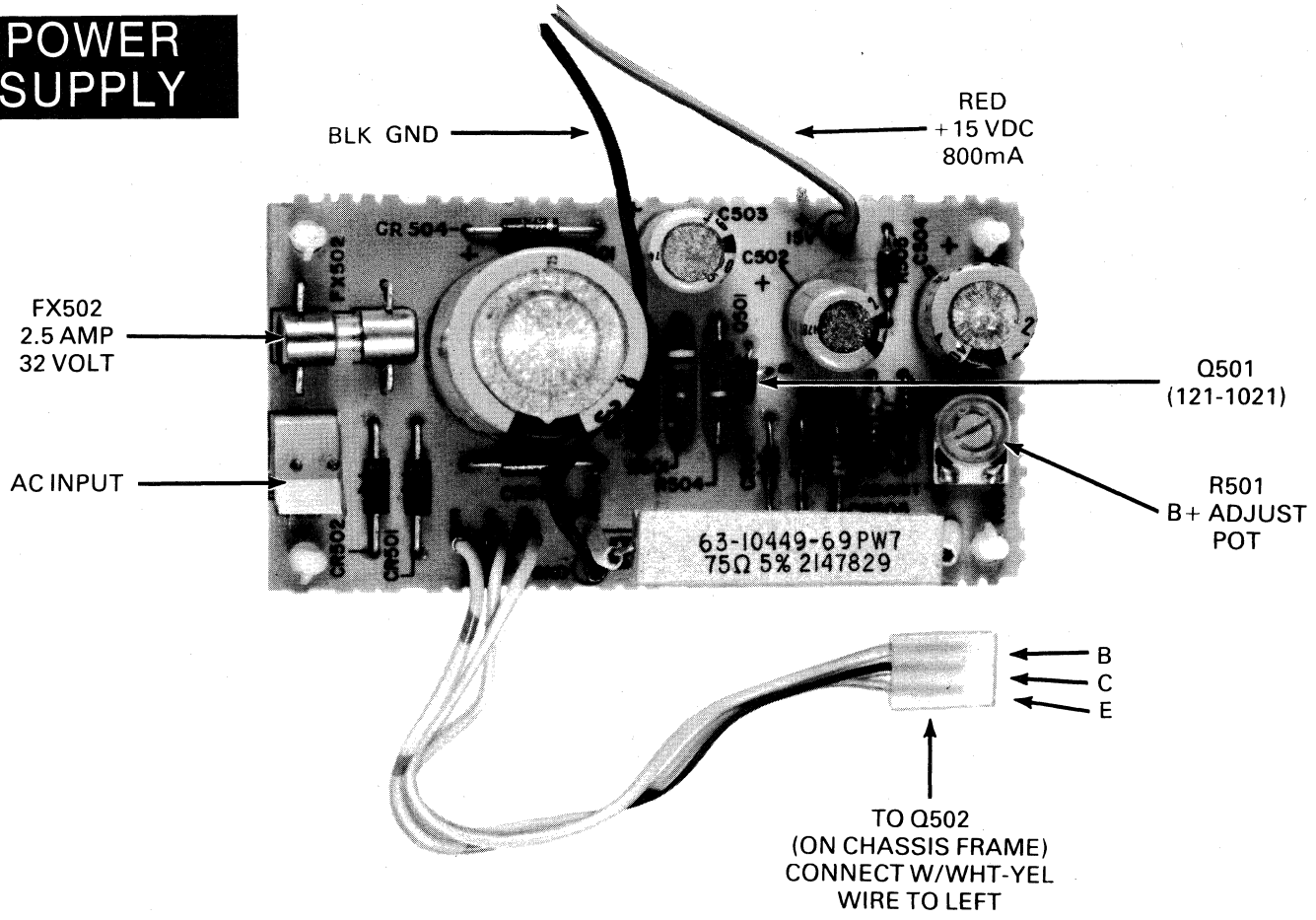
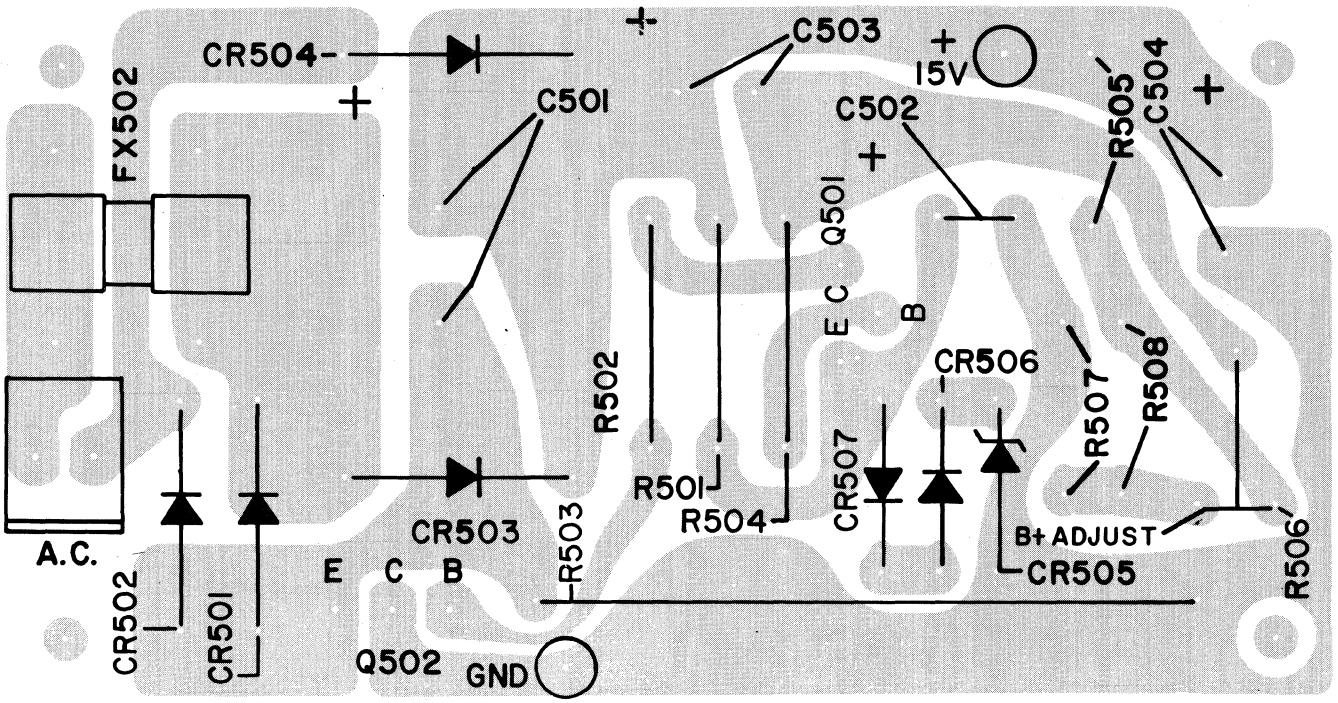
LEGEND

ITEM NO.	PART NO.	DESCRIPTION	
C101	22-7614-06A	330 PFD. CAPACITOR ±20% DISC.	50V
C102	22-7619-39A	180 PFD. CAPACITOR ±5% DISC. NPO	50V
C103	22-7619-39A	180 PFD. CAPACITOR ±5% DISC NPO	50V
C104	22-7622-28A	56 PFD CAPACITOR ±10% DISC	50V
C105	22-7619-39A	180 PFD CAPACITOR ±5% DISC NPO	50V
C106	22-7619-37A	130 PFD CAPACITOR ±5% DISC NPO	50V
C107	22-7619-39A	180 PFD CAPACITOR ±5% DISC NPO	50V
C108	22-7619-32A	82 PFD CAPACITOR ±5% DISC NPO	50V
C109	22-7152-03	4.7 MFD CAPACITOR +100%-10% ELEC.	25V
C110	22-7613-04A	220 PFD CAPACITOR ±10% DISC	50V
C111	22-7622-28A	56 PFD CAPACITOR ±10% DISC	50V
C112	22-7614-24A	.01 MFD CAPACITOR ± 20% DISC	50V
C113	22-7440	.0047 MFD CAPACITOR ±10% DISC	500V
C114	22-7530-07	.015 MFD CAPACITOR SPECIAL	
C115	22-7656-13A	22 PFD CAPACITOR ±10% DISC	50V
C116	22-7313	10 MFD CAPACITOR SPECIAL	
C117	22-7719-09	100 MFD CAPACITOR ±20% ELEC. 105°C	35V
C118	22-3748	.001 MFD CAPACITOR ±10% DISC	1KV
C120	22-7722-02	2.2 MFD CAPACITOR ±20% ELEC. 105°C	100V
C121	22-7722-01	1 MFD CAPACITOR ±20% ELEC. 105°C	100V
C122	22-7613-09	560 PFD CAPACITOR ±10% DISC	50V
C123	22-7613-09	560 PFD CAPACITOR ±10% DISC	50V
C201	22-4905-01	.01 MFD CAPACITOR +80-20% DISC.	500V
C202	22-4905-01	.01 MFD CAPACITOR +80-20% DISC.	500V
C203	22-4905-01	.01 MFD CAPACITOR +80-20%DISC.	500V
‡CX205	22-7144-09	220 MFD CAPACITOR +100%-10% ELEC.	35V
‡CX206	22-7142-03	4.7 MFD CAPACITOR +100%-10% ELEC.	25V
C301	22-7613-24A	.01 MFD CAPACITOR ±10% DISC	50V
C302	22-7548	.15 MFD.CAPACITOR ±10% POLYESTER	50V
C303	22-7152-05	22 MFD CAPACITOR +100-10% ELEC.	25V
C304	22-7720-09	100 MFD CAPACITOR ±20% ELEC. 105°C	50V
C305	22-7579-03	4.7 MFD CAPACITOR ±10% ELEC.	16V
C306	22-7613-02A	150 PFD CAPACITOR ±10% DISC	50V
C307	22-7389-02	1 MFD CAPACITOR ±20% ELEC.	25V
C308	22-7718-08	47 MFD CAPACITOR ±20% ELEC. 105°C	25V
C309	22-7152-04	10 MFD CAPACITOR +100-10% ELEC.	25V
C310	22-7614-19A	.0033 MFD CAPACITOR ±20% DISC	50V
C311	22-7613-23A	.012 MFD CAPACITOR ±10% DISC.	50V
C312	22-7579-04	1000 MFD CAPACITOR ±10% ELEC.	16V
C313	22-7389-02	1 MFD CAPACITOR ±20% ELEC.	25V
C314	22-7614-20A	.0047 MFD CAPACITOR ±20% DISC	50V
C401	22-7722-08	47 MFD CAPACITOR ±20% ELEC. 105°C	100V
C402	22-7721-04	4.7 MFD CAPACITOR ±20% ELEC. 105°C	63V
C403	22-7613A	100 PFD CAPACITOR ±10% DISC	50V
C404	22-7724	.02 MFD CAPACITOR +80%-20% DISC.	500V
C405	22-3512	.01 MFD CAPACITOR +40-10% DISC	1KV
R101	63-9922	15K OHM RESISTOR ± 5% FILM	1/4W
R102	63-9919-94	8.2K OHM RESISTOR ±2% FILM	1/4W
R103	63-9919-94	8.2K OHM RESISTOR ± 2% FILM	1/4W
R104	63-10651-11	CONTROL 25K OHM (HORIZ. PHASE)	
R105	63-10533-04	267K OHM RESISTOR ± 1% (METAL FILM)	1/4W
R106	63-9922-14	56K OHM RESISTOR ± 5% FILM	1/4W
R107	63-10533-11	200K OHM RESISTOR ± 1% METAL FILM	1/4W
R108	63-9921-94	8.2K OHM RESISTOR ±5% FILM	1/4W
R109	63-9921-94	8.2K OHM REISITOR ±5% FILM	1/4W
R110	63-9921-66	560 OHM RESISTOR ± 5%	1/4W
R111	63-10351-89	5.1KOHM RESISTOR ± 2% FILM	1/4W
R112	63-9919-84	3.3KK OHM RESISTOR ±2% FILM	1/4W
R113	63-10533-04	267K OHM RESISTOR 1% METAL FILM	1/4W
R114	63-10533-04	267K OHM RESISTOR ± 1% METAL FILM	1/4W
R115	63-9919-84	3.3K OHM RESISTOR ±2%	1/4W
R116	63-9921-79	2K OHM RESISTOR 5% FILM	1/4W
R117	63-9919-86	3.9K OHM RESISTOR ± 2% FILM	1/4W
‡RX118	63-10559-48	100 OHM RESISTOR ±5% FAILSAFE	1/4W
‡RX121	63-10559-14	3.9 OHM RESISTOR ± 5% FAILSAFE	1/4W
R122	63-9921-46	82 OHM RESISTOR ± 5%	1/4W
‡RX123	63-10559-48	100 OHM RESISTOR ± 5% FAILSAFE	1/4W
R 124	63-9321-68	680 OHM RESISTOR ±5% FILM	1/4W
R126	63-10614-20	100K OHM RESISTOR ± 5% CARBON COMP.	1/4W
‡RX128	63-10565-	1 OHM RESISTOR ±5% FAILSAFE	1/2W
R201	63-7763	330 OHM RESISTOR ±5% CARBON COMP.	1/2W
R202	63-7710	16 OHM RESISTOR ±5% CARBON COMP.	1/2W
R203	63-7799	2.2KOHM RESISTOR ±10% CARBON COMP.	1/2W
R204	63-7827	10K OHM RESISTOR ±10% CARBON COMP.	1/2W
R205	63-7855	47K OHM RESISTOR ±10% CARBON COMP.	1/2W
R206	63-7771	470 OHM RESISTOR ±10% CARBON COMP.	1/2W
R301	63-9922-27	200 K OHM RESISTOR ±5% FILM	1/4W
R302	63-9921-92	6.8 K OHM RESISTOR ±5% FILM	1/4W
R303	63-9922-04	22K OHM RESISTOR ±5% FILM	1/4W

ITEM NO.	PART NO.	DESCRIPTION	
R304	63-9921-95	9.1 K OHM RESISTOR ±5% FILM	1/4W
R305	63-9922-10	39K OHM RESISTOR ± 5% FILM	1/4W
R306	63-9921-40	47 OHM RESISTOR ±5% FILM	1/4W
‡RX307	63-10559-36	33 OHM RESISTOR ± 5% FAILSAFE	1/4W
R308	63-9922-42	820K OHM RESISTOR ± 5% FILM	1/4W
R309	63-10651-13	CONTROL 250K OHM VERT. SIZE	1/4W
R310	63-9924-48	1.5 MEG OHM RESISTOR ±10% FILM	1/4W
R311	63-9922-22	120K OHM RESISTOR ±5% FILM	1/4W
R312	63-9922-06	27K OHM RESISTOR ± 5% FILM	1/4W
R313	63-9922-10	39K OHM RESISTOR ± 5% FILM	1/4W
R314	63-9921-78	1.8K OHM RESISTOR ± 5% FILM	1/4W
R315	63-9922	15K OHM RESISTOR ± 5% FILM	1/4W
R316	63-9921-72	.1000 OHM RESISTOR ±5% FILM	1/4W
R317	63-7816	5.6K OHM RESISTOR ± 5% CARBON COMP.	1/2W
‡RX319	63-10565-56	220 OHM RESISTOR ± 5% FAILSAFE	1/2W
R320	63-9921-04	22K OHM RESISTOR ± 5% FILM	1/4W
R321	63-9921-45	75 OHM RESISTOR ± 5% FILM	1/4W
R322	63-9921-84	3.3K OHM RESISTOR ± 5% FILM	1/4W
R323	63-9921-73	1100 OHM RESISTOR ±5% FILM	1/4W
R324	63-9921-44	68 OHM RESISTOR ±5% FILM	1/4W
R325	63-9921-10	2.7 OHM RESISTOR ± 5% FILM	1/4W
R402	63-9921-72	1K OHM RESISTOR ± 5% FILM	1/4W
R403	63-9921-72	1K OHM RESISTOR ± 5% FILM	1/4W
R404	63-9921-40	47 OHM RESISTOR ± 5% FILM	1/4W
R405	63-8821	12K OHM RESISTOR ± 5% FILM	1/4W
R406	63-9921-32	22 OHM RESISTOR ± 5% FILM	1/4W
R407	63-10371-70	820 OHM RESISTOR ± 5% FILM	2W
R408	63-9921-40	47 OHM RESISTOR ±5% FILM	1/4W
R411	63-9922	15K OHM RESISTOR ±5% FILM	1/4W
R412	63-10651-12	CONTROL 100 K OHM BRIGHTNESS	
R413	63-9922	15K OHM RESISTOR ±5% FILM	1/4W
R415	63-10812-01	CONTROL 2 MEG OHM FOCUS	
R416	63-9922-16	68K OHM RESISTOR ±5% FILM	1/4W
R417	63-9922-40	680K OHM RESISTOR ±5% FILM	1/4W
R418	63-9922	15K OHM RESISTOR ±5% FILM	1/4W
CR101	103-142-01	DIODE	
CR102	103-142-01	DIODE	
CR103	103-142-01	DIODE	
CR104	103-295-03A	DIODE	
CR105	103-284	DIODE	
CR106	212-76-02	DIODE	
CR107	103-298-05A	DIODE	
CR108	212-76-02	DIODE	
CR109	103-142-01	DIODE	
CR201A	103-280-04	DIODE	
CR304	103-142-01	DIODE	
CR305	212-76-02	DIODE	
CR401	212-76-02	DIODE	
L101	20-3906-02	COIL, RCF LINEARITY	
L102	20-3905	COIL, RCF TUNABLE WIDTH	
L201	20-3824	COIL, HORIZ. FILTER CHOKE	
L401	20-3887-10C	COIL, RCF 6.8 Uh	
TX101	95-3136-03	TRANSFORMER HORIZ. DRIVER	
TX201	95-3395-01	H.V. SWEEP TRANSFORMER	
TX202	95-3397-02	DEFLECTION YOKE	
Q101	121-975	TRANSISTOR	HORIZ OSC. I
Q102	121-975	TRANSISTOR	HORIZ. OSC. II
Q103	121-975	TRANSISTOR	HORIZ OSC. III
Q104	121-975	TRANSISTOR	HORIZ. OSC. IV
Q105	121-819	TRANSISTOR	HORIZ. DRIVER
Q106	121-1039	TRANSISTOR	HORIZ. OUTPUT
Q301	121-975	TRANSISTOR	VERT. OSC. I
Q302	121-699	TRANSISTOR	VERT. OSC. II
Q303	121-699	TRANSISTOR	VERT. AMP. I
Q304	121-975	TRANSISTOR	VERT. AMP II
Q305	121-972	TRANSISTOR	VERT. DRIVER
Q306	121-819	TRANSISTOR	VERT. OUTPUT I
Q307	121-973	TRANSISTOR	VERT. OUTPUT II
Q308	121-819	TRANSISTOR	VERT. RETRACE CONTROL
Q401	121-1058	TRANSISTOR	VIDEO OUTPUT 121-1034 ALT.
Q402	121-895	TRANSISTOR	VIDEO DRIVER
E201	52-2240-01	SPARK GAP (PART OF CRT SOCKET ASSY)	
E202	52-2240-01	SPARK GAP (PART OF CRT SOCKET ASSY)	
E203	52-2240-01	SPARK GAP (PART OF CRT SOCKET ASSY)	
E204	52-2240-01	SPARK GAP (PART OF CRT SOCKET ASSY)	
VX201	100-684	12" CRT	
	OR		
	100-684-02	12" CRT	

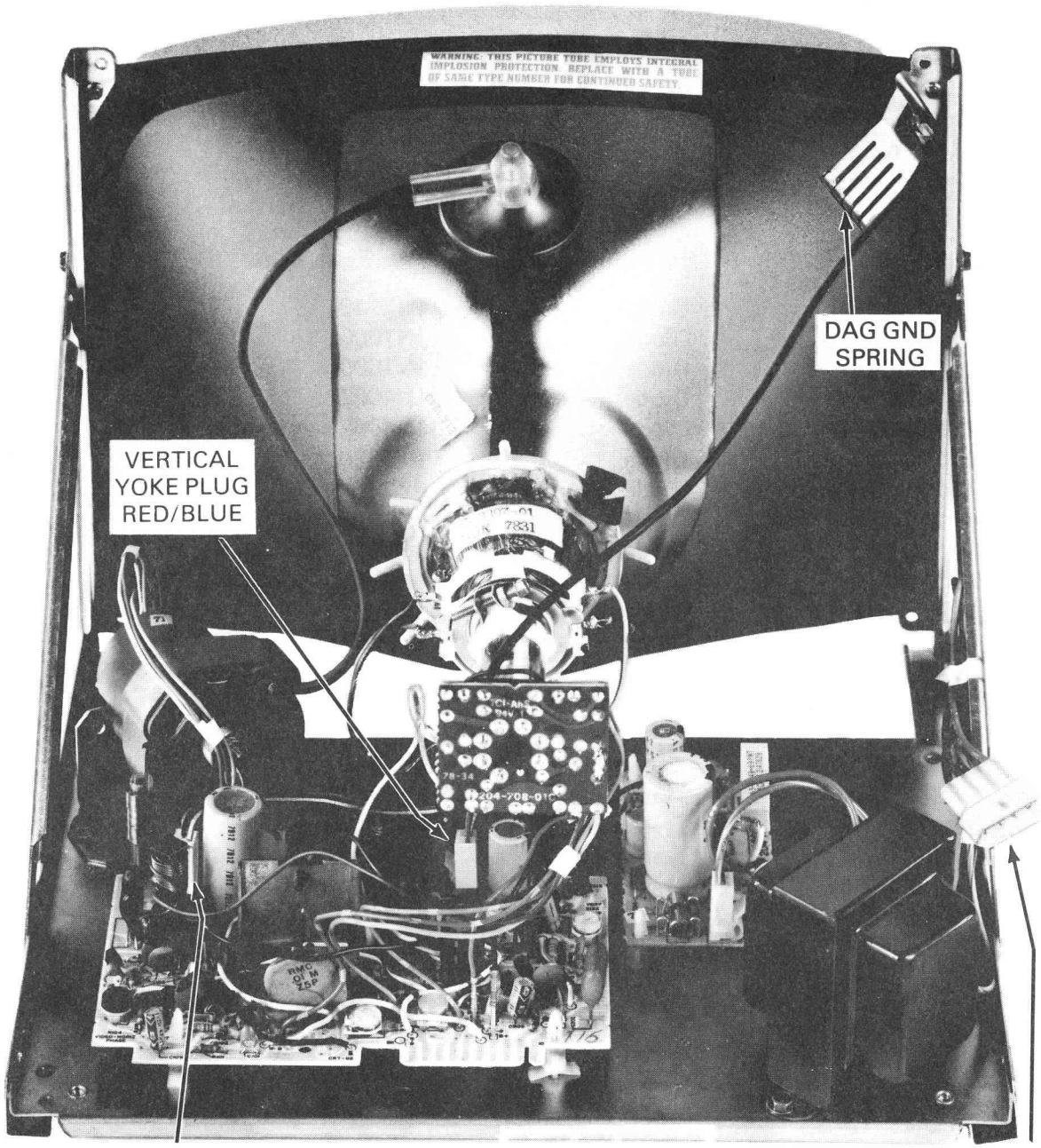
POWER SUPPLY

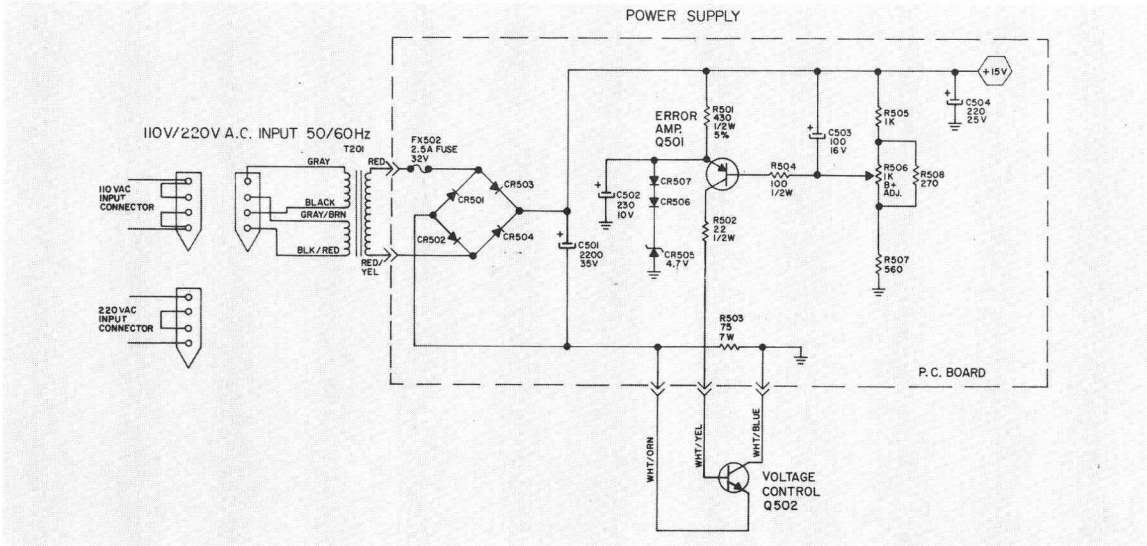




LEGEND

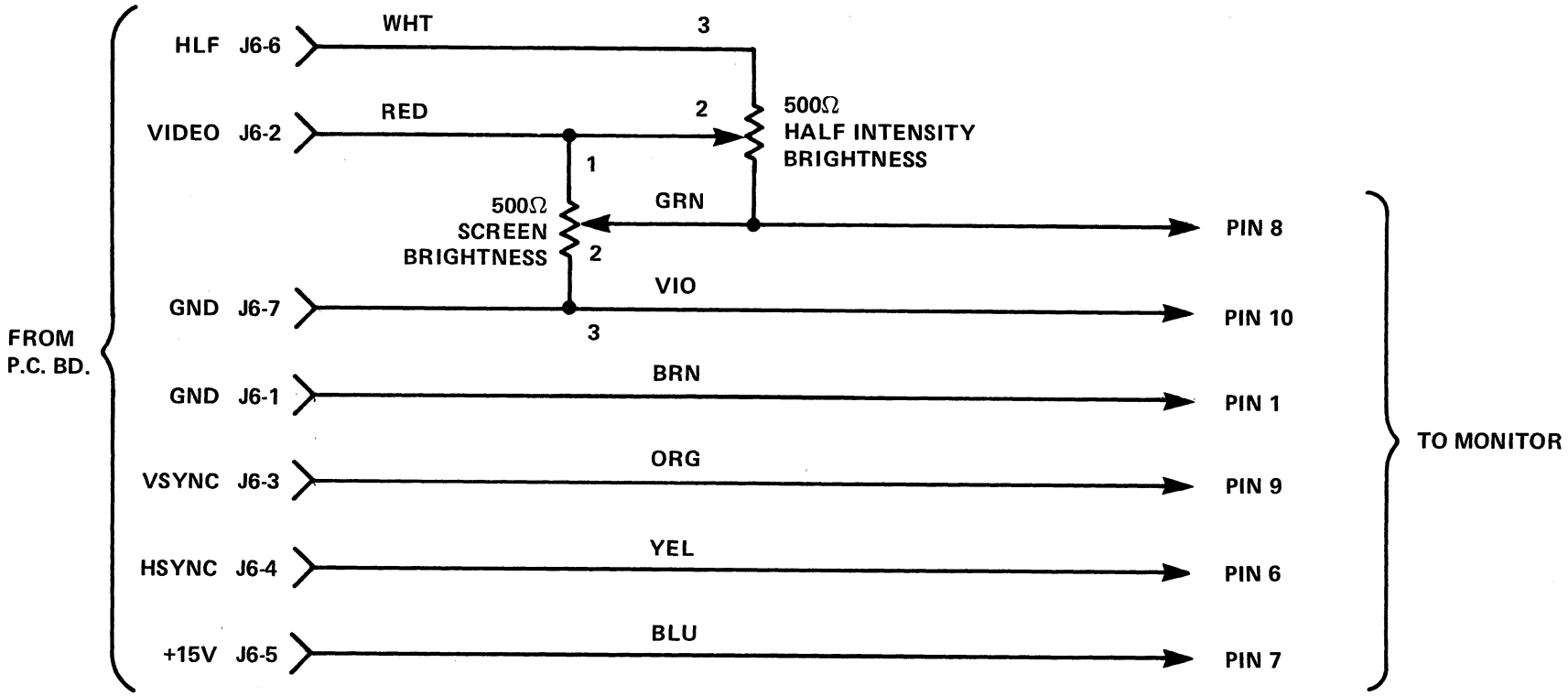
REF NO	PART NO	DESCRIPTION
C501	22-7154-13	2200 MFD CAP ELECT « 100% –10% 35V
C502	22-7152-08	100 μF CAP ELECT « 100% – 10% 25V
C503	22-7717-09	100 μF CAP ELECT 20% 16V
C504	22-7154-08	100μF CAP ELECT ±100% –10% 35V
R501	63-7769	430Ω RESISTOR 5% CARBON 1/2W
R502	63-7715	22Ω RESISTOR 10% CARB COMP 1/2W
R503	63-10449-69	75Ω RESISTOR WW 5% 7W
R504	63-7743	100Ω RESISTOR 10% CARB COMP 1/2W
RX505	63-9921-72	1K Ω RESISTOR 5% FILM 1/4W
RX506	63-10651-01	CONTROL 1K Ω (B ± ADJ)
RX507	63-9921-66	560 Ω RESISTOR 5% FILM 1/4W
RX508	63-9921-58	270 Ω RESISTOR 5% FILM 1/4W
T201	95-3396	TRANSFORMER, POWER 110/220V
CR501	212-76	DIODE
CR502	212-76	DIODE
CR503	212-76	DIODE
CR504	2I2-76	DIODE
CR505	103-279-09A	DIODE ZENER 4.7V
CR506	103-142-01	DIODE
CR507	103-142-01	DIODE
Q501	121-1021	TRANSISTOR ERROR AMP
QX502	121-9992-01	TRANSISTOR VOLTAGE CONTROL
FX502	136-120-06	FUSE 2.5 AMP 32V


WARNING: THIS PICTURE TUBE EMPLOYS INTEGRAL IMPLOSION PROTECTION. REPLACE WITH A TUBE OF SAME TYPE NUMBER FOR CONTINUED SAFETY.
DAG GND SPRING
VERTICAL YOKE PLUG RED/BLUE
HORIZONTAL YOKE PLUG BLK/YEL
AC INPUT


POWER SUPPLY
110V/220V A.C. INPUT 50/60Hz
110 VAC INPUT CONNECTOR
220 VAC INPUT CONNECTOR
T201
GRAY
BLACK
GRAY/BRN
BLK/RED
RED
RED/YEL
FX502 2.5A FUSE 32V
CR501
CR502
CR503
CR504
C501 2200 35V
C502 230 10V
ERROR AMP. Q501
CR507
CR506
CR505 4.7V
R501 430 1/2W 5%
R502 22 1/2W
R503 75 7W
R504 100 1/2W
C503 100 16V
R505 1K
R506 1K B+ ADJ.
R508 270
R507 560
+15V
C504 220 25V
P.C. BOARD
WHT/ORN
WHT/YEL
WHT/BLUE
VOLTAGE CONTROL Q502

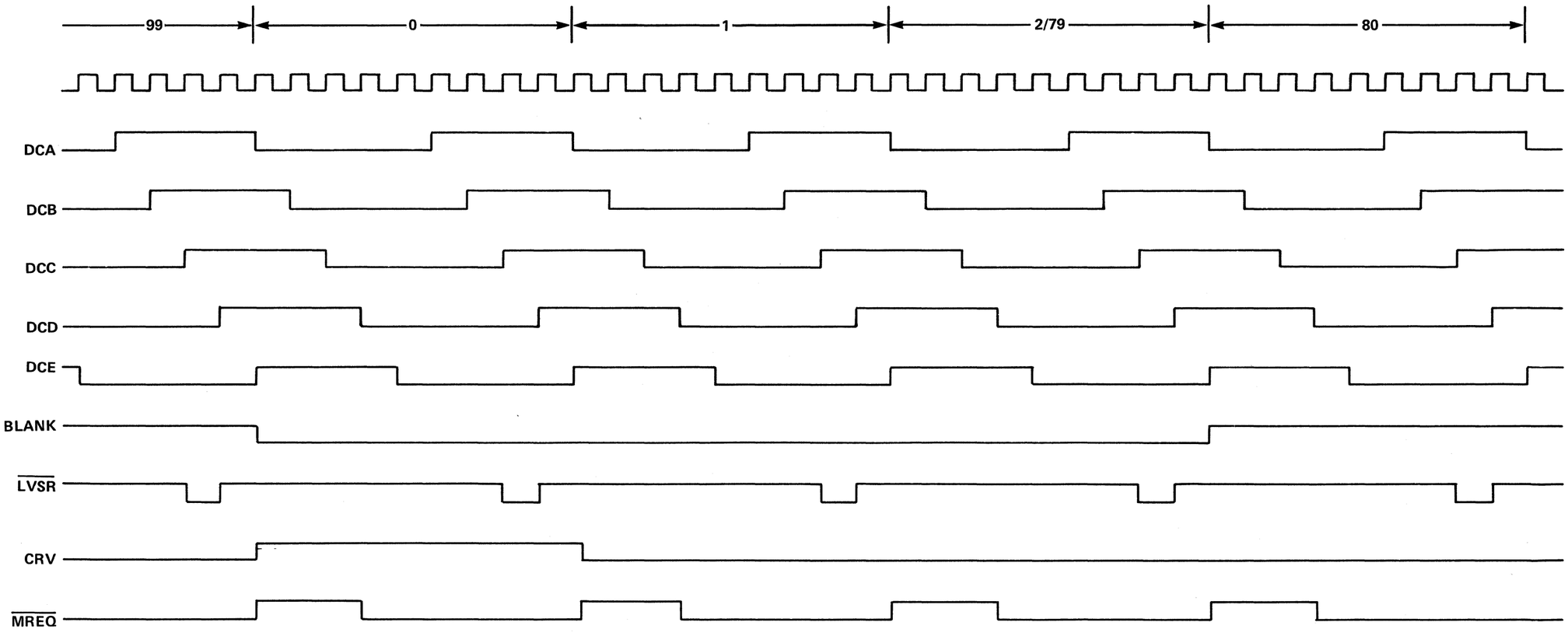
COMPONENT EQUIVALENTS

Zenith No.	Description	Equivalent
103-142-01	Diode	1N4148
103-261-02A	Diode	1N7000
103-261-04A	Diode	1N7000
103-263A	Diode	1N4007
103-280-02	Diode	(2) 1N4007's in parallel
103-284	Diode	1N4820
103-295-02A	Diode	BA245
103-295-03A	Diode	1N4148
103-298-04	Diode	1N4822
103-298-05A	Diode	1N5398
212-76	Diode	1N4005
212-76-02	Diode	1N5061
121-699	Transistor	MPSA 70
121-819	Transistor	MPSA 05
121-895	Transistor	2N5210
121-972	Transistor	2N4048 or 2N3700
121-973	Transistor	MPSA 70
121-975	Transistor	MPSA 20
121-1034	Transistor	2N1893 or 2N2854
121-1039	Transistor	BU409 or 2SD724
121-1058	Transistor	2N1893 or 2N2854

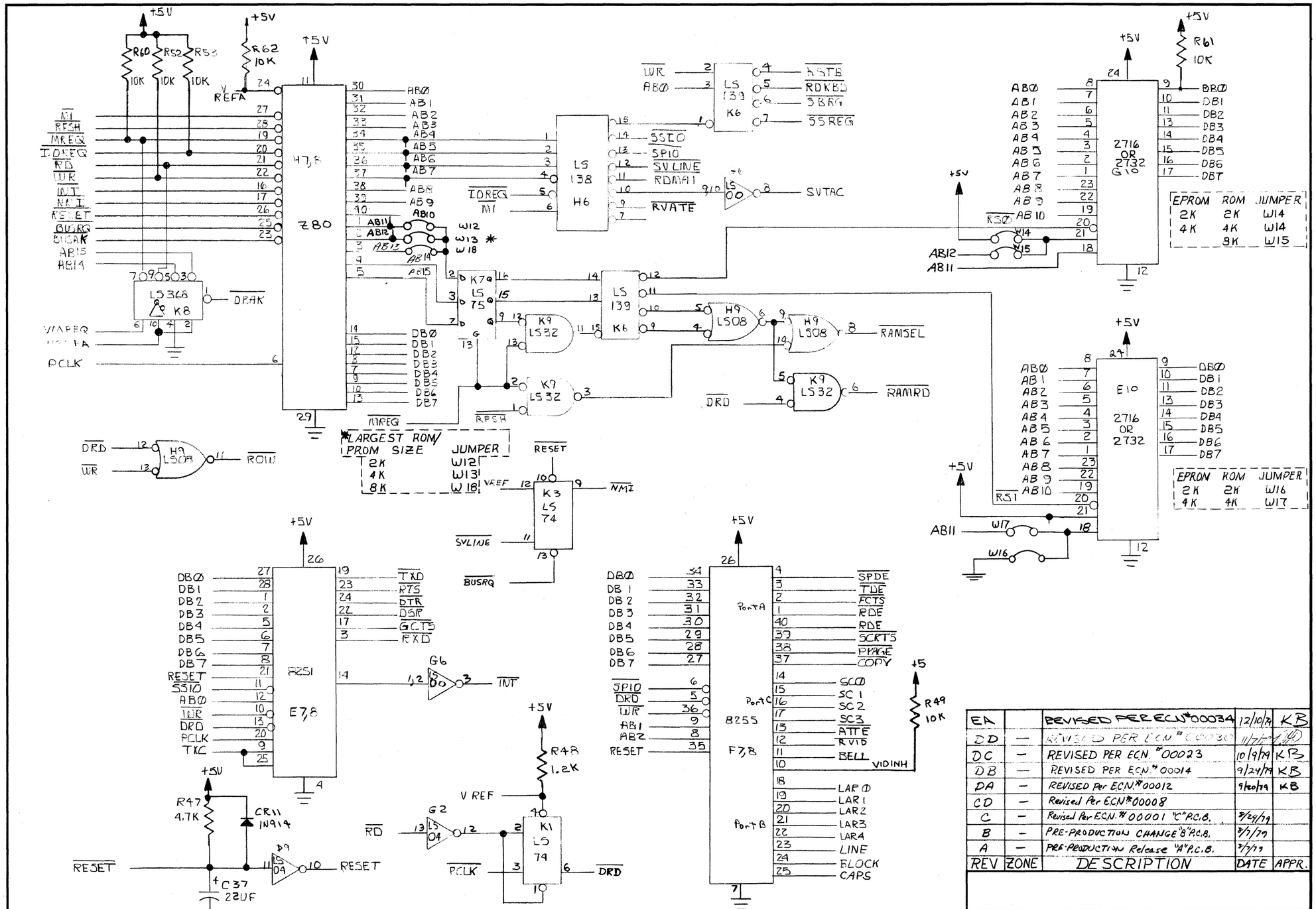


DIAG. VIDEO CABLE

8.0 SCHEMATIC AND TIMING DIAGRAMS



– V200 –
VIDEO TIMING DIAGRAM



REV	ZONE	DESCRIPTION	DATE	APPR.
EA		REVISED PER ECN #00034	12/10/79	KB
DD	—	REVISED PER ECN #00030	11/27/79	KB
DC	—	REVISED PER ECN #00023	10/9/79	KB
DB	—	REVISED PER ECN #00014	9/24/79	KB
DA	—	REVISED PER ECN #00012	9/20/79	KB
CD	—	Revised Per ECN #00008		
C	—	Revised Per ECN #00001 "C" P.C.B.	5/29/79	
B	—	PRE-PRODUCTION CHANGE "B" P.C.B.	5/1/79	
A	—	PRE-PRODUCTION Release "A" P.C.B.	3/1/79	

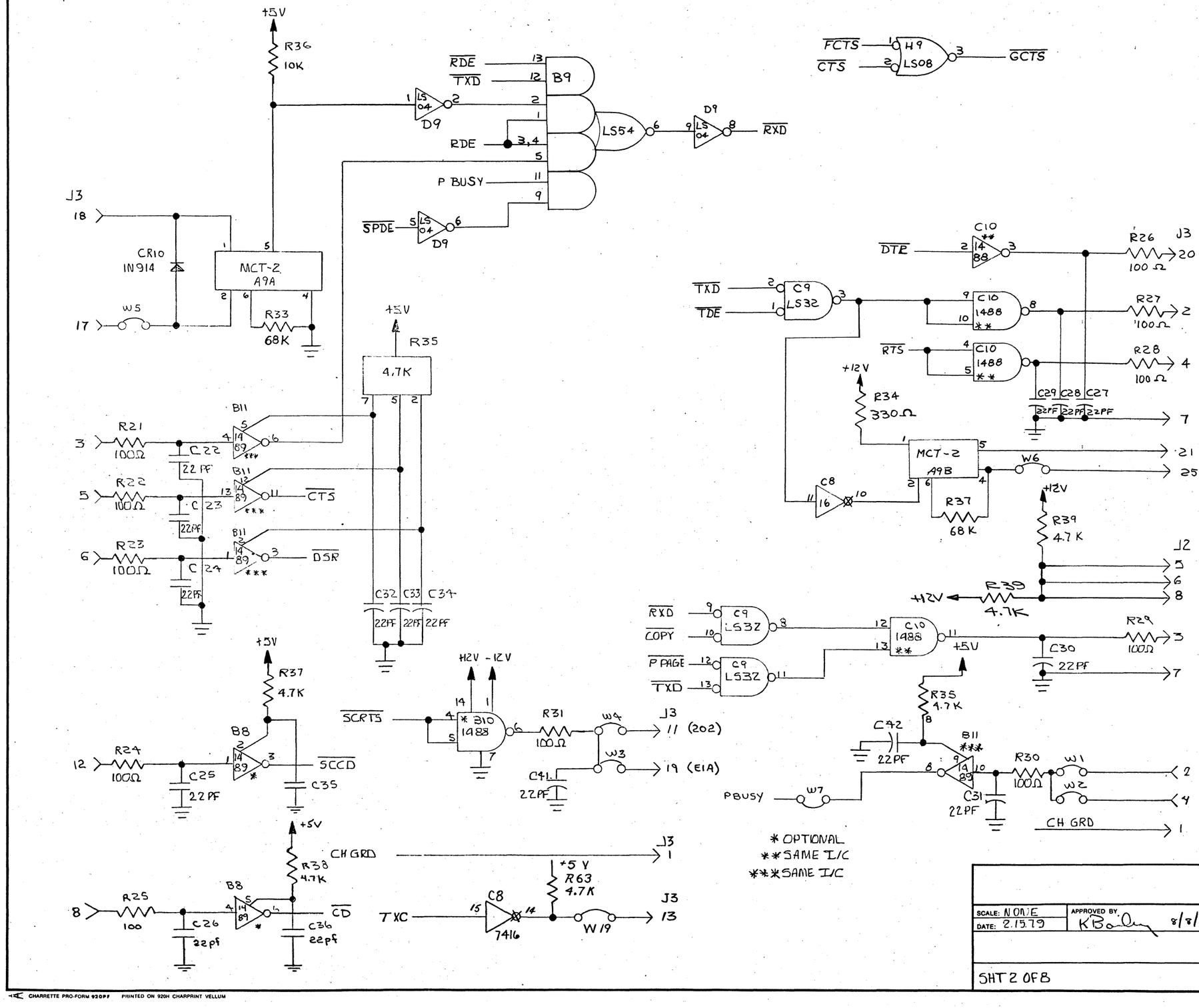
SCALE: NONE
DATE: 2.15.79
APPROVED BY K Bo 8/8/79
DRAWN BY J. PENDERGAST

SCHEMATIC (V200 - VMCS)

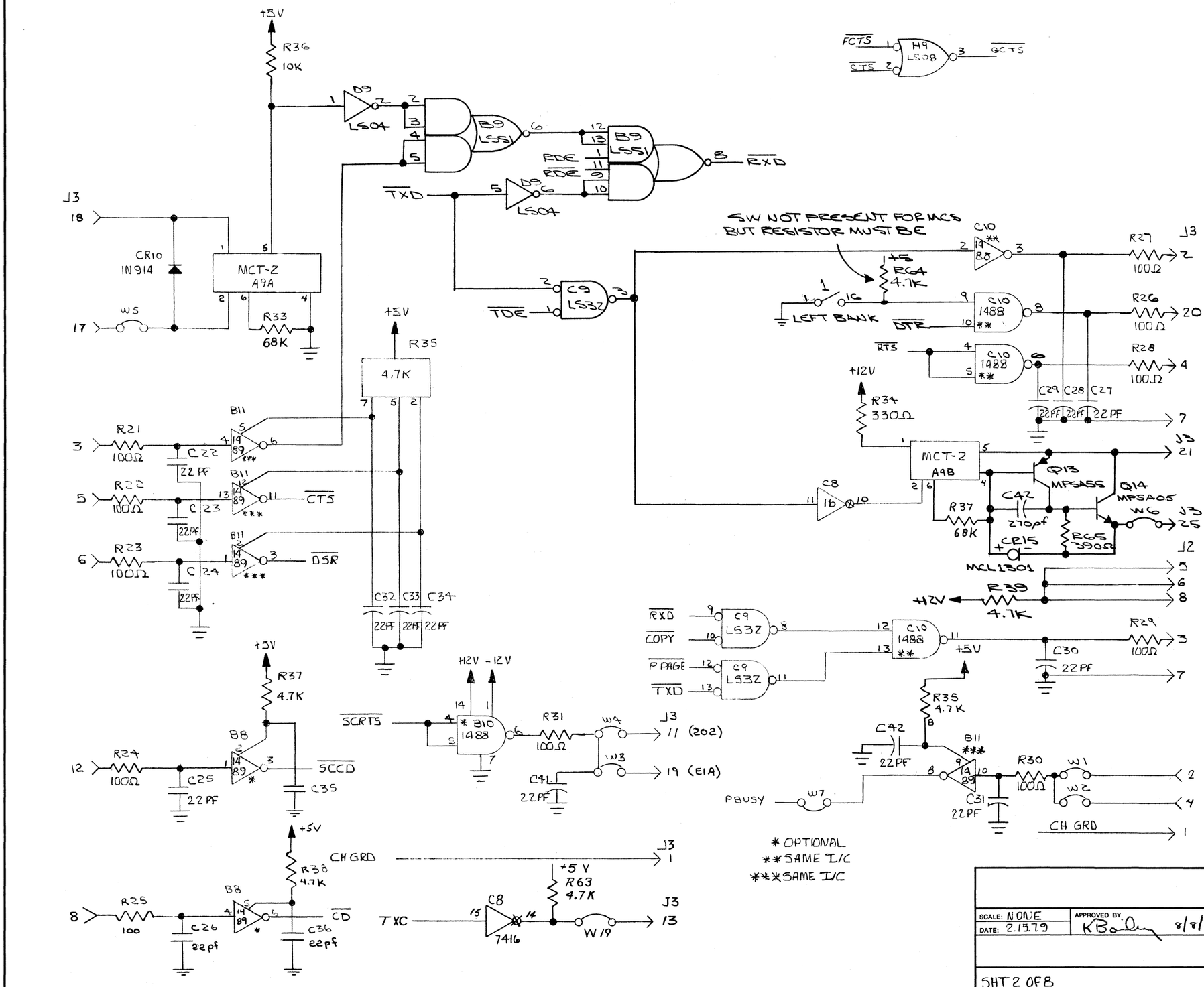
REV EA

SHT 1 OF 8

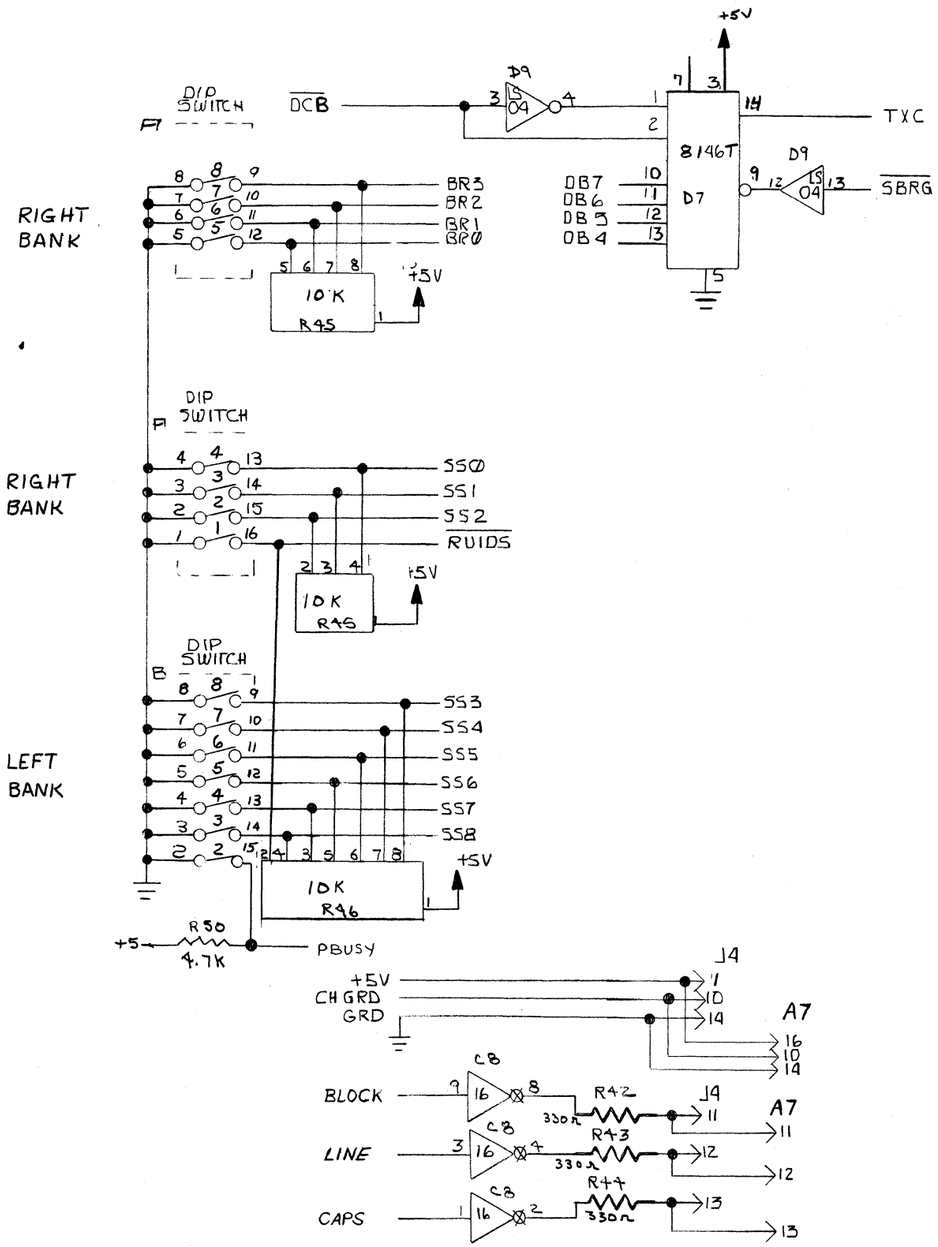
DRAWING NUMBER PS001-001

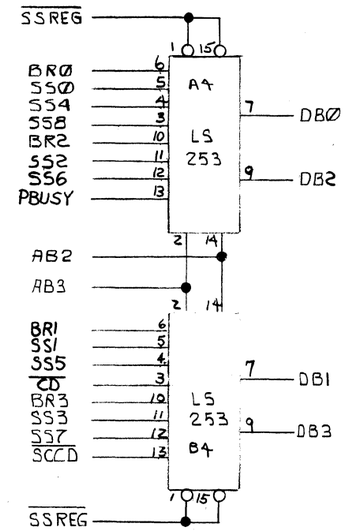


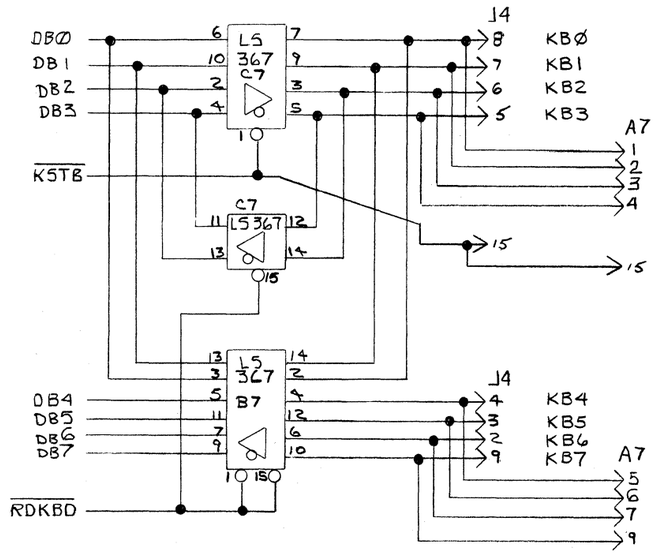
SCALE: NONE	APPROVED BY: KB 8/8/79	DRAWN BY: J. PENDERGAST
DATE: 2.15.79		REV. DD
SHT 2 OF 8		DRAWING NUMBER: PS001-001



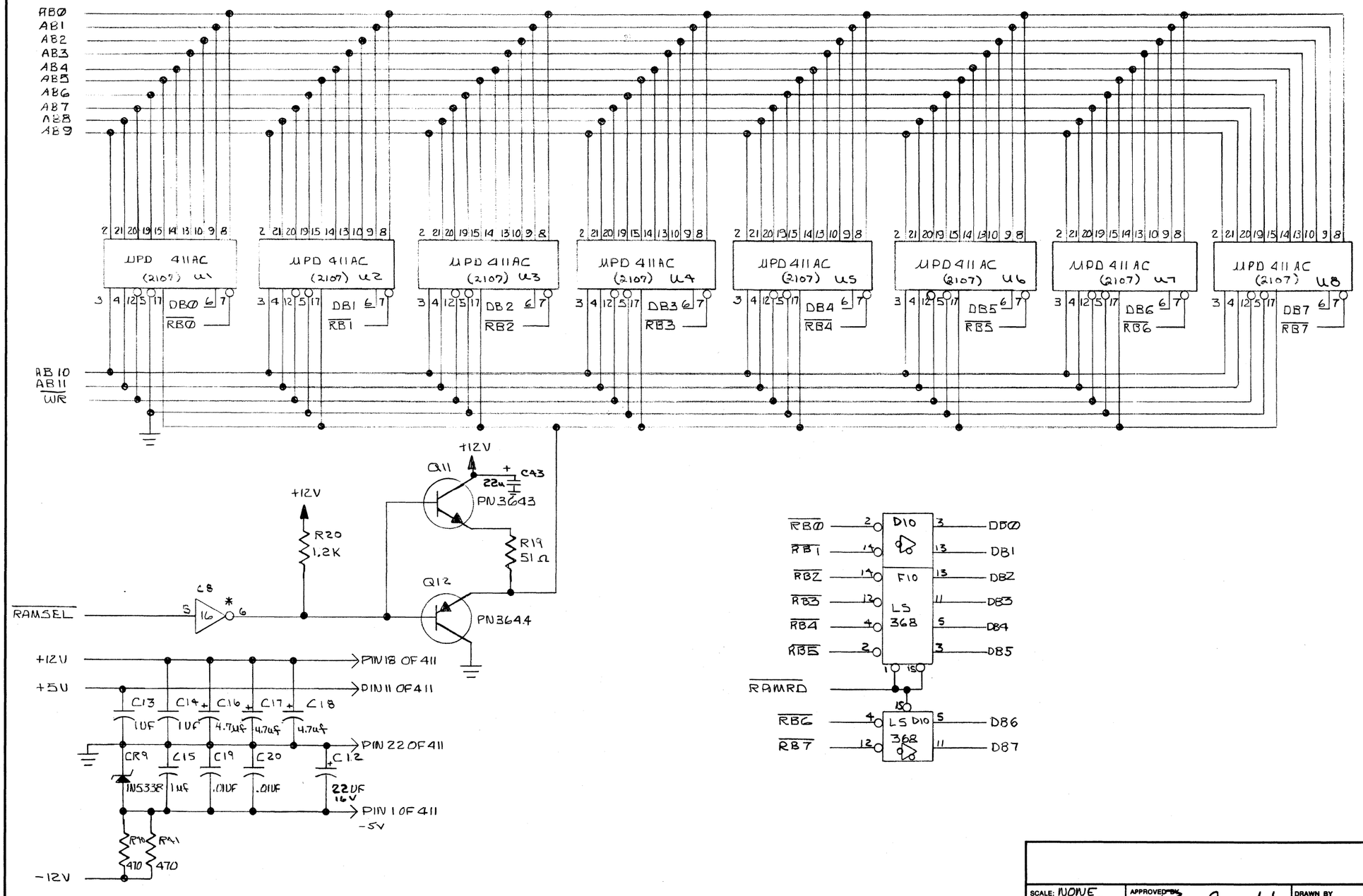
SCALE: NONE	APPROVED BY: KBO 8/8/79	DRAWN BY: J. PENDERGAST	
DATE: 2.15.79			REV EA
SHT 2 OF 8		DRAWING NUMBER: PS001-001	



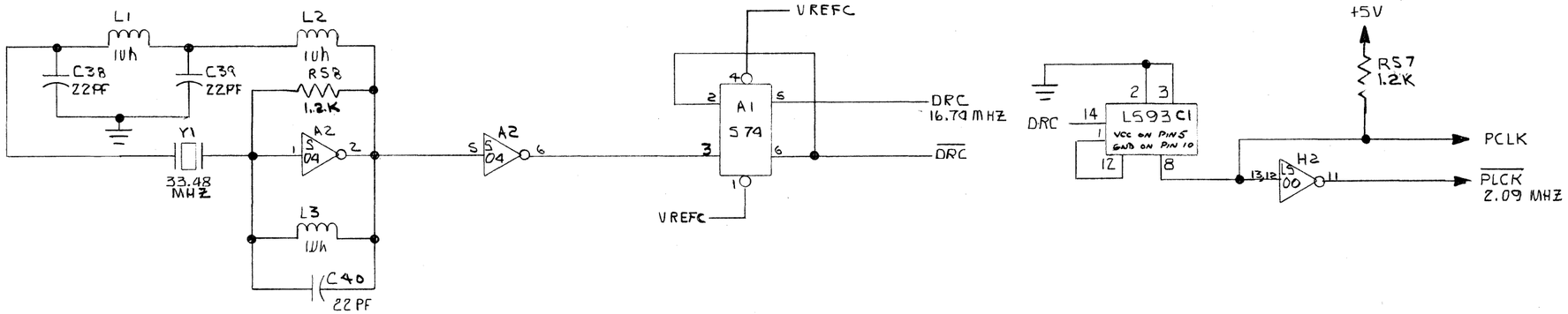


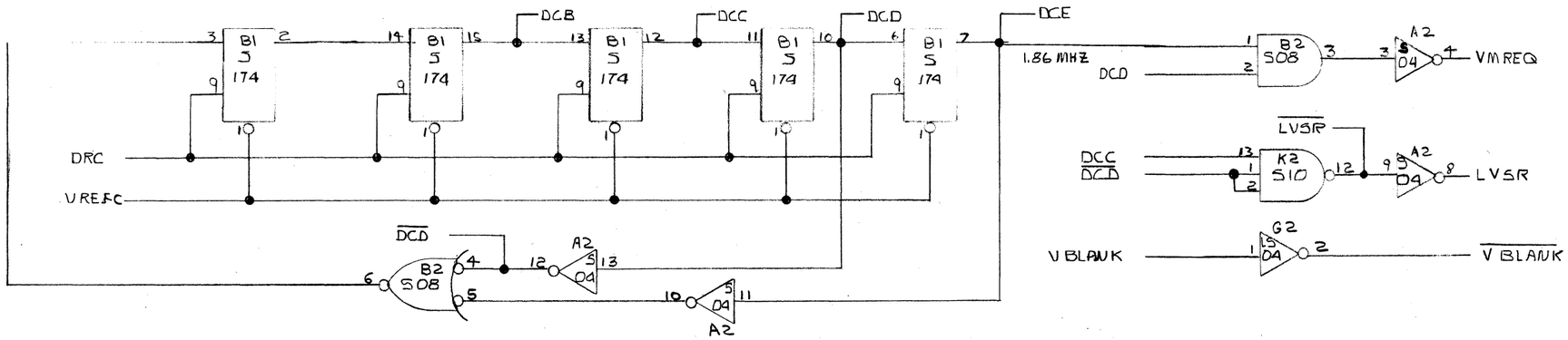


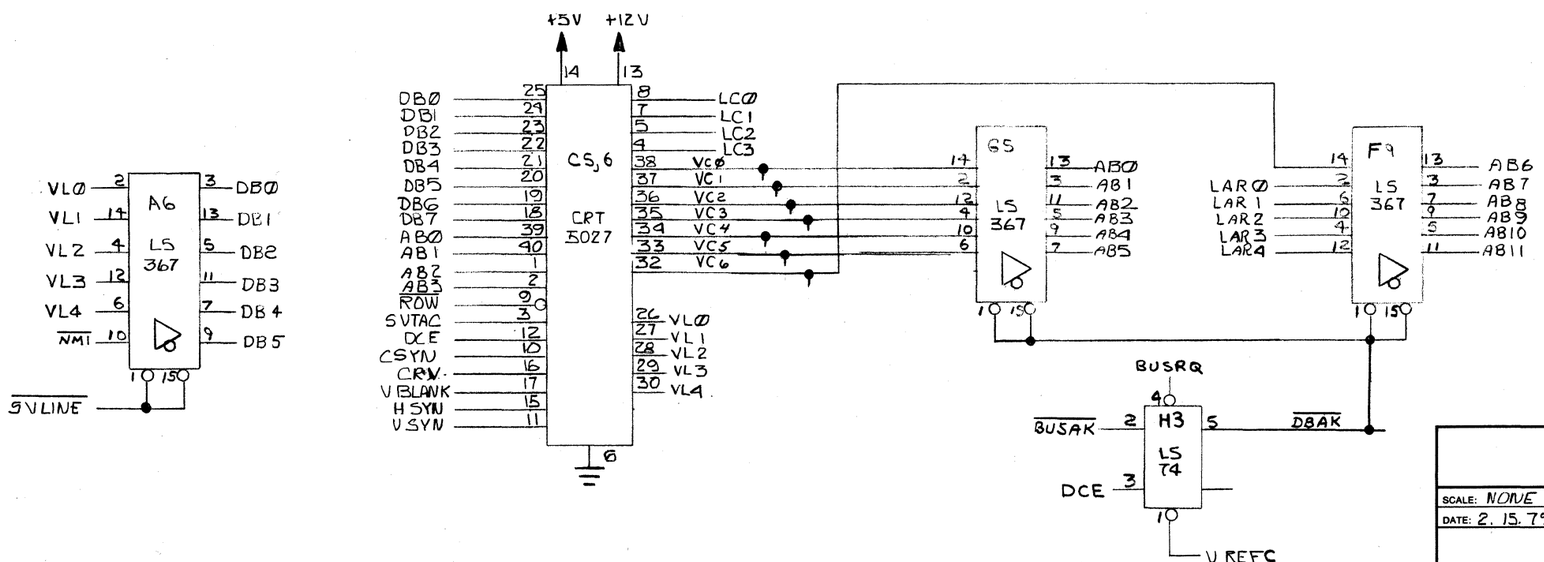
SCALE: NONE	APPROVED BY K Bailey 8/8/79	DRAWN BY J PENDERGAST	
DATE: 2.15.79			REV. EA
SHT 3 OF 8		DRAWING NUMBER PS001-001	



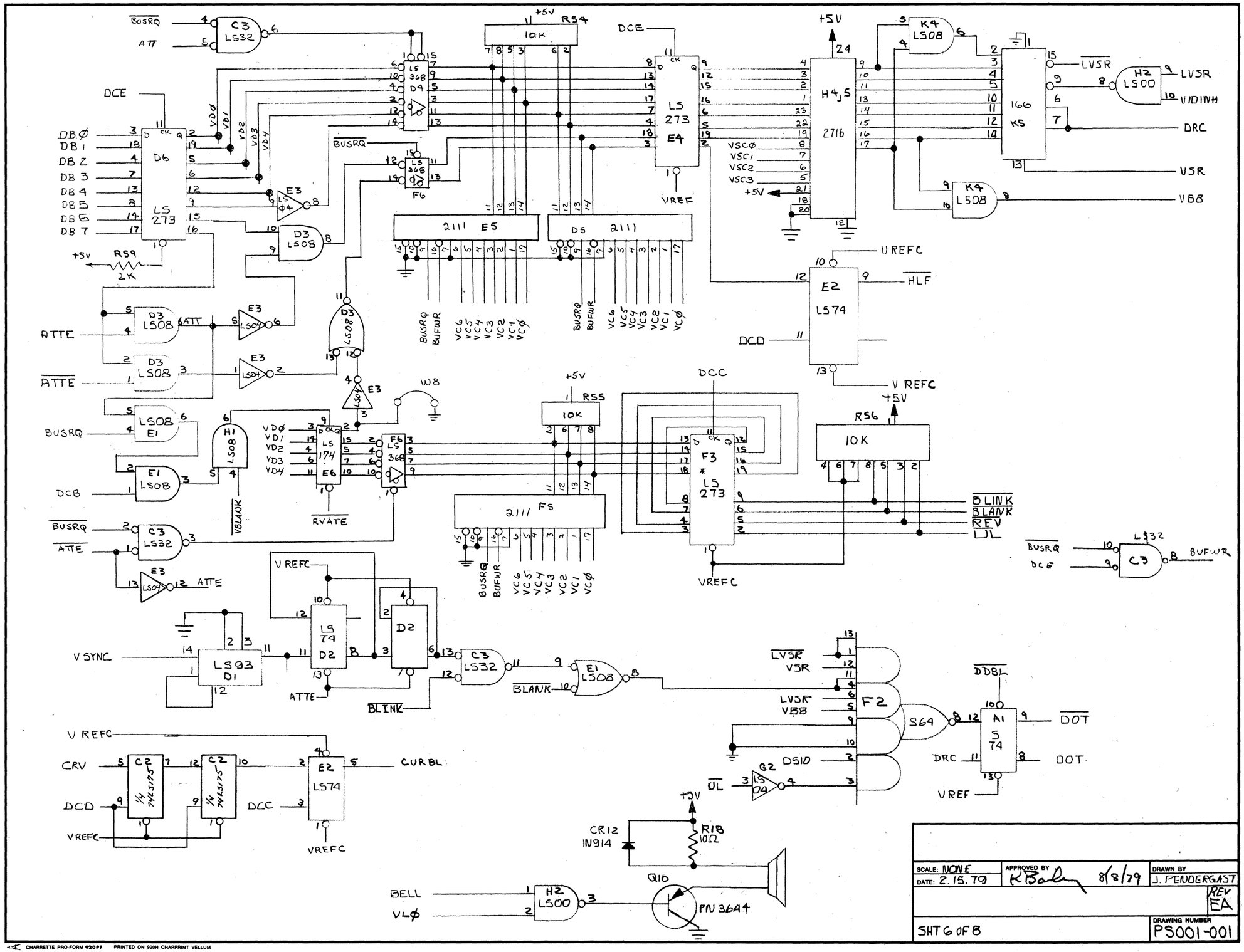
SCALE: NONE	APPROVED BY K Bandy 8/8/79	DRAWN BY J PENDERGAST	
DATE: 2.15.79			REV. EA
SHT 4 OF 8		DRAWING NUMBER PS001-001	



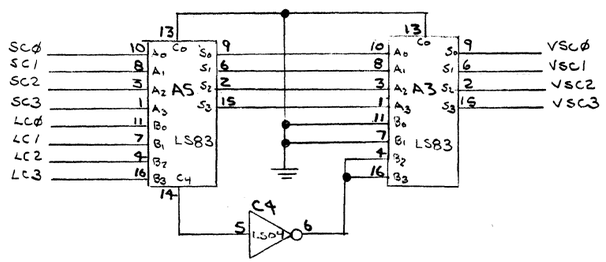


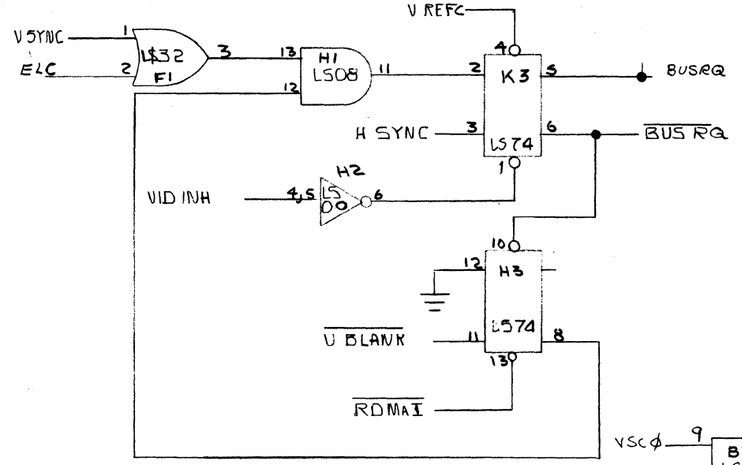


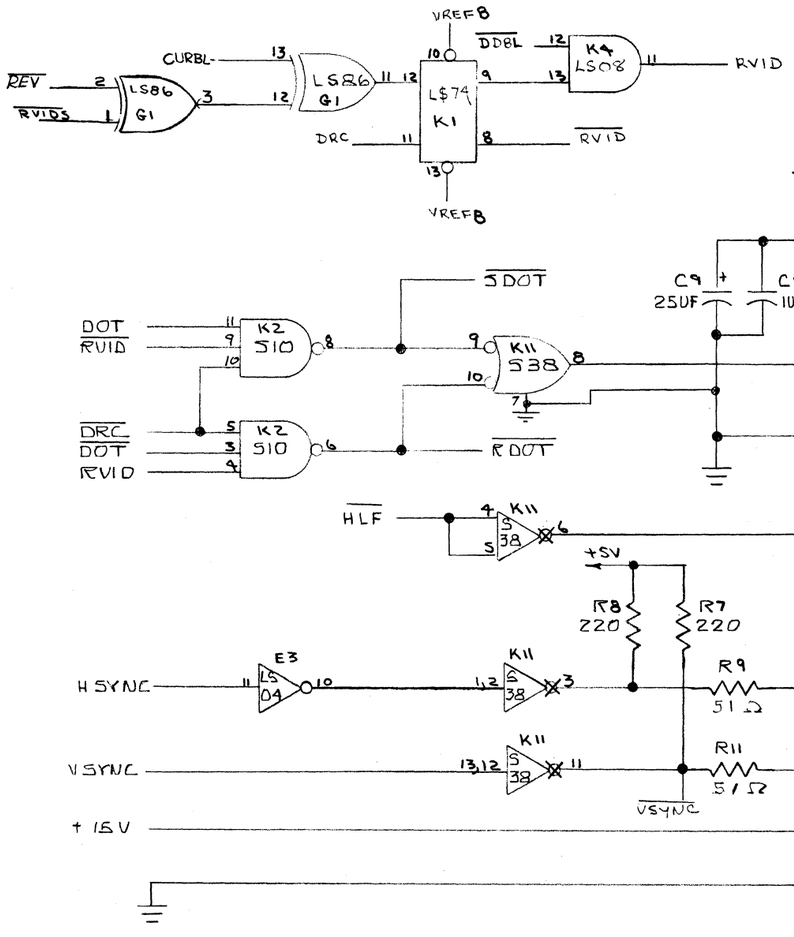
SCALE: NONE	APPROVED BY K Bailey 8/8/79	DRAWN BY J PENDERGAST
DATE: 2.15.79		REV EA
SHT 5 OF 8		DRAWING NUMBER PS001-001

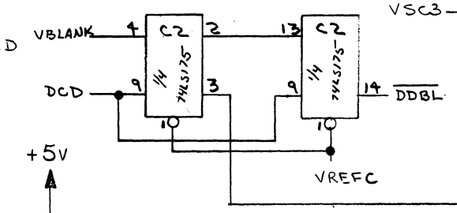


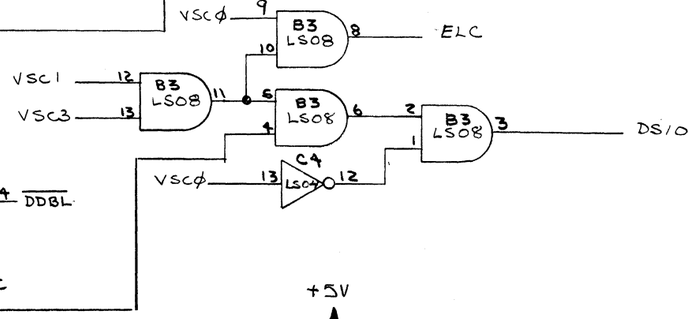
SCALE: NONE	APPROVED BY K Bailey 8/8/79	DRAWN BY J. PENDERGAST	
DATE: 2.15.79			REV EA
SHT 6 OF 8		DRAWING NUMBER PS001-001	

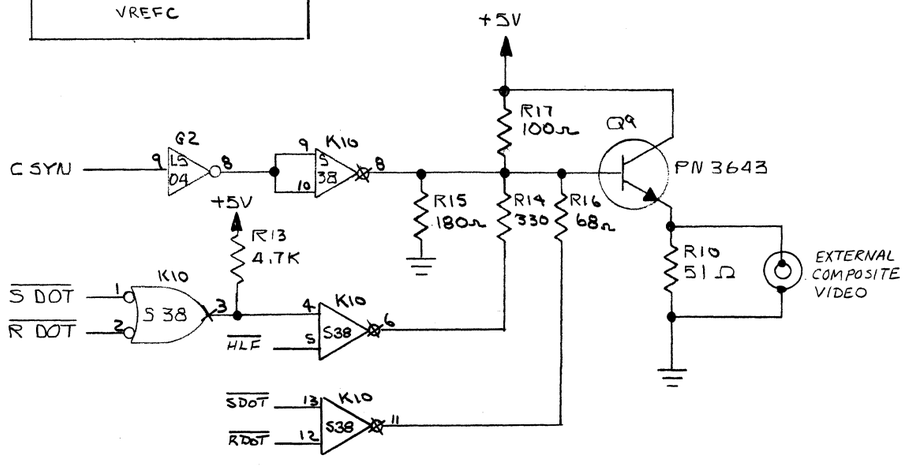




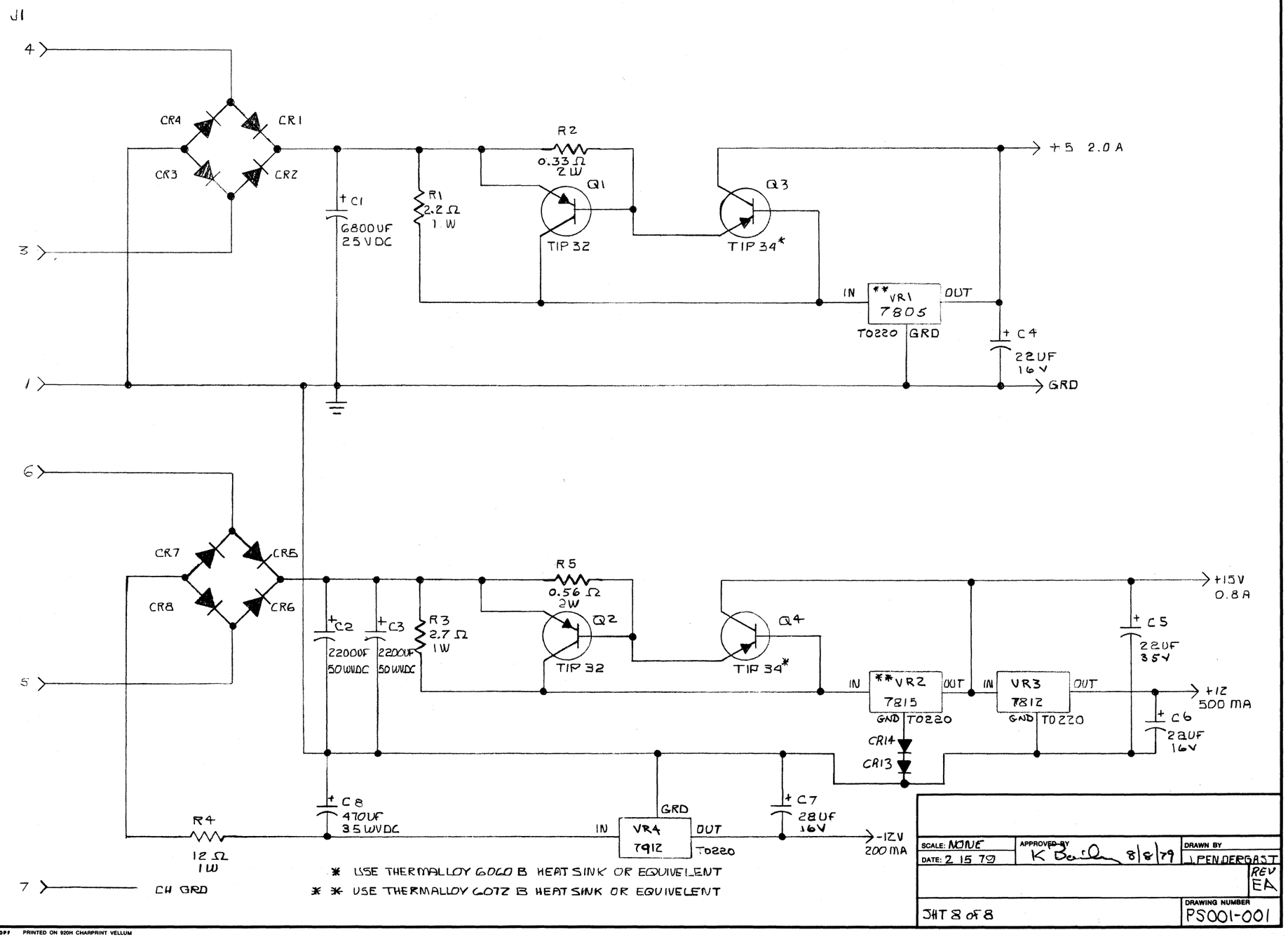




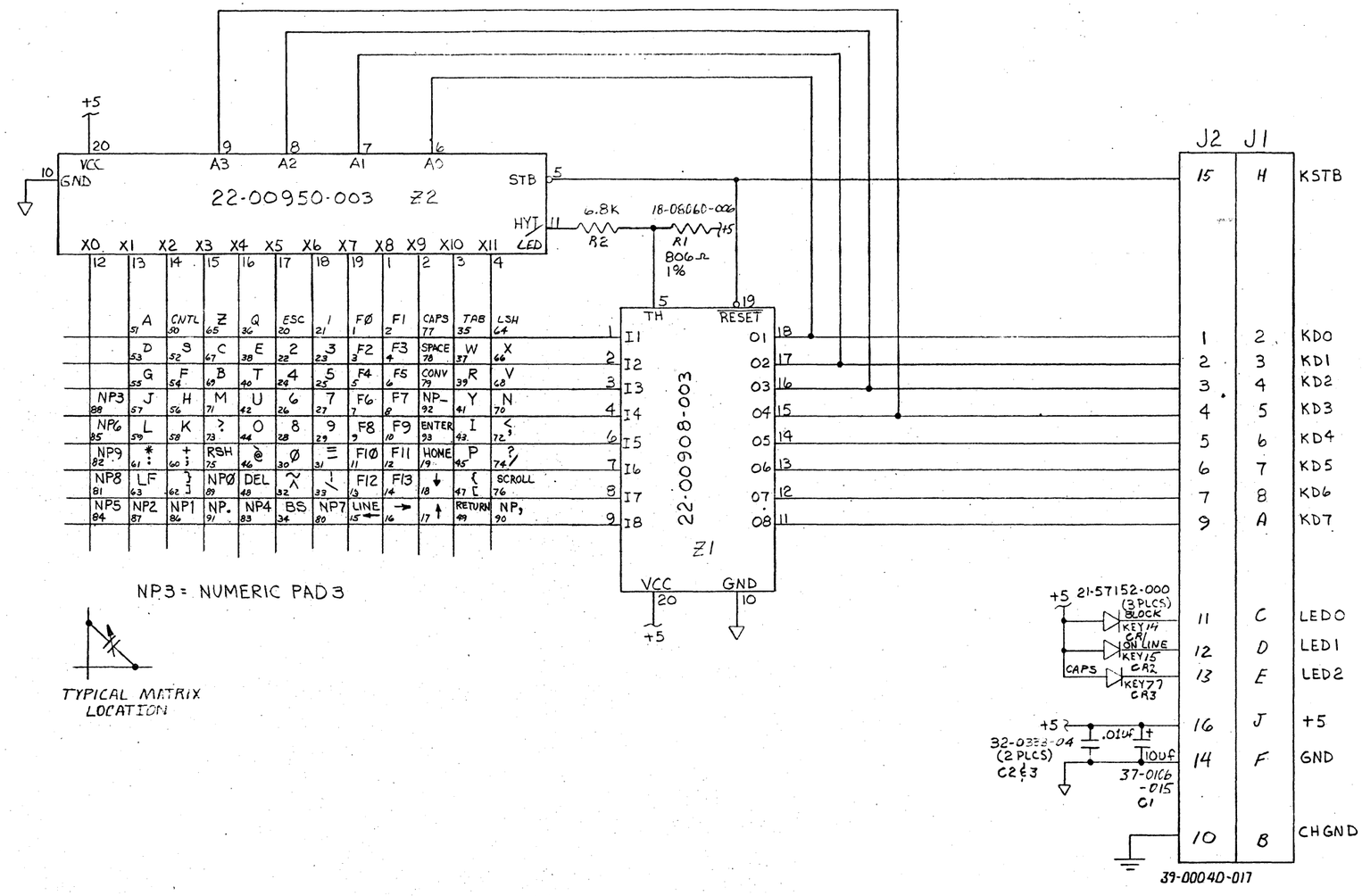




SCALE: NONE DATE: 2.15.79	APPROVED BY K Bem 8/8/79	DRAWN BY J. PENDERGAST	REV EA
SHT 7 OF 8		DRAWING NUMBER PS001-001	



EFF.	REV.	ECO	BY	DESCRIPTION	APP.	DATE
	~		P.T.	PROTO RELEASE		4/24/79
—	A	—	PT	FIRST PROT.		7/13/79
	A	—	WDM	MFG. RFI.		3/14/79
	B	7781	DM	F/A CHG C2 & C3		4/28/83



NP3 = NUMERIC PAD 3

TYPICAL MATRIX LOCATION

LAST REF DES. USED		
R2	C3	CR3
Z2	J2	
REF DES NOT USED		

KB001-002,-003,-004

MANUFACTURE PARTS AND/OR ASSY'S PER K.T.C. DOCUMENT: FTP 36-01022

USED ON VISUAL TECHNOLOGY

UNLESS OTHERWISE NOTED ALL DIMENSIONS ARE IN INCHES
XXX DIMENSION NOT TO SCALE

RELEASED		
APP.		4/24/79
CH.	CM	2-6-79
DR. P. TRAPP		2-5-79

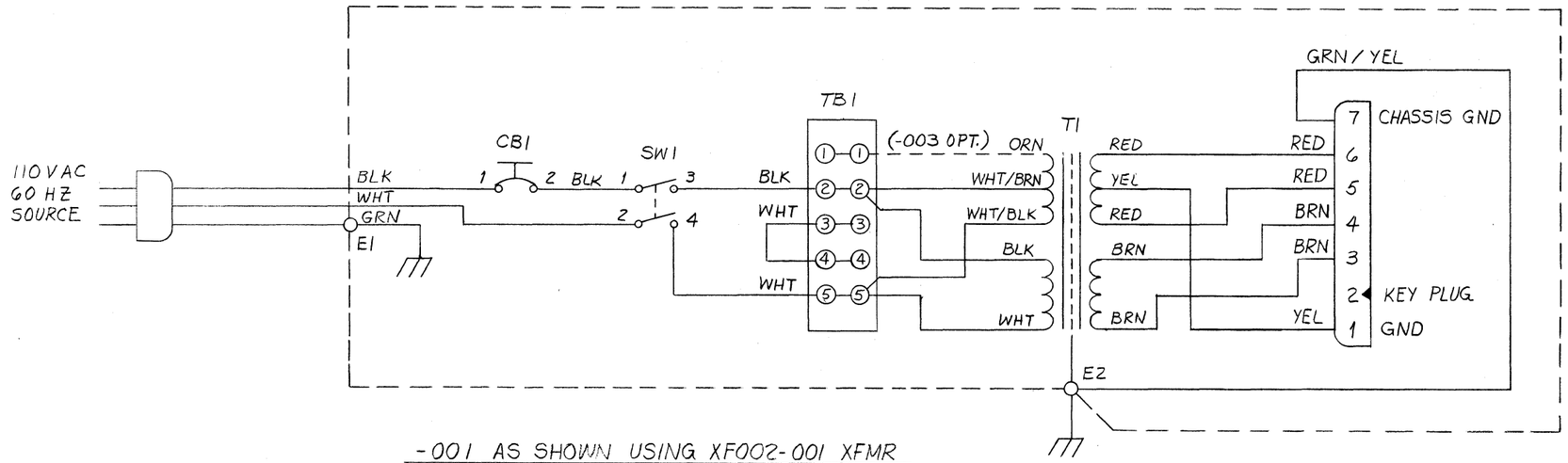
TOL. EXCEPT AS NOTED
HOLE DIA.
FRACT. ± 1/64"
XX ± .01"
XXX ± .005"
ANG. ± 1°

ITEM	PART NO.	DESCRIPTION	QTY.
SCALE		TITLE SCHEMATIC	

key tronic corporation
SPOKANE, WASH., U.S.A.

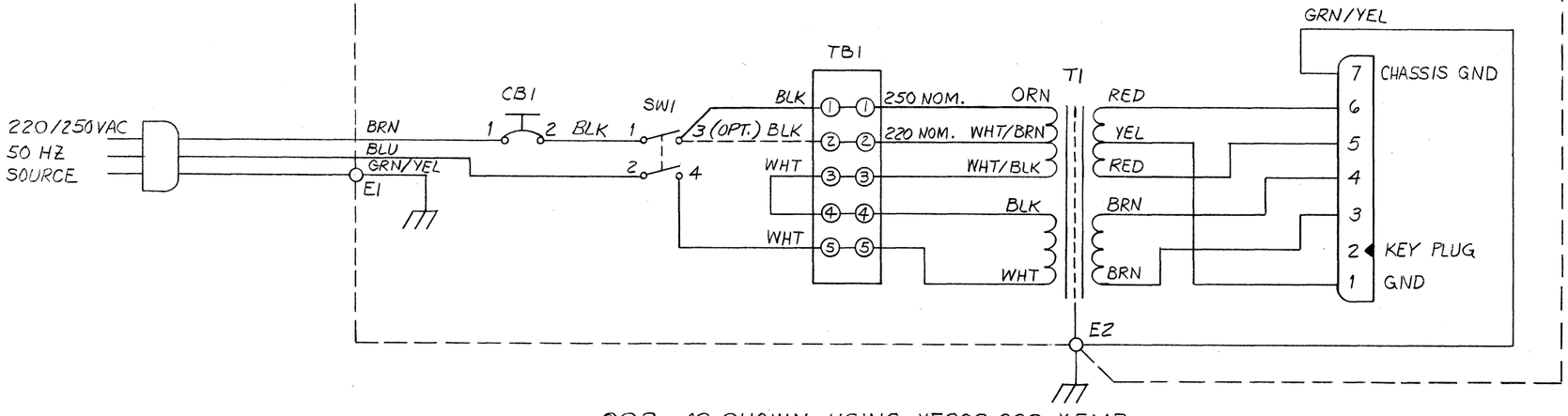
DWG. NO. 35-02006
SHEET 1 OF 1 C

REVISION STATUS				
REV	ZONE	DESCRIPTION	APPROV	DATE
A	-	RELEASED		



-001 AS SHOWN USING XF002-001 XFMR

-003 SAME AS -001 EXCEPT USE XF002-002 XFMR & INSTALL ORG. LEAD IN TB1-1



-002 AS SHOWN USING XF002-002 XFMR

REV-A

VISUAL TECHNOLOGY INC.
DUNDEE PARK, RAILROAD AVE., ANDOVER, MA. 01810

SCALE: NONE	APPROVED BY	DRAWN BY
DATE: 11/8/99		F. Dalton

WIRING DIAGRAM
(PRIMARY POWER V-200)

DRAWING NUMBER WD002-XXX