WD1003V-MM1
Winchester Disk Controller
WD1003V-MM2
Winchester/Floppy Disk Controller

FEATURES

- 100% AT* port and BIOS compatible
- 2:1 interleave
- Look ahead 2 sector cache with 2 KB buffer
- 32-bit ECC, 5-bit correction span, 16-bit CRC
- 5 Mbits/seconds (Mbps) data transfer rate
- Design incorporates the following Western Digital devices:
  - WD42C22
  - WD1017
  - WD10C22
  - WD37C65 (WD1003V-MM2)
- WD1003V-MM2 supports 5 1/4 inch (360 KB or 1.2 MB) and 3 1/2 inch (720 KB or 1.44 MB) floppy drives
- XT height, short form factor (8.33 in. x 3.85 in.)

BENEFITS

- Compatible with all application programs
- Replaces the WD1003-WAH, WD1003A-WA2, or WD1003-WA2
- Enhances sequential access intensive software
- Optimized error detection and correction span
- Standard data transfer rate for MFM drives
- Leading edge technology, highest integration for low power and enhanced reliability
- Frees extra chassis slot
- Fits all chassis types including low profile

DOCUMENT SCOPE

This document describes the functional, electrical and logical design characteristics of the WD1003V-MM1 Winchester disk controller and WD1003V-MM2 Winchester/floppy disk controller. Both Winchester controllers described in this document are identical. All Winchester disk controller descriptions in this document apply to both controllers. Floppy descriptions apply to the WD1003V-MM2 only.

DESCRIPTION

The WD1003V-MM1 is an IBM* Personal Computer AT-compatible controller designed to interface a maximum of two Winchester drives. The drive interface is compatible with the Seagate Technology* ST506/ST412 specifications. Drives connected to the WD1003V-MM1 need not be of the same capacity or configuration. All necessary receivers and drivers are included on the board to allow direct connection to the drive(s).

The WD1003V-MM2 is an IBM Personal Computer AT-compatible Winchester/floppy disk controller designed to interface a maximum of two Winchester drives and two floppy disk drives. The Winchester drive interface is compatible with the Seagate Technology ST506/ST412 specifications. Winchester drives connected to the WD1003V-MM2 need not be of the same capacity or configuration. There are four floppy drive types (360 KB, 720 KB, 1.2 MB, and 1.44 MB) supported by the WD1003V-MM2. The WD1003V-MM2 supports "intelligent" 1.44 MB media drives. These in-

telligent drives determine the drive type and data rate obtained from the drive's media and do not depend upon the state of J1 pin 2 for this information. All necessary receivers and drivers are included on the board to allow direct connection to the drive(s).

ARCHITECTURE

The WD42C22 is the foundation of each Winchester controller's architecture. Other building blocks of each Winchester controller are the WD1017 local microcontroller, WD10C22 self-adjusting data separator and a 2Kx8 RAM for track data buffering. The WD1003V-MM2's floppy disk section includes the WD37C65 floppy disk controller and an associated address decode PAL. Figure 1 is a block diagram of the controllers.

The WD42C22 integrates the central elements of a Winchester controller subsystem, the host interface, buffer management, disk formatter/controller, and drive interface, into an 84-pin device. The WD42C22 communicates to the host, local microcontroller, track buffer, and disk drives through four interface ports.

The WD42C22's host interface port connects directly to the AT (or AT compatible) bus via 12 mA drivers. Operating in AT mode, all host control, data, and task file address lines directly interface to the WD42C22. External address decode is required to map the device at the desired system I/O addresses. System compatibility is assured through integrated I/O port compatible AT task file registers. All fixed disk data transfers are 16-bit Programmed Input/Output (PIO) transfers. Status and control transfers are eight bits wide.

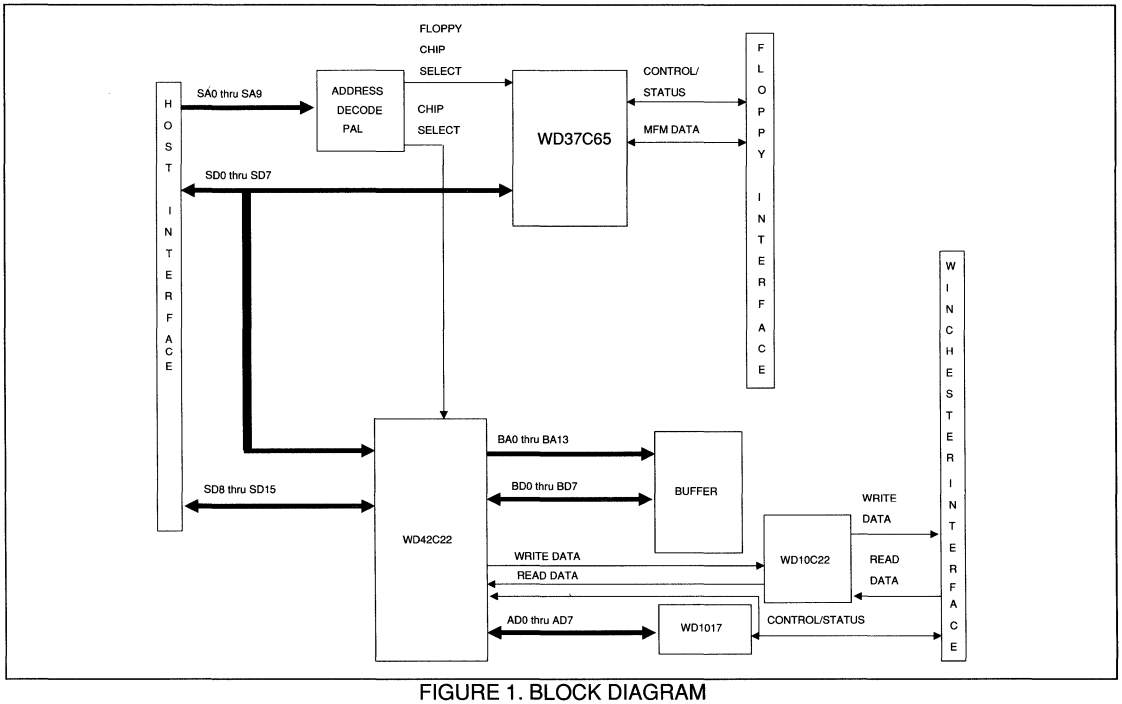

FIGURE 1. BLOCK DIAGRAM

To satisfy requirements for faster system bus rates and data transfers, the WD42C22 operates with 16 MHz 286 microprocessors. The transfer rate between host and WD42C22 under PIO or DMA operation is up to 4 Mwords/sec. (Refer to the WD42C22 data sheet for complete timing information.) Although the WD42C22 is capable of DMA operation, the controller uses the WD42C22's PIO mode only.

The WD42C22 contains an advanced buffer manager that controls a double sector buffer of 2 KB. Pipelined host and disk address counters enable sustained, simultaneous transfers on each port. Sufficient RAM buffer bandwidth is available to allow 2:1 interleaved, 5 Mbps disk transfers while simultaneously performing 16-bit host transfers up to 4 Mwords/sec.

The local microcontroller sends host mode, buffer manager, and drive controller information to the WD42C22's local microcontroller interface port. The local microcontroller is usually idle until assertion of the microcontroller's interrupt signal. Assertion of the microcontroller interrupt occurs when the host writes to the command register or at the end of each host or disk transfer.

The WD42C22's disk formatter/controller allows operation of two MFM Winchester disk drives. Data integrity is significantly enhanced through the use of software selectable retry algorithms and 32-bit ECC polynomials.

The WD42C22's 48-mA $\overline{\text{DRIVE SELECT0}}$ and $\overline{\text{DRIVE SELECT1}}$ signals are connected directly to the drive cable connectors. $\overline{\text{WRITE FAULT}}$, $\overline{\text{INDEX}}$, and $\overline{\text{DRIVE READY}}$ signals are directly received from the cable connector by the WD42C22's 48 mA receivers. Other drive control signals, e.g. HEAD SELECTs, are under control of the local microcontroller.

The WD1017 local microcontroller, an 8-bit microprocessor, controls and coordinates the activity of the Winchester disk drives and the WD42C22. The WD1017 receives and sends command or status information over the WD1003V's internal multiplexed address/data bus, AD0 through AD7. Normally, the WD1017 is idle until the WD42C22 asserts the microcontroller's interrupt line. The WD42C22 asserts a microcontroller interrupt when the host writes to the command register or at the end of either a host or disk transfer. The WD1017 uses 8KB of internal PROM and 256 bytes of internal RAM. Firmware controlling all these functions, including read ahead cache, resides in the WD1017's PROM.

Western Digital's WD10C22 handles the sensitive read/write signals between the WD42C22 and data drivers and receivers. Read data refers to previously written data, with phase, frequency, and write splice noise. The WD10C22 removes the noise and presents clean digital read signals to the WD42C22. The WD10C22 conditions write data to be recorded on the drive. Data from the WD42C22 is precisely clocked to the drive. If write precompensation is enabled, the WD42C22 produces synchronized, precompensated write data, which is sent directly to the drive's write circuits. The WD10C22, as used on the WD1003V-MM1 and WD1003V-MM2, operates at a 5 Mbps data rate and encodes the data in MFM format.

A 2Kx8 static RAM memory buffers the sector data between the drive(s) and the AT system bus. The buffer also stores the ECC correction information generated by the WD42C22 and the WD1017. The double sector buffer and the above control components allow a 2:1 sector interleave format for optimized system performance.

Another Western Digital "superchip", the WD37C65, on the WD1003V-MM2 provides all the needed functionality between the host and the diskette drive cable connector. The WD37C65 integrates the diskette formatter/controller, data separation, write precompensation, data rate selection, clock generation, and drive interface drivers and receivers into a single 44-pin LSI device.

On the floppy interface, the WD37C65 includes a data separator designed to handle high performance error rates on floppy drives. Write precompensation is included, in addition to the normal formatting, encoding/decoding, stepper motor control, and status sensing functions. All inputs are TTL compatible Schmitt trigger line receivers and outputs are high current, open drain with the 48 mA drivers meeting ANSI specifications.

The host interface is improved for high speed operation supporting 8 or 12 MHz, 286 microprocessor based computers. The inputs are Schmitt triggers (except the data bus). Output drive capability is 20 LS TTL loads, allowing direct interconnection to the system bus (SD0 through SD7) without buffers or transceivers. (Refer to the WD37C65 data sheet for complete timing and specifications.) All floppy data transfers are eight bit transfers only.

The WD37C65 has eight internal registers. The eight bit main status register contains status information for the WD37C65 and may be accessed any time. Another four status registers under system control also give various status and error information. The control register provides support logic that latches the two LSBs on the data bus used to select the desired data rate. Data rate selection controls internal clock generation. The operations register in the WD37C65 replaces the standard latched port used in floppy subsystems.

All clock generation (sampling clock, write clock, and master clock) are included in the WD37C65. Crystal oscillator circuits provide the necessary signals for internal timing. There are two oscillator inputs to the WD37C65. First, the 16 MHz crystal handles all standard data rates (500, 250, and 125 kbps). The second crystal oscillates at 9.6 MHz to support the 300 kbps data rate. The 300 kbps data rate supports the 300 RPM spindle speed.

Some AT compatibles use dual speed diskette drives, i.e. the spindle spins at 300 or 360 RPM. If the dual speed drives are used, jumper W5 positions 1 to 2 should be installed.

The controller interfaces to the system bus address, data and I/O control signals. All fixed disk read/write data transfers are 16 bits wide and utilize the host fast programmed I/O transfer protocol. Fixed disk status and control transfers are eight bits wide. All diskette data, control, and status transfers are eight bits wide. All control and status transfers use the lower data byte (SD07-SD00) only. The controller's register address map is fixed (at a primary or secondary range) as are the bus interrupt requests and the floppy DMA channel assignment.

Internally, these controllers use three buses, ADDRESS/DATA 0 through 7 (AD0 through AD7), BUFFER ADDRESS 0 through 14 (BA0 through BA14), and BUFFER DATA 0 through 7 (BD0 through BD7). The AD0 through AD7 is a bi-directional, multiplexed address and data bus. AD0 through AD7 connects the WD42C22 and WD1017. BA0 through BA12 carry buffer addresses from the WD42C22 to the track buffer. BD0 through BD7 is bi-directional bus carrying data between the WD42C22 and track buffer.

INTERFACE CONNECTORS

The WD1003V-MM1 has six connectors:

P1 62-pin card edge connector

Component side. Pins A1 through A31.

Conductor side. Pins B1 through B31

P2 36-pin card edge connector

Component side. Pins C1 through C18

Conductor side. Pins D1 through D18.

J5 34-pin Winchester drive control cable.

J4 20-pin Winchester drive 0 data cable.

J3 20-pin Winchester drive 1 data cable.

J6 Winchester activity LED connector.

The WD1003V-MM2 has seven interface connectors. P1, P2, and J3 through J6 on the WD1003V-MM2 are identical to the WD1003V-MM1 connectors. J1 is the 34-pin floppy drive connector.

HOST INTERFACE CONNECTORS

P1 and P2 on the controller board directly connect to the host bus. Table 1 lists the pin assignments for P1. Table 2 lists the pin assignments for P2. Consult the host technical reference manual for complete descriptions of the signal functions.

TABLE 1. HOST INTERFACE CONNECTOR (P1) PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O
A1, A10, B4, B5, B7, B8, B15 thru B21, B23, B24, B25, B28, B30	NC	NOT CONNECTED	
A2 thru A9	SD7 thru SD0	SYSTEM DATA BUS 7 thru 0	I/O
A11	AEN	ADDRESS ENABLE	I
A12 thru A31	SA19 thru SA0	SYSTEM ADDRESS BUS 19 thru SYSTEM ADDRESS BUS 0	I
B1, B10, B31	GND	GROUND	
B2	RST	RESET	I
B3, B29	+5V	+5V	
B6	DRQ2	DMA REQUEST CHANNEL2	O
B9	NOT USED.	NOT USED.	
B11	$\overline{\text{MEMR}}$	$\overline{\text{MEMORY READ}}$. NOT USED.	
B12	$\overline{\text{MEMW}}$	$\overline{\text{MEMORY WRITE}}$. NOT USED.	
B13	$\overline{\text{IOW}}$	$\overline{\text{I/O WRITE}}$	I
B14	$\overline{\text{IOR}}$	$\overline{\text{I/O READ}}$	I
B22	IRQ6	INTERRUPT REQUEST 6	O
B26	$\overline{\text{DACK2}}$	$\overline{\text{DMA ACKNOWLEDGE 2}}$	I
B27	T/C	TERMINAL COUNT	I

TABLE 2. HOST INTERFACE CONNECTOR (P2) PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O
C1 thru C10, D1, D3 thru D6, D8 thru D15, D17	NC	NOT CONNECTED	
C11 thru C18	SD8 thru SD15	SYSTEM DATA BUS 8 thru SYSTEM DATA BUS 15	I/O
D2	$\overline{\text{IOCS16}}$	$\overline{\text{I/O CHIP SELECT16}}$	O
D7	IRQ14	INTERRUPT REQUEST 14	O
D16	+5V	+5V	
D18	GND	GROUND	

WINCHESTER DRIVE CONTROL CONNECTOR (J5)

The Winchester drive control connector is a 34-pin connector. Drives attached to J5 must be daisy chained. To terminate the control signal on the controller properly, the last drive on the daisy chain must have a 220/330 ohm resistor pack installed. Table 3 lists the pin assignments for J5. Consult the drive's technical manual for further information on the signal functions.

TABLE 3. WINCHESTER DRIVE CONTROL CONNECTOR (J5) PIN ASSIGNMENTS

GND	PIN	MNEMONIC	NAME	I/O
1	2	$\overline{HS3}$	$\overline{HEAD\ SELECT3}$	O
3	4	$\overline{HS2}$	$\overline{HEAD\ SELECT2}$	O
5	6	$\overline{WG}$	$\overline{WRITE\ GATE}$	O
7	8	$\overline{SC}$	$\overline{SEEK\ COMPLETE}$	I
9	10	$\overline{TK0}$	$\overline{TRACK0}$	I
11	12	$\overline{WF}$	$\overline{WRITE\ FAULT}$	I
13	14	$\overline{HS0}$	$\overline{HEAD\ SELECT0}$	O
15	16	NC	NOT CONNECTED	
17	18	$\overline{HS1}$	$\overline{HEAD\ SELECT1}$	O
19	20	$\overline{INDEX}$	$\overline{INDEX}$	I
21	22	$\overline{DRDY}$	$\overline{DRIVE\ READY}$	I
23	24	$\overline{STEP}$	$\overline{STEP}$	O
25	26	$\overline{DS0}$	$\overline{DRIVE\ SELECT0}$	O
27	28	$\overline{DS1}$	$\overline{DRIVE\ SELECT1}$	O
29	30	NC	NOT CONNECTED	
31	32	NC	NOT CONNECTED	
33	34	$\overline{DIRC}$	$\overline{DIRECTION}$	O

WINCHESTER DATA CONNECTORS

The data lines between the controller board and the two Winchester disk drives are connected to J3 and J4. Because the data lines are not identical, J4 must be connected to drive 0 and J3 must be connected to drive 1. Each data connector is a 20-pin connector. Table 4 lists the pin assignments for J3 and J4. Consult the drive technical manual for further information on the signal functions.

TABLE 4. WINCHESTER DRIVE DATA CONNECTORS (J3 and J4) PIN ASSIGNMENTS

GND	PIN	MNEMONIC	NAME	I/O
2	1	NC	NOT CONNECTED	
4	3	NC	NOT CONNECTED	
6	5	NC	NOT CONNECTED	
	7, 8		NOT USED	
	9, 10	NC	NOT CONNECTED	
11				
12				
	13	WMFM+	WRITE MFM DATA+	O
	14	WMFM-	WRITE MFM DATA-	O
15				
16				
	17	RMFM+	READ MFM DATA+	I
	18	RMFM-	READ MFM DATA-	I
19				
20				

WINCHESTER ACTIVITY LED CONNECTOR

The 4-pin Winchester activity LED connector attaches to the computer's front panel via a reversible cable. The controller lights the LED when the controller selects the drive or the host asserts RESET. Table 5 describes J6's pin assignments and functions.

TABLE 5. WINCHESTER ACTIVITY LED CONNECTOR (J6) PIN DESCRIPTION

SIGNAL PIN	SIGNAL NAME	DESCRIPTION
1,4	LED	Connects to LED anode. Tied to +5V with a current limiting resistor.
2,3	$\overline{\text{LED}}$	Connects to LED cathode. Assertion of $\overline{\text{LED}}$ lights the LED.

DISKETTE DRIVE DATA and CONTROL CONNECTOR

Cables from the diskette drives attach to a 34-pin connector, J1, on the WD1003V-MM2. Table 6 lists the pin assignments for J1. Consult the diskette drive's technical manual for further descriptions of the signal functions.

TABLE 6. DISKETTE DRIVE CONTROL AND DATA (J1) CONNECTOR PIN DESCRIPTION

GND	PIN	MNEMONIC	NAME	I/O
1	2	$\overline{\text{FRWC}}$	$\overline{\text{FLOPPY REDUCED WRITE CURRENT}}$	O
3, 5	4, 6	NC	NOT CONNECTED	
7	8	$\overline{\text{IDX}}$	$\overline{\text{INDEX}}$	I
9	10	$\overline{\text{MO1}}$	$\overline{\text{MOTOR ENABLE 1}}$	O
11	12	$\overline{\text{FDS2}}$	$\overline{\text{FLOPPY DRIVE SELECT 2}}$	O
13	14	$\overline{\text{FDS1}}$	$\overline{\text{FLOPPY DRIVE SELECT 1}}$	O
15	16	$\overline{\text{MO2}}$	$\overline{\text{MOTOR ENABLE 2}}$	O

TABLE 6. DISKETTE DRIVE CONTROL AND DATA (J1) CONNECTOR PIN DESCRIPTION (CONT'D.)

GND	PIN	MNEMONIC	NAME	I/O
17	18	$\overline{\text{FDIRC}}$	$\overline{\text{FLOPPY DIRECTION}}$	O
19	20	$\overline{\text{FSTEP}}$	$\overline{\text{FLOPPY STEP}}$	O
21	22	$\overline{\text{FWD}}$	$\overline{\text{FLOPPY WRITE DATA}}$	O
23	24	$\overline{\text{FWE}}$	$\overline{\text{FLOPPY WRITE ENABLE}}$	O
25	26	$\overline{\text{FTK0}}$	$\overline{\text{FLOPPY TRACK 0}}$	I
27	28	$\overline{\text{FWP}}$	$\overline{\text{FLOPPY WRITE PROTECT}}$	I
29	30	$\overline{\text{FRDD}}$	$\overline{\text{FLOPPY READ DATA}}$	I
31	32	$\overline{\text{FHS}}$	$\overline{\text{FLOPPY HEAD SELECT}}$	O
33	34	$\overline{\text{DCHG}}$	$\overline{\text{DISKETTE CHANGE}}$	I

REGISTER ADDRESS MAP

All controllers use the WD42C22's task file registers and control ports. The WD42C22's AT task file register include the read/write data register, host error, write pre-compensation cylinder, sector count, sector number, cylinder number, Sector size, Drive, and Head (SDH), host status and host command registers. The WD42C22 AT control ports include the alternate status, fixed disk control and digital input registers. All floppy control, status, and data registers on the WD1003V-MM2 reside in the WD37C65. All disk and floppy registers are mapped into the host primary and secondary I/O port scheme. All Winchester data, control, and status information pass between the task files or control ports. Floppy data, control, and status information pass between the WD37C65 registers and the host. All Winchester data transfers are word transfers except ECC bytes during read long and write long commands. ECC bytes are transferred in byte mode. Control and status information are also transferred in byte mode. The task files and control ports are multiplexed with IOR and IOW to give 14 possible ports. Six of the ports are bi-directional. Two ports have different definitions for read and write operations. Jumpers select primary or secondary addresses.

Table 7 summarizes the port address map for the controllers. Table 8 lists the task file bit assignments. Table 9 lists the WD42C22 control port, floppy status, control, and data registers. (Consult the WD42C22 data sheet for detailed descriptions of the task file and control port bit assignments.) Table 10 defines the control and status register bits. Bit assignments are with respect to the lower byte host bus terms, SD0 thru SD7.

The SDH register description in Table 8 slightly differs from the standard description in the WD42C22 data sheet. Note that the SDH register is set for the ECC option mode and 512 bytes per sector. The SDH register also limits the number of drives to two and the number of heads to 16.

The WD42C22 contains several additional control and buffer management registers. The WD1017 accesses these registers through the WD42C22's local microcontroller interface ports. The host can not directly address the local microcontroller ports.

TABLE 7. REGISTER ADDRESS MAP

PRIMARY	SECONDARY	READ	WRITE
		WD42C22 TASK FILES	
1F0	170	Data register (16 bits)	Data register (16 bits)
1F1	171	Error register	Write pre-compensation
1F2	172	Sector count	Sector count
1F3	173	Sector number	Sector number
1F4	174	Cylinder number (low byte)	Cylinder number (low byte)
1F5	175	Cylinder number (high byte)	Cylinder number (high byte)
1F6	176	SDH register	SDH register
1F7	177	Status register	Command register
		CONTROL AND STATUS REGISTERS	
3F2	372		Digital output register (WD37C65 operations register)
3F4	374	Main floppy status register (WD37C65)	
3F5	375	Floppy data register (WD37C65)	Floppy data register (WD37C65)
3F6	376	Alternate fixed status (WD42C22 control port)	Fixed disk (WD42C22 control port)
3F7	377	Digital input register	Floppy control register (WD37C65)

NOTE

All addresses in Table 7 are in hex.

TABLE 8. WD42C22 TASK FILE BIT ASSIGNMENTS

REGISTER	7	6	5	4	3	2	1	0
Write pre-comp (1F1/171, write)	Cylinder number divided by 4							
Error (1F1/171, read)	BB	ECC	0	IDNF	0	AC	TK0	DMNF
Sector count (1F2/172, read/ write)	Number of sectors							
Sector number (1F3/173, read/ write)	Starting sector number							
Cylinder number (1F4/174, read/ write)	Cylinder number (low byte)							
Cylinder number (1F5/175, read/ write)	0	0	0	0	0	Cyl. no. MSB		
SDH (1F6/176, write)	1	0	1	DS	HS3	HS2	HS1	HS0
Command (1F7/177, write)	Command							
Status (1F7/177, read)	ABSY	RDY	WF	SC	DRQ	DWC	IDX	ERR

TABLE 9. CONTROL AND STATUS REGISTERS

REGISTER	7	6	5	4	3	2	1	0
Digital output (3F2/372, write)	X	X	MOEN2	MOEN1	FDMA	FRST	X	FDSEL
Main floppy status (3F4/374, read)	RQM	DIO	EXM	CB	0	0	D_1B	D_0B
Alternate status (3F6/376, read)	BSY	RDY	WF	SC	DRQ	DWC	IDX	ERR
Fixed disk (3F6/376, write)	0	0	0	0	HS3EN	RST	$\overline{IEN}$	0
Digital input (3F7/377, read)	DCHG*	$\overline{WTG}$	$\overline{HS3}$	$\overline{HS2}$	$\overline{HS1}$	$\overline{HS0}$	$\overline{DS1}$	$\overline{DS0}$
Floppy control (3F7/377, write)	0	0	0	0	0	0	SDB_1	SDB_0

*Applies to the WD1003V-SM2 only. This bit originates from the floppy controller.

TABLE 10. CONTROL AND STATUS REGISTER BIT DEFINITIONS

REGISTER	BIT MNEMONIC	BIT NAME/DEFINITION
Digital	X	Reserved.
output	MOEN2	MOTOR ENABLE 2 and MOTOR ENABLE 1.
(3F2/372, write)	MOEN1	Controls floppy drive motors. Setting this bit to 0 turns off the associated drive and drive selection cannot occur.
	FDMA	FLOPPY DISK INTERRUPT and DMA ENABLE. Setting this bit to 1 gates floppy DMA and interrupt requests to the I/O interface. Setting this bit to 0 disables the DMA and interrupt requests drivers.
	FRST	FLOPPY RESET. Setting to 0 resets the floppy controller. Floppy reset time is 3.5 µsec. Set to 1 by host software enables the floppy controller.
	FDSEL	FLOPPY DISK SELECT. Setting to 0 selects drive A. Setting to 1 selects drive B. Appropriate MOTOR ENABLE bit must be set.
Main floppy	RQM	REQUEST FOR MASTER. Set to 1 to indicate
status		that the floppy controller register is ready
(3F4/374, read)		for a data transfer. Used with the DIO bit.
	DIO	DATA INPUT/OUTPUT. Controls data transfer direction. Setting to 0 indicates data transfer is from host to floppy. Setting to 1 indicates data transfer is to host from floppy.
	EXM	EXECUTION MODE. Set to 1 only during the execution phase in non-DMA mode.
	CB	Set to 1 to indicate a read or write command in progress.
	D_1B	Set to 1 when floppy drive B is in seek mode.
	D_0B	Set to 1 when floppy drive A is in seek mode.
Alternate	BSY	Controller busy flag.
fixed disk	RDY	READY from selected drive.
status	WF	WRITE FAULT from selected drive.
(3F6/376, read)	SC	SEEK COMPLETE from selected drive.

TABLE 10. CONTROL AND STATUS REGISTER BIT DEFINITIONS (CONT'D.)

REGISTER	BIT MNEMONIC	BIT NAME/DEFINITION
Alternate fixed disk status	DWC	DATA WAS CORRECTED. Set to 1 by the WD1017 indicates a detected and corrected error in the data field.
(3F6/376, read)	IDX	INDEX. INDEX pulse from selected drive.
(cont'd.)	ERR	ERROR. WD1017 sets this bit upon occurrence of a non-recoverable error. The error register describes the error condition when this bit is active.
Fixed disk	HS3EN	Setting to 1 enables $\overline{HS3}$.
(3F6/376, write)	RST	RESET. Writing a 1 to this bit resets the WD42C22. The RESET output remains asserted until this bit is changed to 0. This bit must be set for a minimum of 5.0 µsec. If the WD1017 disables RESET, then writing a 1 to this bit only resets the WD42C22. RESET is not asserted in this case. The WD42C22 asserts the microcontroller interrupt and the WD1017 is responsible for resetting the drive controller board logic.
	$\overline{IEN}$	$\overline{INTERRUPT\ ENABLE}$. Enables or disables IRQ14. Setting to 1 disables interrupts. This bit does not clear the interrupt level in the disabled state. A pending interrupt would occur when the interrupt is enabled again. A system master reset clears the interrupt but leaves the interrupt disabled. Set $\overline{IEN}$ to zero after a master reset to enable the interrupts.
Digital input (3F7/377, read)	DCHG	DISKETTE CHANGE. Set to 1 if no floppy is in the drive, drive door is open, or the drive is not ready. The floppy subsection outputs the DCHG bit.
	$\overline{WTG}$, $\overline{HS3}$ thru $\overline{HS0}$, $\overline{DS1}$, $\overline{DS0}$	$\overline{WRITE\ GATE}$, $\overline{HEAD\ SELECT\ 3}$ thru $\overline{HEAD\ SELECT\ 0}$, $\overline{DRIVE\ SELECT\ 1}$, $\overline{DRIVE\ SELECT\ 0}$. These bits show the status of the appropriate drive control pins. The WD42C22 ouptuts these drive control bits.
Floppy control (3F7/377, write)	SDB_1, SDB_0	These bits control the data transfer rate between the floppy controller and drive as well as the data encoding format. The floppy control registers bit definitions are as follows:

TABLE 10. CONTROL AND STATUS REGISTER BIT DEFINITIONS (CONT'D.)

REGISTER	BIT MNEMONIC	BIT NAME/DEFINITION		
Floppy control (3F7/377, write) (cont'd.)		SDB_1	SDB_0	
		0	0	500 kbps MFM*
		0	1	300 kbps MFM
		1	0	250 kbps MFM
		1	1	125 kbps FM**

*Default data rate after reset.

**International exchange standard for 5 1/4 inch floppies.

WINCHESTER COMMANDS

The Winchester command set contains eight commands. Table 11 describes the eight Winchester commands and their bit assignments. A description of typical Winchester command sequences and the Winchester commands follow Table 11.

TABLE 11. COMMANDS AND COMMAND CODES

COMMAND	HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0
Restore	0	0	0	1	R3	R2	R1	R0
Seek	0	1	1	1	R3	R2	R1	R0
Read sector	0	0	1	0	0	0	L	T
Write sector	0	0	1	1	0	0	L	T
Format track	0	1	0	1	0	0	0	0
Read verify	0	1	0	0	0	0	0	T
Diagnose	1	0	0	1	0	0	0	0
Set parameters	1	0	0	1	0	0	0	1

LEGEND

R3 through R0 — Step rate selection bits. Refer to Table 12 for more details.

L — Read or write long bit. Setting to 1 enables read or write long mode.

T — Retry bit. Setting to 1 disables retries.

The stepping rates for the commands that perform implied seeks are set in the least significant nibble of the last executed restore or seek command. Table 12 describes the Winchester step rates.

TABLE 12. STEPPING RATES

R3	R2	R1	R0	HEX EQUIVALENT	STEPPING RATE
0	0	0	0	0	35 µsec
0	0	0	1	1	0.5 msec
0	0	1	0	2	1.0 msec
0	0	1	1	3	1.5 msec
0	1	0	0	4	2.0 msec
0	1	0	1	5	2.5 msec
0	1	1	0	6	3.0 msec
0	1	1	1	7	3.5 msec
1	0	0	0	8	4. 0 msec
1	0	0	1	9	4.5 msec
1	0	1	0	A	5.0 msec
1	0	1	1	B	5.5 msec
1	1	0	0	C	6.0 msec
1	1	0	1	D	6.5 msec
1	1	1	0	E	3.2 µsec
1	1	1	1	F	16 µsec

NOTE

Stepping rates 0_{16}, E_{16}, and F_{16}, follow the WD42C22 specifications. Following a reset or diagnose command, the step rate defaults to D_{16} (6.5 msec). The WD1017's instruction loop timing governs the step rate accuracy.

WINCHESTER COMMAND SEQUENCE

This section describes a typical Winchester command execution sequence. This description illustrates the relationship between the host and the major components of the controller during command execution.

In the idle state, the WD42C22 and WD1017 drive control signals are off. The controller status indicates ready. Drive status is valid. The controller interrupt is enabled, but not asserted. The WD1017 is in a status control loop, monitoring the microcontroller interrupt signal.

The host outputs the command parameters to the WD42C22 task file image registers and the operation command (seek, read, write, etc.) and the command attributes (long mode, retry, etc.).

The operation command output sets the command register, sets the controller busy flag, and the WD42C22 asserts the control interrupt. For write and format commands, the WD1017 initializes the data buffer pointers and asserts DRQ in the host status register. Completion of the data transfer asserts the WD1017 control interrupt. For read or non-data transfer commands, only the command output interrupt is generated.

The WD1017 examines the task file image registers for valid parameters and controls the drive's head positioning for seek and restore commands. For data transfer commands, the WD1017 performs any implied seek requirements and sends the command to the WD42C22 formatter section for execution.

Command execution proceeds with the WD42C22 providing data transfer control, error monitoring, and completion status. The WD10C22 controls read/write data control for data transfers to the drive. Multiple sector transfers with 2:1 interleave cause the WD42C22 and host to access the RAM data buffer simultaneously. Circuitry in the WD42C22 control the memory accesses.

The WD42C22 interrupts the WD1017 at the end of each sector operation. The WD1017 examines the command and status transfers and sends the sector status to the WD42C22 task file image registers. Controller status returns to not busy. The WD42C22 interrupts the host. For multiple sector operations, the host data transfer continues to interrupt the WD1017 until all sectors are received.

On final command completion, the WD1017 and WD42C22 return to idle. The host can examine final controller status, then issue a new command.

WINCHESTER COMMAND DESCRIPTIONS

Restore

The Restore command is used to move the read/write heads to the track 0 position. The controller issues step pulses to the drive until the TRACK 0 indicator from the drive is asserted. If TRACK 0 is not asserted within 2047 steps, the error bit in the status register is set and a track 0 error is posted in the error register. The implied seek step rate may be set up according to Table 12 by the restore command. The restore step rate is established by the SC signal from the drive; i.e., each step pulse is issued only after SC is asserted by the drive from the previous step. If the DRIVE READY is de-asserted or WRITE FAULT is asserted, this command terminates with the error bit set in the status register and the error register reports an aborted command.

Seek

This command moves the read/write heads to the cylinder specified in the task file cylinder high and low registers. The implied seek step rate is also set by this command. The lower order four bits of the command are used to select one of 16 available step rates. An interrupt is generated at the completion of the command. If the DRIVE READY signal is de-asserted or WRITE FAULT is asserted, this command is terminated with the error bit set in the status register and the error register reports an aborted command.

Read Sector

A number of sectors (1-256) can be read from the selected drive with this command. The sector count register in the task file determines the number of sectors to be transferred. A sector count of zero specifies a 256 sector transfer. Multiple sector reads may cross head and cylinder boundaries.

If the read command is issued prior to initializing a step rate, the default value of 6.5 msec is selected. If the read/write heads are not positioned over the target track, the controller performs an implied seek to the proper cylinder. The stepping rate used during the implied seek is the value specified during the previous seek or restore command.

The optional long bit (L set to 1 enables read long) informs the controller whether or not to include the four ECC bytes. These four ECC bytes are transferred as individual bytes, not words, as is the data field information. The DRQ in the status register must be valid before each byte is transferred.

With retries disabled, the WD1017's firmware aborts all error types except for data field ECC errors. For data field ECC errors, the WD1017 issues a compute ECC correction to the WD42C22. If a correctable error condition exists, the WD1017

performs the correction and reports a corrected data status for that sector to the host. Data errors up to five bits in length will be automatically corrected on normal read commands. With retries enabled, ECC correctable data errors are corrected after two consecutive matching ECC syndromes are detected. With retries disabled, immediate ECC correction is attempted. If the ECC data error is uncorrectable, the controller terminates the command with an error status and ECC error type.

With retries enabled, recoverable type errors (ID not found, data address mark (DAM) not found, and ECC errors are retried as follows:

	WD42C22	WD1017 firmware
ID not found		
Inital command	10	
Re-seek and re-start command	10	1
Total retries*	20	
DAM not found		
Initial command	1	
Re-start command		9
Total retries*	10	
ECC data error		
Initial command	1	
Matching syndrome search		8
Total retries*	9	

*Twenty total retries occur for ID not found because the WD42C22 automatically searches for the ID for ten index pulses. If unsuccessful, the WD1017 firmware reissues the command which attempts to find the ID field for another ten index pulses. For DAM errors and ECC data errors, the WD1017 reissues the command nine times (one for DAM, eight for ECC) since the WD42C22 attempts to recover DAM and ECC once per command.

The WD1017 terminates the command if a multiple error condition is encountered. For example, if an ID not found error occurs while in the DAM not found retry routine, the command terminates without further retry effort. Interrupts occur as each sector is ready to be read by the system. No interrupt is generated at the end of the command. If the DRIVE READY signal is de-asserted or WRITE FAULT is asserted, the command terminates with the error bit set in the status register and the error register reports an aborted command.

Write Sector

A number of sectors (1-256) can be written to the selected drive. The sector count register in the task file determines the number of sectors to be transferred. A sector count of zero specifies a 256 sector transfer. Multiple sector writes may cross head and cylinder boundaries.

If the write command is issued prior to initializing a step rate, the default value of 6.5 msec is selected. If the heads are not positioned at the cylinder specified in the cylinder high and low registers, the controller performs an implied seek. The step rate used is determined by the step rate field of the most recently executed restore or seek command.

The optional long bit (L set to 1 enables write long) informs the controller whether or not to append the host supplied ECC bytes. These four bytes are transferred as individual bytes, not words, as is data field information. The DRQ bit in the status register must be valid before each byte is transferred.

The optional retry bit (T set to 1 disables retries) disables or enables retries. For write commands, the ID not found retry algorithm is identical to the read command's algorithm. The other recoverable error types do not apply.

The controller interrupt is generated as the data for each sector is required to be transferred into the RAM buffer (except the first sector) and at the end of the command. The first sector may be writ-

ten to the buffer immediately after the command has been sent, and the DRQ bit is set. If the DRIVE READY signal is de-asserted or WRITE FAULT is asserted, this command terminates with the error bit set in the status register and the error register reports an aborted command.

Format Track

The track specified by the task file is formatted with ID and data fields according to the interleave table transferred to the buffer. The interleave table consists of two bytes per sector. The first byte is the bad sector mark. "00_{16}" represents a good sector. "80_{16}" represents a bad sector. The second byte contains the sector number in the ID field.

The data transfer must be 512 bytes even though the table may be only 34 bytes. The sector count register must be loaded with the number of sectors per track before each format track command. The format track command supports no error reporting. A bad block may be specified by replacing a 00 table entry with and 80_{16}. Command completion leaves all data fields initialized to zeroes. The completion interrupt is generated after each track has been formatted.

Read Verify

This command functions similarly to a normal read command except that data is not output to the host. One to 256 sectors may be verified at one time. The generated ECC bytes are compared with the recorded ECC bytes for data verification. ECC correctable data errors are corrected after two consecutive matching ECC syndromes are detected. A single interrupt is generated upon completion of the command or in the event of an error.

If the read verify command is issued prior to initializing a step rate, the default value of 6.5 msec is selected. Refer to the read command description for further information on the retry algorithm. The WRITE FAULT and DRIVE READY inputs are checked throughout the command's execution.

Diagnose

The diagnose command causes the controller to perform an on-board diagnostic and to report the result in the error register. An interrupt is performed upon completion of the command.

The diagnose command performs tests on the WD1017's ROM and RAM, the WD42C22 data paths, and the sector buffer. If any component fails, the appropriate error code is loaded into the error register. Error codes are as follows:

01_{16}	No error
02_{16}	WD1017-WD42C22 register access error (formatter section)
03_{16}	Buffer data error
04_{16}	WD1017-WD42C22 register access error (buffer management section)
05_{16}	WD1017 ROM checksum or WD1017 RAM data error
06_{16}-FF_{16}	Not used. Undefined.

In addition, the diagnose command sets the write pre-compensation task file register to 32. This causes write pre-compensation to begin at cylinder 128. (This is because the write pre-compensation register holds the desired value divided by four.) The sector count register is reset to one while the cylinder high, cylinder low, and SDH registers are all set to zero. The step rate defaults to 6.5 msec.

Set Parameters

This command sets up the drive parameters regarding the maximum number of heads and sectors per track. The controller uses these two parameters when performing multiple sector operations. The SDH task file register specifies the drive affected. The sector count and SDH registers must be set up before this command is issued. An interrupt is set at the completion of the command.

This command should be issued before any multiple sector operations are undertaken. By setting the SDH register for each of the two possible drives, this command allows the controller to support two drives with different characteristics.

FLOPPY COMMAND SEQUENCE DESCRIPTION

In the reset or idle state, the WD37C65 control signals are off. The WD37C65 status indicates ready. Floppy motor control signals are off. DMA control terms and diskette interrupt are disabled.

The host initializes the external DMA controller for read/write operations. The host clears the floppy controller with a reset. After the reset, the host enables the DMA and interrupt circuits. The host sets the operations control and rate registers. Finally the host outputs the required WD37C65 command phase register data sequence.

The WD37C65 executes the command, selects and controls the drive. The WD37C65 also initiates any required DMA transfer requests and updates the result phase data registers. The controller interrupts the host. The host verifies controller status and, if necessary, DMA status.

WD37C65 COMMAND SET

The WD1003V-MM2 supports all WD37C65 commands. Each command except seek, recalibrate, sense interrupt status, specify, sense drive status, and invalid performs a command, result, and execution phase. Seek and recalibrate use the command and execution phase only. Sense interrupt status, specify, sense drive status, and invalid perform the command and result phases only.

The data register is actually a register stack written to during a command phase and read from during the result phase. The data register stack is accessed at system I/O map address $3F5_{16}$ (375_{16} secondary).

Read Data, Read Deleted Data, and Read A Track

The host outputs the nine command phase bytes and the WD37C65 selects the drive, and loads the drive heads. The WD37C65 begins reading ID address marks and ID data fields to locate the selected sector. When the sector is found data is transferred via DMA to host memory. Multiple sector and multiple track operations are allowed. Completion of the command updates the result phase registers, interrupts the host and unloads the heads.

The read deleted data and read a track commands have the same command and result phase register requirements except the command opcode. The read deleted data transfers sectors which have the deleted data address mark. The read a track command transfers all sectors from the index mark through the end of track sector.

Read ID

A read identification field command transfers the first correct ID field data to the sector identification result registers and interrupts the host. Sector data is not transferred to system memory. It should be noted that the result register stack is the same as a normal read command but the command phase requires only the command and select register information.

Write Data, Write Deleted Data

The host outputs the nine command phase bytes and the WD37C65 selects the drive, loads the heads and searches the sector ID fields. When the cylinder number, head address, record, and number of sector fields match the command register data, the floppy controller transfers byte data to the drive. Command completion updates the result registers and interrupts the host. The write deleted data command is the same as a normal write except that a deleted data address mark is written at the beginning of the data field, replacing the normal address mark.

Format A Track

The selected track is formatted from index through the last track sector with address marks, ID fields, data fields, and field gaps for either the standard single or double density format. The ID field data (four bytes) is furnished by the host for each sector. The data field is filled with the data defined in the command stack register.

Scan Commands

Scan equal, scan low or equal, and scan high or equal compare a sector on a byte by byte basis between the drive information and host data. If the scan condition is satisfied the scan hit bit is set in status register 2. If the scan is not satisified, the scan not hit bit is set in status register 2.

Recalibrate

The heads of the selected drive are retracted to track 0. Track 0 flag is available as a separate signal from the selected drive and in the status register 3 byte.

Seek

The selected drive is stepped to the new cylinder position.

Specify

The specify command sets the head load and unload rates, the drive step rate, and the DMA transfer mode.

Sense Interrupt Status

Controller status register 0 and the current cylinder are available in the result registers following this command. The command clears the floppy interrupt level.

Sense Drive Status

The command returns selected drive status during the result phase.

INSTALLATION

This section briefly describes the installation of the controller board.

A minor incompatibility exists between the WD1003V-MM2) and the WD1003-WAH (or WD1003-WA2). If the drive contains more than eight heads, e.g. a 16 head drive, the WD1003-WAH numbers heads 8 through 15 as 0 through 7 in the media's ID fields. The WD1003V controllers number heads 8 through 15 as 8 through 15. To correct this problem, install a jumper on W1 pin 7-8 when using the WD1003V controller formatted with the WD1003-WAH (WD1003-WA2). This problem is not manifested in drives with less than eight heads.

CAUTION

Handle the controller board by the ends of the board. Some of the chips are static sensitive and damage may occur if the board is incorrectly handled.

1. Verify the controller jumper settings. Refer to Table 13 for further information. Figure 2 illustrates the controllers' jumper locations.

2. Verify termination on last drive. Verify proper setting of drive select switches. Consult the drive technical manual for proper drive termination and selection information.

3. Remove the blank expansion slot bracket. Put the bracket away and save it for possible future use. The screw will be used to hold the new controller board in place. It is best to locate the controller in the closest available expansion slot relative to the drive.

4. Attach the drive control cable connector to J5.

5. Attach the control cable to drive(s).

6. Attach drive 0 data cable connector to J4.

7. Attach data cable to drive 0.

8. Attach drive 1 data cable connector to J3.

9. Attach data cable to drive 1.

10. For WD1003V-MM2 users, attach the floppy cable connector to J1.

11. For WD1003V-MM2 users, attach cable to floppy drive(s).

12. Attach the Winchester activity cable connector to J6.

13. Check the cable connections carefully. Ensure that pin 1 on the board connectors mates with pin 1 on the cable connectors. Pin 1 on the cable connectors is usually on the color coded side.

14. Install the controller board into the expansion slot. Make sure that the board is seated properly by pressing down on both ends of the board. Secure the board with the bracket screw.

Software Installation

This section contains instructions for low level formatting the Winchester drives.

1. Insert your Advanced diagnostic diskette (or equivalent for AT compatibles).

2. Turn on the power.

3. Boot the diagnostic and select the setup option.

CAUTION

Avoid system damage by consulting your system technical reference manual to ensure that your Winchester drive type is supported by the host BIOS drive tables. Not all AT compatibles share the same drive tables as IBM.

4. Select proper drive type. Consult the technical reference manual for further information on these parameters.

CAUTION

Step 5 requires execution of low level format. Use of the IBM Advanced Diagnostic (or similar program for IBM compatibles) is necessary since these controllers contain no on-board Basic Input/Output System (BIOS) ROM. Furthermore, the low level format destroys all data on the drive. If the drive contains useful data, backup the drive before executing the low level format program.

5. Insert the Advanced Diagnostic diskette and execute the low level format.

6. Load and execute the FDISK and FORMAT programs.

TABLE 13. JUMPER SETTINGS

Jumper*	Pin number	Position	Description
W1	1-2	OFF	Winchester(s) in latched mode.
		ON	Winchester(s) in non-latched mode.
	3-4	OFF	Four byte ECC. ON reserved.
	5-6	OFF	Cache enabled.
		ON	Cache disabled.
	7-8	OFF	Drives with more than 8 heads **incompatible** with the WD1003-WAH (WD1003-WA2).
		ON	Drives with more than 8 heads **compatible** with the WD1003-WAH (WD1003-WA2).
W3	1-2	OFF	Primary Winchester I/O addresses
		ON	Secondary Winchester I/O addresses
W4	1-2	OFF	Primary floppy I/O addresses.
		ON	Secondary floppy I/O addresses. Not used.
W5	1-2	OFF	Single speed drives.**
		ON	Dual speed drives.**
W6	1-2	OFF	Bracket ground option not used.
		ON	Connects bracket to board ground.

*Not all jumper headers are installed. Modify jumpers only under the direction of a qualified individual.

**Do not combine single and dual speed drives in the same system.

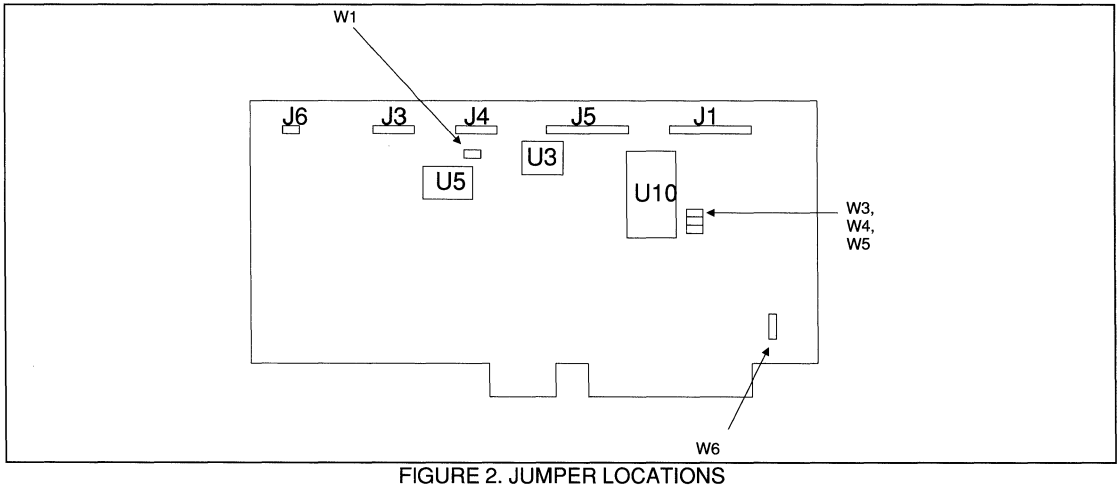

FIGURE 2. JUMPER LOCATIONS

GENERAL SPECIFICATIONS

Power

+5 V ± 5.0%, 0.6 A typical, 0.7 max

+12 V ± 10.0%, 0.02 A max

Environmental

Temperature	
Operating	0°C to 55°C (32°F to 131°F)
Non-operating	-40°C to 60°C (-40°F to 140°F)
Air flow	100 LFM minimum constant unidirectional, measured on a plane 1/4 inch equidistant from PCB surface
Humidity	
Operating	8% to 85% non-condensing
Non-operating	5% to 95% non-condensing
Altitude	
Operating	0 to 3000 meters (0 to 10000 feet)
Non-operating	0 to 5000 meters (0 to 16000 feet)
Shock and Vibration	
Shock	35G/20 msec square wave maximum
Vibration	1 G/0-600 Hz, dwell not to exceed 30 seconds at any resonance
PHYSICAL	
Length	21.1 centimeters (8.33 inches)
Width	8.78 centimeters (3.85 inches)
Height	1.27 centimeters (0.5 inches)

WINCHESTER CONTROLLER SPECIFICATIONS

Recording Specifications

Encoding method	Modified Frequency Modulation
Data rate	5 Mbps
Write precompensation	12 nsec early/late
Sector format	Soft sectored, 512 bytes/sector, 17 sectors/track
Drives supported	2 maximum
Heads supported	16 maximum
Tracks supported	32768 (2048 cylinders)
Hard error rate	<1 per 10^{12} bits read
Soft error rate	< 1 per 10^{10} bits read
Seek error rate	< 1 per 10^{06} seeks

WINCHESTER CONTROLLER SPECIFICATIONS (CONT'D.)

Data Separation

Maximum acquistion time	12 μsec at 5.0 Mbs
Jitter rejection	>35 db at 2.5 MHz
	>40 db when tracking
Bit error rate	$<10^{10}$
Bit jitter tolerance	± 34 nsec
W/C asymmetry margin	± 20 nsec
Kd-pump output	4/2 mA at pump pin
Ko-VCO gain	5% per volt

Error Correction Specifications

Method	Polynomial division
Degree	32
Forward polynomial	$X^{32} + X^{28} + X^{26} + X^{19} + X^{17} + X^{10} + X^{06} + X^{02} + 1$
Reciprocal polynomial	$X^{32} + X^{30} + X^{26} + X^{22} + X^{15} + X^{13} + X^{06} + X^{04} + 1$
Record length (r)	516 x 8
Correction span (b)	5 bits
Single burst detection span	19 bits,r,b
Double burst detection span	3 bits,r,b
Non-detection probability	$2.3(10^{10})$, r,b
Miscorrection probability	$1.57(10^{5})$, r, b

FLOPPY CONTROLLER SPECIFICATIONS

Recording Specifications

Recording method	MFM or FM
Data rates (5 1/4" drive)	500 kbps MFM, 250 kbps MFM, 300 kbps MFM, 125 kbpsFM
Data rates (3 1/2" drive)	500 kbps, 250 kbps
Write precompensation	125 nsec early/late standard
Sector format	Soft sectored, 512 bytes/sector, 15 sectors/track
Drives supported	2 maximum
Heads supported	2 maximum

FLOPPY CONTROLLER SPECIFICATIONS (CONT'D.)

Recording Specifications

Tracks supported	160 maximum
Hard error rate	<1 per 10^{12} bits read
Soft error rate	< 1 per 10^{09} bits read
Seek error rate	<1 per 10^{06} seeks

Error Detection and Correction Specifications

ID field CRC	X16 + X12 + X5 + 1
Data field CRC	X16 + X12 + X5 +1

Data Separator Specifications

Error rate window margin	60% minimum of window for 10^{09} error rate if actual data rate is within ±6%
Peak shift tolerance	50% minimum of window
Capture range	± 8% minimum
DCO frequency tracking	±6% of nominal steady state
Lock response time	4 bytes (00 hex data)

TIMING

Refer to the WD42C22 and WD37C65 data sheets for complete interface timing information.

Radio Frequency Interference

This Western Digital product has been verified to comply with limits for a Class B computing device pursuant to Subpart J of Part 15 of F.C.C. Rules.

This does not guarantee that interference will not occur in individual installations. Western Digital is not responsible for any television, radio, or other interference caused by unauthorized modifications of this product.

If interference problems do occur, please consult the system equipment owner's manual for suggestions. Some of these suggestions include relocation of the computer system away from the television or radio, or placing the AC power connection on a different circuit or outlet.

This digital apparatus does not exceed the Class B limits for radio noise emissions from digital apparatus set out in the Radio Interference Regulations of the Canadian Department of Communications.

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