Tape Dimension / Q-Bus CacheCoupler User's Manual

TAPE DIMENSION Q-BUS—CACHECOUPLER™
DEC™ COMPATIBLE ½" TAPE COUPLER

TDQ-III—Pertec Interface
TDQ-IV—STC or Telex Interface

PRODUCT DESCRIPTION

The Western Peripherals Tape Dimension Q-Bus III and IV (TDQ-III & TDQ-IV) CacheCouplers are part of Western Peripheral's family of cache buffer couplers emulating the DEC TS11 and TSV05 tape subsystem. The TDQ-III and TDQ-IV contain a 64k byte cache buffer which can store multiple records to ensure that streaming tape devices operate at maximum efficiency on DEC's Q-Bus family of computer systems. The TDQ-III and TDQ-IV provide the interface for an industry compatible formatted streaming tape drive at 1600, 3200 or 6250 bpi at speeds up to 125 ips, and also support start/stop tape drives at densities up to 6250 bpi and tape speeds of 200 ips.
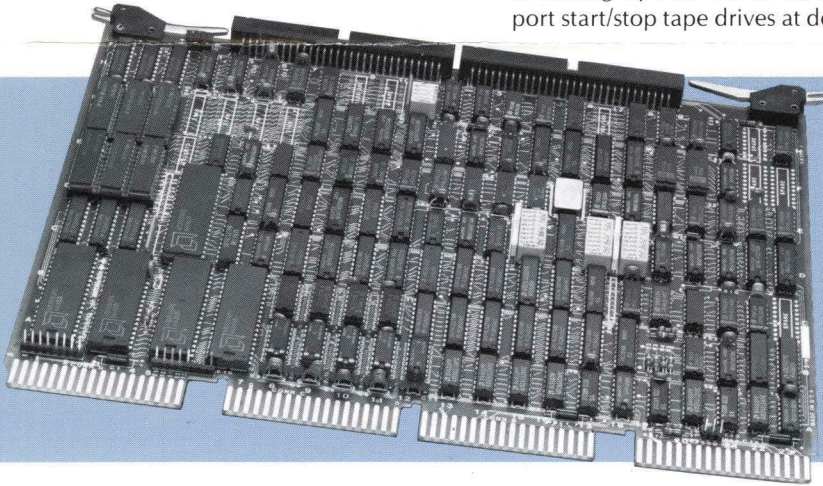
HARDWARE DESCRIPTION

The coupler is a single standard quad wide printed circuit board, containing a microprocessor plus all the interface and control electronics to emulate the DEC TS11 and TSV05 tape subsystems. The TDQ-III and TDQ-IV install directly into any available Q-Bus card slot in the computer or expansion chassis. Cables are available for the STC, Telex, or Pertec standard interfaces.

COMPUTER COMPATIBILITY

The TDQ-III and TDQ-IV are hardware compatible with the DEC LSI-11, Micro PDP-11, and Micro VAX families of Q-Bus computer systems.

EMULATION

Emulating the DEC TS11 and TSV05 tape subsystems, the TDQ-III and TDQ-IV use the standard TS11 and TSV05 registers and vector to simplify the system interface.

BUS LOADING

The coupler presents a one-unit load to the Q-Bus at all times.

HARDWARE CONFIGURATION

Single standard quad wide printed circuit board.
MOUNTING: Installs directly into a standard LSI-11 or Micro VAX Q-Bus slot.
CABLING: Two 50-conductor 3M-type ribbon cables (Industry Standard Pertec) or two 60-conductor 3M-type ribbon cables (STC/Telex). Telex drives require a special cable adapter board.

CACHE BUFFER FEATURE

The coupler's 64k byte cache buffer provides total immunity to "DATA LATE" conditions on heavily populated buses while maintaining the tape at streaming speeds.

SELF-TEST

Upon power up, the coupler utilizes the power of the microprocessor to exercise the hardware and insure reliable operation. LED's identify any functional segment in question. This self-test feature is standard and transparent to the operating system.

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TECHNICAL SPECIFICATIONS

DRIVE INTERFACE
TDQ-III Industry standard Pertec interface.
TDQ-IV STC or Telex Standard interfaces.

DEVICE ADDRESS
Each coupler and drive subsystem has its own address to maintain TS11 and TSV05 compatibility as defined by DEC. Up to four (4) subsystems per computer system.

1st Coupler	(MS0)	772520, 772522
2nd Coupler	(MS1)	772524, 772526
3rd Coupler	(MS2)	772530, 772532
4th Coupler	(MS3)	772534, 772536

(Alternate address sets: switch selectable)

INTERRUPT VECTOR
1st Subsystem = 224; others floating.
Alternate vector sets: switch selectable.

PRIORITY LEVEL
Normal Level 5; others available by jumper selection.

TRANSFER RATE:
1.5M byte/sec start/stop mode.
750k byte/sec streaming mode.

NUMBER OF DRIVES
One drive per coupler, couplers may be stacked in system for additional subsystems.

POWER REQUIREMENTS
+5 volts DC (5% tolerance) @ 6.0 amps.

SOFTWARE COMPATIBILITY
The coupler is transparent to the standard operating system tape drivers and compatible with operating systems supporting TS11 and TSV05 such as RSTS/E, RSX-11M, RSX-11M+, XXDP+ and RT-11.

MEDIA COMPATIBILITY
The coupler is designed to emulate DEC format and is compatible with pre-existing library or archival storage ½" 9-track 800/1600/6250 formats per ANSI specs plus 3200 bpi format.

6250 bpi per ANSI × 3.54-1976
1600 bpi per ANSI × 3.59-1973
800 bpi per ANSI × 3.22-1972

OPERATIONAL COMMAND SET (TS-11)

GET STATUS	Get Status
READ	Read next (forward)
	Read previous (reverse)
	Reread previous (space reverse, read forward)
	Reread next (space forward, read reverse)
WRITE CHARACTERISTICS	
	Load message buffer address and set device characteristics
WRITE	Write data
	Write data retry (space reverse, erase, write data)
POSITION	Space records forward
	Space records reverse
	Skip tape marks forward
	Skip tape marks reverse
	Rewind
FORMAT	Write tape mark
	Erase
	Write tape mark retry (space reverse, erase, write tape mark)
CONTROL	Message buffer release
	Rewind and unload
	Clean tape
	Rewind with Immediate Interrupt*
INITIALIZE	Drive initialize

STATUS SET
Upon executing a "Get Status" command, the controller returns a comprehensive status summary TSSR that when used with the five extended status registers defines in great detail any malfunction or problems encountered.

*Extended feature function only available with TSV05 emulation

RELIABILITY
Western Peripherals designed the TDQ-III and TDQ-IV with reliability in mind. You benefit from Western Peripherals' experience in fielding over 41,000 controller systems presently sustaining MTBF rates in excess of 50,000 hours. An advanced Quality Assurance program is in effect, providing a superior level of quality unmatched in the industry.

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Tape Dimension / Q-Bus CacheCoupler User's Manual

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PRODUCT SATISFACTION

Dear Customer:

    We are pleased with your continued interest in WESPERCORP
products. We have made every effort to design-in superior
performance and to manufacture the product to the highest
standards of quality and reliability. The next step is to
support the product to assure greatest value in your application.

    In the event of a problem or if you need any help with the
installation or advice on your particular application, please
call us at (714) 261-0606. (Or you may also contact us by Telex
at 4720629 WESPER.) We want to know that the shipment arrived
with all the required cables, manual, and other accessories. If
anything was missing or damaged, please let us know.

    Even if you have had no problems, we would still appreciate
hearing what you did and did not like about the product, sugges-
ted product improvements, and any other comments you feel
appropriate. A form is provided for your convenience at the back
of this manual.

    If you must return the product for any reason, please call
us first for a Return Authorization Number so we may serve you
better. Again, please let us know if we may be of further
assistance with your equipment requirements or if we may help in
any other way.

                              Sincerely,
                              WESPERCORP
                              Technical Support

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TAPE DIMENSION - Q-BUS

USER'S GUIDE

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PREFACE

This User's Manual provides information necessary for the installation and operation of the Western Peripherals TAPE DIMENSION / Q-BUS Tape Coupler, used with the DEC LSI-11, MICRO PDP-11 and MICRO VAX family of Q-Bus computer systems.

The manual is divided into the following sections:

Section I	General Description
Section II	Installation
Section III	Programming
Section IV	Computer Interface
Section V	Pertec-Compatible Formatter Interface
Section VI	STC Formatter Interface
Section VII	NRZI and PE Tape Formats
Section VIII	GCR Tape Format

*   *   *

Q-BUS is a trademark of Digital Equipment Corporation

RELATED DOCUMENTS

ANSI X3.22   American National Standard:
                          Recorded Magnetic Tape for Information
                          Interchange (800 CPI, NRZI)

ANSI X30.39-1973   American National Standard:
                          Recorded Magnetic Tape for Information
                          Interchange (1600 CPI, Phase Encoded)

ANSI X3.40-1973   American National Standard:
                          Unrecorded Magnetic Tape for Information
                          Interchange (9-track 200 and 800 CPI, NRZI;
                          and 1600 CPI, PE)

ANSI X3.54-1976   American National Standard:
                          Recorded Magnetic Tape for Information
                          Interchange (6250 CPI, GCR)

DEC   Q-Bus Protocol

DEC EK-OTS11-UG-001   TS-11 Tape Transport Subsystem User's Guide

DEC EK-TSV05-UG-001   TSV05 Tape Transport Subsystem User's Guide

PROBLEM: MICRO-VMS REPORTS ERRORS DURING MULTI-VOLUME COPY

POSSIBLE
SOLUTION: The OPCOM UTILITY must be running for a multi-
                  volume copy cimmand to execute properly.   In
                  addition, there must be a separate operator's
                  console to receive the messages from the OPCOM
                  Utility. VMS always designates OPA0 as the
                  operator's console.

                  If the OPCOM Utility is not running, start it by
                  typing:

                      @SYS$SYSTEM:STARTUP OPCOM

                  The next step is to issue the copy cimmand from
                  the user terminal. When the tape reaches the EOT
                  marker, the ancillary control processor will re-
                  wind the tape, take the tape offline, and send a
                  message to the operator's console, requesting the
                  next relative volume. The operator mounts a new
                  tape and issues the command:

                      REPLY /INITIALIZE_TAPE = #

                  where "#" is the number of the next relative
                  volume. At this point, the user's process will
                  continue the copy operation.

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SECTION I - GENERAL DESCRIPTION

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SECTION I

GENERAL DESCRIPTION

INTRODUCTION

This section describes the Western Peripherals TAPE DIMEN-
SION / Q-BUS CACHECOUPLER. This coupler is designed to emulate
Digital Equipment Corporation (DEC) Models TS-11 and TSV05 Tape
Subsystems.   This Group Code Recording tape controller/coupler,
contains 64K bytes of on-board data buffering to facilitate
start/stop functionality on streaming tape drives.   Contained on
a single standard-sized quad-wide printed circuit board, the Tape
Dimension / Q-BUS CACHECOUPLER is compatible with the DEC LSI-11,
MICRO PDP-11 and MICRO VAX families of computer systems and
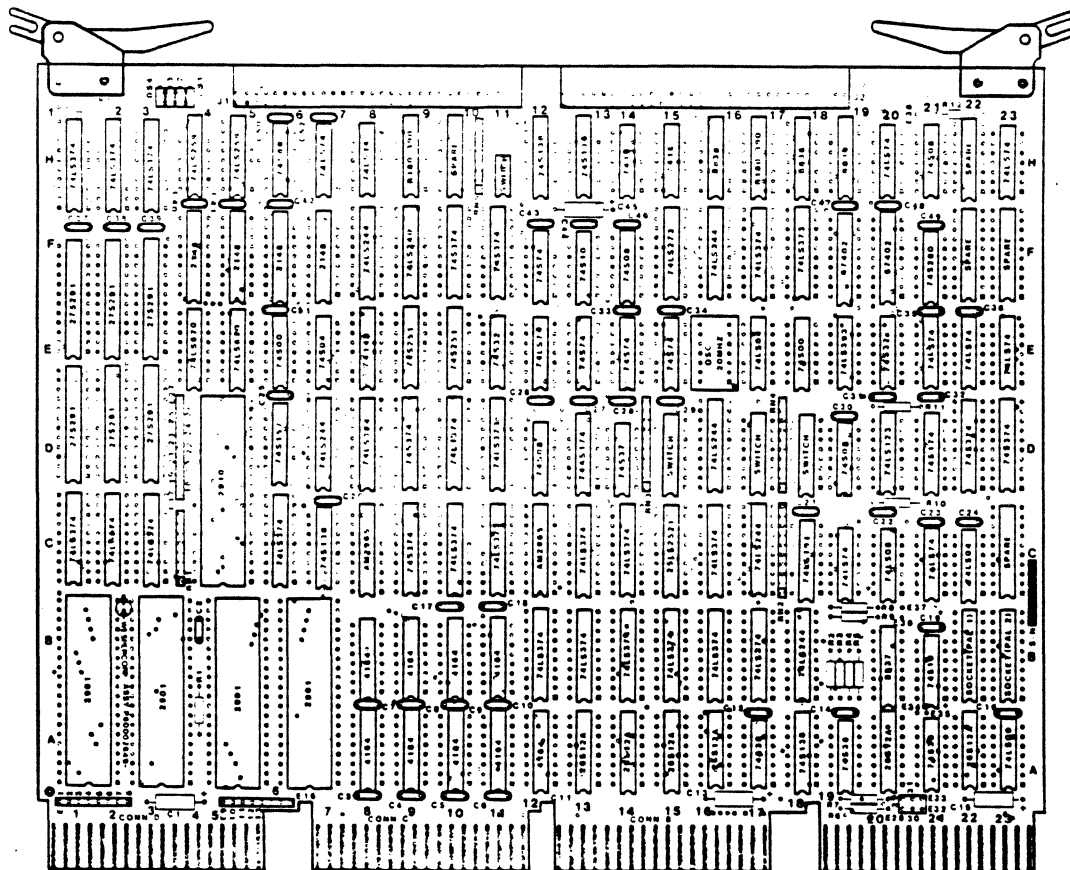interfaces with these processors via a standard Q-Bus slot.

FIGURE 1-1   TAPE DIMENSION / Q-BUS CACHECOUPLER

The Tape Dimension / Q-Bus provides the interface for a tape subsystem using industry-compatible formatted start/stop and streaming drives with dual density (NRZI/PE) or tri-density capability, which includes the 6250 bit per inch (bpi) Group Code Recording (GCR) format. Drives writing double-density 3200 bpi PE tape can also be used with the TDQ. The on-board data buffer allows the TDQ to emulate operation of the the DEC TS-11 and TSV05 start/stop tape subsystem, while fully supporting streaming tape drives. It also takes advantage of bus speeds without concern for data late conditions, even at fast data rates on a highly populated peripheral bus, while remaining transparent to standard DEC software.

EMULATION - SOFTWARE COMPATIBILITY

The Tape Dimension / Q-Bus is compatible with DEC operating systems that can support TS-11 and TSV05 tape subsystems. The coupler uses these standard TS-11 and TSV05 registers and vector to simplify the system interface, and since the coupler is fully buffered, it is immune to data late conditions, even when operating with high speed disk drives. Alternate TS-11 and TSV05 register addresses and vectors are also available via simple switch selection.

HARDWARE COMPATIBILITY

The Tape Dimension / Q-Bus interfaces the DEC LSI-11, MICRO PDP-11 or MICRO VAX system processor via the Q-Bus. The quad-wide TDQ Coupler board mounts inside the cabinet of the host computer and plugs directly into an available slot in its Q-Bus.

TAPE UNIT OPERATION AND INTERFACE

The Tape Dimension / Q-Bus supports the industry-standard (Pertec) tape drive interface as well as the special interfaces and other requirements to run GCR and other formats on STC tape drives.

Two different coupler boards support these interfaces: Model TDQ-IV handles STC tape drives while Model TDQ-III handles the industry-standard (Pertec) tape drive interface.

Standard 50-conductor "P1" and "P2" formatter interface cables are used to connect Pertec-compatible tape drives to the TDQ-III/PERTEC Coupler through two connectors at the top edge of the board. Two 60-conductor connectors are used on the TDQ-IV/STC for the STC interface. Various drive types are supported, including drives operating in the PE, NRZI and/or GCR format. Contact your Western Peripherals representative or the Western Peripherals Marketing department for a list of drives which are compatible with the TDQ.

CACHE BUFFER

In the Cache Mode, the 64 KByte data buffer contained on the TDQ board acts as a cache for data being transmitted between the host and the formatter in the tape drive. After fetching the first complete record, the coupler initiates a write operation on the drive and waits for the next command from the host. If the next command is also a Write, the coupler will fetch and store the next block of data in its buffer. The coupler will continue to accept data until the 64 KByte data buffer is full.

As data is written to tape, space becomes available in the buffer, and the coupler will accept more data. Should data transfer operations be suspended momentarily, data in the buffer will maintain the drive in the streaming mode, reducing the amount of repositioning activity required by the drive. The maximum transfer rate for streaming operations is 750 KBytes per second.

In the Buffered Mode, single records up to 64K bytes in length are stored for operations on start/stop drives. The maximum transfer rate for start/stop operations is 1.5 megabytes per second.

Because data is always transferred as complete blocks through the buffer, the coupler remains immune to data late conditions. This provides flexibility in assigning priorities on the bus without regard to bus grant late errors no matter how busy the host bus may be.

ERROR HANDLING

A switch-selectable feature allows the Tape Dimension / Q-Bus to handle Write errors on the coupler board. Any routine Write errors resulting from bad tape are corrected by automatic retries. No host computer intervention is required, saving valuable computer time.

TAPE FORMATS

Group Code Recording (GCR) is featured by the TDQ, allowing the user to take advantage of this modern high density recording technology. All data and control characters are recorded in groups and subgroups. Data groups contain error correcting characters for high data reliability. Each tape block contains preamble and postamble groups as well as ending data, control, and CRC groups. Resynchronization groups are also provided if the data block is longer than 1112 bytes.

The coupler also uses the standard nine track 1600 bit per inch (bpi) phase encoded and 800 bpi NRZI tape formats. In PE, each tape block contains a 41 character preamble of 40 tape characters with all-zero bits followed by one character of all-

one bits.   The preamble is followed by the data field which also contains an odd parity bit for each data character.   Following the data field is the postamble, which is the mirror-image of the preamble.   The TDQ coupler also supports drives writing double-density 3200 bpi PE tape.

Like PE, the data field of the NRZI format contains an odd parity bit for each data character.   Following the data field are the Cyclic Redundancy Check (CRC) and Longitudinal Redundancy Check (LRC) characters to ensure data integrity.

DATA BLOCK SIZE

Although the recommended maximum is 2K to 4K, the maximum data block size is only limited by the Byte/Record Count word to a full 64K byte block.   While the coupler can handle a single-byte tape block, the minimum recommended data block size can vary from system to system where the generated tapes will be used.

SPECIFICATIONS

COMPUTER INTERFACE – SOFTWARE

LSI-11 Interface Protocol –

DEC TS-11 and TSV05.

Emulation –

One DEC TS-11 or TSV05 subsystem

Q-Bus Register Addressing Assignments –

——   Standard = 772520_8, 772522_8 (TSDB/TSBA, TSSR)

Optional= 770000_8-777760_8 (TSDB/TSBA register, in modulo 40_8 increments, via option switches).

Q-Bus Interrupt Vector –

——   Standard = 224 (octal)

Optional = 0 – 377 (via option switches).

LSI-11 Bus Level –

Bus level 4, 5, 6, or 7; (level 5 is standard).

COMPUTER INTERFACE - HARDWARE

Q-Bus interface -

(fits in a standard Q-Bus slot).

DMA Addressing -

18 or 22 bits.

Buffering -

64 Kbytes single block (read and write)

Multi-block Cache buffering on write via sw. selection.

Bus Loading -

One standard Q-Bus load.

TAPE DRIVE INTERFACE

Formatter Interface (Start-Stop or Streaming operation) -

TDQ-III: Pertec-compatible NRZI/PE/GCR Formatter
(Pertec, CDC, Kennedy, Cipher, Ampex, etc.)

TDQ-IV: STC-compatible formatter.

Formatted Tape Drive Protocol -

Industry (Pertec) Standard for formatted drive.
STC drives have a different interface, described
later.)

Number Of Drives -

One tape drive per coupler module.

Tape Interface Cabling -

20 foot maximum length recommended

Two 50 cond. 3M-type ribbon cables (Pertec-compatible)

Two 60 conductor 3M-type ribbon cables (STC)

Recording Formats -

6250 BPI GCR per ANSI X3.54
3200 BPI double density Phase Encoded
1600 BPI Phase Encoded per ANSI X3.39
800 BPI NRZI per ANSI X3.22

Tape Transfer Rate (maximum) -

1.5 mb/sec. with single-block buffering.
Operation with Cache Buffer. - 0.75 mb/sec.

SELF-TEST FEATURE

Provides a full basic test of coupler's internal pro-
cessor and storage to assure reliable operation every time
power is applied to the system.

SIZE   One Standard LSI-11 quad-wide PC Board

POWER   +5 volts (5% tolerance) @ 5.9 amps power consumption
              (maximum).

ENVIRONMENT
Operating temperature   0 to 55 degrees Celsius
Storage temperature   -10 to 70 degrees Celsius
Relative humidity   10% to 90% (without condensation)

SECTION II - INSTALLATION

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LIST OF ILLUSTRATIONS

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SECTION II

INSTALLATION

INTRODUCTION

This section provides information for use in preparing and installing the TAPE DIMENSION / Q-BUS CACHECOUPLER in a DEC LSI-11, MICRO PDP-11 or MICRO VAX computer system. The TDQ consists of one standard quad-wide printed circuit board which plugs into a standard Q-Bus backplane in the computer mainframe or expansion chassis. One cable set is provided for interconnecting the coupler to the formatter of the STC or PERTEC-type industry standard tape drive. An optional diagnostic tape is available (P/N P68000280) and a User's Manual is included with each coupler.

Included in this section are instructions for unpacking and inspection, installation, setting switches and installing jumpers, and interfacing the coupler board with the computer and the tape drive formatter. The installation information in this section applies to standard TDQ assembly number P60002649. If your board has a different part number, contact Western Peripherals for information concerning the proper installation of your coupler board.

UNPACKING AND INSPECTION

On receipt of the TDQ coupler from the carrier, immediately inspect the shipping carton for evidence of damage. If the shipping carton is damaged or water-stained, request the the carrier's agent be present when the carton is opened; if the carrier's agent is not present at the time of opening, keep the carton and packing materials for subsequent agent inspection.

For repairs or replacement of WESPERCORP product damaged during shipment contact the Technical Support Center to obtain a Return Authorization Number and further instructions. A copy of the Purchase Order should be submitted to the carrier with any claim.

Carefully unpack the shipping carton and verify that the following items are included:

* TAPE DIMENSION / Q-BUS Coupler Printed circuit Assembly.
* TAPE DIMENSION / Q-BUS User's Manual
* Interconnect cables

After removal of the coupler board and associated components from the shipping container, visually inspect them for physical damage. Check off each item on the enclosed packing list. In case of damage, retain all packaging material and notify the carrier to make a report. Always ensure all minor parts and small items are accounted for before discarding any shipping material.

BOARD INSTALLATION CONSIDERATIONS

The coupler is a single board that can be installed in any Q-Bus cardcage/backplane slot. Determine the position in the computer where the coupler is to be installed. Remember that its physical location in the system determines its bus priority within the specified bus level. You may subsequently want to adjust the position of the devices on the bus to take advantage of the priority structure of the bus to minimize or eliminate bus grant late errors in the other various devices in the system. The TDQ remains immune to data late errors.

Refer to the appropriate tape drive manual to install the tape drive. The drive must be prepared and the processor checked out before the coupler can be expected to operate properly.

SWITCH/JUMPER CONFIGURATION SELECTIONS

A number of switches and jumpers are provided on the coupler board that allow the user to conveniently set the coupler for the system environment in which it is to operate. Figure 2-1 helps to identify the various installation features of the coupler board, and the locations of user-selectible switches and jumpers.

SELF-
TEST
DISPLAY
LEDs

FORMATTER
CONNECTOR
J1

UNIT
SELECT
SWITCH
11H

FORMATTER
CONNECTOR
J2

CSR
ADDRESS
SWITCH
15D

SWITCH
17D

VECTOR
SWITCH
18D

INTERRUPT
REQUEST
LEVEL
JUMPERS
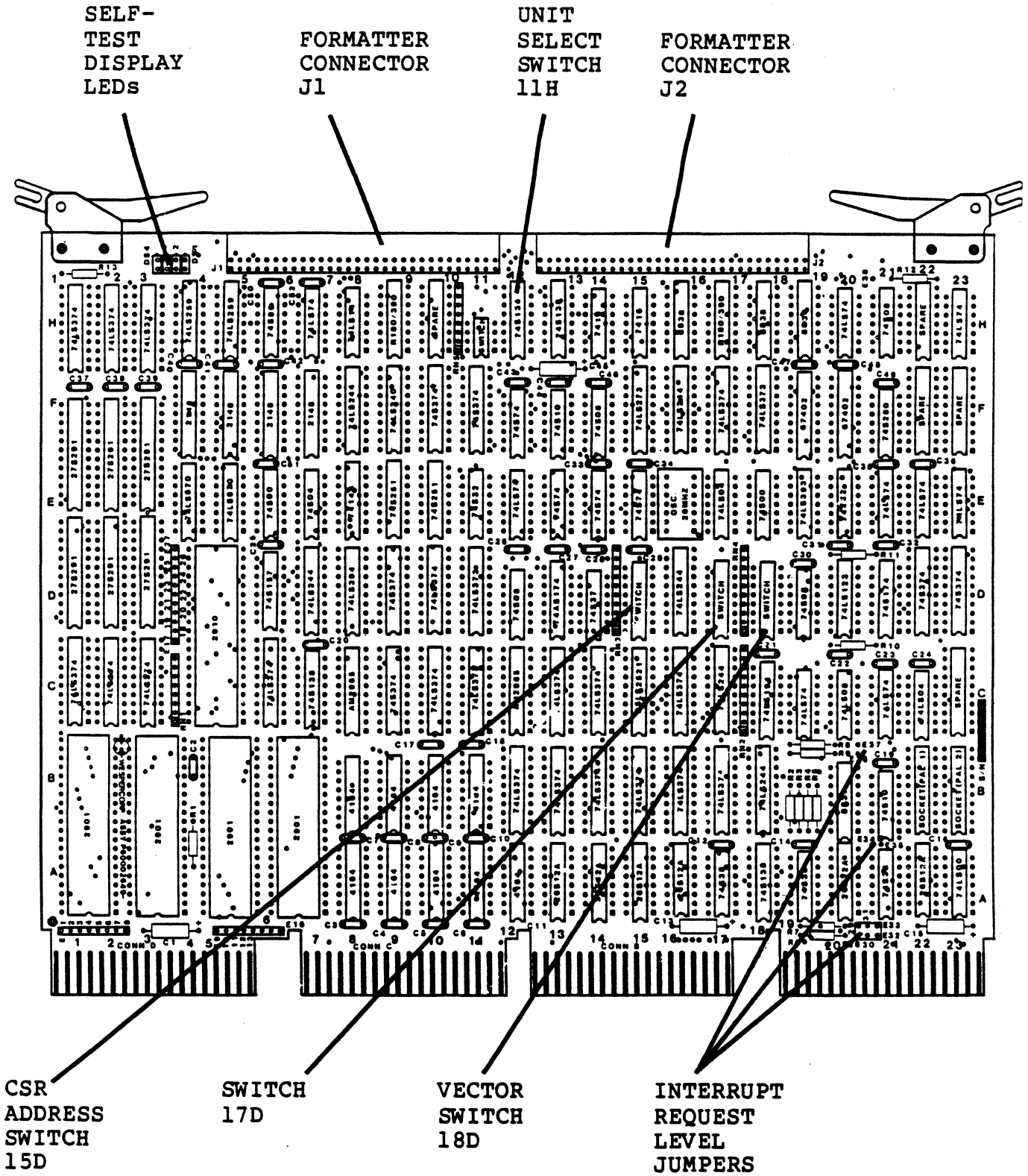
Figure 2-1   Tape Dimension / Q-Bus Board Illustration
Assembly Number P60002649 Layout

Q-Bus CSR Address Selection

Q-Bus address bits 2 through 11 for the coupler registers are switch selectable. These bits are controlled by switch toggles 1 through 8 of the switch module at location 15D and switch toggles 3 and 4 of the switch module at location 11H on the coupler board. The switch settings required to set up the factory-set standard Q-Bus address (772520) are illustrated in Table 2-1.

First, determine the bit values of the desired CSR Address like we did in the example. Then fill-in the spaces below with your CSR Address bit values and set the switches designated for each bit.

OCTAL	7		7			2			5			2			0-2		
BIT	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BINARY	1	1	1	1	1	1	0	1	0	1	0	1	0	1	0	0	X	0
	IGNORED VALUES					SELECTABLE VALUES										*		

* Register-determined Values

ADDRESS BIT NUMBER:	SWITCH PACK LOCATION:	SWITCH TOGGLE NUMBER:	DESIRED BIT (FILL-IN):	SETTING FOR A "ONE":	SETTING FOR A "ZERO":
12 and above - N/A (Ignored Values)					
11	15D	1	O	OFF	ON
10	15D	2	l	OFF	ON
09	15D	3	O	OFF	ON
08	15D	4	l	OFF	ON
07	15D	5	O	OFF	ON
06	15D	6	l	OFF	ON
05	15D	7	O	OFF	ON
04	15D	8	l	OFF	ON
03*	11H	4	O	ON	OFF
02*	11H	3	O	ON	OFF
01 & 00 - N/A (Register-determined Values)					

* SET 11H SWITCHES 1 & 2 OFF. FOR OLDER BOARDS, SEE NEXT PAGE.

Table 2-1   Standard Q-Bus Address Selection (15D & 11H)

NOTE:

Set switch pack 11H, switches 1 through 4 as shown below for the following older boards:

P60002649-011 Rev. A or B
P60002649-012 Rev. A or B
P60002649-021 Rev. A, B or C

CSR Bits 3 & 2		Switch Pack 11H Switch Position: 1	2	3	4	Registers	Address Offset	Typical Address
0	0	ON	OFF	OFF	OFF	TSDB/TSBA	0	772520
						TSSR	+ 2	772522
0	1	OFF	ON	OFF	OFF	TSDB/TSBA	+ 4	772524
						TSSR	+ 6	772526
1	0	OFF	OFF	ON	OFF	TSDB/TSBA	+10	772530
						TSSR	+12	772532
1	1	OFF	OFF	OFF	ON	TSDB/TSBA	+14	772534
						TSSR	+16	772536

Vector Address Selection

The interrupt vector address for the drive is selected by positioning the switch toggles of the switch module at location 18D on the coupler board. Switch toggles 1 through 6 control bits 07 through 02. (Bits 01 & 00 are always 0) Placing a switch toggle in the ON position selects a binary 0 while placing it in the OFF position selects a binary 1 in its respective bit position.

In addition, bit 08 can be selected by setting switch 8 of switch pack 17D. Placing the switch toggle in the ON position selects a binary 1 while placing it in the OFF position selects a binary 0.

The switch settings required to set up the standard drive interrupt vector address (224) are illustrated in Table 2-2.

OCTAL	2			2			4		
BINARY	0	1	0	0	1	0	1	0	0
SWITCH #	*	1	2	3	4	5	6	–	–
ON			X	X		X			
OFF		X			X		X		

* Bit 8 is set by switch 17D-8, See Table 2-6.

Table 2-2   Standard Interrupt Vector Selection (18D)

Interrupt Request Level Selection

By placement of jumpers in accordance with Table 2-3, any of Interrupt Levels 4, 5, 6 or 7 can be selected. Level 5 is standard. These jumpers are located near the bottom of the board near IC 21A and Board Connector A.

JUMPER	INTERRUPT REQUEST LEVEL				SIGNAL
CONNECTIONS	4	5	6	7	LINE
ASSERTION JUMPERS					
E30-E31	INSTALL	INSTALL	INSTALL	INSTALL	BIRQ4
E32-E33	REMOVE	INSTALL	REMOVE	REMOVE	BIRQ5
E33-E35	REMOVE	REMOVE	INSTALL	INSTALL	BIRQ6
E28-E29	REMOVE	REMOVE	REMOVE	INSTALL	BIRQ7
MONITOR JUMPERS					
E36-E30	REMOVE	REMOVE	REMOVE	REMOVE	BIRQ4
E36-E32	INSTALL	REMOVE	REMOVE	REMOVE	BIRQ5
E34-E35 *	INSTALL	INSTALL	REMOVE	REMOVE	BIRQ6
E36-E28	REMOVE	REMOVE	INSTALL	REMOVE	BIRQ7

* FACTORY INSTALLED IN ETCH

Table 2-3 Interrupt Request level Selection

Additional Feature Selection

The switch packs at locations 17D and 18D are used to configure the coupler for additional features. Table 2-4, below, lists the features and their appropriate switch settings.

Switch	Feature
18D-7 Off*	TS-11 emulation.
18D-7 ON	TSV05 emulation (Extended Features enabled).
18D-8 Off*	Single-block buffering enabled. The single-block mode optimizes operation with start/stop tape drives for the highest data transfer rates.
18D-8 ON	Cache buffer enabled. The Cache Buffer feature optimizes operation with streaming tape drives for highest overall throughput.
17D-1 ON	Write Retries Inhibited.
17D-1 Off	Write Retries ENABLED (ONLY if 18D-8 is ON).

NOTE: 17D-2 THRU 17D-4 ARE FOR TDQ - PERTEC VERSION ONLY.

Switch	Feature
17D-2 ON	Selects high-speed tape operation when Cache Feature is enabled (18D-8 ON). *√ 1400 .. Dual Space*
17D-2 OFF	No automatic high-speed tape operation selection.
17D-3 ON	For use with drives that do not latch the EOT signal, such as Pertec T9000, Cipher 920, etc.
17D-3 OFF	Normal operation. (NOTE: On/off function is backwards on older boards.)
17D-4 ON	Performs the Unload Command without issuing the Rewind Pulse (for use with drives such as Telex 9250).
17D-4 OFF	Normal operation.
17D-5, 6	DMA Burst Mode (see table below).

SWITCH 5	6	# WORDS PER CYCLE
Off	Off	1
Off	On	2
On	Off	4
On	On	8

Switch	Feature
17D-7	Not defined.
17D-8 ON	Interrupt Vector bit 8 true.
17D-8 OFF	Interrupt Vector bit 8 false.

* Recommended standard switch settings.

Table 2-4 Feature Selection

TAPE DIMENSION / Q-BVS BOARD INSTALLATION

The DMA Request and Interrupt Request lines are daisy-chained from one backplane connector to the next. To maintain continuity, unused A and C backplane connector slots are usually jumpered with a jumper card and/or a jumper wires between pins M2 and N2 and also between R2 and S2. Any OPEN slots between the tape coupler and the processor must have these jumpers installed. Western Peripherals supplies part number P76000223 for this purpose. Be sure to check for (by continuity test) and remove these jumpers from the backplane connector of the slot selected for coupler installation.

Place the tape coupler board into the selected card slot in the backplane, assuring that it seats properly to make a good connection. Also, check that the computer's Q-Bus is properly terminated.

INTERCONNECTIONS

Connections between the TDQ and the formatter are completed via two cables supplied with the coupler. When connecting the cables, be sure pin 1 (the triangle or arrow) on each plug is oriented to the triangle on the socket. You should check the manual of the tape drive to ensure proper connection at the drive's formatter.

For an STC formatter interface, the ribbon cables plug into the two 60-pin socket connectors, J1 and J2 on the controller board. The pin assignments for the two connectors J1 and J2 on the coupler are listed in Table 2-7. For an STC drive, the cable from J1 attaches to connector B4 on the drive and the cable from J2 attaches to connector A4 on the drive.

For the Pertec-compatible formatter interface, these cables plug into the two 50-pin socket connectors J1 and J2 on the coupler board. The pin assignments for these two connectors are listed in Tables 2-5 and 2-6.

Table 2-5 Pin Assignments for Pertec-compatible
Formatter Interface (Connector J1)

Signal Pin	Ground Pin	TDQ Mnemonic	Formatter Mnemonic
2	1	FBSY	FBY
4	2	LBYT	LWD
6	5	WRD03	W4
8	7	CMDCLK	GO
10	9	WRD07	W0
12	11	WRD06	W1
18	17	CMD1	REV
20	19	REW	REW
22	21	WRDP	WP
24	23	WRD00	W7
26	25	WRD04	W3
27	26	WRD01	W6
30	29	WRD05	W2
32	31	WRD02	W5
34	33	CMD2	WRT
36	35	DS0	LGP
38	37	DS1	EDIT
40	39	CMD4	ERASE
42	41	CMD3	WFM
46	45	TA0	TAD0
48	47	RD05	R2
50	49	RD04	R3

NOTE: All interface signals are low-true.

**Table 2-6   Pin Assignments for Pertec-compatible
Formatter Interface (Connector J2)**

Signal Pin	Ground Pin	TDQ Mnemonic	Formatter Mnemonic
1	5	DP	RP
2	5	RD07	R0
3	5	RD06	R1
4	5	LP	LDP
6	5	RD03	R4
8	7	RD00	R7
10	9	RD01	R6
12	11	ERR	HER
14	13	FM	FMK
16	15	IDB	IDENT
18	17	FEN	FEN
20	19	RD02	R5
22	21	EOT	EOT
24	23	ESC1	UNL
28	27	RDY	RDY
30	29	RW	RWD
32	31	FP	FPT
34	33	RSTR	RSTR
36	35	WSTR	WSTR
38	37	DBSY	DBY
40	39	ER1	SPD
42	41	CERR	CER
44	43	ONL	ONL
46	45	TA1	TAD1
48	47	TA2	TAD2
50	49	CMD0	HISP

NOTE: All interface signals are low-true.

Table 2-7   Pin Assignments for STC Interface

| SIGNAL PIN | GROUND PIN | CONNECTOR J1 | | CONNECTOR J2 | |
		TDQ MNEMONIC	STC MNEMONIC	TDQ MNEMONIC	STC MNEMONIC
A1	B1	–	–	TA0	AD0
A2	B2	ER0	ERMX-0	TA1	AD1
A3	B3	ER1	ERMX-1	CMD1	CMD0
A4	B4	ER2	ERMX-2	CMD2	CMD1
A5	B5	ER3	ERMX-3	CMD3	CMD2
A6	B6	ER4	ERMX-4	CMD4	CMD3
A7	B7	ER5	ERMX-5	DS0	DS0
A8	B8	ER6	ERMX-6	CMDCLK	START
A9	B9	ER7	ERMX-7	LBYT	STOP
A10	B10	FBSY	BUSY	DACK	TRAK
A11	B11	DREQ	TREQ	WRDP	DATA-P
A12	B12	–	–	WRD07	DATA-0
A13	B13	IDB	ID BURST	WRD06	DATA-1
A14	B14	OPI	OPINC	WRD05	DATA-2
A15	B15	DBSY	ENDATP	WRD04	DATA-3
A16	B16	FMT	TMS	WRD03	DATA-4
A17	B17	RJS	REJECT	WRD02	DATA-5
A18	B18	OVR	OVRNS	WRD01	DATA-6
A19	B19	EM	DATA CHK	WRD00	DATA-7
A20	B20	RPE	ROMPS	SRST	RESET
A21	B21	CERR	CRERR	ESC1	SLX1
A22	B22	BLK	BLOCK	ESC0	SLX0
A23	B23	DD0	NRZI	DS1	DS1
A24	B24	DPE	BUPER	ESC2	SLX2
A25	B25	ONL	ONLS	ERR	SSC
A26	B26	DD1	HDENS	OSC	OSC
A27	B27	RDY	RDYS	EOT	EOTS
A28	B28	–	–	LP	BOTS
A29	B29	CMD0	–	FP	FPTS
A30	B30	TA2	–	RW0	REWS

NOTE: All interface signals are low-true.

SELF-TEST

The TAPE DIMENSION / Q-BUS uses its internal self-test firmware to verify the coupler every time power is applied to the system. If no problem is detected, the LED indicators on the top edge of the board will be OFF. Table 2-8 lists other indications which define specific failures.

LED NUMBER:					
1	2	3	4	HEX	TEST RESULT
OFF	OFF	OFF	OFF	0	Self Test OK
OFF	OFF	OFF	ON	1	Sequencer Failure
OFF	OFF	ON	OFF	2	ALU Test Condition Failure
OFF	OFF	ON	ON	3	DBUS Test Condition Failure
OFF	ON	OFF	OFF	4	ALU Register Address Failure
OFF	ON	OFF	ON	5	Static Memory Failure
OFF	ON	ON	OFF	6	Dynamic RAM Address Failure
OFF	ON	ON	ON	7	FIFO Failure
ON	X	X	X		Dynamic Memory Failure (See Table 2-9 below)

Table 2-8   Self-Test Indications

LED NUMBER:					
1	2	3	4	HEX	LOCATION
ON	OFF	OFF	OFF	8	8A
ON	OFF	OFF	ON	9	9A
ON	OFF	ON	OFF	A	10A
ON	OFF	ON	ON	B	11A
ON	ON	OFF	OFF	C	8B
ON	ON	OFF	ON	D	9B
ON	ON	ON	OFF	E	10B
ON	ON	ON	ON	F	11B

Table 2-9   Failing Memory Chip Look-Up Table

CHECKOUT

With your tape system installed, you may now power-up the system and test the installation. To check the coupler installation and the connection of the cables to the drive, examine the Control/Status Register of the coupler. The Off-Line status bit (bit 6) should change when the drive is placed on-line.

You may then run the ZTSHC0 test program contained in the optional diagnostic tape available for the coupler. An operational test should also be performed, such as performing a tape back-up from disk.

MICRO VAX OPERATING PROCEDURES

Since the emulated DEC TS-11/TSV05 tape systems operate at one density only (PE), TDQ tape couplers cannot select tape density. Density is manually selected at the tape drive for the particular tape mounted.

A procedural problem can therefore occur, especially on Micro VAX computers operating under the VMS system. When writing a new blank tape or re-writing an existing tape using a different density, tape runaway will occur or the system will announce:

ERROR READING TAPE LABEL / NON-ANSI FORMAT

The simplest solution is to enter the following command (or create a command file, with the following format):

(For initializing in FILES-11 Format:)

INIT/OVERRIDE=(ACCESSABILITY,EXPIRATION,OWNER)

-- or --

(For backup or other non-FILES-11 Format):

MOUNT/FOREIGN/OVERRIDE=(ACCESSABILITY,EXPIRATION,OWNER)

System response: DEVICE?

MSA0 (or other device number, as required)

System response: LABEL?

Specify an appropriate label, as desired.

The operator requires VOLPRO privilege to issue these commands. This procedure will write the appropriate header onto the tape. Be sure that the tape drive is set to the proper density before issuing these commands.

XXDP+ DIAGNOSTICS

Boot the XXDP+ DIAGNOSTIC TAPE using the HARDWARE BOOT, (if available on the CPU) by hitting CONTROL/BOOT and typing MS<CR> after the prompt.

If no HARDWARE BOOT is available, MANUALLY enter the BOOTSTRAP ROUTINE shown belowW.

After the XXDP+ BOOTABLE TAPE has been BOOTED, load the DATA RELIABILITY PROGRAM bu typing:

.R ZTSHC0 <CR>

Then ANSWER THE QUESTIONS as follows:

```
DR> STA <CR>
(REMOVE PROGRAM TAPE AND LOAD A GOOD SCRATCH TAPE)
CHANGE HW (L) ? Y <CR>
# UNITS (D) ? 1    <CR>
UNIT 0
TSSR ADDRESS (0) 172522 <CR>
VECTOR (0) 224 ?    <CR>
CHANGE SW (L) ? N <CR>
UNIT 0 TS11 CODE LEVEL P377   (START OF DATA RELIABILITY)
```

At the end of the test pass, a SUMMARY of the test will be DISPLAYED on the screen.

BOOTSTRAP ROUTINE (TS11)

ADDRESS	DATA		COMMENTS
1000	012700	START:	ADRS OF TSBA INTO R0
1002	772520		*
1004	012701		ADRS OF TSSR INTO R1
1006	772522		*
1010	005011		INIT
1012	105711		IS 'SSR' SET?
1014	100376		WAIT IF NOT
1016	012710		ISSUE A SET CHARACTERISTICS CMD.
1020	001064		
1022	105711		IS 'SSR' SET?
1024	100376		WAIT IF NOT

BOOTSTRAP ROUTINE (Continued)

ADDRESS	DATA		COMMENTS
1026	012710		READ A RECORD
1030	001104		
1032	105711		IS 'SSR' SET?
1034	100376		WAIT IF NOT
1036	012710		READ A RECORD
1040	001104		
1042	105711		IS 'SSR' SET?
1044	100376		WAIT IF NOT
1046	005711		ERROR?
1050	100421		GO TO MESSAGE AND HALT
1052	012704		ADRS OF 'NUM' TO R4
1054	001102		
1056	005000		RESUME EXECUTION AT ZERO (IF NO ERRORS)
1060	005007		
1062	046523	NUM:	MS(ASCII)
1064	140004	PKT1:	SET CHARACTERISTICS PACKET
1066	001074		
1070	000000		
1072	000010		
1074	001116	PK:	MESSAGE
1076	000000		
1100	000016		
1102	000000		
1104	140001	PKT2:	READ DATA PACKET
1106	000000		
1110	000000		
1112	001000		
1114	000000	HLT:	
1116		MES:	OPTIONAL MESSAGE

* TSBA:=772520   TSSR:=772522

BOOT CODE (TSV05)

The Boot Code provided on the previous pages of the TDQ Manual works for TS11. For TSV05 functions, use the following code to boot RT11, RSX11, RSTS, and XXDP+ tapes. The Boot Code assumes that the hardware is functioning properly and that the tape contains the proper boot block. Recovery from errors is accomplished by retrying.

ADDRESS	CONTENTS	INSTR & OPERAND	COMMENT
007776	046523	LITERAL = "SM"	DEVICE ID "MS" BACKWARDS
010000	012701 172522	MOV TSDB+2,R1	R1=TSSR *START ADDRESS*
010004	010102	MOV R1,R2	R2=TSSR
010006	005000	CLR R0	SELECT UNIT 0
010010	105711	TSTB (R1)	WAIT FOR SSR BIT
010012	100376	BPL -1	
010014	010704	MOV PC,R4	R4=PC OF "SM"+20
010016	112737 000200 172523	MOVB #200,@#TSDB+3	WRITE HIGH BYTE TO SET TSSR BIT 15
010024	005242	INC -(R2)	WRITE INTO TSDB
010026	105711	TSTB (R1)	WAIT FOR SSR BIT
010030	100376	BPL -1	
010032	005711	TST (R1)	TEST FOR ERROR
010034	100761	BMI START	IF SC=1 RETRY
010036	005007	CLR PC	JUMP TO ZERO TO EXECUTE BOOT

STARTING ADDRESS IS 010000.

After executing the Boot Code, Registers R0-R4 will contain the following information:

```
RO          0  Unit Number 0
R1     172522  TSSR Address
R2     172520  TSBA/TSDB Address
R4     010016  PC of "SM" +20
```

SECTION III - PROGRAMMING

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SECTION III

PROGRAMMING

INTRODUCTION

This section contains machine-level programming reference information which describes the registers of the TAPE DIMENSION / Q-BUS. Also contained in this section is information on the operation of the coupler including register transfers, packet transfers, data transfers, and interrupts.

GENERAL

Communication between the LSI-11 program and the coupler involves program-addressable registers in the coupler and various classes of buffer space in LSI-11 main memory.

Two switch-selectable register addresses are assigned to the coupler. The first address is shared by the write-only TSDB register and the read-only TSBA register. The second address is assigned to the read/write TSSR register.

To implement any tape command, two packet buffers in LSI-11 memory must be assigned to that transport. These packet buffers include the Command Packet Buffer in which the LSI-11 program writes command information and the Message Buffer in which the coupler writes tape status information.

After writing a command packet in a command buffer, the LSI-11 program then writes the command buffer address in the TSDB register associated with the transport to which the command is addressed. This causes the coupler to read the command packet and, if possible, execute the command. Upon completion or rejection of the command, the coupler writes the appropriate transport status information in the TSSR register and in the message packet buffer. If the interrupt-enable bit is set in the command packet, it also interrupts the LSI-11 program to inform it of the ending status.

A separate command, the Set Characteristics command, points to a characteristics data buffer in LSI-11 main memory. The LSI-11 program writes the address and length of the message buffer to be assigned to the transport in the characteristics data buffer and also writes a characteristics mode byte. The write characteristics command causes the coupler to access the characteristics data buffer and obtain this information. Once a message

buffer address has been obtained, the message buffer continues to be assigned to the transport until initialization occurs. Since a message packet buffer is required to complete each command transaction, it follows that the first command to a transport following initialization must be a write Characteristics command.

The coupler uses non-processor direct memory accesses to obtain information from the command buffer and the characteristics data buffer and to write status information in the message buffer. During a tape read or write operation, the coupler uses non-processor direct memory transfers to access a tape data buffer in LSI-11 memory.

The TSBA register holds the 16 least significant bits of the LSI-11 memory address for each direct memory access. The two most significant bits of the LSI-11 memory address are held in the TSSR register.

The two least significant bits of each command packet buffer address are always 0s. Thus, the LSI-11 can specify the command packet buffer address by means of a single 16-bit transfer to the TSDB register. Bits 0 and 1 of the word transferred to the TSDB are the two most significant bits of the command packet buffer address. Bits 2 through 15 represent bits 2 through 15 of the command packet buffer address.

In addition to holding the two most significant bits of LSI-11 memory addresses, the TSSR register holds 13 bits of tape status. Although the TSSR register is defined as a read/write register, a DOUT operation addressed to the TSSR register has the effect of resetting five of the status bits held in it rather than transferring information to it. Such an operation also results in transport initialization during which a load sequence returns the tape to the BOT position if the transport is on-line.

PACKET BUFFER PROTOCOL

There is a specific protocol for accessing packet buffers and this protocol is defined in terms of buffer ownership. In general, ownership of both buffers belongs to the LSI-11 program at the time that a command transaction begins and passes to the coupler when the LSI-11 program writes the command packet buffer address in the TSDB register with the Acknowledge bit set in the Command Packet header word. Ownership of the two buffers then passes back to the LSI-11 program after the command has been completed when the coupler updates status and (if the Interrupt-Enable bit in the command packet is set) interrupts the LSI-11 program.

Since only the current owner is allowed to access a buffer, the coupler cannot report a change of status occurring during an idle period after it has returned ownership to the LSI-11 program. If a change between on-line and off-line status occurs when the coupler does not own the message buffer, it waits until

the next command is received. This gives it the message buffer
ownership required to update the message buffer so as to reflect
the change in status. In this case, it does not accept ownership
of the command buffer. If the attention-interrupt bit was set in
the characteristics mode byte obtained during the most recent
write-characteristics command transaction, then an attention
interrupt occurs following the status update. This interrupt is
independent of the state of the interrupt-enable bit of the
command which returns message buffer ownership to the coupler
allowing the status update.

Because the coupler has not accepted command buffer owner-
ship, the transaction (which would normally have resulted in the
processing of a command) in this case has resulted only in the
reporting of a change in on-line/off-line status. If the command
is still appropriate after this status change, the LSI-11 must
restart the transaction by writing the command buffer address in
the TSDB register in order to obtain command execution.

There is a message-buffer-release command whose only purpose
is to leave ownership of the message buffer to the coupler so
that a subsequent change of on-line/off-line status can be
reported immediately under transport-idle conditions. The
coupler updates the TSSR but not the message buffer during the
message-buffer-release command transaction. If the release-
interrupt-enable bit was set in the characteristics mode byte
obtained during the most recent write-characteristics command
transaction, then an interrupt is generated at the end of the
message-buffer-release command transaction. This occurs indepen-
dently of the state of the interrupt-enable bit of the message-
buffer-release command.

If a change of on-line/off-line status occurs following the
execution of the message-buffer-release command, then the message
buffer is updated immediately to report this change of status.
This update returns ownership of the message buffer to the LSI-11
program. If the attention-interrupt-enable bit was set in the
characteristics mode byte obtained during the most recent write-
characteristics command transaction, then an interrupt is genera-
ted at the time of the message buffer update. (This interrupt is
also independent of the state of the interrupt-enable bit of the
message-buffer-release command.)

LSI-11 PROGRAM-CONTROLLED INPUT/OUTPUT OPERATIONS

Two consecutive word addresses are assigned to the transport interfacing with the coupler. The address assignments are established by setting toggle switches on the coupler board. Standard addresses are as follows:

Unit #	Switch Pack 11H Switch Position: 1	2	3	4	Registers	Address Offset	Typical Address
0 (1)	ON	OFF	OFF	OFF	TSDB/TSBA	0	772520
					TSSR	+ 2	772522
1 (2)	OFF	ON	OFF	OFF	TSDB/TSBA	+ 4	772524
					TSSR	+ 6	772526
2 (3)	OFF	OFF	ON	OFF	TSDB/TSBA	+10	772530
					TSSR	+12	772532
3 (4)	OFF	OFF	OFF	ON	TSDB/TSBA	+14	772534
					TSSR	+16	772536

Table 3-1 summarizes the LSI-11 program-controlled input and output transfer operations associated with each register.

The format of the TSDB and TSBA register is defined in the description of the input and output operations. The format of the TSSR is summarized in Table 3-2.

Table 3-1
LSI-11 Program-Controlled Input/Output Operations

Transfer Class and Register	Description
DOUT, TSDB	Sixteen bits of command buffer address information from Q-Bus are accepted by the coupler. Bits 15 through 02 from Q-Bus are stored in corresponding bit positions of TSBA and bits 01 and 00 from Q-Bus (MSBs of command buffer address) are stored in bit positions 09 and 08 of TSSR. SSR bit in TSSR is reset. Coupler fetches command information from buffer and processes command without further program intervention if the ACK bit is set.
DOUT, TSDB, Upper Byte	Upper byte from Q-Bus is loaded into both bytes of TSBA and bits 09 and 08 from Q-Bus are loaded into corresponding bit positions in TSSR. Used to test integrity of coupler Q-Bus addressing function for transport n. After this operation, DOUT to TSSR must be performed to provide necessary initialization before command for transport n can be accepted.
DOUT, TSDB, Lower Byte	Lower byte from Q-Bus is loaded into lower byte of TSBA and lower byte of TSSR. Used for diagnostic purposes. After this operation, DOUT to TSSR must be performed to provide necessary initialization before command for transport n can be accepted.
DIN, TSBA	Sixteen least significant bits of current Q-Bus address pointer for transport n are placed on Q-Bus.
DOUT – word or byte, TSSR	SPE, UPE, RMR, NXM, and SSR bits of TSSR are reset. Any transport n operation currently in progress is aborted. If transport n is on-line, a rewind-to-loadpoint operation is executed. SSR bit of TSSR is then set to indicate that transport n is ready to accept a command.
DIN TSSR	Contents of TSSR are placed on Q-Bus.

Table 3-2   TSSR Format

Bit(s)	Mnemonic	Meaning When Set
15	SC	A special condition was detected during execution of last command. More information is contained in the termination class code (bits 04-01)
14	UPE	Q-Bus parity error
13	SPE	Not used by the coupler. Always 0.
12	RMR	Register modification refused. The LSI-11 program has loaded a command packet address into the TSDB when SSR (bit 07) is reset. This can occur if the last command was a message buffer release command and the coupler is updating the message buffer to report a change in on-line/off-line status at the time that the LSI-11 program loads the TSDB.
11	NXM	The coupler has attempted to access a non-existent memory location. The attempted access may involve a command, message, or data buffer.
10	NBA	The coupler needs a message buffer address. A write characteristics command has not been executed since the last TSSR initialization.
09, 08	A17, A16	Bits 17 and 16 of the Q-Bus address for non-processor direct memory access
07	SSR	The transport is not busy and another command addressed to it can be accepted.
06	OFL	The transport is off line.
05, 04	FC1, FC0	Fatal termination class code. Not supported.
03-01	TC2-TC0	Termination class code. See Table 3-3.
00		Not used.

Table 3-3 Termination Class Codes

Code Value

TC2,1,0	Class	Description
0 0 0	Normal	No special condition detected.
0 0 1	Attention	Transport has gone off line or come on line.
0 1 0	Tape Status Alert	Tape status having program significance detected. Further information in TMK, RLS, RLL, EOT, or BOT bit of XSTAT0 word of message packet.
0 1 1	Function Reject	Command has been rejected. Further information in VCK, BOT, WLE, LLC, or ILA bit of XSTAT0 word of message packet or in OFL bit of TSSR.
1 0 0	Recoverable error, tape moved	An uncorrected error has been detected, and tape has moved one record position. Recommended procedure is to log error and issue retry command.
1 0 1	Recoverable error, tape not moved	Not used by the coupler.
1 1 0	Unrecoverable error	Tape position has been lost. No valid recovery procedure is available.
1 1 1	Fatal error	Not used by the coupler.

COMMAND PACKET

Figure 3-1 illustrates command packet formats. Every packet contains a command packet header word. For some commands, additional information is required. Packets for commands which require access to a data buffer in main memory have two address words and a count word. The first address word contains the 16 least significant bits of the address. The second address contains the two most significant address bits, right justified. The count word specifies the data buffer length in positive byte count format. Packets for position commands contain a count word which specifies the number of records or file marks to be spaced over. For other commands, the header word contains all the required information.

Table 3-4 summarizes the information contained in the command packet header word. Two fields of the header word, the command mode field and the command code field, specify the operation to be performed. The decoding of these fields is summarized in Table 3-5.

HEADER WORD															
A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00	*
0	0	0	0	0	0	0	0	0	0	0	0	0	0	A17	A16	*
COUNT WORD															

* Address Words

A. Read, Write, Write Characteristics Command Packet Format

HEADER WORD
COUNT WORD

B. Position Command Packet Format

HEADER WORD
NOT USED

C. Control or Format Command Packet Format

Figure 3-1   Command Packet Formats

Table 3-4   Command Packet Header Word Format

Bit(s)	Mnemonic/ Name	Meaning When Set
15	ACK	Indicates the LSI-11 program has read message buffer. Is normally set for all commands except those occurring when the coupler owns message buffer due to execution of a message-buffer-release command.
14-12	Device- Depend. Field	(Individual bits described below)
14	CVC	Clears volume check bit of XSTAT0 word.
13	OPP	Alters read retry commands so that the read occurs in the opposite direction (Reread previous record is executed by reading in reverse and then spacing forward. Reread next record is executed by reading forward and then back-spacing.)
12	SWB	When this bit is reset, the order of data buffer byte addresses is the same as the order in which the characters appear on tape with the character associated with the lowest byte address being closest to the BOT. Setting this bit swaps the positions of the two bytes of each word so that the upper byte appears closer to the BOT on the tape. (See paragraph: "TAPE DATA BUFFERS")
11-8	Command Mode	In conjunction with command code (bits 4-0) these bits specify the operation to be performed as summarized in Table 3-5.
7-5	Packet Format:	(Individual bits described below)
7	IE	Interrupt enable
6,5	-	These bits always have value 00, speci- fying one word header.
4-0	Command Code	In conjunction with command note bits (11-8), these bits specify the operation to be performed as summarized in Table 3-5.

Table 3-5 Command Summary

Command Code		Command Mode	
Value	Command	Value	Operation
00001	Read	0000	Read one record forward.
		0001	Read one record reverse.
		0010	Reread previous record (backspace over record and then read forward).
		0011	Reread next record (Space forward one record and then read reverse).
00100	Write characteristics	0000	Get message buffer address and characteristics byte from characteristics data buffer.
00101	Write	0000	Write one data record.
		0010	Retry to write one data record (Backspace over record and the erase and write record).
00110	Write Subsystem Memory	0000	Not supported.
01000	Position	0000	Space forward n records, where n is specified by count word.
		0001	Space reverse n records, where n is specified by count word.
		0010	Skip n tape marks forward, where n is specified by count word.
		0011	Space reverse n tape marks, where n is specified by count word.
		0100	Rewind tape to loadpoint.
01001	Format	0000	Write tape mark.
		0001	Erase forward 3 inches of tape.
		0010	Retry to write tape mark (Space reverse, erase, and write tape mark).
01010	Control	0000	This constitutes a message buffer release command. It leaves ownership of the message buffer with the coupler so as to allow immediate reporting of transport on-line/off-line status change.
		0001	Rewind tape completely onto supply reel (unload).
		0010	Clean tape (not supported).
01111	Get status immediate	0000	Update message buffer.

CHARACTERISTICS DATA BUFFER

The information contained in the characteristics data buffer includes the message buffer address and the characteristics mode byte. The location and length of the characteristics data buffer are specified in the address and count words of the write characteristics command packet. The coupler uses non-processor direct memory accesses to obtain the information from the characteristics data buffer.

Figure 3-2 illustrates the characteristics data buffer format. Table 3-6 summarizes the information contained in the characteristics mode byte.

A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00	*
0	0	0	0	0	0	0	0	0	0	0	0	0	0	A17	A16	*
0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	**

CHARACTERISTICS MODE BYTE

    * Message Buffer Address
    ** Message Buffer Length

Figure 3-2   Characteristics Data Buffer

TAPE DATA BUFFERS

Data to be written on tape or data read from tape is stored in a data buffer in LSI-11 main memory. This buffer is specified by the address and count words of the write or read command packet. Data transfers between the data buffer and the coupler are implemented by means of non-processor direct memory accesses.

Figure 3-3A illustrates the standard relationship between the order in which characters are stored in the data buffer in main memory and the order in which they appear on tape. This relationship is independent of the direction in which characters are being transferred and, for tape read operations, is independent of the direction in which the tape is being read.

If swap-byte bit SWB is set in the header of the command packet, then character positions within each word are reversed with respect to the standard relationship. To illustrate this in terms of the data buffer address (B) two cases must be shown. Figure 3-3B, illustrates the case of an even buffer address, BE.

For this case, character 0 (the character that appears closest to the BOT) is stored at $(B_E + 1)$ and character 1 is stored at B_E. Character 2 is stored at $(B_E + 3)$ and character 3 is stored at $(B_E + 2)$. And so on.

For an odd buffer address, B_O, character 0 is stored at $B_O - 1$); character 1 is stored at $(B_O + 2)$; character 2 is stored at $(B_O + 1)$, and so on. This case is illustrated in Figure 3-3C.

Table 3-6   Characteristics Mode Byte Format

Bit	Mnemonic	Meaning
07	ESS	Instructs the tape transport to stop on a double tape mark during a Skip Tape Marks Position Command.
06	ENB	If the tape is at BOT and if ESS is set, instructs the tape transport to stop on a tape mark if it is the first tape block record encountered during a Skip Tape Marks Position Command. (LET status will be indicated.)
05	EAI	Enables ATTN interrupts when reporting on-line/off-line status change provided that interrupt-enable bit is set in command which passes message buffer ownership to coupler, allowing status update to occur.
04	ERI	Enables interrupt in response to message buffer release command if IE is set in command packet header word.

	B	B+1	B+2	B+3	B+4	B+5	B+6	B+7	DATA
	0	1	2	3	4	5	6	7	BUFFER
BOT <--	0	1	2	3	4	5	6	7	TAPE

A. Standard (DEC) Relationship (SWB=0)

	B_E	B_E+1	B_E+2	B_E+3	B_E+4	B_E+5	B_E+6	B_E+7	DATA
	1	0	3	2	5	4	7	6	BUFFER
BOT <--	0	1	2	3	4	5	6	7	TAPE

B. Swapped Bytes (IBM), Even Buffer Address (SWB=1)

	B_O-1	B_O	B_O+1	B_O+2	B_O+3	B_O+4	B_O+5	B_O+6	B_O+7	B_O+8	DATA
	0	-	2	1	4	3	6	5	-	7	BUFFER
BOT <--	0	1	2	3	4	5	6	7			TAPE

C. Swapped Bytes (IBM), Odd Buffer Address (SWB=1)

NOTE: 0 - 7 denote particular characters

Figure 3-3   Order of Characters

MESSAGE PACKET

Figure 3-4 illustrates the overall format of the message packet. The first word is the header word. The information in this word is summarized in Table 3-7. The second word is the data length word which always contains the value 10 (decimal) corresponding to the number of data bytes in the packet. The remaining words are extended status words RBPCR, XSTAT0, XSTAT1, XSTAT2, and XSTAT3. The information contained in these words is summarized in Table 3-8.

Figure 3-4   Message Packet Format

PACKET HEADER WORD
LENGTH WORD
RBPCR
XSTAT0
XSTAT1
XSTAT2
XSTAT3

Table 3-7   Message Packet Header Word Format

Bit(s)	Mnemonic/ Name	Meaning
15	ACK	Indicates that coupler has accessed the command packet buffer. In an ATTN message reporting an on-line status change, this bit is false.
14-12	-	Not used
11-8	Class Code Field	In a FAIL or ATTN message (see bits 4-0), this code defines the type of event. The coupler ATTN messages are always type 0000 (indicating a change of on-line/off-line status). For a FAIL message, 0010 indicates a write-lock error or non-executible function and 0001 indicates other types of failures.
7-5	Packet Format Field	Always 000 indicating one word header.

Bit(s)	Mnemonic/ Name	Code Value	Name	Associated Termination Class Codes in TSSR
4-0	Message Code	10000	End	0, 2
		10001	Fail	3
		10010	Error	4, 5, 6
		10011	Attention	1

Table 3-8
Extended Status Word Formats

Bit(s)   Mnemonic   Meaning

RBPCR REGISTER

15-0   C15-C0   Residual byte, record, or tape mark count for
                       Read, Space Record, or Skip Tape Mark
                       commands, respectively.

XSTAT0

15   TMK   Tape mark detected during Read, Space, Skip,
                       or Write Tape Mark command. Causes termina-
                       tion class code 2 if set during a Read or
                       Space command.

14   RLS   For a Read operation, indicates that record
                       length was less than byte count. For a Space
                       Record operation, indicates that tape mark
                       was encountered before specified number of
                       records were spaced over. For Skip Tape
                       Mark operation, indicates BOT was encountered
                       before specified number of tape marks were
                       spaced over. Causes termination class code
                       2.

13   LET   Logical End of Tape - Indicates a stop has
                       occurred during a Skip Tape Marks Position
                       command as a result of ESS or ENB bit of
                       Characteristics Mode Byte being set and
                       double tape mark or tape mark immediately
                       following BOT being encountered.

12   RLL   Record read contained more bytes than speci-
                       fied by byte count. Causes termination class
                       code 2.

11   WLE   Indicates attempt to write on or erase write
                       protected tape. Causes termination class
                       code 3: write-enable ring not installed.
                       Causes termination class code 6 if WRITE LOCK
                       switch is activated during operation.

10   NEF   The command could not be executed. Causes
                       termination class code 3. (A command re-
                       quiring reverse motion cannot be executed if
                       the tape is at the BOT position. A write
                       command cannot be executed if the write-
                       enable ring is not installed on the tape. A
                       motion command cannot be executed if VCK (bit
                       4) is set and the CVC bit in the command
                       header is not set or if the unit is off-
                       line.)

Table 3-8   (Continued)
Extended Status Word Formats

Bit(s)	Mnemonic	Meaning
09	ILC	Command code/command mode value does not correspond to operation supported by transport. Causes termination class code 3.
07	MOT	Capstan is moving.
06	ONL	Tape transport is On-Line. When tape switches on-line, termination class code 1 is presented with ATTN interrupt. If motion command is received when tape is off-line, termination class code 3 is presented.
05	IE	Interrupt Enable bit from most recent command.
04	VCK	Volume Check bit set after initialization and when transport switches between on-line and off-line status. Reset in response to CVC bit in command header. Causes termination class code 3 if it remains set.
03	PED	Indicates transport is capable of phase-encoded mode operation only.
02	WLK	Mounted tape reel does not have write-enable ring installed.
01	BOT	Beginning-of-tape reflective strip is being detected. Causes termination class code 3 if set when command requiring reverse motion is received. Causes termination class code 2 if set during command execution.
00	EOT	Indicates tape position is beyond reflective end-of-tape marker. Causes termination class code 2 if set during a write operation.

XSTAT1

Bit(s)	Mnemonic	Meaning
15	DLT	Indicates that data transfers between coupler and LSI-11 memory have not been accomplished at rate required by tape read or write rate. Causes termination class code 4.
14	-	Not assigned.
13	COR	Indicates that a correctible error has been encountered during a read command.
12	CRS	Not supported.

Table 3-8   (Continued)
Extended Status Word Formats

Bit(s)	Mnemonic	Meaning
11	TIG	Not supported.
10	DBF	Not supported.
09	SCK	Not supported.
08	-	Not used.
07	IPR	Not supported.
06	SYN	Not supported.
05	IPO	Not supported.
04	IED	Not supported.
03	POS	Not supported.
02	POL	Not supported.
01	UNC	Indicates that an uncorrectable parity error has occurred during a read operation or that any parity error has occurred during a write operation. Causes termination class code 4.
00	MTE	Indicates that a multitrack dropout has been detected.

XSTAT2

Bit(s)	Mnemonic	Meaning
15	OPM	Indicates tape has moved in response to most recent command.
14	SIP	Not supported.
13	BPE	Not supported.
12	CAF	Not supported.
11	-	Not used.
10	WCF	Not supported.
09	-	Not used.
08	DTP	Not supported.
07-00	DT7-DT0	Not supported.

Table 3-8   (Continued)
Extended Status Word Formats

Bit(s)   Mnemonic   Meaning

XSTAT3

15-08   -   Not supported.

07   LMX   Not supported.

06   OPI   Indicates a Read, Space or Skip operation
                      moved 25 feet of tape without encountering
                      data.   Also set in a Write operation if the
                      read head doesn't encounter data after moving
                      four feet of tape.

05   REV   Indicates that reverse motion was required to
                      execute most recent motion command.   (This
                      includes all retry commands.)

04   CRF   Not supported.

03   DCK   Indicates that an identification burst error
                      has been detected.   If set when a write com-
                      mand is executed, causes termination class
                      code 6.

02   NOI   Not supported.

01   LXS   Not supported.

00   RIB   Indicates that the BOT marker was encountered
                      after the start of reverse tape motion during
                      a Read, Space, or Skip command. Causes ter-
                      mination class code 2. Tape motion is halted
                      at the BOT position.

SECTION IV - COMPUTER INTERFACE

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SECTION IV

COMPUTER INTERFACE

DEC LSI-11 Q-BUS

The tape coupler interfaces to the Q-Bus of the DEC LSI-11 computer system and other computers which use the DEC Q-Bus. The Q-Bus is an asynchronous I/O bus which multiplexes address and data over the same 16-bit bus lines. In addition to address and data information, the bus contains signal lines for DMA Operations, Interrupt Requests, data transfer handshaking, initialization of devices and other miscellaneous control signals.

BUS INTERFACE SIGNALS

The interface signals used by the tape coupler to communicate with the bus, along with the connector and pin assignments, are shown in Figure / Table 4-1. Your DEC Microcomputer and Memories Handbook (EB-20912-20) should be reviewed for a complete discussion of the DEC Q-Bus. The functions of these signals, as illustrated in Figure 4-2, are:

BBS7 (BANK 7 SELECT) - The bus master asserts BBS7 when a memory address within the I/O page is placed on the bus.

BDAL0-21 (DATA/ADDRESS LINES) - These lines are the 22-bit multiplexed data/address bus over which data, memory address and peripheral register information is communicated. Address information is first placed on the bus by the bus master device and is received and decoded by the selected slave device. The master device then either receives input data from, or outputs data to the addressed slave device (or memory) over these same bus lines. Data transfers use only 16 bits of the 22-bit bus.

BDCOK (DC POWER OK) - This signal from the power supply, when false, initiates power-up/down sequencing in the computer and some devices.

BDIN (DATA INPUT) - This signal is used for two types of bus operations: (1) When asserted during SYNC, it indicates the bus master is receiving data from the bus, and requires a response (RPLY). This operation is also known as a DATI (Data In). (2) Asserted without SYNC, it indicates an interrupt operation.
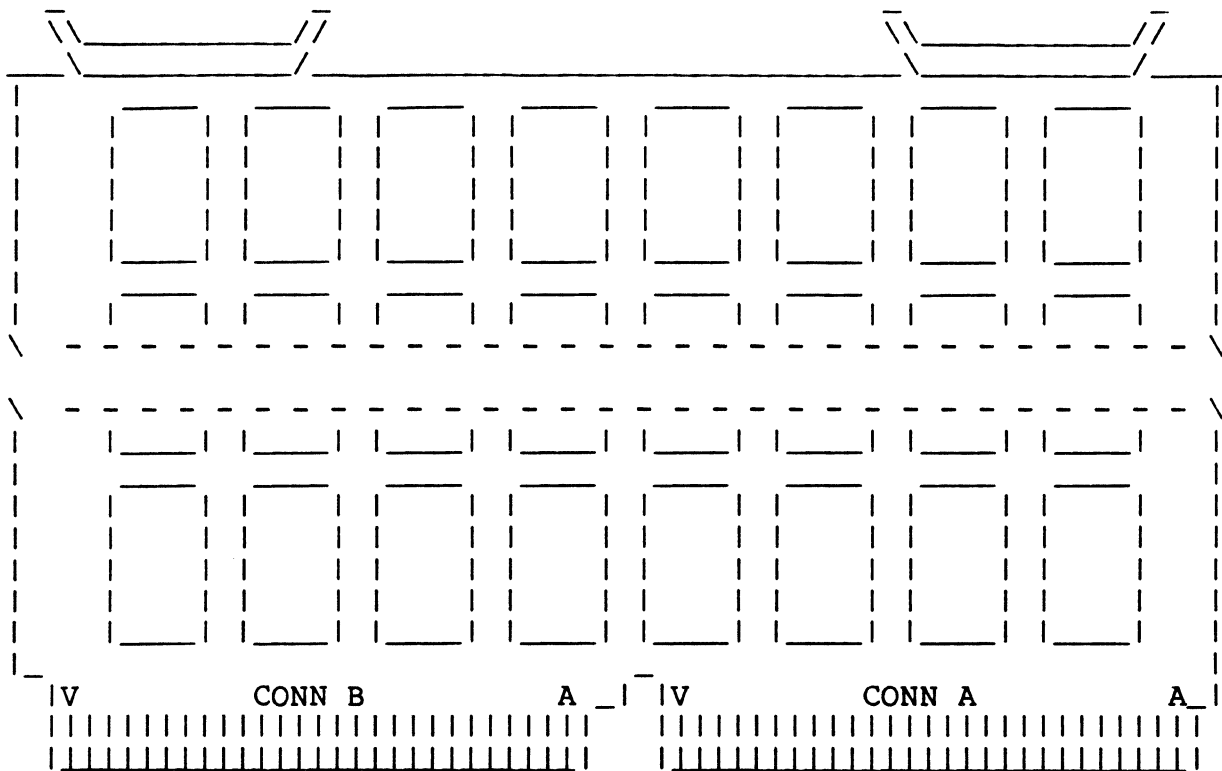
Figure 4-1   Q-Bus Connector arrangement

CONNECTOR A   CONNECTOR B

PIN	SIDE 1 (FRONT)	SIDE 2 (BACK)	PIN	SIDE 1 (FRONT)	SIDE 2 (BACK)
A	BIRQ5 L	+5	A	BDCOK H	+5V
B	BIRQ6 L	-12	B	- BPOK H	-12
C	BDAL16 L	GND	C	BDAL18 L	GND
D	BDAL17 L	+12	D	BDAL19 L	+12
E	SSPARE1	BDOUT L	E	BDAL20 L	BDAL2 L
F	SSPARE2	BRPLY L	F	BDAL21 L	BDAL3 L
H	SSPARE3	BDIN L	H	SSPARE8	BDAL4 L
J	GND	BSYNC L	J	GND	BDAL5 L
K	MSPAREA	BWTBT L	K	MSPAREB	BDAL6 L
L	MSPAREB	BIRQ4 L	L	MSPAREB	BDAL7 L
M	GND	BIAKI L	M	GND	BDAL8 L
N	BDMR L	BIAKO L	N	BSACK L	BDAL9 L
P	BHALT L	BBS7 L	P	BIRQ7 L	BDAL10 L
R	BREF L	BDMGI L	R	BEVNT L	BDAL11 L
S	+12B/+5B	BDMGO L	S	+12B	BDAL12 L
T	GND	BINIT L	T	GND	BDAL13 L
U	PSPARE1	BDAL0 L	U	PSPARE2	BDAL14 L
V	+5B	BDAL1 L	V	+5	BDAL15 L

Table 4-1   Q-Bus Signals

```
 ┌──────────────────┐                    ┌──────────────────────┐
 │ Q-BUS            │                    │ TAPE COUPLER         │
 │                  │                    │                      │
 │      <═══ BDAL∅-21 ═══ 22 ═══>        │ DATA & ADDRESS       │
 │                  │                    │ - - - - - - - - - - -│
 │      <───── BDMR ─────                │                      │
 │      ────── BDMGI ──────>             │ DMA                  │
 │      <───── BDMGO ─────                │                      │
 │      <───── BSACK ─────>               │ - - - - - - - - - - -│
 │                  │                    │                      │
 │      <───── BWTBT ─────>               │                      │
 │      ────── BBS7 ──────>               │ HANDSHAKING          │
 │      <───── BSYNC ─────>               │ AND                  │
 │      <───── BDIN ──────>               │ CONTROL              │
 │      <───── BDOUT ─────>               │                      │
 │      <───── BRPLY ─────>               │ - - - - - - - - - - -│
 │      <───── BIRQ ─────                 │                      │
 │      ────── BIAKI ──────>              │ INTERRUPT            │
 │      <───── BIAKO ─────                │                      │
 │      ────── BINIT ──────>              │ - - - - - - - - - - -│
 │      ────── BDCOK ──────>              │ INITIALIZE           │
 │      ────── BPOK ──────>               │                      │
 │                  │                    │                      │
 └──────────────────┘                    └──────────────────────┘
```
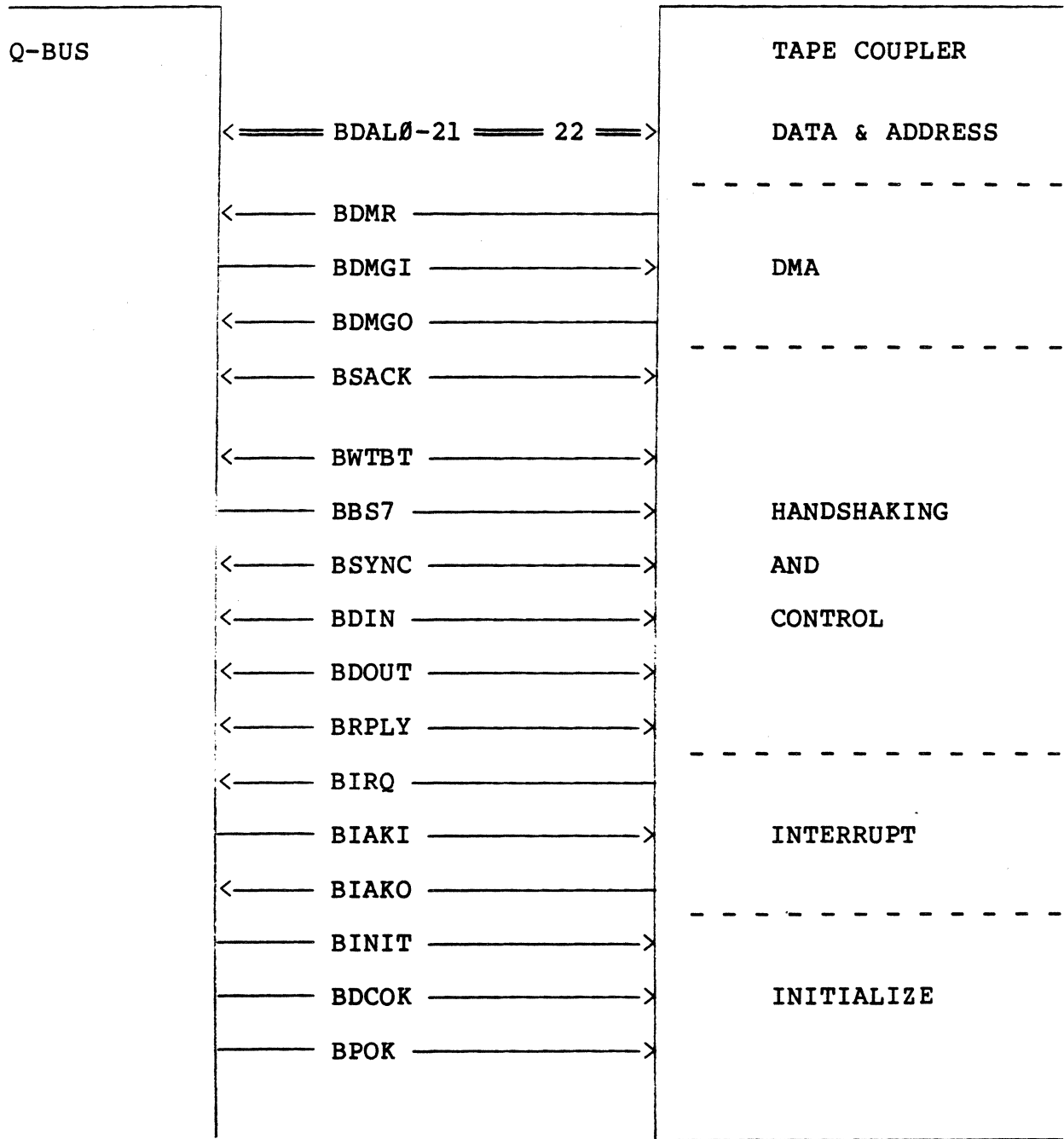
Figure 4-2   Computer Interface

BDMGI/O (DMA GRANT IN/OUT) - This signal is generated at the processor, in response to BDMR. Since BDMGI/O is daisy-chained through the devices connected to the bus, it is received and regenerated by each device until it reaches the requesting device.

BDMR (DIRECT MEMORY REQUEST) - This signal is asserted by the device to request control of the bus for the purpose of transferring device data directly to or from memory.

BDOUT (DATA OUTPUT) - This line indicates the bus master is placing data on the bus. This operation is also known as a DATO (Data Out) or DATOB - Data Out, Byte (from master).

BINIT (INITIALIZE) - This signal is asserted by the processor to initialize or clear all devices connected to the bus. This signal is generated in response to a power-up condition.

BIAKI/O (INTERRUPT ACKNOWLEDGE IN/OUT) - This signal is generated at the processor in response to an interrupt request. The processor asserts bIAKO, which is routed to the pin of the first device on the bus. Since the BIAKI/O line is daisy-chained through the devices connected to the bus, it is received and regenerated by each device until it reaches the requesting device.

BIRQ4-7 (INTERRUPT REQUEST) - The device asserts interrupt request at its assigned level to request interrupt service from the processor.

BPOK (AC POWER OK) - This signal from the power supply initiates power-fail sequencing in the computer and some devices.

BRPLY (REPLY) - This control signal is issued by the slave device in response to the signals BDIN or BDOUT generated by the master device to indicate that data has been placed on the bus or data has been accepted from the bus. BRPLY is also a response to BIAKI to indicate that the vector has been placed on the bus.

BSACK (SELECTION ACKNOWLEDGE) - This signal is asserted by the device in response to the processor's DMGO signal, indicating that the DMA device is bus master.

BSYNC (BUS SYNCHRONIZE) - The bus master device asserts this control signal to indicate that it has placed Address information on the bus. The transfer is in progress until SYNC is negated.

BWTBT (WRITE BYTE) - This signal controls the bus in two ways: (1) It is asserted during SYNC to indicate that an output sequence is to follow. (2) It is asserted during DOUT in a DATOB bus cycle to indicate byte addressing.

NOTE: Other signals on the backplane are not used.

BUS OPERATIONS

The tape coupler receives commands from and provides status information to the processor, with the tape coupler being the slave device. After the tape coupler receives the proper commands to transfer data, the tape coupler becomes a bus master device, handling the data transfers directly with memory (a process which requires no processor intervention). When the tape coupler has completed all data transfers, it alerts the processor by issuing an interrupt request. Bus operations are illustrated in Figures 4-3 and 4-4 and are described in the following paragraphs.
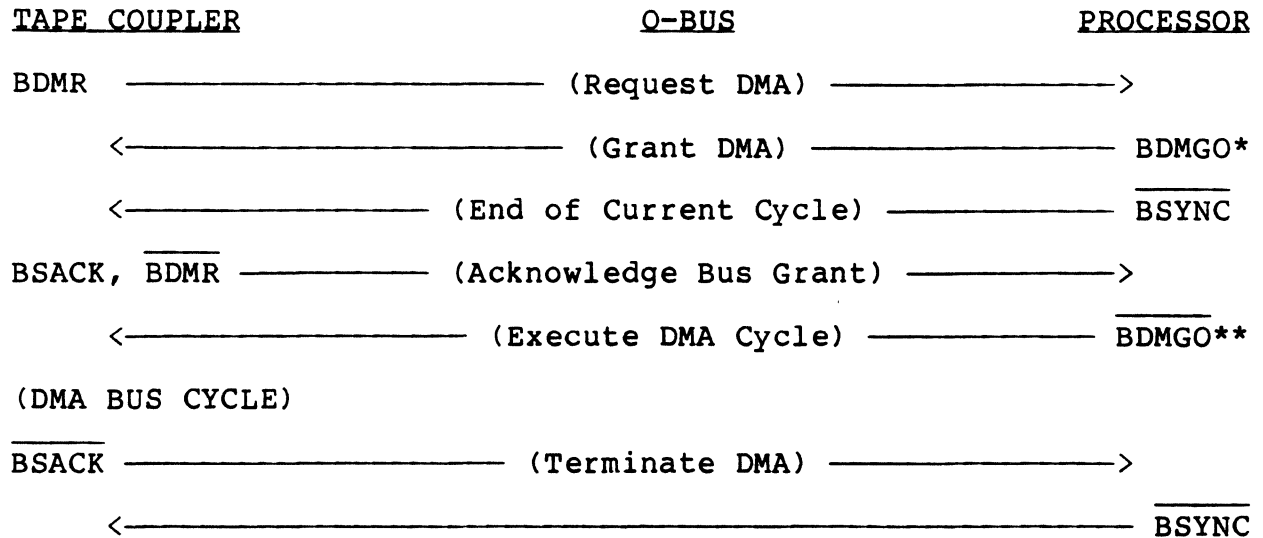
The tape coupler requests a data transfer on the bus by asserting BDMR. After completing the current bus cycle, the processor inhibits initiation of a new bus cycle and responds by asserting BDMGO. The tape coupler then asserts SACK and removes BDMR, causing the processor to terminate BDMGO. The tape coupler becomes bus master, and will execute the required bus transfer: an input transfer when writing to tape and an output transfer when reading from tape. (See below for explanation.) When the data transfer is completed, the tape coupler relinquishes the bus to the processor by terminating the SACK signal. The processor then returns to its programmed operations.

INPUT AND OUTPUT OPERATIONS

Input operations are used by the processor to receive status information from the tape coupler and are used by the tape coupler to obtain data from memory to be written onto tape. Output operations are used by the processor to provide the tape coupler with command information and are used by the tape coupler when transferring information read from tape to the desired location in memory.

To begin any transfer, BSYNC and the address are placed on the bus together with BBS7 (if the I/O page is addressed) and BWTBT (if the transfer will be an output transfer). After the device is selected and the address taken off of the bus lines, BDIN is asserted for an input transfer. The slave device responds by placing data and BRPLY on the bus. The master device then receives the data, terminating BDIN, which causes the slave device to remove both BRPLY and the data from the bus lines. The BSYNC signal is then removed by the master device, terminating the input transfer.

For an output transfer, BDOUT replaces the BDIN signal and is asserted by the bus master together with the output data and the BWTBT if it is a byte transfer. The slave device accepts the data and acknowledges by asserting the BRPLY signal, which causes the master device to remove the data and terminate the BDOUT signal. This action by the master device causes the slave to remove the BRPLY signal which in turn causes the master to remove the BSYNC signal, terminating the output transfer.

TAPE COUPLER   Q-BUS   PROCESSOR

BDMR ————————————————————— (Request DMA) ————————————————>

       <————————————————————— (Grant DMA) ———————————————— BDMGO*

       <————————————————— (End of Current Cycle) ———————————— $\overline{BSYNC}$

BSACK, $\overline{BDMR}$ ——————————— (Acknowledge Bus Grant) ——————————>

       <——————————————— (Execute DMA Cycle) ——————————— $\overline{BDMGO}$**

(DMA BUS CYCLE)

$\overline{BSACK}$ ————————————————————— (Terminate DMA) ————————————————>

       <——— $\overline{BSYNC}$

* NOTE: Daisy-chained signal

Figure 4-3   DMA Request/Grant Sequence

<u>MASTER</u>   <u>SLAVE</u>

Addressing Phase

Address*, BSYNC ——— (Device Addressing) ——————>

        <————————— (Device Selected) ——————————

$\overline{\text{Address}}$ ————————————————————————————————————>

Input Operation

BDIN ————————————— (Request Data) ——————————————>

        <———————————— (Input Data) ————————— Data, BRPLY

$\overline{\text{BDIN}}$ ———————— (Terminate Input Transfer) ——————>

        <—————————— (Terminate Input Cycle) ——— $\overline{\text{Data}}$, $\overline{\text{BRPLY}}$

$\overline{\text{BSYNC}}$ ———>

Output Operation

Data, BWTBT, BDOUT ——— (Output Data) ——————————>

        <————————————— (Data Accepted) ———————————— BRPLY

$\overline{\text{Data}}$, $\overline{\text{BDOUT}}$ ——— (Terminate Output Transfer) —————>

        <————————— (Terminate Output Cycle) ————— $\overline{\text{BRPLY}}$

$\overline{\text{BSYNC}}$ ———>

* Assert BBS7 if the I/O page is addressed and
  assert BWTBT for output transfers

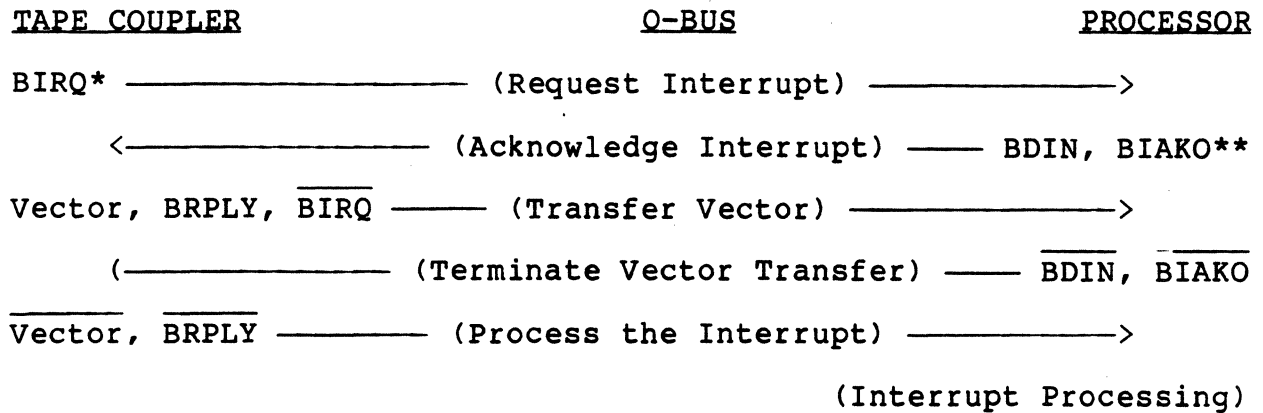**Figure 4-4   Bus Transfer Sequences**

INTERRUPTS

Interrupts are used in the system so that the processor is not burdened with the responsibility of determining when a device has completed an operation. Interrupt processing allows the processor to continue with its programmed tasks until alerted by the device.

When enabled in the device, the Interrupt Request (BIRQ4-7) is issued to the processor upon occurrence of a a specified event, such as upon completion of an operation. When the instruction in progress has been completed and if the processor currently is accepting Interrupt Requests at the specified priority level, further program execution is suspended and the the daisy-chained Interrupt Acknowledge (BIAKO) signal is issued as a response.

The daisy-chained Interrupt Acknowledge signal is passed along by each device until captured by the requesting device, which also must monitor the Interrupt Request lines as defined in Table 4-2 to be sure no device of higher priority is also requesting service. The interrupting device will then remove the Interrupt Request, assert BRPLY, and place its hardware-selected vector address onto the bus.

The vector points to memory locations containing a new processor status word (psw) and the program counter address (pc) of the interrupt handling routine. The processor saves its current processor status word and program counter address, receives the vector, and then terminates the BDIN and BIAKO signals. This causes the device to terminate the BRPLY signal and remove the vector from the bus.

The processor will then enter the tape coupler's interrupt service routine to handle the interrupt. The new PSW received can raise the interrupt priority level to prevent low-level interrupts from breaking into the interrupt handler.

TAPE COUPLER   Q-BUS   PROCESSOR

BIRQ* ————————————— (Request Interrupt) ——————————>

    <————————————— (Acknowledge Interrupt) ——— BDIN, BIAKO**

Vector, BRPLY, $\overline{BIRQ}$ ———— (Transfer Vector) ——————————>

    (————————————— (Terminate Vector Transfer) ——— $\overline{BDIN}$, $\overline{BIAKO}$

$\overline{Vector}$, $\overline{BRPLY}$ ————— (Process the Interrupt) ——————————>

                                          (Interrupt Processing)

NOTE: * See priority-level explaination ** Daisy-chained signal

Figure 4-5   Interrupt Request Sequence

INTERRUPT LEVEL	LINES ASSERTED BY DEVICE	LINES MONITORED BY DEVICE
4	BIRQ4	BIRQ5/6
5	BIRQ4/5	BIRQ6
6	BIRQ4/6	BIRQ7
7	BIRQ4/6/7	(None)

Table 4-2   Interrupt Request Priority

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SECTION V − PERTEC−COMPATIBLE FORMATTER INTERFACE

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SECTION V

PERTEC-COMPATIBLE FORMATTER INTERFACE

FORMATTED TAPE DRIVE INTERFACE

This section defines the interface to the tape formatter for the streaming or non-streaming tape units controlled by the tape coupler. This interface is based on the industry standard interface for 1/2 inch formatted tape units, The basic industry conventions such as cabling, electrical characteristics, data and command transfer characteristics, and timing have been maintained.

Two 50-conductor 3M-type ribbon cables are used for interconnection between the standard or streaming transport formatter and the tape coupler. These cables are connected between the card connectors on the tape coupler and the formatter PC board. Cable length can be a maximum of 6.0 meters (20 feet).

The formatter input circuits are designed such that either a disconnected wire or removal of power at the transmitter results in a false signal being interpreted at the receiver end. All lines between the tape coupler and the drive's formatter are low-true and driven by tri-state devices,

The following tables provide a list of pins and a definition of terms as used on the interface between the tape coupler and the formatter.

CONNECTOR J1			CONNECTOR J2		
SIGNAL PIN	RETURN PIN	LO-TRUE SIGNAL	SIGNAL PIN	RETURN PIN	LO-TRUE SIGNAL
2	1	FFBY	1	5	FRDP
4	3	FLWD	2	5	FRDO
6	5	FWD4	3	5	FRD1
8	7	FGO	4	5	FLDP
10	9	FWD0	6	5	FRD4
11	12	FWD1	8	7	FRD7
14	13	SPARE	10	9	FRD6
16	15	NOT USED	12	11	FHER
18	17	FREV	14	13	FFMK
20	19	FREW	16	14	FID
22	21	FWDP	18	17	FFEN
24	23	FWD7	20	19	FRD5
26	25	FWD3	22	21	FEOT
28	27	FWD6	24	23	FOFL
30	29	FWD2	26	25	NOT USED
32	31	FWD5	28	27	FRDY
34	33	FWRT	30	29	FRWD
36	35	NOT USED	32	31	FFPT
38	37	FLGAP	34	33	FRSTR
40	39	FERASE	36	35	FDWDS
42	41	FWFM	38	37	FDBY
44	43	NOT USED	40	39	NOT USED
46	45	FTAD0	42	41	FCER
48	47	FRD2	44	43	FONL
50	49	FRD3	46	45	FTAD1
			48	47	FFAD
			50	49	FSMC

Table 5-1   I/O Cable Pin Assignments

Table 5-2   Tape Coupler To Formatter Signals

LO-TRUE SIGNAL	DEFINITION	DESCRIPTION
FFAD	Formatter Address	This signal level selects one of two possible transports attached to to transport interface: 1. FFAD False = Address 0 2. FFAD True = Address 1 The transport's address is pre-determined by a strap on the formatter PWA.
FTAD0,1	Transport Address	Addresses up to 4 transports per formatter.
FGO	Initiate Command	This signal is used to strobe the following command lines on the trailing edge: 1. FREV 4. FERASE 2. FWRT 5. FLGAP 3. FWFM 6. FSMC
FREV	Reverse/Forward	This signal specifies the direction of tape motion as follows: 1. False = Forward 2. True = Reverse
FWFM	Write File Mark	
FERASE	Erase Tape	If FERASE and FWRT are low, the transport is positioned to execute a Dummy-Write command. The transport will go through all of the operations of a normal Write command except that data is recorded. A length of tape will be erased equivalent to the length of the Dummy-Record (as defined by FLWD). Alternatively, if FERASE, FWRT, and FWFM command lines are all low, the transport is conditioned to execute a Dummy-Write File Mark command. A fixed length of tape of approximately 3.6 inches will be erased.

Table 5-2   Tape Coupler To Formatter Signals (Continued)

LO-TRUE SIGNAL	DEFINITION	DESCRIPTION
FLGAP	Long Gap	When true, this line causes the transport to be set up for 1.2 inch gap. When false, will select the normal 0.6 inch gap.
FSMC	Speed Mode change	This signal causes selected transports to change the mode of operation (12.5 ips/100 ips).
FREW	Rewind	This signal (minimum 1.0 microsecond pulse) causes the selected transport to rewind to BOT. The FRWD signal is asserted during the rewind operation. Formatter Busy is not set during a Rewind.
FOFL	Off-line & Rewind	This line must be held true for a minimum of 1.0 microsecond. It causes the transpoert to rewind and unload the tape. Formatter Busy is not set.
FWDO-7,P	Write Data	These lines transmit data to the transport. FWDO represents the most significant bit.
FFEN	Formatter Enable	This signal, when false, causes the transport to be reset to initialized state. It is independent to FFAD. This is a level signal that will hold the transport reset while false.
FLWED	Last Word	During Write and Controlled Erase, this line, when true with FWDO-7, FWDP indicates that the character being strobed into the formatter is the last of the record.

Table 5-3   Formatter Interface Commands

COMMAND	LOOP	SNSR	REV	WRT	WFM	ERASE
Read Forward*	Low	Low	Low	Low	Low	Low
Read Reverse*	Low	Low	High	Low	Low	Low
Write*	Low	Low	Low	High	Low	Low
Write File Mark	Low	Low	Low	High	High	Low
Space Forward	Low	Low	Low	Low	Low	High
Space Reverse	Low	Low	High	Low	Low	High

Low = False
High = True

* FLGAP is also strobed during these command transfers indicating
the setting of a long or normal gap length (2.2 inch IBG or 0.6
inch IBG nominal, respectively). FSMC is also strobed by FGO.
However, FSMC is not issued during data operations. (FLGAP,
FSMC and FGO are low-true signals.)

Table 5-4   Formatter To Tape Coupler Signals

LO-TRUE SIGNAL	DEFINITION	DESCRIPTION
FFBY	Formatter Busy	Only goes true when FGO command is received. Remains true until completion of command execution.
FDBY	Data Busy	Only goes true when the transport has reached operating speed, traversed the IBG, and the transport is about to write data on the tape or read data from the tape. Data Busy remains low until the data transfer is finished. A new command may be given when Data Busy goes false for an "on-the -fly" operation. "On-the-fly" commands must be the same read/write mode and same tape direction.
FID	PE Identification	Set when writing first record from load point or reading first record from load point if tape is PE.
FHER	Hard Error	This line is set low if any error has been detected. This line will be set low as soon as an error occurs and stays low until the next FGO signal is transmitted, or the FFEN signal is set high. all error information will be reported to the coupler before FDBY signal goes false.
FCER	Corrected Error	This line is set low whenever a single track error occurs during a read or read-after-write operation. The signal will stay true until the next FGO signal is transmitted or FFEN signal is set high. If the FCER signal is set low during the read-after-write operation, the record should be rewritten.
FFMK	File Detected	
FRDY	Selected Transport On-Line	
FRWD	Rewind	
FEOT	End of Tape	

Table 5-4   Formatter To Tape Coupler Signals (Continued)

LO-TRUE SIGNAL	DEFINITION	DESCRIPTION
FFPT	File Protect	
FLDP	Load Point	
FDWDS	Demand Write Data Strobe	
FDWDS	Demand Write Data Strobe	This line consists of a pulse for each data character to be written onto tape. The pulse width of signal FWDS is 1 microsecond. The first data character should be available on the write data input lines within one character period after the FDBY signal has been set true, and remain true until the trailing edge of the first FDWDS signal.
		Succeeding characters must then be placed on these lines within one-half of a character period after the trailing edge of each FDWDS signal. During a Write File Mark command, the required file mark pattern is generated internally by the formatter and the FDWDS signal is not used. During erase operation (variable length), this line will also be used. However, no data are transferred or written onto tape. The coupler may use this line to determine the length of tape which has been erased.

Table 5-4   Formatter To Tape Coupler Signals (Continued)

LO-TRUE SIGNAL	DEFINITION	DESCRIPTION
FRSTR	Read Data Strobe	This line consists of a pulse for each character of read information to be transmitted to the customer coupler interface and should be used to sample the read data lines FRDP, FRDO-7. The pulse width of this signal is 1.2 microseconds. The average time between pulses on the FRSTR line is given by: $$\frac{1}{S \times D}$$ Where D = 1600 bpi and S = tape speed (ips) The customer coupler interface must be able to accept the whole block of data at the specified data rate. Due to bit crowding, tape speed variation, and signal drop-out correction (PE), the customer coupler interface must be able to receive characters at a rate which can vary twice the nominal rate and half the nominal rate.
FRDO-7, P	Read Data	These nine lines transmit read data from the formatter to the customer coupler. Each character read from tape is available to sampling these lines in parallel with the FRSTR. Data will be placed on the read to the leading edge of the FRSTR pulse. The data remans on the read datsa 1;ines for at least 0.5 microseconds after the trailing edge of the FRSTR pulse. Sense data is also transmitted on this bus analogous to the read data at 160K byte/second rate.

SECTION VI - STC TAPE INTERFACE

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GCR FORMATTED TAPE DRIVE INTERFACE

This section defines the interface to the STC tape formatter
for tape units with GCR tape format capability controlled by the
TAPE DIMENSION coupler. This interface is based on the
manufacturer specifications for interfacing 1/2 inch GCR-
formatted tape drives.

Two 60-pin cables are used for the connection between the
tape formatter and the tape coupler. These cables are connected
between the card connectors on the tape coupler and the tape
formatter. Cable length can be a maximum of 6.0 meters (20
feet).

Formatter input circuits are typically designed such that
either a disconnected wire or removal of power at the transmitter
results in a false signal being interpreted at the receiver end.
All lines between the tape adapter and the drive's formatter are
low-true and driven by tri-state devices.

The following paragraphs and tables provide a list of pins
and a definition of terms as used on the interface between the
coupler and the formatter.

COUPLER-TO-FORMATTER SIGNALS

Initiate Command (Start) - This line clocks the command, address
and density into the formatter and initiates the command. The
coupler asserts this signal until the formatter goes Busy.

Tape Unit Address (AD0,1) - Tape unit address lines are available
at the interface for selection of a specific tape unit connected
to the formatter.

Density Select (DS0,1) - During a read operation, tape density is
automatically set according to the ID Burst. For a write opera-
tion (with the drive positioned at load point and set for remote
software density selection) these lines select the density as
follows:

DS0	DS1	Density Selected
0	0	Phase Encoded
1	0	Group Code Recording
0	1	NRZI
1	1	Selected on drive panel

Command Select (CMD0-3) - The commands to the formatter are specified by the code present on these lines when the Command Clock line is asserted.

STC CMD0-3	Function
0 0 0 0	No Operation
0 0 0 1	Drive Clear
0 0 1 0	Diagnostic Mode
0 0 1 1	Sense Drive Status
0 1 0 0	Read One Block
0 1 0 1	Read Reverse One Block
0 1 1 0	Write One Data Block
0 1 1 1	Loop Write-to-Read
1 0 0 0	Backspace One File
1 0 0 1	Backspace One Block
1 0 1 0	Forward Space One File
1 0 1 1	Forward Space One Block
1 1 0 0	Write Tape Mark
1 1 0 1	Erase 3.5 Inch Gap
1 1 1 0	Rewind Tape
1 1 1 1	Rewind and Unload

Data Transfer Acknowledge (TRAK) - The coupler responds to the Data Transfer Request signal from the formatter with this signal. These handshaking signals are used to transfer all write and read data with the following meanings:

	Handshaking Signals	
Function	Data Req.	Data Ack.
Write	Data Req'd.	Data Avail.
Read	Data Avail.	Data Stored

Last Byte (STOP) - This signal indicates to the formatter that the last write data byte has been placed on the formatter bus. This signal (asserted in response to Data Transfer Request or Block Sensed) also terminates read transfers and spacing operations.

Tape Subsystem Reset (SRS) - This signal resets the formatter and tape drive, discontinuing any operations in progress and resetting all command, data and status conditions. (Reset during tape motion could result in incorrect positioning or incomplete blocks.)

Multiplexed Error Status Select Code (ESC0,1) - The code on these lines selects the information to be placed on the Multiplexed Error Status Bus, as follows:

STC SLX2-0	DESCRIPTION	MULTIPLEXED ERROR BIT								
		P	7	6	5	4	3	2	1	0
0 0 0	Dead Tracks	DTP	DT7	DT6	DT5	DT4	DT3	DT2	DT1	DT0
0 0 1	Read/Write Errors	CRC ERR	WTM CHK	UCE	PART REC	MTE	NOT USED	END DATA CHK	VEL ERR	DIAG MODE LTCH
0 1 0	Diag. Aids	TACH	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
0 1 1	Drive Sense Byte	WRT STAT	EOT STAT	BOT STAT	WRT INHB	FILE PROT	BKWD STAT	HIGH DENS	RDY STAT	ON-LINE
1 0 0	CRC-F	P	7	6	5	4	3	2	1	0
1 0 1	Reserved									
1 1 0	Reserved									
1 1 1	Reserved									

Bidirectional Data Bus (DATA 0-7,P) - These nine data lines transmit data between the coupler and the tape drive.

FORMATTER-TO-COUPLER SIGNALS

Data Transfer Request (TREQ) - This handshaking signal requests a transfer of read or write data between the coupler and the formatter. (See Data Transfer Acknowledge)

Block Sensed (BLOCK) - This signal indicates that the formatter has detected a data or tape mark block.

Oscillator (OSC) - This signal line is derived from the internal crystal oscillator in the formatter, as follows:

```
GCR 50-75 ips    2.72 MHz
GCR    125 ips    2.27 MHz
NRZI and PE      1.40 MHz
```

End of Data Pulse (ENDATP) - This signal is asserted to indicate the last data byte has been read and (implied) transferred to the coupler.

Formatter Busy (BUSY) - This signal is true from the time the command is initiated until it is rejected or completed.

Identification Burst (ID BRST) - This signal indicates an Identification Burst (6250 or 1600) has been read or is being written.

Tape/File Mark Status (TMS) - This signal indicates a File/Tape Mark has been read or is being written.

Command Reject (REJECT) - This signal indicates the previous command is inappropriate to formatter/drive status.

Operation Incomplete (OP INC) - This signal is set to indicate the command was initiated but was not completed by the formatter.

Overrun Status (OVRNS) - This signal indicates the data rate of the formatter has exceeded the transfer rate of the coupler/bus and data has been lost.

ROM Parity Error Status (ROMPS) - This signal indicates an internal microcode failure in the formatter.

Slave Status Change (SSC) - This line indicates a drive has gone Ready, On-Line or Off-Line.

Data Check (DATA CHK) - This signal indicates one or more of the following conditions has occurred: Any bit (exc. bit 1) of Multiplexed Error Status Byte 1, (CRC Error, Write Tape Mark Check, Uncorrectable Error, Partial Record, Multiple Track Error, End of Data Check, Velocity Error), Overrun, VRC Error, LRC Error, TIE Cannot be Found, Write Skew Error, BOT Detected, PE Postamble Error, Single Track Error.

Multiplexed Error Status Bus (ERRMX 0-7,P) - These nine lines provide the Error Status Bytes previously described.

Corrected Error (CRERR) - This signal is set to indicate the following errors have been corrected:

1 - PE single track read or read-after-write error.
2 - GCR single or double track read or read-after-write error.
3 - NRZI tape error - resulting in a reread.

Data Bus Parity Error (BUPER) - This line indicates incorrect data parity was detected on the formatter data bus.

On Line Status (ONLS) - This status line indicates the tape drive is On Line.

Ready Status (RDYS) - This status line indicates the tape drive is On Line with tape loaded and not rewinding.

Beginning of Tape Status (BOTS) - This status line indicates the tape is positioned at the BOT marker.

End of Tape Status (EOTS) - This status line indicates the tape is positioned at or beyond the EOT marker.

File Protect Status (FPTS) - This status line indicates the tape was loaded on the drive without a write-enable ring in the supply reel.

Rewinding Status (REWS) - This status line indicates the tape is rewinding to BOT.

High Density Status (HDENS) - This status line indicates the GCR format is selected.

NRZI Status (NRZI) - Unless High Density Status is selected, this status line indicates the NRZI format is selected.

Table 6-1 Pin Assignments for STC Interface
(Connector J1)

COUPLER
CONNECTOR J1

SIGNAL PIN	GROUND PIN	COUPLER SCHEM. MNEMONIC	STC MNEMONIC
A2	B2	ER0	ERMX-0
A3	B3	ER1	ERMX-1
A4	B4	ER2	ERMX-2
A5	B5	ER3	ERMX-3
A6	B6	ER4	ERMX-4
A7	B7	ER5	ERMX-5
A8	B8	ER6	ERMX-6
A9	B9	ER7	ERMX-7
A10	B10	FBSY	BUSY
A11	B11	DREQ	TREQ
A12	B12		
A13	B13	IDB	ID BURST
A14	B14	OPI	OPINC
A15	B15	DBSY	ENDATP
A16	B16	FMT	TMS
A17	B17	RJS	REJECT
A18	B18	OVR	OVRNS
A19	B19	EM	DATA CHK
A20	B20	RPE	ROMPS
A21	B21	CERR	CRERR
A22	B22	BLK	BLOCK
A23	B23	DD0	NRZI
A24	B24	DPE	BUPER
A25	B25	ONL	ONLS
A26	B26	DD1	HDENS
A27	B27	RDY	RDYS
A28	B28		
A29	B29	CMD0	RESERVED
A30	B30	TA0	RESERVED

NOTE: All interface signals are low-true.

Table 6-2   Pin Assignments for STC Interface
(Connector J2)

COUPLER
CONNECTOR J2

SIGNAL PIN	GROUND PIN	COUPLER SCHEM. MNEMONIC	STC MNEMONIC
A1	B1	TA0	AD0
A2	B2	TA1	AD1
A3	B3	CMD1	CMD0
A4	B4	CMD2	CMD1
A5	B5	CMD3	CMD2
A6	B6	CMD4	CMD3
A7	B7	DS0	DS0
A8	B8	CMDCLK	START
A9	B9	LBYT	STOP
A10	B10	DACK	TRAK
A11	B11	(NO NAME)	DATA-P
A12	B12	(NO NAME)	DATA-0
A13	B13	(NO NAME)	DATA-1
A14	B14	(NO NAME)	DATA-2
A15	B15	(NO NAME)	DATA-3
A16	B16	(NO NAME)	DATA-4
A17	B17	(NO NAME)	DATA-5
A18	B18	(NO NAME)	DATA-6
A19	B19	(NO NAME)	DATA-7
A20	B20	SRST	RESET
A21	B21	ESC1	SLX1
A22	B22	ESC0	SLX0
A23	B23	DS1	DS1
A24	B24	ESC2	SLX2
A25	B25	ERR	SSC
A26	B26	OSC	OSC
A27	B27	EOT	EOTS
A28	B28	LP	BOTS
A29	B29	FP	FPTS
A30	B30	RW0	REWS

NOTE: All interface signals are low-true.

N O T E S

SECTION VII – NRZI AND PE TAPE FORMAT

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ILLUSTRATIONS

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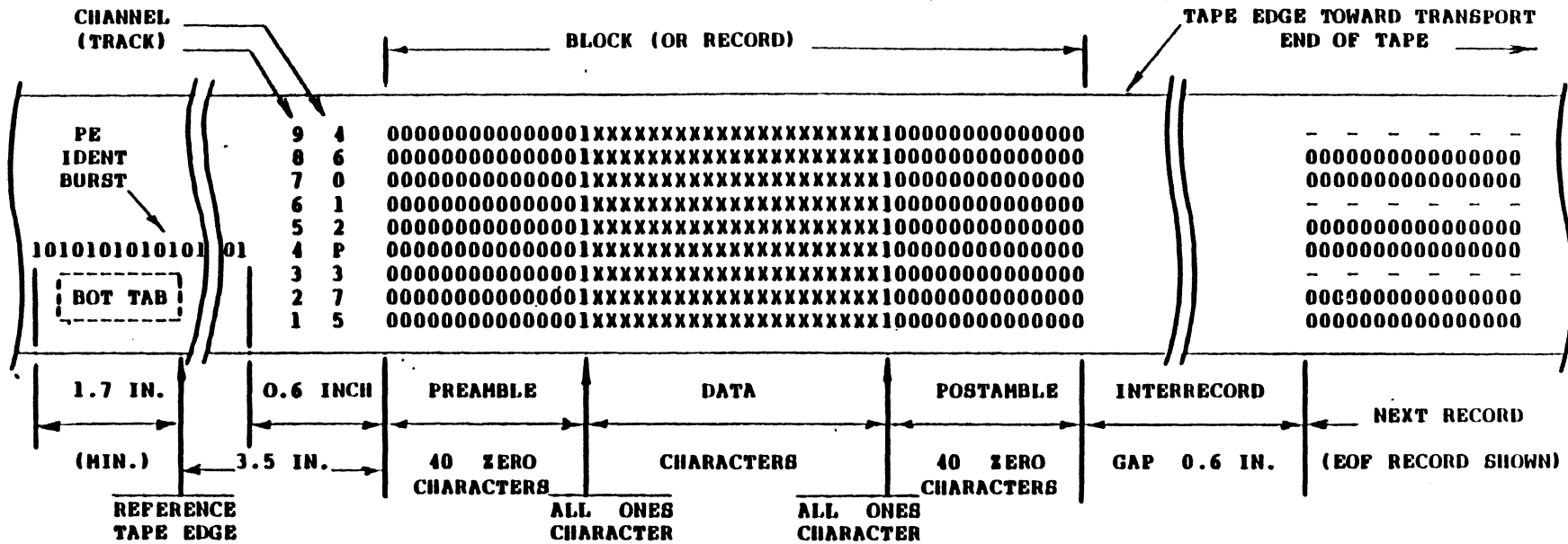
SECTION VII

NRZI AND PE TAPE FORMAT

INTRODUCTION

The TAPE DIMENSION / Q-BUS Tape Coupler interfaces to industry standard formatted tape drives which write nine bit characters laterally across the tape. While the formatter in the drive is responsible for actually writing the data, this section provides an insight into how the data is formatted on tape. The density of the characters written on the tape is determined by the type of tape unit and (in some cases) the density selection made at the drive and/or the command issued by the CPU. A data block (record) written on the tape consists of data characters and error checking characters (or a preamble and postamble). Every data character consists of the data byte plus an odd parity bit that is generated by the formatter to conform with odd parity as specified by the format. A record (or block) of data on tape represents the data transferred to or from a block of memory in response to one read or write command. Adjacent records are separated by automatically erasing a 0.6 inch segment of tape to form an interrecord gap (IRG).

NINE-TRACK PE FORMAT

The tape coupler uses the standard nine track Phase Encoded (PE) 1600 bits per inch tape format. Each tape block contains a preamble, a variable length data field, and a postamble. The 41 character preamble consists of 40 tape characters with all-zero bits followed by one character of all-one bits. The preamble is followed by the data field which also contains an odd vertical parity bit for each data character. Following the last character of the data field is the postamble which contains an all-ones character followed by 40 all-zero characters (the reverse-image of the preamble).

When the tape is at load point (beginning of tape) and the first data block is to be written, it is preceded by an identification burst consisting of alternating one and zero bits in the track for the parity (P) channel. with all other tracks erased. The file mark consists of 40 all-zero characters similar to those in the preamble or postamble, except that the tracks for channels 1, 3 and 4 are erased.

```
CHANNEL ____                                                           TAPE EDGE TOWARD TRANSPORT
(TRACK) ____            |◄————————  BLOCK (OR RECORD) ————————►|          END OF TAPE ————►

    PE          9  4    000000000000001xxxxxxxxxxxxxxxxxxxxxxxx100000000000000    _ _ _ _ _ _
  IDENT         8  6    000000000000001xxxxxxxxxxxxxxxxxxxxxxxx10000000000000    0000000000000000
  BURST         7  0    000000000000001xxxxxxxxxxxxxxxxxxxxxxxx10000000000000    0000000000000000
                6  1    000000000000001xxxxxxxxxxxxxxxxxxxxxxxx10000000000000    _ _ _ _ _ _
                5  2    000000000000001xxxxxxxxxxxxxxxxxxxxxxxx10000000000000    0000000000000000
101010101010101 01  4  P 000000000000001xxxxxxxxxxxxxxxxxxxxxxxx10000000000000    0000000000000000
                3  3    000000000000001xxxxxxxxxxxxxxxxxxxxxxxx10000000000000    _ _ _ _ _ _
  BOT TAB       2  7    000000000000001xxxxxxxxxxxxxxxxxxxxxxxx100000000000000   0000000000000000
                1  5    000000000000001xxxxxxxxxxxxxxxxxxxxxxxx10000000000000    0000000000000000
```

1.7 IN.	0.6 INCH	PREAMBLE	DATA	POSTAMBLE	INTERRECORD	
(MIN.)	3.5 IN.	40 ZERO CHARACTERS	CHARACTERS	40 ZERO CHARACTERS	GAP 0.6 IN.	NEXT RECORD (EOF RECORD SHOWN)

REFERENCE
TAPE EDGE

ALL ONES CHARACTER   ALL ONES CHARACTER

NOTES:

1. Tape shown oxide side up.

2. Channels 0 thrtough 7 contain data in decending order of significance.

3. Parity channel (P) always contains odd data character parity.

4. The PE Identification Burst contains alternating one and zero bits.

5. Data is recorded at 1600 characters per inch.

6. A File Mark is a 40 character burst, with "0" bits in channels P. 0, 2, 5, 6 and 7. Channels 1, 3, and 4 are erased and indicate dead tracks when read back. The EOF is preceded by a normal 0.6 inch gap, and is also separated by any following data record by a 0.6 inch inch gap.

Figure 7-1   1600 BPI PE Tape Format

NINE-TRACK NRZI FORMAT

In the nine-track NRZI format, characters are written on the tape in 800 bits per inch density. Each data character contains eight data bits and one odd vertical parity bit. Following the last data character, the End of Record (EOR) gap (three blank characters) is written, followed by a Cyclic Redundancy Check (CRC) character, followed by three more blank characters, concluded by a Longitudinal Redundancy Check (LRC) character. The LRC character produces an even longitudinal parity in each of the tracks along the length of the tape. Reading or Writing, the tape coupler checks to ascertain that the lateral parity of every data character is odd, that the CRC character is correct, and that every track has even longitudinal parity.

The nine-track NRZI file mark consists of a single character record with a one-bit in channels 3, 6 and 7; the remaining channels contain zeros. The CRC character is left blank, but an LRC character is written which is identical to the file mark character.

RECORDING METHODS

NRZI and Phase Encoded formats are recorded on tape. using different recording techniques. In Figure 7-3, NRZI and PE waveforms are compared. The NRZI waveform shows a change in flux polarity for each binary one bit. A binary zero is represented by the absence of a flux change.

Phase encoded recording requires at least one flux change per bit cell. A binary zero leaves the flux polarized opposite to that of the interrecord gap.

DATA BLOCK SIZE

The maximum data block size is only limited by the Byte/Record Counter to a full 64K byte block. The minimum recommended data block size can vary with the application. depending upon the system where the generated tapes will be used.
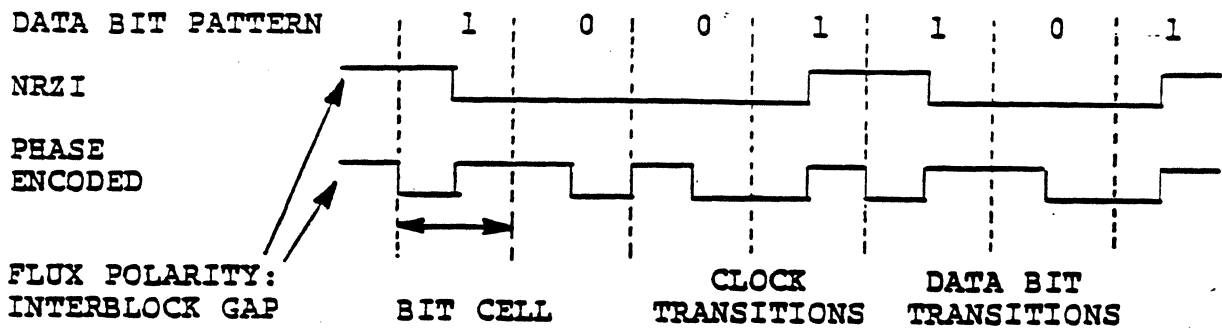
END-OF-FILE MARKS

The program can group sets of data records into files. The end of a file is indicated by an End Of File (EOF) mark. The PE File Mark consists of 40 all-zero characters in a special combination of active and dead tracks. The NRZI File Mark is a special record containing only one special data character and its corresponding LRC character. Each EOF in the NRZI format is preceded by an extended record gap.
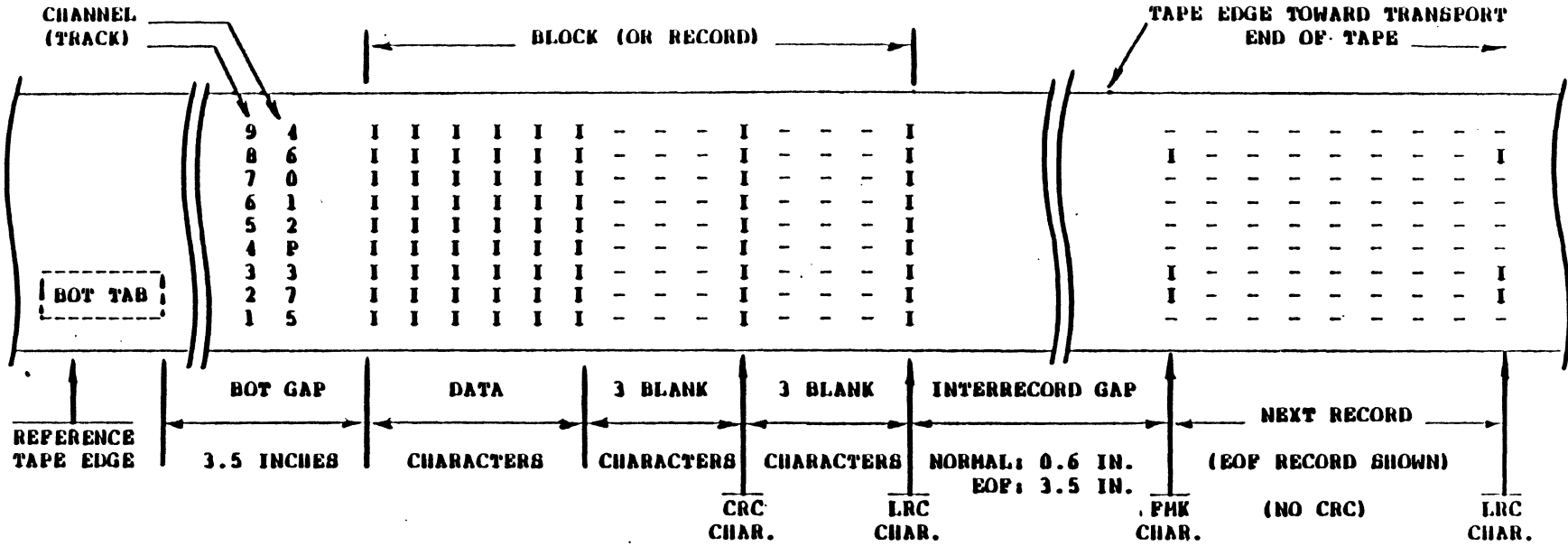
Figure 7-2   800 BPI NRZI Tape Format

NOTES:

1. Tape shown oxide side up.

2. Channels 0 thrtough 7 contain data in decending order of significance.

3. Parity channel (P) always contains odd data character parity.

4. Each bit of the LRC ensures even parity for that track, including total of all data and CRC bits. The LRC is never all zero bits.

5. It is possible for the CRC to be all zeros.

6. A File Mark is a single character record, with "1" bits in channels 3, 6 and 7 for both the data character and the LRC. The CRC contains all zeros. The EOF is preceded by a 3.5 inch gap, and is separated by any following data record by a normal 0.6 inch gap.

7. Data is recorded at 800 characters per inch.

DATA BIT PATTERN | 1 | 0 | 0 | 1 | 1 | 0 | 1

NRZI

PHASE
ENCODED

FLUX POLARITY:
INTERBLOCK GAP   BIT CELL   CLOCK   DATA BIT
                                    TRANSITIONS   TRANSITIONS

NOTES:

NRZI: Any change in polarity   PE: Data bit transition in
      is a "1" bit.   direction of gap polarity
      No change in polarity   is a "1" bit, opposite
      is "0" bit.   direction is a "0" bit.

      Last transition (LRC) returns flux to gap polarity.

Figure 7-3 PE and NRZI Recording Comparison

TRANSFERS

When writing, the coupler divides each computer word into
two eight-bit bytes. In reading, the bytes from the tape are
reassembled into a full sixteen-bit word for the computer bus.

TAPE-END MARKERS

The ends of the tape contain reflective strips that are
detected by photo cells in the tape drive.   The Load Point
marker identifies the logical Beginning of Tape (BOT) and is
positioned to allow at least ten feet of leader at the front of
the tape. A Space Reverse or Rewind command automatically stops
at this marker. At least three inches of tape are erased between
the BOT marker and the first record.

The End of Tape (EOT) marker is located at least 14 feet
from the physical end of the tape. The program should not record
more than a few feet beyond the EOT marker, allowing at least ten
feet of tape for a trailer. A status bit is set and any Space
Reverse operations are terminated when the tape passes beyond the
EOT marker.

DOUBLE DENSITY RECORDING

Some newer tape drives are now recording Phase Encoded tapes at half the normal tape speed. The result is a recorded density of 3200 bits per inch instead of the normal 1600 bits per inch. Since only the tape speed is changed, all other characteristics of normal Phase Encoded recording are retained.

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SECTION VIII

GCR TAPE FORMAT

INTRODUCTION

The Group Code Recording method, known as the GCR Format, allows writing and reading magnetic tapes at high density. The higher tape error rate generated by the high density is virtually eliminated by elaborate error detecting and correcting methods inherent in this format.

ANSI COMPATIBILITY

The coupler will write and read magnetic tapes as specified by ANSI X3.54-1976. The interface signals required to write and read ANSI compatible tapes must be as specified in Section 7 "GCR Tape Interfaces" and Section 3 "Programming". The following paragraphs clarify certain aspects of GCR operation and format compatibility.

DENSITY

The density of recording is 6250 data characters per inch, nominal.

BLOCK LENGTH

The coupler does not control or limit the number of data characters per tape block (within the limits of the byte count) except to disallow the writing of data blocks containing no data characters. The formatter will format the input data, in-dependent of total number of data characters, into the data group and/or residual data group in the ANSI specified format. The coupler may generate data blocks outside the ANSI specified minimum length or maximum length, if desired.

MAXIMUM INTERBLOCK GAP (IBG)

The user may generate extended length IBG's by repeated Erase Gap (ERG) commands to the formatter. The user may thus exceed the ANSI specified 15 foot maximum. Upon detecting a 15 foot IBG during read operations, the formatter will halt tape motion and set REJECT status according to Section 6.

END OF RECORDING AREA

The coupler reports EOT status, but does not control or limit operations past EOT (in the End of Recording Area).

RECORDING FORMAT

The GCR recorded format is described by the diagrams and text in the remainder of this section.

Identification Burst - The GCR recording method is identified by a burst of PE recording on track 6 with all other tracks erased. The ID Burst starts at least 1.7 inches before the trailing edge of the BOT marker and continues past the BOT marker.

ARA Burst - The Automatic Read Amplification Burst is used by some drives to initialize their Dynamic Amplitude Control. The burst begins at least 1.5 inches but not farther than 4.3 inches from the leading edge of the BOT marker. The ARA Burst is written at 9042 fci and consists of the ARA ones-burst and the ARA ID burst.

ARA Ones-Burst - An undefined gap separates the ID Burst from the ARA ones-burst (all-ones in all tracks). The length of this burst is approximately 5 to 10 inches.

ARA ID Burst - The all-ones pattern continues with tracks 1,4, and 7 erased during the ID Burst. The ID Burst is approximately 2 inches long. A normal IBG follows.

IBG - The interblock gap is 0.3 inches, nominal. The IBG immediately preceeding the tape mark is 3.3 inches, nominal.

Tape Mark - The Tape Mark consists of 250 to 400 flux changes recorded at 9042 fci, with tracks 3, 6, and 9 erased.

Data Blocks - (Described in detail below.)

Preamble - Sixteen subgroups of five bytes each. The subgroups initiate the Read Circuits and synchronize them to the data coming from tape

Terminator Control Subgroup - The data pattern in this subgroup provides for long wave length inputs into the read circuits at the beginning of a Read operation. These inputs in turn ensure that the Read Detectors are turned on before they are synchronized.

The Terminator Control subgroup consists of a set of nine parallel 5-bit serial values of 10101 in all tracks located at the BOT end of each block, and 1010L at the EOT end of each block where L represents the resetting of the last character (which restores the Write Triggers to the erase state).

Second Control Subgroup - This subgroup is an important part of the synchronization process. The Second Control Subgroup consists of five bit serial values of 01111 in all tracks for the BOT end of the block and 11110 for the EOT end of the block.

Sync Control Subgroups - these are fourteen five-byte subgroups which synchronize the Read Reference Oscillator. Each subgroup consists of five-bit serial values of all ones in all tracks.

Mark 1 - This subgroup marks the coming of data. It ensures that the buffer counters are properly initiated so the data being read is formatted into the correct five-byte groups. This is necessary for correct decoding (translation from five to four bit codes) of the data which is being read. The Mark 1 control Subgroup is a set of five-bit serial values of 00111 on all tracks. During Backward operations, the Mark 1 looks like the Mark 2 Subgroup.

Data - The Data section of the tape has only data and the ECC recorded on it (no Control Subgroups). The data is divided into groups and the groups are divided into subgroups. These data subgroups are identified as data subgroup A and data subgroup B.

Data subgroup A consists of four data bytes before translation into the storage group. The same is true for data subgroup B except that it is made up of three data bytes and one ECC (Error Correction Character) before translation. The ECC is used for data correction within the eight-byte data groups (byte 8 is the ECC).

Data Values/Record Values - After the ECC is mathematically generated from the group of seven data bytes, the parity bits are also added and the resulting eight characters are divided into two groups of four characters each. During GCR recording, The four-bit pattern for each tape channel is translated into a five-bit pattern for storage on tape. These storage patterns assure that there are no more than two successive zeros in any track, a feature that provides more reliable synchronism of the read circuits. During a Read operation. the five-bit code is converted to the original four bits. Thus, the data sent to the CPU is in its original form.

Resync Burst - There may be no more than 158 contiguous data groups (1106 data bytes) in a recorded data block. Then, if there are more than six data bytes (before translation) remaining in an incoming record, a Resync Burst must be added before more data groups can be recorded. This burst is used to resynchronize the data of failing tracks when a data record is longer than 1112 bytes of data (before translation).

Mark 2 - This subgroup marks the end of data and the coming of non-data information. The Mark 2 Control Subgroup consists of a set of five-bit serial values of 11100 on all tracks. On Backward operations, the Mark 2 looks like the Mark 1 Subgroup.

End Mark - This control subgroup warns of the approach of the Residual Data Group, which is defined below. The End Mark Control Subgroup consists of one set of five-bit serial values of 11111 on all tracks.

Residual Data Group - This group is formed when there are six or fewer data bytes remaining in a data record. If six data bytes remain, the seventh byte of the Residual Data Group is the Auxiliary CRC Character (a data validity check character) and byte eight is the normal ECC. If there are fewer than six residual data bytes, pad characters of all zeros (with correct parity) are added to the data group to pad it to six bytes. (All data groups must have eight bytes total in GCR mode.) Thus, the Residual Data Group consists of remaining data bytes and/or the pad characters (H), the Auxiliary CRC Character (N) and the ECC character (E).

CRC Data Group - The CRC character has odd parity if there was an odd number of data groups and would normally have even parity if there was an even number of data groups. Since an even parity byte is not allowed in a GCR Data Group, the CRC Character must be made odd. To accomplish this, an additional pad byte consisting of all zeros and a parity bit (B) is added to the record. The addition of this byte changes the number of bytes in the CRC generation and provides an odd parity CRC Character.

The next five bytes of the CRC Data Group are identical CRC Characters. The additional CRC Characters serve to fill the CRC Data Group, since no more data will be written.

Next in the CRC Data Group is the Residual Character (X). This character is defined and used as a record data counter. (Bits 3-7 are a modulo 32 count.) These bits are used by some drives in a proprietary manner (pointers for internal data buffering in the subsystem). Bits 0-2 are used as a Modulo 7 counter to indicate how many of the Residual Data Group bytes are data bytes. The modulo 7 count of the Residual Character indicates how many data bytes are to be retrieved from the Residual Data Group.

The ECC in this data group (E), as in all other data groups, is used to verify the correctness of data in the group and to isolate any error, and to correct bad data during read operation.

Postamble - The Postamble is essentially the mirror image of the Preamble In Read Backward operations, the Postamble is used the same way the Preamble is used in Read Forward operations. (Refer to the description of the Preamble above.)

Check Characters - Three Check Characters are used in the GCR tape format: CRC (B), Auxiliary CRC (N), and ECC (E).

The CRC Characters are used to verify data validity during writing and reading operations. The ECC is used to to verify data validity and for Data Error Identification and Correction.

TAPE MARK BLOCK

The Tape Mark written is 250 to 400 flux changes (all "ones") at 9042 fci in zones 1 and 2 (physical tracks 1/4/7 and 2/5/8, respectively) and no recording in zone 3 (physical tracks 3/6/9).

A tape mark will be detected on reading if sufficient contiguous characters in either zone 1 or zone 2, in conjunction with zone 3, contain their appropriate format.

9 BITS	IBG	PRE	DATA	S	DATA	S	DATA	E	R	C	POST	IBG
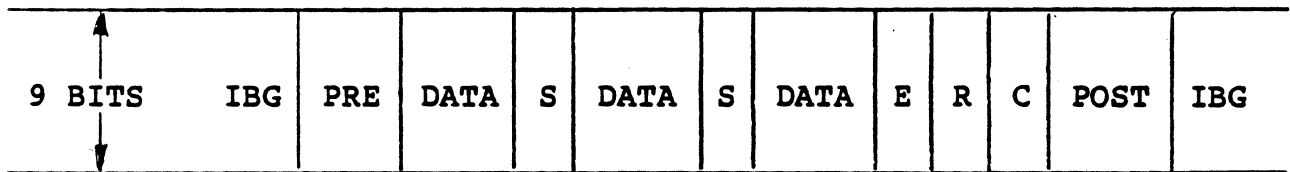
Figure 8-2   GCR Data Block Format

IBG | ◄─────────────── PREAMBLE ───────────────►

9 BITS	TERM. CONTROL SUB- GROUP 10101	SECOND CONTROL SUB- GROUP 01111	SYNC CONTROL SUB- GROUP 11111	SYNC (2)	SYNC (13)	SYNC (14)	MARK 1 CONTROL SUB- GROUP	DATA
				11	11	11111	00111	

├──── 14 SUBGROUPS-ALL 1`S ──►
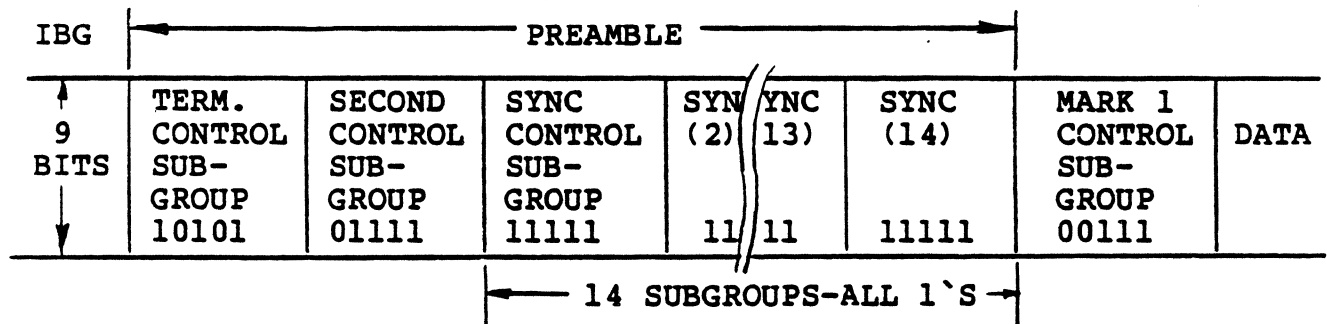
Mark 2 + Postamble (POST) is reverse image of Preamble + Mark 1

Figure 8-3   GCR Preamble and Mark 1 (PRE)

TAPE DIMENSION / Q-BUS

TAPE EDGE TOWARD TRANSPORT

| IDENT BURST | ARA BURST 1'S BURST | ID BURST | IBG | DATA BLOCK (SEE DETAILS) | TAPE MARK IBG | TAPE MARK | CHANNEL |

```
                                 //////////////////////    //////////////////////
                                 //////////////////////    //////////////////////         9  4
                                 //////////////////////    //////////////////////    //////////// 8  6
                                 //////////////////////    //////////////////////    //////////// 7  0
//////////////////////////////////////////////////////    //////////////////////                6  1
                                 //////////////////////    //////////////////////    //////////// 5  2
                                 //////////////////////    //////////////////////    //////////// 4  P
  ┌───────────┐                  //////////////////////    //////////////////////                3  3
  │ BOT MARK  │                  //////////////////////    //////////////////////    //////////// 2  7
  └───────────┘                  //////////////////////    //////////////////////    //////////// 1  5
```

REFERENCE   TAPE SHOWN   TRACK
TAPE EDGE   OXIDE SIDE UP   END OF TAPE ───►   CHANNEL
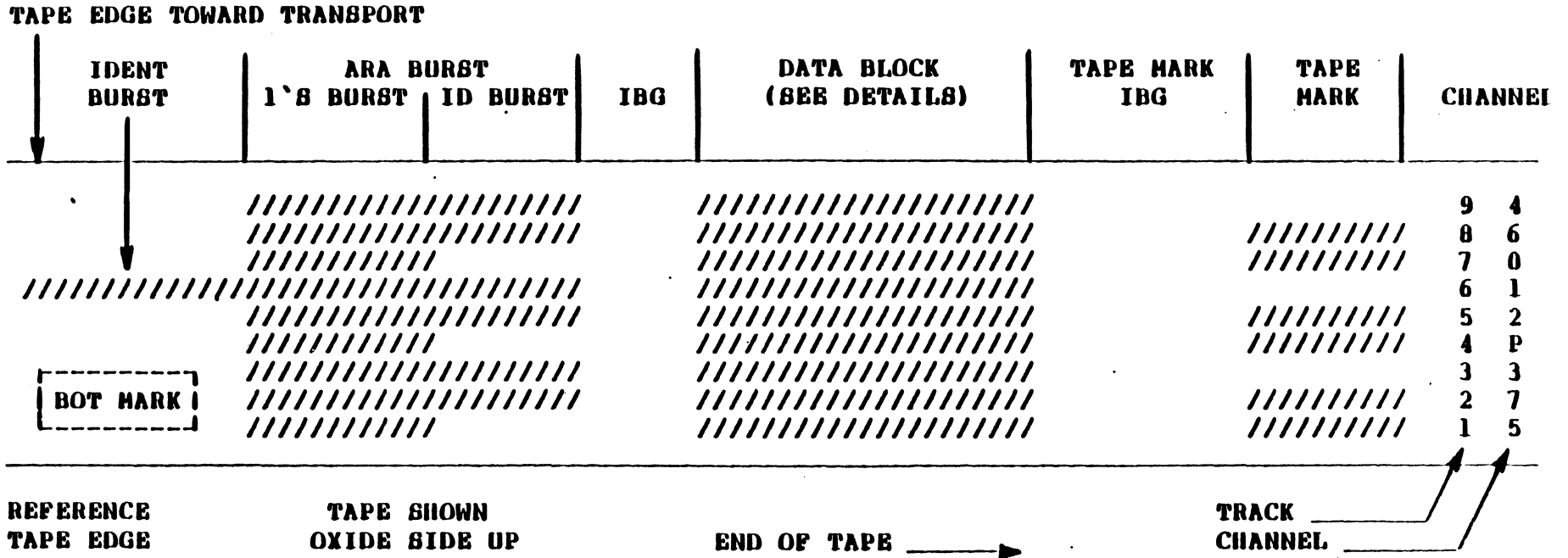
Figure 8-1   6250 BPI GCR Tape Format

←——DATA GROUP——→							
9 BITS	FIRST DATA SUB- GROUP SSSSS	SECOND DATA SUB- GROUP SSSSS	DATA GROUP 2		DATA GROUP 3		DATA GROUP 158
			SSSSS	SSSSS	SSSSS	SSSSS	SSSSS	SSSSS

```
     DDDD     DDDE
```
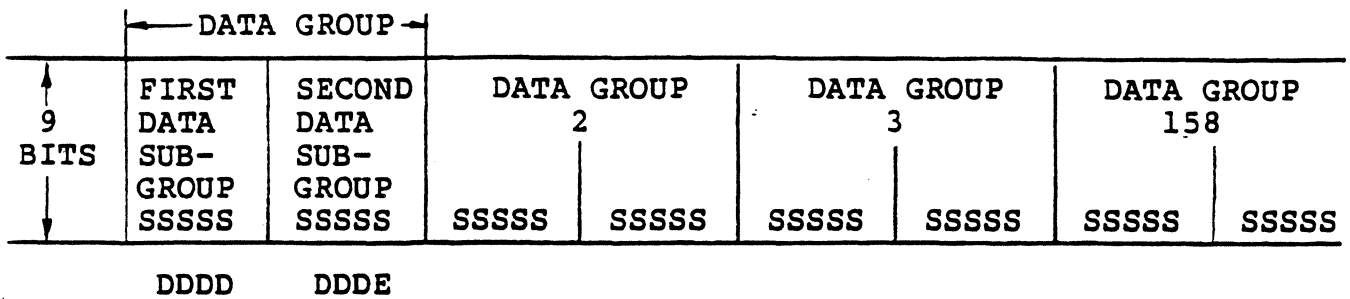
Seven data bytes + ECC are   D = Data Character
encoded into two subgroups   E = ECC Character
of ten stored (S) bytes.   S = Stored Character

Figure 8-4   GCR Data Groups (DATA)

DATA VALUES	STORAGE VALUES
0000	11001
0001	11011
0010	10010
0011	10011
0100	11101
0101	10101
0110	10110
0111	10111
1000	11010
1001	01001
1010	01010
1011	01011
1100	11110
1101	01101
1110	01110
1111	01111

Figure 8-5   Stored Data Translation

DATA	←————— RESYNC BURST —————→				DATA
9 BITS	MARK 2 CONTROL SUB- GROUP 11100	SYNC CONTROL SUB- GROUP 11111	SYNC CONTROL SUB- GROUP 11111	MARK 1 CONTROL SUB- GROUP 11100	

Figure 8-6   Resync Burst (S)

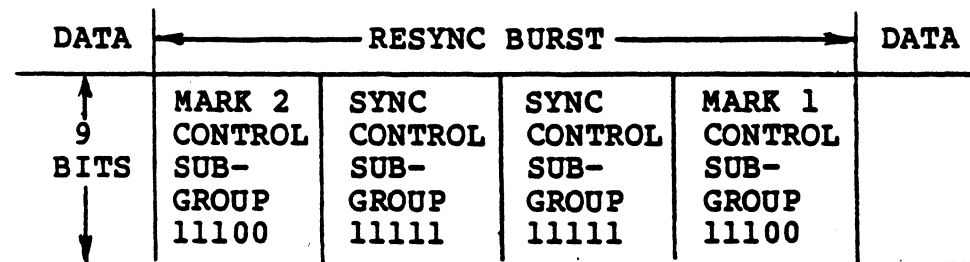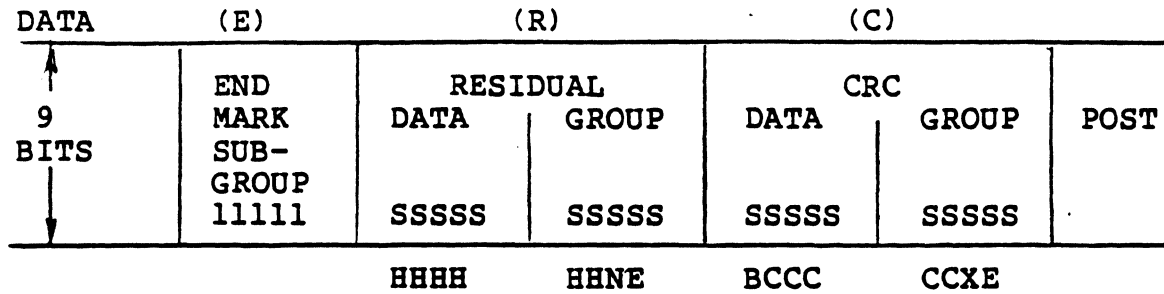| DATA	(E)	(R)		(C)		
		RESIDUAL		CRC		
↑	END	DATA	GROUP	DATA	GROUP	POST
9	MARK					
BITS	SUB-					
	GROUP					
↓	11111	SSSSS	SSSSS	SSSSS	SSSSS	.
		HHHH	HHNE	BCCC	CCXE	

H — RESIDUAL DATA OR PAD CHARACTER (ZEROS)
N — AUXILIARY CRC CHARACTER
E — ERROR CORRECTION CODE (ECC) CHARACTER
B — CRC OR PAD CHARACTER
C — CYCLIC REDUNDANCY CHECK (CRC) CHARACTER
X — RESIDUAL CHARACTER

Data/Pad/CRC/ECC are encoded into two data groups
of ten stored bytes each.

Figure 8-7   End Mark/Residual Group/CRC Group

MANUAL REVISION HISTORY

REVISION	DATE	DESCRIPTION
A	12/05/84	DOCUMENTATION RELEASE
A1	03/11/86	ADDED BURST SWITCH SETTINGS, TSV05 BOOT CODE; ADDRESSING CHANGES, MISC. CHANGES
A2	6/11/86	IMPROVED PROGRAMMING SECTION

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- -

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