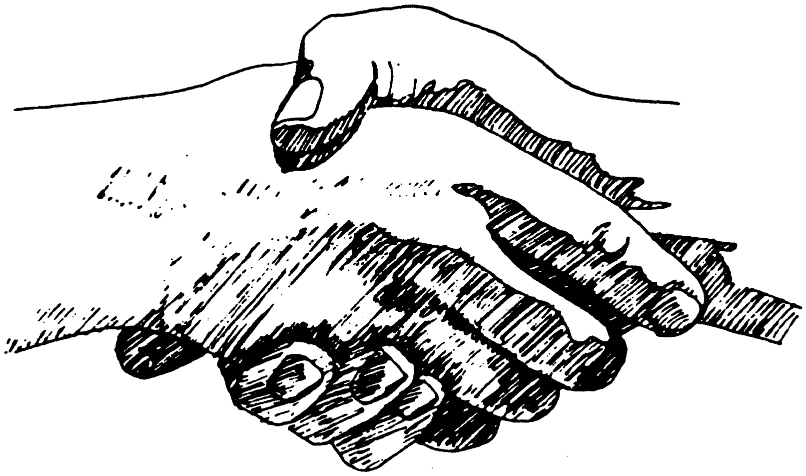
SMD - E Disk

Xylogics

Model 752
User's Manual



YOUR PARTNER FOR PERFORMANCE.

166-752-001
Revision A
June 15, 1987

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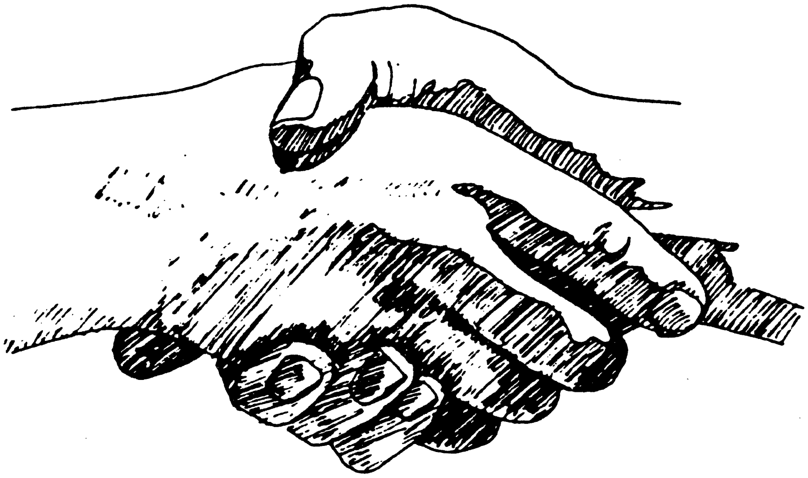

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166-752-001
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752 REVISION LEVEL HISTORY

REVISION	DESCRIPTION
A (6/15/87)	Initial release.

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SECTION 1: SPECIFICATIONS

1.0 GENERAL

The Xylogics Model 752 disk controller accommodates up to two SMD-E interface disk drives to VMEbus[1] systems using VME 9U backplanes (accepting a 15.75- by 14.44-inch board size).

1.1 USING THIS MANUAL

This manual provides two software reference cards for fast reference of the IOPB structure and codes (see insert). Section 2 describes how to install and test the 752; Section 3 describes the 752 registers; Section 4 describes the IOPBs; and Section 5 describes the 752 commands. Section 6 describes error processing; Section 7 is a programming tutorial; Section 8 explains the 752's special functions; Section 9 describes the 752 theory of operation; and Section 10 includes drive interface information.

1.1.1 Abbreviations

This manual uses the following mnemonics:

AIO	Add IOPB
AIOP	AIO Pending
AM	Address Modifier
ASR	Automatic Seek Retry
AUD	Auto-update
C450	450-Compatible Format
CHEN	Chain Enable
CRIO	Clear Remove IOPB
CRBS	Clear Register Busy
CTYP	Controller Type
DFLT	Drive Fault
DMA	Direct Memory Access
DPB	Dual Port Busy
DRA	Disable Read Ahead
DRDY	Drive Ready
EC32	32-Bit ECC
ECC	Error Correction Code
ECCM	Error Correction Mode
EDT	Enable DMA Timeout
ERRS	Error Summary
ESD	Embedded Servo Drive

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[1] VMEbus is a trademark of the VMEbus International Trade Association.

1.1.1 Abbreviations (continued)

FERR	Fatal Error
FIFO	First In/First Out Buffer
FIXD	Fixed/Removable Media
H	Notation for Hexadecimal Values
HDP	Hold Dual Port
ICS	IOPB Checksum
IOPB	Input/Output Parameter Block
MMA	Maintenance Mode Active
MM	Maintenance Mode
NPRM	Non-privileged Register Mode
ONCL	On-cylinder
OVS	Overlap Seek Enable
PNUM	Prom Number
PSEL	Priority Select
RAIO	Read Ahead IOPB
RBC	Retry Before Correction
RBS	Register Busy Semaphore
RIO	Remove IOPB
RMM	Register Maintenance Mode
ROR	Release On Request
SGM	Scatter/Gather Mode
SKER	Seek Error
TDT	Throttle Dead Time
THRO	Throttle
TMOD	Transfer Mode
WRPT	Write-protect

1.2 DESIGN RELIABILITY

Xylogics implements the following features to minimize the likelihood of product failure:

- Design for worst case voltage and temperature.
- Extensive evaluation testing.
- Low parts count through extensive use of custom LSI.
- Buffer parity for continuous error checking.
- Low-stress design on all components.
- All components burned-in.
- One card; resides in backplane or expansion chassis.
- Controller is power-cycled under thermal stress during test.

1.3 PHYSICAL

PACKAGING -- The 752 completely resides on one printed circuit board (PCB).

DIMENSIONS -- The 752 is a 3 by 3 Eurocard, measuring 14.44-inches high by 15.75-inches deep (366.7 mm by 400 mm). It is identical in form-factor to the VME triple high-triple wide PCB.

SHIPPING WEIGHT -- 5 pounds (2.3 kg).

FRONT PANEL -- Xylogics offers the 752 with an optional front panel.

CONNECTORS -- The 752 uses a 60-pin connector for the "A" cable, and two 30-pin connectors for the "B" cables. The SMD connectors are on the edge of the board facing out; they protrude through the optional face plate. The optional straight connectors do not protrude the face plate.

1.4 ENVIRONMENTAL

The 752 environmental requirements are 0 - 55°C, with a maximum relative humidity of 90% (without condensation). Air flow across the board must maintain a maximum temperature differential of 7°C to prevent hot spots.

1.5 ELECTRICAL

POWER -- The 752 uses 4.1 amperes at +5 volts DC (VDC), and 0.6 amperes at -12 VDC. The -5 volts for the differential transceivers is derived on-board.

TOLERANCE -- Voltages must be within plus or minus five percent (4.75 to 5.25; -11.4 to -12.6).

GROUNDING -- Common earth ground must be established between the disk drives and the CPU chassis, backplane, and expansion cabinets.

1.6 SYSTEM RELATED SPECIFICATIONS

DATA BUFFERING -- The 752 has a FIFO buffer that is 8K-bytes long and incorporates parity error detection. Data can be put into one end of the FIFO and simultaneously removed at the other end; there are no delays associated with filling and emptying the FIFO.

1.6 SYSTEM RELATED SPECIFICATIONS (continued)

READ AHEAD — Causes the 752 to complete an initial read and then continue reading ahead, thereby satisfying future reads with data from the FIFO.

FORMAT — The 752 Format command formats a specified number of tracks. Use the Read/Write Track Headers commands to incorporate custom interleaving schemes. Standard interleaving is 1:1; 2:1 to 15:1 interleaving is software programmable.

MEDIA DEFECTS — The 752 has several methods for remapping bad blocks. One method leaves spare sectors on each track that can slip bad sectors with Read/Write Track Headers commands. An alternate method has the spare sectors on the last part of the maximum head. The 752 also remaps entire tracks. This reduces the total number of spare sectors required with minimal affect on system performance.

READ DEFECT MAP FEATURE — The 752 can read the manufacturer's defect information directly from the unformatted disk.

STATUS LEDs — The 752 implements two status LEDs. L1 (BSY) indicates the controller is active; L2 (ERR) indicates the on-board diagnostics did not complete successfully, or an error occurred.

SCATTER/GATHER — The 752 supports Scatter/Gather on Read and Write commands. The controller can gather data from various memory locations and transfer it to the buffer for use in a Write command; it can scatter the data out from the disk drive to the appropriate memory locations with a Read command. To execute a scatter/gather, software issues a normal Read or Write command along with a DMA list that contains a memory address and the number of words to transfer to/from that location. The smallest granularity of scatter/gather is a 16-bit word.

ON-BOARD DIAGNOSTICS — The 752 runs an extensive on-board diagnostic routine upon power-up or a bus reset. If an error occurs during this test, the 752 posts the failure in a special error register.

1.6 SYSTEM RELATED SPECIFICATIONS (continued)

ERROR DETECTION AND CORRECTION — The 752 supports a 48-bit data ECC with a redundant header check; it optionally supports a 32-bit ECC on the header and data (for supporting earlier controller formats, i.e., 451). Software controls automatic detection and correction.

The 48-bit ECC detects an error burst up to 28-bits long, and corrects error bursts up to 14-bits long. The 32-bit ECC detects an error burst up to 22-bits long, and corrects error bursts up to 11-bits long, assuring data integrity.

IMPLIED SEEK CAPABILITY — Data transfer instructions contain an implied seek. Data transfers cross sector, head, and cylinder boundaries as required (spiral read/write).

OVERLAP SEEKS — The 752 supports overlap seeks. When overlap seeks are enabled, the 752 may have both drives simultaneously seeking to the appropriate cylinders.

DIAGNOSTIC SUPPORT — Comprehensive set of stand-alone diagnostics written in 'C' are available.

1.7 DISK DRIVE RELATED SPECIFICATIONS

PHYSICAL DRIVE INTERFACE — The 752 supports the Extended SMD Interface ([SMD-E]; See the Control Data Corporation (CDC) 64712402, Revision A, and Fujitsu B03P-4760-0101A).

INTERFACE DATA RATE — The 752 supports a maximum disk data rate of 2.4 megabytes per second (MBS). The 752 supports this data rate at a 1:1 interleave factor. This allows continuous data transfers, crossing sector and head boundaries with no loss of disk revolutions (assuming the controller has enough bus time to transfer the data).

MIXED DATA RATES — The 752 mixes drives with different data rates (i.e., 1.2 MBS, mixed with 1.8 MBS, or mixed with 2.4 MBS drives).

EMBEDDED SERVO DRIVES — The 752 supports embedded servo drives.

NUMBER OF DISK DRIVES — The 752 supports up to two SMD-E drives.

DISK SECTOR FORMAT — The 752 sector format includes a header field separated from a data field by a splice area.

1.7 DISK DRIVE RELATED SPECIFICATIONS (continued)

HEADER FORMAT — Header contains sector, head, cylinder address, and header ECC or a redundant header.

CABLING — The 752 uses standard SMD flat cabling or equivalent.

DUAL PORT — The 752 supports dual port drives.

1.8 VMEbus RELATED SPECIFICATIONS

VME COMPLIANCE NUMBER — IEEE P1014/D1.0.

TRANSFER MODE — Direct Memory Access (DMA).

DMA THROTTLE CONTROL -- Each time the 752 becomes bus master, it executes DMA transfers to or from system memory up to the max throttle limit or the number of words/longwords available in the FIFO buffer.

DYNA-THROTTLE — During a Read command, each time firmware executes the DMA scheduler, the 752 calculates the amount of data currently in the FIFO and DMAs from one to seven sectors to system memory. Dyna-throttle does not override the normal throttle and throttle dead time features that tune system bus activity.

DMA DATA TRANSFER RATE — The 752 has a maximum transfer rate of 18 MBS based on 30 nanoseconds (ns) memory response time (assuming longword mode transfers). Typically, the 752 transfers data at a rate of up to 10 MBS based on 200 ns memory response time (assuming longword mode transfers).

DMA DEAD TIME — The 752 supports a programmable throttle dead time between throttle bursts. This prevents the 752 from taking over the bus and allows time for other DMA devices to access the bus.

DATA TRANSFER LIMIT — Data transfer length, from 1 to 65,535 sectors with a single IOPB.

BUS COMPATIBILITY — The 752 is compatible with the standard VMEbus.

ADDRESSING CAPABILITY — The 752 supports master A32, and slave A16, as per the VMEbus Specification. As a slave, the 752 responds to address modifiers 29H and 2DH (software programmable).

1.8 VMEbus RELATED SPECIFICATIONS (continued)

DATA WIDTH -- The 752 supports D16 and D32 as per the VMEbus Specification.

RELEASE ON REQUEST -- Software programmable; the 752 releases the bus at the request of other peripheral devices.

RELEASE WHEN DONE -- The 752 releases the bus after each bus access.

BUS REQUEST LEVELS -- The 752 supports four bus request levels (jumper selectable).

EARLY RELEASE OF BUS BUSY/ -- The 752 does not support early release of Bus Busy/.

INTERRUPT PRIORITY -- Software programmable interrupt level and vector.

CONTROLLER I/O PARAMETER BLOCK (IOPB) LENGTH -- 30 bytes.

CONTROLLER REGISTERS -- Seven 8-bit I/O Registers; byte or word addressable. Only eight bits respond during word access.

1.9 SOFTWARE RELATED SPECIFICATIONS

SOFTWARE INTERFACE -- The 752 supports a high level software interface that allows host software to use the same method to add IOPBs to a chain while the controller is busy or while it is free.

1.9.1 Software Interface

The software interface includes seven byte-wide registers. Four of these bytes comprise the VME Address Register, the fifth byte is the Address Modifier Register, the sixth byte is the Control and Status Register (CSR), and the last byte is the Fatal Error Register (the 752 returns the fatal error codes in this register). The CSR includes two bits that are very important to IOPB processing: Add IOPB (AIO) and Remove IOPB (RIO).

1.9.1 Software Interface (continued)

The IOPB is a block of command and status information; it includes the disk address, the bus address, and the type of operation to be performed. The software driver sets up the IOPB in memory, sends the IOPB address to the VME Address Registers, and sets AIO. After the 752 receives the IOPB address it resets AIO. The 752 then performs the IOPB function and, upon completion or error, updates the IOPB status and sets RIO. The VME Address Registers point to the completed IOPB; the software driver reads the address and then resets RIO.

Software may add IOPBs to the queue, providing AIO is clear, by writing the IOPB address to the address registers and setting AIO (regardless of the 752's busy status).

1.10 PROGRAMMABLE FEATURES

- Software Controlled Interrupt or Polled Operations.
- Software Programmable DMA Parameters.
- Software Programmable Drive Size Parameters.
- Software Controlled Transfer Retry/Correction.

SECTION 2: INSTALLING AND TESTING THE 752

2.0 GENERAL

Section 2 describes how to unpack, configure, install, and test your 752 controller.

2.1 UNPACKING AND INSPECTION

2.1.1 Inspect the Shipping Carton

Inspect the carton for possible shipping damage. If you determine there is damage, do not unpack the unit. Notify Xylogics and the freight carrier immediately.

If no damage is visible, carefully unpack the 752. Save the carton and other packing material for possible later use.

2.1.2 Contents

The 752 is a single printed circuit board. Optional items include a manual and/or software on a floppy disk, or 1/4-inch magnetic tape cartridge.

If any items are missing or damaged, please contact Xylogics at one of the following telephone numbers.

United States:	(617) 272-8140
United Kingdom (Milton Keynes):	44-908-569444

2.1.3 Handling Precautions

Observing proper handling precautions minimizes the risk of damaging the 752 with electrostatic discharge. When transporting the 752, use an antistatic bag, antistatic bin, or the original shipping carton and packing material. Personnel handling the 752 should observe proper grounding methods including, but not limited to, wrist bands, heel straps, and antistatic mats.

2.1.4 Inspect the 752

Inspect the 752 for socketed parts that may have loosened during shipment. Make sure all parts are firmly seated in their sockets. If any parts need reinsertion, observe proper orientation.

2.2 CONFIGURING THE 752

You can configure the 752 with several jumper options. The following subsections describe these options.

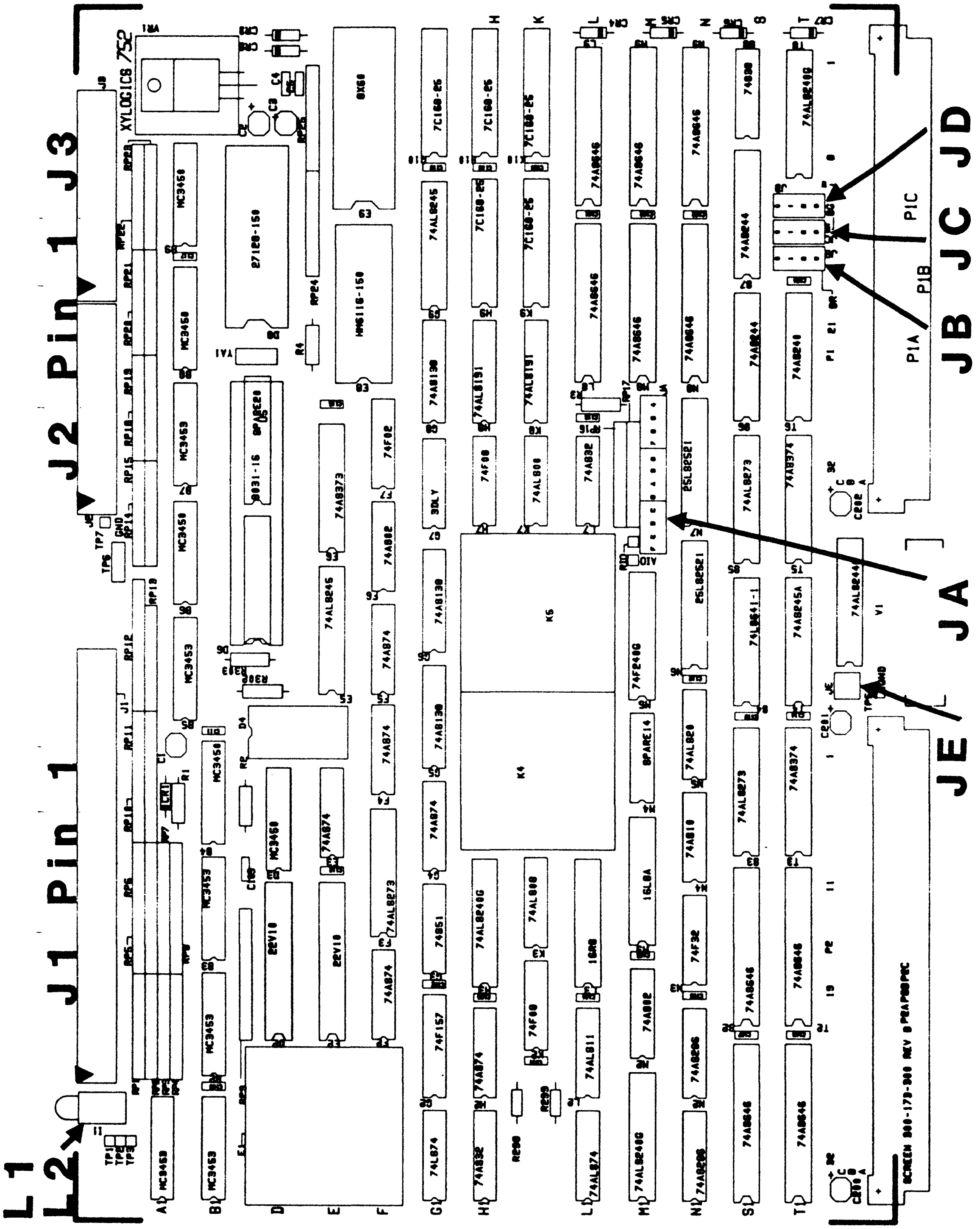
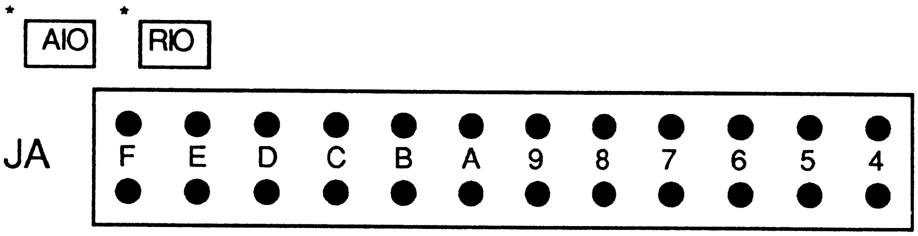


Figure 2-1. 752 - Component Location

2.2.1 Base Address Selection

Jumper block JA controls the base address. Table 2-1 shows how to set the jumpers for commonly used base addresses. Inserting a jumper makes the 752 respond to a 0 on that address line; removing a jumper makes the 752 respond to a 1. Connect the jumper between similar pin numbers on each block. (The 752 uses bits 1 through 3 to determine which register is being accessed.) The 752 is an A16 Slave, and responds to address modifier 02DH, and optionally 029H.



* These two pins are test points, not address jumpers

Figure 2-2. Base Address Jumper Block

Screen Label —>	F	E	D	C	B	A	9	8	7	6	5	4
Address:												
0100	I	I	I	I	I	I	I	O	I	I	I	I
0800	I	I	I	I	O	I	I	I	I	I	I	I
EE40*	O	O	O	I	O	O	O	I	I	O	I	I
EE80	O	O	O	I	O	O	O	I	O	I	I	I

O = Out; I = In;

* Standard Factory Configuration

Table 2-1. Base Address Selection

2.2.2 Bus Request and Bus Grant Lines

The 752 uses the Bus Request and Bus Grant lines to become bus master. In VMEbus arbitration, there are four Bus Request/Grant levels: 0 through 3. The 752 drives one Bus Request line according to the jumper scheme you choose. The arbiter drives the four Bus Grant In lines: BG0IN* through BG3IN*. If the 752 receives a Bus Grant, and is not requesting the bus, it passes the grant by driving the appropriate Bus Grant Out line: BG0OUT* through BG3OUT*.

Select a request level by jumpering one Bus Request (BR0* through BR3*), one Bus Grant In, and one Bus Grant Out line to match the selected request level. Jumper the remaining Bus Grant In/Out lines so that the incoming signal passes through the board (i.e., jumper BGxIN* to BGxOUT*, where x represents the remaining grant levels).

For example, Figure 2-3 shows the jumpering scheme for level 3 (Figure 2-3A shows the jumper blocks as they actually appear on the board; 2-3B is labeled for this example): jumper JB4 to JB8; then jumper JC4 to JC8, and JD4 to JD8. Jumper the remaining Grant levels from JC5 to JD1, JC6 to JD2, and JC7 to JD3. Factory configuration: Bus Request Level 3.

NOTE

Certain processors (i.e., Sun Microsystems) only support Bus Request Level 3.

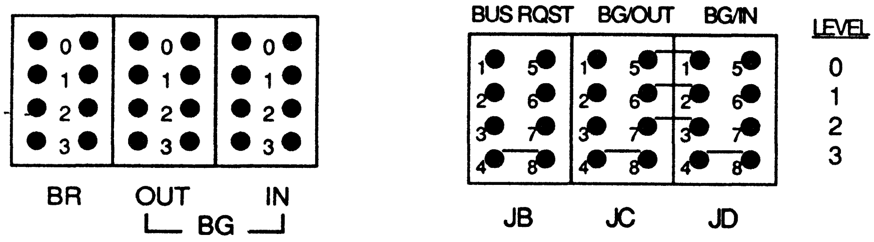


Figure 2-3A. Actual Board Layout

Figure 2-3B. Sample Jumpering Scheme

Figure 2-3. Jumpering Bus Request and Bus Grant Levels

2.2.3 Parallel Arbitration

If you are using the 752 in parallel arbitration, and the Bus Grant Out lines must be isolated from the next slot's Bus Grant In lines, remove all jumpers between JC 5-8 and JD 1-4.

2.3 MAINTENANCE MODE LOCKOUT JUMPER

Installing jumper JE 1-2 gives you unrestricted use of the maintenance mode.

When jumper JE 1-2 is removed, you may only execute the diagnostic portion of the maintenance mode. (The non-diagnostic portion of the maintenance mode is proprietary to Xylogics and subject to change without notice.)

2.4 SELF TEST DISABLE

When jumper JE 3-4 is installed, the 752 does not execute the self test on power-up.

2.5 PROMS AND PALS

Location	Part Number	Type
D8	180-002-173	EPROM
L3	181-001-015	PAL
M3	181-001-016	PAL
D2	181-001-017	PAL
E2	181-001-041	PAL

Table 2-2. PROM / PAL Part Number and Location

2.6 LIGHT EMITTING DIODES

The 752 has two light emitting diodes (LEDs). L1 (BSY) is the Busy LED; when lit, the 752 is active. L2 (ERR) is the Error LED. During power-up, L2 lights for a moment (indicating the self test is running), and goes off; if L2 stays on, a fatal error occurred.

2.7 BOARD LABELS / REVISION CONTROL

All Xylogics controllers use various revision control labels. This information is important when discussing configuration issues with us. Please familiarize yourself with your board revision levels before contacting us.

```
                 752-101-01
Product _____|   |   |
Configuration ___|   |___ Revision Level
```

Figure 2-4. Sample Part Number

2.8 PREPARING THE COMPUTER SYSTEM FOR INSTALLATION

The backplane of your system must provide a VMEbus slot for the 752. The slot must be capable of handling a bus master, and the power source must handle the power consumption of the entire system, including the 752.

2.8.1 Backplane Jumpers

Remove any jumpers that short, or cause the Interrupt Acknowledge (IACK IN/OUT) and DMA Grants (BG 0-3 IN/OUT) to bypass the slot in which you are installing the 752.

2.8.2 Card Cage Slot

The card cage must have a slot at the proper DMA priority available for the 752. The 752 uses DMA to transfer data and IOPBs. Placement of the 752 in the DMA priority chain may be critical. The amount of bus bandwidth it uses will be high at times; this may affect other boards in the system. Likewise, other boards may not allow enough time for the 752 to DMA enough data to keep up with the disk; consider this when choosing a slot. If the 752 does not get a high enough priority, then its DMA falls behind what the disk requires, and it has to wait until the next revolution before continuing the transfer. If the 752 priority is high, it gets enough DMA time, but other boards having insufficient buffers may starve from lack of DMA time. The priorities must be balanced for your system to work properly.

2.8.3 Power Considerations

The 752 affects the power consumption of the entire computer system. The 752 uses +5 volts for logic and -12 volts to provide -5 volts to power the differential drivers/receivers for the SMD interface. Be sure the power supplies can handle the entire power load. Readjust the voltages after plugging in the 752. A power supply that is just adequate may cause intermittent and unusual problems due to noise generated by occasionally going into overcurrent protection.

Limits: +5 volts (4.75 to 5.25 volts) at 4.1 amps;
-12 volts (-11.4 to -12.6 volts) at 0.6 amps.

2.9 PREPARING THE DISK DRIVE FOR INSTALLATION

Follow the manufacturer's instructions for unpacking and inspecting the disk drive.

Configure the drive for use with the 752. This entails setting up such parameters as the unit select, number of sectors per track, and ensuring the sector and index pulses are provided on the "A" cable. Consult the drive manual for the exact method of configuring your drive.

2.9.1 Drive Unit Select

A plug on the front of the drive, or switches on one of the drive's internal circuit cards, usually selects the drive unit number. The 752 accesses drives with unit numbers ranging from 0 through 7. Set the first drive to Unit 0.

2.9.2 Number of Sectors Per Track

Switches on one of the drive's internal circuit cards usually select the number of sectors per track. The 752 standard format uses 88 bytes of overhead per sector. This is a nominal number derived from the defaults set at the factory. See Section 8.2 for a more detailed description.

If you are using the sector slip feature, the number of sectors available to the program is the total number of physical sectors on the drive less the spares (see Section 8.3 for more information on media defect mapping).

Many disk drives have a runt sector (a very small sector at the end of the disk). The 752 requires that all sectors except the runt are formatted. The minimum runt size is six bytes.

2.9.3 Sector and Index Pulses

Both the "A" (Control) cable and the "B" (Radial) cable can provide the sector and index pulses. Disk vendors usually provide drives with sector and index on the "A" cable. The 752 requires the "A" cable to carry sector and index.

2.9.4 Tags 4 and 5

Some disk drives use the spare lines (see Section 10) for maintenance functions (Tag 4). Other disk drives use the spare lines for Extended Cylinder bits (Bit 10). The 752 supports both options; configure the drive for its intended use.

2.9.5 Extended Cylinder Addressing

There are two methods for addressing cylinders beyond 1023. Xylogics supports the method that uses the spare lines on the "A" cable as cylinder address bit 10. (The 752 does not support the alternate method of using the upper bits of the common interface bus and Tag 2 [Head Tag].)

2.10 INITIAL TESTS

This section relies upon your familiarity with your computer system's monitor and diagnostics.

2.10.1 Power-up and Self Test

The 752 initiates a self test upon power-up. The Error LED (L2) lights for a moment, and then goes off. If L2 remains on, the board is not functioning properly (the Fatal Error Register may indicate the nature of the problem). When L2 is on, SYSFAIL is asserted on the VMEbus. Contact Xylogics for further assistance. (Check the power supply voltages to ensure they are within limits [4.75 to 5.25 volts, and -11.4 to -12.6 volts]).

2.10.2 Drive Ready

Spin the drive up and wait for it to become ready. Issue a Read Drive Parameters command. The Drive Status byte indicates the drive status at execution time. If DRDY is clear, recheck the drive cable connections and try again. If you are still unable to get the proper status, check the -12V supply on the bus. If the problem persists, check the disk drive with an off-line tester.

2.11 DIAGNOSTICS

When you run your diagnostics:

- o Format the disk with either a diagnostic or format program.
- o Run a full pass of your diagnostic (or determine that the system is working properly).
- o Cable and test any additional drives.

SECTION 3: THE 752 REGISTERS

3.0 GENERAL

The 752 programming interface is based on the use of seven, one-byte long, I/O registers. The bus address jumpers define the base address of the register set. Table 3-1 lists the registers along with the address offset from the base address. The 752 responds to either bytes or 16-bit words; when it responds to words, only 8 bits are valid.

The registers have one function when read, and another when written. The following subsections detail their definitions.

Register	Offset
IOPB Address Byte 0 (Least Significant Byte)	1
IOPB Address Byte 1	3
IOPB Address Byte 2	5
IOPB Address Byte 3 (Most Significant Byte)	7
IOPB Address Modifier	9
Control and Status Register	B
Fatal Error Register	D

Table 3-1. Register Offsets

3.1 IOPB ADDRESS REGISTERS

The first four registers define the 32-bit address of an IOPB or IOPB chain. When these registers are written, the 752 interprets it as the address of the IOPB or IOPB chain to be executed. When read, and the Remove IOPB (RIO) bit is set, the registers point to the IOPB or IOPB chain just completed by the 752.

The protocol for reading and writing this address register is defined by the use of the Add IOPB (AIO) and Remove IOPB (RIO) bits in the Control and Status Register (see Section 3.3).

3.2 IOPB ADDRESS MODIFIER

This register defines the IOPB address modifier. Address modifiers are used for many purposes, such as memory mapping, privilege levels, and addressing range. Please consult the VMEbus Specification for more information regarding address modifiers.

3.2 IOPB ADDRESS MODIFIER (continued)

Section 3.3 defines the protocol for reading and writing this register.

```
                                     IOPB ADDRESS MODIFIER
                              ---------------------------------
                              | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
                              ---------------------------------
RESERVED _____________________|___|   |   |   |   |   |   |
ADDRESS MODIFIER _____________________|___|___|___|___|___|
```

Bit	Mnemonic	Description
7-6		RESERVED.
5-0	AM	ADDRESS MODIFIER - Most systems use the standard AM code of 3D. (See the VMEbus Specification.)

3.3 CONTROL AND STATUS REGISTER

When written, this register provides the host with control of the 752 operation; when read, it provides the host with 752 status information. Section 3.3.1 defines the bits in this register when written; Section 3.3.2 defines the bits when read.

3.3.1 Control Register (Write)

```
                                  CONTROL REGISTER  (Write)
                              ---------------------------------
                              | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
                              ---------------------------------
REGISTER MAINTENANCE MODE ____|   |   |   |   |   |   |   |
RESERVED _________________________|   |   |   |   |   |   |
ENABLE MAINTENANCE MODE ______________|   |   |   |   |   |
RESERVED _________________________________|   |   |   |   |
CONTROLLER RESET _____________________________|   |   |   |
ADD IOPB _________________________________________|   |   |
CLEAR RIO ____________________________________________|   |
CLEAR RBS ________________________________________________|
```

3.3.1 Control Register (Write) (continued)

Bit	Mnemonic	Description
7	RMM	REGISTER MAINTENANCE MODE - When RMM and MM are set, the values previously written in all the registers (except the CSR) are echoed back.
6		RESERVED.
5	MM	ENABLE MAINTENANCE MODE - Setting MM and AIO places the 752 in Maintenance mode. This mode supports a different Register protocol and is used as a diagnostic tool. Section 8 outlines the Maintenance mode.
4		RESERVED.
3	CRST	CONTROLLER RESET - CRST signals the 752 microprocessor to perform a "soft" reset; it deselects all the drives (and releases dual port), stops the DMA and disk sequencers (potentially during sector transfers), and cancels any IOPBs in the queue. When the Controller Reset completes, the 752 resets the CSR to zero. CRST does not initiate a power-up self test.

NOTE

A Controller Reset takes up to one second to complete.

Bit	Mnemonic	Description
2	AIO	ADD IOPB - When set, the 752 executes the IOPB (chain) at the address pointed to by the IOPB Address and Address Modifier Registers. As soon as the host sets AIO, the 752 sets AIO Pending (AIOP) in the Status Register (indicating the 752 has received AIO, but has not yet processed the new chain's address). AIOP is negated in the Status Register after the 752 internally stores the new (chain) address. The 752 can store up to 41 IOPB addresses in this manner. Clearing AIO if AIOP is set violates the register protocol.

3.3.1 Control Register (Write) (continued)

Bit	Mnemonic	Description
1	CRIO	CLEAR RIO - The host sets CRIO to clear RIO in the Status Register. Typically, the host sets CRIO after it reads the address of a completed IOPB chain from the IOPB Address and Modifier Registers. Clearing RIO enables the 752 to update the IOPB Address and Modifier Registers with the address and address modifier of a newly completed IOPB (chain). Clearing RIO if it is not set in the Status Register violates the register protocol.
0	CRBS	CLEAR RBS - The host sets Clear Register Busy (CRBS) to clear RBS in the Status Register. Clearing RBS releases the registers for use by another host (see Section 8.7.2). (CRBS is only relevant in a multiprocessor environment.)

3.3.2 Status Register (Read)

```
                                       STATUS REGISTER (Read)
                                  ---------------------------------
                                  | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
                                  ---------------------------------
BUSY _______________________________|   |   |   |   |   |   |   |
FATAL ERROR ____________________________|   |   |   |   |   |   |
MAINTENANCE MODE ACTIVE ____________________|   |   |   |   |   |
RESERVED _______________________________________|   |   |   |   |
CONTROLLER RESET ACTIVE ____________________________|   |   |   |
AIO PENDING ____________________________________________|   |   |
REMOVE IOPB ________________________________________________|   |
REGISTER BUSY SEMAPHORE ________________________________________|
```

Bit	Mnemonic	Description
7	BUSY	BUSY - The 752 is executing an IOPB. The 752 sets BUSY when it clears AIOP to acknowledge the first IOPB address; it clears BUSY after completing all the IOPBs with no new ones pending (within 500 microseconds of the host clearing RIO on the last IOPB). The 752 redefines this bit in Maintenance mode (see Section 8.6).

3.3.2 Status Register (Read) (continued)

Bit	Mnemonic	Description
6	FERR	FATAL ERROR - The 752 detected a fatal hardware error (a fatal error asserts SYSFAIL). A Controller Reset clears this bit. The Fatal Error Register contains more specific information. The 752 asserts FERR under the following conditions: (1) Maintenance Mode Test Failure; (2) Power-up Self Test Failure; (3) IOPB Checksum Miscompare; (4) IOPB DMA Fatal; (5) IOPB Address Alignment Error; (6) Firmware Error; (7) Illegal Maintenance Mode Test Number; and (8) ACFAIL Asserted.
5	MMA	MAINTENANCE MODE ACTIVE - When set, the 752 is in Maintenance mode (see Section 8.6).
4		RESERVED.
3	RSTA	CONTROLLER RESET ACTIVE - The host set CRST in the Control Register and the 752 is resetting itself.
2	AIOP	AIO PENDING - When set, AIO has been set in the Control Register, but the 752 has not acknowledged its receipt. When clear, AIO may be set again.
1	RIO	REMOVE IOPB - The 752 sets RIO after completing an IOPB (chain) and placing the address in the IOPB Address and Address Modifier Registers. After the host reads the address and modifier, it must clear RIO by writing Clear RIO (CRIO) in the Control Register.
0	RBS	REGISTER BUSY SEMAPHORE - RBS allows multiple hosts to share access to the 752 registers without simultaneous access (see Section 8.7.2). (RBS is only relevant in a multiprocessor environment.)

3.4 FATAL ERROR REGISTER

If a fatal error occurs, the 752 returns the appropriate Completion Code in this register. Table 3-2 lists the fatal error codes; Section 6.4 describes them.

Code	Description
E0	Reserved
E1	IRAM Self Test Failure
E2	Reserved
E3	Maintenance Test 3 Failure (DSKCEL RAM)
E4	Maintenance Test 4 Failure (Header Shift Register)
E5	Maintenance Test 5 Failure (VMEDMA Registers)
E6	Maintenance Test 6 Failure (REGCEL Chip)
E7	Maintenance Test 7 Failure (Buffer Parity)
E8	Maintenance Test 8 Failure (Disk FIFO)
E9-EF	Reserved
F0	IOPB Checksum Miscompare
F1	IOPB DMA Fatal
F2	IOPB Address Alignment Error
F3	Firmware Error
F5	Illegal Maintenance Mode Test Number
F6	ACFAIL Asserted

Table 3-2. Fatal Error Codes

SECTION 4: IOPB DESCRIPTION

4.0 GENERAL

The Input/Output Parameter Block (IOPB) passes messages between the 752 and host software: software passes the type of transfer, disk address, data address, and count to the 752; the 752 returns the transfer status and, if AUD is set or an error occurs, the ending addresses upon command completion. This section begins with the standard IOPB for most data transfer commands and follows with variations of the IOPB.

4.1 STANDARD IOPB

The 752 uses the standard IOPB for data transfer commands and some general purpose commands.

STANDARD IOPB

	7	6	5	4	3	2	1	0
00	ERRS	DONE	CHEN	SGM	COMMAND			
01	COMPLETION CODE							
02	DPB	SR	CSE	WRPT	DFLT	SKER	ONCL	DRDY
03	INTERNAL STATUS							
04	SUBFUNCTION CODE							
05	FIXD	RDP	PSEL	0		UNIT		
06	LINK LIST LENGTH					INTERRUPT LEVEL		
07	INTERRUPT VECTOR							
08	COUNT HIGH							
09	COUNT LOW							
0A	CYLINDER HIGH							
0B	CYLINDER LOW							
0C	HEAD							
0D	SECTOR							
0E	0		DATA OR LINK ADDRESS MODIFIER					
0F	0		NEXT IOPB ADDRESS MODIFIER					
10	DATA OR LINK ADDRESS HIGH							
11	DATA OR LINK ADDRESS							
12	DATA OR LINK ADDRESS							
13	DATA OR LINK ADDRESS LOW							
14	NEXT IOPB ADDRESS HIGH							
15	NEXT IOPB ADDRESS							
16	NEXT IOPB ADDRESS							
17	NEXT IOPB ADDRESS LOW							
18	IOPB CHECKSUM HIGH							
19	IOPB CHECKSUM LOW							

4.1.1 IOPB Byte 0 (Command)

```
                                   --------------------------------
                                   | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
                                   --------------------------------
ERROR SUMMARY ___________________|   |   |   |   |   |   |   |
DONE __________________________________|   |   |   |   |   |   |
CHAIN ENABLE _______________________________|   |   |   |   |   |
SCATTER/GATHER ___________________________________|   |   |   |   |
COMMAND __________________________________________|___|___|___|___|
```

Bit	Mnemonic	Description
7	ERRS	ERROR SUMMARY - ERRS is only valid if DONE is set. When set, a hard or soft error occurred during IOPB processing. When clear, the 752 successfully completed the IOPB. **NOTE** Clear DONE and ERRS before executing an IOPB.
6	DONE	DONE - When set, the IOPB is complete; if chained, software may remove the IOPB from the chain and reuse it.
5	CHEN	CHAIN ENABLE - When set, the Next IOPB Address Modifier and Next IOPB Address point to the next chained IOPB. When clear, this IOPB is not chained to another IOPB. The 752 always returns one IOPB at a time.
4	SGM	SCATTER/GATHER MODE - When set, the IOPB is either a scatter (read) or a gather (write) transfer; a linked list describes the number of 16-bit words and to what address the 752 transfers each section of the data. The link address modifier and the link address specify the link list location. When clear, this IOPB specifies the data transfer address; the data is transferred to/from contiguous memory. SGM is only valid for standard reads and writes.
3-0	COMM	COMMAND - See Table 4-2.

4.1.2 IOPB Byte 1 (Status Byte 1)

After the 752 executes the IOPB, it sets DONE and posts a Completion Code in this byte. Completion Codes are only valid if DONE is set. A code of 0x indicates a successful completion; any other value indicates an error occurred (see Section 6).

4.1.3 IOPB Byte 2 (Status Byte 2)

IOPB Byte 2 is the Disk Status byte; it is only valid if DONE is set. Byte 2 (excluding bits 5 and 6) is read from the drive selected by this IOPB.

```
                                 ---------------------------------
                                 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
                                 ---------------------------------
DUAL PORT BUSY ___________________|   |   |   |   |   |   |   |
SLIPPED REVOLUTION ___________________|   |   |   |   |   |   |
COUNT SECTORS EXECUTED ___________________|   |   |   |   |   |
WRITE-PROTECT ________________________________|   |   |   |   |
DISK FAULT _______________________________________|   |   |   |
SEEK ERROR ___________________________________________|   |   |
ON-CYLINDER __________________________________________________|   |
DRIVE READY ______________________________________________________|
```

Bit	Mnemonic	Description
7	DPB	DUAL PORT BUSY - Sets if the selected port in a dual ported drive is busy.
6	SR	SLIPPED REVOLUTION - Sets if the 752 is unable to DMA enough data to keep up with the disk; it waits until the sector comes around on the next revolution.
5	CSE	COUNT SECTORS EXECUTED - Sets if the current sector count is invalid and the 752 has to recount the sectors.
4	WRPT	WRITE-PROTECT - Sets if the selected drive is write-protected.
3	DFLT	DISK FAULT - Sets if a fault condition exists in the selected drive.

4.1.3 IOPB Byte 2 (Status Byte 2) (continued)

Bit	Mnemonic	Description
2	SKER	SEEK ERROR - Sets if the 752 selects a cylinder higher than the drive maximum, or a seek does not complete within 500 milliseconds.
1	ONCL	ON-CYLINDER - The 752 sets ONCL when the selected drive is on-cylinder.
0	DRDY	DRIVE READY - The 752 sets DRDY when the last drive selected is ready.

4.1.4 IOPB Byte 3 (Status Byte 3)

IOPB Byte 3 is reserved. It reflects the 752's internal status.

4.1.5 IOPB Byte 4 (Subfunction)

IOPB Byte 4 is the Subfunction byte. Subfunction Codes follow a convention that indicates whether the code is generic to all VME controllers, generic to a group of controllers (i.e., 772, 712, 751, 752, 7053, etc.), or specific to a particular controller. See Table 4-1.

The 752 combines standard Command Codes with Subfunction Codes to define the required operation. Table 4-2 lists the 752 Command and Subfunction Codes.

Subfunction Codes (Hex)	Class
00-1F	Generic to All
20-3F	Generic Tape
40-5F	772-Specific
60-7F	Reserved
80-9F	Generic Disk
A0-AF	751-, 752-, and 7053-Specific
B0-BF	712-Specific
C0-FF	Reserved

Table 4-1. Subfunction Code Classes

4.1.5 IOPB Byte 4 (Subfunction) (continued)

Code	Command	Subfunction	Description
0	NOP	00	No Operation
1	WRITE	00	Normal Write
2	READ	00	Normal Read
3	SEEK	00	Report Current Address
		01	Seek and Report Current Address
		02	Start Seek and Report Completion Immediately
4	DRIVE RESET	00	Drive Reset
5	WRITE PARAMETERS	00	Write Controller Prmtrs.
		80	Write Drive Parameters
		81	Write Format Parameters
6	READ PARAMETERS	00	Read Controller Prmtrs.
		80	Read Drive Parameters
		81	Read Format Parameters
		A0	Read Drive Status Xtnd.
7	EXTENDED WRITE	80	Write Track Headers
		81	Write Format
		82	Write Header, Header Verify, Data, and Data ECC
		A0	Write Defect Map
		A1	Write Defect Map Xtnd.
8	EXTENDED READ	80	Read Track Headers
		81	Verify Data
		82	Read Header, Header Verify, Data, and Data ECC
		A0	Read Defect Map
		A1	Read Defect Map Extended
9	DIAGNOSTICS	00	Self Test
A-F	RESERVED		

Table 4-2. Command/Subfunction Codes

4.1.6 IOPB Byte 5 (Unit)

```
                                        ---------------------------------
                                        | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
                                        ---------------------------------
FIXED/REMOVABLE MEDIA ____________________|   |   |   |   |   |   |   |
RELEASE DUAL PORT ____________________________|   |   |   |   |   |   |
PRIORITY SELECT __________________________________|   |   |   |   |   |
RESERVED _____________________________________________|___|   |   |   |
UNIT NUMBER __________________________________________________|___|___|
```

Bit	Mnemonic	Description
7	FIXD	FIXED/REMOVABLE MEDIA - When set, the 752 is accessing the fixed media portion of a disk drive. When clear, the 752 is accessing the removable media portion of a drive. This bit allows you to treat a fixed/removable drive as two separate disk drives. See Section 8.12.
6	RDP	RELEASE DUAL PORT - This bit is specifically used with dual ported disk drives. When set, the 752 releases the disk drive's port when it completes a command. When clear, the 752 does not release the disk drive's port when it completes a command. See Section 8.14.
5	PSEL	PRIORITY SELECT - When set, it forces the selection of a dual port drive. See Section 8.14.
4-3		RESERVED.
2-0	UNIT	UNIT NUMBER - This value specifies the Unit Number of the attached drive to which the transfer is directed (in the range of 0 to 7).

NOTE

Depending on the command, Bytes 6 through 13 have different definitions (see Sections 4.2 through 4.4).

4.1.7 IOPB Byte 6 (Interrupt Level)

```
                                  ---------------------------------
                                  | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
                                  ---------------------------------
LINK LIST LENGTH _________________|___|___|___|___|___|   |   |   |
INTERRUPT LEVEL __________________________________________|___|___|
```

Bit	Mnemonic	Description
7-3	LLL	LINK LIST LENGTH - Bits 3-7 specify the length, in elements, of a linked list for Scatter/ Gather commands. Each element refers to an 8-byte block in the linked list. See Table 8-2.
2-0	INTL	INTERRUPT LEVEL - The 752 uses these bits as the VMEbus hardware interrupt level when it completes the IOPB. The 752 will not interrupt if bits 0 through 2 are clear.

4.1.8 IOPB Byte 7 (Interrupt Vector)

IOPB Byte 7 determines the interrupt vector that the 752 uses upon command completion. This byte is not valid if the interrupt level is zero.

4.1.9 IOPB Bytes 8 and 9 (Count)

Byte 8 is Count High; Byte 9 is Count Low. These bytes specify the number of sectors to be transferred in a data transfer IOPB. The format command uses this count to determine the number of tracks to format.

4.1.10 IOPB Bytes A and B (Cylinder)

Byte A is Cylinder High; Byte B is Cylinder Low. These bytes specify the starting cylinder address for a transfer.

4.1.11 IOPB Byte C (Head)

IOPB Byte C specifies the starting head number for a transfer.

4.1.12 IOPB Byte D (Sector)

IOPB Byte D specifies the starting sector number for a transfer.

4.1.13 IOPB Byte E (Data or Link Address Modifier)

```
                                 ---------------------------------
                                 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
                                 ---------------------------------
RESERVED ________________________|___|   |   |   |   |   |   |   |
DATA OR LINK ADDRESS MODIFIER ___________|___|___|___|___|___|___|
```

Bit	Description
7-6	RESERVED.
5-0	DATA OR LINK ADDRESS MODIFIER - If SGM is set, this field specifies the Link List Address Modifier; if SGM is clear, this field specifies the Data Address Modifier. The 752 uses these modifiers to complete the address.

4.1.14 IOPB Byte F (Next IOPB Address Modifier)

```
                                 ---------------------------------
                                 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
                                 ---------------------------------
RESERVED ________________________|___|   |   |   |   |   |   |   |
NEXT IOPB ADDRESS MODIFIER ______________|___|___|___|___|___|___|
```

Bit	Mnemonic	Description
7-6		RESERVED.
5-0		NEXT IOPB ADDRESS MODIFIER - If CHEN is set, the Next IOPB Address Modifier, along with the Next IOPB Address, point to the next IOPB in the chain. If CHEN is set, the 752 ignores this byte.

4.1.15 IOPB Bytes 10 through 13 (DMA Data Address)

IOPB Byte 10 is DMA Data Address High; Byte 13 is DMA Data Address Low. These bytes comprise the data or link list address pointers. The 752 uses these bytes with the data or link list address modifier to point to the data or linked list address. If SGM is set, this address points to the linked list; if SGM is clear, this address points to the data address. **(The link list address must be on a 16-bit word boundary.)**

4.1.16 IOPB Bytes 14 through 17 (Next IOPB Address)

IOPB Byte 14 is Next IOPB Address High; Byte 17 is Next IOPB Address Low. These bytes comprise the Next IOPB Address pointers. The 752 uses these bytes with the Next IOPB Address modifier to point to the next IOPB in the chain (if CHEN is set in Byte 0). **(The Next IOPB address must be on a 16-bit word boundary.)**

4.1.17 IOPB Bytes 18 and 19 (IOPB Checksum)

Byte 18 is IOPB Checksum High; Byte 19 is IOPB Checksum Low. The 752 calculates the checksum by adding the IOPB bytes and comparing the value against the value software calculated and put in these bytes. See Section 8.15.

4.1.18 IOPB Bytes 1A and 1B (ECC Pattern Word)

Byte 1A is ECC Pattern Word High; Byte 1B is ECC Pattern Word Low. These bytes are required for ECC Mode 0 and may be required for Mode 2 (see Section 6.4).

4.1.19 IOPB Bytes 1C and 1D (ECC Offset Word)

Byte 1C is ECC Offset Word High; Byte 1D is ECC Offset Word Low. These bytes are required for ECC Mode 0 and may be required for Mode 2 (see Section 6.4).

4.2 CONTROLLER PARAMETERS IOPB

This IOPB sets and reads various controller parameters. The 752 uses the standard IOPB, but redefines bits in Bytes 8 through E, and 10 through 13.

CONTROLLER PARAMETERS

	7	6	5	4	3	2	1	0
00	ERRS	DONE	CHEN	SGM	COMMAND			
01	COMPLETION CODE							
02	DPB	SR	CSE	WRPT	DFLT	SKER	ONCL	DRDY
03	INTERNAL STATUS							
04	SUBFUNCTION CODE							
05	0					UNIT		
06	0					INTERRUPT LEVEL		
07	INTERRUPT VECTOR							
08	AUD	TMOD	DACF	ICS	EDT	NPRM	0	
09	TDT		0	ROR	0			DRA
0A	OVS	0		ASR	0	RBC	ECCM	
0B	THROTTLE							
0C	EPROM RELEASE LEVEL							
0D	0							
0E	CONTROLLER TYPE							
0F	0		NEXT IOPB ADDRESS MODIFIER					
10	EPROM PART NUMBER HIGH							
11	EPROM PART NUMBER LOW							
12	EPROM REVISION LEVEL							
13	0							
14	NEXT IOPB ADDRESS HIGH							
15	NEXT IOPB ADDRESS							
16	NEXT IOPB ADDRESS							
17	NEXT IOPB ADDRESS LOW							
18	IOPB CHECKSUM HIGH							
19	IOPB CHECKSUM LOW							

4.2.1 IOPB Byte 8 (Controller Parameters A)

```
                                  ---------------------------------
                                  | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
                                  ---------------------------------
AUTO-UPDATE ______________________|   |   |   |   |   |   |   |
TRANSFER MODE ________________________|   |   |   |   |   |   |
DISABLE ACFAIL ___________________________|   |   |   |   |   |
IOPB CHECKSUM ________________________________|   |   |   |   |
ENABLE DMA TIMEOUT ___________________________________|   |   |
NON-PRIVILEGED REGISTER MODE _____________________________|   |
RESERVED ______________________________________________________|___|
```

4.2.1 IOPB Byte 8 (Controller Parameters A) (continued)

Bit	Mnemonic	Description
7	AUD	AUTO-UPDATE - When set, the 752 updates the IOPB to the transfer's ending parameters; it updates the disk address, the sector count, and the data address after completing the transfer or detecting an error. When clear, the 752 only updates the IOPB if an error occurs. The values are then set up so that host software can tell the 752 to continue (the values should point to the sector in error, the correct remaining sector count, and proper data address).
6	TMOD	TRANSFER MODE - When set, the 752 executes data transfers in Longword mode. When clear, it executes transfers in Word mode. (IOPB transfers are always in Word mode.) If a transfer starts on an improper address boundary, the 752 first transfers a byte and/or a word, as necessary to align boundaries, and continues the transfer in the selected mode. The 752 may end the transfer with a byte and/or word.
5	DACF	DISABLE ACFAIL — When set, the 752 ignores the ACFAIL line on the VMEbus.
4	ICS	IOPB CHECKSUM - When set, the 752 reads the IOPB, compares the checksum it generated during the read with the checksum the software driver appended to the IOPB. The 752 also updates the Checksum bytes in any IOPB if AUD is set. Clearing ICS disables this feature. See Section 8.15. NOTE Since this feature adds at least 100 microseconds to each transfer, it effects the 752's performance.
3	EDT	ENABLE DMA TIMEOUT - When set, the 752 enables a DMA bus error timer. When clear, the 752 relies on an external VMEbus transfer timer.

4.2.1 IOPB Byte 8 (Controller Parameters A) (continued)

Bit	Mnemonic	Description
2	NPRM	NON-PRIVILEGED REGISTER MODE - When set, the 752 responds to address modifiers 2DH and 29H. When clear, the 752 only responds to 2DH. (See the VMEbus Specification for more information on address modifiers.)
1-0		RESERVED.

4.2.2 IOPB Byte 9 (Controller Parameters B)

```
                                      ---------------------------------
                                      | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
                                      ---------------------------------
THROTTLE DEAD TIME _____________________|___|   |   |   |   |   |   |
RESERVED _______________________________________|   |   |   |   |   |
RELEASE ON REQUEST _________________________________|   |   |   |   |
RESERVED _______________________________________________|___|___|   |
DISABLE READ AHEAD _________________________________________________|
```

Bit	Mnemonic	Description
7-6	TDT	THROTTLE DEAD TIME - TDT selects one of four minimum time periods that determines the time the 752 remains off the bus between throttle bursts (see Section 8.10).
5		RESERVED.
4	ROR	RELEASE ON REQUEST - When set, the 752 releases the bus at the request of other bus masters; otherwise, it continues with the next throttle burst. The 752 monitors the bus request lines and releases bus busy only if another bus request is pending. It completes its specified throttle burst before releasing the bus due to a pending request. When clear, the 752 releases the bus at the end of each throttle burst and rearbitrates if more data transfers are pending. See Section 8.16.
3-1		RESERVED.
0	DRA	DISABLE READ AHEAD - When set, the 752 disables its read ahead feature. When clear, the 752 satisfies all subsequent reads with data from the read ahead buffer (if possible).

4.2.3 IOPB Byte A (Controller Parameters C)

```
                               ---------------------------------
                               | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
                               ---------------------------------
ENABLE OVERLAP SEEKS ____________|   |   |   |   |   |   |   |
RESERVED ____________________________|___|   |   |   |   |   |
AUTOMATIC SEEK RETRY ________________________|   |   |   |   |
RESERVED ________________________________________|   |   |   |
RETRY BEFORE CORRECTION _____________________________|   |   |
ERROR CORRECTION MODE ___________________________________|___|
```

Bit	Mnemonic	Description
7	OVS	ENABLE OVERLAP SEEKS - When set, the 752 initiates overlap seeks if more than one drive is present. When clear, the controller does not initiate Overlap Seek operations.
6-5		RESERVED.
4	ASR	AUTOMATIC SEEK RETRY - When set, the 752 resets the drive, seeks to the commanded cylinder and retries the transfer up to two times on any of the following errors: Seek, Header Error/Cylinder, Header Error/Head, Drive Not On-cylinder, and Drive Faulted.
3		RESERVED.
2	RBC	RETRY BEFORE CORRECTION - When set, the 752 retries the operation once on an ECC error without calculating the error syndrome. If an error occurs, on the second try, the 752 reverts to the specified error correction mode.
1-0	ECCM	ERROR CORRECTION MODE - There are three Error Correction modes. Mode 0 stops a transfer and provides the driver with the error's offset and pattern. The driver performs the actual correction. Mode 1 flags an error and continues the transfer. Mode 2 performs the correction in host memory, flags a soft error, and continues the transfer.

4.2.4 IOPB Byte B (Controller Parameters D)

Bits 0 through 7 are the Throttle (THRO) bits. The throttle is the maximum number of transfers allowed each time the 752 becomes bus master. The throttle value determines the maximum DMA burst length for both data and IOPB DMA transfers. This byte allows a throttle setting from 1 to 256.

Value	Weight
0	256
1	1
2	2
3	3
:	:
255	255

Table 4-3. Throttle Values

4.2.5 IOPB Byte C (EPROM Release Level)

The 752 returns the EPROM release level on a Read Controller Parameters command.

4.2.6 IOPB Byte E (Controller Type)

IOPB Byte E is the Controller Type byte. Xylogics assigns each VME controller a unique controller type code.

Controller	Code (H)	
712	12	(ESDI Disk Controller)
772	72	(Pertec Tape Controller)
752	52	(SMD Controller)

Table 4-4. Controller Type Codes

4.2.7 IOPB Bytes 10 and 11 (EPROM Part Number)

The 752 returns a portion of the EPROM part number on a Read Controller Parameters command. The 4 nibbles in these 2 bytes refer to the part number's last 4 digits. For example, if the part number is 180-002-173, Byte 10 holds 21H and Byte 11 holds 73H.

4.2.8 IOPB Byte 12 (EPROM Revision Level)

This byte contains the revision level of the EPROM plugged into the board.

4.3 DRIVE PARAMETERS IOPB

DRIVE PARAMETERS

	7	6	5	4	3	2	1	0
00	ERRS	DONE	CHEN	0	COMMAND			
01	COMPLETION CODE							
02	DPB	SR	CSE	WPRT	DFLT	SKER	ONCL	DRDY
03	INTERNAL STATUS							
04	SUBFUNCTION CODE							
05	FIXD	RDP	PSEL	0		UNIT		
06	0		C450	EC32	0	INTERRUPT LEVEL		
07	INTERRUPT VECTOR							
08	MAX SECTOR LH							
09	HEAD OFFSET							
0A	MAX CYLINDER HIGH							
0B	MAX CYLINDER LOW							
0C	MAX HEAD							
0D	MAX SECTOR							
0E	SECTORS PER TRACK (RD. DR. PRM.) = 200 H							
0F	0		NEXT IOPB ADDRESS MODIFIER					
10	0							
11	0							
12	0							
13	0							
14	NEXT IOPB ADDRESS HIGH							
15	NEXT IOPB ADDRESS							
16	NEXT IOPB ADDRESS							
17	NEXT IOPB ADDRESS LOW							
18	IOPB CHECKSUM HIGH							
19	IOPB CHECKSUM LOW							

4.3.1 IOPB Byte 6 (Drive Parameters)

```
                               ---------------------------------
                               | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
                               ---------------------------------
RESERVED ________________________|___|   |   |   |   |   |   |
450-COMPATIBLE MODE _____________________|   |   |   |   |   |
32-BIT ERROR CORRECTION CODE ________________|   |   |   |   |
RESERVED ________________________________________|   |   |   |
INTERRUPT LEVEL _____________________________________|___|___|
```

Bit	Mnemonic	Description
7-6		RESERVED.
5	C450	450-COMPATIBLE MODE - When set, the 752 reads and writes 450-compatible format disks. The format is compatible with disks having less than 64-sectors per track. The 752 ignores the Drive Type field in the 450 header; it does not format in 450-Compatible mode. C450 does not override the format parameters set in the 752. EC32 must be set.

NOTE

Using C450, and EC32 in different modes on the two connecting disks reduces the disk subsystem's performance. The 752 must modify the disk sequencer code each time it switches drives.

C450 only allows word boundary transfers since it swaps data bytes as DMAed to memory.

Bit	Mnemonic	Description
4	EC32	32-BIT ECC - When set, the 752 uses a 32-bit ECC on the header and data. When clear, it uses a redundant header check, and a 48-bit data ECC. EC32 must be set when using the 450-compatible mode. **(See the note below bit 5.)**
3		RESERVED.
2-0	INTL	INTERRUPT LEVEL - See Section 4.1.7.

4.3.2 IOPB Byte 8 (Max Sector/Last Head)

IOPB Byte 8 specifies the max sector value on the last head for use in cylinder sparing (this value is zero-based). Bytes 0DH and 08H must be equal if cylinder sparing is not used. See Section 8.3.2.

4.3.3 IOPB Byte 9 (Head Offset)

IOPB Byte 9 specifies the drive's head offset value. Use zero for non-fixed/removable drives. Section 8.12 explains using the head offset to access fixed/removable drives.

4.3.4 IOPB Bytes A and B (Max Cylinder)

IOPB Byte A is Max Cylinder High; Byte B is Max Cylinder Low. These bytes specify the drive's max cylinder value. This value is zero-based, i.e., the max cylinder on an 823 cylinder drive is 822.

4.3.5 IOPB Byte C (Max Head)

IOPB Byte C specifies the drive's max head value. This value is zero-based.

4.3.6 IOPB Byte D (Max Sector)

IOPB Byte D specifies the drive's max sector value. This value is zero-based. See Section 8.3.

4.3.7 IOPB Byte E (Sectors Per Track)

IOPB Byte E returns the number of sectors per track (the 752 determines this value by counting the sector pulses from the drive) on a Read Drive Parameters command. This is the actual number of sectors; it has not been modified to be zero-based. This value does not include a runt sector (only one per track).

The Format command uses this count to determine the number of sectors to format. Normal Read and Write commands use this count to limit the number of header compares before a Header Not Found error occurs.

4.4 FORMAT PARAMETERS IOPB

FORMAT PARAMETERS

	7	6	5	4	3	2	1	0
00	ERRS	DONE	CHEN	SGM	COMMAND			
01	COMPLETION CODE							
02	DPB	SR	CSE	WPRT	DFLT	SKER	ONCL	DRDY
03	INTERNAL STATUS							
04	SUBFUNCTION CODE							
05	FIXD	0				UNIT		
06	INTERLEAVE				0	INTERRUPT LEVEL		
07	INTERRUPT VECTOR							
08	FIELD 1							
09	FIELD 2							
0A	FIELD 3							
0B	FIELD 4							
0C	BYTES PER SECTOR HIGH							
0D	BYTES PER SECTOR LOW							
0E	0							
0F	0		NEXT IOPB ADDRESS MODIFIER					
10	FIELD 6							
11	FIELD 7							
12	0							
13	0							
14	NEXT IOPB ADDRESS HIGH							
15	NEXT IOPB ADDRESS							
16	NEXT IOPB ADDRESS							
17	NEXT IOPB ADDRESS LOW							
18	IOPB CHECKSUM HIGH							
19	IOPB CHECKSUM LOW							

4.4.1 IOPB Byte 6 (Interleave)

```
                                   ---------------------------------
                                   | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
                                   ---------------------------------
INTERLEAVE FACTOR __________________|___|___|___|   |   |   |   |
RESERVED ___________________________________________|   |   |   |
INTERRUPT LEVEL ________________________________________|___|___|
```

4.4.1 IOPB Byte 6 (Interleave) (continued)

Bit	Mnemonic	Description
7-4	INTF	INTERLEAVE FACTOR - The 752 uses INTF during format operations. For 1:1 interleaving, the interleave factor is zero. The interleave factor for other ratios is (n+1):1, where n is the interleave factor.
3		RESERVED.
2-0	INTL	INTERRUPT LEVEL - See Section 4.1.7.

Interleave Factor Bits 7-4	Ratio
0	1:1
1	2:1
2	3:1
:	:
F	16:1

Table 4-5. Interleave Factors

4.4.2 IOPB Byte 8 (Field 1)

Field 1 is the number of bytes from one byte after the index or sector pulse to when the 752 enables the Read Gate for headers; this value must be greater than or equal to one (Xylogics recommends using one). See the note below Section 4.4.3.

4.4.3 IOPB Byte 9 (Field 2)

Field 2 is the number of bytes from when the 752 enables the Read Gate to when it starts looking for the Header Sync byte. Field 2 must equal a non-zero value (Xylogics recommends 0AH).

NOTE

The combined value of Fields 1 and 2 must not exceed 255.

4.4.4 IOPB Byte A (Field 3)

Field 3 is the number of bytes from the sector pulse to the Header Sync byte; this value must be greater than or equal to the sum of Field 1 plus Field 2 (Xylogics recommends 1BH).

4.4.5 IOPB Byte B (Field 4)

Field 4 is the number of bytes between the Header ECC and the Data Sync byte; this value must be larger than 11 (Xylogics recommends 14H).

NOTE

> Field 4 is actually four bits longer than this byte specifies. The 752 uses the extra four bits to test for a successful header compare and header verify.

4.4.6 IOPB Bytes C and D (Bytes Per Sector High/Low)

Byte C specifies Bytes Per Sector High; Byte D specifies Bytes Per Sector Low. The sector size (in bytes) must be larger than 254, even, and smaller than 3073.

4.4.7 IOPB Byte 10 (Field 6)

Field 6 is the number of bytes from enabling Read Gate to when the 752 starts looking for data sync; this value must be larger than nine (Xylogics recommends 0AH).

4.4.8 IOPB Byte 11 (Field 7)

Field 7 is the number of bytes the Write Gate remains on after the Data ECC; this value must be greater than or equal to one (Xylogics recommends three).

SECTION 5: COMMANDS

5.0 GENERAL

Each disk command begins a new page. An IOPB diagram follows each command description. The diagrams are highlighted to indicate which fields the 752 absolutely requires for command execution, which fields are optional for the command, and which fields it returns after execution.

Each 752 IOPB is 30-bytes long. Reserving all 30 bytes for each IOPB maintains IOPB integrity. Generally, all commands use Bytes 0 through 19H (Bytes 1AH through 1DH are reserved).

5.0.1 Setting Up the Command

Each IOPB diagram indicates the bytes or fields that must be set for each operation. Certain parameters are essential; others are optional. All commands require the Command, Unit, and Interrupt Level fields to contain valid information. The Interrupt Vector field must be valid if the Interrupt Level is not zero.

5.0.2 Completing the Command

After the 752 completes the command, it updates IOPB Bytes 0 through 3 with ERRS, DONE, a Completion Code, and an internal status. The 752 only updates the entire IOPB if Auto-update (AUD) is enabled, an error occurs, or if Read Parameters or Read Extended Status commands are executed. If AUD is set, and no errors occur, the 752 sets DONE, posts a Completion Code of zero in Byte 1, and disk drive status information in Byte 2; for any command that DMAs data to/from memory, the 752 updates the data and disk addresses to point to the last address plus one of the transfer.

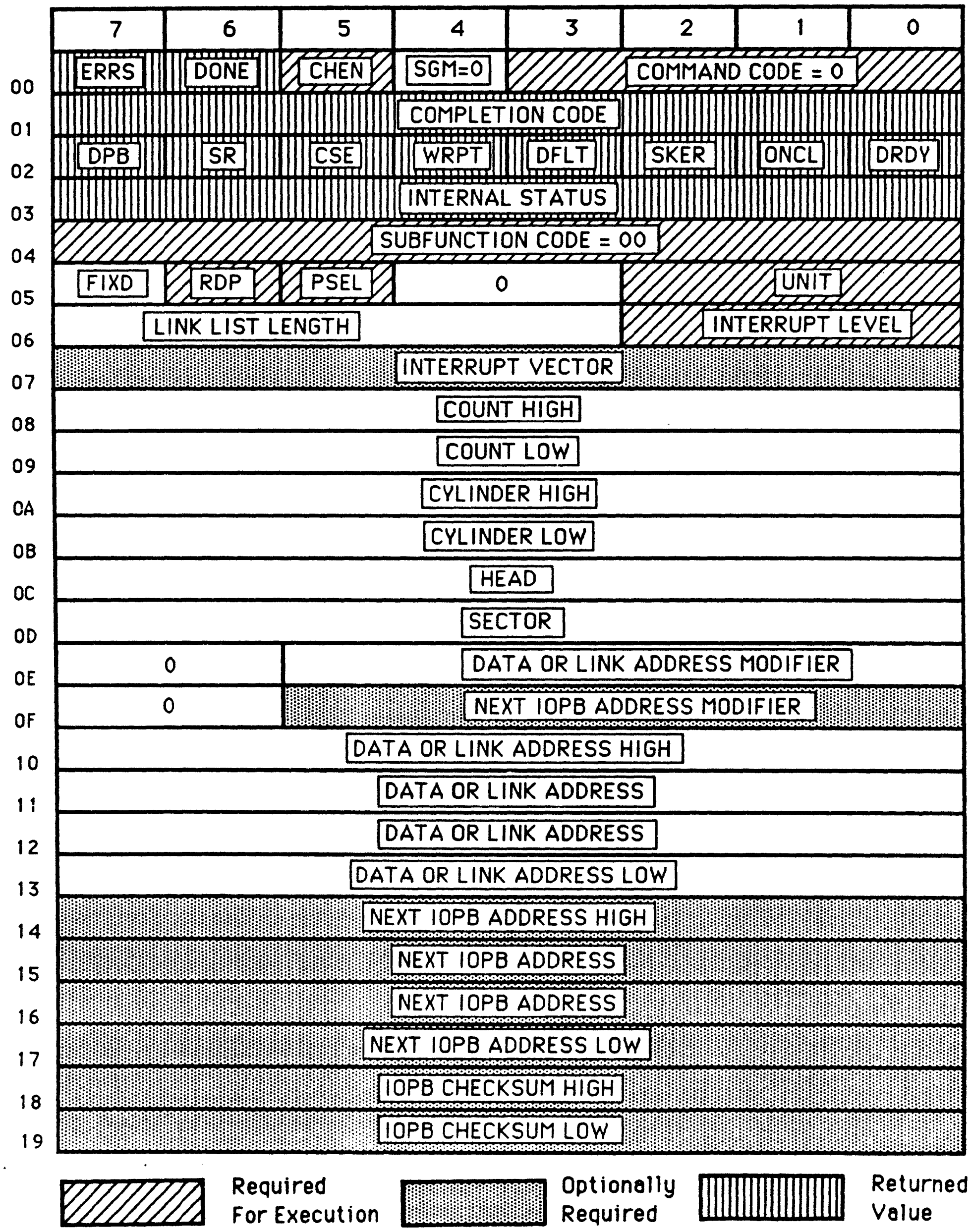
Status	Action
AUD Clear/No Error Occurs	752 updates Bytes 0-3 with ERRS, DONE, Completion Code, and internal status
AUD Set/No Error Occurs	752 updates the entire IOPB
AUD Clear/Error Occurs	752 updates the entire IOPB
AUD Clear/A Read Parameters or Read Extended Status Command is Executed	752 updates the entire IOPB

Table 5-1. Command Completion

5.1 NO OPERATION

The No Operation (NOP) command is a diagnostic tool. The 752 reads the IOPB and marks it complete.

NOP



	7	6	5	4	3	2	1	0
00	ERRS	DONE	CHEN	SGM=0	COMMAND CODE = 0			
01	COMPLETION CODE							
02	DPB	SR	CSE	WRPT	DFLT	SKER	ONCL	DRDY
03	INTERNAL STATUS							
04	SUBFUNCTION CODE = 00							
05	FIXD	RDP	PSEL	0		UNIT		
06	LINK LIST LENGTH					INTERRUPT LEVEL		
07	INTERRUPT VECTOR							
08	COUNT HIGH							
09	COUNT LOW							
0A	CYLINDER HIGH							
0B	CYLINDER LOW							
0C	HEAD							
0D	SECTOR							
0E	0		DATA OR LINK ADDRESS MODIFIER					
0F	0		NEXT IOPB ADDRESS MODIFIER					
10	DATA OR LINK ADDRESS HIGH							
11	DATA OR LINK ADDRESS							
12	DATA OR LINK ADDRESS							
13	DATA OR LINK ADDRESS LOW							
14	NEXT IOPB ADDRESS HIGH							
15	NEXT IOPB ADDRESS							
16	NEXT IOPB ADDRESS							
17	NEXT IOPB ADDRESS LOW							
18	IOPB CHECKSUM HIGH							
19	IOPB CHECKSUM LOW							

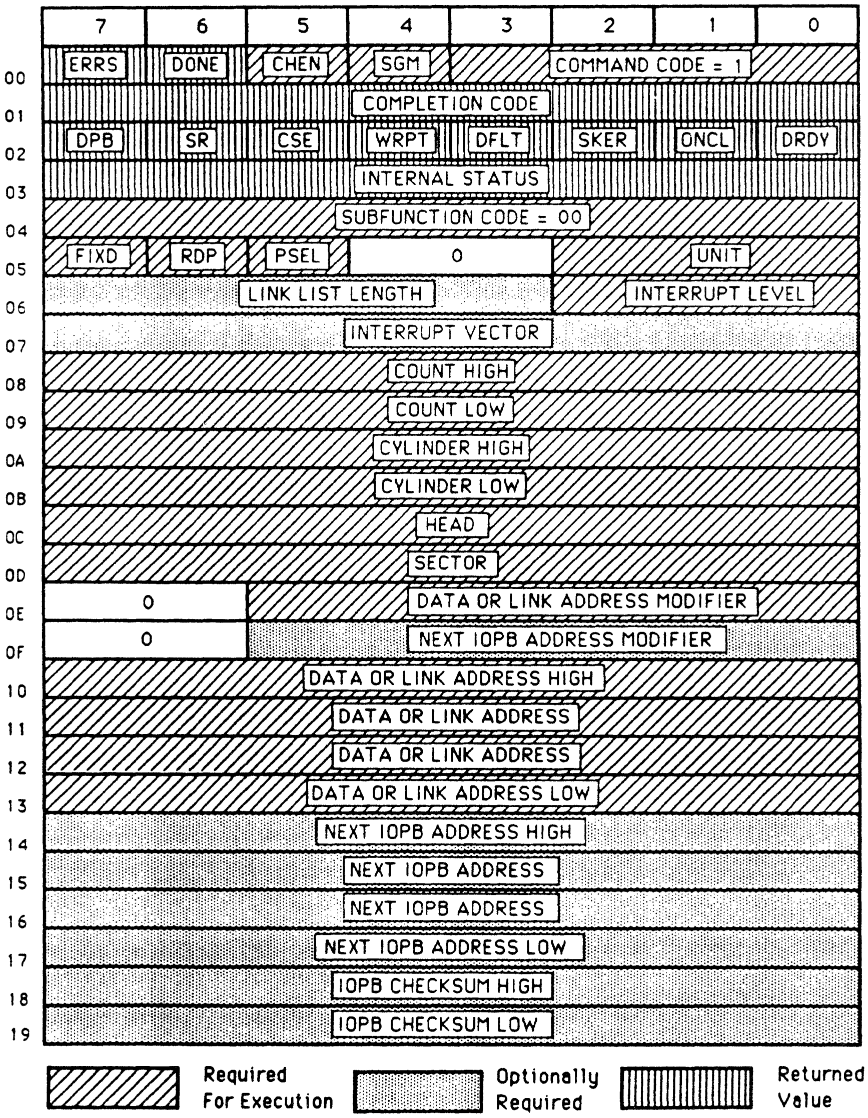
5.2 WRITE DATA

The 752, after reading and decoding the IOPB, positions the disk drive heads at the target cylinder; then it reads in the data from host memory (as per the IOPB) and writes the data contiguously to the specified disk address and subsequent sequential sectors.

Write Data has two IOPB formats: Normal and Scatter/Gather. A Normal IOPB specifies one contiguous block of host memory to write to the disk. A Gather Write IOPB specifies up to 32 different blocks of host memory to be placed in contiguous sectors on the disk (see Section 8.9).

The 752 stores IOPBs in a command queue that holds up to ten full IOPBs. This queue allows the 752 to optimize the commands for overlap seeks.

WRITE DATA



	7	6	5	4	3	2	1	0
00	ERRS	DONE	CHEN	SGM	COMMAND CODE = 1			
01	COMPLETION CODE							
02	DPB	SR	CSE	WRPT	DFLT	SKER	ONCL	DRDY
03	INTERNAL STATUS							
04	SUBFUNCTION CODE = 00							
05	FIXD	RDP	PSEL	0		UNIT		
06	LINK LIST LENGTH					INTERRUPT LEVEL		
07	INTERRUPT VECTOR							
08	COUNT HIGH							
09	COUNT LOW							
0A	CYLINDER HIGH							
0B	CYLINDER LOW							
0C	HEAD							
0D	SECTOR							
0E	0		DATA OR LINK ADDRESS MODIFIER					
0F	0		NEXT IOPB ADDRESS MODIFIER					
10	DATA OR LINK ADDRESS HIGH							
11	DATA OR LINK ADDRESS							
12	DATA OR LINK ADDRESS							
13	DATA OR LINK ADDRESS LOW							
14	NEXT IOPB ADDRESS HIGH							
15	NEXT IOPB ADDRESS							
16	NEXT IOPB ADDRESS							
17	NEXT IOPB ADDRESS LOW							
18	IOPB CHECKSUM HIGH							
19	IOPB CHECKSUM LOW							

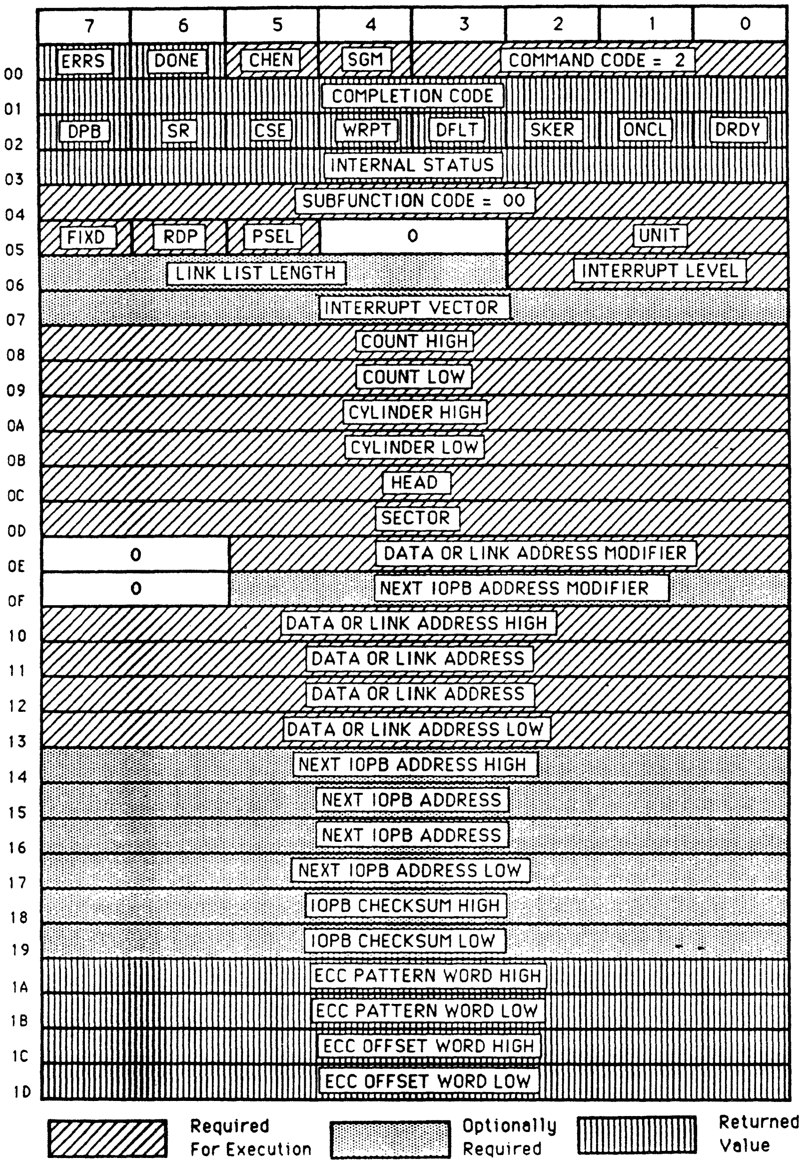
5.3 READ DATA

The 752, after reading and decoding the IOPB, positions the disk drive heads at the target cylinder, then reads the disk data indicated by the IOPB, and writes the data in host memory.

Read Data has two IOPB formats: Normal and Scatter/Gather. A Normal IOPB specifies one contiguous block of host memory that is used to place the data from the disk. A Scatter Read IOPB specifies up to 32 different blocks of host memory where the disk data will be placed (see Section 8.9).

The 752 stores IOPBs in a command queue that holds up to ten full IOPBs. This queue allows the 752 to optimize the commands for overlap seeks.

READ DATA

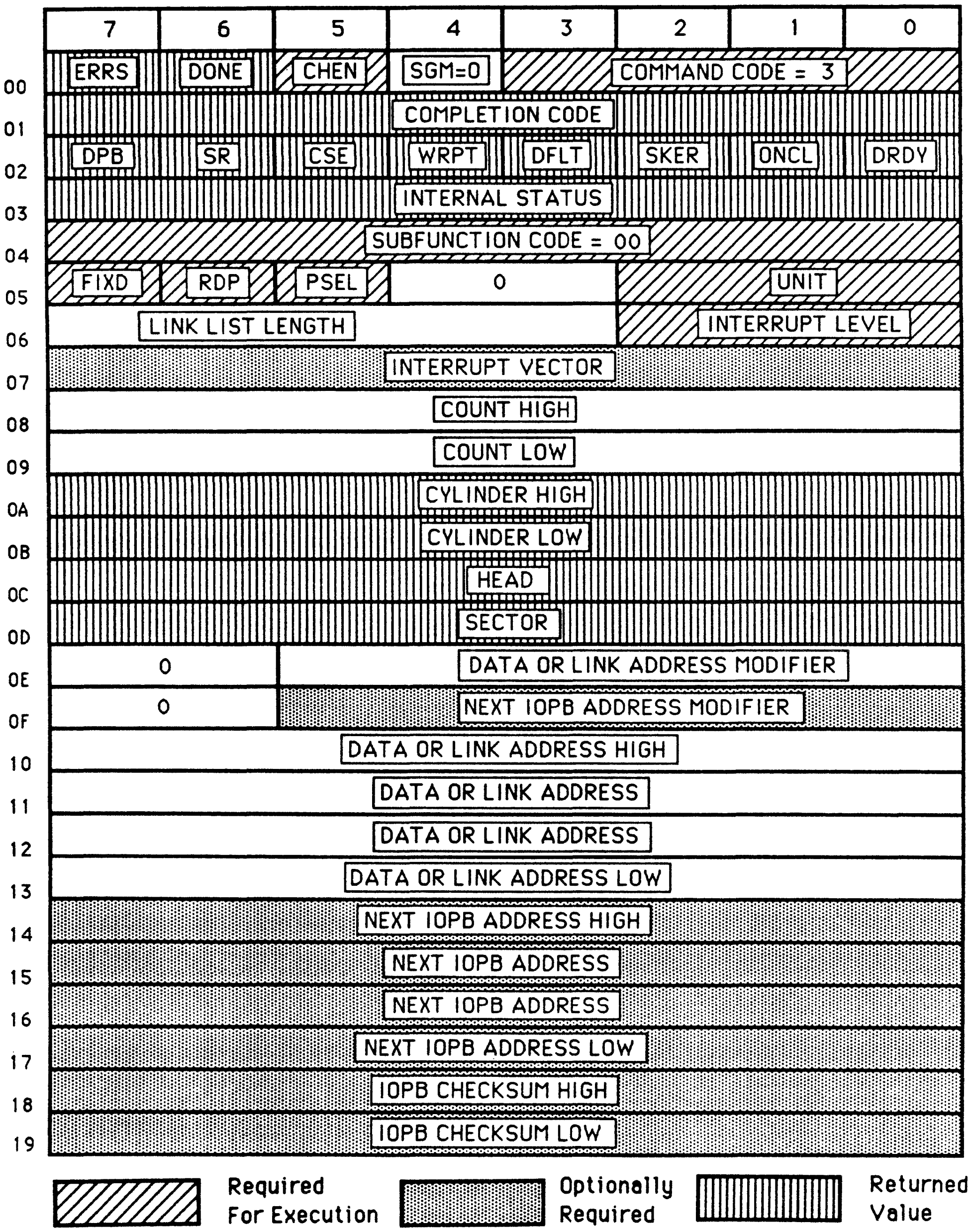


	7	6	5	4	3	2	1	0
00	ERRS	DONE	CHEN	SGM	COMMAND CODE = 2			
01	COMPLETION CODE							
02	DPB	SR	CSE	WRPT	DFLT	SKER	ONCL	DRDY
03	INTERNAL STATUS							
04	SUBFUNCTION CODE = 00							
05	FIXD	RDP	PSEL	0		UNIT		
06	LINK LIST LENGTH					INTERRUPT LEVEL		
07	INTERRUPT VECTOR							
08	COUNT HIGH							
09	COUNT LOW							
0A	CYLINDER HIGH							
0B	CYLINDER LOW							
0C	HEAD							
0D	SECTOR							
0E	0		DATA OR LINK ADDRESS MODIFIER					
0F	0		NEXT IOPB ADDRESS MODIFIER					
10	DATA OR LINK ADDRESS HIGH							
11	DATA OR LINK ADDRESS							
12	DATA OR LINK ADDRESS							
13	DATA OR LINK ADDRESS LOW							
14	NEXT IOPB ADDRESS HIGH							
15	NEXT IOPB ADDRESS							
16	NEXT IOPB ADDRESS							
17	NEXT IOPB ADDRESS LOW							
18	IOPB CHECKSUM HIGH							
19	IOPB CHECKSUM LOW							
1A	ECC PATTERN WORD HIGH							
1B	ECC PATTERN WORD LOW							
1C	ECC OFFSET WORD HIGH							
1D	ECC OFFSET WORD LOW							

5.4 REPORT CURRENT ADDRESS

The 752 selects the disk drive, reads the first good header field, and returns the address to the host via the IOPB; it updates the IOPB regardless of AUD's status.

REPORT CURRENT ADDRESS



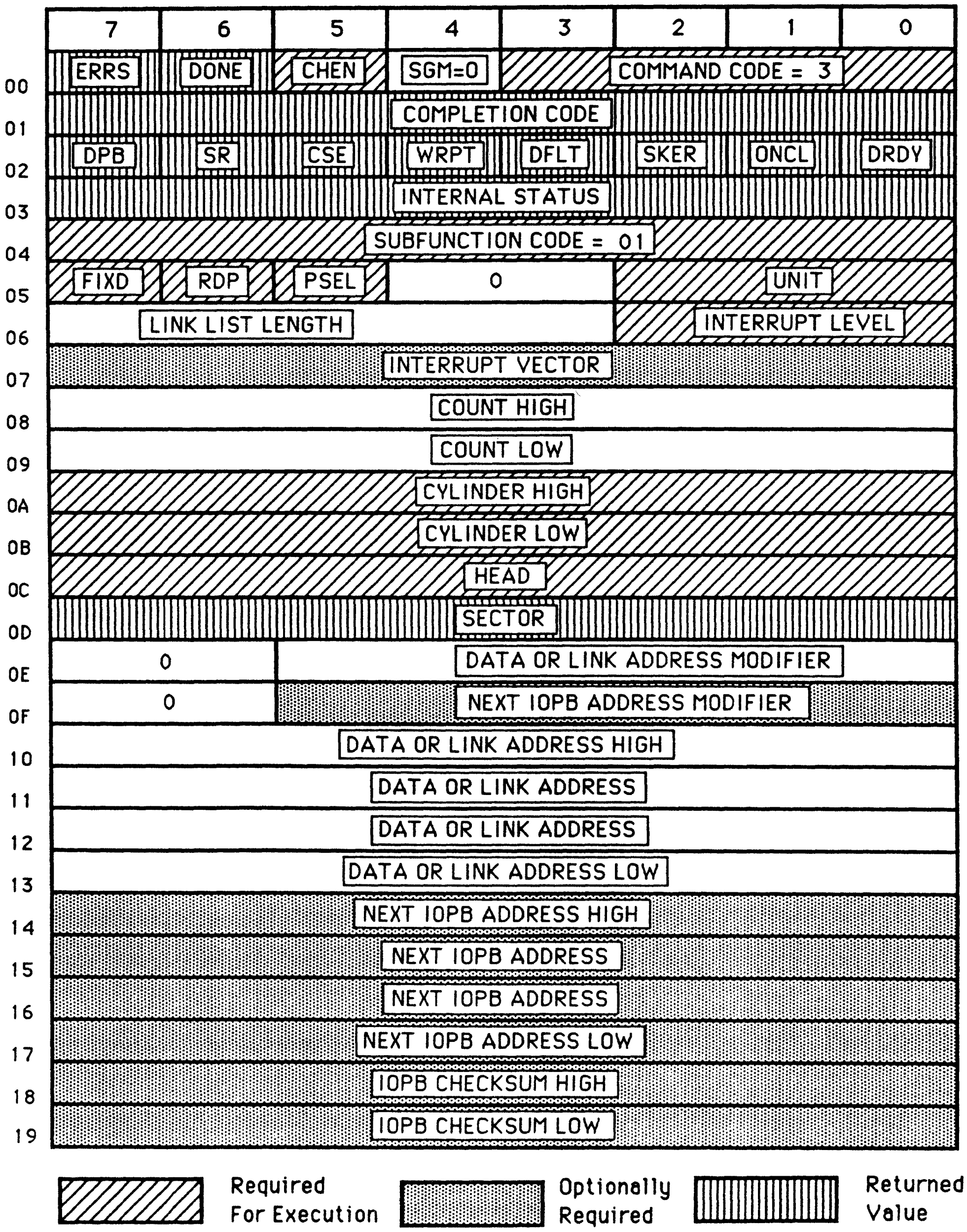
	7	6	5	4	3	2	1	0
00	ERRS	DONE	CHEN	SGM=0	COMMAND CODE = 3			
01	COMPLETION CODE							
02	DPB	SR	CSE	WRPT	DFLT	SKER	ONCL	DRDY
03	INTERNAL STATUS							
04	SUBFUNCTION CODE = 00							
05	FIXD	RDP	PSEL	0		UNIT		
06	LINK LIST LENGTH					INTERRUPT LEVEL		
07	INTERRUPT VECTOR							
08	COUNT HIGH							
09	COUNT LOW							
0A	CYLINDER HIGH							
0B	CYLINDER LOW							
0C	HEAD							
0D	SECTOR							
0E	0		DATA OR LINK ADDRESS MODIFIER					
0F	0		NEXT IOPB ADDRESS MODIFIER					
10	DATA OR LINK ADDRESS HIGH							
11	DATA OR LINK ADDRESS							
12	DATA OR LINK ADDRESS							
13	DATA OR LINK ADDRESS LOW							
14	NEXT IOPB ADDRESS HIGH							
15	NEXT IOPB ADDRESS							
16	NEXT IOPB ADDRESS							
17	NEXT IOPB ADDRESS LOW							
18	IOPB CHECKSUM HIGH							
19	IOPB CHECKSUM LOW							

▨ Required For Execution
░ Optionally Required
▥ Returned Value

5.5 SEEK AND REPORT CURRENT ADDRESS

The 752 issues a seek to the selected disk drive for the target cylinder. After the drive completes the seek, the 752 reads the first good header field it encounters and reports it to the host via the completed IOPB. The 752 updates the IOPB regardless of AUD's status.

SEEK AND REPORT CURRENT ADDRESS



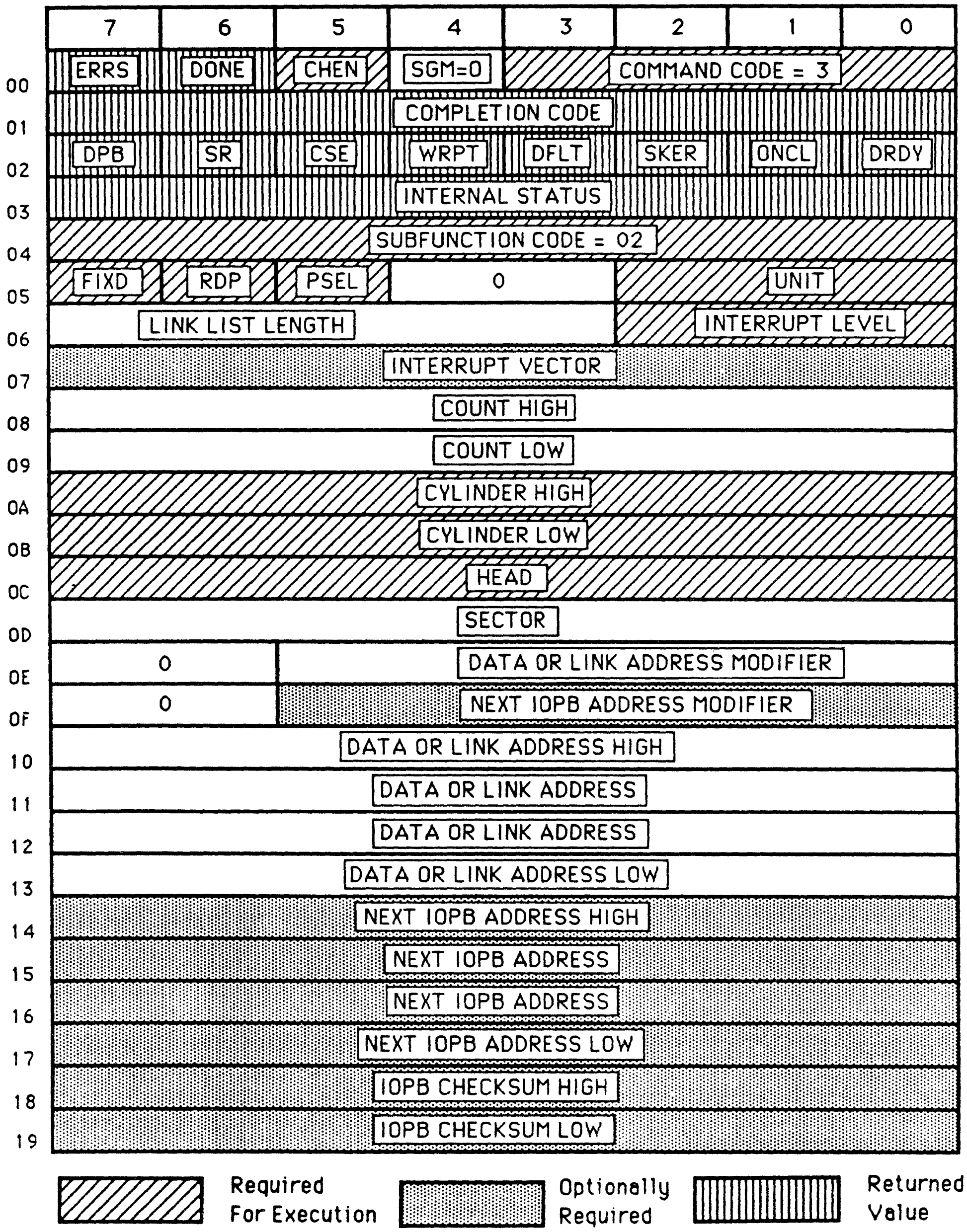
	7	6	5	4	3	2	1	0
00	ERRS	DONE	CHEN	SGM=0	COMMAND CODE = 3			
01	COMPLETION CODE							
02	DPB	SR	CSE	WRPT	DFLT	SKER	ONCL	DRDY
03	INTERNAL STATUS							
04	SUBFUNCTION CODE = 01							
05	FIXD	RDP	PSEL	0		UNIT		
06	LINK LIST LENGTH					INTERRUPT LEVEL		
07	INTERRUPT VECTOR							
08	COUNT HIGH							
09	COUNT LOW							
0A	CYLINDER HIGH							
0B	CYLINDER LOW							
0C	HEAD							
0D	SECTOR							
0E	0		DATA OR LINK ADDRESS MODIFIER					
0F	0		NEXT IOPB ADDRESS MODIFIER					
10	DATA OR LINK ADDRESS HIGH							
11	DATA OR LINK ADDRESS							
12	DATA OR LINK ADDRESS							
13	DATA OR LINK ADDRESS LOW							
14	NEXT IOPB ADDRESS HIGH							
15	NEXT IOPB ADDRESS							
16	NEXT IOPB ADDRESS							
17	NEXT IOPB ADDRESS LOW							
18	IOPB CHECKSUM HIGH							
19	IOPB CHECKSUM LOW							

▨ Required For Execution
░ Optionally Required
▥ Returned Value

5.6 START SEEK AND REPORT COMPLETION IMMEDIATELY

The 752 issues a seek to the selected disk drive for the target cylinder, and reports a completion to the host without waiting for the seek to complete.

START SEEK AND REPORT COMPLETION IMMEDIATELY



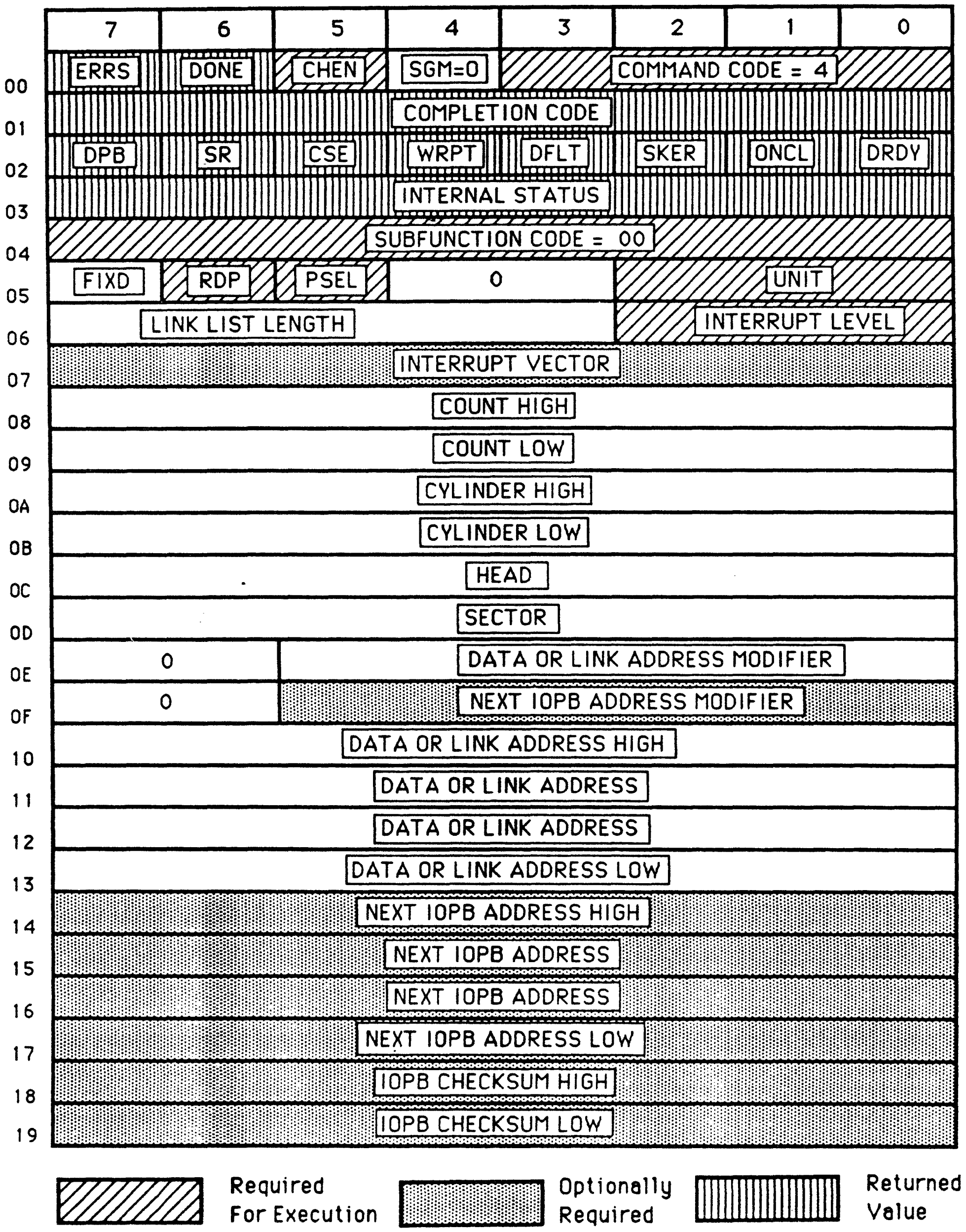
	7	6	5	4	3	2	1	0
00	ERRS	DONE	CHEN	SGM=0	COMMAND CODE = 3			
01	COMPLETION CODE							
02	DPB	SR	CSE	WRPT	DFLT	SKER	ONCL	DRDY
03	INTERNAL STATUS							
04	SUBFUNCTION CODE = 02							
05	FIXD	RDP	PSEL	0		UNIT		
06	LINK LIST LENGTH					INTERRUPT LEVEL		
07	INTERRUPT VECTOR							
08	COUNT HIGH							
09	COUNT LOW							
0A	CYLINDER HIGH							
0B	CYLINDER LOW							
0C	HEAD							
0D	SECTOR							
0E	0		DATA OR LINK ADDRESS MODIFIER					
0F	0		NEXT IOPB ADDRESS MODIFIER					
10	DATA OR LINK ADDRESS HIGH							
11	DATA OR LINK ADDRESS							
12	DATA OR LINK ADDRESS							
13	DATA OR LINK ADDRESS LOW							
14	NEXT IOPB ADDRESS HIGH							
15	NEXT IOPB ADDRESS							
16	NEXT IOPB ADDRESS							
17	NEXT IOPB ADDRESS LOW							
18	IOPB CHECKSUM HIGH							
19	IOPB CHECKSUM LOW							

▨ Required For Execution ░ Optionally Required ▥ Returned Value

5.7 DRIVE RESET

The 752 resets the disk drive. First it issues a fault clear, and then a recalibrate (return to zero). The IOPB is complete when the recalibrate completes or times out on drives that are ready. The 752 does not wait for the recalibrate to complete on drives that are not ready.

DRIVE RESET



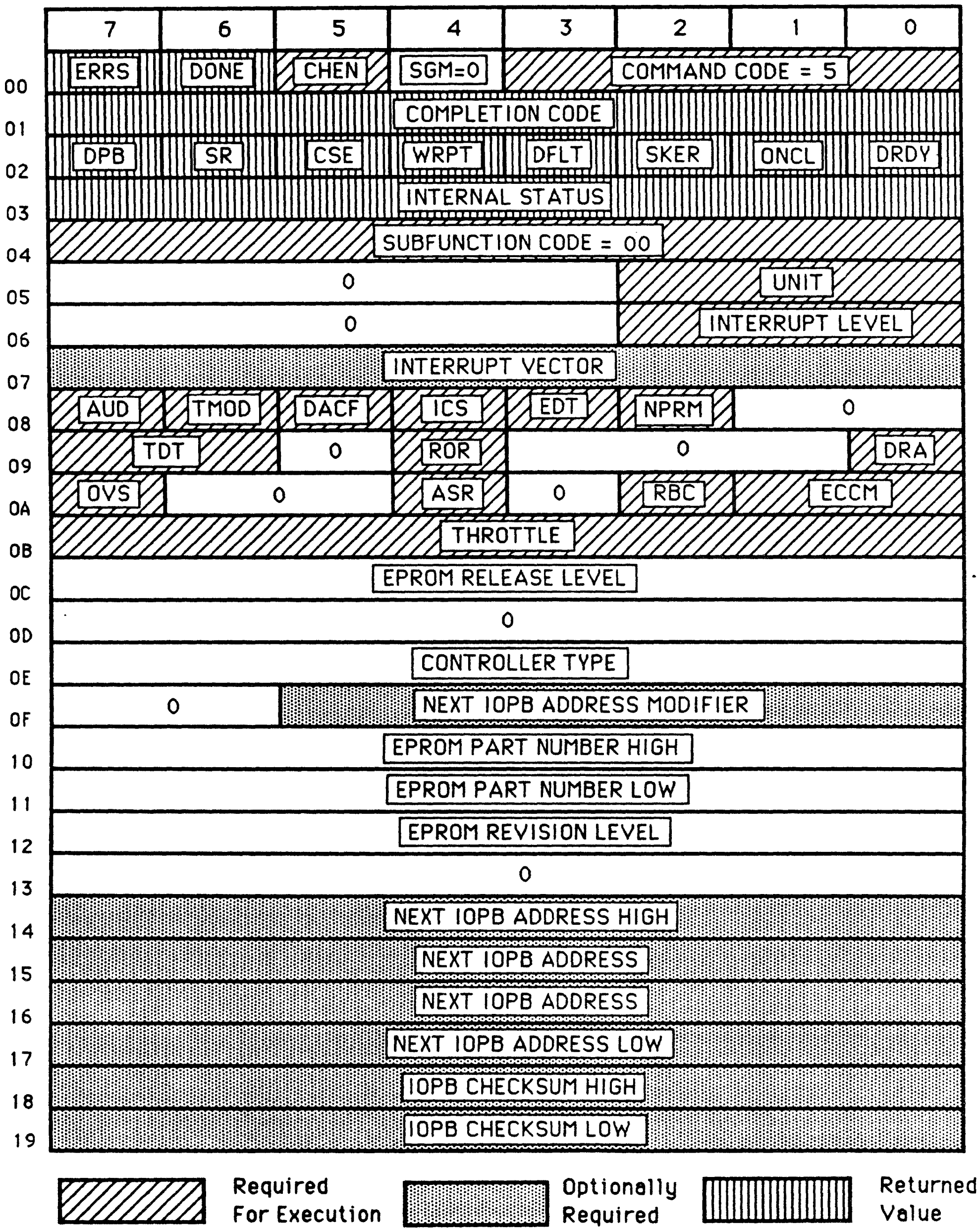
	7	6	5	4	3	2	1	0
00	ERRS	DONE	CHEN	SGM=0	COMMAND CODE = 4			
01	COMPLETION CODE							
02	DPB	SR	CSE	WRPT	DFLT	SKER	ONCL	DRDY
03	INTERNAL STATUS							
04	SUBFUNCTION CODE = 00							
05	FIXD	RDP	PSEL	0		UNIT		
06	LINK LIST LENGTH					INTERRUPT LEVEL		
07	INTERRUPT VECTOR							
08	COUNT HIGH							
09	COUNT LOW							
0A	CYLINDER HIGH							
0B	CYLINDER LOW							
0C	HEAD							
0D	SECTOR							
0E	0		DATA OR LINK ADDRESS MODIFIER					
0F	0		NEXT IOPB ADDRESS MODIFIER					
10	DATA OR LINK ADDRESS HIGH							
11	DATA OR LINK ADDRESS							
12	DATA OR LINK ADDRESS							
13	DATA OR LINK ADDRESS LOW							
14	NEXT IOPB ADDRESS HIGH							
15	NEXT IOPB ADDRESS							
16	NEXT IOPB ADDRESS							
17	NEXT IOPB ADDRESS LOW							
18	IOPB CHECKSUM HIGH							
19	IOPB CHECKSUM LOW							

▨ Required For Execution
░ Optionally Required
▥ Returned Value

5.8 WRITE CONTROLLER PARAMETERS

This command initializes the 752 with its operational parameters. No default parameters are assumed. Section 4.2 defines how to change the parameters for individual applications.

WRITE CONTROLLER PARAMETERS



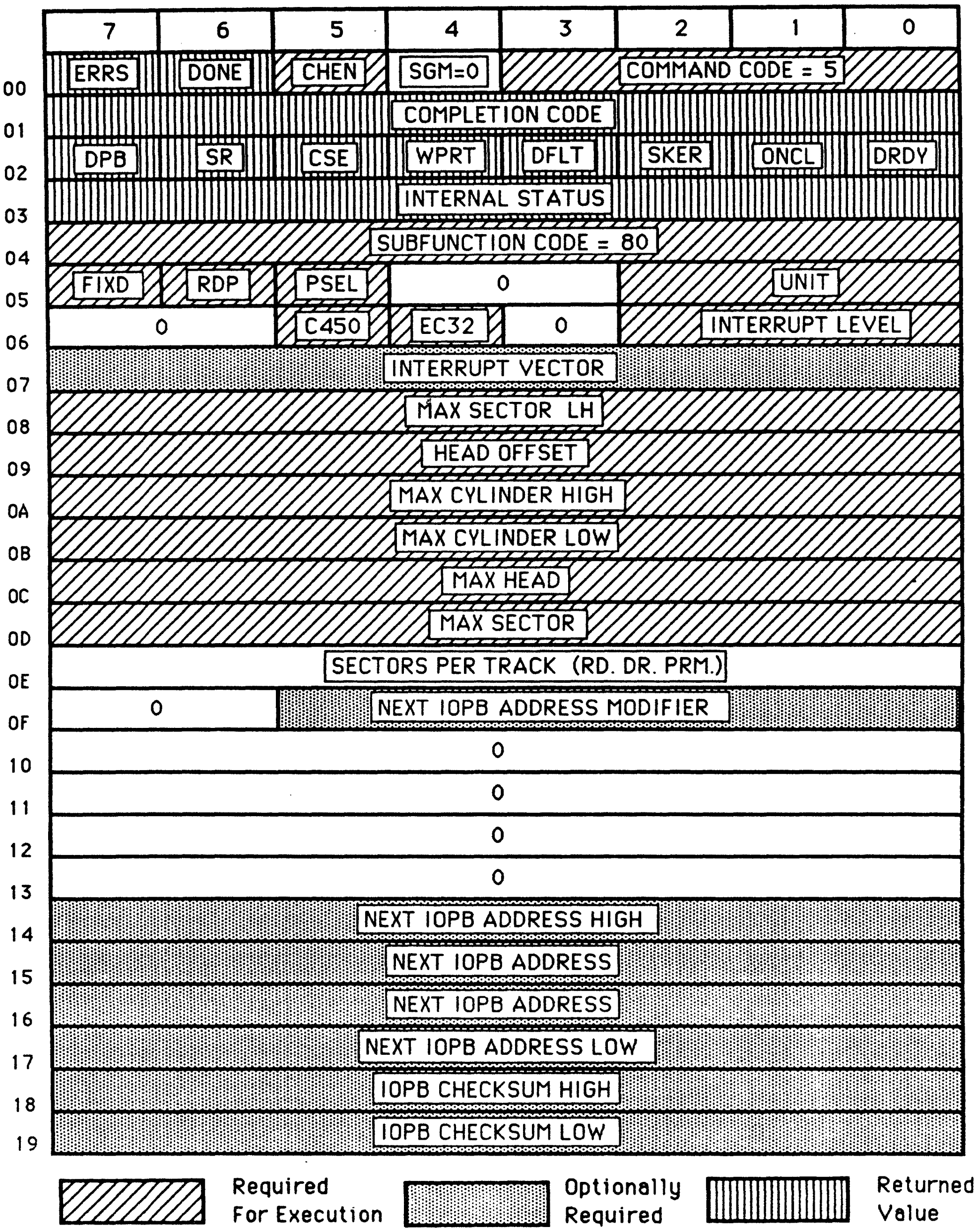
	7	6	5	4	3	2	1	0
00	ERRS	DONE	CHEN	SGM=0	COMMAND CODE = 5			
01	COMPLETION CODE							
02	DPB	SR	CSE	WRPT	DFLT	SKER	ONCL	DRDY
03	INTERNAL STATUS							
04	SUBFUNCTION CODE = 00							
05	0					UNIT		
06	0					INTERRUPT LEVEL		
07	INTERRUPT VECTOR							
08	AUD	TMOD	DACF	ICS	EDT	NPRM	0	
09	TDT		0	ROR	0			DRA
0A	OVS	0		ASR	0	RBC	ECCM	
0B	THROTTLE							
0C	EPROM RELEASE LEVEL							
0D	0							
0E	CONTROLLER TYPE							
0F	0		NEXT IOPB ADDRESS MODIFIER					
10	EPROM PART NUMBER HIGH							
11	EPROM PART NUMBER LOW							
12	EPROM REVISION LEVEL							
13	0							
14	NEXT IOPB ADDRESS HIGH							
15	NEXT IOPB ADDRESS							
16	NEXT IOPB ADDRESS							
17	NEXT IOPB ADDRESS LOW							
18	IOPB CHECKSUM HIGH							
19	IOPB CHECKSUM LOW							

▨ Required For Execution
░ Optionally Required
▥ Returned Value

5.9 WRITE DRIVE PARAMETERS

This command specifies the disk drive's physical characteristics. The 752 assumes no default values. See Section 4.3.

WRITE DRIVE PARAMETERS



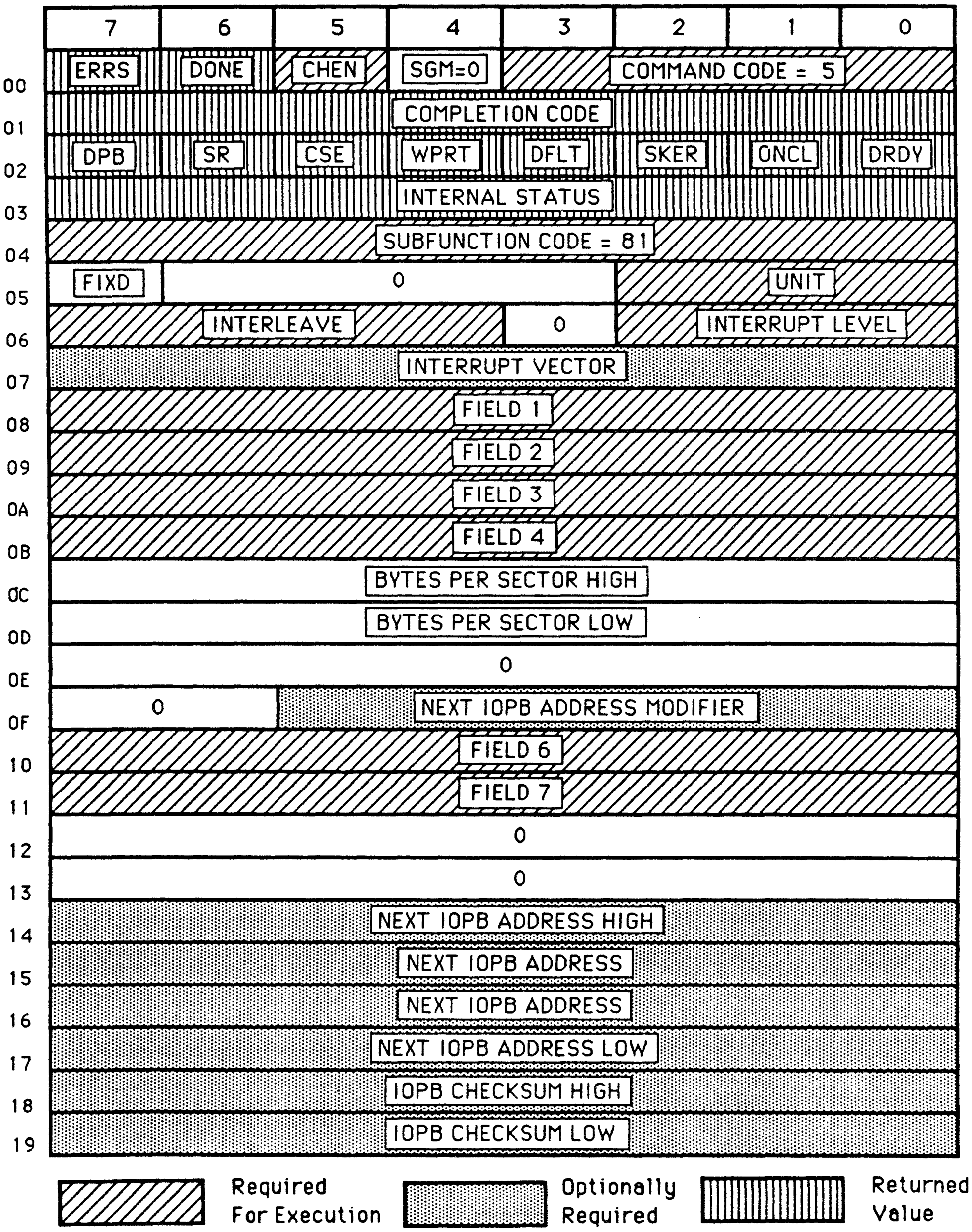
	7	6	5	4	3	2	1	0
00	ERRS	DONE	CHEN	SGM=0	COMMAND CODE = 5			
01	COMPLETION CODE							
02	DPB	SR	CSE	WPRT	DFLT	SKER	ONCL	DRDY
03	INTERNAL STATUS							
04	SUBFUNCTION CODE = 80							
05	FIXD	RDP	PSEL	0		UNIT		
06	0		C450	EC32	0	INTERRUPT LEVEL		
07	INTERRUPT VECTOR							
08	MAX SECTOR LH							
09	HEAD OFFSET							
0A	MAX CYLINDER HIGH							
0B	MAX CYLINDER LOW							
0C	MAX HEAD							
0D	MAX SECTOR							
0E	SECTORS PER TRACK (RD. DR. PRM.)							
0F	0		NEXT IOPB ADDRESS MODIFIER					
10	0							
11	0							
12	0							
13	0							
14	NEXT IOPB ADDRESS HIGH							
15	NEXT IOPB ADDRESS							
16	NEXT IOPB ADDRESS							
17	NEXT IOPB ADDRESS LOW							
18	IOPB CHECKSUM HIGH							
19	IOPB CHECKSUM LOW							

▨ Required For Execution
░ Optionally Required
▥ Returned Value

5.10 WRITE FORMAT PARAMETERS

This command specifies the disk drive's media format. Since the 752 uses a traditional RAM, you must execute a Write Format Parameters command before attempting any disk access (see Section 4.4).

WRITE FORMAT PARAMETERS



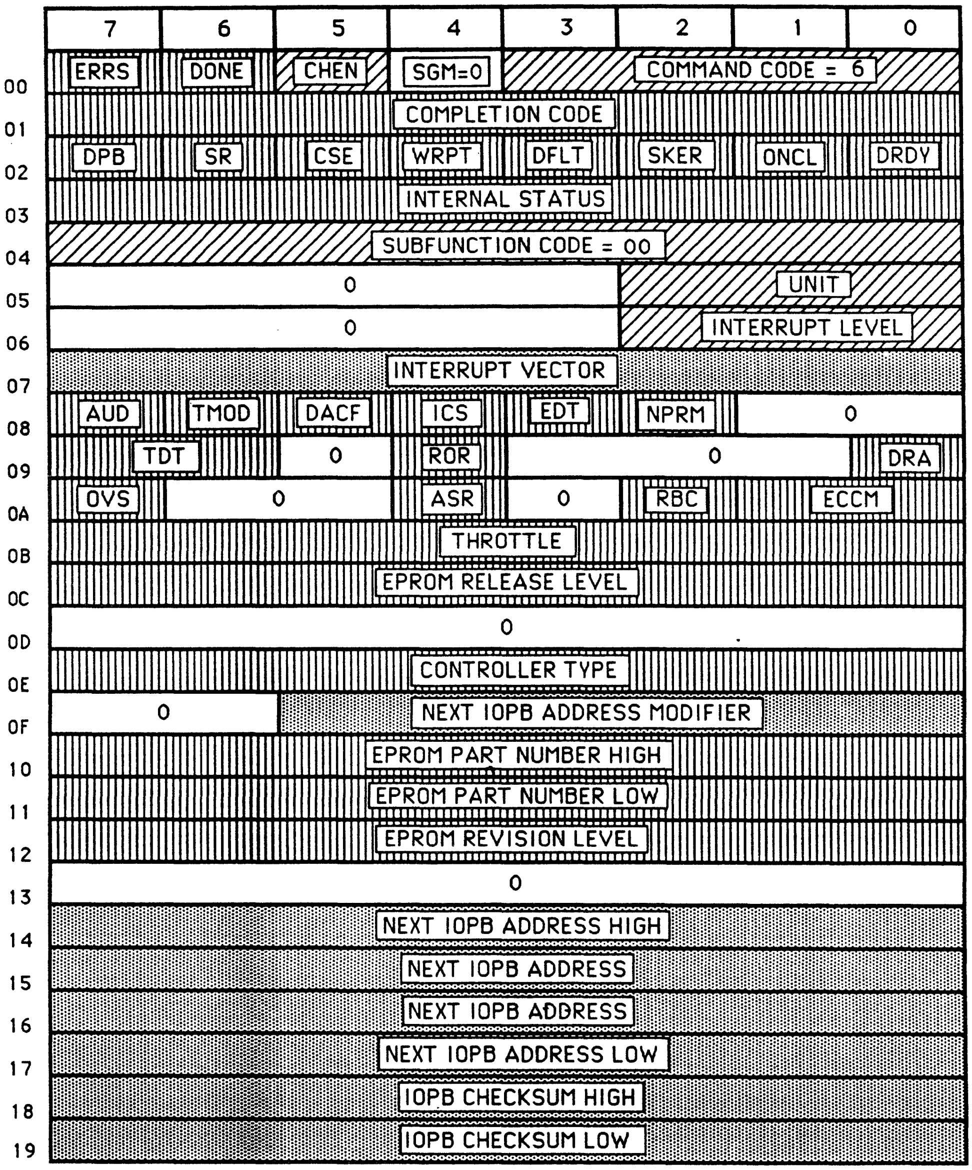
	7	6	5	4	3	2	1	0
00	ERRS	DONE	CHEN	SGM=0	COMMAND CODE = 5			
01	COMPLETION CODE							
02	DPB	SR	CSE	WPRT	DFLT	SKER	ONCL	DRDY
03	INTERNAL STATUS							
04	SUBFUNCTION CODE = 81							
05	FIXD	0				UNIT		
06	INTERLEAVE				0	INTERRUPT LEVEL		
07	INTERRUPT VECTOR							
08	FIELD 1							
09	FIELD 2							
0A	FIELD 3							
0B	FIELD 4							
0C	BYTES PER SECTOR HIGH							
0D	BYTES PER SECTOR LOW							
0E	0							
0F	0		NEXT IOPB ADDRESS MODIFIER					
10	FIELD 6							
11	FIELD 7							
12	0							
13	0							
14	NEXT IOPB ADDRESS HIGH							
15	NEXT IOPB ADDRESS							
16	NEXT IOPB ADDRESS							
17	NEXT IOPB ADDRESS LOW							
18	IOPB CHECKSUM HIGH							
19	IOPB CHECKSUM LOW							

▨ Required For Execution ░ Optionally Required ▥ Returned Value

5.11 READ CONTROLLER PARAMETERS

The 752 returns its current operational parameters to the host via the IOPB; it updates the IOPB regardless of AUD's status. See Section 4.2.

READ CONTROLLER PARAMETERS



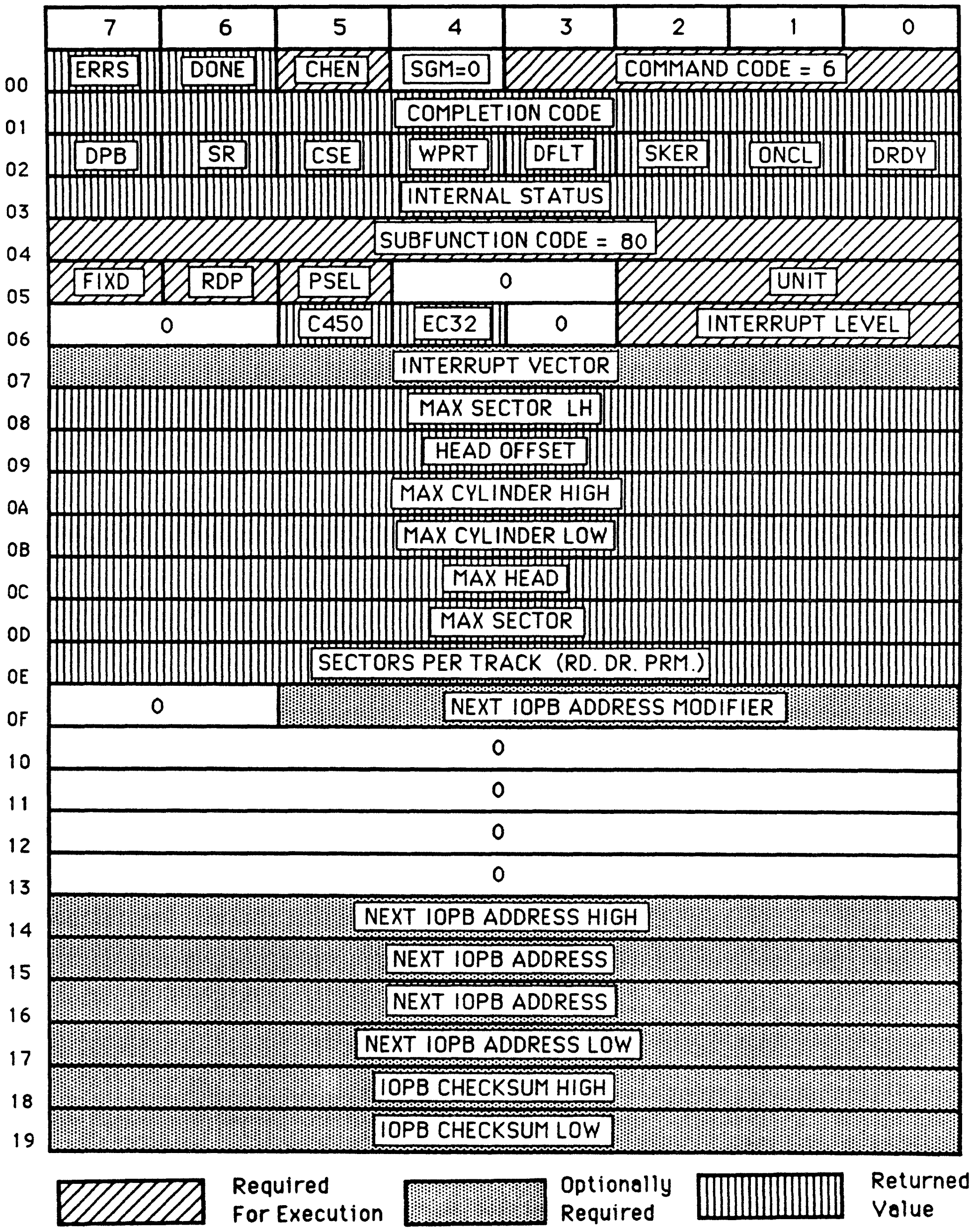
	7	6	5	4	3	2	1	0
00	ERRS	DONE	CHEN	SGM=0	COMMAND CODE = 6			
01	COMPLETION CODE							
02	DPB	SR	CSE	WRPT	DFLT	SKER	ONCL	DRDY
03	INTERNAL STATUS							
04	SUBFUNCTION CODE = 00							
05	0					UNIT		
06	0					INTERRUPT LEVEL		
07	INTERRUPT VECTOR							
08	AUD	TMOD	DACF	ICS	EDT	NPRM	0	
09	TDT		0	ROR	0			DRA
0A	OVS	0		ASR	0	RBC	ECCM	
0B	THROTTLE							
0C	EPROM RELEASE LEVEL							
0D	0							
0E	CONTROLLER TYPE							
0F	0		NEXT IOPB ADDRESS MODIFIER					
10	EPROM PART NUMBER HIGH							
11	EPROM PART NUMBER LOW							
12	EPROM REVISION LEVEL							
13	0							
14	NEXT IOPB ADDRESS HIGH							
15	NEXT IOPB ADDRESS							
16	NEXT IOPB ADDRESS							
17	NEXT IOPB ADDRESS LOW							
18	IOPB CHECKSUM HIGH							
19	IOPB CHECKSUM LOW							

▨ Required For Execution ░ Optionally Required ▥ Returned Value

5.12 READ DRIVE PARAMETERS

The 752 returns the values programmed for each drive's physical characteristics to the host via the IOPB; it returns the specified drive's actual number of sectors per track in Byte 0EH. The 752 updates the IOPB regardless of AUD's status. See Section 4.3.

READ DRIVE PARAMETERS



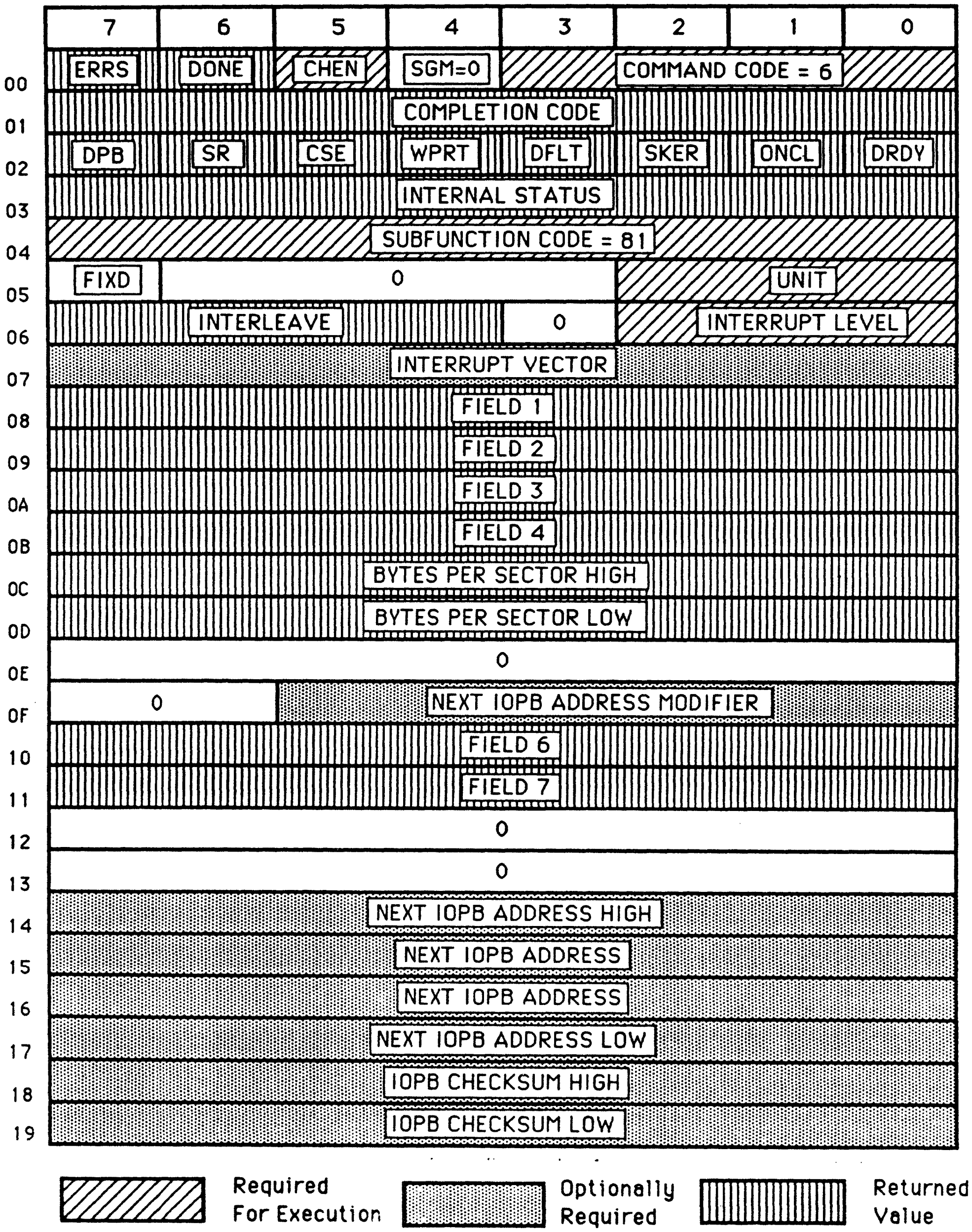
	7	6	5	4	3	2	1	0
00	ERRS	DONE	CHEN	SGM=0	COMMAND CODE = 6			
01	COMPLETION CODE							
02	DPB	SR	CSE	WPRT	DFLT	SKER	ONCL	DRDY
03	INTERNAL STATUS							
04	SUBFUNCTION CODE = 80							
05	FIXD	RDP	PSEL	0		UNIT		
06	0		C450	EC32	0	INTERRUPT LEVEL		
07	INTERRUPT VECTOR							
08	MAX SECTOR LH							
09	HEAD OFFSET							
0A	MAX CYLINDER HIGH							
0B	MAX CYLINDER LOW							
0C	MAX HEAD							
0D	MAX SECTOR							
0E	SECTORS PER TRACK (RD. DR. PRM.)							
0F	0		NEXT IOPB ADDRESS MODIFIER					
10	0							
11	0							
12	0							
13	0							
14	NEXT IOPB ADDRESS HIGH							
15	NEXT IOPB ADDRESS							
16	NEXT IOPB ADDRESS							
17	NEXT IOPB ADDRESS LOW							
18	IOPB CHECKSUM HIGH							
19	IOPB CHECKSUM LOW							

▨ Required For Execution
░ Optionally Required
▥ Returned Value

5.13 READ FORMAT PARAMETERS

The 752 returns the selected disk drive's format parameters to the host via the IOPB; it updates the IOPB regardless of AUD's status. See Section 4.4.

READ FORMAT PARAMETERS



	7	6	5	4	3	2	1	0
00	ERRS	DONE	CHEN	SGM=0	COMMAND CODE = 6			
01	COMPLETION CODE							
02	DPB	SR	CSE	WPRT	DFLT	SKER	ONCL	DRDY
03	INTERNAL STATUS							
04	SUBFUNCTION CODE = 81							
05	FIXD	0				UNIT		
06	INTERLEAVE				0	INTERRUPT LEVEL		
07	INTERRUPT VECTOR							
08	FIELD 1							
09	FIELD 2							
0A	FIELD 3							
0B	FIELD 4							
0C	BYTES PER SECTOR HIGH							
0D	BYTES PER SECTOR LOW							
0E	0							
0F	0		NEXT IOPB ADDRESS MODIFIER					
10	FIELD 6							
11	FIELD 7							
12	0							
13	0							
14	NEXT IOPB ADDRESS HIGH							
15	NEXT IOPB ADDRESS							
16	NEXT IOPB ADDRESS							
17	NEXT IOPB ADDRESS LOW							
18	IOPB CHECKSUM HIGH							
19	IOPB CHECKSUM LOW							

▨ Required For Execution ░ Optionally Required ▥ Returned Value

5.14 READ DRIVE STATUS EXTENDED

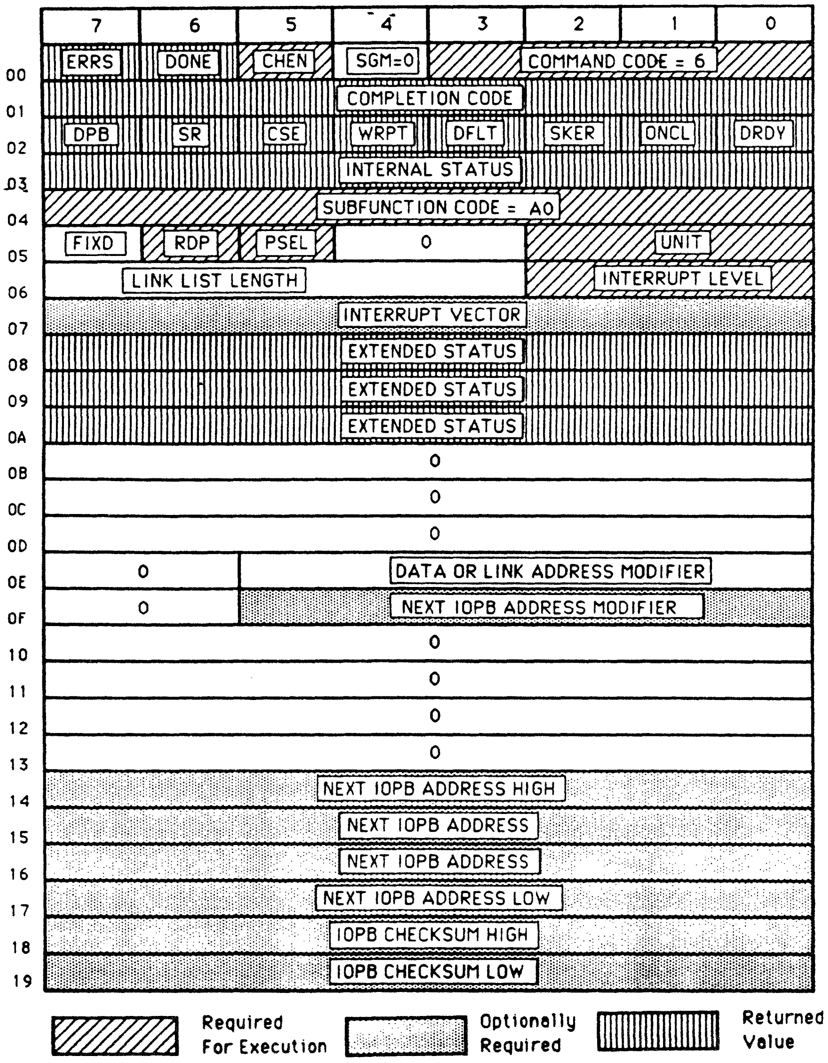
The 752 reads the SMD drive interface's extended status. It returns the drive's status in IOPB Bytes 8 through A regardless of AUD's status (see Table 5-2). The drive-specific bytes follow the same bit alignment as the standard Status byte.

Byte	Tag 4	Tag 5	Bit: 7	6	5	4	3	2	1	0
02	0	0	SECT	INDX	ADM	WRPT	DFLT	SKER	ONCL	DRDY
08	1	0	*	*	*	*	*	*	*	*
09	0	1	*	*	*	*	*	*	*	*
0A	1	1	*	*	*	*	*	*	*	*

* Drive-specific

Table 5-2. Extended Drive Status

READ DRIVE STATUS EXTENDED



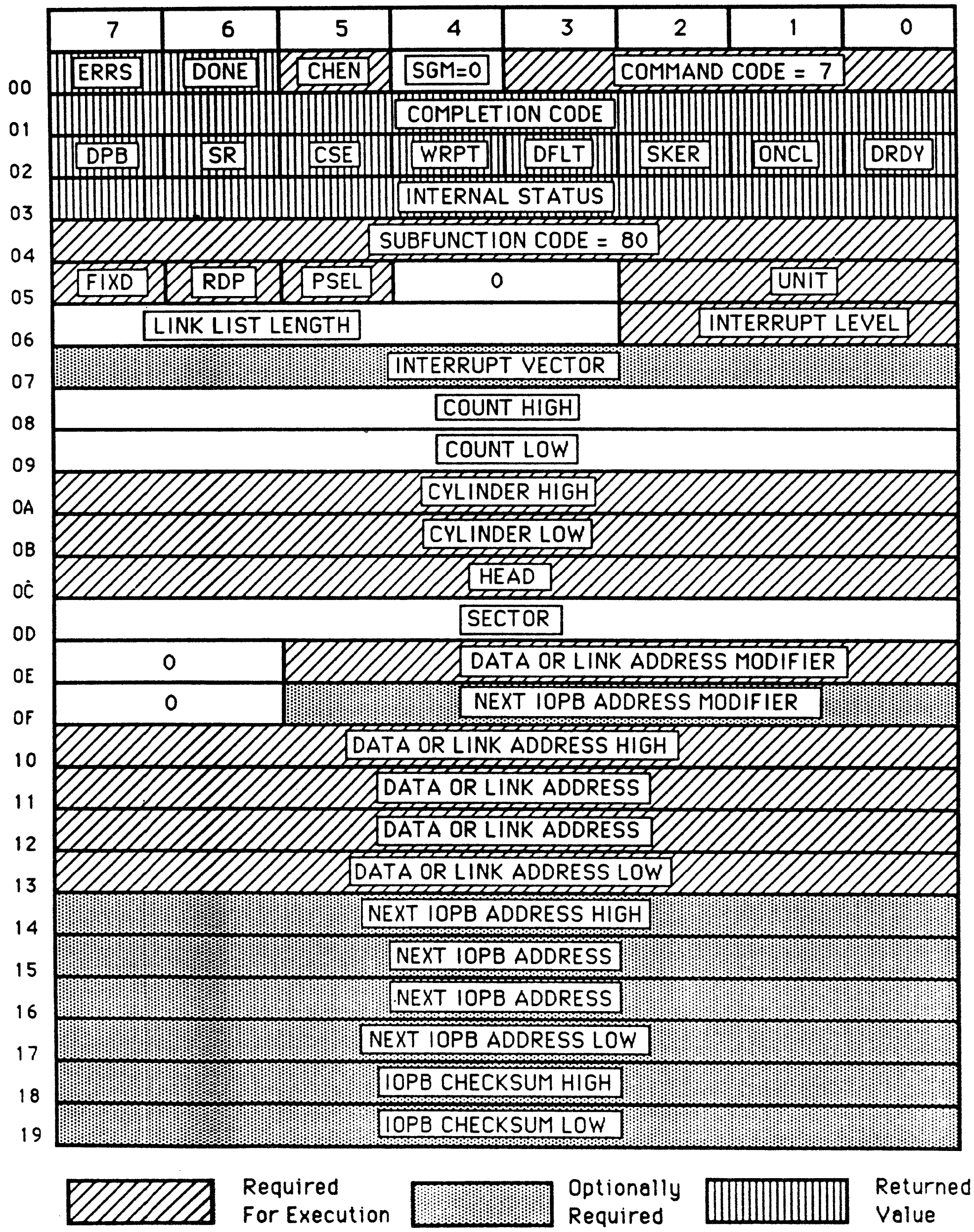
	7	6	5	4	3	2	1	0
00	ERRS	DONE	CHEN	SGM=0	COMMAND CODE = 6			
01	COMPLETION CODE							
02	DPB	SR	CSE	WRPT	DFLT	SKER	ONCL	DRDY
03	INTERNAL STATUS							
04	SUBFUNCTION CODE = A0							
05	FIXD	RDP	PSEL	0		UNIT		
06	LINK LIST LENGTH					INTERRUPT LEVEL		
07	INTERRUPT VECTOR							
08	EXTENDED STATUS							
09	EXTENDED STATUS							
0A	EXTENDED STATUS							
0B	0							
0C	0							
0D	0							
0E	0		DATA OR LINK ADDRESS MODIFIER					
0F	0		NEXT IOPB ADDRESS MODIFIER					
10	0							
11	0							
12	0							
13	0							
14	NEXT IOPB ADDRESS HIGH							
15	NEXT IOPB ADDRESS							
16	NEXT IOPB ADDRESS							
17	NEXT IOPB ADDRESS LOW							
18	IOPB CHECKSUM HIGH							
19	IOPB CHECKSUM LOW							

▨ Required For Execution
░ Optionally Required
▥ Returned Value

5.15 WRITE TRACK HEADERS

The host writes the sector header fields on a track (only one track per IOPB). The 752 takes the data for the header fields from host memory: four bytes per header; one header for each sector on the track. (The data fields are not preserved.) It places the data on the track starting from index. Section 8.3 defines the data format in each header.

WRITE TRACK HEADERS



	7	6	5	4	3	2	1	0
00	ERRS	DONE	CHEN	SGM=0	COMMAND CODE = 7			
01	COMPLETION CODE							
02	DPB	SR	CSE	WRPT	DFLT	SKER	ONCL	DRDY
03	INTERNAL STATUS							
04	SUBFUNCTION CODE = 80							
05	FIXD	RDP	PSEL	0		UNIT		
06	LINK LIST LENGTH					INTERRUPT LEVEL		
07	INTERRUPT VECTOR							
08	COUNT HIGH							
09	COUNT LOW							
0A	CYLINDER HIGH							
0B	CYLINDER LOW							
0C	HEAD							
0D	SECTOR							
0E	0		DATA OR LINK ADDRESS MODIFIER					
0F	0		NEXT IOPB ADDRESS MODIFIER					
10	DATA OR LINK ADDRESS HIGH							
11	DATA OR LINK ADDRESS							
12	DATA OR LINK ADDRESS							
13	DATA OR LINK ADDRESS LOW							
14	NEXT IOPB ADDRESS HIGH							
15	NEXT IOPB ADDRESS							
16	NEXT IOPB ADDRESS							
17	NEXT IOPB ADDRESS LOW							
18	IOPB CHECKSUM HIGH							
19	IOPB CHECKSUM LOW							

▨ Required For Execution

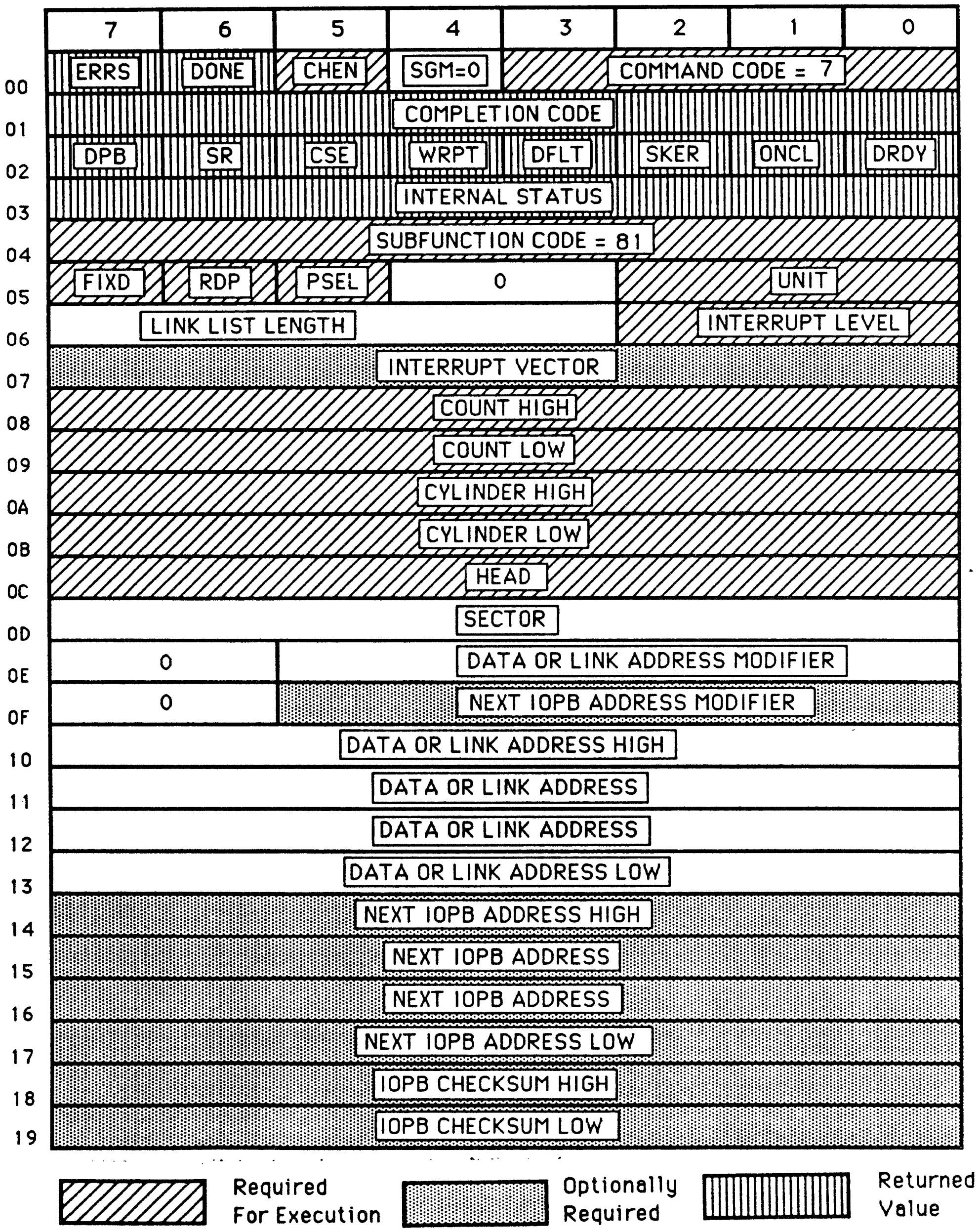
░ Optionally Required

▥ Returned Value

5.16 WRITE FORMAT

The 752 formats the drive, writing the header of all sectors with the appropriate sector ID. The data field contains zeros and a valid ECC. The Count bytes in this command refer to the number of tracks to be formatted. See Section 8.2.

WRITE FORMAT



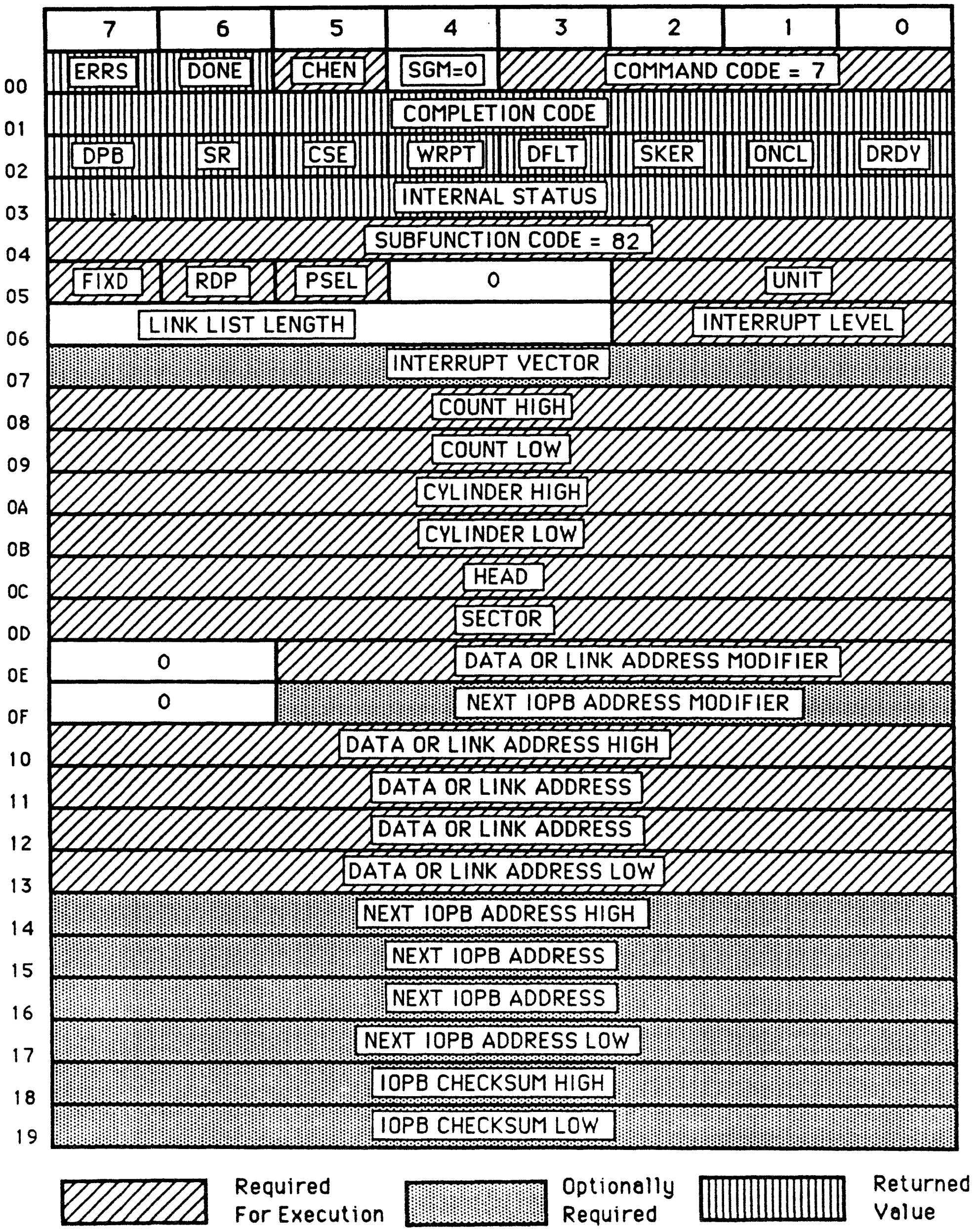
	7	6	5	4	3	2	1	0
00	ERRS	DONE	CHEN	SGM=0	COMMAND CODE = 7			
01	COMPLETION CODE							
02	DPB	SR	CSE	WRPT	DFLT	SKER	ONCL	DRDY
03	INTERNAL STATUS							
04	SUBFUNCTION CODE = 81							
05	FIXD	RDP	PSEL	0		UNIT		
06	LINK LIST LENGTH					INTERRUPT LEVEL		
07	INTERRUPT VECTOR							
08	COUNT HIGH							
09	COUNT LOW							
0A	CYLINDER HIGH							
0B	CYLINDER LOW							
0C	HEAD							
0D	SECTOR							
0E	0			DATA OR LINK ADDRESS MODIFIER				
0F	0			NEXT IOPB ADDRESS MODIFIER				
10	DATA OR LINK ADDRESS HIGH							
11	DATA OR LINK ADDRESS							
12	DATA OR LINK ADDRESS							
13	DATA OR LINK ADDRESS LOW							
14	NEXT IOPB ADDRESS HIGH							
15	NEXT IOPB ADDRESS							
16	NEXT IOPB ADDRESS							
17	NEXT IOPB ADDRESS LOW							
18	IOPB CHECKSUM HIGH							
19	IOPB CHECKSUM LOW							

5.17 WRITE HEADER, HEADER VERIFY, DATA, AND DATA ECC

The 752 writes a sector header, header verify, data, and data ECC. There are always four bytes in the header, but the other fields vary according to the initial 752 set-up. The 752 does not cross head or cylinder boundaries while executing this command.

The host must calculate the ECC in all ECC fields since the controller does not calculate any ECC fields for this command. See Section 8.11.

WRITE HEADER, HEADER VERIFY, DATA, AND DATA ECC



	7	6	5	4	3	2	1	0
00	ERRS	DONE	CHEN	SGM=0	COMMAND CODE = 7			
01	COMPLETION CODE							
02	DPB	SR	CSE	WRPT	DFLT	SKER	ONCL	DRDY
03	INTERNAL STATUS							
04	SUBFUNCTION CODE = 82							
05	FIXD	RDP	PSEL	0		UNIT		
06	LINK LIST LENGTH					INTERRUPT LEVEL		
07	INTERRUPT VECTOR							
08	COUNT HIGH							
09	COUNT LOW							
0A	CYLINDER HIGH							
0B	CYLINDER LOW							
0C	HEAD							
0D	SECTOR							
0E	0		DATA OR LINK ADDRESS MODIFIER					
0F	0		NEXT IOPB ADDRESS MODIFIER					
10	DATA OR LINK ADDRESS HIGH							
11	DATA OR LINK ADDRESS							
12	DATA OR LINK ADDRESS							
13	DATA OR LINK ADDRESS LOW							
14	NEXT IOPB ADDRESS HIGH							
15	NEXT IOPB ADDRESS							
16	NEXT IOPB ADDRESS							
17	NEXT IOPB ADDRESS LOW							
18	IOPB CHECKSUM HIGH							
19	IOPB CHECKSUM LOW							

▨ Required For Execution

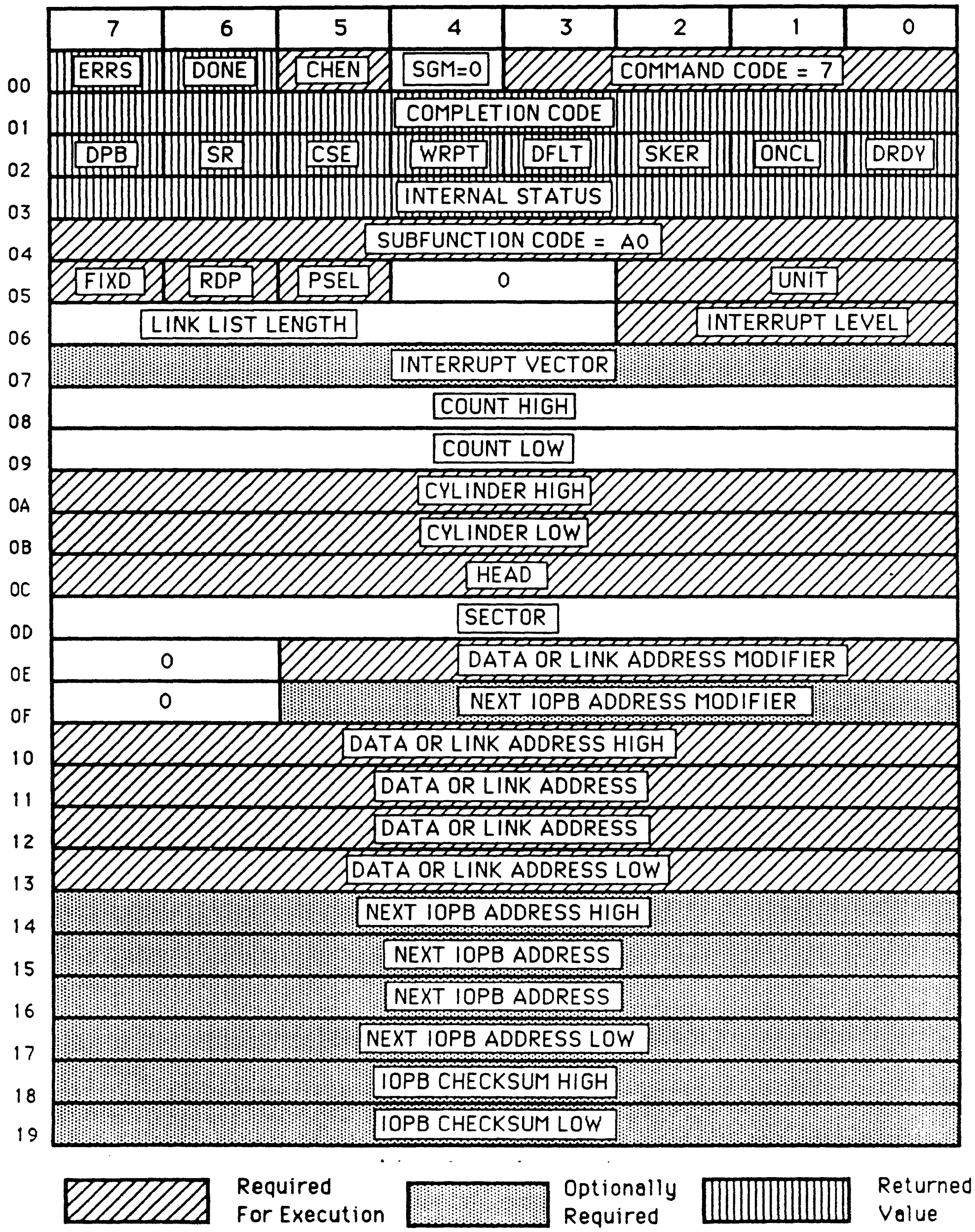
░ Optionally Required

▥ Returned Value

5.18 WRITE DEFECT MAP

Write Defect Map is a useful maintenance command for debugging software. The 752 uses data from host memory and writes a manufacturer's defect map to the disk. See Section 8.1.

WRITE DEFECT MAP



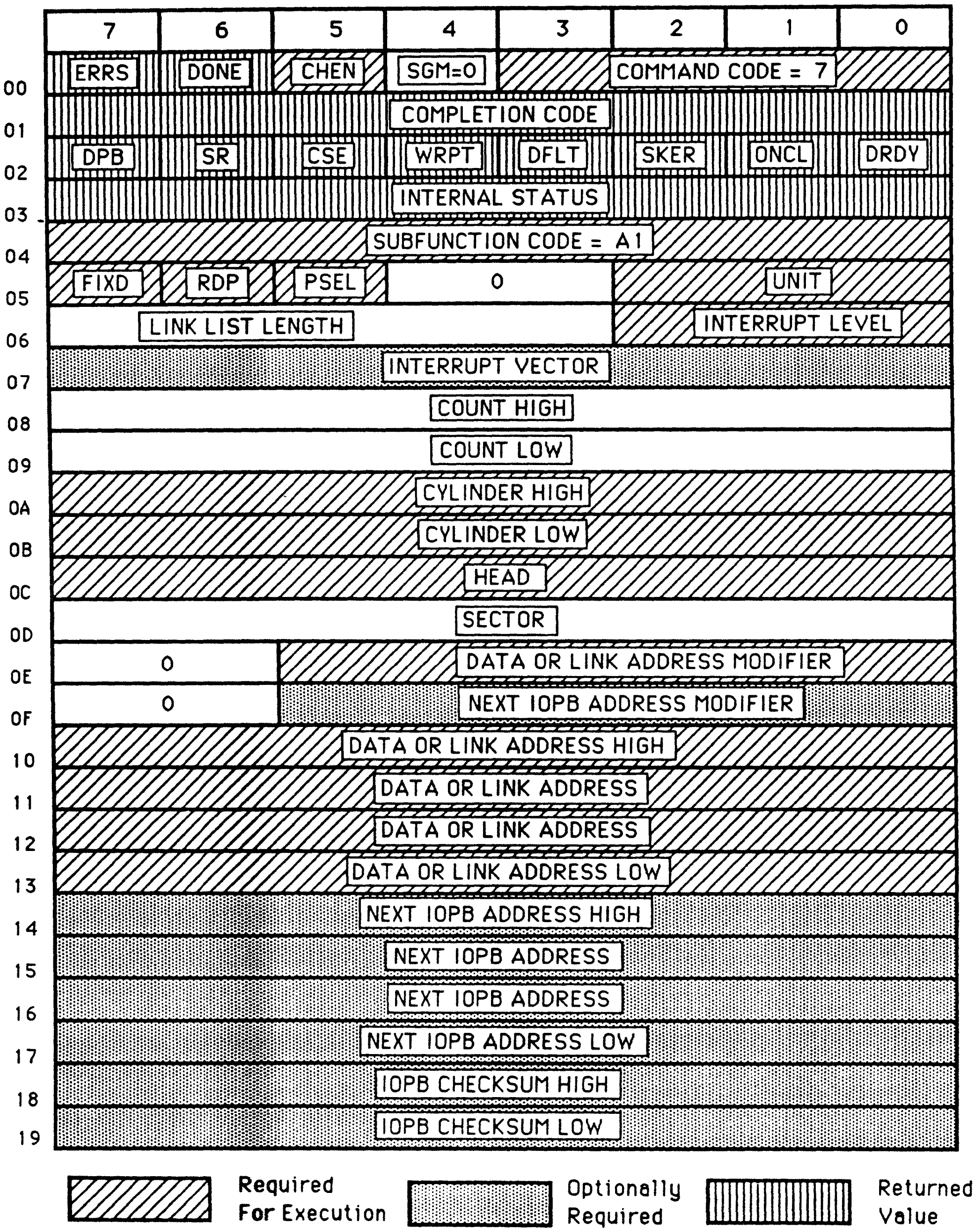
	7	6	5	4	3	2	1	0
00	ERRS	DONE	CHEN	SGM=0	COMMAND CODE = 7			
01	COMPLETION CODE							
02	DPB	SR	CSE	WRPT	DFLT	SKER	ONCL	DRDY
03	INTERNAL STATUS							
04	SUBFUNCTION CODE = A0							
05	FIXD	RDP	PSEL	0		UNIT		
06	LINK LIST LENGTH					INTERRUPT LEVEL		
07	INTERRUPT VECTOR							
08	COUNT HIGH							
09	COUNT LOW							
0A	CYLINDER HIGH							
0B	CYLINDER LOW							
0C	HEAD							
0D	SECTOR							
0E	0		DATA OR LINK ADDRESS MODIFIER					
0F	0		NEXT IOPB ADDRESS MODIFIER					
10	DATA OR LINK ADDRESS HIGH							
11	DATA OR LINK ADDRESS							
12	DATA OR LINK ADDRESS							
13	DATA OR LINK ADDRESS LOW							
14	NEXT IOPB ADDRESS HIGH							
15	NEXT IOPB ADDRESS							
16	NEXT IOPB ADDRESS							
17	NEXT IOPB ADDRESS LOW							
18	IOPB CHECKSUM HIGH							
19	IOPB CHECKSUM LOW							

▨ Required For Execution ░ Optionally Required ▥ Returned Value

5.19 WRITE DEFECT MAP EXTENDED

Write Defect Map Extended is a useful maintenance command for debugging software. The 752 uses data from host memory and writes a manufacturer's defect map to the alternate location on the track. This offsets the defect map from index, avoiding media defects.

WRITE DEFECT MAP EXTENDED

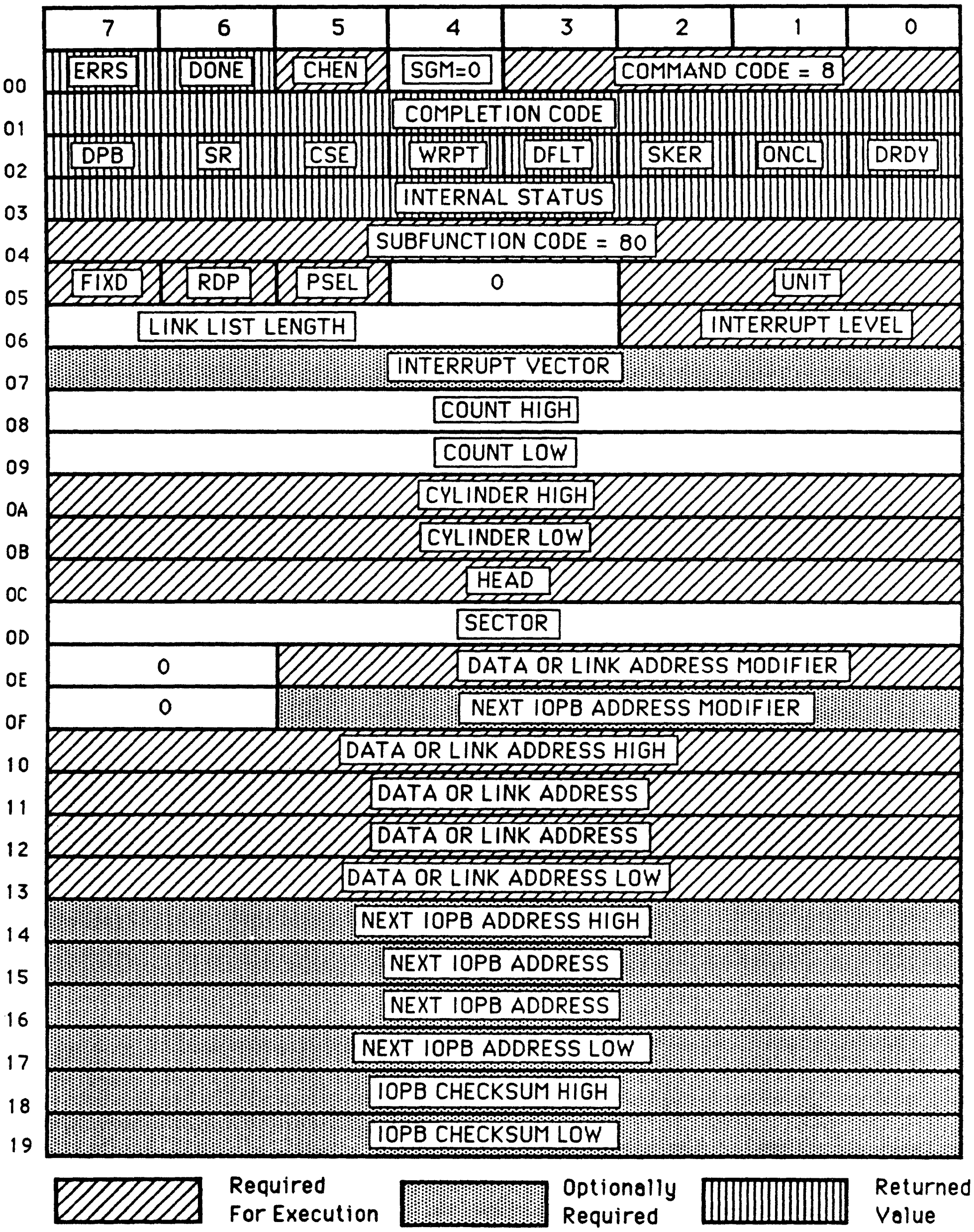


	7	6	5	4	3	2	1	0
00	ERRS	DONE	CHEN	SGM=0		COMMAND CODE = 7		
01	COMPLETION CODE							
02	DPB	SR	CSE	WRPT	DFLT	SKER	ONCL	DRDY
03	INTERNAL STATUS							
04	SUBFUNCTION CODE = A1							
05	FIXD	RDP	PSEL	0		UNIT		
06	LINK LIST LENGTH					INTERRUPT LEVEL		
07	INTERRUPT VECTOR							
08	COUNT HIGH							
09	COUNT LOW							
0A	CYLINDER HIGH							
0B	CYLINDER LOW							
0C	HEAD							
0D	SECTOR							
0E	0		DATA OR LINK ADDRESS MODIFIER					
0F	0		NEXT IOPB ADDRESS MODIFIER					
10	DATA OR LINK ADDRESS HIGH							
11	DATA OR LINK ADDRESS							
12	DATA OR LINK ADDRESS							
13	DATA OR LINK ADDRESS LOW							
14	NEXT IOPB ADDRESS HIGH							
15	NEXT IOPB ADDRESS							
16	NEXT IOPB ADDRESS							
17	NEXT IOPB ADDRESS LOW							
18	IOPB CHECKSUM HIGH							
19	IOPB CHECKSUM LOW							

5.20 READ TRACK HEADERS

The host reads the sector header fields on a track. The 752 places the data from the header fields in host memory: four bytes per header; one header for each sector on the track. Section 8.3 defines the data format in each header.

READ TRACK HEADERS



	7	6	5	4	3	2	1	0
00	ERRS	DONE	CHEN	SGM=0	COMMAND CODE = 8			
01	COMPLETION CODE							
02	DPB	SR	CSE	WRPT	DFLT	SKER	ONCL	DRDY
03	INTERNAL STATUS							
04	SUBFUNCTION CODE = 80							
05	FIXD	RDP	PSEL	0		UNIT		
06	LINK LIST LENGTH					INTERRUPT LEVEL		
07	INTERRUPT VECTOR							
08	COUNT HIGH							
09	COUNT LOW							
0A	CYLINDER HIGH							
0B	CYLINDER LOW							
0C	HEAD							
0D	SECTOR							
0E	0		DATA OR LINK ADDRESS MODIFIER					
0F	0		NEXT IOPB ADDRESS MODIFIER					
10	DATA OR LINK ADDRESS HIGH							
11	DATA OR LINK ADDRESS							
12	DATA OR LINK ADDRESS							
13	DATA OR LINK ADDRESS LOW							
14	NEXT IOPB ADDRESS HIGH							
15	NEXT IOPB ADDRESS							
16	NEXT IOPB ADDRESS							
17	NEXT IOPB ADDRESS LOW							
18	IOPB CHECKSUM HIGH							
19	IOPB CHECKSUM LOW							

▨ Required For Execution

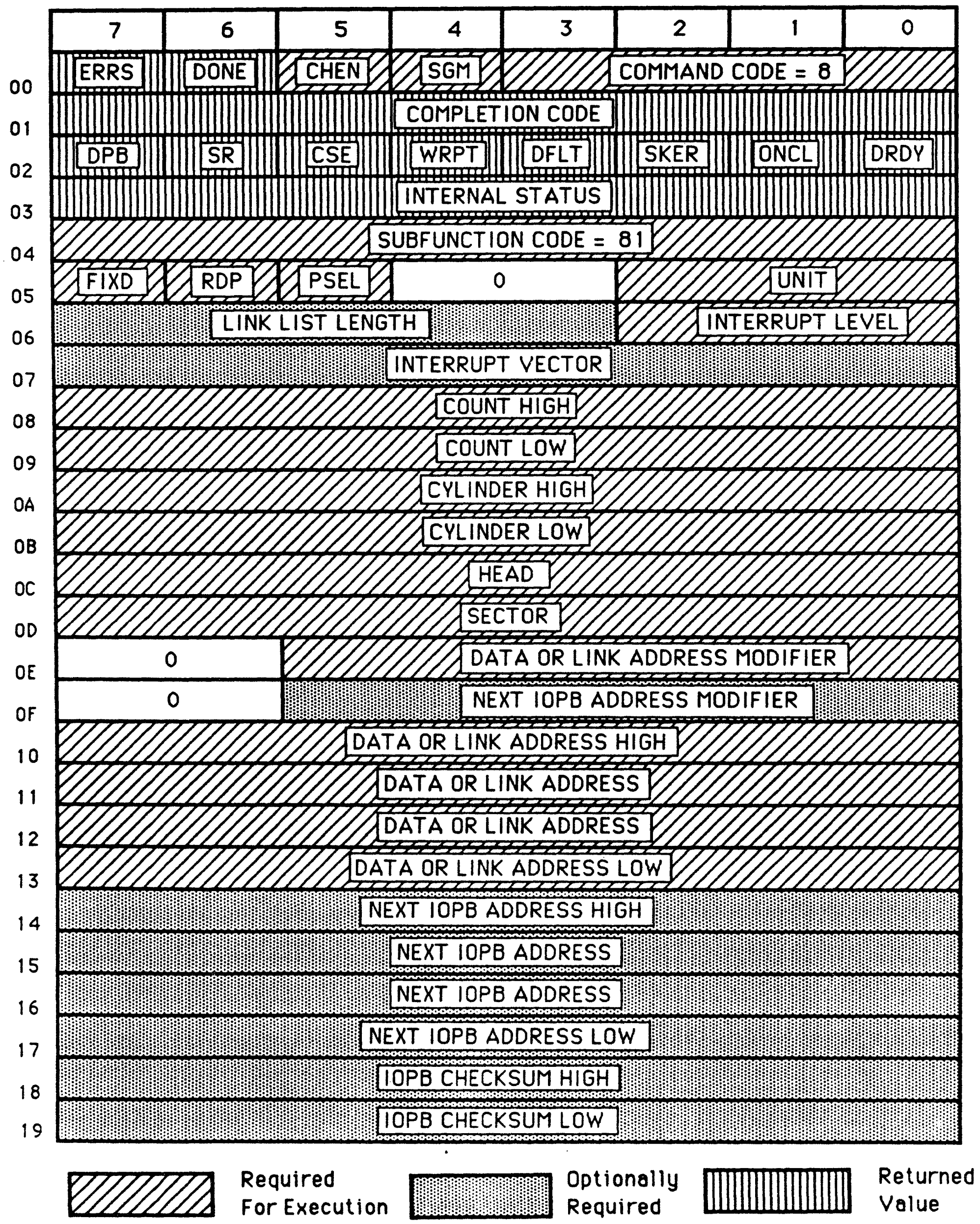
░ Optionally Required

▥ Returned Value

5.21 VERIFY DATA

The 752 verifies the data on the disk: it reads the data from the host and the disk simultaneously, and compares them on a bit-by-bit basis. The granularity of the mismatch reporting is one sector. The ending data address does not indicate where a mismatch error occurred.

VERIFY DATA



	7	6	5	4	3	2	1	0
00	ERRS	DONE	CHEN	SGM	COMMAND CODE = 8			
01	COMPLETION CODE							
02	DPB	SR	CSE	WRPT	DFLT	SKER	ONCL	DRDY
03	INTERNAL STATUS							
04	SUBFUNCTION CODE = 81							
05	FIXD	RDP	PSEL	0		UNIT		
06	LINK LIST LENGTH					INTERRUPT LEVEL		
07	INTERRUPT VECTOR							
08	COUNT HIGH							
09	COUNT LOW							
0A	CYLINDER HIGH							
0B	CYLINDER LOW							
0C	HEAD							
0D	SECTOR							
0E	0		DATA OR LINK ADDRESS MODIFIER					
0F	0		NEXT IOPB ADDRESS MODIFIER					
10	DATA OR LINK ADDRESS HIGH							
11	DATA OR LINK ADDRESS							
12	DATA OR LINK ADDRESS							
13	DATA OR LINK ADDRESS LOW							
14	NEXT IOPB ADDRESS HIGH							
15	NEXT IOPB ADDRESS							
16	NEXT IOPB ADDRESS							
17	NEXT IOPB ADDRESS LOW							
18	IOPB CHECKSUM HIGH							
19	IOPB CHECKSUM LOW							

▨ Required For Execution

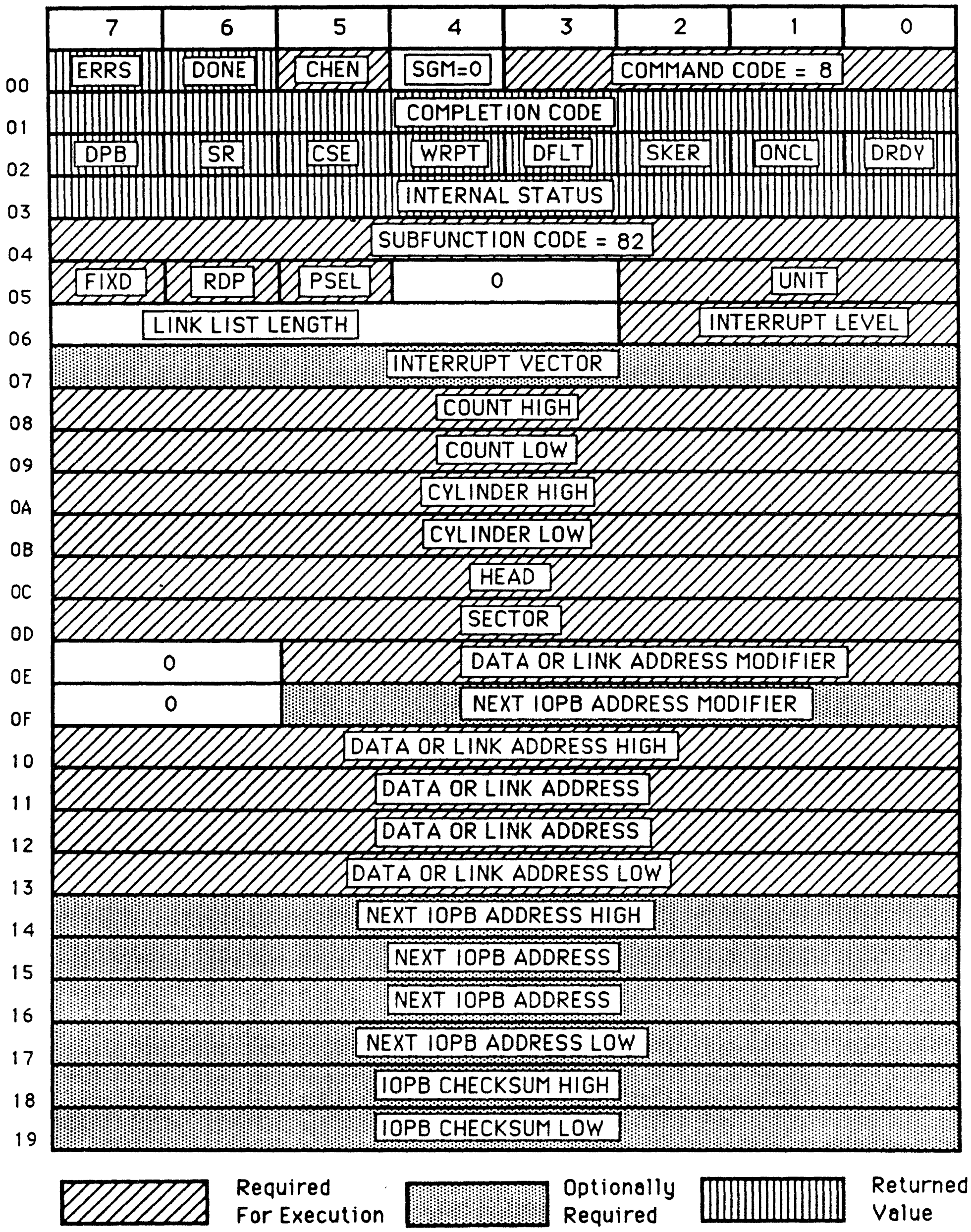
░ Optionally Required

▥ Returned Value

5.22 READ HEADER, HEADER VERIFY, DATA, AND DATA ECC

The 752 reads a sector header, header verify, data, and data ECC. There are always four bytes in the header, but the other fields vary according to the initial 752 set-up. The 752 reads the physical sectors regardless of the interleave factor; it does not cross head or cylinder boundaries. See Section 8.11.

READ HEADER, HEADER VERIFY, DATA, AND DATA ECC



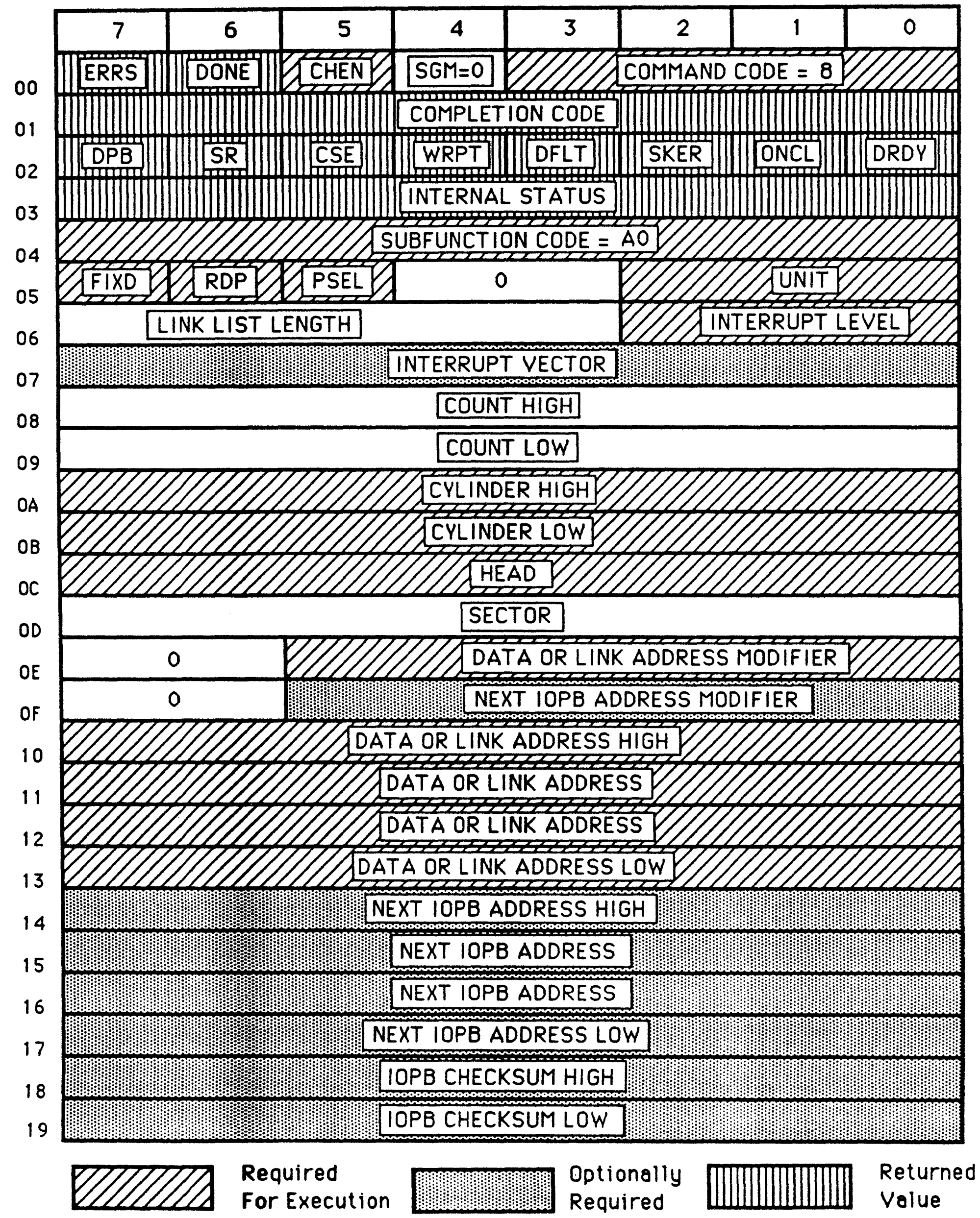
	7	6	5	4	3	2	1	0
00	ERRS	DONE	CHEN	SGM=0	COMMAND CODE = 8			
01	COMPLETION CODE							
02	DPB	SR	CSE	WRPT	DFLT	SKER	ONCL	DRDY
03	INTERNAL STATUS							
04	SUBFUNCTION CODE = 82							
05	FIXD	RDP	PSEL	0		UNIT		
06	LINK LIST LENGTH					INTERRUPT LEVEL		
07	INTERRUPT VECTOR							
08	COUNT HIGH							
09	COUNT LOW							
0A	CYLINDER HIGH							
0B	CYLINDER LOW							
0C	HEAD							
0D	SECTOR							
0E	0		DATA OR LINK ADDRESS MODIFIER					
0F	0		NEXT IOPB ADDRESS MODIFIER					
10	DATA OR LINK ADDRESS HIGH							
11	DATA OR LINK ADDRESS							
12	DATA OR LINK ADDRESS							
13	DATA OR LINK ADDRESS LOW							
14	NEXT IOPB ADDRESS HIGH							
15	NEXT IOPB ADDRESS							
16	NEXT IOPB ADDRESS							
17	NEXT IOPB ADDRESS LOW							
18	IOPB CHECKSUM HIGH							
19	IOPB CHECKSUM LOW							

▨ Required For Execution ░ Optionally Required ▥ Returned Value

5.23 READ DEFECT MAP

The 752 reads the manufacturer's defect map and returns the data to memory in the correct bit order. See Section 8.1.

READ DEFECT MAP

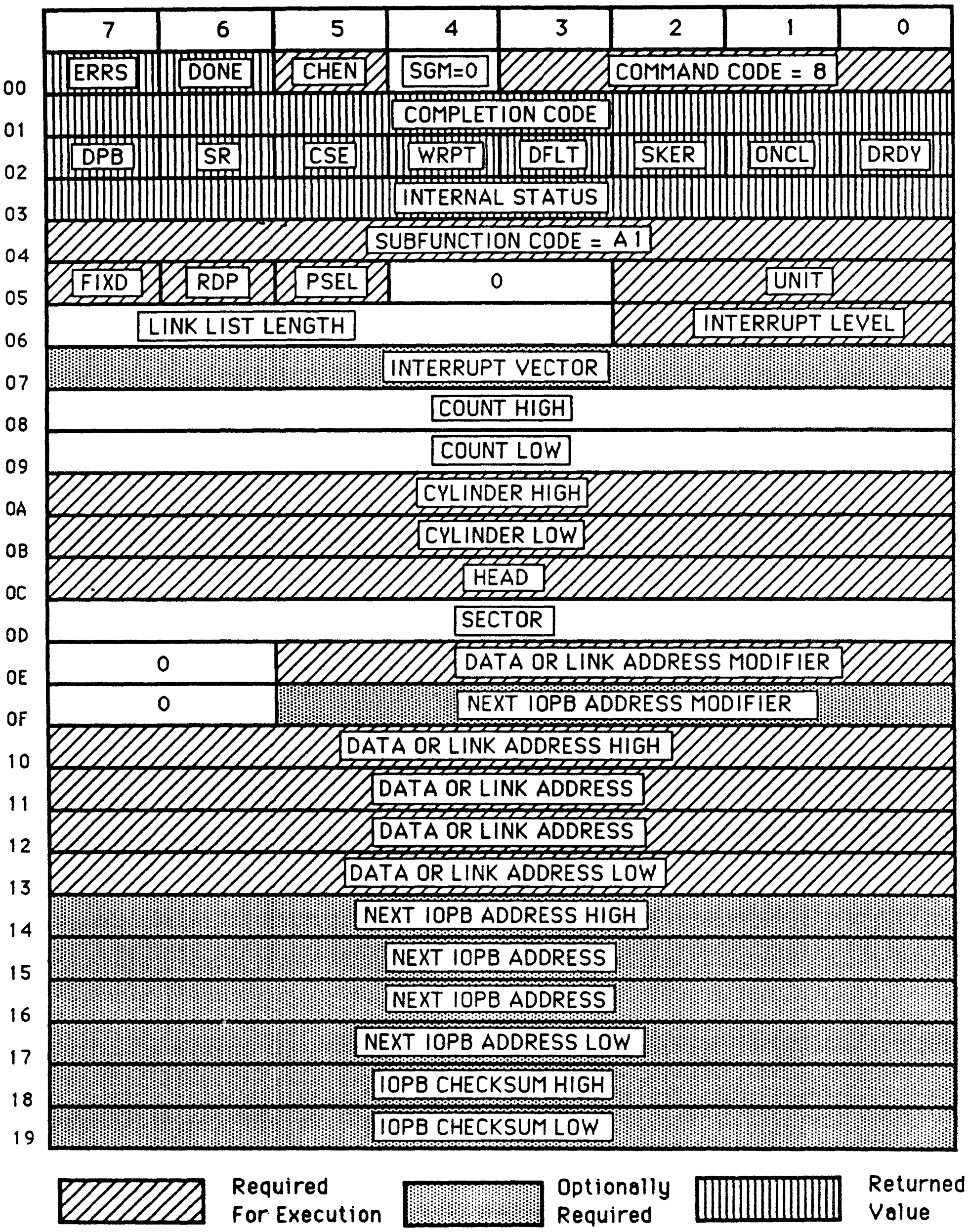


	7	6	5	4	3	2	1	0
00	ERRS	DONE	CHEN	SGM=0	COMMAND CODE = 8			
01	COMPLETION CODE							
02	DPB	SR	CSE	WRPT	DFLT	SKER	ONCL	DRDY
03	INTERNAL STATUS							
04	SUBFUNCTION CODE = A0							
05	FIXD	RDP	PSEL	0		UNIT		
06	LINK LIST LENGTH					INTERRUPT LEVEL		
07	INTERRUPT VECTOR							
08	COUNT HIGH							
09	COUNT LOW							
0A	CYLINDER HIGH							
0B	CYLINDER LOW							
0C	HEAD							
0D	SECTOR							
0E	0		DATA OR LINK ADDRESS MODIFIER					
0F	0		NEXT IOPB ADDRESS MODIFIER					
10	DATA OR LINK ADDRESS HIGH							
11	DATA OR LINK ADDRESS							
12	DATA OR LINK ADDRESS							
13	DATA OR LINK ADDRESS LOW							
14	NEXT IOPB ADDRESS HIGH							
15	NEXT IOPB ADDRESS							
16	NEXT IOPB ADDRESS							
17	NEXT IOPB ADDRESS LOW							
18	IOPB CHECKSUM HIGH							
19	IOPB CHECKSUM LOW							

5.24 READ DEFECT MAP EXTENDED

The 752 bypasses any media defects and reads the manufacturer's defect map from the alternate location on the track. See Section 8.1.

READ DEFECT MAP EXTENDED



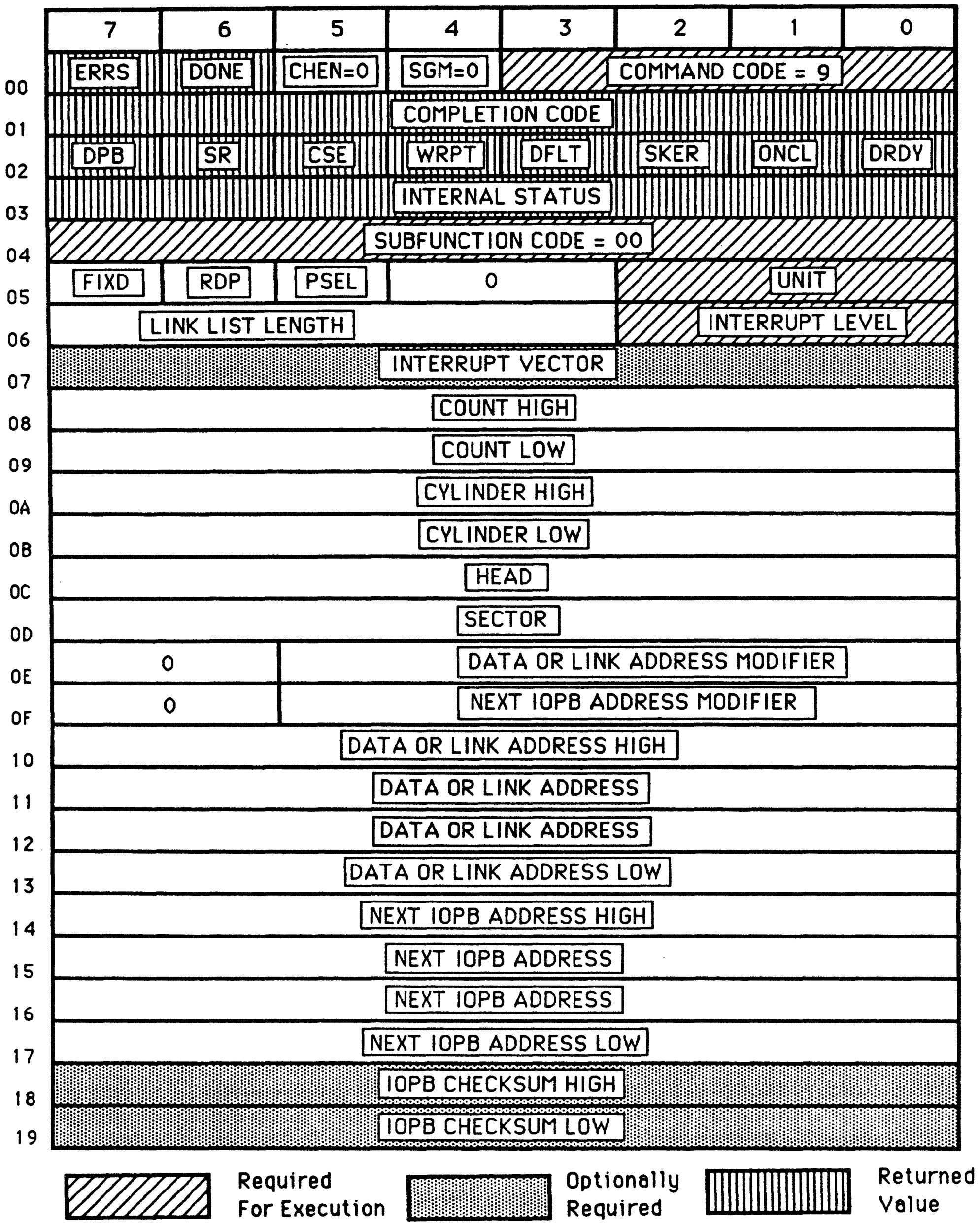
	7	6	5	4	3	2	1	0
00	ERRS	DONE	CHEN	SGM=0	COMMAND CODE = 8			
01	COMPLETION CODE							
02	DPB	SR	CSE	WRPT	DFLT	SKER	ONCL	DRDY
03	INTERNAL STATUS							
04	SUBFUNCTION CODE = A1							
05	FIXD	RDP	PSEL	0		UNIT		
06	LINK LIST LENGTH					INTERRUPT LEVEL		
07	INTERRUPT VECTOR							
08	COUNT HIGH							
09	COUNT LOW							
0A	CYLINDER HIGH							
0B	CYLINDER LOW							
0C	HEAD							
0D	SECTOR							
0E	0		DATA OR LINK ADDRESS MODIFIER					
0F	0		NEXT IOPB ADDRESS MODIFIER					
10	DATA OR LINK ADDRESS HIGH							
11	DATA OR LINK ADDRESS							
12	DATA OR LINK ADDRESS							
13	DATA OR LINK ADDRESS LOW							
14	NEXT IOPB ADDRESS HIGH							
15	NEXT IOPB ADDRESS							
16	NEXT IOPB ADDRESS							
17	NEXT IOPB ADDRESS LOW							
18	IOPB CHECKSUM HIGH							
19	IOPB CHECKSUM LOW							

▨ Required For Execution
░ Optionally Required
▥ Returned Value

5.25 DIAGNOSTICS

The 752 executes the on-board self test diagnostics. Do not chain this IOPB to another IOPB. It cannot be used in conjunction with other IOPBs in the command queue.

DIAGNOSTICS



	7	6	5	4	3	2	1	0
00	ERRS	DONE	CHEN=0	SGM=0	COMMAND CODE = 9			
01	COMPLETION CODE							
02	DPB	SR	CSE	WRPT	DFLT	SKER	ONCL	DRDY
03	INTERNAL STATUS							
04	SUBFUNCTION CODE = 00							
05	FIXD	RDP	PSEL	0	UNIT			
06	LINK LIST LENGTH				INTERRUPT LEVEL			
07	INTERRUPT VECTOR							
08	COUNT HIGH							
09	COUNT LOW							
0A	CYLINDER HIGH							
0B	CYLINDER LOW							
0C	HEAD							
0D	SECTOR							
0E	0		DATA OR LINK ADDRESS MODIFIER					
0F	0		NEXT IOPB ADDRESS MODIFIER					
10	DATA OR LINK ADDRESS HIGH							
11	DATA OR LINK ADDRESS							
12	DATA OR LINK ADDRESS							
13	DATA OR LINK ADDRESS LOW							
14	NEXT IOPB ADDRESS HIGH							
15	NEXT IOPB ADDRESS							
16	NEXT IOPB ADDRESS							
17	NEXT IOPB ADDRESS LOW							
18	IOPB CHECKSUM HIGH							
19	IOPB CHECKSUM LOW							

▨ Required For Execution

░ Optionally Required

▥ Returned Value

SECTION 6: ERROR PROCESSING

6.0 GENERAL

The 752 Error Summary (ERRS) bit, Fatal Error (FERR) bit, and Completion Code represent the controller's status after executing a command. FERR indicates the transfer failed and the 752 requires a Controller Reset before continuing. ERRS only affects the specific IOPB and may be tested in lieu of checking the Completion Code; the 752 does not require a Controller Reset before continuing. The Completion Code informs software that the 752 successfully completed a command, failed to complete a command, or encountered and corrected a problem with one of several internal recovery procedures.

6.1 THE COMPLETION CODE

The 752 posts a Completion Code in IOPB Byte 1 (Status Byte 1); a Completion Code is only valid if DONE is set. Table 6-2 lists the Completion Codes (all codes not listed in this table are reserved). The following subsections describe these codes, along with any required corrective action.

6.1.1 Completion Code Convention

Completion Codes follow a convention that recommends the action required by either the software driver or manual intervention. The byte's upper nibble is the recovery code, and the lower nibble is the actual error code (see Table 6-1).

Recovery Code	Recovery Procedure
0	No Action / Status Only
1	Non-retryable Programming Error
3	Successfully Recovered Soft Error
4	Hard Error / Retry
6	Hard Error / Reset and Retry
7	Fatal Hardware Error
8	Miscellaneous Error
9	Requires Manual Intervention

Table 6-1. Recovery Codes

6.1.1 Completion Code Convention (continued)

Action	Code (Hex)	Description
No Action / Status Only	00	Successful Completion
Non-retryable Programming Errors	10	Illegal Cylinder Address
	11	Illegal Head Address
	12	Illegal Sector Address
	13	Count Zero
	14	Unimplemented Command
	15-1B	Illegal Field Lengths 1-7
	1C	Illegal Scatter/Gather Length
	1D	Not Enough Sectors/Track
	1E	Next IOPB Alignment Error
	1F	Scatter/Gather Addr. Alignment
	20	Scatter/Gather With Auto ECC
Successfully Recovered Soft Errors	30	Soft ECC Corrected
	31	ECC Ignored
	32	Auto Seek Retry Recovered
	33	Soft Retry Recovered
Hard Errors/Retry	40	Hard Data ECC
	41	Header Not Found
	42	Drive Not Ready
	43	Operation Timeout
	44	VMEDMA Timeout
	45	Disk Sequencer Error
	46	FIFO Parity Error
	47	Dual Port Busy Timeout
	48	Header ECC Error
	49	Read Verify
	4A	Fatal VMEDMA Error
	4B	VMEbus Error
Hard Errors - Reset/Retry	60	Drive Faulted
	61	Header Error/Cylinder
	62	Header Error/Head
	63	Drive Not On-cylinder
	64	Seek Error
Fatal Hardware Errors	70	Illegal Sector Size
	71	Firmware Failure
Miscellaneous Errors	80	Soft ECC
Requires Manual Intervention	90	Write-protect Error

Table 6-2. Summary of Completion Codes

6.1.2 Completion Code Descriptions

6.1.2.1 No Action / Status Only

Typically, the following Completion Code requires no action; the 752 returns the code for status only.

Code(H)	Description
00	SUCCESSFUL COMPLETION — Not an error; indicates the IOPB is complete.

6.1.2.2 Non-retryable Programming Errors

This group of errors is usually encountered while debugging drivers; they should not occur in a normal operating system environment.

Code(H)	Description
10	ILLEGAL CYLINDER ADDRESS — Host software specified a cylinder address greater than the maximum cylinder number specified in the last Set Drive Parameters command for this drive.
11	ILLEGAL HEAD ADDRESS — Host software specified a head address greater than the maximum head address specified in the last Set Drive Parameters command for this drive.
12	ILLEGAL SECTOR ADDRESS — Host software specified a sector address greater than the maximum sector number specified in the last Set Drive Parameters command for this drive.
13	COUNT ZERO — Host software issued the 752 an IOPB that required a count, but the count was zero. Read, Write, and Format commands require a valid count.
14	UNIMPLEMENTED COMMAND — This error occurs on all reserved commands.
15	ILLEGAL FIELD LENGTH 1 — See Section 8.2.2.1.
16	ILLEGAL FIELD LENGTH 2 — See Section 8.2.2.2.
17	ILLEGAL FIELD LENGTH 3 — See Section 8.2.2.3.

6.1.2.2 Non-retryable Programming Errors (continued)

Code(H)	Description
18	ILLEGAL FIELD LENGTH 4 — See Section 8.2.2.4.
1A	ILLEGAL FIELD LENGTH 6 — See Section 8.2.2.5.
1B	ILLEGAL FIELD LENGTH 7 — See Section 8.2.2.6.
1C	ILLEGAL SCATTER/GATHER LENGTH — The linked list specified a number of words to transfer that does not agree with the amount of data contained in the requested number of sectors for transfer.
1D	NOT ENOUGH SECTORS PER TRACK — The format routine was unable to format since too few sectors were actually available on the track.
1E	NEXT IOPB ALIGNMENT ERROR — The Next IOPB Address did not start on a 16-bit boundary; the 752 does not execute the NIOPB.
1F	SCATTER/GATHER ADDRESS ALIGNMENT ERROR — A Scatter/Gather address did not start on a 16-bit boundary.
20	SCATTER/GATHER WITH AUTO ECC ERROR — A Scatter/Gather operation ended with a soft ECC error; due to Scatter/Gather boundaries, the 752 did not automatically correct the error, but reverted to ECC Mode 0.

6.1.2.3 Successfully Recovered Soft Errors

This group of errors is for status only. If some errors recur often, the operating system should try to map out the sectors involved. Allowing these errors to recur degrades performance.

Code(H)	Description
30	SOFT ECC CORRECTED — The 752 detected and corrected one or more ECC errors, during a disk read, in ECC Mode 2.
31	ECC ERROR IGNORED — The 752 detected, but ignored, an ECC error (during a Read command, in ECC Mode 1) and continued the transfer.

6.1.2.3 Successfully Recovered Soft Errors (continued)

Code(H)	Description
32	AUTO SEEK RETRY RECOVERED — The 752 completed the transfer successfully but, during the transfer, it recovered from an error by resetting the drive.
33	SOFT RETRY RECOVERED — A retry was successful: either by setting RBC or issuing a zero latency read.

6.1.2.4 Hard Errors/Retry

These errors indicate the transfer failed; retry the operation. If several retries fail, manual intervention is required or the operating system may crash.

Code(H)	Description
40	HARD DATA ECC ERROR — The 752 detected a hard data ECC error in the data field during a Read command. Retry the previous Read operation.
41	HEADER NOT FOUND — The 752 cannot find the requested sector. The controller searches for one disk revolution plus one sector to locate the header. See Section 9.3.2.
42	DRIVE NOT READY — The selected drive is not ready, but not faulted; issue a Drive Reset. Causes include: o Drive not up-to-speed. o Drive hardware error. o Bad or improperly connected cable(s). o No drive of the specified unit number is connected to the 752.
43	OPERATION TIMEOUT — The 752 did not complete the IOPB within a two second timeout period.
44	VMEDMA TIMEOUT — The DMA controller did not complete within its allotted time limit. One reason could be that memory did not respond in time.
45	DISK SEQUENCER ERROR — The disk sequencer did not complete its task within the allotted time limit.

6.1.2.4 Hard Errors/Retry (continued)

Code(H)	Description
45	DISK SEQUENCER ERROR (continued) — The 752 cannot send or receive the appropriate signals from the selected drive. Causes include: o Improper or defective cabling. o Unformatted drive.
46	FIFO PARITY ERROR — The transfer failed; the 752 detected a FIFO buffer parity error.
47	DUAL PORT BUSY — The 752 timed out while waiting for the port on a dual ported drive. The timeout is two seconds.
48	HEADER ECC ERROR — The 752 found a header match, but the Header ECC did not compare.
49	READ VERIFY ERROR — The data read from the disk did not match the data read from memory.
4A	FATAL VMEDMA ERROR — The VMEDMA stopped for no apparent reason. The count nor the address overflowed, and there was no bus error.
4B	VMEBUS ERROR — The VME BERR* signal was asserted while the 752 was bus master (see the VMEbus Specification).

6.1.2.5 Hard Errors - Reset/Retry

This group of errors indicate the transfer failed. Software should issue a Drive Reset command to the drive in use before retrying the operation.

Code(H)	Description
60	DRIVE FAULTED — The selected drive is faulted. Issue a Drive Reset. If the fault persists, you must intervene.
61	HEADER ERROR/CYLINDER — The cylinder address did not match during a sector search. Check the cylinder address and retry the operation.
62	HEADER ERROR/HEAD — The head address did not match during a sector search.

6.1.2.5 Hard Errors - Reset/Retry (continued)

Code(H)	Description
63	DRIVE NOT ON-CYLINDER — At some point during the transfer, the 752 expected the drive to be on-cylinder, and it was not.
64	SEEK ERROR — The disk drive reported a seek error.

6.1.2.6 Fatal Hardware Errors

These errors indicate the hardware failed. Manual intervention or a Controller Reset may be the only recovery approach.

Code(H)	Description
70	ILLEGAL SECTOR SIZE — The disk drive's sector size is not large enough to hold the header, data, and specified field lengths. Verify your drive's sector switch settings against the 752's minimum sector size requirements.
71	FIRMWARE FAILURE — Flag settings or counter values are inconsistent with the firmware routines being executed. Document the conditions and call Xylogics.

6.1.2.7 Miscellaneous Errors

Code(H)	Description
80	SOFT ECC ERROR — The 752 detected a correctable error in the data field of the current sector, during a Read operation, in ECC Mode 0. Software must perform the final correction. See Section 6.3.

6.1.2.8 Requires Manual Intervention

The write-protect error requires you to manually remove the write-protection.

Code(H)	Description
90	WRITE-PROTECT ERROR — A command that writes to the disk (e.g., Write, Format, Write Track Headers) is issued, but the drive is write-protected.

6.2 SOFT ERROR COMPLETION CODES

The 752 updates the IOPB with the last error it encounters; it may overwrite previous soft errors with a new soft error status or a hard error status.

6.3 ERROR CORRECTION CODE

Most ECC algorithms require retrying the operation at least once before attempting the correction. When RBC is set, the 752 automatically retries the operation once before applying the correction algorithm.

6.3.1 Error Correction Code - Mode 0

When using Mode 0, the following procedure corrects a soft ECC error. The 752 provides a pattern and offset for the correction process.

1. Reserve 32 bits of storage for the shifted ECC pattern, and initialize them to zero. Take the ECC Pattern word from the IOPB and put it in the lowest 16 bits of the reserved space.
2. Get the offset from the IOPB and decrement by one. This makes the count zero-based instead of one-based.
3. Use the three low order bits of the offset as a count to shift the pattern the number of count bits left.
4. Divide the bit address by eight (by performing three logical shifts to the right). The result is the word offset into the bad sector. Adding this offset to the starting memory address of the sector in error creates a pointer to the first word to be corrected.
5. Exclusive-OR the three Memory bytes at the pointer and the two Pattern words generated in step 1.

6.3.2 Error Correction Code - Mode 1

The 752 does not correct any detected errors in Mode 1. After completing the operation, it posts a Completion Code indicating that at least one ECC error occurred during the transfer.

6.3.3 Error Correction Code - Mode 2

The 752 automatically corrects a soft ECC error in this mode. The 752 determines the pattern and offset, completes the DMA, and goes to host memory to fetch the data in error; it corrects the data, and returns it to memory.

6.4 FATAL ERROR CODES

If a fatal error occurs, the 752 sets FERR in the Status Register and posts the error code in the Fatal Error Register. (The following error codes appear only in the Fatal Error Register.) The only way to clear a fatal error is by issuing a Controller Reset (CRST).

Code(H)	Description
E0	RESERVED.
E1	IRAM SELF TEST FAILURE — The 752 tests the IRAM with an incrementing data pattern then tests it with a decrementing pattern. An error indicates a bad IRAM.
E2	RESERVED.
E3	MAINTENANCE TEST 3 FAILURE — The 752 tests the Writable Control Store in the DSKCEL with an incrementing data pattern then tests it with a decrementing pattern. An error indicates a bad DSKCEL.
E4	MAINTENANCE TEST 4 FAILURE — The 752 shifts a pattern of 0's and 1's through the Header Shift Register (HSR). An error indicates a bad HSR.
E5	MAINTENANCE TEST 5 FAILURE — The 752 writes, and then reads, the VMEDMA Registers. An error indicates a bad VMEDMA.
E6	MAINTENANCE TEST 6 FAILURE -- There is a problem with the REGCEL chip.

6.4 FATAL ERROR CODES (continued)

Code(H)	Description
E7	MAINTENANCE TEST 7 FAILURE — The FIFO parity circuit failed its diagnostic.
E8	MAINTENANCE TEST 8 FAILURE — The 752 fills the Disk FIFO with sequential data and then reads it. An error indicates a problem with the DSKCEL or FIFO.
F0	IOPB CHECKSUM MISCOMPARE — The generated checksum did not match the appended checksum. This error can only occur while IOPB checksum feature is active. ICS is controlled via controller parameters. See Section 8.11.
F1	IOPB DMA FATAL — The 752 did not complete the DMA within the prescribed timeout period. The memory could be defective or not present; the 752 may not have been able to become bus master.
F2	IOPB ADDRESS ALIGNMENT ERROR — The IOPB address did not start on a 16-bit boundary. Change the address of the IOPB and retry.
F3	FIRMWARE ERROR — Flag settings or counter values are inconsistent with the firmware routines being executed; the IOPB cannot DMA the appropriate error status. The 752's state is indeterminate; you must issue a Controller Reset.
F5	ILLEGAL MAINTENANCE MODE TEST NUMBER — The command is invalid, or the Maintenance mode jumper is not in.
F6	ACFAIL ASSERTED — The VMEbus signal ACFAIL is asserted, causing the 752 to stop. Correct the problem asserting ACFAIL and then reset the 752.

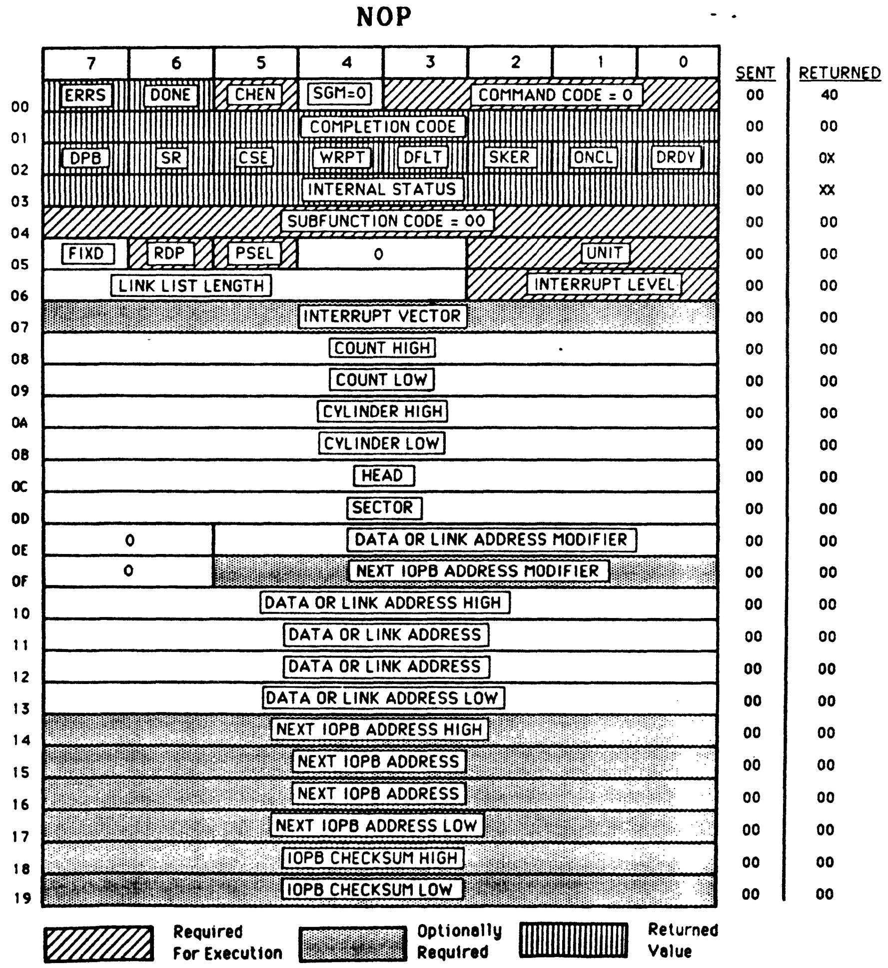
SECTION 7: A TUTORIAL IN PROGRAMMING THE 752

7.0 GENERAL

This section describes programming the 752 for basic use. This tutorial programming procedure begins with a single NOP IOPB and progresses to normal Read and Write commands. Each section builds on the previous section's information. (In the Sent/Returned portion of each sample IOPB, the x represents an indeterminate value that depends on the external conditions.)

7.1 NO OPERATION (NOP)

The NOP command allows you to become familiar with the 752 programming interface.



NOP

	7	6	5	4	3	2	1	0	SENT	RETURNED
00	ERRS	DONE	CHEN	SGM=0	COMMAND CODE = 0				00	40
01	COMPLETION CODE								00	00
02	DPB	SR	CSE	WRPT	DFLT	SKER	ONCL	DRDY	00	0X
03	INTERNAL STATUS								00	XX
04	SUBFUNCTION CODE = 00								00	00
05	FIXD	RDP	PSEL	0		UNIT			00	00
06	LINK LIST LENGTH					INTERRUPT LEVEL			00	00
07	INTERRUPT VECTOR								00	00
08	COUNT HIGH								00	00
09	COUNT LOW								00	00
0A	CYLINDER HIGH								00	00
0B	CYLINDER LOW								00	00
0C	HEAD								00	00
0D	SECTOR								00	00
0E	0		DATA OR LINK ADDRESS MODIFIER						00	00
0F	0		NEXT IOPB ADDRESS MODIFIER						00	00
10	DATA OR LINK ADDRESS HIGH								00	00
11	DATA OR LINK ADDRESS								00	00
12	DATA OR LINK ADDRESS								00	00
13	DATA OR LINK ADDRESS LOW								00	00
14	NEXT IOPB ADDRESS HIGH								00	00
15	NEXT IOPB ADDRESS								00	00
16	NEXT IOPB ADDRESS								00	00
17	NEXT IOPB ADDRESS LOW								00	00
18	IOPB CHECKSUM HIGH								00	00
19	IOPB CHECKSUM LOW								00	00

Figure 7-1. Sample NOP IOPB

7.1.1 Allocating Memory for an IOPB

First, allocate space in host memory to store the IOPB. This allocation is a function of the operating system or the program that is currently executing. Next, set up the IOPB to execute a simple NOP command.

7.1.2 Point the 752 to the IOPB

The IOPB is now in host memory. Point the 752 to the IOPB by loading the IOPB address and address modifier into the appropriate 752 registers. The 752 looks for the IOPB at the physical address to which the registers point.

NOTE

> Make sure the address compensates for any memory mapping that may be done between virtual and physical addressing in your system.

7.1.3 Starting the Operation

The 752 now points to the IOPB in host memory. Setting AIO in the CSR directs the 752 to process the IOPB.

7.1.4 752 Operation

At this point, the 752 performs the following functions:

1. Clears AIOP and sets BUSY.
2. Reads the IOPB from host memory.
3. Decodes the command.
4. Performs the operation (NOP).
5. Sets the DONE bit.
6. Updates the IOPB.
7. Puts the completed IOPB's address into the registers.
8. Sets RIO.
9. Clears BUSY.

7.1.5 Command Completion

Software has been polling RIO (since interrupts are not enabled [Interrupt Level = 0]). The 752 sets RIO when it is done. Software should get the completed IOPB's address from the registers, and then clear RIO. This completes the NOP command.

NOTE

Do not poll the DONE bit in the IOPB. The 752 sets DONE while the rest of the IOPB is still updating.

7.1.6 Returned Values

DONE is set in the returned IOPB. Status Byte 2 reflects the status of Disk Drive 0. Status Byte 3 reflects the 752's internal status.

NOTE

Status Byte 3 is proprietary to Xylogics and may change definition without notice.

7.2 READ CONTROLLER PARAMETERS

Next, implement a Read Parameters command with a Controller Parameters subfunction (see Section 4.2). This command returns several controller parameters in the IOPB. See Figure 7-2.

7.2.1 Execute the IOPB

Set up the IOPB in host memory; point the 752 to the IOPB. Set AIO and the 752 executes the IOPB in Figure 7-2.

7.2.2 752 Operation

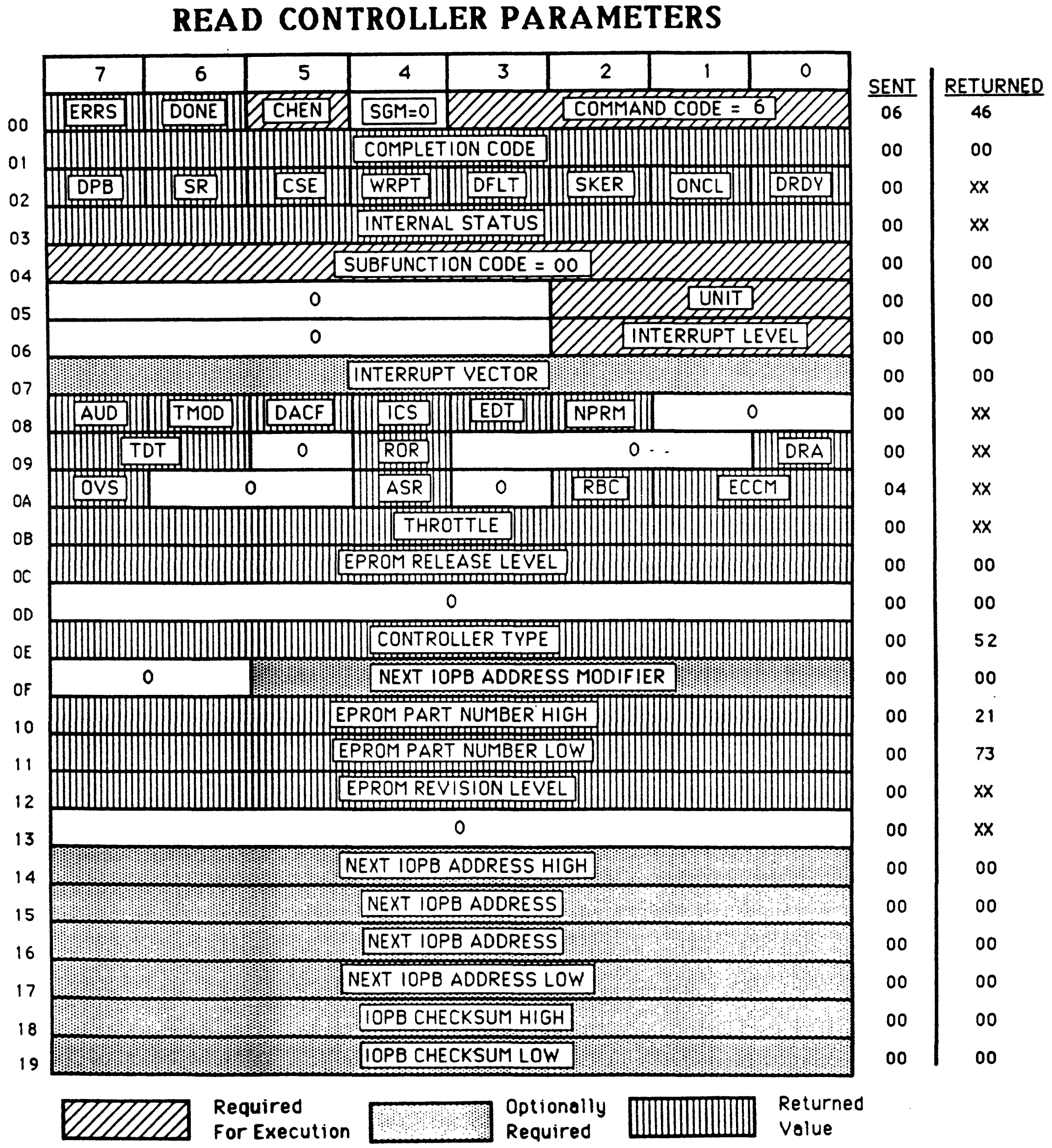
The controller operation changes slightly from the example in Section 7.1.4:

The 752 performs the Read Controller Parameters operation instead of the NOP. The controller gets the parameters from its internal store, and puts them in the proper IOPB locations. The 752 fully updates the IOPB, including the returned values.

7.2.3 The Returned IOPB

The values in the returned IOPB describe the last setting of the software-programmable parameters. Determine if each value works for your application. After making any necessary changes, write the parameters back to the 752.

Specific bytes have known values. The Controller Type byte contains a 53H; the EPROM Part Number bytes contain 21H and 73H. See Section 4.2 for more information.



READ CONTROLLER PARAMETERS

	7	6	5	4	3	2	1	0	SENT	RETURNED
00	ERRS	DONE	CHEN	SGM=0	COMMAND CODE = 6				06	46
01	COMPLETION CODE								00	00
02	DPB	SR	CSE	WRPT	DFLT	SKER	ONCL	DRDY	00	XX
03	INTERNAL STATUS								00	XX
04	SUBFUNCTION CODE = 00								00	00
05	0					UNIT			00	00
06	0					INTERRUPT LEVEL			00	00
07	INTERRUPT VECTOR								00	00
08	AUD	TMOD	DACF	ICS	EDT	NPRM	0		00	XX
09	TDT		0	ROR	0 - -			DRA	00	XX
0A	OVS	0		ASR	0	RBC	ECCM		04	XX
0B	THROTTLE								00	XX
0C	EPROM RELEASE LEVEL								00	00
0D	0								00	00
0E	CONTROLLER TYPE								00	52
0F	0		NEXT IOPB ADDRESS MODIFIER						00	00
10	EPROM PART NUMBER HIGH								00	21
11	EPROM PART NUMBER LOW								00	73
12	EPROM REVISION LEVEL								00	XX
13	0								00	XX
14	NEXT IOPB ADDRESS HIGH								00	00
15	NEXT IOPB ADDRESS								00	00
16	NEXT IOPB ADDRESS								00	00
17	NEXT IOPB ADDRESS LOW								00	00
18	IOPB CHECKSUM HIGH								00	00
19	IOPB CHECKSUM LOW								00	00

▨ Required For Execution
░ Optionally Required
▥ Returned Value

Figure 7-2. Sample Read Controller Parameters IOPB

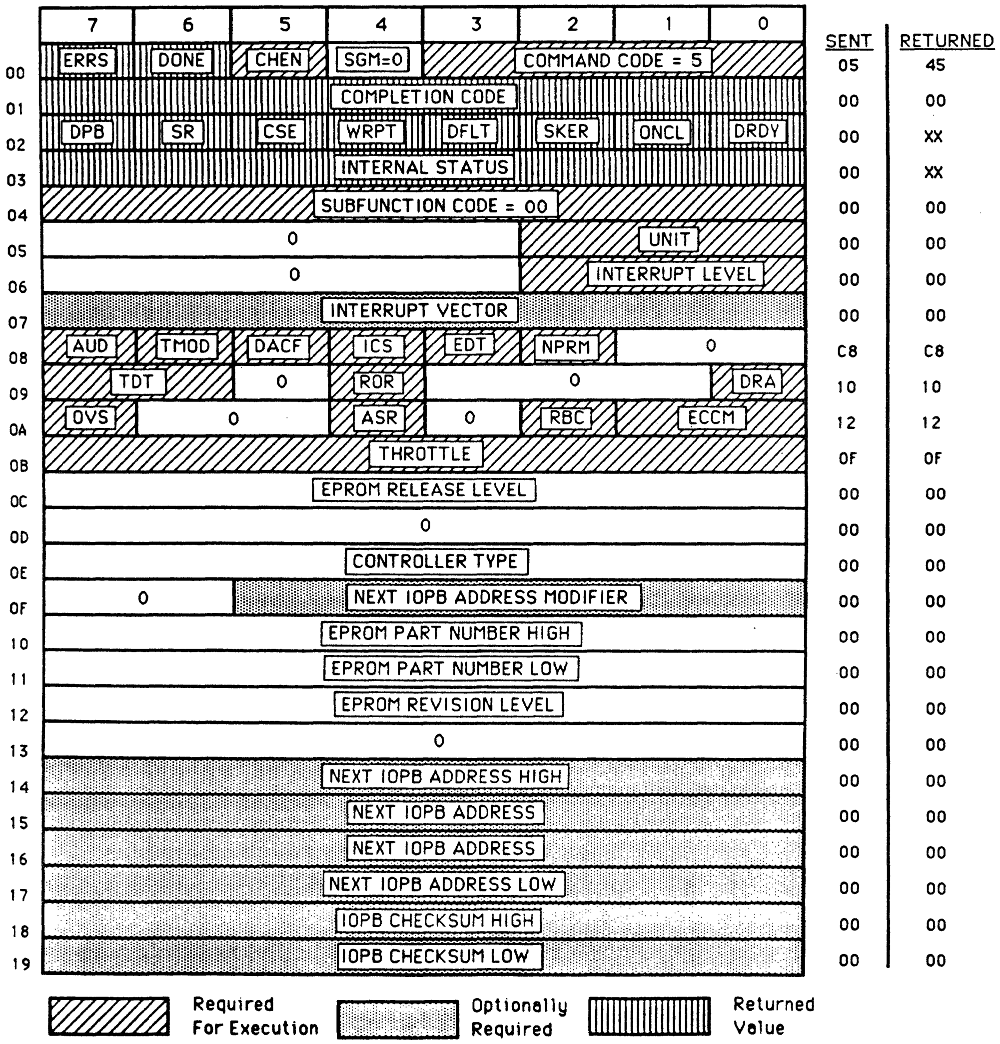
7.3 WRITE CONTROLLER PARAMETERS

Next, write the controller parameters. Xylogics recommends reading the current parameters, modifying the ones in question, and then writing them back to the 752. This method allows you to change only those parameters that affect your system.

7.3.1 752 Operation

The 752 executes the IOPB slightly different than in Sections 7.1.4 and 7.2.2: it performs this function by taking the values of all programmable parameters out of the IOPB and setting the appropriate flags and variables in its internal code.

WRITE CONTROLLER PARAMETERS



	7	6	5	4	3	2	1	0	SENT	RETURNED
00	ERRS	DONE	CHEN	SGM=0	COMMAND CODE = 5				05	45
01	COMPLETION CODE								00	00
02	DPB	SR	CSE	WRPT	DFLT	SKER	ONCL	DRDY	00	XX
03	INTERNAL STATUS								00	XX
04	SUBFUNCTION CODE = 00								00	00
05	0					UNIT			00	00
06	0					INTERRUPT LEVEL			00	00
07	INTERRUPT VECTOR								00	00
08	AUD	TMOD	DACF	ICS	EDT	NPRM	0		C8	C8
09	TDT		0	ROR	0			DRA	10	10
0A	OVS	0		ASR	0	RBC	ECCM		12	12
0B	THROTTLE								0F	0F
0C	EPROM RELEASE LEVEL								00	00
0D	0								00	00
0E	CONTROLLER TYPE								00	00
0F	0		NEXT IOPB ADDRESS MODIFIER						00	00
10	EPROM PART NUMBER HIGH								00	00
11	EPROM PART NUMBER LOW								00	00
12	EPROM REVISION LEVEL								00	00
13	0								00	00
14	NEXT IOPB ADDRESS HIGH								00	00
15	NEXT IOPB ADDRESS								00	00
16	NEXT IOPB ADDRESS								00	00
17	NEXT IOPB ADDRESS LOW								00	00
18	IOPB CHECKSUM HIGH								00	00
19	IOPB CHECKSUM LOW								00	00

Figure 7-3. Sample Write Controller Parameters IOPB

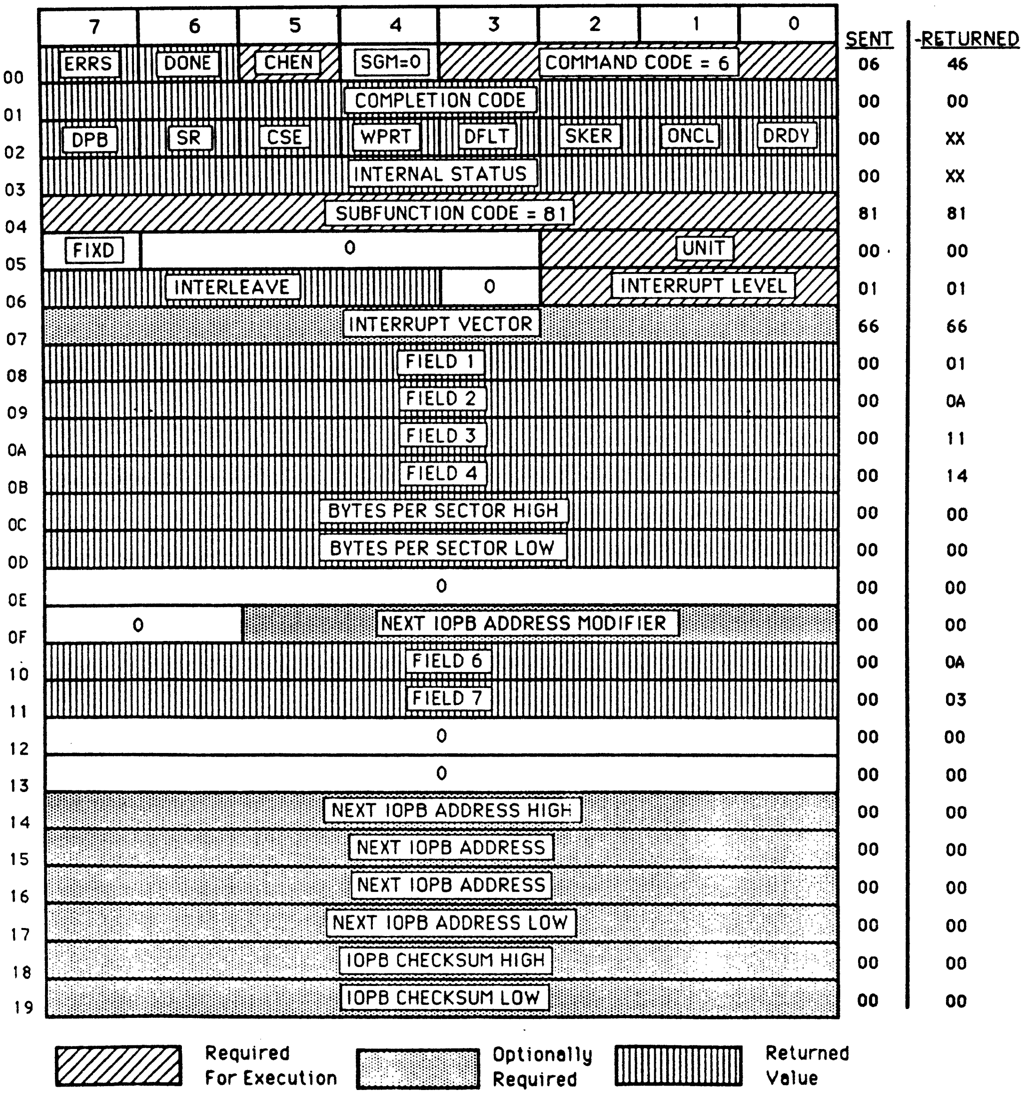
7.4 READ/WRITE FORMAT PARAMETERS

The format parameters are handled similarly to the controller parameters. Use extra caution when modifying the format parameters as improper selection may cause data corruption and/or unreliable operation. The data field size is the only parameter Xylogics recommends changing.

7.4.1 Execute the IOPB with Interrupts

Building on 752 functionality, enable interrupts for this example by specifying an interrupt level and vector.

READ FORMAT PARAMETERS



	7	6	5	4	3	2	1	0	SENT	RETURNED
00	ERRS	DONE	CHEN	SGM=0	COMMAND CODE = 6				06	46
01	COMPLETION CODE								00	00
02	DPB	SR	CSE	WPRT	DFLT	SKER	ONCL	DRDY	00	XX
03	INTERNAL STATUS								00	XX
04	SUBFUNCTION CODE = 81								81	81
05	FIXD	0				UNIT			00	00
06	INTERLEAVE				0	INTERRUPT LEVEL			01	01
07	INTERRUPT VECTOR								66	66
08	FIELD 1								00	01
09	FIELD 2								00	0A
0A	FIELD 3								00	11
0B	FIELD 4								00	14
0C	BYTES PER SECTOR HIGH								00	00
0D	BYTES PER SECTOR LOW								00	00
0E	0								00	00
0F	0			NEXT IOPB ADDRESS MODIFIER					00	00
10	FIELD 6								00	0A
11	FIELD 7								00	03
12	0								00	00
13	0								00	00
14	NEXT IOPB ADDRESS HIGH								00	00
15	NEXT IOPB ADDRESS								00	00
16	NEXT IOPB ADDRESS								00	00
17	NEXT IOPB ADDRESS LOW								00	00
18	IOPB CHECKSUM HIGH								00	00
19	IOPB CHECKSUM LOW								00	00

▨ Required For Execution
░ Optionally Required
▥ Returned Value

Figure 7-4. Sample Read Format Parameters IOPB

7.4.2 752 Operation

The 752 performs the operation almost identically to the examples in Sections 7.2.2 and 7.3.1, but with two additional steps. It makes sure the new format parameters are within the valid ranges. After the 752 sets RIO, it performs an interrupt sequence.

7.4.3 Command Completion

Enabling interrupts modifies the command completion. Software does not poll RIO when it is set, but may be off doing something else (probably waiting for an interrupt). When the interrupt occurs, hardware and software execute an Interrupt Service Routine (ISR) and process the interrupt. Hardware resets the actual hardware interrupt when the ISR is called.

The ISR reads the address of the completed IOPB from the registers, and clears RIO. This completes the Read/Write Format Parameters operation.

7.4.4 Returned Values

Figure 7-4 illustrates the read portion of this subsection. The 752 returns the data for which it was last programmed. The sector size is set to 512 (200H). The other fields are all set to the recommended values.

7.5 READ/WRITE DRIVE PARAMETERS

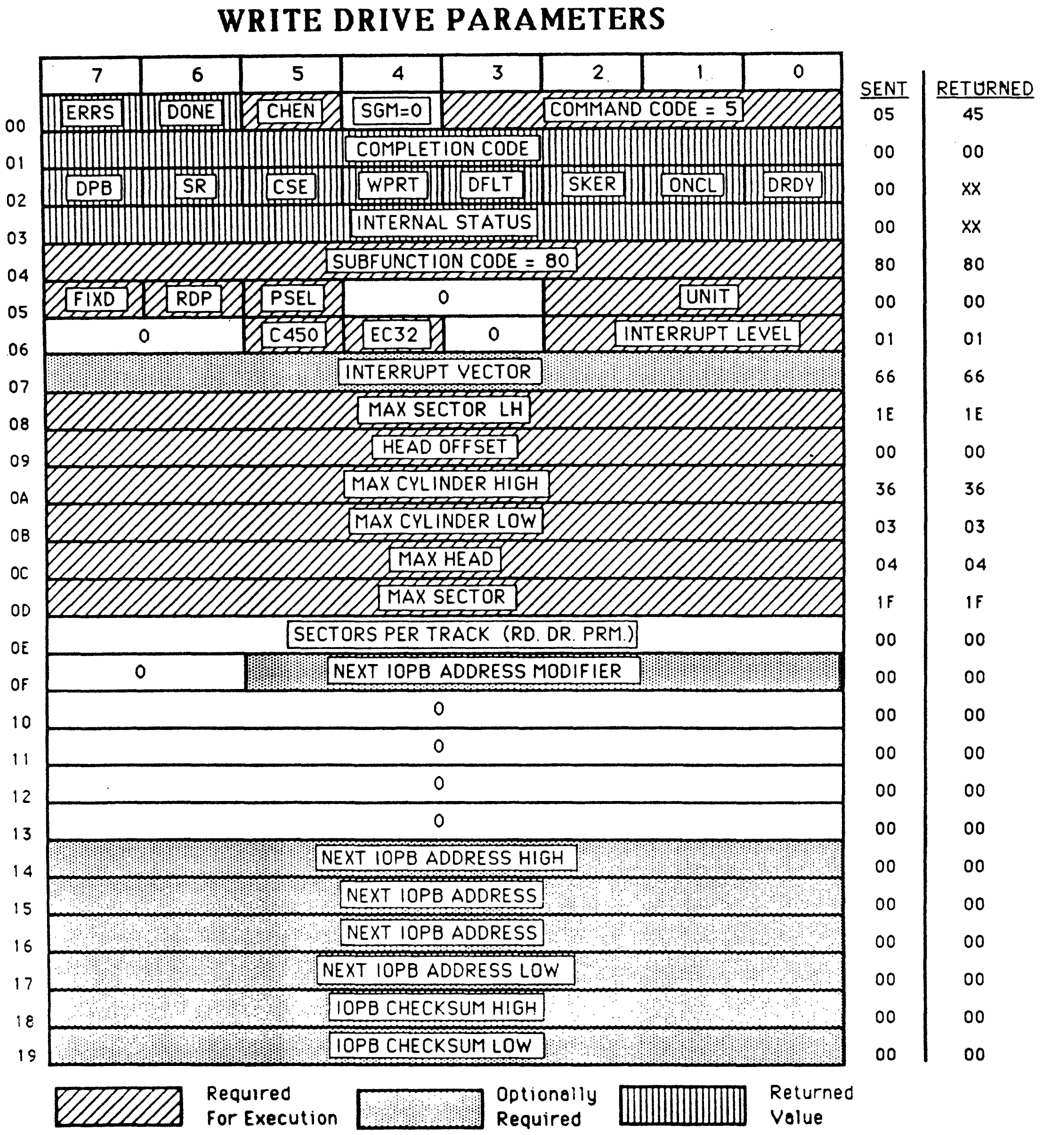
The Drive Parameters commands allow you to configure the 752 to your drive's size and parameters. Section 4.3 describes the size and configuration variables that may be modified with these commands. The operation is similar to both format and controller Parameters.

7.5.1 752 Operation

On a Write Drive Parameters command, the 752 performs an operation similar to that of both controller and format parameters. The Read Drive Parameters function differs in that the 752 returns the number of physical sectors on the drive.

The 752 selects the disk drive specified in the Unit bits. It times the interval between index pulses and, using this time value, counts the number of sector pulses. The 752 puts this count into Byte E of the IOPB. This count is the number of sectors per track. See Figure 7-5.

7.5.1 752 Operation (continued)



WRITE DRIVE PARAMETERS

	7	6	5	4	3	2	1	0	SENT	RETURNED
00	ERRS	DONE	CHEN	SGM=0	COMMAND CODE = 5				05	45
01	COMPLETION CODE								00	00
02	DPB	SR	CSE	WPRT	DFLT	SKER	ONCL	DRDY	00	XX
03	INTERNAL STATUS								00	XX
04	SUBFUNCTION CODE = 80								80	80
05	FIXD	RDP	PSEL	0		UNIT			00	00
06	0		C450	EC32	0	INTERRUPT LEVEL			01	01
07	INTERRUPT VECTOR								66	66
08	MAX SECTOR LH								1E	1E
09	HEAD OFFSET								00	00
0A	MAX CYLINDER HIGH								36	36
0B	MAX CYLINDER LOW								03	03
0C	MAX HEAD								04	04
0D	MAX SECTOR								1F	1F
0E	SECTORS PER TRACK (RD. DR. PRM.)								00	00
0F	0		NEXT IOPB ADDRESS MODIFIER						00	00
10	0								00	00
11	0								00	00
12	0								00	00
13	0								00	00
14	NEXT IOPB ADDRESS HIGH								00	00
15	NEXT IOPB ADDRESS								00	00
16	NEXT IOPB ADDRESS								00	00
17	NEXT IOPB ADDRESS LOW								00	00
18	IOPB CHECKSUM HIGH								00	00
19	IOPB CHECKSUM LOW								00	00

▨ Required For Execution

░ Optionally Required

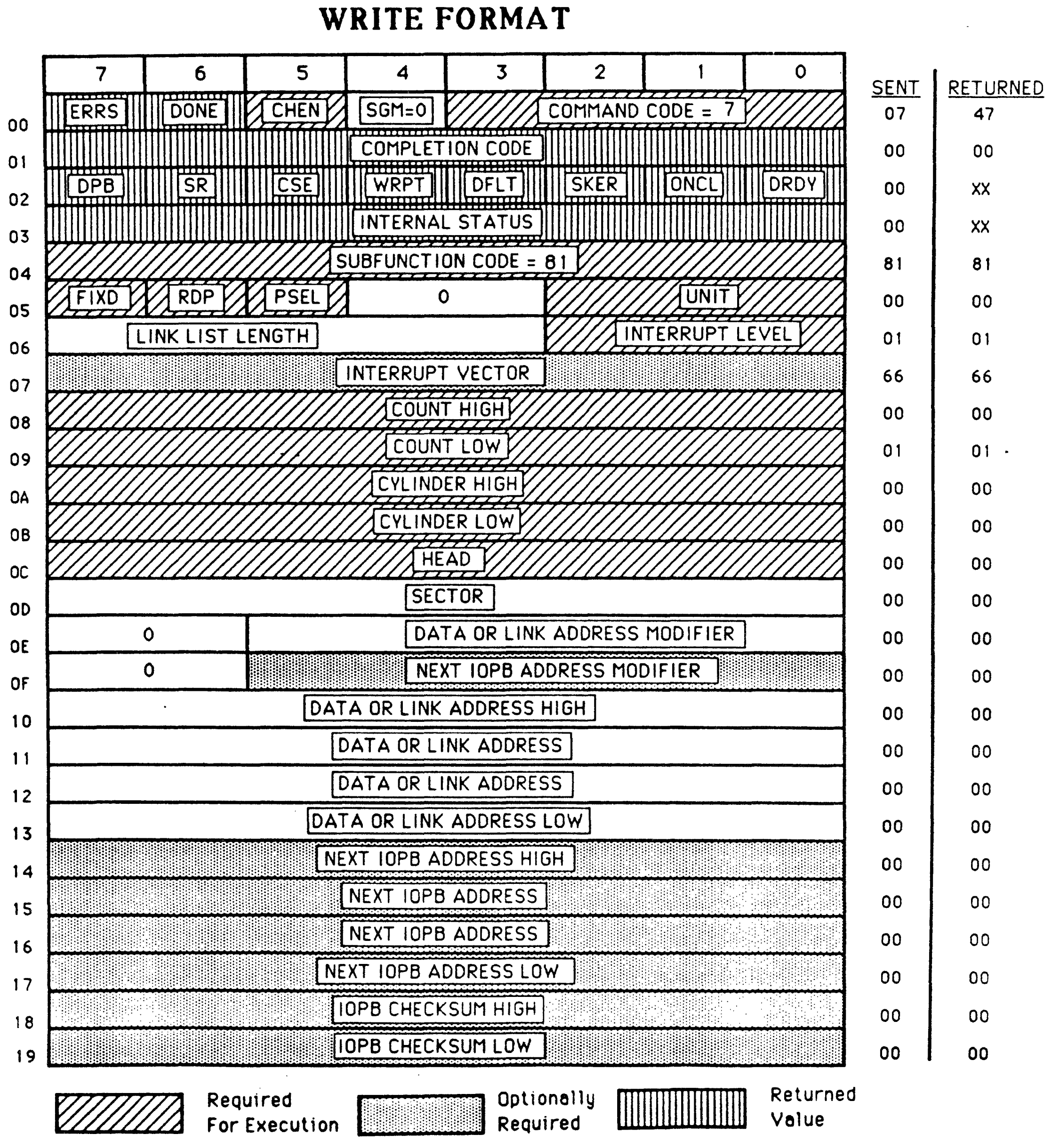
▥ Returned Value

Figure 7-5. Sample Write Drive Parameters IOPB

7.6 FORMAT A TRACK

Up to this point we have been initializing the 752. Initialization informs the 752 of the drive size, and parameters it requires before it can properly function. Now, let's format one track of the drive. The 752 can only execute Read and Write commands on a formatted track. (Typically, formatting is done only once in the lifetime of the media.)

7.6 FORMAT A TRACK (continued)



	7	6	5	4	3	2	1	0	SENT	RETURNED
00	ERRS	DONE	CHEN	SGM=0	COMMAND CODE = 7				07	47
01	COMPLETION CODE								00	00
02	DPB	SR	CSE	WRPT	DFLT	SKER	ONCL	DRDY	00	XX
03	INTERNAL STATUS								00	XX
04	SUBFUNCTION CODE = 81								81	81
05	FIXD	RDP	PSEL	0		UNIT			00	00
06	LINK LIST LENGTH					INTERRUPT LEVEL			01	01
07	INTERRUPT VECTOR								66	66
08	COUNT HIGH								00	00
09	COUNT LOW								01	01
0A	CYLINDER HIGH								00	00
0B	CYLINDER LOW								00	00
0C	HEAD								00	00
0D	SECTOR								00	00
0E	0		DATA OR LINK ADDRESS MODIFIER						00	00
0F	0		NEXT IOPB ADDRESS MODIFIER						00	00
10	DATA OR LINK ADDRESS HIGH								00	00
11	DATA OR LINK ADDRESS								00	00
12	DATA OR LINK ADDRESS								00	00
13	DATA OR LINK ADDRESS LOW								00	00
14	NEXT IOPB ADDRESS HIGH								00	00
15	NEXT IOPB ADDRESS								00	00
16	NEXT IOPB ADDRESS								00	00
17	NEXT IOPB ADDRESS LOW								00	00
18	IOPB CHECKSUM HIGH								00	00
19	IOPB CHECKSUM LOW								00	00

Figure 7-6. Sample Write Format IOPB

7.6.1 752 Operation

The Format command is the first command in this tutorial that transfers data from the controller to the disk. The 752 operation for data transfer commands differs greatly from initialization commands.

7.6.1 752 Operation (continued)

To format a track:

1. The 752 still clears AIOP, sets BUSY, and reads the IOPB from memory. The next step occurs after the IOPB is in the 752.

2. The 752 decodes the function, and determines if a seek is required. All Write, Read, Write Extended, and Read Extended functions require the drive to seek to the commanded cylinder. Format is a Write Extended function; it requires the drive to seek. The 752 issues a seek to the drive by sending it the commanded cylinder number.

3. The 752 waits for the drive to complete the seek; the drive indicates it's done by returning on-cylinder.

4. When the drive is on-cylinder, the 752 determines if the current physical sector count for that drive is valid. If the count is not valid, it repeats the sequence in Section 7.5.1 to determine the actual physical sector count. The 752 proceeds to Step 5 when the count is valid.

5. The 752 loads the data for the new sector header into the FIFO, waits for index, and writes the new header on Sector 0; it writes the data field with zeros, and writes the data field error correction code (ECC).

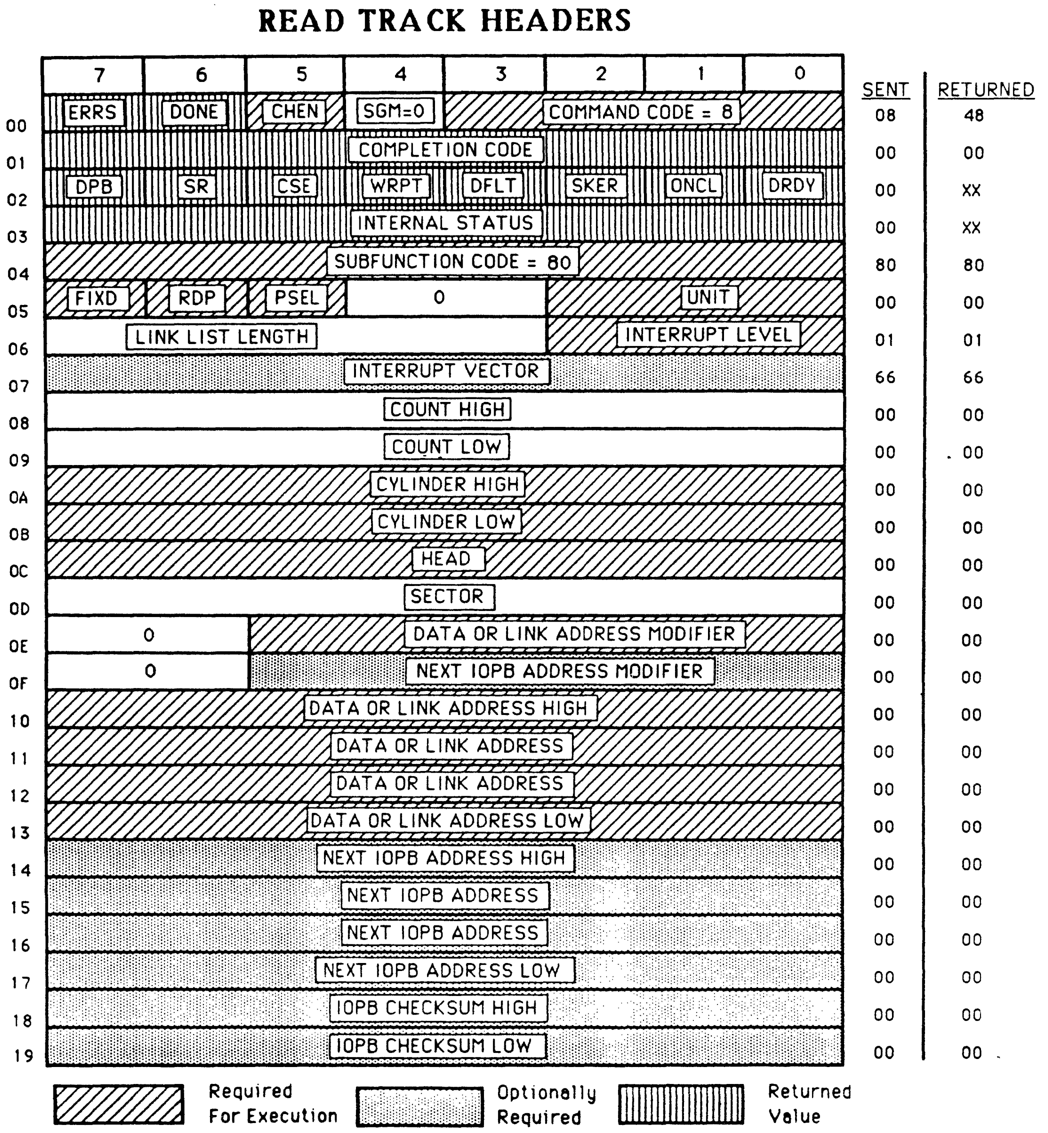
6. The 752 repeats Step 5 for each sector on the track, except it uses the sector pulse instead of index to start the operation.

7. The 752 updates the IOPB with the ending values, and completes the command.

7.7 READ TRACK HEADERS

Now that the track is formatted, read the headers back and verify they are correct. This command requires a data buffer; allocate space in host memory just as you did for the IOPB. The buffer length must be four bytes (per sector) times the number of sectors per track. (The Read Drive Parameters command gives you the number of sectors per track.) Make sure software passes the 752 the physical buffer address, not the virtual address. See Figure 7-7.

7.7 READ TRACK HEADERS (continued)



READ TRACK HEADERS

	7	6	5	4	3	2	1	0	SENT	RETURNED
00	ERRS	DONE	CHEN	SGM=0	COMMAND CODE = 8				08	48
01	COMPLETION CODE								00	00
02	DPB	SR	CSE	WRPT	DFLT	SKER	ONCL	DRDY	00	XX
03	INTERNAL STATUS								00	XX
04	SUBFUNCTION CODE = 80								80	80
05	FIXD	RDP	PSEL	0		UNIT			00	00
06	LINK LIST LENGTH					INTERRUPT LEVEL			01	01
07	INTERRUPT VECTOR								66	66
08	COUNT HIGH								00	00
09	COUNT LOW								00	00
0A	CYLINDER HIGH								00	00
0B	CYLINDER LOW								00	00
0C	HEAD								00	00
0D	SECTOR								00	00
0E	0		DATA OR LINK ADDRESS MODIFIER						00	00
0F	0		NEXT IOPB ADDRESS MODIFIER						00	00
10	DATA OR LINK ADDRESS HIGH								00	00
11	DATA OR LINK ADDRESS								00	00
12	DATA OR LINK ADDRESS								00	00
13	DATA OR LINK ADDRESS LOW								00	00
14	NEXT IOPB ADDRESS HIGH								00	00
15	NEXT IOPB ADDRESS								00	00
16	NEXT IOPB ADDRESS								00	00
17	NEXT IOPB ADDRESS LOW								00	00
18	IOPB CHECKSUM HIGH								00	00
19	IOPB CHECKSUM LOW								00	00

Figure 7-7. Sample Read Track Headers IOPB

7.7.1 752 Operation

The Read Track Headers is the first command in this tutorial that transfers data to or from host memory. Data transfers to or from memory modify the 752 operation as follows:

7.7.1 752 Operation (continued)

1. The 752 reads the IOPB, issues a seek, and decodes the command identically to the previous examples.

2. The 752 waits for index from the drive. It tests the physical sector count to determine if it is valid. If the count is not valid, the 752 determines the actual count (see Section 7.5.1).

3. After index arrives, the 752 synchronizes itself with the data in the header, and reads the data into its on-board FIFO.

4. The 752 repeats Step 3 for each sector on the track, except it waits for the sector pulse instead of index. The actual physical sector count determines the number of sectors the 752 transfers into its FIFO.

5. After the 752 transfers all sector headers into the FIFO, it begins the DMA. The controller transfers the data from the FIFO to host memory.

6. When the 752 completes the DMA transfer, it places the updated information into the IOPB, and completes the command.

7.7.2 Verifying the Data

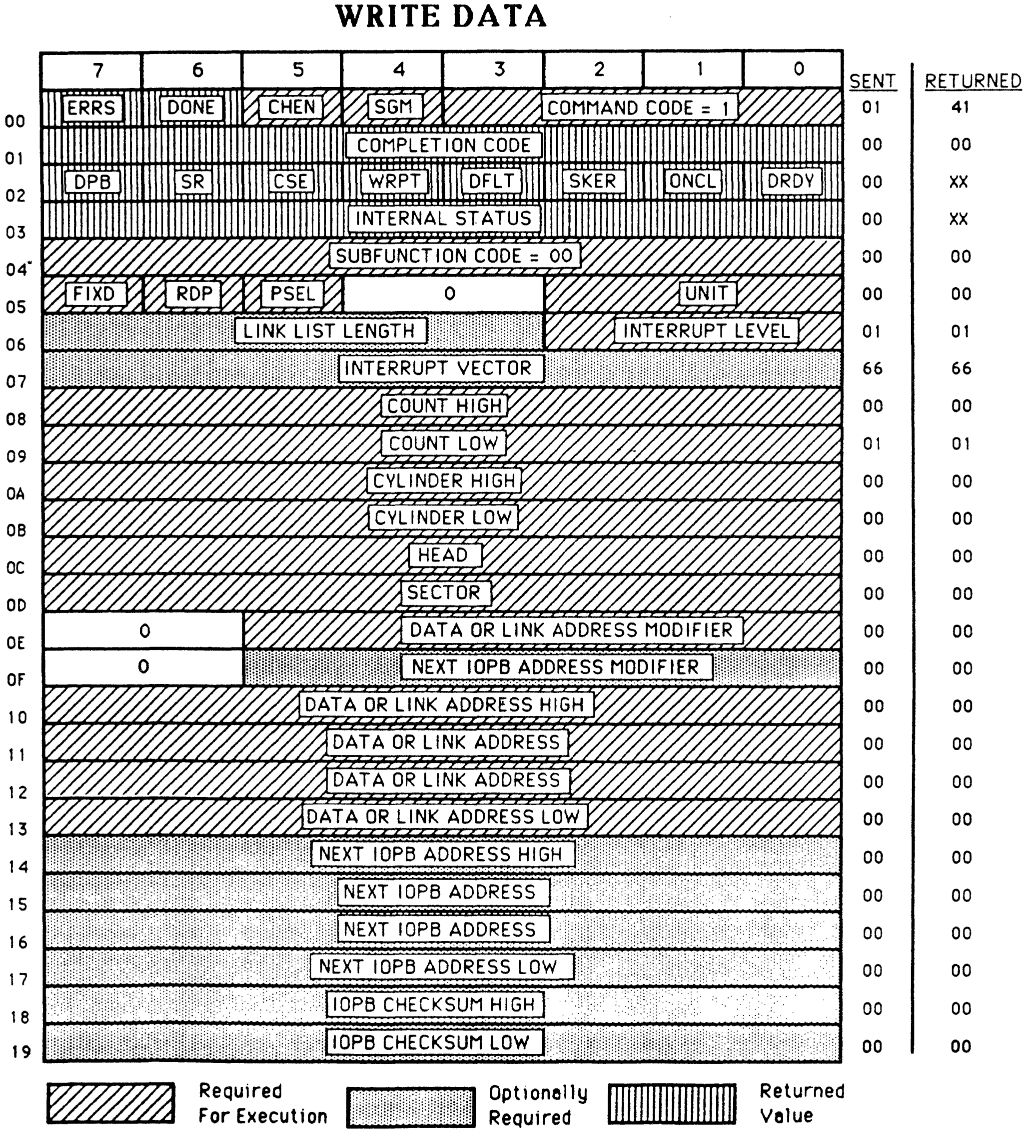
After the 752 completes the transfer, verify the data against what is expected. The data should be divided into groups having four bytes each. Each group describes a sector header. The first sector header should have four bytes of 00. The second header should have three bytes of 00 and one byte of 01. The last byte of the third header should equal 02, etc. (see Section 8.3 for more information on headers).

Header 1				Header 2				Header 3			
00	00	00	00	00	00	00	01	00	00	00	02

Figure 7-8. Sample Sector Headers

7.8 WRITE DATA

The format is valid after verifying the headers. This subsection describes a Write operation, and the following subsection describes reading back the data. Allocate space in host memory for the buffer, and set up a data pattern in this buffer; an incrementing count in the buffer will suffice. See Figure 7-9.



WRITE DATA

	7	6	5	4	3	2	1	0	SENT	RETURNED
00	ERRS	DONE	CHEN	SGM		COMMAND CODE = 1			01	41
01	COMPLETION CODE								00	00
02	DPB	SR	CSE	WRPT	DFLT	SKER	ONCL	DRDY	00	XX
03	INTERNAL STATUS								00	XX
04	SUBFUNCTION CODE = 00								00	00
05	FIXD	RDP	PSEL	0		UNIT			00	00
06	LINK LIST LENGTH					INTERRUPT LEVEL			01	01
07	INTERRUPT VECTOR								66	66
08	COUNT HIGH								00	00
09	COUNT LOW								01	01
0A	CYLINDER HIGH								00	00
0B	CYLINDER LOW								00	00
0C	HEAD								00	00
0D	SECTOR								00	00
0E	0		DATA OR LINK ADDRESS MODIFIER						00	00
0F	0		NEXT IOPB ADDRESS MODIFIER						00	00
10	DATA OR LINK ADDRESS HIGH								00	00
11	DATA OR LINK ADDRESS								00	00
12	DATA OR LINK ADDRESS								00	00
13	DATA OR LINK ADDRESS LOW								00	00
14	NEXT IOPB ADDRESS HIGH								00	00
15	NEXT IOPB ADDRESS								00	00
16	NEXT IOPB ADDRESS								00	00
17	NEXT IOPB ADDRESS LOW								00	00
18	IOPB CHECKSUM HIGH								00	00
19	IOPB CHECKSUM LOW								00	00

▨ Required For Execution

░ Optionally Required

▥ Returned Value

Figure 7-9. Sample Write Data IOPB

7.8.1 752 Operation

The 752 operation is similar to the previous examples; the differences are in DMAing data into the FIFO, and writing data to the disk.

The 752 starts the DMA from host memory to the FIFO after determining the drive is on-cylinder; it enables the disk sequencer when the FIFO contains one full sector of data.

The 752 compares and verifies the header: the disk sequencer tests all the headers as they pass under the head, until it finds the sector designated for transfer. At the proper point in the sector, the 752 writes a new Sync byte, and then the data it read from memory. The 752, using the data to be written, generates and appends an ECC on the end of the sector.

7.8.2 Command Completion

The command is complete as soon as the disk sequencer completes its operation. The 752 puts the ending values into the internal IOPB, and performs an appropriate update.

7.9 READ DATA

In Section 7.8 the 752 wrote the data to the drive on Sector 0, Head 0, and Track 0. This subsection describes reading back the data and verifying it. You must allocate a data buffer for the 752 to write the data in memory. After allocation, it is a good idea to fill the buffer with a known pattern that differs from the expected data. See Figure 7-10.

7.9.1 752 Operation

The 752 treats this command like the previous operations, except in the way it DMAs the data into the FIFO and writes the data to the disk.

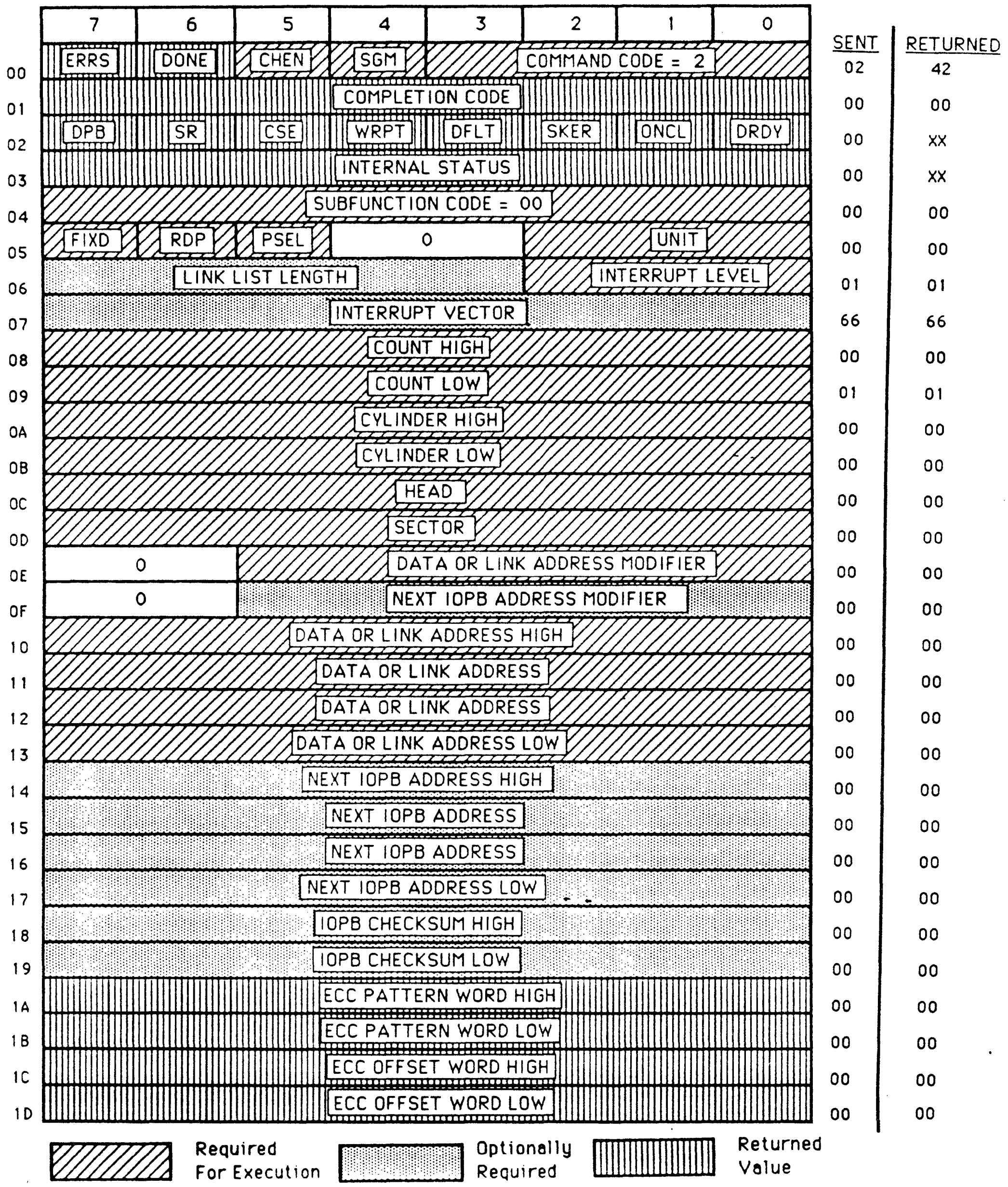
The 752 enables the disk sequencer as soon as the drive is on-cylinder. After the controller finds the correct header, it transfers the data from the disk to the FIFO. As soon as the first sector of data is available from the buffer, the DMA controller DMAs the data from the FIFO to host memory. The transfer is done when the DMA controller completes the DMA.

7.9.2 Command Completion

The 752 completes the command when the DMA to memory is complete. The next subsection describes how to verify the data.

7.9.2 Command Completion (continued)

READ DATA



	7	6	5	4	3	2	1	0	SENT	RETURNED
00	ERRS	DONE	CHEN	SGM	COMMAND CODE = 2				02	42
01	COMPLETION CODE								00	00
02	DPB	SR	CSE	WRPT	DFLT	SKER	ONCL	DRDY	00	XX
03	INTERNAL STATUS								00	XX
04	SUBFUNCTION CODE = 00								00	00
05	FIXD	RDP	PSEL	0		UNIT			00	00
06	LINK LIST LENGTH					INTERRUPT LEVEL			01	01
07	INTERRUPT VECTOR								66	66
08	COUNT HIGH								00	00
09	COUNT LOW								01	01
0A	CYLINDER HIGH								00	00
0B	CYLINDER LOW								00	00
0C	HEAD								00	00
0D	SECTOR								00	00
0E	0		DATA OR LINK ADDRESS MODIFIER						00	00
0F	0		NEXT IOPB ADDRESS MODIFIER						00	00
10	DATA OR LINK ADDRESS HIGH								00	00
11	DATA OR LINK ADDRESS								00	00
12	DATA OR LINK ADDRESS								00	00
13	DATA OR LINK ADDRESS LOW								00	00
14	NEXT IOPB ADDRESS HIGH								00	00
15	NEXT IOPB ADDRESS								00	00
16	NEXT IOPB ADDRESS								00	00
17	NEXT IOPB ADDRESS LOW								00	00
18	IOPB CHECKSUM HIGH								00	00
19	IOPB CHECKSUM LOW								00	00
1A	ECC PATTERN WORD HIGH								00	00
1B	ECC PATTERN WORD LOW								00	00
1C	ECC OFFSET WORD HIGH								00	00
1D	ECC OFFSET WORD LOW								00	00

Figure 7-10. Sample Read Data IOPB

7.9.3 Verify Data

First, make sure the buffer was modified. If it was not modified, either an error occurred, or software specified the wrong buffer address. Next, compare the data written with the data read; they should match.

7.10 MULTIPLE SECTOR TRANSFERS

You can repeat the steps in Sections 7.8 and 7.9 using a larger sector count. The 752 crosses head and cylinder boundaries, as required, to complete the required number of sectors. Be sure to allocate enough buffer space for the increased sector count.

7.11 SUMMARY

This section was an exercise in testing the 752's functionality in your system. The steps are basically the same when the software driver controls the 752. (Operating systems always allocate the buffers.)

SECTION 8: SPECIAL FUNCTIONS

8.0 GENERAL

This section describes how to implement the various 752 special functions. Each subsection descibes how minor functions implement a given major function.

8.1 READ DEFECT MAP

The 752 reads the data recorded on the media by the manufacturer that describes the location and length of factory-detected media defects. The defect map's format must conform to the following specifications: M2331/M2333 Disk Drive Engineering Specification; Fujitsu LTD. Doc. No. B03P-4760-0101A; and CDC Product Specification No. 64400400.

8.1.1 The Defect Map

The header format is divided into two parts. The first part of the format is a fixed sector format; the second part is a variable sector format. The fixed sector format is normally included in the first 56 bytes following the index mark. The 752 does not support the variable sector format.

The following rules apply to defect recording:

1. The position of a defect is listed in bytes (hex) after the index mark, plus or minus one byte.
2. The length of a defect is in bits (hex), plus or minus one bit.
3. The unused defect locations are all zeros.
4. Every track is recorded with this defect format whether defects exist or not.
5. A track that has more than one defect may be flagged as defective. Log the first four media defects on the track.
6. Figure 8-1 shows the format when there are no defects in the first 105 bytes after the index mark.

8.1.1 The Defect Map (continued)

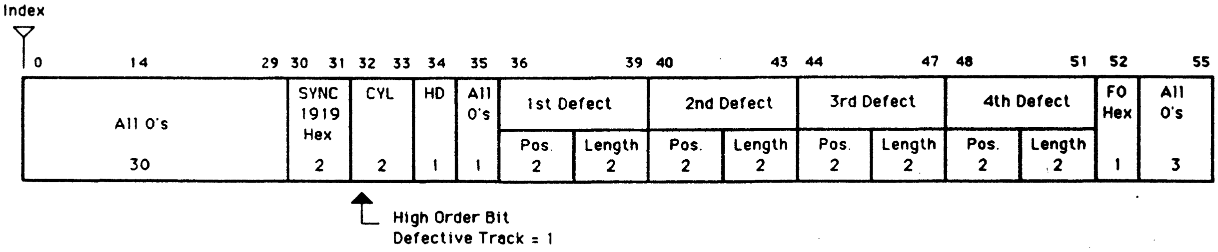


Figure 8-1. Defect Map Format

7. Figure 8-2 shows the format when the beginning of a defect is located between Bytes 10 and 55; 60 bytes of zeros are added to Gap 1. In the extended defect map format, the defect map is always relocated to a defect-free area.

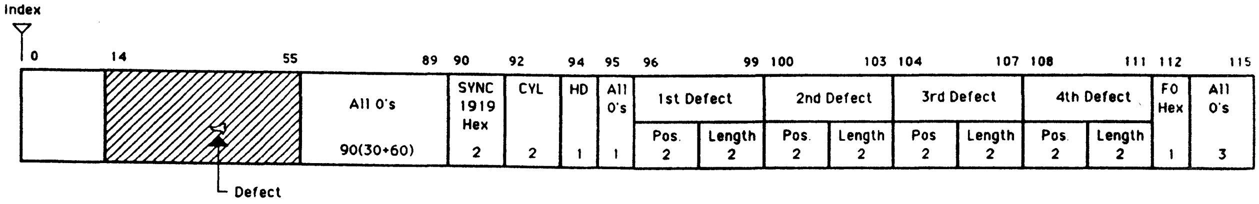


Figure 8-2. Extended Defect Map Format

8.1.2 Read the Defect Map

Set up a 24-byte buffer in memory. Issue an Extended Read with a subfunction of Read Defect Map. Since the defect maps do not use a checksum, verify the data.

8.1.3 Verify the Data

The first byte in the buffer should be a 19H. This is the second of two Sync bytes. The head and cylinder addresses should agree. The last byte should be an F0H.

8.1.4 Determining the Location of a Defect

The position of a defect is provided in bytes from the index mark. You must convert this value to a sector number before using it for defect mapping. The drive switch settings determine the actual number of bytes per sector. Divide this value into the defect position. This number, truncated, points to the physical sector containing the defect. Adjusting this physical sector number by any interleaving or skewing scheme determines the logical sector number for remapping.

8.2 FORMATTING

This subsection describes formatting, including how to set the number of spares for use in media defect handling and setting the sector size.

8.2.1 Allocating Spare Sectors

You must allocate spare sectors at format time. The Write Drive Parameters command allows setting the maximum size parameters for the drive. Any sectors in excess of the drive size parameters are marked as spares. For example, a drive with 46 physical sectors is specified as having only 45 in the Write Drive Parameters command. The 752 formats 45 normal sectors and 1 spare sector.

A separate variable (max sector/last head) specifies the number of sectors on max head. This allows extra spares on max head for use with cylinder sparing. Given the above example, max sector/last head is set to 40. The 752 formats the last head of the same drive with 40 normal sectors, and 6 spare sectors.

8.2.2 Specify Sector Gap Size

First a note of caution, **don't do this.** Modifying the gap sizes may reduce your disk subsystem's performance. The drive interface has many specifications and parameters to which you must adhere. Slight miscalculations may not show up in the engineering lab, but may cause unreliability in the field. The failure modes may be undetectable because field lengths are only marginally long enough. A word to the wise: if you decide to use this feature, please be very careful.

Xylogics' values work with all standard SMD drives (see Sections 4.4.6 through 4.4.8). Modified values may work with some drives, and cause unreliable results with others. See Figure 8-3.

8.2.2 Specify Sector Gap Size (continued)

The following subsections outline the parameters that affect each of the gap sizes. Many of the parameters that affect the gap sizes are specifications for the drive in use. Drives from different manufacturers, and even drives in one manufacturer's line, may have very different specifications.

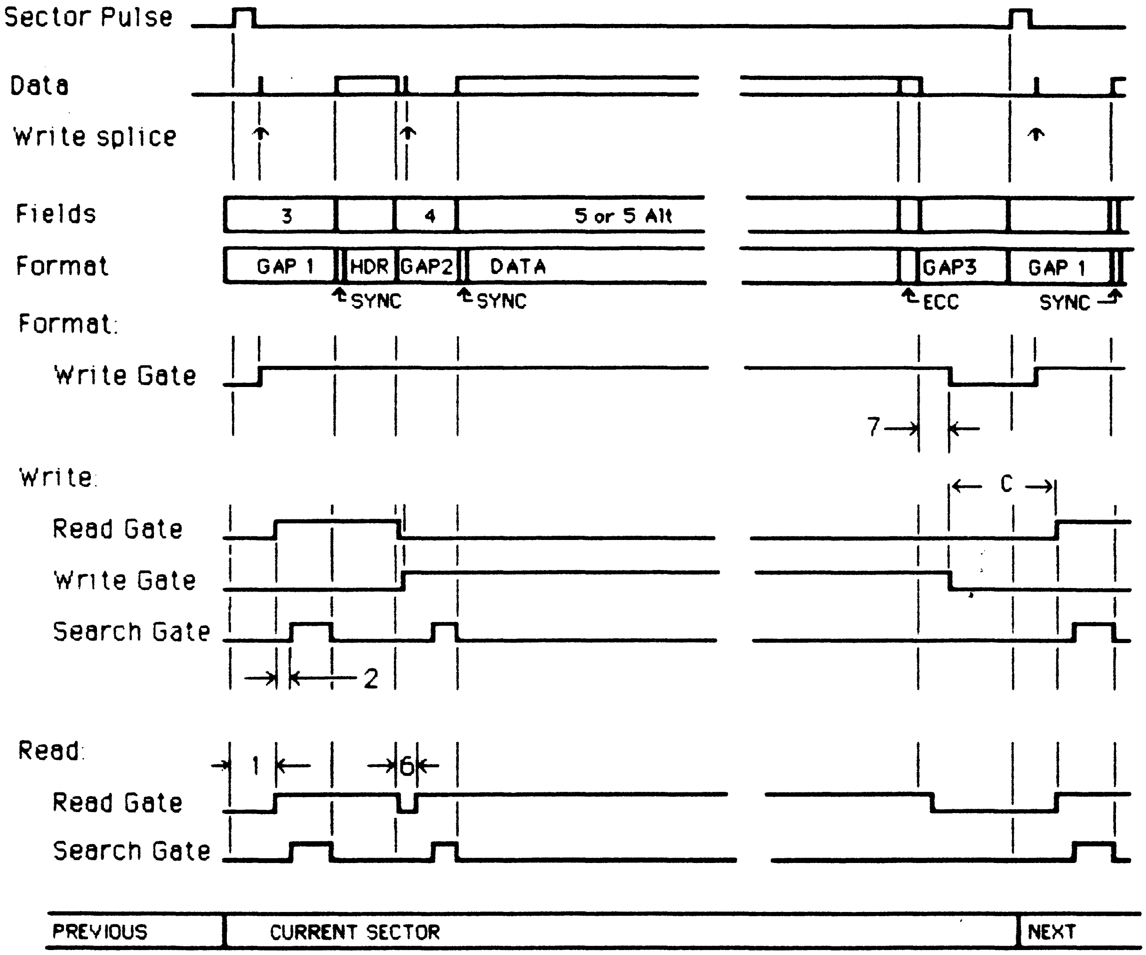


Figure 8-3. Sector Gap Sizes

8.2.2.1 Field 1 - Read Gate Delay - Gap 1

Field 1 specifies the time in bytes from one byte past the leading edge of sector or index to when Read Gate is asserted. The applicable drive specifications include head settling time, allowing enough time to lock the Phase Lock Oscillator, and the minimum Write Gate to Read Gate timing. Field 1 also provides for skipping over the write splice area.

The head settling time is the time required for the heads to settle after the drive completes a seek. We do not know how long before the sector or index pulse the seek completed, therefore this field must be large enough to encompass the head settling time.

When subtracted from Field 3, this field indicates the amount of time left for the Phase Lock Oscillator in the drive to lock onto the data. Drive requirements vary from 3 to 16 bytes.

When Write Gate is deasserted, a minimum time must be allowed for the read heads and amplifiers to stabilize. In a multisector transfer, Write Gate is deasserted after the last sector, and Read Gate is asserted for reading the next header. Figure 8-3 indicates this time as "C". Field 1 and the remaining bytes in the sector after Field 7 comprise this critical time. Drive requirements are usually in the 10 to 12 microsecond range.

Write Splice: as Write Gate is asserted (or deasserted), the changing write current causes a magnetic field to build (or collapse) which "writes" garbage onto the disk. This is called the write splice, and it occurs whenever Write Gate is asserted or deasserted.

8.2.2.2 Field 2 - Sync Search Delay

Field 2 is the delay from asserting Read Gate to when data is compared for the Sync byte. Field 2 masks any read data from being detected as a sync until the data is stable.

8.2.2.3 Field 3 - Gap 1

Field 3 is equivalent to Gap 1. Fields 3 and 1 together define the amount of time allowed for the Phase Lock Oscillator (PLO) in the drive to lock up. See Section 8.2.2.1.

8.2.2.4 Field 4 - Gap 2

Field 4 is equivalent to Gap 2. It is the time (in bytes) between the end ot the Header ECC and the Data Sync byte. This field includes the time required to allow the PLO in the drive to sync to the data and to skip the write splice. On a Write command, Write Gate is asserted four bit cells after Read Gate is deasserted. This field is actually four bits longer than specified. These four bits are used to test the header.

8.2.2.5 Field 6 - Read Gate Delay

Field 6 asserts Read Gate after the write splice during Gap 2. The time left over, Field 4 minus Field 6, is the time allowed for the PLO in the drive to lock up.

8.2.2.6 Field 7 - Write Continuation

The write continuation field is necessary so that when Write Gate is deasserted, the collapsing magnetic field does not splash over the ECC that was just written. The end of Field 7 is the beginning of the minimum Write Gate to Read Gate period described in Section 8.2.2.1.

8.2.2.7 Head Switch Time

The 752 requires 6 bytes of time after Field 7 to switch heads. If the sector size is too short to allow this 6-byte field, the 752 will miss revolutions on every head switch. This should not be a problem; typically, the minimum Write Gate to Read Gate time allows for this field.

8.2.3 Format Interleave

The 752 can optionally format with an interleave pattern from 2:1 to 16:1. Specify the interleave factor when writing the format parameters; it is invisible to the operating system.

Interleaving can increase the throughput of a disk subsystem on a fully loaded system by effectively cutting the disk speed in half. On a contiguously formatted pack (1:1 interleave), the sectors increase by one each time. As the disk spins, the sectors arrive under the head in the following order for a 32-sector disk:

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 ...31

8.2.3 Format Interleave (continued)

If you interleaved the same disk with a 2:1 interleave factor, it would look like this:

0 16 1 17 2 18 3 19 4 20 5 21 6 22 7 23 8 24 9 25 10 ...31

The 2:1 interleave allows the 752 two sector times to transfer a sector to memory. For example, if you are transferring sectors 0 and 1 to memory, the following occurs in each case.

In 1:1 interleaving, when the first sector finishes reading from the disk, the next sector is almost under the head and ready for reading. At this time there must be enough room in the buffer or the 752 misses a revolution.

In 2:1 interleaving, when the first sector finishes reading from the disk, the next sector is still a full sector time away, thereby giving the 752 twice the time to empty the buffer to memory. The scheme above shows the extra sector time as sector 16.

Interleaving schemes from 2:1 to 15:1 are software programmable. Since the 752 determines the drive's sector location by comparing headers, you can use the Write Track Headers command to customize the interleaving scheme to your application. For example, if your system transfers data in 2K-blocks, then the most effective interleaving scheme may be:

0 1 2 3 16 17 18 19 4 5 6 7 20 21 22 23 8 9 10 11 ...

8.3 MEDIA DEFECT HANDLING

There are three methods for handling media defects: 1) slipping a sector; 2) remapping a sector to a new sector on the last head of that cylinder; and 3) remapping the entire track to a different track on the disk.

8.3.1 Slipping a Sector

Slipping a sector requires using the Read and Write Track Headers commands to mark the bad sector and slip the rest of the sectors into the next position on the disk. Figure 8-4 shows an 8-sector track before and after slipping Sector 3.

8.3.1 Slipping a Sector (continued)

0	1	2	3	4	5	6	7	Spare

0	1	2	Bad	3	4	5	6	7

Figure 8-4. Sector Slip

8.3.1.1 Sector Slip Procedure

1. Determine which sector is bad by writing and reading the track with several patterns, and/or by using the manufacturer's defect map information.
2. Read the track headers into a buffer in host memory.
3. Compare each header with the bad sector's header.
4. After locating the bad sector, mark it by writing EEH into each of the four header bytes (see Figure 8-6).
5. Test the last sector to determine if it is a spare. If it is a spare, continue; if not, you must find another sparing method.
6. Move each sector header into the next location, "slipping" the sectors down the track (see Figure 8-4).
7. Write the track headers back to the disk.

The following figures depict 752 headers:

Sync	Cylinder Low	Cylinder High	Head	Sector

Figure 8-5. Normal Header

Sync	EE	EE	EE	EE

Figure 8-6. Header Marked Bad

8.3.1.1 Sector Slip Procedure (continued)

Sync	DD	DD	DD	DD

Figure 8-7. Header Marked Spare

00	00	00	00	00

Figure 8-8. Runt Header *

* This header is invisible in normal 752 operation.
It appears here for informational purposes only.

Sync	New Cyl Low	CC	New Cyl High	Head

Figure 8-9. Track Remap Header

8.3.1.2 Advantages of Sector Slipping

A full track of information is still transferred in one revolution of the disk. Other methods of sector slipping require two or more revolutions to transfer one track of information.

8.3.1.3 Disadvantages of Sector Slipping

Having one or more spares on each track uses disk space inefficiently.

8.3.2 Cylinder Sparing

Cylinder sparing is similar to sector slipping, except the spares are on the maximum head of the cylinder.

8.3.2.1 Cylinder Sparing Procedure

1. Determine the defective sector.
2. Read the track headers and mark the defective sector bad (see Figure 8-6).
3. Write the track headers back to the disk.
4. Read the track headers on the maximum track of that cylinder.
5. Find a spare sector; it contains four bytes of 0DDH. (see Figure 8-7.)
6. Put the bad sector's header into this sector. The header contains the head and sector values for the sector being remapped on the original track.
7. Write the track headers back to the drive.

8.3.2.2 Advantages of Cylinder Sparing

Cylinder sparing uses less disk space for remapping bad sectors. You may decide to allow only 10 spares for a drive with 20 heads. Sector slipping is less efficient as it requires a minimum of 20 sectors per cylinder for this drive (one per head).

8.3.2.3 Disadvantages of Cylinder Sparing

Cylinder sparing is slower than sector slipping. The 752 looks for the requested sector for one revolution plus one sector on the original track; then it switches to max head and looks for another revolution plus one sector. This method takes up to three revolutions to transfer one track of information (assuming only one bad sector).

8.3.3 Track Remapping

The 752 remaps an entire track to another location on the same disk drive by writing the defective track's headers with a code and new disk address.

8.3.3.1 Track Remapping Procedure

1. Read and save the defective track's headers.

2. Allocate space for a write track headers buffer. Each header has 0CCH in the second byte. The first, third, and fourth bytes contain the new Head, Cylinder High, and Cylinder Low. Write this information to the defective track with a Write Track Headers command. See Figure 8-9.

3. Write the track headers that were read in Step 1 to the destination track with a Write Track Headers command.

8.3.3.2 Advantages of Track Remapping

Track remapping is useful in sparing tracks with very large or multiple defects.

8.3.3.3 Disadvantages of Track Remapping

Track remapping is relatively slow as the 752 must seek to the first track and then determine if it has been remapped. Then the 752 seeks to the spare track area (usually at the end of the disk). This sequence can add up to four revolutions to the 752 overhead.

8.3.4 Recommended Remapping Procedure

Xylogics recommends using all three methods of defect mapping. Allowing one spare sector per track takes care of 95% of the media defects. An additional 0.2% of the sectors on the cylinder to be spared on the last head provide up to 99% remapping. Allowing three or four tracks for remapping should provide a defect-free media. Allocating this amount of disk space for defect handling totals 2% of the media. Having two spares per track on the same drive (a Fujitsu Eagle with 512-byte sectors) uses 4% of the media.

8.4 CHAINING AND MULTIPLE I/O REQUESTS

The 752 has two ways of speeding up multiple IOPB execution. One method allows the driver to chain IOPBs together, and then give the 752 a command-chain. The second method allows the driver to add IOPBs to the 752's queue by the same procedure as starting the first IOPB.

8.4.1 Chaining

Each IOPB has a Chain Enable (CHEN) bit and a Next IOPB pointer. IOPBs can be chained together by setting CHEN and having the Next IOPB pointer point to the next IOPB to be executed. Each IOPB in the chain points to the next, and, in order to stop the chain, CHEN is not set in the last IOPB.

NOTE

The Next IOPB Address is the physical address, not the virtual address.

8.4.2 Multiple I/O Requests

The following procedure allows you to add IOPBs to the 752 queue:

1. AIOP must be clear. If it is not clear, wait; it normally clears within 100 microseconds (see Sections 3.3.2 and 4.2.1).
2. Write the five IOPB address registers to point to the beginning of the IOPB (chain).
3. Write AIO.

8.4.3 752 Operation

The 752 treats IOPBs the same, regardless of how they were added to the queue. Overlap seeks function only when they are enabled and the 752 is working with a queue or chain of IOPBs.

8.5 ERROR RECOVERY

The 752 may automatically retry operations that have errored. Two options are available. One option involves retrying drive fault- and seek-type errors. The other option involves the retry algorithms for ECC recoveries. The Read and Write Controller Parameters commands enable or disable these options.

8.5.1 Automatic Operation Retry

The 752 automatically retries an operation if the reason for the initial failure is a seek error or drive fault. Setting ASR with a Write Controller Parameters command enables this option.

8.5.2 ECC Error Recovery

ECC algorithms have a much better chance of recovery if the 752 retries the operation before using the ECC correction. The 752 retries the Read operation once before applying the ECC correction if RBC is set. Set RBC with a Write Controller Parameters command.

There are three options for applying ECC correction. Using Mode 0, the 752 provides the correcting pattern and offset for the driver to go and correct the actual error in memory. Mode 1 flags the fact that an error occurred, but does not stop the transfer to calculate any correction information. Mode 2 calculates the correction information and applies it to the data in host memory.

8.5.3 Using the Error Recovery Options

Changing the appropriate controller parameter enables or disables the error recovery options. Once set, the 752 takes care of applying the retries as requested. The 752 provides a completion status to indicate a recovery operation took place. The driver applies the ECC correction if ECC Mode 0 is used. If a retry fails, the Completion Code reflects the fatal error.

8.6 MAINTENANCE MODE

Firmware supports a non-IOPB driven Maintenance mode. It allows you to perform basic testing within the 752 by setting Control bits in the CSR and entering the desired test number and data through the address registers. This firmware also provides a window through which internal registers may be examined or modified.

8.6.1 Register Use in Maintenance Mode

The Function Code in the Test Number Register determines whether or not the 752 uses the Input Data Byte and Output Data Byte Registers (see Table 8-1). Familiarize yourself with the Control and Status Register before reading this section (see Section 3.3).

Register	Description
1	Test Number or Function Code
3	Input Address Low
5	Input Address High
7	Input Data Byte (If Required)
9	Output Data Byte (If Required)
B	Control and Status Register
D	Fatal Error Register

Table 8-1. Register Use in Maintenance Mode

8.6.2 Maintenance Mode Protocol

8.6.2.1 Executing a Maintenance Command or Entering the Maintenance Mode

First, set the Maintenance Mode (MM) and AIO bits. This forces entry into the maintenance kernel. The kernel initializes the CSR and Poll mask and sets the Remove IOPB (RIO) bit; then clear RIO.

The kernel expects the Input Address Low Register to contain a maintenance test number or function code for execution. Data may be expected or may be returned (see register layout).

BUSY and AIO are configured for polling. Setting BUSY and AIO selects the register image test; clearing BUSY returns control to the maintenance kernel.

AIO causes the maintenance firmware to read and decode the command string from the Input Address Registers. After successfully decoding the command string, the firmware echoes it (command, address, and data) to the Output Address Registers and clears AIO. This acknowledges receipt of and attempts to execute the requested command. After completing the requested command, the 752 updates the Output Address Registers with test-pertinent data and sets the RIO bit. The AIO/RIO protocol is identical to Normal mode. (RIO indicates the end of firmware involvement and valid contents in the Output Address Registers.)

Since each test and its expected results are different in nature, the Output Address Registers hold the test result information (address, data, etc.). In any case, the firmware sets RIO upon command completion; it sets the Fatal Error bit if a failure occurs or if host software issues an illegal command.

8.6.2.2 Exiting the Maintenance Mode

To exit the Maintenance mode, clear MM and RIO, and set AIO. This returns control to the Normal mode kernel. The 752 acknowledges by setting RIO.

8.6.2.3 Diagnostic Considerations

The Input/Output Address Register Verify is the first test the diagnostic should execute.

Firmware flags the power-up self test failures by setting the Fatal Error bit while leaving the Maintenance mode bit set. Firmware saves the self test error numbers internally until it verifies the Input and Output Registers.

8.6.2.4 Register Tests

You must request entry into the Maintenance mode to invoke the Register test. After the firmware acknowledges the request, you should set BUSY. BUSY remains set during this test.

NOTE

> You must enter the Maintenance mode as a separate step because the Normal mode firmware does not allow setting BUSY (defined as RMM when Maintenance mode is enabled).

Writing the Input Address Registers, followed by AIO, signals the firmware to copy the data to the Output Address Registers. Firmware sets RIO when it completes the copy. Host software should then clear RIO.

Clearing the BUSY bit exits this test and returns the 752 to Maintenance mode.

8.6.2.5 Test Variables

Some of the internal tests require the address and data to perform their particular function. On-board memory has space allocated for this data. These locations are loaded with default values for initial use. However, you may alter these variables through the Manual mode. (As the internal tests are defined, the protocol and results expected will be made available.)

8.7 MULTIPROCESSOR SUPPORT

The 752 has several options that make multiprocessor environments easier to support: the programmable interrupt vector, interrupt level, register address modifiers, and busy semaphore.

8.7.1 Interrupts

Each IOPB specifies the interrupt level and vector for that command. In a multiprocessor environment, each processor can have its own assigned interrupt level and vector.

8.7.2 Register Busy Semaphore

RBS allows multiple processors to share the registers without colliding. Hardware supports the RBS bit. The register access protocol involves reading the CSR. If RBS is clear, the host has control of the register, and retains control until it clears RBS in the Control Register. If the first read to the Status Register indicates that RBS is set, then another host has control of the register and this host must wait until RBS clears.

The 752 sets RBS immediately after a host reads the CSR. If a host attempts a read, and RBS is clear, the 752 sets RBS; any successive reads by other hosts will "see" that RBS is set. When the host using the registers is done, it must clear RBS. Clearing RBS and setting AIO can occur in the same register write. Clearing RBS without having control of the registers violates the register protocol.

8.7.3 Address Modifiers

The address modifiers can be used to assign separate address space for each of the processors.

8.8 SOFTWARE CONTROL

The 752 has many parameters that can be modified by software control. The parameters can be set in bulk with three write parameters commands: Write Format Parameters, Write Drive Parameters, and Write Controller Parameters.

8.8.1 Modifying a Single Parameter

The best method for modifying a single parameter (assuming the 752 was previously set up) is to first execute a read parameters command for the associated parameter block, modify the single parameter, and then write the parameter block back to the 752.

8.8.2 Modifying a Group of Parameters

Use the same method as in Section 8.8.1, or set all the parameters in the specific IOPB and execute the appropriate write parameters command. For example, Fields 1 through 7 and the interleave factor must be set to the appropriate values before issuing the Write Format Parameters command. The 752 sets all parameters to the new values contained in the IOPB.

8.8.3 Parameter Reference Point

After the 752 is working as intended, read the parameters and save the information for future use.

8.9 SCATTER/GATHER

The Scatter/Gather feature is used in conjunction with standard Read and Write commands. In a Scatter Read, the 752 transfers the data to up to 32 blocks of memory. Gather Writes gathers data from up to 32 blocks of memory and writes it to the disk. The size of each memory block must be an even byte count and less than 64K-bytes long. The blocks may be scattered throughout memory.

8.9.1 Scatter/Gather Link List

You can determine the length of the linked list by multiplying the number of elements in the list by 8 (each element is 8-bytes long). All data addresses must be on word boundaries and the byte count must be even. For Read and Write operations, enter the number of elements in the linked list into Byte 6, bits 3 through 7. A zero in this field indicates the linked list has 32 elements.

Link Number	Byte	Description
1	00-01	Byte Count (Multiples of 2)
	02	Reserved
	03	Data Address Modifier
	04-07	Data Address (Word Boundaries Only)
2	08-09	Byte Count
	:	
	:	
n	xx	

Table 8-2. Scatter/Gather Link List

8.9.1 Scatter/Gather Link List (continued)

Link Field Value	Decimal Equivalent
0	32
1	1
2	2
:	:
9	9
A	10
B	11
:	:
1E	30
1F	31

Table 8-3. Link List Field Values

8.9.2 Setting Up a Scatter/Gather Transfer

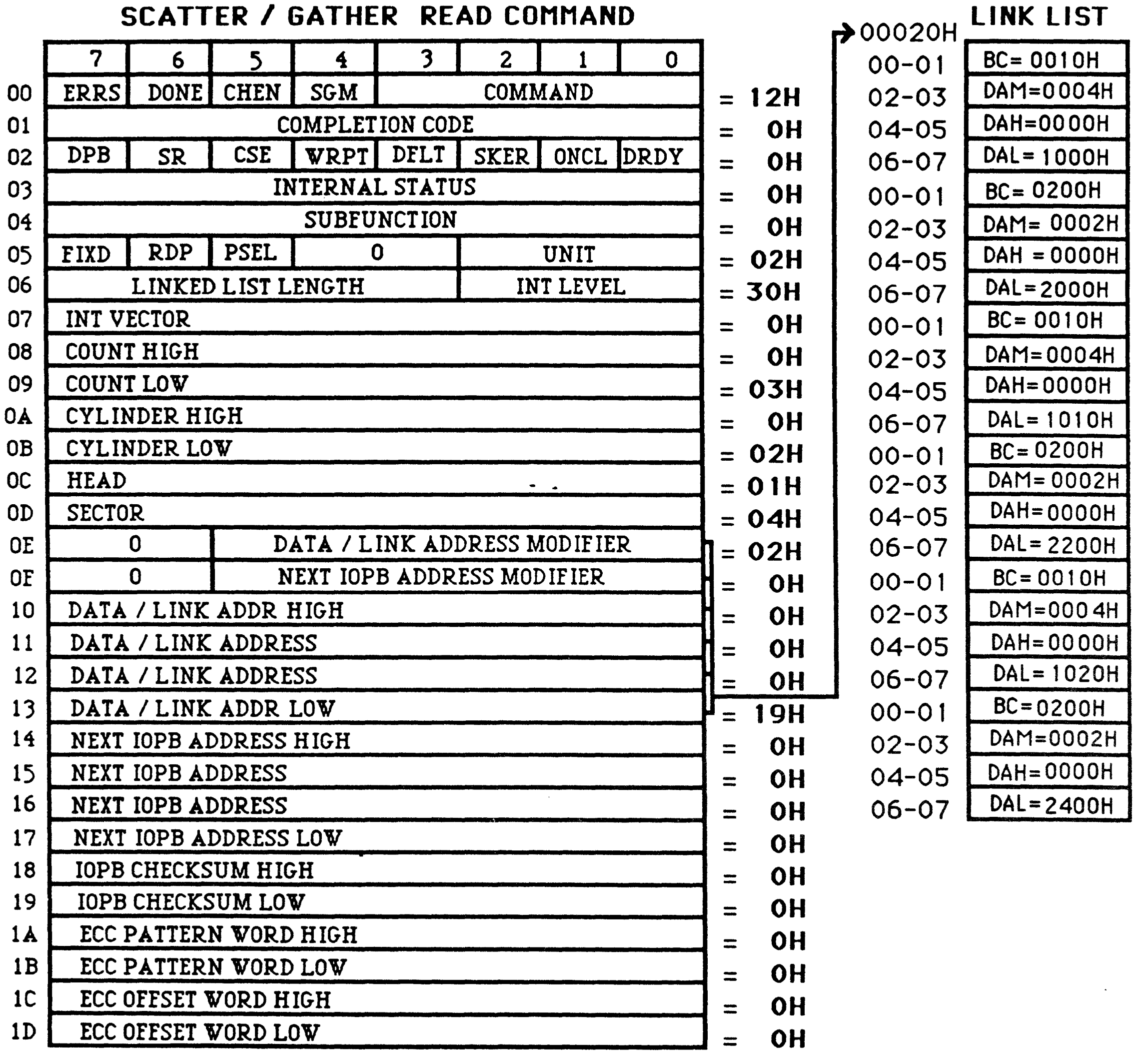
The Data Address and Modifier bytes in the IOPB should now point to the start of the linked list. The linked list length field should give the total number of elements on the list.

Elements of memory descriptors comprise the linked list. Each element describes the starting address and the length in bytes of the memory block. The sum of the byte count of all the elements in the linked list must equal the sector count times the sector size in bytes.

The IOPB and Linked List in Figure 8-10 illustrate a Read transfer to 6 blocks of memory. The sector size in this case is 512-bytes per sector; we are transferring 3 sectors of information. The 752 transfers the first 16 bytes of data from each sector to a separate data buffer. It scatters the bulk of the data, 512-bytes per sector, into memory as 3 blocks having 512 bytes each.

Set SGM and execute the IOPB in Figure 8-10.

8.9.2 Setting Up a Scatter/Gather Transfer (continued)



	7	6	5	4	3	2	1	0	
00	ERRS	DONE	CHEN	SGM	COMMAND				= 12H
01	COMPLETION CODE								= 0H
02	DPB	SR	CSE	WRPT	DFLT	SKER	ONCL	DRDY	= 0H
03	INTERNAL STATUS								= 0H
04	SUBFUNCTION								= 0H
05	FIXD	RDP	PSEL	0		UNIT			= 02H
06	LINKED LIST LENGTH					INT LEVEL			= 30H
07	INT VECTOR								= 0H
08	COUNT HIGH								= 0H
09	COUNT LOW								= 03H
0A	CYLINDER HIGH								= 0H
0B	CYLINDER LOW								= 02H
0C	HEAD								= 01H
0D	SECTOR								= 04H
0E	0		DATA / LINK ADDRESS MODIFIER						= 02H
0F	0		NEXT IOPB ADDRESS MODIFIER						= 0H
10	DATA / LINK ADDR HIGH								= 0H
11	DATA / LINK ADDRESS								= 0H
12	DATA / LINK ADDRESS								= 0H
13	DATA / LINK ADDR LOW								= 19H
14	NEXT IOPB ADDRESS HIGH								= 0H
15	NEXT IOPB ADDRESS								= 0H
16	NEXT IOPB ADDRESS								= 0H
17	NEXT IOPB ADDRESS LOW								= 0H
18	IOPB CHECKSUM HIGH								= 0H
19	IOPB CHECKSUM LOW								= 0H
1A	ECC PATTERN WORD HIGH								= 0H
1B	ECC PATTERN WORD LOW								= 0H
1C	ECC OFFSET WORD HIGH								= 0H
1D	ECC OFFSET WORD LOW								= 0H

00020H	LINK LIST
00-01	BC= 0010H
02-03	DAM=0004H
04-05	DAH=0000H
06-07	DAL= 1000H
00-01	BC= 0200H
02-03	DAM= 0002H
04-05	DAH = 0000H
06-07	DAL=2000H
00-01	BC= 0010H
02-03	DAM=0004H
04-05	DAH=0000H
06-07	DAL= 1010H
00-01	BC=0200H
02-03	DAM= 0002H
04-05	DAH=0000H
06-07	DAL= 2200H
00-01	BC= 0010H
02-03	DAM=0004H
04-05	DAH=0000H
06-07	DAL= 1020H
00-01	BC=0200H
02-03	DAM=0002H
04-05	DAH=0000H
06-07	DAL=2400H

Figure 8-10. Scatter/Gather Transfers

8.9.3 752 Operation

The 752 proceeds as if doing a normal read until it starts the data transfer into memory. The contents of the linked list now controls the DMA processor; it gives the processor the byte count and address for each element on the list. The processor takes the data out of the FIFO and transfers it to memory as described in each element on the list.

8.10 DMA THROTTLE / THROTTLE DEAD TIME

The 752 always transfers IOPBs in Word mode; it uses the last specified values for the throttle and throttle dead time.

Host software can set the Throttle Dead Time (TDT) field in the Controller Parameters IOPB. This value defines the time that the 752 waits before attempting to regain control of the bus between throttle bursts. There are four valid TDT values.

TDT Value	Time
0	0 microseconds
1	3.2 "
2	6.4 "
3	12.8 "

Table 8-4. Throttle Dead Time Values

8.11 IOPB CHECKSUM

While debugging the driver, you may choose to append the checksum to the IOPB. The checksum is the sum of Bytes 0 through 17 in the IOPB, and is expressed as a 16-bit quantity. The 752 generates a checksum with the data from the IOPB and compares it to the appended checksum; a miscompare causes a fatal error. If AUD and ICS are set, the 752 appends a new checksum as it updates the IOPB. If you want to disable the checksum, the Write Controller Parameters IOPB must have a valid checksum.

8.12 FIXED/REMOVABLE MEDIA

Any physical drive with fixed and removable media, like the CDC CMD, or LMD, is accessed as one logical unit (FIXD is clear for the removable media of Unit 0, and set for the fixed media of Unit 0).

8.12.1 Head Offset

The head offset refers to the bit(s) that must be set during a drive head select sequence to select between the fixed and removable portions of the drive. Host software must specify a headoffset value for fixed/removable drives: one for the removable portion ot the drive, and one for the fixed portion. The offset value is a hexadecimal number that the 752 adds to the head number in order to select either the fixed or removable portion of the disk. Two such fixed/removable drives are the CDC Lark and CMD. The head offset value for the removable portion of a CMD is zero; the head offset value for the fixed portion is 10H. Reference the appropriate vendor manual to determine the head offset values for the fixed and removable portions of the disk.

8.13 EMBEDDED SERVO DRIVES

The 752 inherently supports embedded servo drives. Configure the drives to seek on every head select. The 752 always waits for an on-cylinder condition before starting a new sector.

8.14 DUAL PORTED DRIVES

Some SMD drives have an optional second port that connects to a second disk controller. This allows two computers to access a single disk drive.

Dual ported drives are requested by executing a normal Unit Select (which is a normal controller function, invisible to the software). Once selected, the drive port remains selected and reserved until a Release command is issued. Deselecting the drive without a release leaves the drive deselected but reserved, and unavailable to the other port. If the Release Dual Port (RDP) bit is set, the 752 executes a Release command after completing the IOPB. RDP should be set for normal transfers to a dual ported drive, unless you are trying to lockout the other controller.

Priority Select or Trespass is available if the other controller refuses to give up the port. This is an override command, and as such forces connection to a port, regardless of the other port's activity (including writing to the disk). Priority Select provides emergency access to the disk, but you must understand that it can clobber the disk if the other controller is updating the directory.

8.14 DUAL PORTED DRIVES (continued)

Leaving the disk drive in a released state when it is not being accessed provides equal access for both controllers.

NOTE

> When using dual ported drives with read ahead, you must configure the drive to release the port via a timeout mechanism. If software sets RDP, the 752 prematurely releases the port while read ahead is active. If software must set RDP to function properly with a particular dual ported drive, then you must disable read ahead by setting DRA.

8.14.1 Software Write Access Control

Host software must control access to the drive so that the two computers do not simultaneously write onto the same sectors or directory. This can corrupt the file system. Software can implement several methods for providing this control.

One control method allows one computer read/write access, and the other only read access. A second method employs disk partitioning, allowing each controller read/write access to its own partition, and read only access to the other controller's partition. The most commonly used method allows both controllers read/write access to the files, but only one controller has read/write access to the directory and allocation maps.

Another method for controlling drive access is to lock out the other controller while doing a write. Clearing RDP in the IOPB locks the other port by not releasing the first port. You have to lock out the other controller from the time you read the allocation map and directory, to when both are updated after the transfer. The IOPBs from the first read to the next to the last write have RDP clear; the last write has RDP set.

8.15 READ/WRITE HEADER, HEADER VERIFY, DATA, AND DATA ECC

This maintenance command tests the controller and software driver. It enables simulating ECC errors to verify the ECC is working. The operation includes reading a sector with its header into memory, modifying the data and then writing the sector back to the disk; the 752 does not recalculate the ECC.

8.15 READ/WRITE HEADER, HEADER VERIFY, DATA, AND DATA ECC (continued)

The data read back is either 12 or 14 bytes larger than the data sector size (depending on EC32's status). For example, given a 512-byte sector size, the 752 returns 524 bytes if EC32 is set, and 526 bytes if EC32 is clear. Table 8-5 shows the relationship between EC32's status and the returned data.

Byte	EC32 Clear	Byte	EC32 Set
0-3	Header*	0-3	Header*
4-7	Redundant Header*	4-7	Header ECC
8-(n+8)	Data	8-(n+8)	Data
(n+8)-(n+14)	48-bit ECC	(n+8)-(n+12)	32-bit ECC

* Figures 8-5 through 8-9 describe the header information

Table 8-5. EC32 vs. Returned Data

8.15.1 Simulating an ECC Error

To simulate an ECC error, read a sector by issuing a Read Header, Header Verify, Data, and Data ECC command. Then change a data byte or bit, and write the sector back by issuing a Write Header, Header Verify, Data, and Data ECC command. Reading this sector with a normal Read command should return an ECC error.

There are two common problems associated with simulating an ECC error. First, the corrected data byte may be next to the one in error. Second, the data may not be serially written to the disk as you see it on your terminal screen. Thus, a "2-bit error" crossing a byte boundary may be uncorrectable.

The 752 usually accesses memory in Word or Longword mode, but corrects data in ECC Mode 2 via byte transfers. Since some bus adapters reverse the byte addressing scheme within a word, the 752 corrects the wrong data. The only solution for this situation is to either correct the adapter or use ECC Mode 0.

The serial data is placed on the disk with bit 0 of each byte first. Table 8-6 shows a simulated 2-bit error crossing byte boundaries. Since the two bits in error are really fifteen bits apart, they may be uncorrectable. This situation can only occur when testing because a 2-bit adjacent error refers to two adjacent bits on the media.

8.15.1 Simulating an ECC Error (continued)

Before Simulated Error

Memory Data: 45 67

Serial Disk Data: 5 4 7 6
1010 0010 1110 0110

Simulated Error

Memory Data: 44 E7

Serial Disk Data: 4 4 7 E
0010 0010 1110 0111

Table 8-6. Simulated 2-Bit Error Crossing Byte Boundaries

8.16 RELEASE ON REQUEST

When ROR is enabled, the 752 tests the VMEbus between each throttle for other pending bus requests. If another request is pending, the 752 releases the bus. If there are no bus requests, the 752 remains bus master. The throttle value determines how often the 752 tests the bus: higher throttle values cause the 752 to test the bus less frequently; lower throttle values slow down the DMA.

SECTION 9: THEORY OF OPERATION

9.0 GENERAL

This section is an overview of how the controller works. It deals with the functional blocks of the hardware and microcode, and how the code affects 752 operation.

9.1 The Hardware

The 752 accommodates up to two SMD-E disk drives to VMEbus systems using these logic blocks:

VMEbus Interface
Register Read/Write and Interrupt (REGCEL)
Microcontroller
Direct Memory Access Controller (VMEDMA)
Disk Data Buffer (FIFO)
Disk Front End (DSKCEL)
SMD-E Interface

9.1.1 VMEbus Interface

This block contains interface logic for the signals on the VMEbus. The 752 is a VME slave for programming purposes, i.e., the register file. The 752 is also a slave when it responds to an interrupt acknowledge with the interrupt vector. The REGCEL performs both of these functions. The address modifier transceiver is used by the REGCEL (receive mode) and VMEDMA (driving mode). The 752 is a VME master for DMA purposes; it uses DMA to read and update IOPBs and also to read and write disk data from host memory. The VMEDMA chip performs this function. The VME data bus is 8-, 16-, or 32-bits wide; the VME address bus is 32-bits wide.

NOTE

> The 752 uses only 16 address bits for decoding its register addresses (it only compares 12 bits). It drives all 32 address bits as a master. The VMEDMA updates the lower 16 address bits while the microcontroller updates the upper 16 address bits.

9.1.2 Register Read/Write and Interrupt

The REGCEL provides the program interface for the 752. The 752 uses registers to point to an IOPB to be executed, to point to a completed IOPB, and to perform various control functions.

9.1.2 Register Read/Write and Interrupt (continued)

The VMEbus accesses the registers via a bus that is shared between the REGCEL and VMEDMA. There is no contention because the VMEDMA cannot acquire the bus while a slave (register) access is in progress. The REGCEL answers a register access by the VMEbus with the signal DTACK. The upper address bits are decoded and the proper address modifier is required to do a register access.

The microcontroller (micro) accesses the registers via the internal data bus. It programs the REGCEL to interrupt it if certain bits are set in the CSR or if a timer overflows. Other conditions are programmed to assert another interrupt to the micro.

The REGCEL also supports the VMEbus interrupt protocol. It is programmed by the micro to assert the request line to start an interrupt sequence. When the system responds with IACK and DS0 the REGCEL drives the interrupt vector onto the bus and asserts DTACK. This process causes the system to execute an interrupt routine. The interrupt service routine should clear RIO in the CSR. In this way, the 752 passes the completed IOPB back to the system.

The REGCEL has a register for storing the address modifier that the VMEDMA enables onto the bus. Like the VME address, the address modifier is pipelined. A new modifier can be loaded into the REGCEL while a different modifier is being driven onto the VMEbus.

The REGCEL also has two timers. Timer 0 is a watchdog timer: it expires and interrupts the microcontroller if it is not periodically reset by the firmware. Timer 1 is a counter for header errors. A clock comes from the DSKCEL and is asserted when a disk header does not match the expected header. If Timer 1 overflows before the desired header is found, a Header Not Found error results.

9.1.3 The Microcontroller

The 752 uses a 16-MHz 8031 microcontroller. It fetches instructions by asserting an address on Port 0, latching the address with ALE-L, and reading the data from the EPROM; it reads data into Port 0. Many of the instructions cause the micro to access an external byte using strobe decoders and a transceiver. Many of these external bytes are in the Xylogics LSI chips: REGCEL, VMEDMA, and DSKCEL. External bytes are accessed through Port 0. Port 1 is used for DSKCEL related outputs. Port 2 is used for the upper byte of the EPROM address.

Port 3 is used for miscellaneous control signals. Inputs can all be considered micro interrupts, although most are actually polled. Two inputs are from the REGCEL, one from the VMEDMA, and two from the DSKCEL.

9.1.3 The Microcontroller (continued)

This block also includes the internal RAM (IRAM) logic. The micro really uses the IRAM as a scratch pad RAM; it stores the controller, drive, and format parameters there as well as IOPBs.

The IRAM is single ported, but is used by both the VMEDMA and the micro. Since the microcontroller starts the VMEDMA, it knows when the IRAM is off limits for micro access. IOPBs are always DMAed in full words for better performance.

9.1.4 Direct Memory Access Controller

The VMEDMA controls the transfer of data between the disk buffer or IRAM, and the VMEbus. The micro programs the VMEDMA to transfer a certain amount of data to/from a specified area in system memory. To properly handle odd starting addresses, the amount of data is always a sector's worth or less. In this way, the DSKCEL can be instructed to do an even or odd address transfer on a per sector basis. Before the VMEDMA can transfer data, it must acquire the bus by sending out BUSREQ (which must be jumpered to one of the Bus Request lines). The system arbiter sends back BGIN via another jumper. The VMEDMA then asserts BUSY on the VMEbus and enables the 752 to control the VME address, data, and control lines.

A transfer involves asserting a valid address, asserting DS0 and/or DS1 and valid write data or read data, waiting for DTACK, and proper buffer control. The order of the buffer request and data strobe is reversed, depending on the direction of the transfer.

The DMA circuitry pipelines data to increase performance. The pipeline allows one word of data to be transferred on the bus while another is transferred to the buffer. In this way, the access times of the buffer and the bus can be overlapped (except for the first and last transfers of a burst). A prefetch primes the pipeline, and at the end of the burst the pipeline is emptied.

The disk buffer is word wide and uses a longword wide pipeline. The interface logic turns a VMEDMA longword request into two buffer (word) requests. The IRAM is byte wide and uses a word wide pipeline. The interface logic turns the VMEDMA word request into two IRAM requests.

9.1.5 Disk Data Buffer

The 8K-byte buffer is organized word wide. Disk data has byte parity and the parity bits are stored in a RAM. The DSKCEL will not start a write unless a sector's worth of data is in the buffer. The DSKCEL will not start a read unless the buffer has room for a sector's worth of data. The micro tracks buffer use and starts/stops the VMEDMA and DSKCEL as necessary.

9.1.6 Disk Front End

The DSKCEL is a downloadable disk sequencer. The micro loads the disk read, write, and format programs into the DSKCEL on power up, and modifies the programs when new format parameters are loaded or an alternate command (such as Read Header, Data, ECC) is received. The DSKCEL issues some SMD control signals, such as Read Gate and Write Gate, while the micro issues others, such as Cylinder Tag and Unit Tag. Generally, if timing is critical, the DSKCEL issues the signal since it runs off the disk bit clock. The DSKCEL has serial registers for FIFO data, the Header, and ECC. It performs sync bit search, header check, and ECC check and provides status bits to the micro. The DSKCEL interrupts the micro when done. DSKCEL Done may mean Header Found, End of Sector, or Bad Spot Found. Generally, the DSKCEL runs on a sector-by-sector basis, with the micro controlling how many sectors are transferred. The micro allows the DSKCEL to run. The program starts running when a sector or index pulse comes in from the disk. The micro informs the DSKCEL when the next sector involves an odd address DMA and when the current sector is the last. The DSKCEL also performs other functions, such as ECC correction, runt sector detection, and mid-transfer head tags.

9.1.7 SMD-E Interface

This block contains interface logic for SMD Connectors. The micro controls the tags for Unit Select, Cylinder, Head, Control (read/write) and the Unit Select lines. Various disk status lines, and the sector and index pulses are received and used by either the micro or the disk sequencer. The micro controls whether the pulses to the DSKCEL include sector pulses or just the index pulse.

9.1.7 SMD-E Interface (continued)

The SMD interface chips require -5 volts from an on-board regulator in order to operate properly. A drive configured as any Unit Number, from 0 thru 7, can be used with any port.

NOTE

> When no disk unit is selected, servo clock is a free-running 10-MHz clock. This is typically used during ECC correction. The clock synchronizer ensures that no clock slivers get into the DSKCEL when the Read Gate is switched. The disk sequencer clock is servo clock (interface clock) when writing the disk and read clock when reading the disk. The write clock is simply delayed servo clock.

9.1.8 Power-up

During power-up, the Open Cable Detect signal is asserted on the drive interface. This signal disables any erroneous writes. The bus signal SYSRESET sets the error LED (L2) and asserts SYSFAIL on the bus. The micro runs its diagnostics and then clears L2 and SYSFAIL.

9.1.9 Power-down

During power-down, the 752 responds to ACFAIL by turning off the DSKCEL (it allows any writes to finish the current sector) and then asserting Open Cable Detect to the drive. This sequence generates a fatal error which cannot be reset until ACFAIL is deasserted.

9.1.10 System Reset

When the 752 detects SYSRESET, it resets its internal micro and the three custom integrated circuits. This sequence immediately terminates any writes to the disk (possibly leaving it with an unreadable sector). The 752 then executes the power-up diagnostics.

9.2 THE MICROCODE

9.2.1 The Kernel

Figure 9-1 illustrates the kernel. It is entered after the Power-up test and initialization. It has four major functions, of which three will be discussed. The fourth function is scheduling DMA, and would needlessly complicate this discussion.

9.2.2 Is AIO Set?

Each time around the kernel, the 752 tests to see if the host set AIO. If AIO is set, the 752 must process the AIO. This processing entails reading the IOPB and placing it in its internal command queue. If the queue is full, the 752 saves the address of the IOPB so that it can later read it into the queue. The queue can accommodate 14 IOPBs, plus a priority IOPB; the 752 saves the next 32 IOPB (chain) addresses. This function is really tested several times in the kernel, but for simplicity Figure 9-1 shows it as a single function.

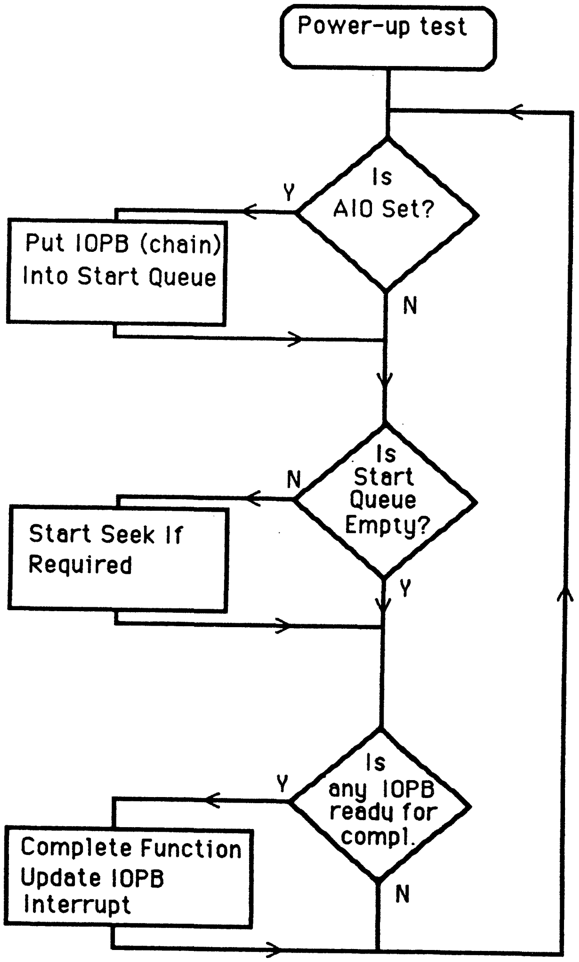


Figure 9-1. The Microcode Kernel

9.2.3 Is Start Queue Empty?

The IOPBs in the internal queue are divided into three groups: seek not started queue, seek started, and seek complete or not required. When first entering the queue, the IOPBs belong to the first group, seek not started queue. This step examines the IOPBs to determine if a seek is required. If a seek is required, and the drive is not busy, the 752 issues the Seek command to the drive and assigns the IOPB to the second queue, seek started. If a seek is not required, the 752 marks the IOPB as having its seek complete and assigns it to the third qroup, seek done or not required.

9.2.4 Is Any IOPB Ready for Completion?

The 752 checks for an IOPB in the third group, seek complete or not required. It does this by first checking if an IOPB has a seek done set; if not, it selects each drive in the second group, seek started, to determine if a seek is complete. The 752 executes the first seek done IOPB. When the 752 completes the function, it updates the IOPB and issues an interrupt.

9.2.5 Queuing IOPBs for Execution

The 752 command queue accommodates 14 IOPBs. The first AIOs have their respective IOPBs (IOPB chains) read directly into the queue until it is full. If COP is set, the 752 reorders the IOPBs inside the queue, so that it executes them in proper order.

As the 752 completes an IOPB, it frees up a slot in the internal queue, and reads in a new IOPB. If COP is set, the 752 inserts the new IOPB at the proper point in the reordered IOPBs.

9.3 PERFORMING A FUNCTION

The 752 performs each function differently. If a function requires a seek, the 752 issues the seek and waits for it to complete before performing the function. The following subsections group similar functions together and explains their differences.

9.3.1 NOP

The NOP command verifies the 752 is operational: it reads the IOPB from host memory, sets DONE, and posts a completion code.

9.3.2 Normal Reads and Writes

Normal reads and writes are very similar commands regarding 752 processing. The main difference between reads and writes is which way, and when, the data moves. On writes, the 752 DMAs the data and begins the disk transfer when the FIFO holds one sector's worth of data. On reads, the 752 begins the disk transfer immediately and begins the DMA as soon as the first word is available from the FIFO.

When enabled, the disk sequencer compares every header that arrives under the heads with the target sector. When a header compare is successful, the 752 also tests the header verify. If both tests are successful, the transfer occurs on that sector. To continue the transfer, the 752 loads the next target header so it can do a comparison on the next sector that arrives under the heads. The 752 does not wait for index before comparing headers.

If more than one sector is specified, the 752 increments the disk address on successive sectors. First, the controller increments the sector number until it reaches the maximum sector address. When the 752 reaches the maximum sector address, it clears the sector address and increments the head address. When the 752 reaches the maximum head and sector addresses, it clears them and increments the cylinder address. When the 752 reaches the maximum sector, head, and cylinder addresses, the next sector causes an Illegal Cylinder Address error.

The 752 continues, and completes the IOPB as soon as it completes the DMA and disk transfers, or an uncorrectable error occurs.

9.3.3 Seeks

Depending on the subfunction, the 752 may select the drive and read the first header that arrives under the heads. If it is a spare or bad header, the 752 reads the next header until it gets a good one. The 752 returns the data read in the header in the IOPB.

9.3.4 Drive Reset

This command issues a Fault Clear and then a Recalibrate (Return To Zero) command to the drive. The 752 waits for the Recalibrate to complete before completing the IOPB. The wait for recalibrate done is a background task, and the contoller continues processing other IOPBs (not on the drive being recalibrated).

9.3.5 Write and Read Parameters

Section 7 describes these functions in detail.

9.3.6 Extended Read and Write Commands

This section is similar to Section 9.3.2; the following subsections detail their differences.

9.3.6.1 Track Headers Commands

The disk sequencer waits for index before determining where to start the transfer. Track headers commands always start at index. The number of sector headers returned equals the physical sector count (read with a Read Drive Parameters command).

9.3.6.2 Header, Header Verify, Data, and Data ECC

The disk sequencer waits for index before determining where to start the transfer. Header, Header Verify, Data, and Data ECC commands use the sector address as an offset count from index when determining where to start. The 752 increments the sector address during a multisector transfer, but does not clear it if it reaches max sector. The controller inhibits the Illegal Sector Address error and does not increment the head and cylinder addresses.

9.3.6.3 Defect Map Extended

The disk sequencer waits for index, syncs up to the manufacturer's Defect Map and reads it into memory. The 752 only executes one track per IOPB.

9.3.6.4 Read Verify

The disk sequencer executes a Read command, and the DMA sequencer performs as if it is doing a disk write. The 752 compares the serial data from the FIFO/SERDES with the data from the disk. A miscompare causes a verify failure. The 752 returns the failing disk address in the IOPB.

9.3.7 Diagnostics

The 752 executes the power-up self test.

9.3.8 Read Ahead Theory of Operation

The 752, using an 8K-byte FIFO, reads data into the buffer before the UNIX device driver actually requests it. After completing any normal Read command, the 752 continues reading disk data into its buffer until the buffer fills (fifteen 512-byte sectors) or software requires a cylinder seek. If the next request to the 752 is a read for the next logically contiguous sector of data, it transfers the data from its buffer to system memory and completes the I/O request. The 752 terminates read ahead when it reaches a buffer full condition, or when software requires a cylinder seek. The controller satisfies subsequent reads from its buffer until it exhausts all read ahead data. It completes the next Read command with a standard disk read, and refills the read ahead buffer.

The 752 refills any buffer space freed by a Read command while the read ahead is in process before terminating read ahead. Thus, the 752 can transfer an entire cylinder's worth of data at disk speed even though the UNIX I/O requests may not be sent at disk speed. Any request other than a logically contiguous read causes the 752 to flush the buffer and execute the specific command.

9.3.9 Dyna-throttle Theory of Operation

During a Read command, each time firmware executes the DMA scheduler, the 752 calculates the amount of data currently in the buffer and DMAs from one to seven sectors to system memory. This method proves extremely efficient when transferring data previously brought in from the disk via read ahead; it also enables the 752 to catch up from heavy bus load periods when the DMA falls behind. Dyna-throttle does not override the normal throttle and throttle dead time features that tune system bus activity.

9.4 COMPLETING A FUNCTION

The 752 completes the transfer when both the DMA and disk transfers are complete. The 752 updates the IOPB in host memory, interrupts, and clears BUSY if all IOPBs in its queue are complete.

If an error occurs, the 752 completes the errored IOPB and continues processing the other IOPBs.

If a fatal error occurs, the 752 finishes the IOPB(s) in process, posts the fatal error code, and sets FERR. The host must execute a Controller Reset before sending any IOPBs to the 752.

SECTION 10: DRIVE INTERFACE

10.0 GENERAL

This section provides useful information for installing and maintaining your Xylogics Model 752 disk controller.

10.1 VMEbus INTERFACE SIGNALS

Mnemonic	Conn.	Pin	Used By 752	Description
A01	P1A	30	Y	Address Bus
A02	P1A	29	Y	
A03	P1A	28	Y	
A04	P1A	27	Y	
A05	P1A	26	Y	
A06	P1A	25	Y	
A07	P1A	24	Y	
A08	P1C	30	Y	
A09	P1C	29	Y	
A10	P1C	28	Y	
A11	P1C	27	Y	
A12	P1C	26	Y	
A13	P1C	25	Y	
A14	P1C	24	Y	
A15	P1C	23	Y	
A16	P1C	22	Y	
A17	P1C	21	Y	
A18	P1C	20	Y	
A19	P1C	19	Y	
A20	P1C	18	Y	
A21	P1C	17	Y	
A22	P1C	16	Y	
A23	P1C	15	Y	
A24	P2B	4	Y	
A25	P2B	5	Y	
A26	P2B	6	Y	
A27	P2B	7	Y	
A28	P2B	8	Y	
A29	P2B	9	Y	
A30	P2B	10	Y	
A31	P2B	11	Y	
AM0	P1B	16	Y	Address Modifier
AM1	P1B	17	Y	
AM2	P1B	18	Y	
AM3	P1B	19	Y	
AM4	P1A	23	Y	
AM5	P1C	14	Y	

10.1 VMEbus INTERFACE SIGNALS (continued)

Mnemonic	Conn.	Pin	Used By 752	Description
D00	P1A	1	Y	
D01	P1A	2	Y	
D02	P1A	3	Y	
D03	P1A	4	Y	
D04	P1A	5	Y	
D05	P1A	6	Y	
D06	P1A	7	Y	
D07	P1A	8	Y	
D08	P1C	1	Y	
D09	P1C	2	Y	
D10	P1C	3	Y	
D11	P1C	4	Y	
D12	P1C	5	Y	
D13	P1C	6	Y	
D14	P1C	7	Y	
D15	P1C	8	Y	Data Bus
D16	P2B	14	Y	
D17	P2B	15	Y	
D18	P2B	16	Y	
D19	P2B	17	Y	
D20	P2B	18	Y	
D21	P2B	19	Y	
D22	P2B	20	Y	
D23	P2B	21	Y	
D24	P2B	23	Y	
D25	P2B	24	Y	
D26	P2B	25	Y	
D27	P2B	26	Y	
D28	P2B	27	Y	
D29	P2B	28	Y	
D30	P2B	29	Y	
D31	P2B	30	Y	

Strobes

AS*	P1A	18	Y	Address Strobe
DS0*	P1A	13	Y	Data Strobe Zero
DS1*	P1A	12	Y	Data Strobe One
DTACK*	P1A	16	Y	Data Transfer Acknowledge

10.1 VMEbus INTERFACE SIGNALS (continued)

Mnemonic	Conn.	Pin	Used By 752	Description
Clocks				
SERCLK	P1B	21	N	Serial Clock
SYSCLK	P1A	10	N	System Clock
DMA				
BBSY*	P1B	1	Y	Bus Busy
BCLR*	P1B	2	N	Bus Clear
BERR*	P1C	11	Y	Bus Error
BG0IN*	P1B	4	Y	Bus Grant In
BG1IN*	P1B	6	Y	
BG2IN*	P1B	8	Y	
BG3IN*	P1B	10	Y	
BG0OUT*	P1B	5	Y	Bus Grant Out
BG1OUT*	P1B	7	Y	
BG2OUT*	P1B	9	Y	
BG3OUT*	P1B	11	Y	
BR0*	P1B	12	Y	Bus Request
BR1*	P1B	13	Y	
BR2*	P1B	14	Y	
BR3*	P1B	15	Y	
Interrupts				
IRQ1*	P1B	30	Y	Interrupt Request Levels
IRQ2*	P1B	29	Y	
IRQ3*	P1B	28	Y	
IRQ4*	P1B	27	Y	
IRQ5*	P1B	26	Y	
IRQ6*	P1B	25	Y	
IRQ7*	P1B	24	Y	
IACK*	P1A	20	Y	Interrupt Acknowledge
IACKIN*	P1A	21	Y	Interrupt Acknowledge In
IACKOUT*	P1A	22	Y	Interrupt Acknowledge Out

10.1 VMEbus INTERFACE SIGNALS (continued)

Mnemonic	Conn.	Pin	Used By 752	Description
Miscellaneous				
ACFAIL*	P1B	3	Y	AC Failure
LWORD*	P1C	13	Y	Longword
RESERVED	P2B	3	N	Reserved
SERDAT*	P1B	22	N	Serial Data
SYSRESET*	P1C	12	Y	System Reset
WRITE*	P1A	14	Y	Write
Power				
+5V	P1A,B,C	32	Y	+5 VDC
+5V	P2B	1,13,32	Y	+5 VDC
+5V STDBY	P1B	31	N	+5 VDC Standby
+12V	P1C	31	N	+12 VDC
-12V	P1A	31	N	-12 VDC
GND	P1A	9,11,15,17,19	Y	Signal Ground
GND	P1B	20,23	Y	Signal Ground
GND	P2B	2,12,22,31	Y	Signal Ground
GND	P1C	9	Y	Signal Ground

10.2 EXTENDED STORAGE MODULE DRIVE INTERFACE

Several different pin-numbering systems define the SMD-E interface. This section lists both CDC's method, and the industry standard (STND). (Physically, the cables are ribbon cables with crimp connectors on each end.)

NOTE

Xylogics follows the industry standard for pin-numbering.

10.2 EXTENDED STORAGE MODULE DRIVE INTERFACE (continued)

Name	Cable	Pin+/- CDC	Pin+/- STND	Description
Unit Select				
Unit Select Tag	A	52/22	44/43	Initiates a unit select sequence along with the Unit Select bits.
Unit Sel. Bit 0 Unit Sel. Bit 1 Unit Sel. Bit 2 Unit Sel. Bit 3	A A A A	53/23 54/24 56/26 57/27	46/45 48/47 52/51 54/53	These binary weighted signals determine which drive (out of sixteen) the 752 selects.
Open Cable Det.	A	44/14	28/27	The 752 uses this signal to deselect the drive in the event of power failure.
Unit Selected	B	09/22	17/18	A "B" cable signal; the drive has been selected.
Unit Ready	A	49/19	38/37	The selected drive is up to speed; the heads are loaded, and not faulted.
Control				
Tag 1	A	31/01	02/01	Cylinder Select Tag; the drive seeks to the cylinder selected by Bus bits 0-10.
Tag 2	A	32/02	04/03	Head Select Tag; the drive selects the head specified by Bus bits 0-9.
Tag 3	A	33/03	06/05	Control Tag; the drive executes the function defined by Bus bits 0-9.
Pwr. Seq. Hold	A	59	58	Used for power-sequencing with Remote/Local; always enabled on the 752.
Sequence Pick In	A	29	57	Used for power-sequencing with Remote/Local; always enabled on the 752.

10.2 EXTENDED STORAGE MODULE DRIVE INTERFACE (continued)

Name	Cable	Pin+/- CDC	Pin+/- STND	Description
Bus Bit 0	A	34/04	08/07	Write Gate Enable or bit 0 of head or cylinder.
Bus Bit 1	A	35/05	10/09	Read Gate Enable or bit 1 of head or cylinder.
Bus Bit 2	A	36/06	12/11	Servo Offset (+) or bit 2 of head or cylinder.
Bus Bit 3	A	37/07	14/13	Servo Offset (-) or bit 3 of head or cylinder.
Bus Bit 4	A	38/08	16/15	Fault Clear or bit 4 of head or cylinder.
Bus Bit 5	A	39/09	18/17	Address Mark Enable or bit 5 of head or cylinder.
Bus Bit 6	A	40/10	20/19	Recalibrate or bit 6 of head or cylinder.
Bus Bit 7	A	41/11	22/21	Data Strobe Early or bit 7 of head or cylinder.
Bus Bit 8	A	42/12	24/23	Data Strobe Late or bit 8 of head or cylinder.
Bus Bit 9	A	43/13	26/25	Release or bit 9 of head or cylinder.
Bus Bit 10	A	60/30	60/59	Bit 10 of cylinder address.
Clocks and Data				
Index	A	48/18	36/35	Pulses for every index mark.
Read Clock	B	17/05	08/09	Synchronizes read data.
Read Data	B	16/03	06/05	Reads data from drive.

10.2 EXTENDED STORAGE MODULE DRIVE INTERFACE (continued)

Name	Cable	Pin+/- CDC	Pin+/- STND	Description
Clocks and Data (continued)				
Sector	A	55/25	50/49	Pulses for every sector (except during index).
Servo Clock	B	14/02	02/03	Synchronizes write data.
Write Clock	B	19/06	12/11	Clock sent to drive with synchronized write data.
Write Data	B	20/08	14/15	Write data sent to drive.
Status				
Address Mark	A	50/20	39/40	The drive encountered a sector mark.
Busy	A	51/21	42/41	One port is busy in a dual port drive.
Fault	A	45/15	30/29	The drive is faulted.
On-cylinder	A	47/17	34/33	The drive is on-cylinder.
Seek End	B	23/10	20/19	The drive completed a seek, or loaded the heads.
Seek Error	A	46/16	32/31	The drive has a seek error.
Write-protect	A	58/28	56/55	The drive is write-protected.

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