REV	ECN NO	ENGR BY DATE	MFGR BY DATE
A	PINK RELEASE	DL/KD/BD 2/24/98	JG 3/98
B	ECN RELEASE	BD 8/24/98	AG 8/98
C	ECN 000465	BD 11/98	AG 11/98
D	ECN 001928	CO 7/24	AG 7/24
E	PCO 002097	KL 11/00	GM/GG 11/00
F	MI2112	YE 9/12/01	GBS 9/13/01
H	MI2574	YE 9/12/01	GBS 9/13/01
J	MI2887	ER 02/19/02	GP 02/19/02
K	MI3036	CO 04/25/02	MR 04/25/02
L	MI3409	YE 1/14/03	GP 1/14/03

NOTES:

UNLESS OTHERWISE SPECIFIED:
RESISTANCES ARE IN OHMS.
CAPACITANCES ARE IN MICROFARADS.
INDUCTANCES ARE IN MICROHENRIES.

2/1B MATCHING CONNECTIONS FOR SIGNAL FLAGS ARE LOCATED BY SHEET NUMBER AND GRID COORDINATE.

(2) DENOTES TEST POINT.

DENOTES DIGITAL GROUND.

DENOTES ANALOG GROUND.

REFERENCE DESIGNATORS

LAST USED	NOT USED
BT1	
C546	C215
CR30	
E1802	E395,E1182
F2	E1469,E1700-E1745
J21	
JP6	
L12	
MP4	
P1	
Q3	
R203	R15,R56,R73,R92,R168
RN61	RN36
SP1	
SW3	
T1	
TP24	
U186	U168
VR6	
Y4	

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PROPRIETARY INFORMATION OF ANRITSU COMPANY

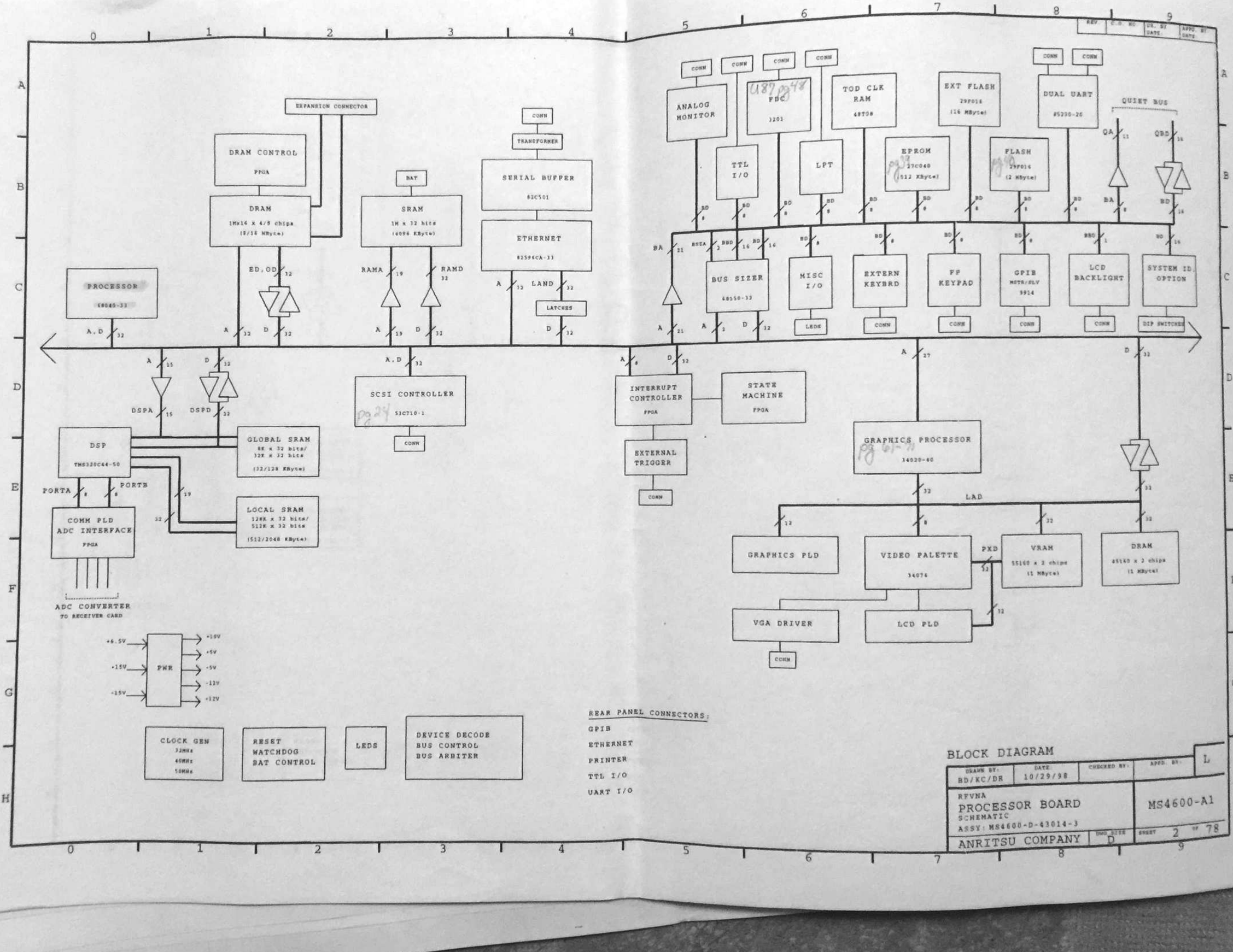
DRAWN BY/DATE	CHECKED BY/DATE	UNDER ECN CONT.	REV
BD/KC/DR	10/29/98	8/98 BY AG	L

RFVNA
PROCESSOR BOARD
SCHEMATIC
ASSY: MS4600-D-43014-3

MS4600-A1

ANRITSU COMPANY | FSCM 28944 | SHEET 1 OF 78

CPU THUAN



BLOCK DIAGRAM

DRAWN BY: BD/KC/DR	DATE: 10/29/98	CHECKED BY:	APPD. BY:	L
RFVNA PROCESSOR BOARD SCHEMATIC ASSY: MS4600-D-43014-3				MS4600-A1
ANRITSU COMPANY		SIZE D		SHEET 2 OF 78

Y1 60-212
OSC32EN
OSC32
32 MHZ
R101 0
E1756
OSC32_REF
SYNC1
REF_SEL
PLL_PU
PLL_FB
PLL_AVCC
PLL_RC
PLL_AGND
PLL_LOCK
U30 88915T70
FB SYNC0 SYNC1 REF_SEL FQ_SEL ANA_VCC RC1 AGND RST PLL_EN GND VCC
Q0 Q1 Q2 Q3 Q4 Q5 2X_Q Q/2 LOCK
RN34 15x10K
C187 0.1
C193 0.1
C166 0.1
C167 0.1
C192 0.1
R91 1K
C24 10
C188 0.1
R102 1M
C189 0.1
R103 316
RN17 15x1K
R105 0
R106 0
R107 0
R108 0
R104 0
RN27 8x51
CLK32.0
CLK32.1
CLK32.2
CLK32.3
CLK64
C191 100pF
C190 100pF
C216 100pF
C218 100pF
C217 100pF
Y4 60-263
OSC50EN
OSC50
50MHZ
C478 0.1
R190 1K
R183 0
RN56 15x10K
PU25
U173 ACT74S
C500 0.1
CLK50D2
CLK50D2*
R181 1K
R182 0
CLK25
CLK50
R159 51.1
R187 82.5
C398 100pF
C503 100pF
Y2 60-262
OSC40EN
OSC40
40 MHZ
C272 0.1
R132 1K
R131 0
RN20 15x10K
PU20
U72 ACT74S
C296 0.1
CLK40D2
CLK40D2*
R136 1K
R134 1K
R135 0
R133 0
CLK20
CLK20*
CLK40
R124 82.5
C244 100pF
R112 51.1
R96 51.1
C212 100pF
C159 100pF
CLOCKS
DRAWN BY: BD/KC/DR
DATE: 10/29/98
CHECKED BY:
APPD. BY:
L
RFVNA
PROCESSOR BOARD
SCHEMATIC
ASSY: MS4600-D-43014-3
ANRITSU COMPANY
DWG SIZE D
MS4600-A1
SHEET 3 OF 78

REV
C.O. NO.
DR BY DATE:
APPD BY: DATE:
+5V
Q3
2N2907AS
C443
0.1
C71
10
E827
E598
17/0A
SRAMVCC
E1183
R170
1K
U156
MAX691S
REPLACE BATTERY WHEN VOLTAGE IS < 3.0 V
VCC
E1184
VBATT = 3V, 500mAH
VBATT
BATTON
BATTON
E1243
R169
511K
BT1
CR3032
OSCI
VOUT
OSCSEL
LLINE
E1244
E1185
CEIN
CEOUT
16/0G
SRAMCSMX*
17/0D
SRAMCSMX*
R178
511K
E1245
WDI
WDO
PFI=1.25V
PFI
PFO
E1246
36/0E
BATTFAIL*
RESET
RESET
10/0C
MAXRESET*
GND
R171
10K
SRAMCS*
9/9B
WDEN*
19/9B
+5V
C242
0.1
WDRES*
19/9B
U56
HCT125S
+5V
R65
10K
CR25
1N914S
+5V
C442
0.1
RSTSW*
R64
100
E1177
RESET_SW*
R167
1K
E1178
U155
74HCT14S
E1179
U155
74HCT14S
10/0C
RESETSW*
RESET
JP5
C72
1
+5V
R66
10K
CR26
1N914S
ABRTSW*
R69
100
E1241
ABORT_SW*
R177
1K
E1240
U155
74HCT14S
E1242
U155
74HCT14S
19/0E
ABORTIRQ*
ABORT
JP6
C74
1
RESET/ABORT, BAT CNTRL, WDOG
L
DRAWN BY: BD/KC/DR
DATE: 10/29/98
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RFVNA
PROCESSOR BOARD
SCHEMATIC
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ANRITSU COMPANY
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U40
68040
(PGA-179)

RN28 15x1K
RN28 15x1K
R121 475
R122 475
R126 475
R114 475
R113 475
CR16 LX20465Y
CPU HALT

P_TA* 8/0F
TEA* 19/9E
TCI* 9/9A
TBI* 10/9F
CPU_BG* 10/9A
RESI* 10/9D
IPL0* IPL1* IPL2*
IPL* 19/9B
CLK32.0 3/9A
CLK64 3/9C

P_TM0 P_TM1 P_TM2 → 8/0A P_TM
P_TT0 P_TT1 → 8/0B P_TT
P_SIZ0 P_SIZ1 → 8/0F P_LOCK* / 8/0B P_SIZ
8/0D P_TS* / 8/0E P_TIP* / 8/0E P_WR* / 8/0G P_MI* / 8/0G P_RSTO*
8/0G P_BR* / 8/0E P_BB*
T/0E D
6/0A PA

+5V
+12V
CPU FAN POWER
J21

C288 C289 C259 C286 C285 C284 C260 C283 0.1
C240 C239 C235 C214 C264 C237 C236 C306 0.1
C262 C263 C305 C304 C287 C291 C303 C282 0.1
C238 C261 C290 0.1

DRAWN BY: BD/KC/DR	DATE: 10/29/98	CHECKED BY:	APPD. BY:	L
RFVNA PROCESSOR BOARD SCHEMATIC ASSY: MS4600-D-43014-3				MS4600-A1
ANRITSU COMPANY		DWG SIZE D		SHEET 5 OF 78

CPU

REV.	C.O. NO.	DR. BY DATE	APPD. BY DATE

U5
58-1783
CS2
EPM7192SQC160-10
(PQFP-160)
(1 OF 2)

+5V

VCCIO 10 25 40 55 74 89 102 118 131 155 VCCINT 56 65 137 144

A
6/9F
A0 150 A0
A1 160 A1
A2 87 A2
A12 50 A12
A13 52 A13
A14 88 A14
A15 95 A15
A16 158 A16
A17 75 A17
A18 92 A18
A19 159 A19
A20 101 A20
A21 2 A21
A22 157 A22
A23 72 A23
A28 7 A28
A29 145 A29
A30 147 A30
A31 97 A31

TM
8/9A
TM0 94 TM0
TM1 48 TM1
TM2 37 TM2

TT
8/9B
TT0 70 TT0
TT1 38 TT1

SIZ
8/9B
SIZ0 62 SIZ0
SIZ1 77 SIZ1

TA*
8/9F
TEA*
19/9E
TS*
8/9D
WR*
8/9E
CLK32.0
3/9A
RESET*
10/9B

90 TA_IN
91 TEA
108 TS
58 WR
139 CLK
141 RESET

E178 CSPLDDIS 140 CSPLDDIS

HRDY
62/9A
HOE*
62/9A
SCCIACK*
19/9B
ROM0*
19/9B

142 HRDY
51 HOE
49 SCCIACK
73 ROM0
45 PRM/FLSH

RN17
15x1K
1
16

IACKYC TP 129
SRAM2OE* 79
SRAM2WR0* 153
SRAM2WR1* 152
SRAM2WR2* 84
SRAM2WR3* 85

GND 3 18 32 47 57 64 66 81 96 111 126 138 143 148

HBS0 21
HBS1 20
HBS2 19
HBS3 17

FLASHBUF 14
FLASHEX 12
FLASHEN 11 17

E169

+5V
RN34
15x10K
16
10
JP1

PROM/FLASH
IN -> BOOT FROM FLASH
OUT -> BOOT FROM EPROM

C113 0.1
C139 0.1
C163 0.1
C164 0.1
C165 0.1
C141 0.1
C99 0.1
C97 0.1
C98 0.1
C96 0.1
C95 0.1
C112 0.1
C140 0.1
+5V
C114 0.1

TA_OUT 122
TBI 69
TCI 60
TS_DLYD 83
DSPCS 5
EPROMCS 9
FLASHCS 13
FLASHWR 123
SRAM1CS 80
SRAM1OE 76
SRAM1WR0 156
SRAM1WR1 154
SRAM1WR2 86
SRAM1WR3 78
FFF400 6
FFF420 8
SCCCS 93
SCCRD 68
LAN_PORT 125
LAN_CA 149
SCSI 63
TODCS 16
BSZCS 71
BSZDS0 61
BSZDS1 59
MIORD 151
MIOWR 104
TTLIN 35
TTLOUT 44
LPTCS 31
FDCCS 22
FDCTCNT 102
FDCDACK 33
FPKPDCS 30
KBDCS 27
TWIDCS 24
GPIBMCS 28
GPIBSCS 26
80C090 4
MSMCS 29
CPUMSMRQ 41
INREAD 34
OUTLATCH 36
CPUDSPRQ 43
NVRAMCS 15
QBCS 53
QBRD 124
QBWR 105
HCS 112
HDREAD 106
HDWRITE 100
LEDCS 42

E3
E52
E53
E50
E51
E49
E48
E6
E45
RN9
8x51
E56

E122
E47
E123
E124
E125
E120
RN11
8x51

E126
E58
RN10
8x51
E64
E57
E61
E59
E55
E62
E8
E7

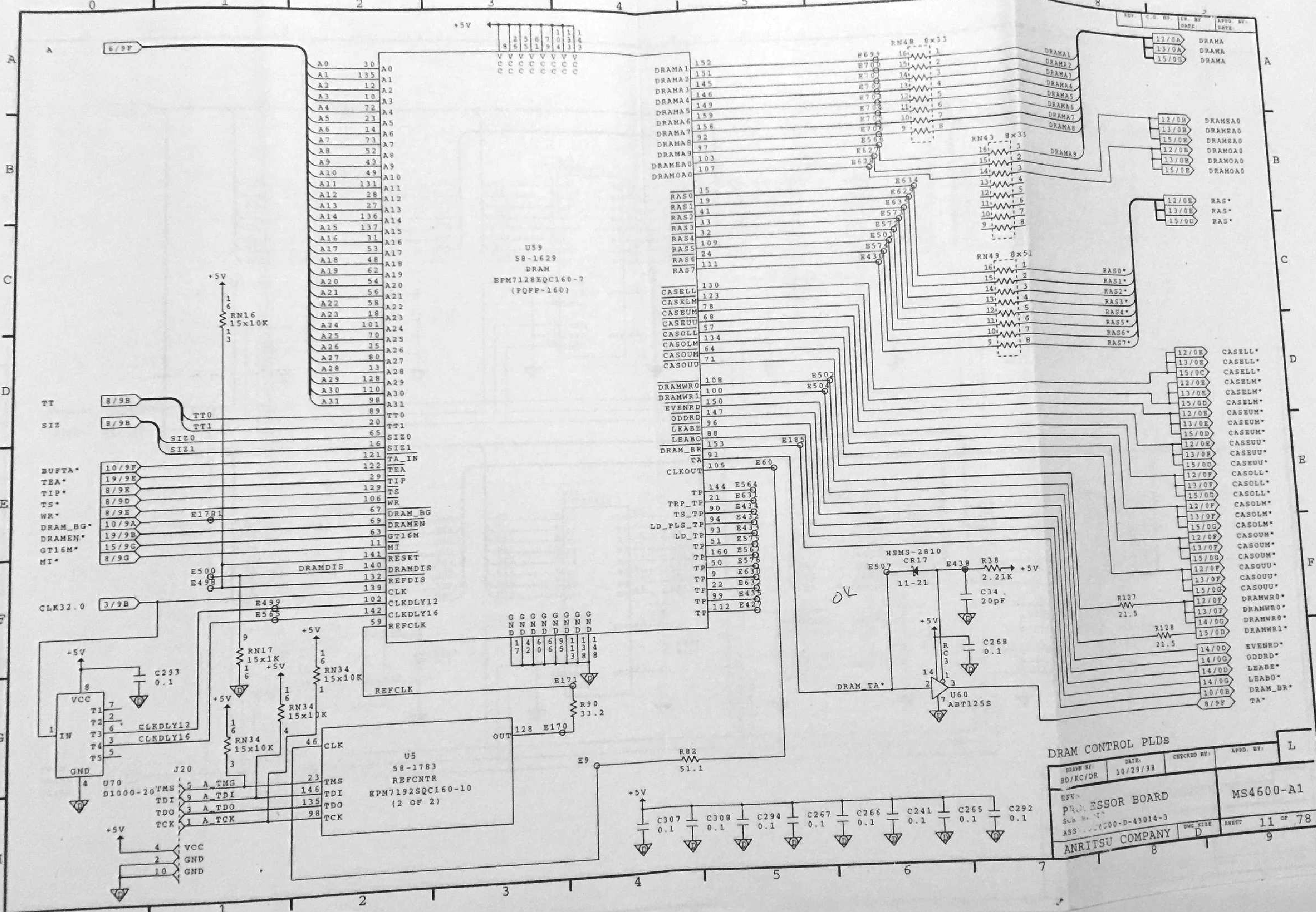
E119
E118
E117
E116
E115
E114
E113
E54
RN12
8x51
17/0H
17/0H
17/0H
17/0H
17/0G
SRAM2WR3*
SRAM2WR2*
SRAM2WR1*
SRAM2WR0*
SRAM2OE*

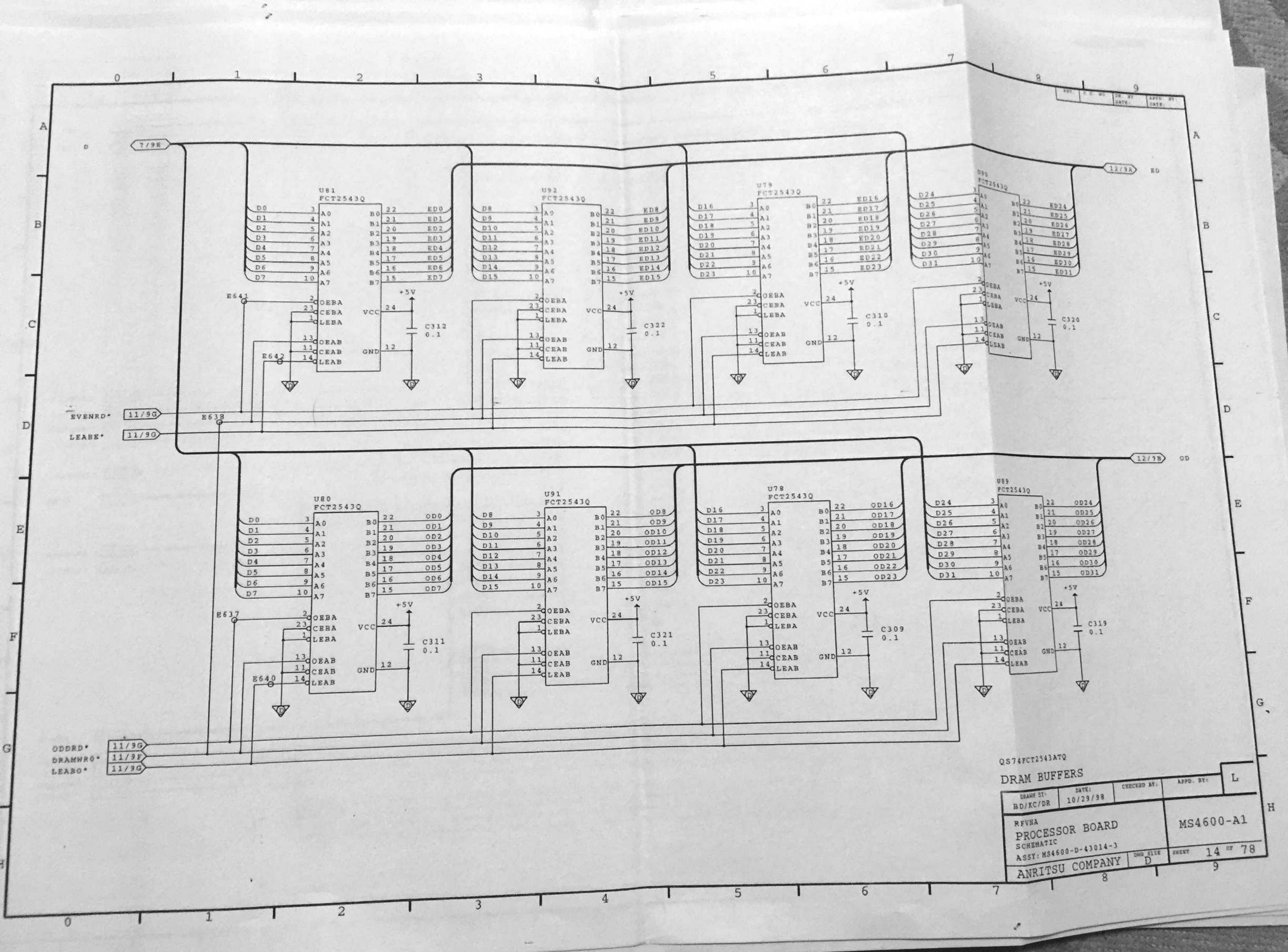
10/0F CS_TA*
10/0E CS_TBI*
5/0B TCI*
19/0D DLYD_TS*
28/0D DSPCS*
39/0D EPROMCS*
41/0E FLASHCS*
41/0E FLASHWR*
42/0E FLASHWR*
43/0E FLASHWR*
4/0D SRAMCS*
17/0D SRAM1OE*
17/0D SRAM1WR0*
17/0D SRAM1WR1*
17/0D SRAM1WR2*
17/0D SRAM1WR3*
19/0C FFF400*
19/0D FFF420*
52/0D SCCCS*
52/0B SCCRD*
20/0B LAN_PORT*
20/0C LAN_CA
24/0D SCSI*
38/0D TODCS*
34/0E BSZCS*
34/0E BSZDS0*
34/0E BSZDS1*
44/0C MIORD*
44/0C MIOWR*
50/0F TTLIN*
50/0C TTLOUT*
47/0C LPTCS*
48/0E FDCCS*
48/0E FDCTCNT
48/0E FDCDACK*
45/0G FPKPDCS*
44/0C XKBDCS*
46/0G TWIDCS*
54/0G GPIBMCS*
53/0G GPIBSCS*
19/0D CS80C090*
57/0C MSMCS*
57/0C CPUMSMRQ*
36/0E INREAD*
36/0F OUTLATCH*
28/0E CPUDSPRQ*
55/0C QBCS*
56/0F QBCS*
56/0C QBRD*
56/0C QBWR*
62/0D HCS*
51/0B HDREAD*
61/0B HDWRITE*
49/0C LEDCS*
36/0E FLASH_WEN
10/0H FLASHX*
40/0F FLASHBUF*
62/0C HBS
19/0G PRM/FLSH*

CHIP SELECT PLD

DRAWN BY: BD/KC/DR	DATE: 10/29/98	CHECKED BY:	APPD. BY	L
RFVNA PROCESSOR BOARD SCHEMATIC ASSY: MS4600-D-43014-3				MS4600-A1
ANRITSU COMPANY		DWG. SIZE D	SHEET 9 OF 78	9

DRAM_BR* 11/9G
LAN_HOLD 20/9C
LAN_LOCK* 20/9C
SCSI_BR* 24/9B
CPU_BR* 8/9G
CPU_LOCK* 8/9F
IRQCDONE 19/9F
MAXRESET* 4/9C
RESETSW* 4/9F
RSTO* 8/9G
WR* 8/9E
CLK32.0 3/9A
CS_TBI* 9/9A
CS_TA* 9/9A
A 6/9F
FLASHX* 9/9G
+5V
RN34 15x10K
E295
E293
E182 ARBRES*
E184 OE_ARB*
RN17 15x1K
C196 0.1
C195 0.1
C219 0.1
C197 0.1
VCC
DRAM_BR
LAN_HOLD
LAN_LOCK
SCSI_BR
CPU_BR
CPU_LOCK
IRQC_DONE
TTC_DONE
MAX_RESET
RESET_SW
CPU_RSTO
WR
TA
RESET
CLK
OE_ARB
BB_ENB
DRAM_BG
LAN_HOLDA
SCSI_BG
CPU_BG
CPU_MSTR
BB
MRESET
CPU_RSTI
BUFWR
RD
TA_RECLK
S0
S1
S2
BB_DRV
CPU_MST*
E376
E297
E183
U32
58-1635
RESARB
EPM7032LC44-7
GND
ARBDRV*
11 13 10 12
U56 HCT125S
E194
E754
E136
R109 51.1
E299
E490
OK
HSMS-2810
CR13
11-21
E283
E287
R28 2.21K
C25 20pF
C194 0.1
U31 ABT125S
E291
N/A OK
CR14
E285
E284
R33 2.21K
C28 20pF
E289
RN16 15x10K
E190
E130
A21
A22
A23
U44 FCT138QS
C225 0.1
RN30 8x51
11/0E DRAM_BG*
20/0C LAN_HOLDA
22/0D LAN_HOLDA
24/0D SCSI_BG*
5/0C CPU_BG*
8/9F BB*
9/0E 19/0D 22/0D 24/0D 28/0D 66/0D 68/0A RESET*
36/0F 41/0E 42/0E 43/0E 45/0A 49/0B RESET1*
44/0D 47/0G 52/0C 53/0H 54/0H 62/0E RESET2*
20/0D RESET
5/0C RESI*
34/0E 53/0G 54/0G 62/0D BUFWR*
16/0G 38/0D 39/0D 47/0B 55/0C 62/0D RD*
40/0F 41/0E 42/0E 43/0E FRD*
5/0B 24/0C TBI*
11/0E 22/0D 23/0B BUFTA*
8/9F TA*
41/0F FLASHX0*
41/0G FLASHX1*
42/0E FLASHX2*
42/0F FLASHX3*
42/0G FLASHX4*
43/0E FLASHX5*
43/0F FLASHX6*
43/0G FLASHX7*
RESET/ARBITER PLD
DRAWN BY: BD/KC/DR
DATE: 10/29/98
CHECKED BY:
APPD. BY:
L
REVNA
PROCESSOR BOARD
SCHEMATIC
ASSY: MS4600-D-43014-3
ANRITSU COMPANY
DWG SIZE D
SHEET 10 OF 78
MS4600-A1


U59
58-1629
DRAM
EPM7128EQC160-7
(PQFP-160)
U5
58-1783
REFCNTR
EPM7192SQC160-10
(2 OF 2)
U60
ABT125S
HSMS-2810
OK
DRAM CONTROL PLDs
DRAWN BY: BD/KC/DR
DATE: 10/29/98
CHECKED BY:
APPD. BY:
PROCESSOR BOARD
ANRITSU COMPANY
MS4600-A1
SHEET 11 OF 78


7/9E
12/9R
ED
12/9B
OD
U81
FCT2543Q
U92
U79
U90
U80
U91
U78
U89
D0 D1 D2 D3 D4 D5 D6 D7
D8 D9 D10 D11 D12 D13 D14 D15
D16 D17 D18 D19 D20 D21 D22 D23
D24 D25 D26 D27 D28 D29 D30 D31
A0 A1 A2 A3 A4 A5 A6 A7
B0 B1 B2 B3 B4 B5 B6 B7
OEBA CEBA LEBA
OEAB CEAB LEAB
VCC GND
+5V
E641
E642
E638
E637
E640
C312 0.1
C322 0.1
C310 0.1
C320 0.1
C311 0.1
C321 0.1
C309 0.1
C319 0.1
ED0 ED1 ED2 ED3 ED4 ED5 ED6 ED7
ED8 ED9 ED10 ED11 ED12 ED13 ED14 ED15
ED16 ED17 ED18 ED19 ED20 ED21 ED22 ED23
ED24 ED25 ED26 ED27 ED28 ED29 ED30 ED31
OD0 OD1 OD2 OD3 OD4 OD5 OD6 OD7
OD8 OD9 OD10 OD11 OD12 OD13 OD14 OD15
OD16 OD17 OD18 OD19 OD20 OD21 OD22 OD23
OD24 OD25 OD26 OD27 OD28 OD29 OD30 OD31
EVENRD* 11/9G
LEABE* 11/9G
ODDRD* 11/9G
DRAMWR0* 11/9F
LEABO* 11/9G
QS74FCT2543ATQ
DRAM BUFFERS
DRAWN BY: BD/KC/DR
DATE: 10/29/98
CHECKED BY:
APPD. BY:
L
RFVNA
PROCESSOR BOARD
SCHEMATIC
ASSY: MS4600-D-43014-3
MS4600-A1
ANRITSU COMPANY
DWG SIZE D
SHEET 14 OF 78
9

OD 12/9B
ED 12/9A

J13: ED2 7, ED3 8, ED6 9, ED7 10, ED10 11, ED11 12, ED14 13, ED15 14, ED18 27, ED19 28, ED22 29, ED23 30, ED26 33, ED27 34, ED30 35, ED31 36

J13: OD0 15, OD1 16, OD4 19, OD5 20, OD8 21, OD9 22, OD12 23, OD13 24, OD16 37, OD17 38, OD20 39, OD21 40, OD24 41, OD25 42, OD28 43, OD29 44

+5V: 3, 4, 57, 58

J12: ED0 5, ED1 6, ED4 7, ED5 8, ED8 9, ED9 10, ED12 11, ED13 12, ED16 25, ED17 26, ED20 27, ED21 28, ED24 29, ED25 30, ED28 33, ED29 34

J12: OD2 15, OD3 16, OD6 19, OD7 20, OD10 21, OD11 22, OD14 23, OD15 24, OD18 37, OD19 38, OD22 39, OD23 40, OD26 41, OD27 42, OD30 43, OD31 44

+5V: 3, 4, 57, 58

CASELL* 11/9D
CASELM* 11/9D
CASEUM* 11/9E
CASEUU* 11/9E

DRAMWR1* 11/9G

RAS* 11/9C
RAS4*
RAS5*

DRAMEA0 11/9B
DRAMOA0 11/9B

DRAMA3
DRAMA4
DRAMA7
DRAMA8

DRAMA1
DRAMA2
DRAMA5
DRAMA6
DRAMA9

+5V
RN34 15x10K
11/8E GT16M*

DRAMA 11/9A

CASOLL* 11/9E
CASOLM* 11/9F
CASOUM* 11/9F
CASOUU* 11/9F

RAS2*
RAS3*
RAS6*
RAS7*

REV.	C.O. NO.	DR. BY DATE:	APPD. BY: DATE:

DRAM EXPANSION CONNECTOR

DRAWN BY: BD/KC/DR	DATE: 10/29/98	CHECKED BY:	APPD. BY:	L
RFVNA PROCESSOR BOARD SCHEMATIC ASSY: MS4600-D-43014-3				MS4600-A1
ANRITSU COMPANY		DWG SIZE D		SHEET 15 OF 78

REV.	C.O. NO.	DR. BY / DATE:	APPD. BY / DATE:

6/9F

QS74FCT2827ATQ
U53
FCT2827Q

A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 → D0 D1 D2 D3 D4 D5 D6 D7 D8 D9

Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8 Y9 → RAMA0 RAMA1 RAMA2 RAMA3 RAMA4 RAMA5 RAMA6 RAMA7 RAMA8 RAMA9

E431 → OE1, OE2

RN17 15x1K

+5V, VCC, C30 0.1, GND

U52
FCT2827Q

A12 A13 A14 A15 A16 A17 A18 A19 A20 → D0 D1 D2 D3 D4 D5 D6 D7 D8 D9

Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8 Y9 → RAMA10 RAMA11 RAMA12 RAMA13 RAMA14 RAMA15 RAMA16 RAMA17 RAMA18

E428 → OE1, OE2

RN17 15x1K

+5V, VCC, C29 0.1, GND

17/0A RAMA

7/9E

U102
FCT2245Q

D0 D1 D2 D3 D4 D5 D6 D7 → A0 A1 A2 A3 A4 A5 A6 A7

B0 B1 B2 B3 B4 B5 B6 B7 → RAMD0 RAMD1 RAMD2 RAMD3 RAMD4 RAMD5 RAMD6 RAMD7

T/R, OE

+5V, VCC, C58 0.1, GND

QS74FCT2245ATQ

U101
FCT2245Q

D8 D9 D10 D11 D12 D13 D14 D15 → A0 A1 A2 A3 A4 A5 A6 A7

B0 B1 B2 B3 B4 B5 B6 B7 → RAMD8 RAMD9 RAMD10 RAMD11 RAMD12 RAMD13 RAMD14 RAMD15

T/R, OE

+5V, VCC, C57 0.1, GND

U100
FCT2245Q

D16 D17 D18 D19 D20 D21 D22 D23 → A0 A1 A2 A3 A4 A5 A6 A7

B0 B1 B2 B3 B4 B5 B6 B7 → RAMD16 RAMD17 RAMD18 RAMD19 RAMD20 RAMD21 RAMD22 RAMD23

T/R, OE

+5V, VCC, C56 0.1, GND

U99
FCT2245Q

D24 D25 D26 D27 D28 D29 D30 D31 → A0 A1 A2 A3 A4 A5 A6 A7

B0 B1 B2 B3 B4 B5 B6 B7 → RAMD24 RAMD25 RAMD26 RAMD27 RAMD28 RAMD29 RAMD30 RAMD31

T/R, OE

+5V, VCC, C55 0.1, GND

17/9A RAMD

SRAMCSMX* 4/9C

RD* 10/9E

BAT-BACKED SRAM ADR\DATA BFFRS

DRAWN BY:	DATE:	CHECKED BY:	APPD. BY:	
PD/KC/DR	10/29/98			L

RFVNA
PROCESSOR BOARD
SCHEMATIC
ASSY: MS4600-D-43014-3

MS4600-A1

ANRITSU COMPANY | DWG SIZE: D | SHEET 16 OF 78

RAMA 16/9A

SRAMVCC 4/9A

RAMA17

CS/A17

+5V

JP2

R67 10K

Note: trace on outside layer

SRAM1OE* 9/9B E1099

SRAM1WR0* 9/9B E1100

SRAMCSMX* 4/9C E1100

SRAM1WR1* 9/9B

SRAM1WR2* 9/9B

SRAM1WR3* 9/9B

SRAM2OE* 9/6H E914 E829

SRAM2WR0* 9/7G

SRAM2WR1* 9/7G

SRAM2WR2* 9/7G

SRAM2WR3* 9/7G

E830

C381 0.1 C380 0.1 C379 0.1 C378 0.1

C341 0.1 C340 0.1 C339 0.1 C318 0.1

U139 HM628512 — RAMA0-18 → RAMD0-7

U138 HM628512 — RAMA0-18 → RAMD8-15

U137 HM628512 — RAMA0-18 → RAMD16-23

U136 HM628512 — RAMA0-18 → RAMD24-31

U123 HM628512 — RAMA0-18 → RAMD0-7

U122 HM628512 — RAMA0-18 → RAMD8-15

U121 HM628512 — RAMA0-18 → RAMD16-23

U120 HM628512 — RAMA0-18 → RAMD24-31

16/9E RAMD

HM628512LFP-7 (512K X 8, 70ns) SOP-32
KM681000LG7L (128K X 8, 70ns) SOP-32

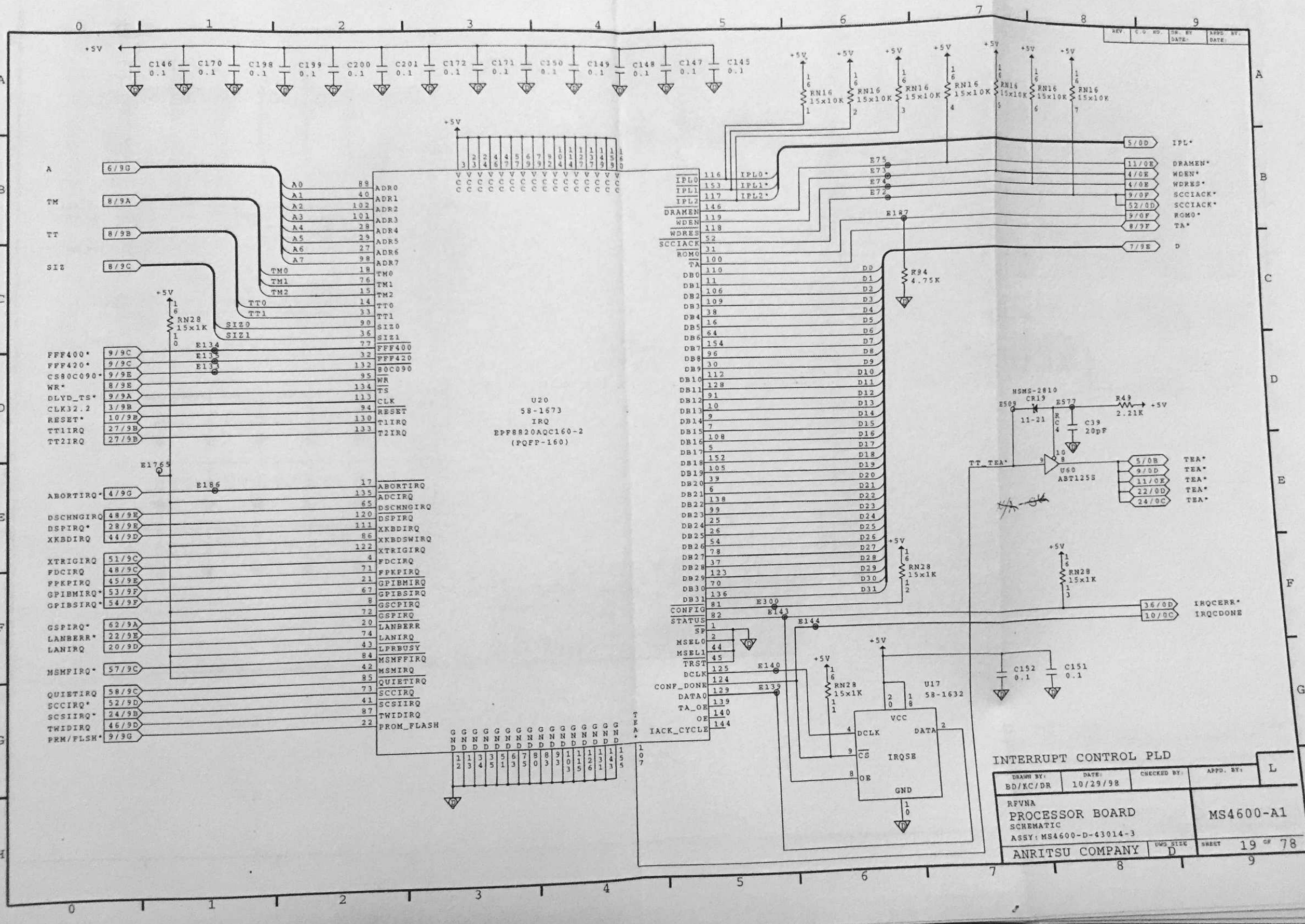
BATTERY-BACKED SRAM

DRAWN BY:	DATE:	CHECKED BY:	APPD. BY:	
SD/KC/DR	10/29/98			L

RFVNA
PROCESSOR BOARD
SCHEMATIC
ASSY: MS4600-D-43014-3

MS4600-A1

ANRITSU COMPANY | DWG SIZE D | SHEET 17 OF 78


C146 0.1
C170 0.1
C198 0.1
C199 0.1
C200 0.1
C201 0.1
C172 0.1
C171 0.1
C150 0.1
C149 0.1
C148 0.1
C147 0.1
C145 0.1
RN16 15x10K
RN28 15x1K
R94 4.75K
R49 2.21K
C39 20pF
C152 0.1
C151 0.1
HSMS-2810
CR19
U60 ABT125S
U17 58-1632
IRQSE
U20 58-1673 IRQ EPF8820AQC160-2 (PQFP-160)
INTERRUPT CONTROL PLD
RFVNA
PROCESSOR BOARD
SCHEMATIC
ASSY: MS4600-D-43014-3
ANRITSU COMPANY
MS4600-A1
DRAWN BY: BD/KC/DR
DATE: 10/29/98
SHEET 19 OF 78

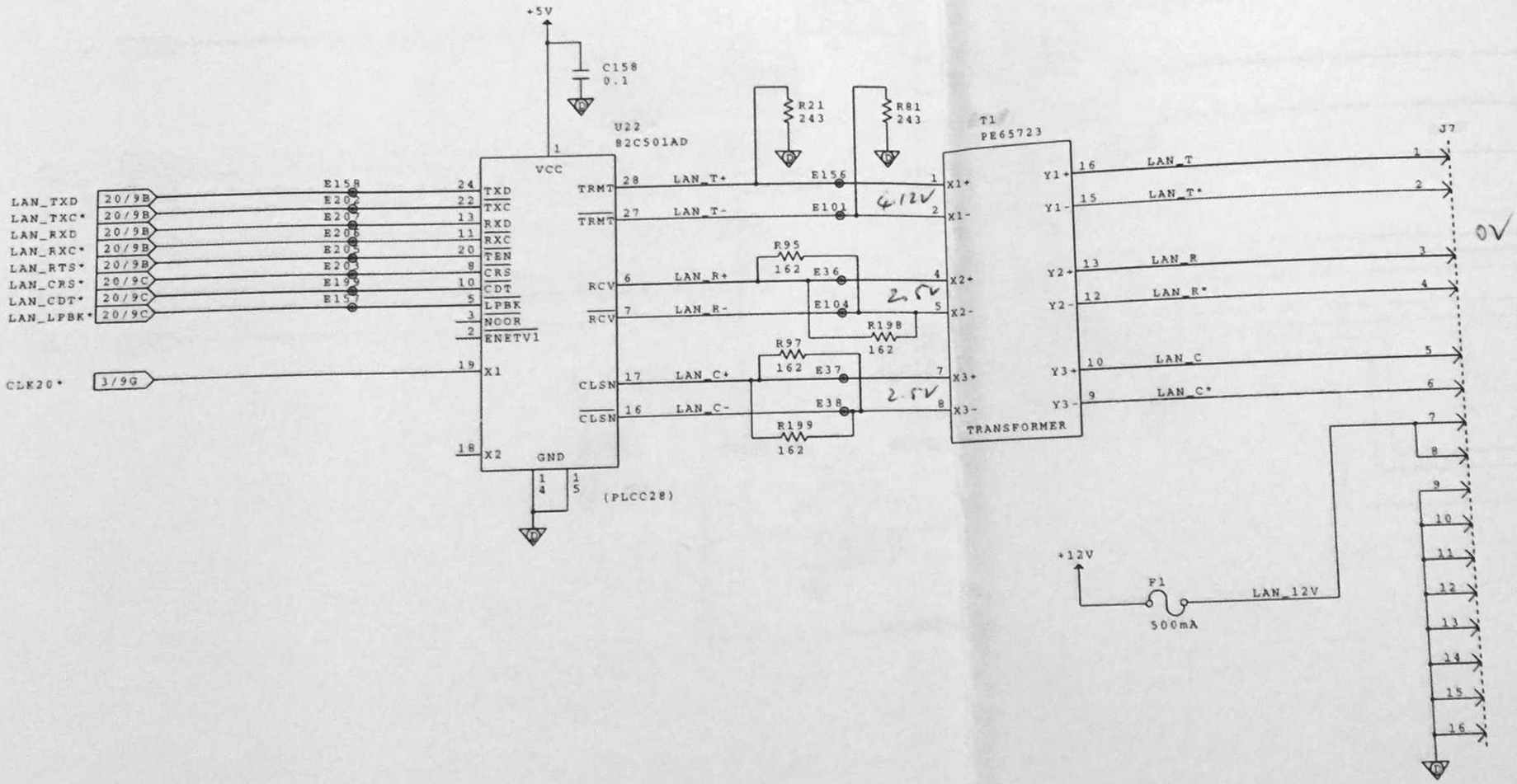
LAN CONTROLLER

DRAWN BY:	DATE:	CHECKED BY:	APPD. BY:	L
BD/KC/DR	10/29/98			

RFVNA
PROCESSOR BOARD
SCHEMATIC
ASSY: MS4600-D-43014-3

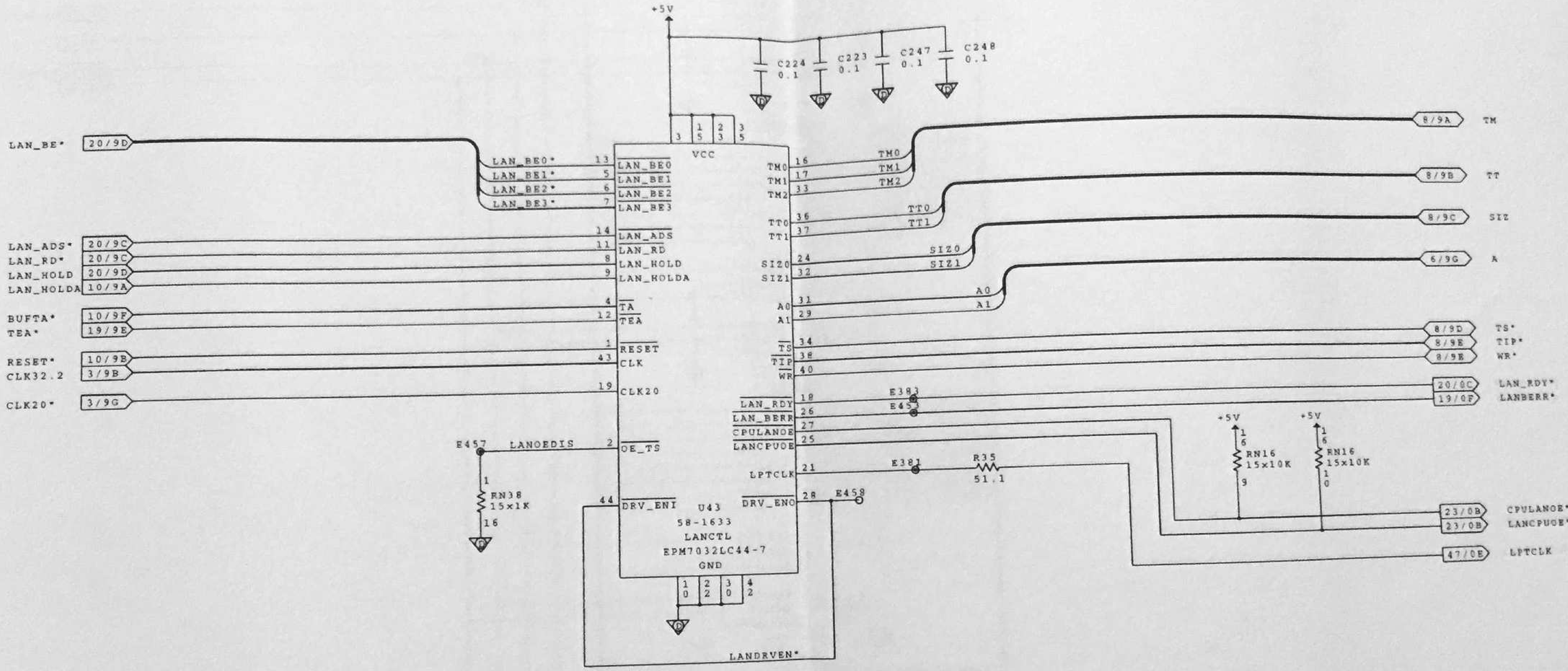
MS4600-A1

ANRITSU COMPANY — DWG SIZE D — SHEET 20 OF 78



LAN TRANSCEIVER & CONNECTOR

DRAWN BY: BD/KC/DR	DATE: 10/29/98	CHECKED BY:	APPD. BY:	L
RFVNA PROCESSOR BOARD SCHEMATIC ASSY: MS4600-D-43014-3				MS4600-A1
ANRITSU COMPANY		SIZE: D		SHEET 21 OF 78



LAN PLD

DRAWN BY:	DATE:	CHECKED BY:	APPD. BY:	L
BD/KC/DR	10/29/98			

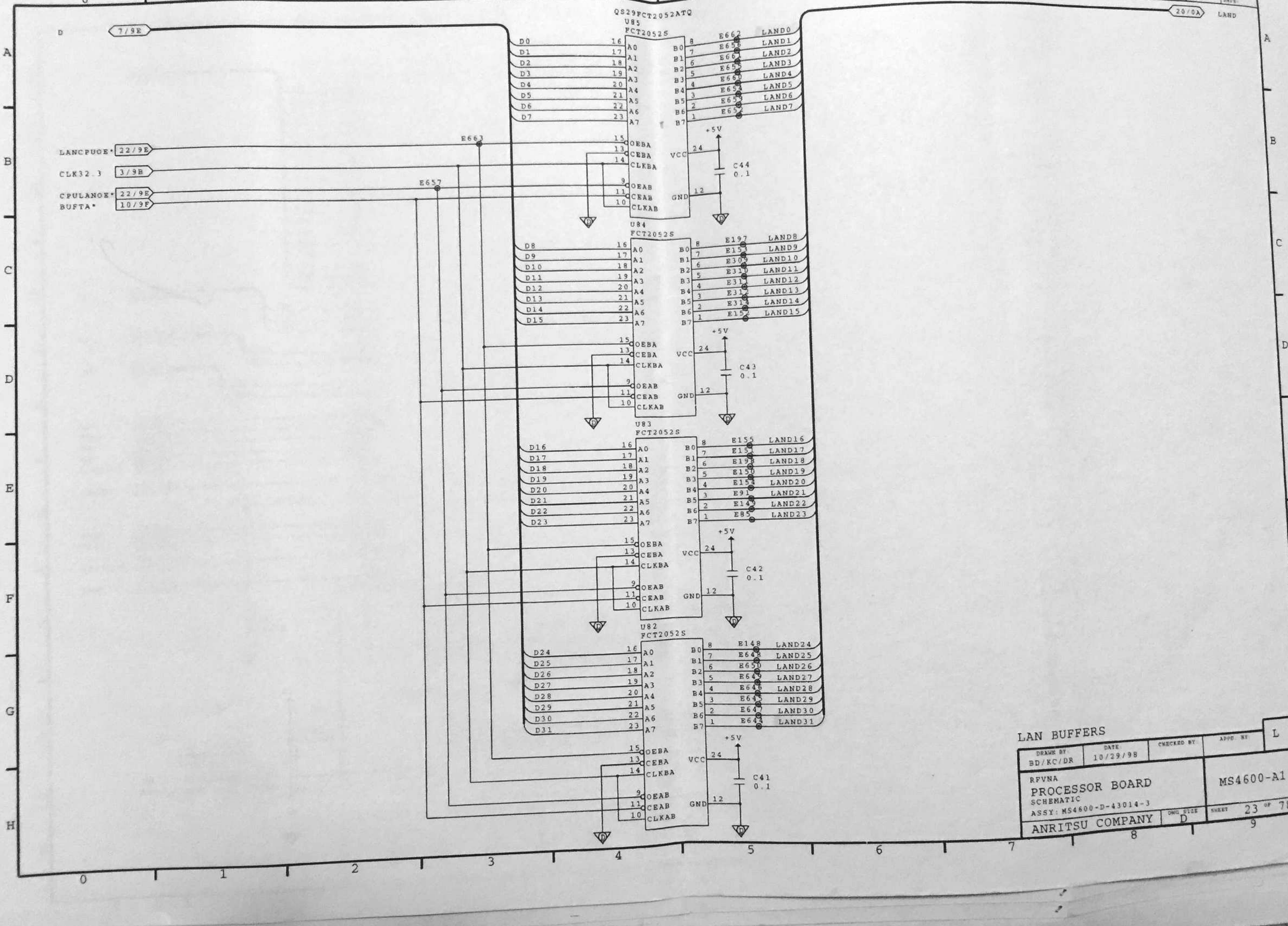
RFVNA
PROCESSOR BOARD
SCHEMATIC
ASSY: MS4600-D-43014-3

MS4600-A1

DWG SIZE D

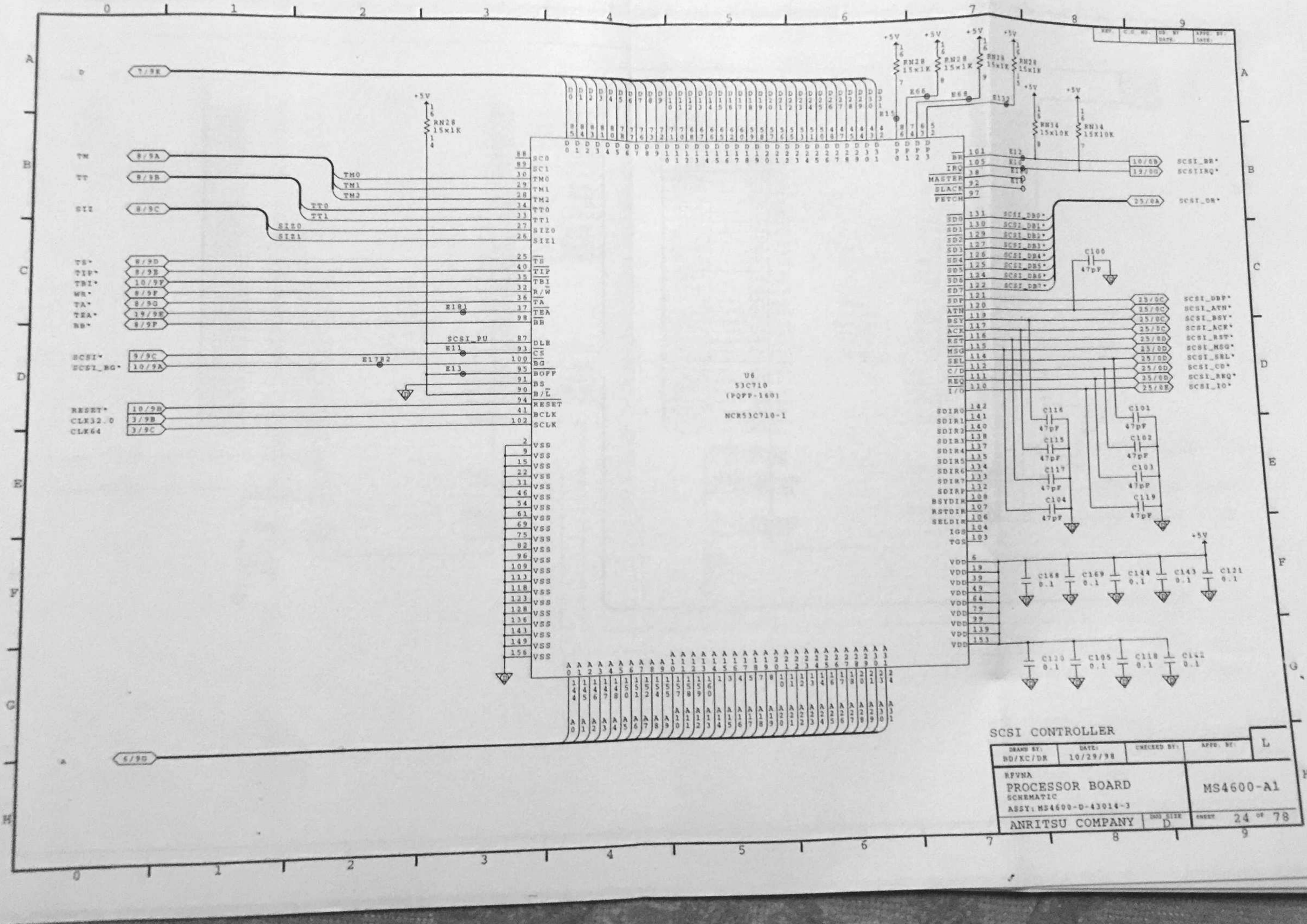
SHEET 22 OF 78

ANRITSU COMPANY



LAN BUFFERS

DRAWN BY: BD/KC/DR	DATE: 10/29/98	CHECKED BY:	APPD. BY:	L
RFVNA PROCESSOR BOARD SCHEMATIC ASSY: MS4600-D-43014-3				MS4600-A1
ANRITSU COMPANY		DWG. SIZE D		SHEET 23 OF 78


U6
53C710
(PQFP-160)
NCR53C710-1
SCSI CONTROLLER
DRAWN BY: BD/XC/DR
DATE: 10/29/98
CHECKED BY:
APPD. BY:
L
RFVNA
PROCESSOR BOARD
SCHEMATIC
ASSY: MS4600-D-43014-3
MS4600-A1
ANRITSU COMPANY
SIZE D
SHEET 24 OF 78

CPU THUAN

REV.	C.O. NO.	DR. BY DATE:	APPD. BY: DATE:

DSPLD 29/9A

DSPD 31/9B

DSPD0 104 D0
DSPD1 105 D1
DSPD2 106 D2
DSPD3 107 D3
DSPD4 108 D4
DSPD5 110 D5
DSPD6 111 D6
DSPD7 112 D7
DSPD8 113 D8
DSPD9 114 D9
DSPD10 115 D10
DSPD11 118 D11
DSPD12 120 D12
DSPD13 122 D13
DSPD14 123 D14
DSPD15 125 D15
DSPD16 127 D16
DSPD17 128 D17
DSPD18 129 D18
DSPD19 130 D19
DSPD20 131 D20
DSPD21 132 D21
DSPD22 135 D22
DSPD23 136 D23
DSPD24 137 D24
DSPD25 138 D25
DSPD26 140 D26
DSPD27 141 D27
DSPD28 142 D28
DSPD29 143 D29
DSPD30 144 D30
DSPD31 145 D31

DSPAEDE* 28/9C → 57 AE, 89 DE

DSPGRRDY* 28/9C → 91 RDY0 CE0, 93 DSPPD1, E1274 98 RDY1 101 CE1

2 RN57 15x1K 1 6 → D

U164
320C44S
(PQFP-302)
(1 of 3)
GLOBAL

A0 149 DSPA0
A1 150 DSPA1
A2 151 DSPA2
A3 152 DSPA3
A4 154 DSPA4
A5 155 DSPA5
A6 156 DSPA6
A7 157 DSPA7
A8 158 DSPA8
A9 159 DSPA9
A10 160 DSPA10
A11 162 DSPA11
A12 165 DSPA12
A13 166 DSPA13
A14 167 DSPA14
A15 168
A16 169
A17 170
A18 171
A19 174
A20 175
A21 176
A22 177
A23 178 DSPA23

STAT0 68 DSPGSTAT0
STAT1 66 DSPGSTAT1
STAT2 64 DSPGSTAT2
STAT3 61 DSPGSTAT3

LOCK 95

STRB0 58 R/W0 59 PAGE0 60
STRB1 69 R/W1 70 PAGE1 72

DSPLD0 183 LD0
DSPLD1 184 LD1
DSPLD2 185 LD2
DSPLD3 186 LD3
DSPLD4 187 LD4
DSPLD5 192 LD5
DSPLD6 194 LD6
DSPLD7 195 LD7
DSPLD8 196 LD8
DSPLD9 197 LD9
DSPLD10 200 LD10
DSPLD11 203 LD11
DSPLD12 204 LD12
DSPLD13 205 LD13
DSPLD14 206 LD14
DSPLD15 208 LD15
DSPLD16 210 LD16
DSPLD17 211 LD17
DSPLD18 212 LD18
DSPLD19 213 LD19
DSPLD20 215 LD20
DSPLD21 216 LD21
DSPLD22 219 LD22
DSPLD23 220 LD23
DSPLD24 221 LD24
DSPLD25 222 LD25
DSPLD26 224 LD26
DSPLD27 225 LD27
DSPLD28 226 LD28
DSPLD29 227 LD29
DSPLD30 228 LD30
DSPLD31 229 LD31

DSPPD2 287 LAE
291 LDE
E1276 298 LRDY0 LCE0
297
293 LRDY1 LCE1
292

3 RN57 15x1K 1 6 → D

U164
320C44S
(PQFP-302)
(2 of 3)
LOCAL

LA0 232 DSPLA0
LA1 233 DSPLA1
LA2 234 DSPLA2
LA3 235 DSPLA3
LA4 237 DSPLA4
LA5 238 DSPLA5
LA6 239 DSPLA6
LA7 240 DSPLA7
LA8 241 DSPLA8
LA9 242 DSPLA9
LA10 243 DSPLA10
LA11 245 DSPLA11
LA12 248 DSPLA12
LA13 249 DSPLA13
LA14 250 DSPLA14
LA15 251 DSPLA15
LA16 252 DSPLA16
LA17 253 DSPLA17
LA18 254 DSPLA18
LA19 255
LA20 257
LA21 258
LA22 259
LA23 260

LSTAT0 279
LSTAT1 277
LSTAT2 275
LSTAT3 273

LLOCK 284

LSTRB0 301 E1368
LR/W0 300 E1406
LPAGE0 299

LSTRB1 296 E1281
LR/W1 295 E1284
LPAGE1 294

28/0B DSPA
30/9A DSPA
31/0B DSPA
29/0A DSPLA

R188 51.1 29/0G DSPECS*

1 U159 74F04S 2 E1226 R68 51.1 29/0G DSPEOE*

+5V
C467 0.1

13 U159 74F04S 12 E1280 1 RN59 8x33 16 29/0E DSPLROE*

7 U159 74F04S

2 RN59 8x33 15 29/0E DSPLRCS*

3 RN59 8x33 14 29/0E DSPLRWR*

28/0C DSPGSTAT
28/0D DSPGLOCK*
28/0C DSPGRCS*
28/0C DSPGRWR*
28/0E GSTRB1*

DSP (GLOBAL & LOCAL)

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BD/KC/DR	10/29/98			L

RFVNA
PROCESSOR BOARD
SCHEMATIC
ASSY: MS4600-D-43014-3

MS4600-A1

ANRITSU COMPANY | DWG SIZE D | SHEET 26 OF 78

CPU

U164
320C44S
(PQFP-302)
(3 of 3)

COMMON

DSP (COMMON)

DRAWN BY:	DATE:	CHECKED BY:	APPD. BY:	
BD/KC/DR	10/29/98			L

RFVNA
PROCESSOR BOARD
SCHEMATIC
ASSY: MS4600-D-43014-3

ANRITSU COMPANY | DWG SIZE D | SHEET 27 OF 78 | MS4600-A1

CPU THUAN

GRAPHICS CONTROLLER

REV.	C.O. NO.	DR. BY DATE:	APPD. BY DATE:

PROPRIETARY INFORMATION OF ANRITSU COMPANY

DRAWN BY/DATE:	CHECKED BY/DATE	UNDER PCO CONT. DATE	BY M.E	REV
BD/KC/DR	10/29/98			L

RFVNA
PROCESSOR BOARD
SCHEMATIC
ASSY: MS4600-D-43014-3

ANRITSU COMPANY — FSCM 28944

MS4600-A1

SHEET 62 OF 78

VIDEO INTERFACE PALETTE

U12B
TLC34076

PXD0	29	P0
PXD1	28	P1
PXD2	27	P2
PXD3	26	P3
PXD4	25	P4
PXD5	24	P5
PXD6	23	P6
PXD7	22	P7
PXD8	21	P8
PXD9	20	P9
PXD10	19	P10
PXD11	18	P11
PXD12	17	P12
PXD13	16	P13
PXD14	15	P14
PXD15	14	P15
PXD16	13	P16
PXD17	12	P17
PXD18	11	P18
PXD19	10	P19
PXD20	9	P20
PXD21	8	P21
PXD22	7	P22
PXD23	6	P23
PXD24	5	P24
PXD25	4	P25
PXD26	3	P26
PXD27	2	P27
PXD28	1	P28
PXD29	84	P29
PXD30	83	P30
PXD31	82	P31

PXD — 64/9A

LAD0	36	D0
LAD1	37	D1
LAD2	38	D2
LAD3	39	D3
LAD4	40	D4
LAD5	41	D5
LAD6	42	D6
LAD7	43	D7

LAD — 62/9A

LLA5	32	RS0
LLA6	33	RS1
LLA7	34	RS2
LLA8	35	RS3

LLA — 66/9C

	31	RD
	30	WR
	62	SFLAG

PALETRD* — 66/9D
PALETWR* — 66/9D
SFLAG — 66/9D

E1012 — PALPU 77

	CLK0
	CLK1
	CLK2
	CLK3
	CLK3N

CLK25 — 3/9E

RN57 15x1K (6, 1, 16)

GSPRS* — 62/9G
GSPVS* — 62/9F
GSPBL* — 62/9G

HSYNC 58 · VSYNC 59 · BLANK 60 · VGABLANK 61 · FSADJ 51 · VREF 53 · VGA0 65 · VGA1 66 · VGA2 67 · VGA3 68 · VGA4 69 · VGA5 70 · VGA6 71 · 8/6 64

E838 — R59 475 — E1787 — R149 34.8 — E921 — C360 0.1

SCLK	79	E1009	SCLKS
VCLK	78	E1005	VCLKS
HSYNCOUT	46	E923	
VSYNCOUT	47	E922	
IOR	48	E746	
IOG	49	E745	
IOB	50	E839	
COMP	52	E925	COMP
MUXOUT	63		

R160 34.8 · R158 34.8

64/0G SCLK
62/0E VCLK
69/0A VCLK
67/0C HSYNC
67/0A VSYNC
67/0F R
67/0E G
67/0D B

C361 0.1

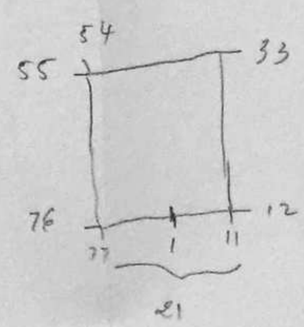
R151 75 · R150 75 · R152 75

+5V

VDD45	45
VDD55	55
VDD57	57
VDD81	81

C359 0.1 · C358 0.1 · C373 0.1 · C399 0.1 · C63 47 50V

GND	44
GND	54
GND	56
GND	80



PROPRIETARY INFORMATION OF ANRITSU COMPANY

DRAWN BY/DATE:	CHECKED BY/DATE:	UNDER PCC CONT.	REV
BD/KC/DR	10/29/98	____ BY ____ DATE ____	L

RFVNA
PROCESSOR BOARD
SCHEMATIC
ASSY: MS4600-D-43014-3

MS4600-A1

ANRITSU COMPANY — PDCN 20946 — SHEET 63 OF 78

DISPLAY VRAM

MAD
62/8C
CAS*
62/9E
CAS0*
CAS1*
CAS2*
CAS3*
E1747
GRAS1*
WE*
TRQE*
VSF
SOE*
SCLK
66/9D
62/9D
62/9F
E1748
66/9D
E1749
66/9C
E1750
63/9A

+5V
C427 0.1
C428 0.1
C455 0.1
C476 0.1
C456 0.1
C429 0.1

MAD0 37 A0
MAD1 36 A1
MAD2 35 A2
MAD3 34 A3
MAD4 31 A4
MAD5 30 A5
MAD6 29 A6
MAD7 28 A7
MAD8 27 A8

26 RAS
24 CASL
39 CASU
25 WE
2 TRG
41 DSF
63 SE
64 SC

DQ0 5 LAD0
DQ1 7 LAD1
DQ2 10 LAD2
DQ3 12 LAD3
DQ4 15 LAD4
DQ5 17 LAD5
DQ6 20 LAD6
DQ7 22 LAD7
DQ8 43 LAD8
DQ9 45 LAD9
DQ10 48 LAD10
DQ11 50 LAD11
DQ12 53 LAD12
DQ13 55 LAD13
DQ14 58 LAD14
DQ15 60 LAD15

SQ0 4 E1019 PXD24
SQ1 6 E1024 PXD25
SQ2 9 E1018 PXD26
SQ3 11 E1023 PXD27
SQ4 14 E1011 PXD28
SQ5 16 E1014 PXD29
SQ6 19 E1010 PXD30
SQ7 21 E1008 PXD31
SQ8 44 E1017 PXD16
SQ9 46 E1027 PXD17
SQ10 49 E1022 PXD18
SQ11 51 E1028 PXD19
SQ12 54 E1021 PXD20
SQ13 56 E1026 PXD21
SQ14 59 E1020 PXD22
SQ15 61 E1025 PXD23

GND 3 13 23 33 42 52 62
QSF 38

U157
PD55160

+5V
C430 0.1
C431 0.1
C457 0.1
C477 0.1
C432 0.1
C458 0.1

MAD0 37 A0
MAD1 36 A1
MAD2 35 A2
MAD3 34 A3
MAD4 31 A4
MAD5 30 A5
MAD6 29 A6
MAD7 28 A7
MAD8 27 A8

26 RAS
24 CASL
39 CASU
25 WE
2 TRG
41 DSF
63 SE
64 SC

DQ0 5 LAD16
DQ1 7 LAD17
DQ2 10 LAD18
DQ3 12 LAD19
DQ4 15 LAD20
DQ5 17 LAD21
DQ6 20 LAD22
DQ7 22 LAD23
DQ8 43 LAD24
DQ9 45 LAD25
DQ10 48 LAD26
DQ11 50 LAD27
DQ12 53 LAD28
DQ13 55 LAD29
DQ14 58 LAD30
DQ15 60 LAD31

SQ0 4 E931 PXD8
SQ1 6 E936 PXD9
SQ2 9 E937 PXD10
SQ3 11 E933 PXD11
SQ4 14 E934 PXD12
SQ5 16 E932 PXD13
SQ6 19 E1015 PXD14
SQ7 21 E1016 PXD15
SQ8 44 E840 PXD0
SQ9 46 E841 PXD1
SQ10 49 E843 PXD2
SQ11 51 E842 PXD3
SQ12 54 E928 PXD4
SQ13 56 E929 PXD5
SQ14 59 E930 PXD6
SQ15 61 E927 PXD7

GND 3 13 23 33 42 52 62
QSF 38

U158
PD55160

62/9B LAD
63/0A PXD
69/0B PXD

PROPRIETARY INFORMATION OF ANRITSU COMPANY

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BD/KC/DB	10/29/98	DATE BY M.K.	L

RFVNA
PROCESSOR BOARD
SCHEMATIC
ASSY: MS4600-D-43014-3

MS4600-A1

ANRITSU COMPANY | FSCM 26944 | SHEET 64 OF 7

DISPLAY DRAM

REV.	C.O. NO.	DR. BY DATE	APPD. BY DATE

MAD — 62/9C

62/9B LAD

+5V

C362 0.1 C363 0.1 C400 0.1

C364 0.1 C365 0.1 C401 0.1

MAD0 16 MAD1 17 MAD2 18 MAD3 19 MAD4 22 MAD5 23 MAD6 24 MAD7 25 MAD8 26

A0 A1 A2 A3 A4 A5 A6 A7 A8

RAS 14 CASL 29 CASU 28 WE 13 OE 27

GRAS0* — 66/9C — E938

CAS0* CAS1* CAS2* CAS3*

CAS* — 62/9E

WE* — 62/9D — E939

RN57 15x1K

U129 PD45160

U130 PD45160

LAD0 2 LAD1 3 LAD2 4 LAD3 5 LAD4 7 LAD5 8 LAD6 9 LAD7 10 LAD8 31 LAD9 32 LAD10 33 LAD11 34 LAD12 36 LAD13 37 LAD14 38 LAD15 39

LAD16 2 LAD17 3 LAD18 4 LAD19 5 LAD20 7 LAD21 8 LAD22 9 LAD23 10 LAD24 31 LAD25 32 LAD26 33 LAD27 34 LAD28 36 LAD29 37 LAD30 38 LAD31 39

PROPRIETARY INFORMATION OF ANRITSU COMPANY

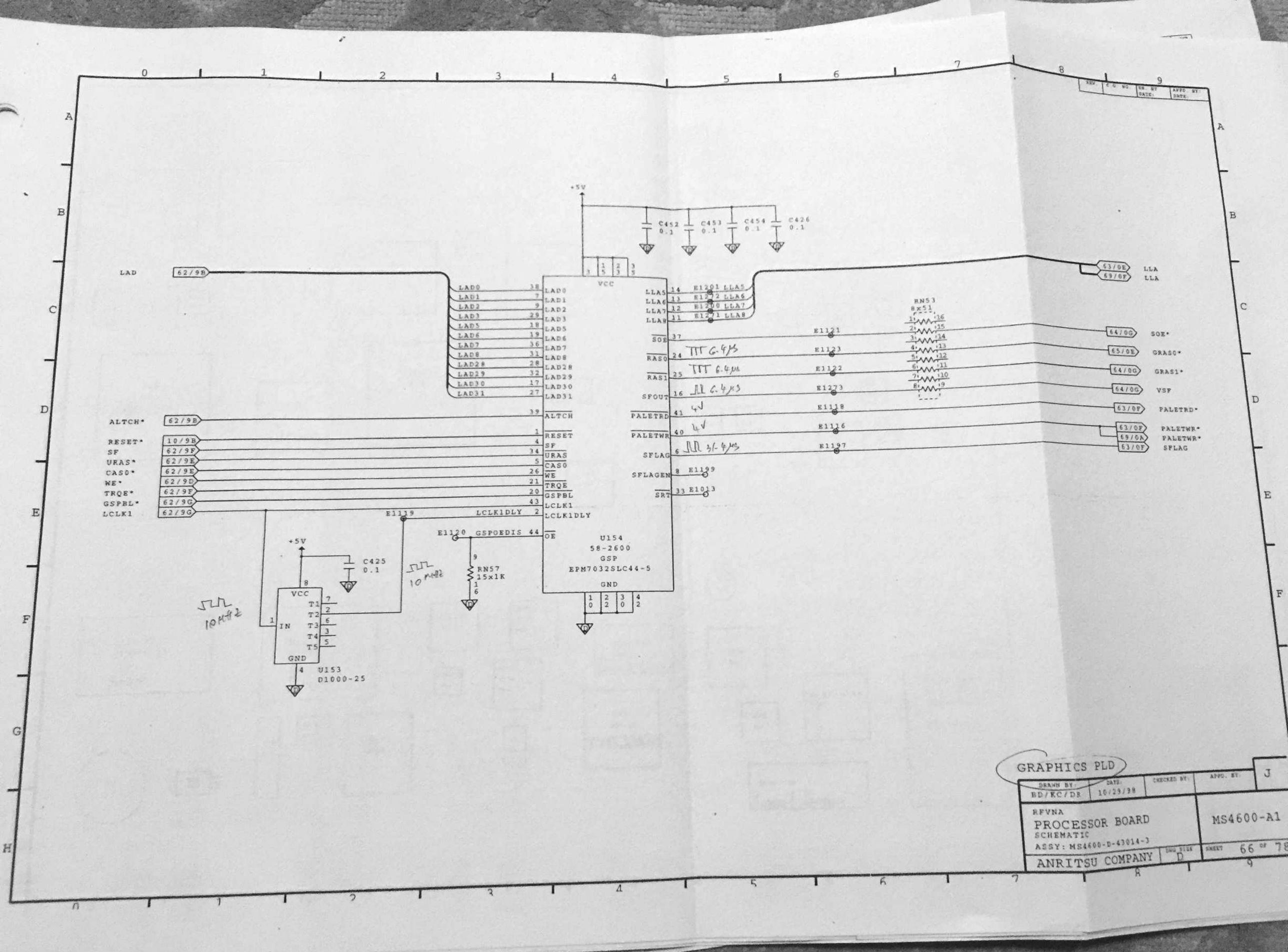
DRAWN BY/DATE	CHECKED BY/DATE	UNDER PCO CONT	REV
BD/KC/DR	10/29/98	DATE BY M.E	L

RFVNA
PROCESSOR BOARD
SCHEMATIC
ASSY: MS4600-D-43014-3

MS4600-A1

ANRITSU COMPANY — FSCM 20944 — SHEET 65 OF 78

C 250-248



GRAPHICS PLD

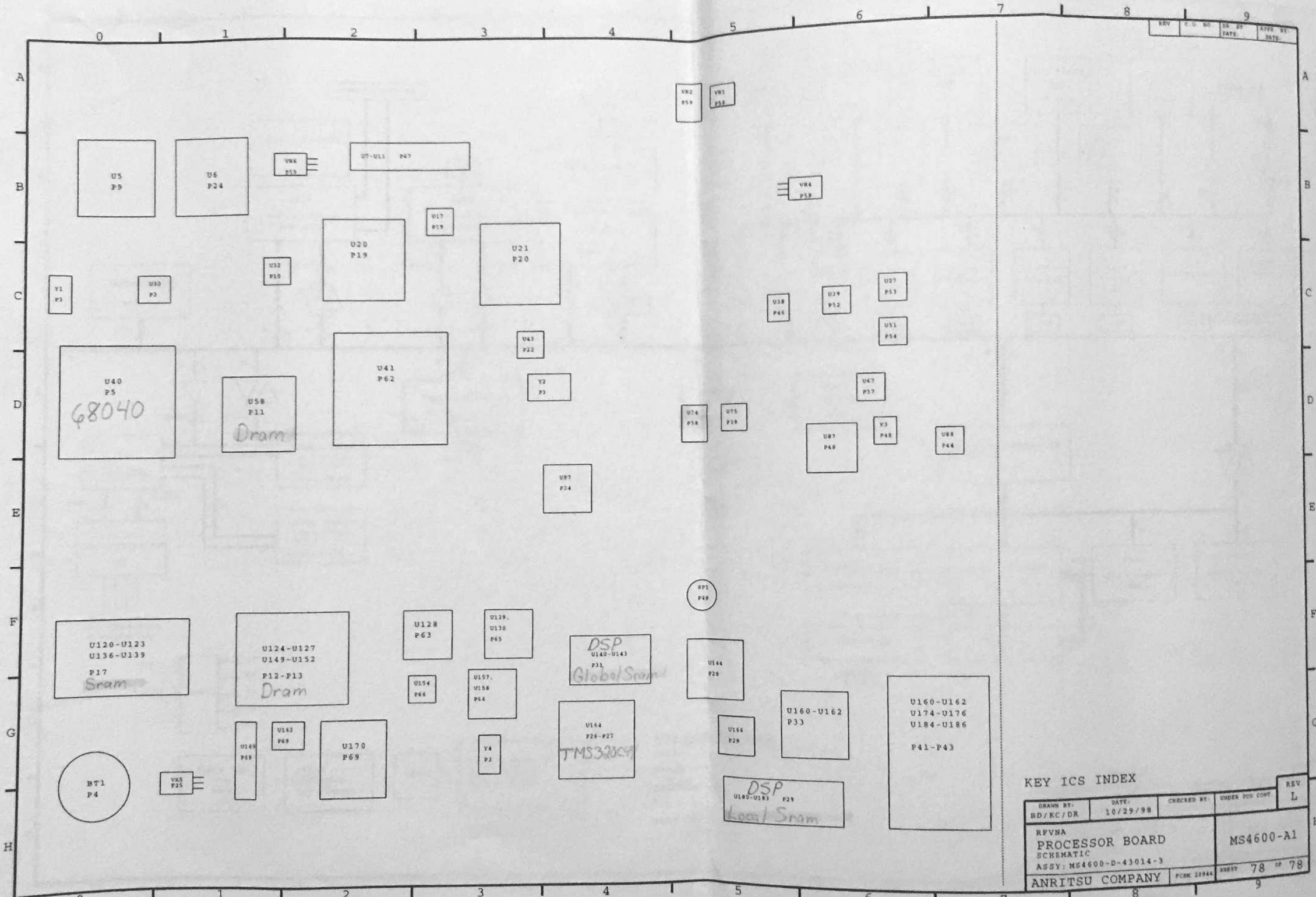
DRAWN BY:	DATE:	CHECKED BY:	APPD. BY:	J
BD/KC/DR	10/29/98			

RFVNA
PROCESSOR BOARD
SCHEMATIC
ASSY: MS4600-D-43014-3

MS4600-A1

ANRITSU COMPANY | DWG SIZE D | SHEET 66 OF 78

CPU THIUAN


REV
C.O. NO.
DR BY DATE
APPR BY DATE
U5 P9
U6 P24
VRK P53
U7-U11 P47
U17 P19
U20 P19
U21 P20
U32 P10
Y1 P3
U30 P3
U40 P5 68040
U58 P11 Dram
U41 P62
U43 P22
Y2 P3
U97 P34
VR2 P59
VR1 P58
VR4 P59
U38 P46
U39 P52
U27 P53
U51 P54
U47 P37
U74 P38
U75 P39
U87 P48
Y3 P48
U88 P44
RP1 P49
U120-U123 U136-U139 P17 Sram
U124-U127 U149-U152 P12-P13 Dram
U128 P63
U129, U130 P65
U154 P66
U157, U158 P64
U163 P69
U169 P69
U170 P69
Y4 P3
BT1 P4
VR5 P25
U140-U143 P31 DSP Global Sram
U164 P26-P27 TMS320C49
U144 P28
U166 P29
U180-U183 P29 DSP Local Sram
U160-U162 P33
U160-U162 U174-U176 U184-U186 P41-P43
KEY ICS INDEX
DRAWN BY: BD/KC/DR
DATE: 10/29/98
CHECKED BY:
UNDER PCO CONT.
REV L
RFVNA
PROCESSOR BOARD
SCHEMATIC
ASSY: MS4600-D-43014-3
MS4600-A1
ANRITSU COMPANY
FCSK 20944
SHEET 78 OF 78

PCS 2574
C7: 233-46
~~C547-C551~~: remove
R124, R187: 138-82R5-1
Y2 = 60-262
Y4: 60-263
233-275 (Heat sink)
790-593 (
~~B 4315 4~~
10-93 (diode - [illegible])

(3) PLACE SERIAL/ISSUE NO. LABELS APPROX. WHERE SHOWN CIRCUIT SIDE

633-25 (Battery)
250-248 (Cap)

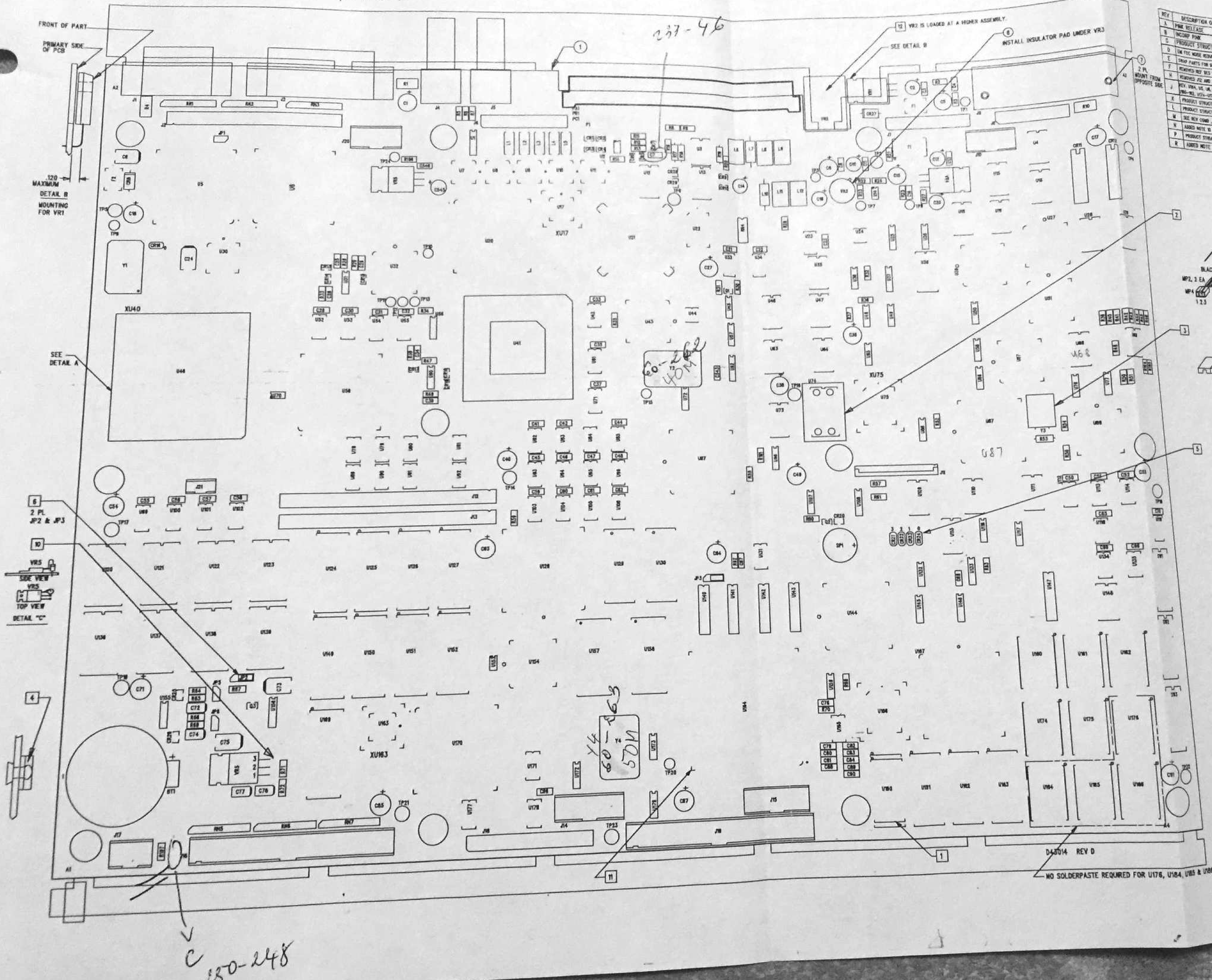
(12) ITEMS PROVIDED FOR BUT NOT INSTALLED

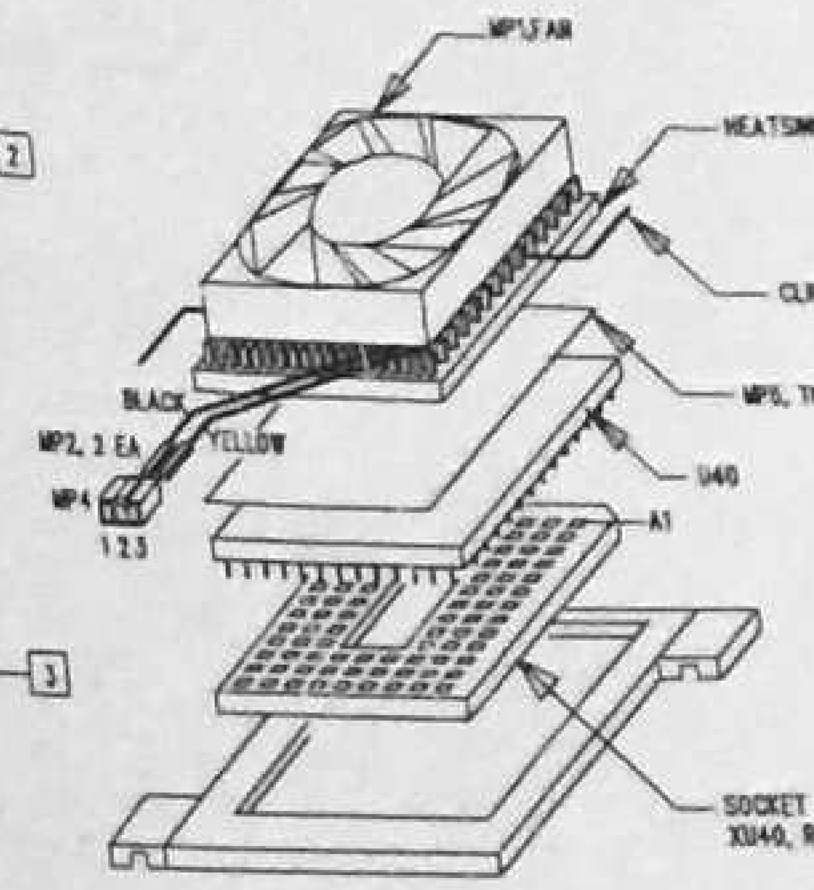
C79–C84,C88–C90,C326–C328,C330–C332,C386–C388,C520,C538
C441,C488,C490–C492,C509,C511,C536–C542,C547–C551
J15,J18,J20
L13
RN5–RN7
TP1–TP24
U162,U174–U176,U184–U186
VR2

PROPRIETARY INFORMATION OF ANRITSU

DRWN BY: T.EBELT	DATE 1/98	MATERIAL: N/A	
CHKD BY: R.BARNES	DATE 4/98	ANRITSU	
TOLERANCES: UNLESS OTHERWISE SPECIFIED		TITLE PC ASSEMBLY PROCESSOR BD MS4600 - A1	
2 PLCS ± — ANGLES ± —		FSCM 20944	DWG NO 043014-3 / REV B
3 PLCS ± —		SCALE: NONE	UNDER ECN CONTROL B/DMBY DATE AG/ME SHEET 2 OF 3
4 PLCS ± — SURFACES ✓			
FINISH: N/A	DO NOT SCALE DWG		

CPU THUAN





DETAIL A

HEATSINK KIT MOUNTING DETAIL [7]

REV	DESCRIPTION OF REVISION	ECN NO	BY	DATE	CHCKD
A	PINK RELEASE	—	TE	4/98	BD
B	INCORP PINK	ECN REL	TE	5/98	AG
C	PRODUCT STRUCTURE UPDATE	[illegible]	JL	6/98	AG
D	UM FCC NOISE REDUCTION CAPS ADDED	M465	TE	11/98	AG
E	SWAP PARTS FOR DETAIL A	M838	JL	3/99	AG
F	REMOVED REF DES U184	M1146	JL	8/17/99	AG
H	REMOVED J2 AND J3 FROM NOTE PG 1	M1257	JL	8/5/99	AG
J	REV U184, U5, U8, U33, U28, U175 & U180–U83, U174–U176, U184–186 F/PRINTS	M1524	JL	12/17/99	AG
K	PRODUCT STRUCTURE CHANGED	M1587	JL	2/29/00	JVD
L	PRODUCT STRUCTURE CHANGED	M2024	KB	8/28/00	AG
M	SEE REV COMB, NOT IMPLEMENTED	[illegible]	KB/KC	8/28/00	AG
N	ADDED NOTE 10	M2112	CO	1/01	DEG
P	PRODUCT STRUCTURE CHANGED	MC2750	CO	1/01	DEG
R	ADDED NOTE 11,12 AND MP5	M2574	TE	8/01	DEG

SURFACE MOUNT ASSEMBLY

NOTES: UNLESS OTHERWISE SPECIFIED

[1] NORMALLY LOAD U180 – U183 WITH USI 58-1605. IF LOADING WITH ALTERNATE USI 58-1609, THEN LOAD PIN 1 OF THE IC AT PIN 2 OF THE FOOTPRINT AS SHOWN.

[2] U74 IS IN TWO PARTS. THE IC IS REFLOWED WITH OTHER PARTS ON PCB. AFTER REFLOW THE BATTERY ITEM (3) IS SNAPPED ONTO THE IC.

[3] ADD A DROP OF RTV (USI 783–412) UNDER Y3.

[4] MOUNT VR4,VR5 & VR6 WITH PUSH PIN , ITEM (4)

[5] LOAD CR18,CR21 – CR24 LEDS WITH CATHODE ON SQUARE PIN NEXT TO SILKSCREENED NUMBERS 0 – 3.

SIDE VIEW OF DIODE IDENTIFYING LEADS.

CATHODE ANODE

[6] MOUNT SUITCASE JUMPERS, ITEM (6) BETWEEN PINS 2–3 ON JP2 AND JP3

[7] MOUNT HEATSINK WITH FAN, ITEMS MP1,MP2, MP4 & MP5 TOGETHER WITH CPU AS SHOWN. CUT FAN WIRES TO RUN LENGTH OF 2 INCHES, CRIMP ENDS WITH MP2. PUT BLACK WIRE IN MP4 POSITION 2 AND YELLOW WIRE IN MP4 POSITION 3.

8. GLUE DOWN U164 TO THE BOARD BEFORE SURFACE MOUNT ASSEMBLY

9. CUT OR BREAK OFF BREAK-AWAY SECTION AFTER ASSEMBLY OF PARTS.

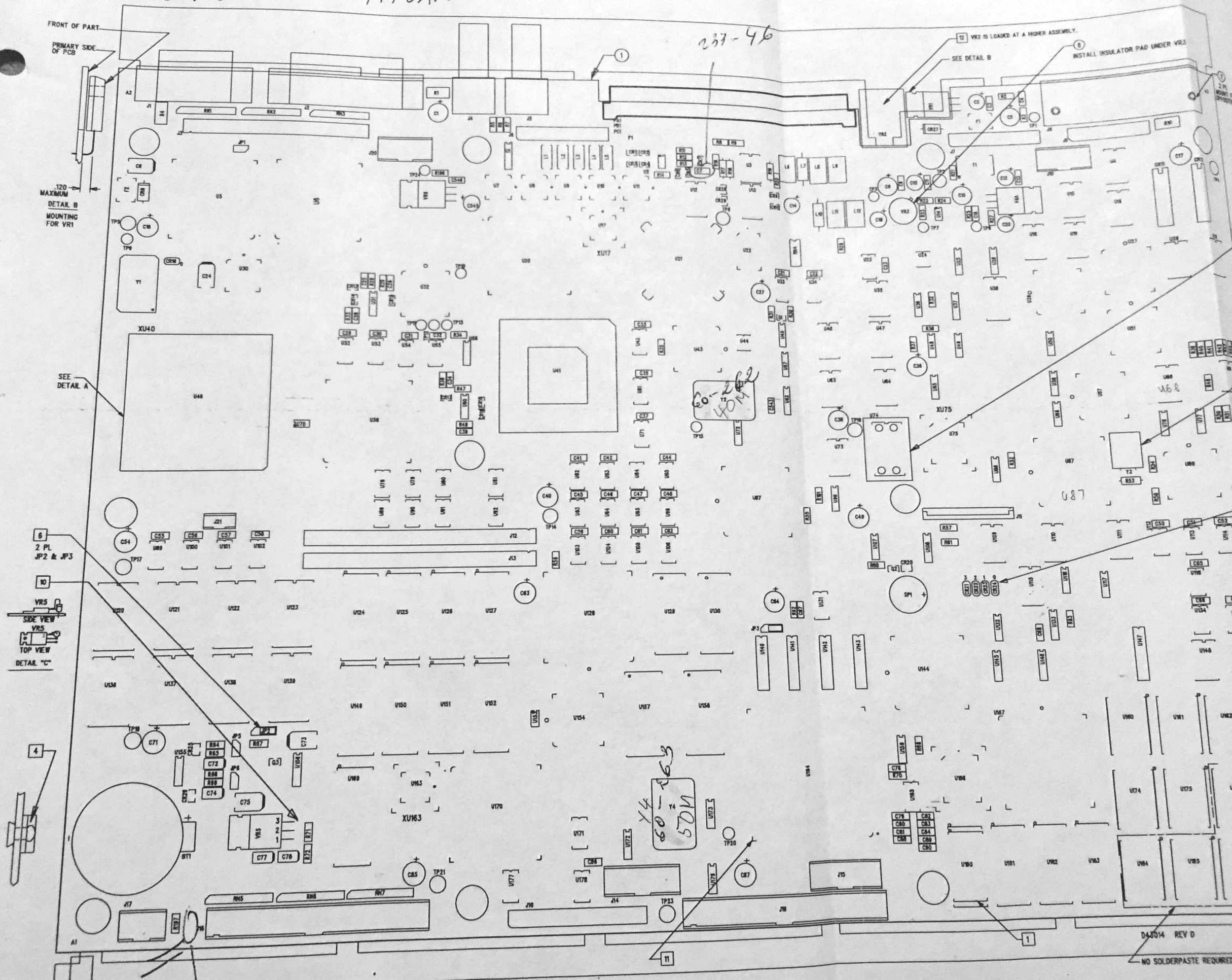
[10] LIFT INPUT PIN (PIN 3) ON VR5. SOLDER CATHODE (STRIPED END) OF A DIODE (P/N 10–83) TO THE LIFTED PIN AND SOLDER THE ANODE LEAD INTO THE BOARD. SEE DETAIL "C"

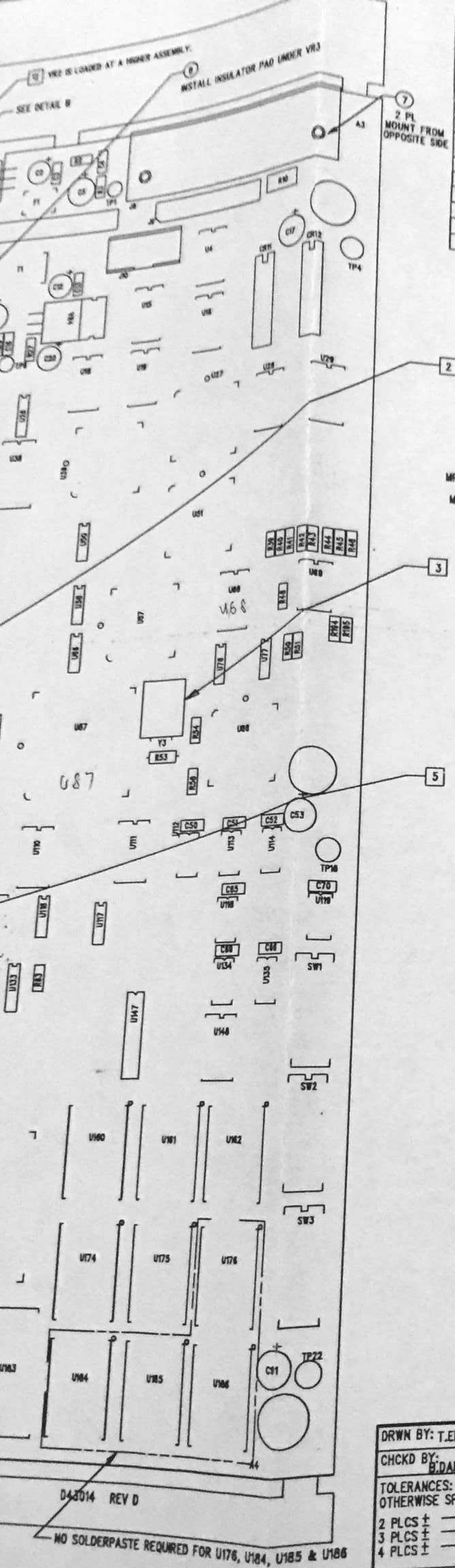
[11] AFTER ASSEMBLY, GLUE DOWN FOUR CORNERS OF U164 TO THE BOARD

PROPRIETARY INFORMATION OF ANRITSU

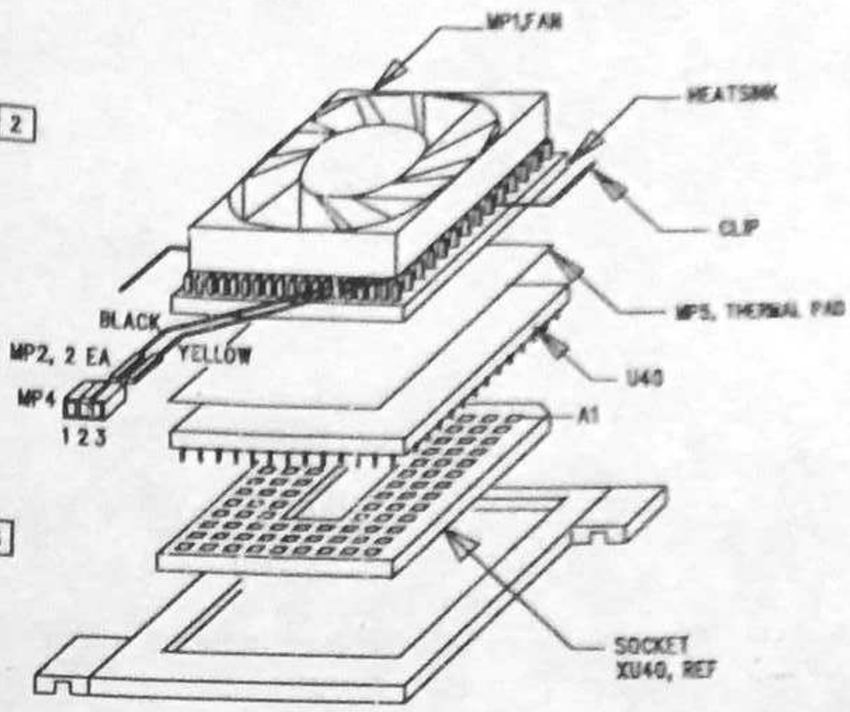
DRWN BY: T.EISELT	DATE 1/98	MATERIAL: N/A	
CHCKD BY: B.DARNELL	DATE 4/98	ANRITSU	
TOLERANCES: UNLESS OTHERWISE SPECIFIED 2 PLCS ± — ANGLES ± — 3 PLCS ± — 4 PLCS ± — SURFACES ✓		TITLE	PC ASSEMBLY PROCESSOR BD MS4600 – A1
		FSCM 20944	DWG NO D43014-3
FINISH: N/A	DO NOT SCALE DWG	SCALE: NONE	UNDER ECN CONTROL 8/98 DATE BY AG M.E.

237-46


FRONT OF PART
PRIMARY SIDE OF PCB
.120 MAXIMUM
DETAIL B
MOUNTING FOR VR1
SEE DETAIL A
SEE DETAIL B
INSTALL INSULATOR PAD UNDER VR3
VR2 IS LOADED AT A HIGHER ASSEMBLY.
2 PL JP2 & JP3
VR5
SIDE VIEW
TOP VIEW
DETAIL "C"
XU40
XU163
XU75
Y1
Y2
Y4
BT1
D42014 REV D
NO SOLDERPASTE REQUIRED



REV	DESCRIPTION OF REVISION	ECN NO	BY	DATE	CHKD
A	PINK RELEASE	———	TE	4/98	BD
B	INCORP PINK	ECN REL	TE	5/98	AG
C	PRODUCT STRUCTURE UPDATE	M1651 M1656	JL	9/98	AG
D	EMI FCC NOISE REDUCTION CAPS ADDED	M1660	TE	11/98	AG
E	SWAP PARTS FOR DETAIL A	M1938	JL	3/99	AG
F	REMOVED REF DES XU164	M1146	JL	5/17/99	AG
H	REMOVED J12 AND J13 FROM NOTE PS 2	M1257	JL	8/5/99	AG
J	REV. U164, U5, U6, U33, U59, U170 & U180–182, U174–U178, U184–186 F/PRNTS	M1524	JL	10/17/98	AG
K	PRODUCT STRUCTURE CHANGED	M1587	JL	2/28/96	AG
L	PRODUCT STRUCTURE CHANGES	M2024	KB	8/28/98	AG
M	SEE REV COMB , NOT IMPLEMENTED	SEE REVISE	KB/KC	8/28/98	AG
N	ADDED NOTE 10	M2112	CO	1/01	GEG
P	PRODUCT STRUCTURE CHANGED	MC2750	CO	1/01	GEG
R	ADDED NOTE 11,12 AND MP5	M2574	TE	8/01	GEG



DETAIL A

HEATSINK KIT MOUNTING DETAIL

7

SURFACE MOUNT ASSEMBLY

NOTES: UNLESS OTHERWISE SPECIFIED

1. NORMALLY LOAD U180 – U183 WITH USI 58–1605. IF LOADING WITH ALTERNATE USI 58–1609, THEN LOAD PIN 1 OF THE IC AT PIN 2 OF THE FOOTPRINT AS SHOWN.

2. U74 IS IN TWO PARTS. THE IC IS REFLOWED WITH OTHER PARTS ON PCB. AFTER REFLOW THE BATTERY ITEM (3) IS SNAPPED ONTO THE IC.

3. ADD A DROP OF RTV (USI 783–412) UNDER Y3.

4. MOUNT VR4,VR5 & VR6 WITH PUSH PIN , ITEM (4)

5. LOAD CR16,CR21 – CR24 LEDS WITH CATHODE ON SQUARE PIN NEXT TO SILKSCREENED NUMBERS 0 – 3.

   SIDE VIEW OF DIODE IDENTIFYING LEADS.

6. MOUNT SUITCASE JUMPERS, ITEM (6) BETWEEN PINS 2–3 ON JP2 AND JP3.

7. MOUNT HEATSINK WITH FAN, ITEMS MP1,MP2, MP4 & MP5 TOGETHER WITH CPU AS SHOWN. CUT FAN WIRES TO RUN LENGTH OF 2 INCHES, CRIMP ENDS WITH MP2. PUT BLACK WIRE IN MP4 POSITION 2 AND YELLOW WIRE IN MP4 POSITION 3.

8. GLUE DOWN U164 TO THE BOARD BEFORE SURFACE MOUNT ASSEMBLY.

9. CUT OR BREAK OFF BREAK–AWAY SECTION AFTER ASSEMBLY OF PARTS.

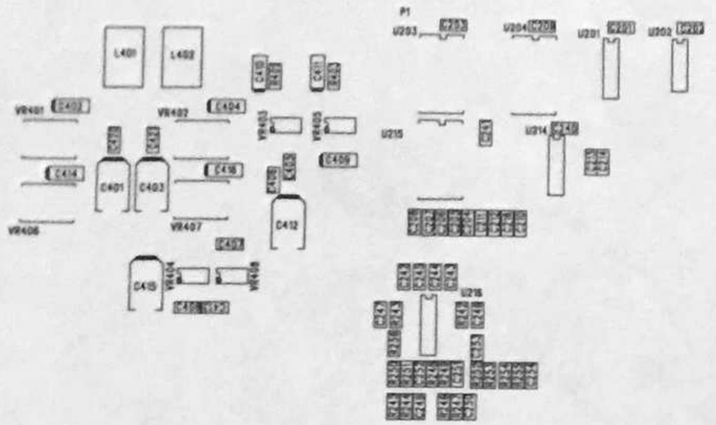
10. LIFT INPUT PIN (PIN 3) ON VR5. SOLDER CATHODE (STRIPED END) OF A DIODE (P/N 10–83) TO THE LIFTED PIN AND SOLDER THE ANODE LEAD INTO THE BOARD. SEE DETAIL "C"

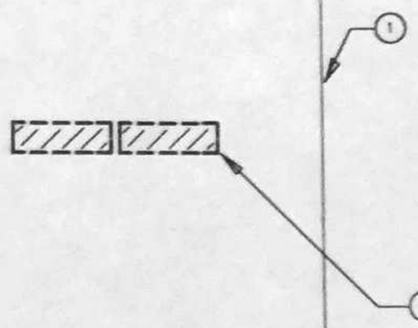
11. AFTER ASSEMBLY, GLUE DOWN FOUR CORNERS OF U164 TO THE BOARD.

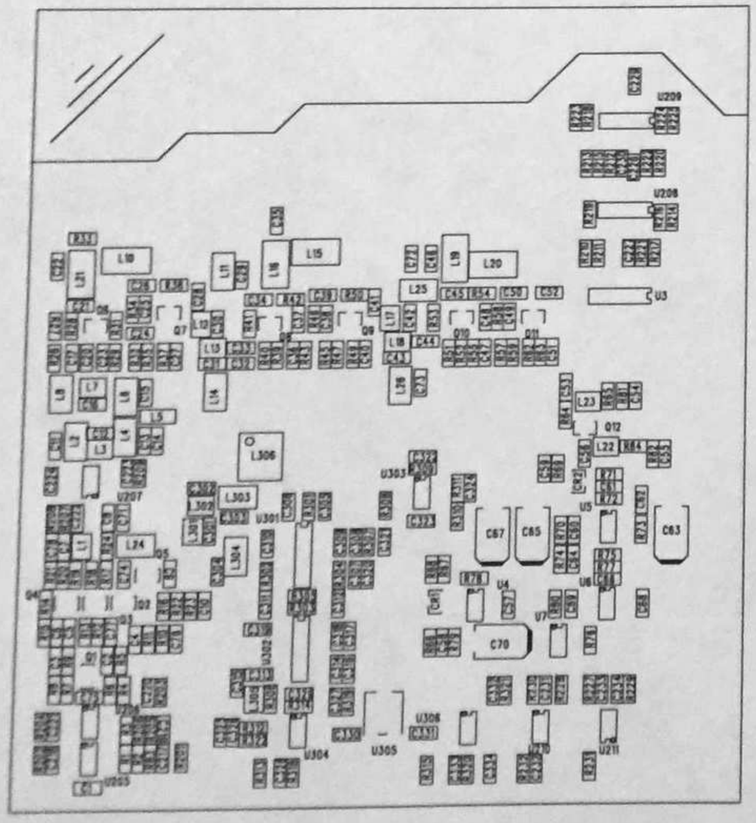
PROPRIETARY INFORMATION OF ANRITSU

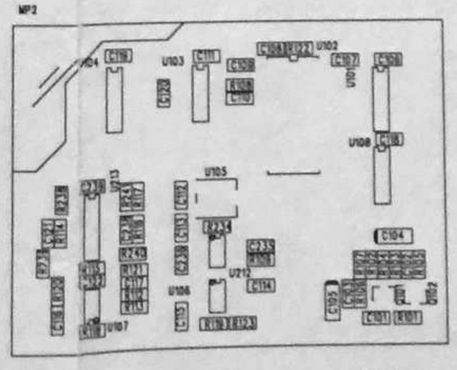
DRWN BY: T.EISELT	DATE 1/98	MATERIAL: N/A	
CHCKD BY: B.DARNELL	DATE 4/98	ANRITSU	
TOLERANCES: UNLESS OTHERWISE SPECIFIED 2 PLCS ± — ANGLES ± — 3 PLCS ± — 4 PLCS ± — SURFACES ✓		TITLE: PC ASSEMBLY PROCESSOR BD MS4600 – A1	
		FSCM 20944 / DWG NO D43014–3	REV R
FINISH: N/A	DO NOT SCALE DWG	SCALE: NONE	UNDER ECN CONTROL 8/98 DATE BY AG M.E. / SHEET 1 OF 2

REV	DESCRIPTION OF REVISION	ECN NO	BY	DATE	CHCKD
A	PINK RELEASE	----	TE	4/98	JG









SURFACE MOUNT ASSEMBLY

NOTES: UNLESS OTHERWISE SPECIFIED

1. CUT OR BREAK OFF BREAK-AWAY SECTION AFTER AFTER ASSEMBLY OF PARTS.
2. LOAD MP1 AND MP2 AFTER SURFACE MOUNT CIRCUIT PARTS.

DRWN BY: T.EISELT	DATE 7/97	MATERIAL: N/A	
CHCKD BY: JG	DATE 4/98	ANRITSU COMPANY	
TOLERANCES: UNLESS OTHERWISE SPECIFIED 2 PLCS ± — ANGLES ± — 3 PLCS ± — 4 PLCS ± — SURFACES ✓		TITLE: PC ASSEMBLY MS4600-A2 OPTIONS BOARD	
		FSCM 20944 DWG NO D43027-3	REV A
FINISH: N/A	DO NOT SCALE DWG	SCALE: NONE UNDER ECN CONTROL ____ BY ____ DATE M.E.	SHEET 1 OF 1

43027 REV A