0811-0100

12/20/73

MODEL 810-D

DIGITAL LOGIC RECORDER

OPERATING AND SERVICE MANUAL

biomation

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OPERATING & SERVICE MANUAL

MODEL 810-D

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SECTION I

General Information

1.1 Certification

Biomation Corporation certifies that this instrument was thoroughly tested and inspected and found to meet its published specifications when it was shipped from the factory.

1.2 Warranty

All Biomation products are warranted against defects in materials and workmanship. This warranty applies for one year from the date of delivery, or, in the case of certain major components listed in the operating manual, for the specified period. We will repair or replace products which prove to be defective during the warranty period. No other warranty is expressed or implied. We are not liable for consequential damages.

1.3 Instrument Description

The 810-D Digital Logic Recorder is a new instrumentation tool for the design and repair of digital logic circuits. Complex logic timing relationships can be conveniently recorded, displayed, and analyzed. Eight channels of digital information can be recorded and monitored at rates up to 10MHz.

The Biomation Model 810-D is designed specifically for analysis of digital logic circuits and signals. The unit can be used on both synchronous and asynchronous signals and can detect random logic pulses as narrow as 10 nanoseconds with the use of the "LATCH" input feature.

The Model 810-D Digital Logic Recorder provides the ability to measure up to eight digital signals against a preset threshold, update the detectors with an internal or external clock, and store 256 such simultaneous decisions for each input signal. This information is then presented

for display on an oscilloscope in an eight trace timing-diagram presentation. Thus, the user can capture unique combinations of digital events for concise and rapid analysis.

The Model 810-D is a bench-type instrument with tilt-up stand and may be rack mounted either as a single unit or two units with the factory option rack mount kit which occupies a 7-inch vertical space in a standard 19" wide rack.

Specifications for the Model 810-D are given in the following paragraphs.

1.4 Specifications

SIGNAL INPUTS

Number 8.

Impedance: 1 MΩ/25pf. Inputs greater than ± 15 V clamped to ± 15 V through 1KΩ.

Threshold: Selectable; -10, -5, -2, -1.3, 0, 1.4, 2, 5, 10 and variable ± 10V. Accuracy of levels is nominally ± 5%.

Max Input Voltage: ± 50V continuous, ± 100V transient.

Input Modes: Selectable; SAMPLE or LATCH.

SAMPLE Mode: Unit stores the detected logic level present at each positive clock transition.

Set Up Time: Zero ns prior to the clock transition.

Hold Time: 15 ns maximum after clock transition typically 10 ns (refer to Figure 1.1).

LATCH Mode: Threshold detector latches in state opposite that stored at previous clock transition in the event that multiple transitions of the threshold occur prior to next clock transition.

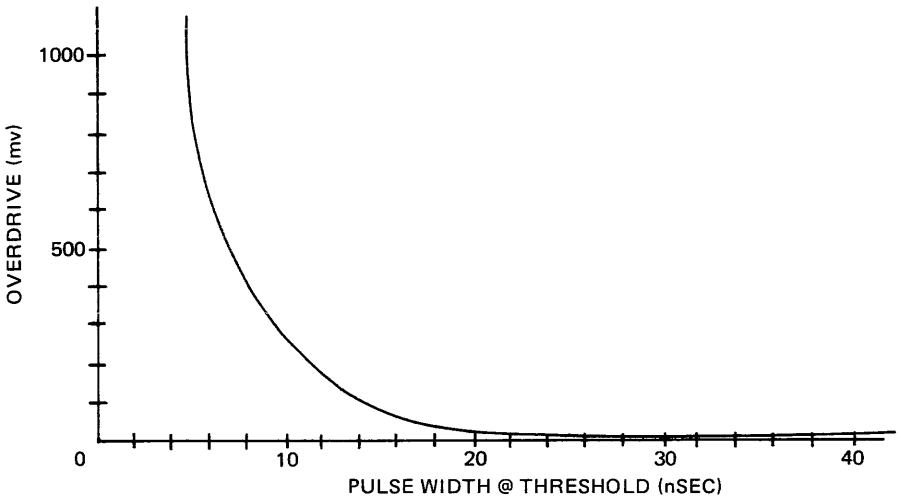
Minimum Pulse width to LATCH: 15 ns with 150 mv overdrive beyond actual threshold, (typically 10 ns, refer to Fig. 1.1).

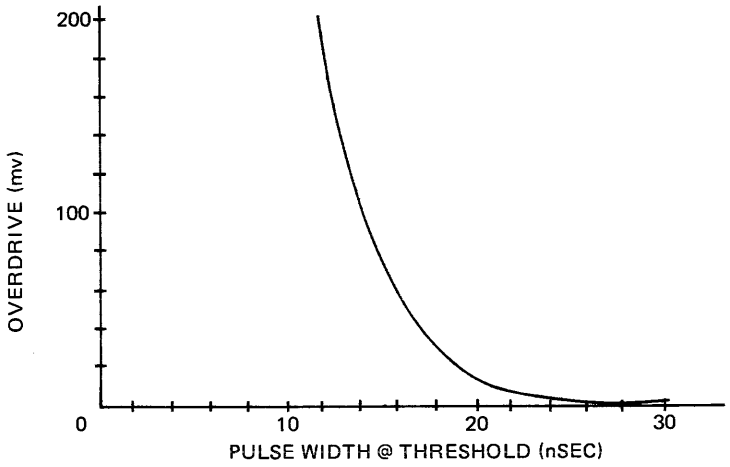
CLOCK

Internal: Selectable .1, .2, .5, 1, 2, 5, 10, 20, 50 microseconds or milliseconds clock intervals.

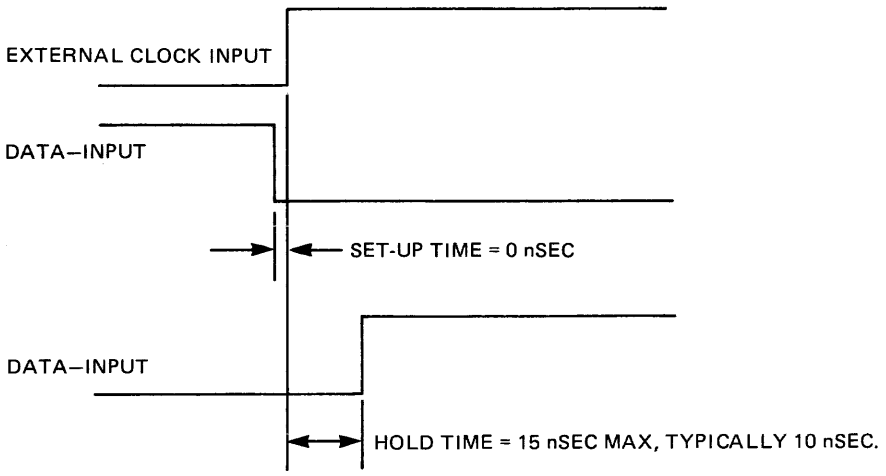
External: Via Front panel BNC connector, continuous rates from 10MHz and to 1kHz and below 1kHz. Clock

LATCH MODE–TYPICAL DATA





SAMPLE MODE–TIMING REQUIREMENTS*



*AS MEASURE WITH 1 nSEC RISE & FALL SIGNALS, CLOCK = 0 to +3 V, DATA = 0 to 2 V & THRESHOLD = 1.4V.

Figure 1.1

pulses to be TTL levels with rise and fall times of less than 100 ns and minimum pulse-width of 50 nS. Clock input impedance is one TTL load. Data is stored on positive clock transition.

TRIGGER

Source: Selectable; Internal or External.

Internal: Via #8 input signal BNC.

External: Via Front panel BNC connector. Input Impedance, 1MΩ/25pf.

Slope: Selectable + or -.

Level: Internal, same as signal threshold; External, adjustable ± 10V.

MEMORY

Size: 8 x 256 bits. *See Note Page 5

Record: Start via Front panel momentary RECORD switch or via rear panel logic pulse input. Stop via trigger detection and after selectable Delay, or via front panel momentary switch.

Delay: Data in 32, 128 or 224 (selectable) clock periods prior to the detected trigger is retained.

DISPLAY OUTPUTS

X Output: Repetitive 1 V p-p ramp waveform, period of 512 µs, origin adjustable ±1.5V.

X Expand: X5, X Ramp Slope increased 5 times. Max amplitude clamped at ± 1.5V.

Y Output: Repetitive 4608 µs long stair step ramp, each step equally spaced in amplitude. Data for each channel modulates each respective step level. Full range nominally 0 to +1V.

Z Output: Nominal zero to +5 V pulse, 8 µsec in duration occuring every 512 µs and synchronized with X ramp.

$\overline{Z}$ Output: Nominal +5V to zero pulse, 8 µsec in duration occuring every 512 µs and synchronized with X ramp.

DIGITAL INTERFACE

Data: Output, 8 bits parallel, TTL levels positive true, word serial asynchronous data transfer under control of Flag and Command signals. Rates 500 kHz down to 2kHz. *See Note Below

Flag: Output of positive TTL transition indicates data word on output lines can be read. Min. width 0.1 µS.

Command: Input of negative TTL transition requests next data word.

Output Request: Input of TTL low or ground stops the display and initiates the digital data output.

Output Enabled: Output occurs within 512 µS after Output Request indicating data output mode is established. Nominal zero to +4 V transition, remains high during output of data and returns low after 256 words are transferred.

Timebase I/O: Record timebase input and output. Used for connecting several 810-D units together for synchronous recording.

Delayed Trigger I/O: Used for connecting several 810-D units together for simultaneous triggering. Provides simultaneous end of record of several units when any one is triggered (after trigger delay).

MISCELLANEOUS

Operating Temp. Range: 0-50C.

Power: 104-126 or 209-253 VAC, approximately, 25 W, 50-400Hz.

Size: Height; 5.25" (13.5 cm.) Width; 8.5"(21.5 cm) Depth 17" (43 cm).

Weight: Approximately 16 lbs (7.3 Kg).

*NOTE: The first data word in the memory (i.e., first bit in each channel) is not specified to contain good data. Therefore, timing measurements with respect to this first word may be invalid. All other data words will be accurate and contiguous relative to the record clock.

SECTION II

Installation

2.1 Introduction

This section contains information on unpacking, inspection, repacking, storage and installation of the Model 810-D.

2.2 Unpacking and Inspection

Inspect instrument for shipping damage as soon as it is unpacked. Check for broken knobs and connectors; inspect cabinet and panel surfaces for dents and scratches. If the instrument is damaged in any way or fails to operate properly, notify the carrier immediately. For assistance of any kind, including help with instruments under warranty, contact your local Biomation representative or Biomation in Cupertino, California, U.S.A.

2.3 Storage and Shipment

To protect valuable electronic equipment during storage or shipment, always use the best packaging methods available. Contract packaging companies in many cities can provide dependable custom packaging on short notice.

2.4 Power Connection

Line Voltage: The Model 810-D may be operated from either 115 or 230 volt (± 10%) power lines. A rear panel line voltage switch permits quick and safe conversion for operation from either voltage.

> CAUTION: Before plugging instrument into AC power line be sure line voltage switch is properly positioned.

Power Cable: The Model 810-D is equipped with a detachable 3-wire power cable. Proceed as follows for installation:

a) Connect line-cord plug (3-socket connector) to AC line jack at rear of instrument.

Power Cable (cont'd)

b) Connect plug (2-blade with round grounding pin) to 3-wire (grounded) power outlet. Exposed portions of instrument are grounded through the round pin on the plug for safety. When only 2-blade outlet is available, use connector adapter, then connect short wire from side of adapter to ground.

2.5 Preparation for Use

The Model 810-D is not a "self-contained" instrument in that it must be interfaced with other types of instrumentation in order for the data to be visible or analyzed. The following sections of this manual cover operation, set ups and interface requirements.

2.6 Initial Warm-Up

Although the Model 810-D is a solid state instrument, a brief warm-up period of approximately 5 minutes is required for the input amplifiers and comparators to reach thermal stabilization. This warm-up period is recommended for both the Model 810-D and its associated output device.

SECTION III

Principle of Operation

3.1 Basic Functional Description

The Model 810-D offers convenient and useful capabilities for the analysis of digital signals. The unit is an eight channel solid state digital recorder which operates at a maximum bit rate of 80 megabits/sec. Figure 3.1 presents a block diagram of the 810-D.

The memory in the 810-D stores a 256 bit record for each of the eight channels. Operation of the RECORD switch causes the unit to monitor and record the status of the eight input lines at the selected clock rate. When a triggering event occurs, recording is terminated after a delay period. Selection of the delay determines the position of the "display window" before and after the triggering event. In this way, eight points in a digital circuit can be continuously monitored, waiting for a specific fault or logic event. When the event occurs, a contiguous record of events before and after the trigger is recorded for display and analysis.

3.11 Input Threshold

The definition of a stored data signal as a binary "1" or "0" is determined by a switch selected logic threshold level. A selection of nine threshold voltages are provided, including a +1.4 Volt "TTL" threshold level. In addition, an adjustable level position can be selected which can be set to any level between $\pm$ 10 Volts.

3.12 Sample Mode

In the "SAMPLE" mode of operation, the input levels are strobed into the memory as "1" or "0" based on the signal level with respect to the selected threshold at the time of the rising edge of the clock.

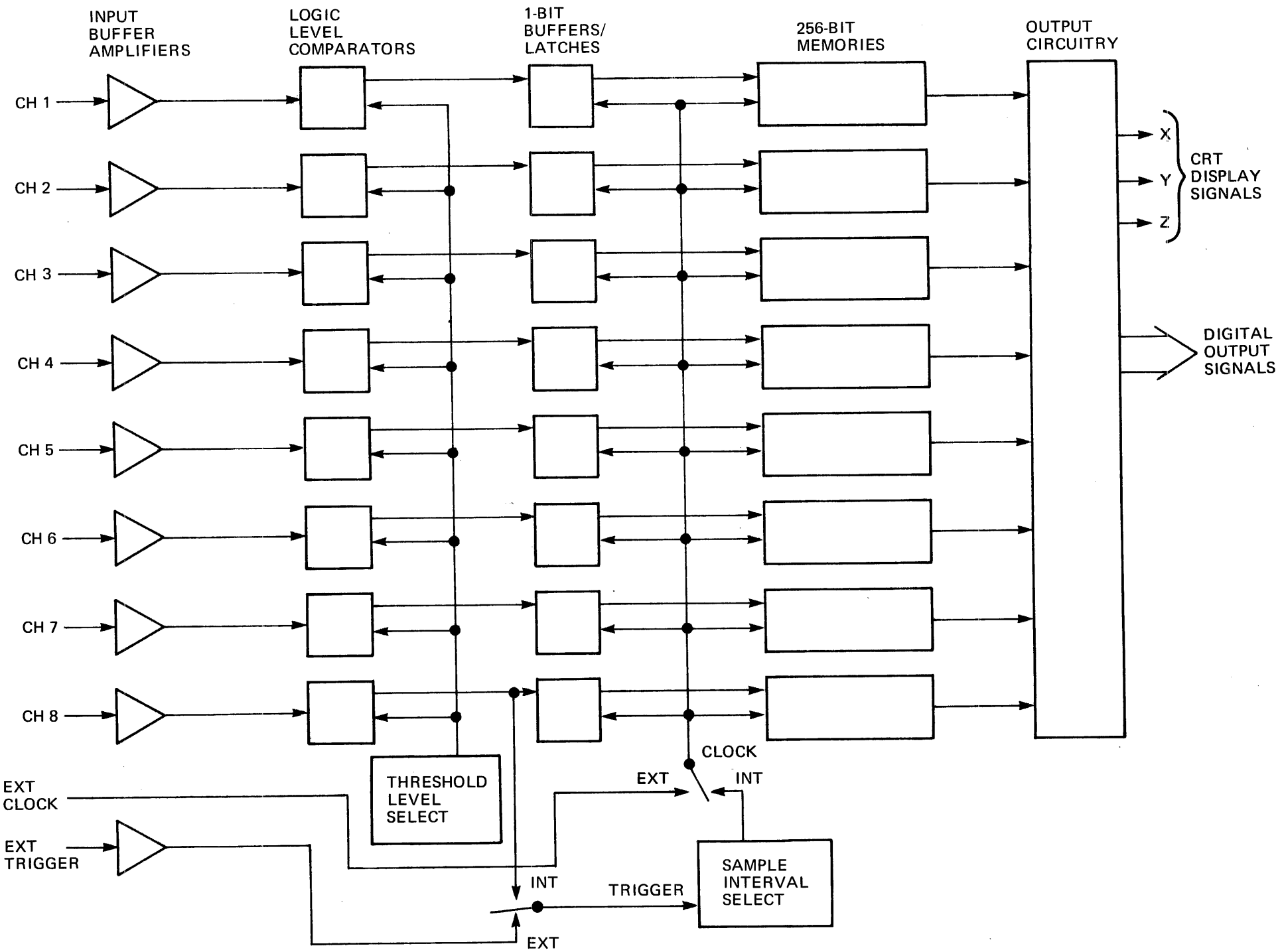

INPUT BUFFER AMPLIFIERS
LOGIC LEVEL COMPARATORS
1-BIT BUFFERS/ LATCHES
256-BIT MEMORIES
OUTPUT CIRCUITRY
CH 1
CH 2
CH 3
CH 4
CH 5
CH 6
CH 7
CH 8
X
Y
Z
CRT DISPLAY SIGNALS
DIGITAL OUTPUT SIGNALS
CLOCK
EXT
INT
THRESHOLD LEVEL SELECT
EXT CLOCK
EXT TRIGGER
INT
TRIGGER
EXT
SAMPLE INTERVAL SELECT

Figure 3.1

3.13 Latch Mode

The "LATCH" mode of recording permits narrow spikes to be recorded. Any spike (positive or negative) with sufficient amplitude that is wider than 15 nS causes an input latch to set. This changes the state of the next bit to be written in memory. In this way, narrow spikes or "glitches" occuring at random times between sample clock transitions can be captured.

3.14 Signal Inputs

The eight signal inputs plus the external trigger inputs are buffered to provide 1 MΩ//25pf input impedances. This permits the use of common passive scope probes for connections to the circuit under analysis.

3.15 Record Rates

Internal clock rates are selectable from 20 samples/second up to 10 Megasamples/second in 1-2-5 steps. Or, the clock of the device under test may be used to provide synchronous recording, a distinct advantage when synchronous logic is under test.

3.16 Record Operation

A record sweep proceeds as follows: pressing the record switch starts the unit recording; i.e., continuously shifting new data into the shift register memories. On trigger detection (External, Manual, or Internal from Channel 8 input), the unit will begin a preset count as determined by the delay control and then stop recording.

If a delay of 1/8 is selected, the unit will count down for 224 clock periods after trigger and stop recording. If a delay of 1/2 is selected, the time out count is 128 clock periods. Similarly, the selection of the 7/8 delay will cause 7/8 of the memory length to contain prior trigger data by counting for 32 clock periods after the detected trigger point.

3.17 Display Output

Once Record is halted, the unit automatically goes into a display mode, where the memory is continuously circulated and the contents are repetitively output in analog form for display on a CRT or oscilloscope.

The display presentation is an eight signal timing diagram on the CRT. With no horizontal expansion, 252 bits of information are displayed on the CRT for each signal (about 25 per div). Using the built-in horizontal expansion switch, the display is expanded by a factor of 5. Therefore, each division of the CRT in the expand mode contains approximately 5 bits of data on each signal.

3.2 Recording Considerations

As the Model 810-D can record as a function of either the internal clock or an external clock, note must be taken of some basic differences in these two methods.

When the internal clock is used for recording no particular phase relationship will exist between this clock and any synchronous information rate in the signals being recorded. Therefore, a "beat" frequency can exist between these two basic rates. If the 810-D internal clock is 10 times or more higher in frequency that the "signal" rate, very little effect will be noted in the recorded data. For higher "signal" rates (with respect to the record clock) a "beat rate" effect can be seen by varying widths in the recorded "pulses" and even periodic "dropped" bits when these rates approach the limiting ratio of two to one.

When the synchronous clock used for the generation of the input signals to the 810-D is used as the record clock in the 810-D, no phase errors exist and no beat frequencies will be evident; i.e., the beat note is zero frequency. In this case, signals with information rates up to and including 1/2 the clock frequency can be recorded, without distortion. This is called synchronous recording.

SECTION IV

Operation

4.1 Introduction

This section identifies and describes front panel controls, rear panel connections and typical operating procedures. Included are complete descriptions of front panel controls and their effective ranges, location and proper use of rear panel connectors, set up procedures prior to using the Model 810-D, and step by step operating procedures for various modes of operation. A thorough understanding of this section is essential to the successful use of the instrument.

4.2 Front Panel Controls and Connectors

4.21 Control Clusters

The controls of the Model 810-D may be divided into five groups. Each group contains separate controls with related functions. Figure 4.1 is a front panel photograph of the 810-D. The five control groups are as follows:

Mode and Threshold
Display
Clock
Record and Trigger
General

4.22 Mode and Threshold

(1) SAMPLE/LATCH. In SAMPLE position, the unit compares input levels with the preselected threshold level and stores a high or low, as appropriate, on the positive transition of the clock. Thus, the data stored in memory reflects the input states at the clock transition.

In the LATCH mode, the unit stores as above for single threshold transitions in a clock period, but also "latches" to a state opposite that last stored when multiple transitions occur in a clock period. For instance, a single narrow pulse between clock transition would not effect the memory contents in SAMPLE mode but would effect the stored data in LATCH mode. This "glitch" catching feature words for either positive or negative pulses by "stretching" the

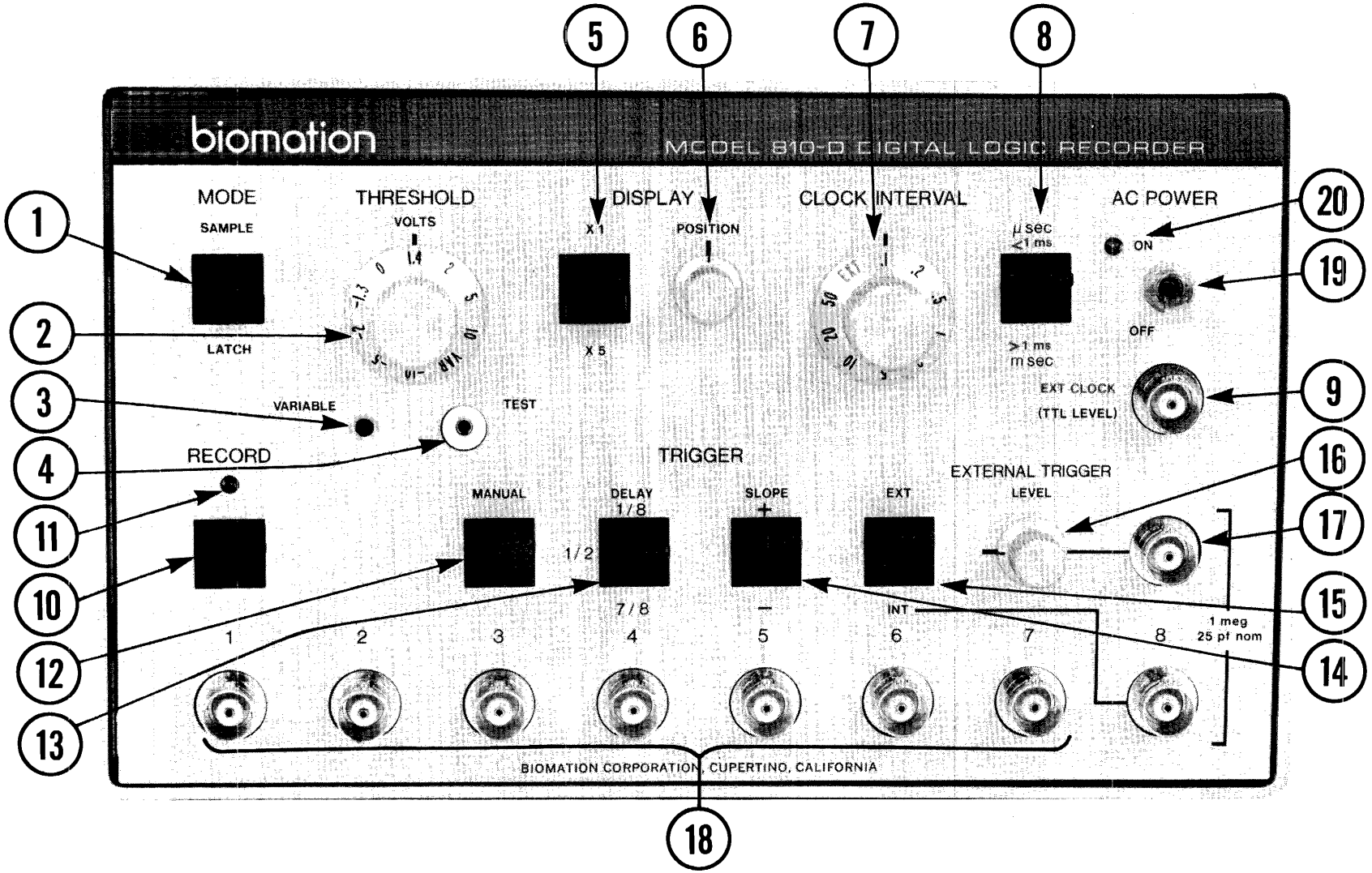


Figure 4.1 810-D Front Panel

random pulse to one full data period. The 810-D will typically "latch" on pulses as narrow as 10 nS.

(2) THRESHOLD, VOLTS.

Provides switch selection of -10, -5, -2, -1.3, 0, 1.4, 2, 5, 10 volts threshold, as well as variable (VAR). In the VAR position, the user may adjust a vernier threshold level, using the potentiometer marked VARIABLE (3) and the test point marked TEST (4).

When the input level is more positive than the threshold, a logic "one" (high) is stored in memory; when the input is less positive, a logic "zero" (low) is stored.

(3), (4) VARIABLE TEST.

To set a vernier threshold, set THRESHOLD, VOLTS (2), to VAR. Adjust VARIABLE (3) with a screwdriver for the desired threshold as measured at TEST (4). The selected threshold voltage for any of the positions on the THRESHOLD selector switch can be checked at the TEST point (4). The output impedance at this test point is 10K Ω. The accuracy of the threshold voltages are nominally ± 5% of the indicated value.

4.23 Display

Note: These controls give the following action only when the 810-D is providing X axis drive to the CRT.

(5) X1/X5. This switch provides a X5 horizontal expansion. Without expansion, 250 clock periods are displayed, or 25 clock periods per division, assuming 10 display divisions. With X5 expansion, 5 clock periods per division are displayed.

(6) POSITION.

This control sets the horizontal position on the CRT display with X1 expansion selected and gives the ability to place any 50 clock periods of data cross the full CRT display width with X5 expansion selected.

4.24 Clock

(7) CLOCK INTERVAL.

Selects, in conjunction with the μSEC/mSEC switch, the choice of internal clock intervals of 0.1, 0.2, 0.5, 1, 2, 5, 10, 20, 50 μSEC/m SEC or EXT. clock input.

(8) μSEC/mSEC.

Provides multiplication factor for switch (7) (when EXT clock interval is selected, this switch must be set per the red legends (<1ms, >1ms) appropriately for the clock interval being used.

(9) EXT CLOCK (TTL LEVEL).

This BNC connector allows input of an external clock when switch (7) is in EXT position. For clock intervals from 1ms to the minimum interval of 0.1μS switch (8) must be in the <1ms position; for intervals greater than 1ms switch (8) must be in the >1ms position.

This input accepts TTL levels, and the input load is one TTL gate. The unit samples on the rising edge of the clock.

4.25 Record and Trigger

(10) RECORD, (11) RECORD Indicator

Pressing this momentary toggle switch starts the unit sampling the inputs and clocking data into memory. The red LED (11) illuminates to indicate Recording in process. When recording at slower rates, hold this switch down to inhibit trigger. This will ensure that the memory is cleared of old data before any new data is loaded.

(12) MANUAL.

This momentary switch provides a manual trigger. Pressing it stops the Record mode and a display is presented.

(13) DELAY.

This three position switch allows three delay selections as follows:

1/8: 32 clock periods prior to trigger are retained in memory.

1/2: 128 clock periods are retained.

7/8: 224 clock periods are retained.

(14) SLOPE, ±.

Allows selection of triggering on the positive (+) or negative (-) going transition.

(15) EXT/INT.

Allows selection of internal or external trigger source.

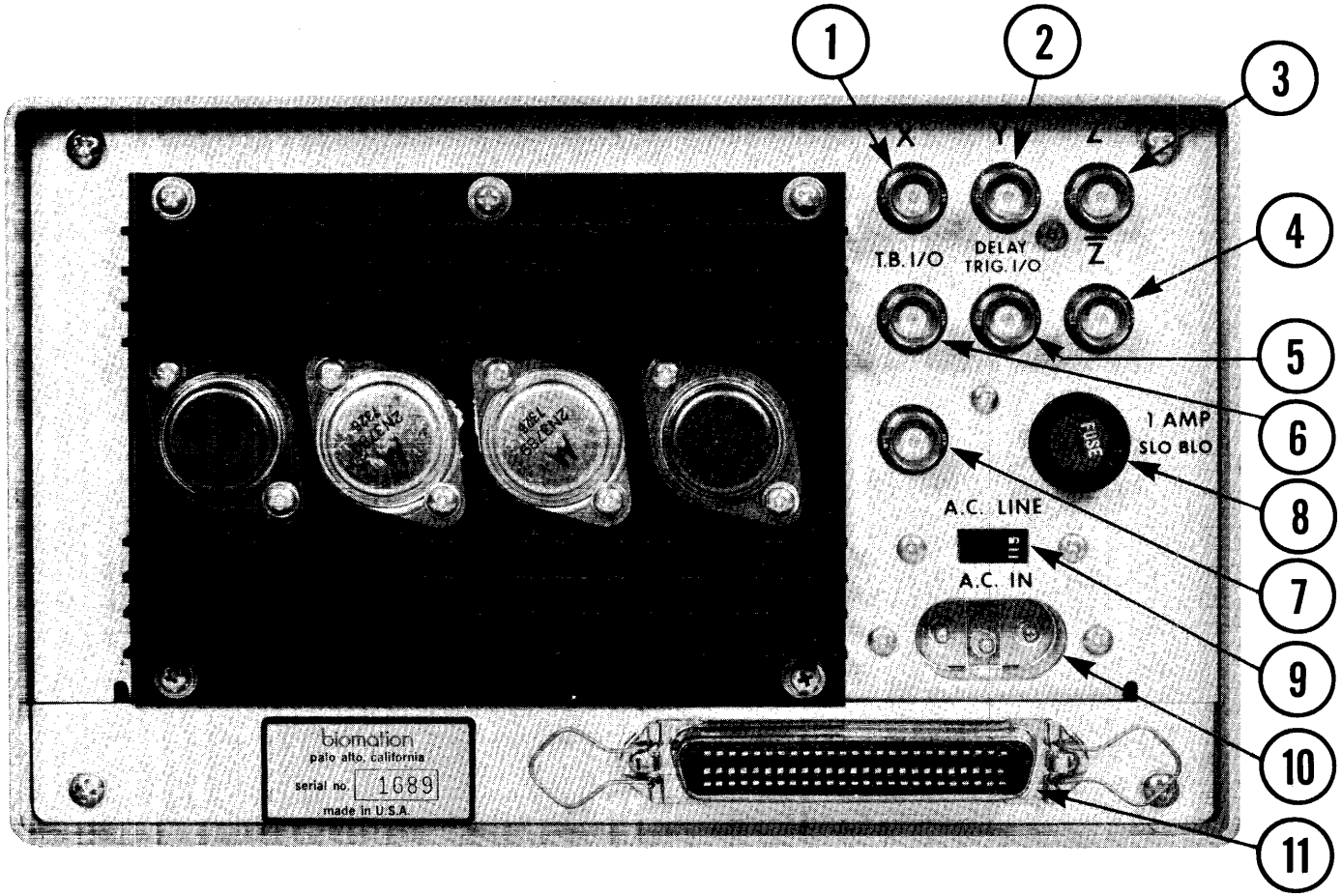


Figure 4.2 810-D Rear Panel

On INT, the unit triggers on a transition (+ or - as selected) of the signal on channel 8 that exceeds the threshold level selected by switch (2).

On EXT, the unit will be triggered by the transition of a signal applied to connector (17).

(16) EXTERNAL TRIGGER, LEVEL.

Allows adjustment of external trigger signal threshold between ± 10 V.

(17) BNC Connector.

External trigger input connector, input impedance of 1MΩ// 25pf.

4.26 General

(18) INPUTS (8 each).

Any or all inputs may be used at one time. Input impedance is 1MΩ/25pf.

(19) AC POWER.

When switch is on, LED (20) illuminates.

4.3 Rear Panel Connectors. (See Figure 4.2).

(1) X Output.

Repetitive 1V pp ramp, waveform, with a period of 512 μS Ramp is 504 μS long with a "retrace" of 8msec. Origin is adjustable ± 1.5V. Using DISPLAY expand switch (5), the slope of the ramp is increased 5 times. The maximum amplitude of the ramp is clamped at ± 1.5V.

(2) Y Output.

Repetitive 4608 μS long stair-step ramp; each step equally spaced in amplitude; total amplitude 1V p-p. Data from each channel modulates each respective step level. A CRT display is swept nine times per Y "ramp." The Y "ramp" step for channel 8 is swept twice by the X signal and each other channel step swept once. The eighth data step is repeated to facilitate operation with a triggered sweep (using the Z (3) or $\overline{Z}$ (4) signal of an oscilloscope. The number of data bits viewed per channel is 252, counting from the first bit in each channel.

(3) Z Output.

Nominal 0 to +5V pulse, 8 µS in duration and occurs every 512 µS. This pulse is synchronized with X and Y outputs.

(4) $\overline{Z}$ Output.

Nominal +5 to OV pulse, the negation of the Z pulse, above.

(5) DELAY TRIG I/O.

Used to connect several 810-D units together for simultaneous triggering. Provides simultaneous end of record of several units when any one is triggered (after trigger delay).

(6) Timebase I/O.

Record timebase input and output. Used to connect several 810-D units together for synchronous recording. To operate select the desired clock interval on one unit, and set the CLOCK INTERVAL switch on the other units to EXT. To use an external clock, set all interconnected units to EXT, and input the external clock to the front panel EXT CLOCK connector (9) of one unit. Ensure that the <1ms/>1ms switch (8) is in the proper position. See Section 4.2.

(7) Spare BNC Connector

(8) Fuse. 1 AMP SLO BLO for 115V operation, 0.5 amp for 230V operation.

(9) AC LINE. Switch for selection of operating line voltage, 115V or 230V. Change fuse to 0.5 amp Slo Blo for 230V operation.

(10) AC IN. Power line connection, 25W input. Use mating power cord, Belden 17358.

(11) Digital Interface Connector J19. For the description of the signals on this connector, refer to Section V, Output Interface.

4.4 Set Up Procedure

4.41 Initial Set Up

This section describes the connection of a Model 810-D with a CRT display or oscilloscope and the steps to record and display a known signal.

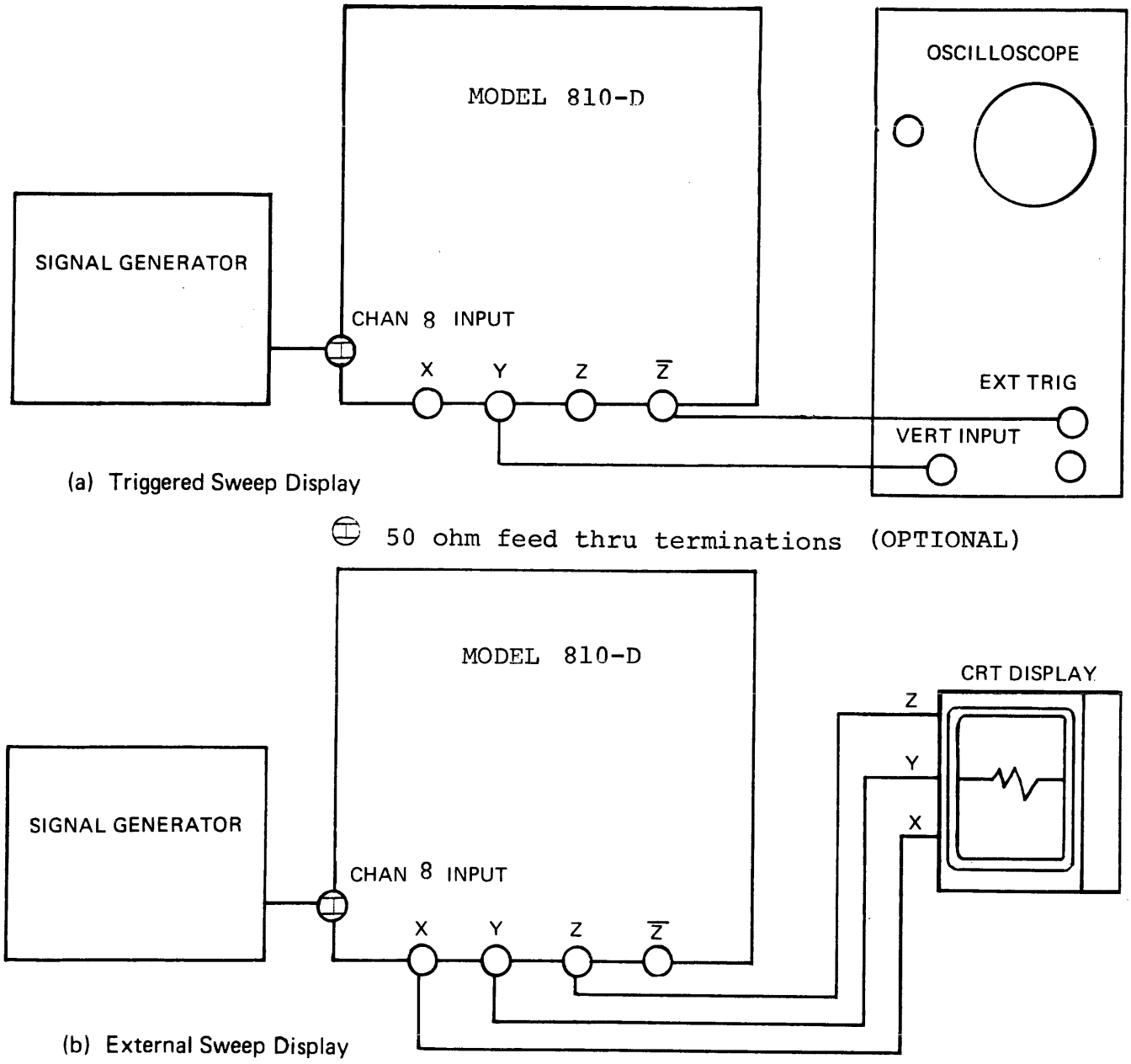


Figure 4.3 Display Interconnections

Before connecting the unit to line power, check the voltage selector switch on the rear panel to ensure that it is set to the proper line voltage and be sure that the correct size fuse (as printed on the rear panel) is installed.

Connect the Model 810-D to a pulse generator with a manual single pulse capability and CRT display as shown in Figure 4.3a or 4.3b. Depending upon the particular CRT or oscilloscope being used, it may be necessary to use the $\overline{Z}$ output of the 810-D for the retrace blanking signal.

CAUTION - Some older "tube type" oscilloscopes have a high voltage on their Z axis inputs. THIS COULD DAMAGE THE Z or $\overline{Z}$ OUTPUT OF THE 810-D. PLEASE CHECK BEFORE CONNECTING THE UNITS TOGETHER.

Set the units (where appropriate) as follows:

Vertical sensitivity	0.1V/div. uncalibrated, DC coupled
Vertical position	Bottom of display
Horizontal sweep	50 µS/div., (Fig. 4.3a)
Horizontal sensitivity	0.1V/div., DC coupled (Fig. 4.3b)
Trigger input	-, DC coupled, external (Fig. 4.3a)
Pulse Generator	Single manual pulse, 2.5 µS wide, 0 to +3V pulses

Set the Model 810-D as follows:

MODE:	Sample
THRESHOLD:	1.4 volts
DISPLAY:	X1
CLOCK INTERVAL:	0.1µS
TRIGGER	
DELAY:	1/8
SLOPE:	Positive
SOURCE:	Internal

When initially powering up the unit, always press RECORD and then TRIGGER, MANUAL to reset circuitry. Center the eight traces on the CRT using the vertical and horizontal controls on the scope or display and the horizontal position control on the 810-D.

4.5 Operating Procedures

In this section two modes of operation will be discussed and illustrated. A pulse generator capable of generating a single pulse upon manual command is required.

Set the generator to give single manually initiated pulses of approximately 2.5 μS wide, and 0 to +3V amplitude.

4.51 Sample Mode

Press RECORD and pulse the generator. Figure 4.4 illustrates the display obtained. Channels 1 through 7 will display a low level, while Channel 8 displays the pulse. The pulse will occupy one division on the CRT, and be comprised of 25 clock intervals. Thirty-two clock intervals will have been recorded before the positive transition of the pulse.

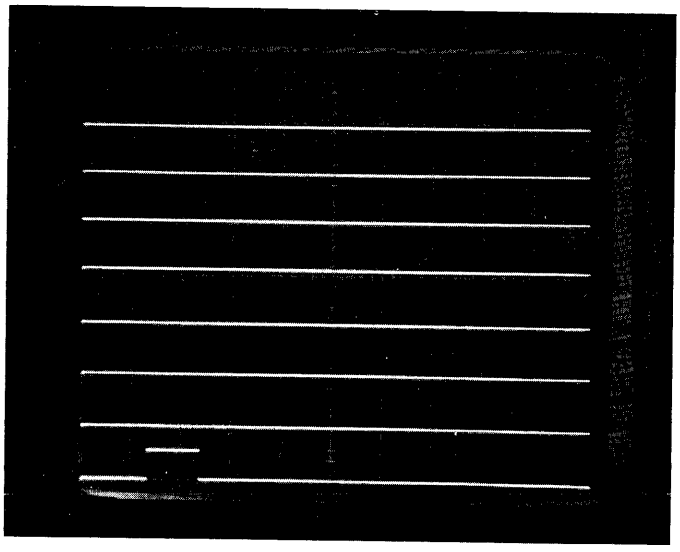


Figure 4.4

4.52 Latch Mode

Set CLOCK INTERVAL to 50 µS. In the SAMPLE MODE, press RECORD and pulse the generator while observing the CRT. Repeat this routine several times. Note that although the unit triggers each time on the pulse it seldom records the pulse. In the SAMPLE MODE, the unit stores the input levels present at the clock edge. The clock interval is approximately 20 times as long as the pulse, so the unit can only see the pulse when the clock transition is coincident with it, an unlikely occurence with 2.5 µS input pulses and 50 µS clock intervals.

Select MODE, LATCH. Repeat pressing the RECORD switch and pulsing the generator. Observe that the unit captures the pulse each time and represents it with one clock interval, or 50 µS. This feature is particularly useful for detecting narrow random noise pulses or "glitches".

This mode operates in the same manner independent of the chosen clock interval. A glitch typically as short as 10 ns may be detected and displayed at any clock interval.

4.53 Manual Trigger

To verify operation of each channel, change the pulse generator to a repetitive output, approximately 5KHz rate, with the same pulse as before. Starting with channel 1, connect the generator to the input BNC. Press the RECORD switch, and then the TRIGGER MANUAL, switch. Several pulses of one clock interval will be displayed on the CRT, on the top trace. Repeat the above procedure for each channel, 1 through 7. The trace corresponding to that channel will display several pulses in turn.

SECTION V

Output Interface

5.1 Introduction

The output interface of the Model 810-D includes two methods of analog output: one, using a CRT in an X-Y mode, and two, using an oscilloscope in the triggered mode. These methods are explained in Section 4.41.

The instrument also offers a digital output of data. This data is output in an 8 bit parallel format, the bits representing a simultaneous data entry for all channels. Two hundred fifty six such 8-bit words are available through the digital output mode.

5.2 Digital Output

All inputs and outputs at the 50 pin rear panel connector J19 are positive logic, TTL signals. Direct access to control gates is available at J19. This connector provides the physical interface for digital data output. The connector is an Amphenol Micro-Ribbon 57-40500. The mating connector is an Amphenol part number 57-30500.

The pin assignments, and signal descriptions for the digital interface are listed in the following table:

Pin #	Signal Name	Description
1	Detected Ch. 1	These outputs are the detected input signals after passing through the Input Buffer, Descriminator, and Data Latch circuits, and a buffer gate. No "sense" inversion takes place. This data requires no clocking.
2	Detected Ch. 2	
3	Detected Ch. 3	
4	Detected Ch. 4	
5	Detected Ch. 5	
6	Detected Ch. 6	
7	Detected Ch. 7	
8	Detected Ch. 8	

(OUTPUTS)

Pin #	Signal Name	Description
9 10 13 16 11 12 14 15	Data Output 1 Data Output 2 Data Output 3 Data Output 4 Data Output 5 Data Output 6 Data Output 7 Data Output 8 (OUTPUTS)	These lines supply data stored in memory when the digital output procedure, outlined in Section 5.21 or 5.22, below, is followed. Buffering is provided.
19	Output Request (INPUT)	Line is normally pulled high. To initiate output, pull low until Output Enable goes high.
21	Output Enable (OUTPUT)	Goes high within 512 µS after Output Request providing the unit is not recording and indicates that the first data word is ready to be read.
18	Command (INPUT)	Normally high. Changing to a low level causes unit to "fetch" next data word. The high to low transition time must be 200 nS or less.
17	Flag (OUTPUT)	Goes high when next data word is available, approximately 100 nS after command goes low.
20	Record (OUTPUT)	High when unit is recording; low otherwise.
45	Trigger (INPUT)	Logic Level Trigger input.
23	+5V Power (OUTPUT)	May be used to power delay counters, combinational trigger circuits, etc. Available current is approximately 500ma.

Pin #	Signal Name	Description
22	Remote Arm (INPUT)	Line is normally held high and brought low to initiate recording process.
27-44	Ground	Power and logic return.

5.21 Digital Output Sequence - After Display

Immediately after recording, the 810-D will enter the display mode, repetitively cycling the memory and producing the X, Y and Z display signals. In this condition, the Record (pin 20) and Output Enable (pin 21) output signals will be low. The Output Request (pin 19) input will be pulled high.

When a low is input to the Output Request, the Output Enable will go high within 512 µS depending on the instantaneous position of the memory in its display cycle. Flag (pin 17) will go high at the same time. Output Request should be held low until Output Enable goes high. Output Request should then be returned high. It is recommended that the Request and Enable signals be externally interlocked for proper operation. When Flag goes high, the first data word in memory may be read on the data output pins 9 through 16.

The next, and subsequent data words will be presented on the data output lines after each Command (pin 18) input negative transition. For proper data output the interval between Command inputs should be from 2 µS to 500 µS, giving asynchronous data word rates of 500KHz through 2KHz.

CAUTION - Once digital output is established (Output Enabled high), the interval between command transitions must be 500 µS or less. Longer intervals may cause permanent loss of the stored data in the 810-D.

The negative transition time of the Command signal must be 200 nS or less. When the command signal goes low, the Flag will go low for 100 nS and then return high again, which indicates that the next data word is settled on the data output lines and can be used. After 256 commands the unit will automatically revert to the display mode. If the Output Request line is held low, the unit will return to output mode after one display cycle.

NOTE: It is essential that at least 256 Command signals are generated. Otherwise, the unit will remain in the Output mode until Record is initiated.

5.22 Digital Output Sequence - After Record

If it is desired to output digital data immediately after Record, proceed as follows: Monitor Record (pin 20). When Record goes high, issue a low to Output Request (pin 19). As soon as Record is complete (Record goes low) Output Enable (pin 21) and Flag (pin 17) will go high, indicating the first data word can be read. When this occurs, proceed with Command Flag operation as described above. The unit will automatically revert to display mode after the 256 Command/Flag sequences necessary to complete one data output cycle are completed.

SECTION VI

CALIBRATION PROCEDURES

6.1 Calibration of Display Output

Adjustments are provided to calibrate the X and Y output to a specific display unit or oscilloscope. In addition, an adjustment is provided for the height of the "1-0" bit. Table 1 gives the location of these adjustments and their nominal P-P output values.

Function	Location	Nominal Level P-P
X-out	R181 (next to ME5)	1V
Y-out	R180	0.8V
Bit Height	R174	0.06V

6.2 Recalibration of Internal Circuits

There are no adjustable components in the 810-D except those listed in Section 6.1 above. No further calibration is required.

SECTION VII

Technical Description

7.1 General Description

The Model 810-D, Digital Logic Recorder, is a very simple instrument. It simultaneously measures whether the input signals are above or below the selected threshold voltage and writes a corresponding 1 or 0 in a semi-conductor memory. The memory used is of the shift register configuration, such that new data is put into the input end of the memory, shifted throughout the length of the memory and discarded at the output end. The recording process may continue for an extended period of time. However, the memory is a finite length (256 data points), so that at any point in time, only the previous 256 data points are remembered.

When data storage is halted by means of a electrical or manual trigger, the data contents of the memory can then be used either visually or by means of the digital output. When the Model 810-D receives a trigger instructing it to stop data storage, a delay process is started. If a delay of 128 (½) data points is selected, then new data will continue to be inserted into the memory for 128 clock intervals. Since the memory contains 256 data points, the result will be that 128 points of information prior to the trigger plus 128 points after the trigger will be stored in the memory for use by the operator. This feature allows the operator to look both forward and backward in time relative to his trigger signal.

When data storage ceases, the instrument normally goes into what is called the "display mode" of operation. In this mode, the contents of the memory are continuously recirculated and made available at the output port of the memory. With the memory outputs being updated at a high rate, it is relatively easy to achieve a non-flickering CRT display of the memory contents. By this technique, an X-Y CRT display unit or any conventional oscilloscope can be used to display the timing relationships between logic

signals on the 8 input lines. The logic waveforms displayed will be identical to those shown by component manufacturers or in the timing diagram provided for a system if the operator of the 810-D has chosen the clock interval sufficiently high.

An alternative to the display mode is the digital output mode. This mode allows the 810-D to be used with a suitable interface to output the stored information to a computer system. Once the computer via its interface requests output data from the 810-D via the interface to the computer, the data is supplied one word at a time sequentially, beginning with the first word in memory through the final word in memory. Each word is available at the output connector (8 bits in parallel) with a Flag signal indicating to the computer that the data is valid and ready to be clocked into the computer. The computer must monitor and count the number of data words removed from the 810-D, and all 256 words must be removed. There are minor clocking restrictions which must not be violated if valid data is to be obtained. These restrictions are covered in other parts of this instruction manual.

7.2 Circuit Details

This section will deal with the individual circuits of the 810-D. Section 7.3 will tie these circuits together as they function in various modes. In using this section, reference will be made to the 810-D Schematic Diagrams (0811-0002). This Schematic is drawn on four individual sheets. Reference will be made at the beginning of each new circuit description to indicate the reference sheet. Any attempt to discuss individual circuits of an instrument must lead to some frustration on the part of the reader. However, it is felt that if the individual circuit groupings can be understood, a better feeling of the overall instrument design and concept will be obtained. Ultimately, such an understanding is necessary if one is to satisfactorily service and maintain an instrument over an extended period of time.

7.21 Input Circuit (Schematic Part 1, Page 56)

Referring to the left side of the schematic, one will note that the eight signal inputs, plus the trigger input, have identical circuits. Each has a X1 buffer amplifier. Each has a passive attenuator following the buffer amplifier, which attenuates the signal by a factor of 3. The attenuated signal from each goes to the non-inverting input of a threshold descriminator. The only difference between these nine signals is that the threshold level for the 8 signal inputs are tied to a common threshold level

and the threshold to the trigger input goes to a separate control. It will be noted that the left side of the Schematic encompassing the buffer amplifiers and the descriminators represents a block diagram of the circuit, and not the circuit details. Now referring to the upper right of the Schematic, the details of the buffer amplifier-descriminator will be described.

The input buffer amplifier has approximately unity gain and virtually zero offset from input to output. It consists of a pair of matched field effect transistors combined in a follower configuration. The passive attenuator consisting of resistors R-65 and R-41, along with the output impedance of the amplifier gives a gain of 1/3 from the input BNC connector to the input of the threshold detector following the amplifier. This reduction in signal is necessary when high input levels are applied to the input, because these high levels (greater than 5 Volts) if unattenuated, would exceed the dynamic range characteristics of the descriminator. Referring back to the input connector, it will be noted that the input impedance consist of a 1 Megohm resistor in parallel with a 20 pf capacitor along with the load associated with the input clamp and the field effect transistor. For signal levels below $\pm$ 15 Volts the input impedance will be determined by the RC network on the input terminal. For signal levels greater than $\pm$ 15 Volts, the dynamic input impedance will drop to 1 K.

The level detector is a monolithic device, fabricated two per package. The component type is NE521. It will be noted from the Schematic Diagram that, in addition to having a level detector, the device also contains a gated output capability. It will also be noted from the Schematic Diagram that the output gate is not used in the Model 810-D. The gate inputs are tied firmly to the +5V power supply, thereby enabling the output gate. Feedback around the descriminator is provided by a 200 K resistor. The feedback is positive and contributes about 25 mv of hystereses to the device. This hystereses entirely dominates the normal hystereses of the threshold detector and when reflected to the input terminal, represents a hystereses of approximately 75 mv.

The threshold level for the 8 input signals is determined by the front panel control. In addition to the 9 levels, there is also a variable level which the user can use within a range of $\pm$ 10 Volts. Referring to the Schematic Diagram, it will be noted that the input switch is buffered by an operational amplifier used in a follower configuration. This provides a low driving point impedance for the common bias line. The threshold level for

the Trigger input is driven directly from a front panel potentiometer and provides a range of approximately ± 10 Volts for the independent trigger input (taking into effect the 1/3 gain of the input section.)

Latch Circuit

If the signal level exceeds the threshold, a high level is written in the 810-D memory section. If the signal does not exceed the threshold, then a low level is written in the memory. However, prior to the memory, a data latch circuit is used as a temporary buffer and to allow two distinctly different modes of operation to be available for the user. This is shown in the center of Sheet 1 and is entitled "Data Latch Circuit". If the unit is operating in the Sample mode, then one input to the routing gates going into the preset and clear inputs on the first D register is grounded by the switch. This prevents the input signal to the latch circuit from influencing the D registers in any mode other than the data input (D input) to the first register. Likewise, the feedback from the second register to the first register is inhibited by the grounded input to the routing gate. Consequently, in the Sample mode the D register is set to a high or low level by the buffered Timebase signal. One clock pulse later, the information is transferred from the first register to the second register and read into the memory of the Model 810-D. In the Sample mode, the operation can be simply stated, "if the input signal is above the threshold at the time of the clock, a logic 1 will be written in memory." Conversely, if the input signal is below the threshold at the time of the clock edge, then a low level will be written in the memory. There is an additional one clock delay caused by the second register. However, since all eight data channels operate in an identical fashion, the data will still be lined up as stored in memory.

The Latch mode is somewhat more complex, but its presence in the unit allows much greater flexibility in the use of the instrument. The Latch mode allows the unit to capture small pulses (glitches) that often occur asynchronously within a system. It is the same narrow pulses occuring infrequently that are the most difficult to measure and to determine a timing relationship for. The latch capability of the Model 810-D largely overcomes these problems.

Let us assume that the input level has been below the threshold for some period of time. In this case, the Q output of the second register (MD-1, pin 9) will be at a low level and pin 8 will be high. The output levels will

condition the routing gates such that the gate to the preset input of the first register is capable of acceping a signal, whereas the clear routing gate is incapable of transmitting a signal. If a narrow input signal occurs which crosses the threshold, a narrow positive pulse will be generated at pin 2 of the first register. The pulse will have no effect at pin 2 because it has occurred unrelated to the Timebase. However, it will be transmitted via the preset routing gate (located above the first register on the Schematic) to preset the first register such that pin 5 goes to a high level. At the next clock pulse, the contents of the first register will be transmitted to the second register and consequently into the memory of the unit. The action just described will occur for pulses as narrow as 10 nanoseconds. It must be understood, however, that to transmit a pulse as narrow as 10 nanoseconds, a considerable amount of over-drive must be applied to the input section. If we reverse the conditions, whereby the input level has been above the threshold for some period of time, with the occurance of a narrow negative pulse, we will see that the same type of action occurs as with a positive pulse. The negative pulse, however, is transmitted to the clear routing gate such that it will cause pin 5 of the first register to go low for subsequent storage into the second register at the next clock pulse. In either the case for a positive or a negative pulse the first clock occuring after the pulse will change the first register back to its original quiescent state (high if the signal has been at the high level or low if the signal had been low), and this same clock pulse will transmit the contents of the first register to the second register where it will remain for a full clock period such that it can be written reliably into the memory section. In the event that a "glitch" occurs between each pair of clock pulses then the data written into the memory will alternate high and low levels. Such a condition if observed on the CRT display would indicate to the user that either there is an excessive amount of noise on this particular line or that a faster clock rate is needed. One point to remember as we leave the discussion of the data latch circuit is that data appears on the output of the second register (pin 8 of MD1-MD8) for a full clock interval and should never change except at the edge of the Time Base signal. Data is transmitted from the data latch circuit to the data circuit.

7.22 Data Circuit (Schematic Part 2, Page 57)

The data circuit consists of shift register memories, routing gates for the memories and buffered outputs to be used by peripheral devices. Referring to sheet 2 we can trace a data signal from the data latch discussed in the previous section through the memory section. Note that

the outputs from the data latches are buffered and made available at the rear panel by means of the inverting buffers (ME1 & MF1). Referring for a moment back to the data latch circuit on Sheet 1 it will be noted that the inverting output of the second latch is used instead of the non-inverting one. The use of an inverting buffer on the input to the data circuit restores the signal to the proper state at the rear panel.

The data circuit serves the purpose of storing the input signal. The heart of the data circuit is a 256 word shift register for each of the 8 input signals. These shift registers are clocked synchronously such that data appearing on the inputs are recorded synchronously within the memory. This maintains the timing relationship present on the original data at the input connectors. If the Insert signal is at a high level, then the input data from the latch circuits is transmitted to the memory. Under these conditions a signal appearing on pin 3 of ME-2 Data -1 would appear on pin 4 of ME-2. In like fashion, the Data 2 signal on pin 6 would appear on pin 7 and so forth. In the event that the Insert signal is at the low level, the Data signals are not transmitted to the memory. Instead, the output of the memory is fed back to its own input. The Insert signal therefore controls whether or not data will be input to the memory or old information will be circulated within the memory. The memory outputs in addition to being routed back to the input multiplexer (AMD 9322) are also buffered (MG 1 & MF1) for use at the rear panel. The two memories, ME-3 and MF-3 are clocked by a two phase clock system common to both units. This will be described in section 7.24 of this manual.

7.23 Y-Display Circuit (Schematic Part 2, Page 57)

The Y-Display Circuit functions to provide a CRT display of the memory contents. With the data stored in memory, the full contents of the memory are output during an interval of 512 microseconds. The timing relationship between each set of 8 bits must be maintained throughout the full display of the memory contents. This is accomplished by sequentially displaying each bit. For example, during 1 memory cycle bit 1 would be displayed. During the second memory cycle bit 2 would be displayed. Under these conditions the entire memory contents would be displayed each 4 milliseconds to provide a refresh frequency of 250Hz. With a reasonable CRT persistence this will provide a flicker-free display. NOTE: Because of the duty cycle limitations of conventional oscilloscopes the display circuit of this instrument has been modified slightly from what is described above. Instead of reproducing the data frame for every 8 memory cycles, an additional cycle has been added. First, visualize the Y-Display circuit without flip-flop

MF-4 in the circuit. Without this flip-flop, $A\text{-}2^7$ which is the most significant address bit would cause the binary counter MG-3 to count zero through seven and repeat itself. This action would occur at any time the address counter is operating and therefore is functional during a data display mode of operation. Counter MG-3 feeds its 3 binary outputs both to a digital-to-analog converter and to a "1 of 8 decoder" (MG-2). When the counter is at zero data bit 8 is routed through MG-2; when the counter is at the binary state 1, bit 7 is routed through the decoder; and when the counter is at the binary condition 7, bit 1 is routed through the decoder. By this technique the state of the binary counter feeds both a selected data bit to the DAC and simultaneously provides the proper offset to the display by means of the DAC.

Recalling that we are assuming that MF-4 is not in the circuit, the above description is of a circuit which would provide a 8 level stair step on the Y-output. Each major stair step portion of the display would be modulated by the data bit selected for that step. The amplitude adjustment is controlled by the Y-gain potentiometer, R180. The height of the bit is controlled by the bit adjust potentiometer, R179. Recalling the earlier comment that the fundamental display cycle described above has been modified because of the limitation on duty cycle for most oscilloscopes, we must now expand our circuit description by a small amount. The purpose of flip-flop MF4 in the Y-Display Circuit is to force the stair step to remain at its zero level for two consecutive memory cycles. This is accomplished by using the overflow from the binary counter to clear the flip-flop MF-4 by means of its direct clear input. When the flip-flop has been cleared it will inhibit the next count from going to the binary counter by means of the gate MG-4, pin 13. The overflow from the address counter ($A\text{-}2^7$) instead sets the flip-flop MF-4 back to its normal state thereby allowing the binary counter to progress normally until it overflows the next time, at which time the sequence repeats. Now if we were to take a look at the Y-output we would see again a stair-step but this time it would remain on the lower step for twice as long as it remains on each of the other positions. This technique allows the 810-D to be used with any oscilloscope without in any way violating the duty cycle capabilities of that oscilloscope.

7.24 Clock Drive Circuit (Schematic Part 2, Page 57)

With a shift register memory it is necessary to provide shift or clock pulses. These pulses read old data from the memory, write new data into the memory and shift data through the memory. The memories employed in this unit require a two-phase clocked system. Referring to sheet 2 it will be noted that the memory in the data

circuit have clocks designated as Ø 1 and Ø 2. The clocks alternate words in the memory such that Ø 1 would write a word in the memory and Ø 2 would be used at the next word. It is the purpose of the clock drive circuitry to generate these clock pulses. Before explaining the circuit in detail, it is well to remember that the clock pulses to the shift register memories are negative going pulses originating from +5 Volts and falling to a low level of about -12 or -13 Volts. These clock pulses have a width of about 80 nanoseconds, with data being read from the memory on the leading or negative going edge of the pulse and new data being written into the memory on the positive or trailing edge of the pulse. In observing the clock drive circuit, it will be noted on the right hand portion of the circuit that there are three fundamental inputs to the circuit. These are: 1. Clock pulses are generated by the Time Base during Record operation at high speed(interlace). 2. Output mode, with the Command signals from the output interface providing the timing for the memory. 3. At 2 µsec intervals when either the Display mode or Record at low speeds (interlace) is the mode of operation. There are no other methods by which a clock signal can be generated. To repeat, clock signals are generated in the Record mode by the Time Base signal at high speeds and by the 2µsec time base at low speeds. They are generated by the Command pulse in the Output mode, and in the Display mode they are generated by the 2µsec time base. The active signal is called Memory Clock and causes the edge triggered flip-flop MG-5 to toggle as a binary counter. The binary counter divides the Memory Clock rate by 2 and on each edge of the flip-flop output causes a clock pulse to be generated. Consequently, for each Memory Clock signal there is a clock pulse generated, but each clock pulse is 1/2 of the rate of the Memory Clock.

The clocks themselves are generated by a monolithic clock driver MH0013C in location ME-4. The inputs to this clock driver on pins 2,4 and 6,8 are driven from the collectors of grounded base transistors Q1 and Q2. Emitter current is injected into each transistor from MF-5 which drives the respective emitter through a 330 ohm resistor. The signal from the gate MF-5 is generated by a shaping circuit connected back to MG-5 the binary divider for the memory clock. The current pulse from transistors Q1 and Q2 is approximately 80 nanoseconds wide and is the primary determining factor for the memory clock pulse width. Additional speed-up drive is given to the clock drive circuit by the feed forward capacitors from the outputs of the memory clock flip-flop to the inputs of the clock driver. These feed forward capacitors serve to overcome the circuit delays associated with the shaping gates and the transistors.

The only critical timing associated with the memory clock drive circuit occurs in the record mode at the fastest recording rate -10MHz. At this rate it is essential that the back edge of a clock pulse is terminated before a data change occurs at the memory inputs from the next Time Base Pulse. The design provides for approximately 25-30 nanoseconds of time from the back edge to the change of new data in the memory. This should more than provide enough data hold time for the memory device.

7.25 Start-Stop Circuit (Schematic Part 3, Page 58)

The record process is normally started with the front panel momentary switch labeled, Record. The process can also be started with the Remote Arm signal located on pin 22 of the rear panel connector. The front panel switch utilizes a de-bouncing flip-flop consisting of two parts of the gate MF-6. In either the manual start or the remote start a positive going signal is generated at pin 5 of gate ME-5. If the signal at pin 5 of ME-5 is positive when A=0 (address = zero) is positive then a negative signal will be generated at pin 1 of ME-5 causing the Record flip-flop to be set with the Record signal at a high level. As we have seen earlier when the Record signal is at a high level the memory clock drive circuit produces memory clock pulses at a rate determined by the time base in the non-interlace mode of operation and at the 2 microsecond rate and the interlace mode. We will also note in the start stop circuit that the insert signal is positive if the record flip-flop is set and if A=0 is also high. As explained in section 7.29 we shall see that A=0 constantly during the Record, interlace mode of operation. During Interlace operation, new data is properly input to the memory only when A=0 is high.

If we assume that the unit was operating in the Display mode prior to pushing the Record button then it is apparent that there will be a latency of up to 512 microseconds before A=0 occurs to set the flip-flop. Since the operation has been started manually this latency period is of little consequence. In the event that the record function has been started by means of the Remote Arm signal, it will be necessary for the Remote Arm signal to be held at the low level for a minimum of 512 microseconds or until the interface detects that the Record signal located on pin 20 of the rear panel connector has gone to the high level. The record process is terminated by a low signal on either pin 9 or pin 10 of MF-7. The signal on pin 9 is generated by the front panel momentary switch, Manual Trigger. The signal on pin 10 is generated from the delay counter which will be described in the next section. If either of these signals goes low, a high level is generated

at pin 12 of MF-6 resetting the Record flip-flop and terminating the record process.

7.26 Delay Counter (Schematic Part 3, Page 58)

The normal process of stopping the recording operation is by means of a Trigger. As seen in the lower portion of Sheet 1, the Trigger signal can come by means of the Trigger input with its separate threshold detector, if External triggering is selected by the front panel control; or it can come via input number 8 with the common threshold, if Internal triggering is selected. In either of these cases a signal called Trigger is generated. Trigger will be in phase with the signal which generated it. In other words trigger will go high as the generating signal crosses the threshold in the positive direction and trigger will go low when the generating signal crosses the threshold going in the low direction. Trigger is one input to the "exclusive or" gate MG-7. The other input comes via the front panel Slope control. If Slope is set positive then Trigger going positive will generate an activating signal into the clock input of the edge trigger flip-flop MG-5. If Slope is set to the negative position then Trigger going low will generate an activating signal into this same input of the flip-flop. Since the D input is held positive the positive transition of pin 3 will cause the Q output to go high and the $\overline{Q}$ signal to go low unless the $\overline{arm}$ or Record signals are holding the flip-flop in the reset condition.

Backing up for just a moment, we can visualize a situation where a manual record operation is started and where input conditions are such that triggers would be continuously generated. Under such a condition the record process would be started and stopped almost immediately. However, the memory contents (old information) would not be completely flushed out and the user would be presented with a scrambled set of data consisting of a mixture of both old and new data. By utilizing the $\overline{arm}$ signal to prevent Triggers from being accepted during the time that the Record push-button is activated we can assure that old data is completely flushed out of the memory during the fast record rates. Picking up where we left off, if we assume that a Record operation has been started and that a Trigger is generated then flip-flop MG-5 will be set. Setting of MG-5 will remove the DC resets on the 8 bit binary counter consisting of MG-8 and MH-5. This reset comes from the $\overline{Q}$ of MG-5 and goes to pins 2 and 3 of MG-8 and MH-5. With the flip-flop set to the true level the Time Base signal is counted in the Delay Counter. When the selected number of counts have been accumulated in the binary counter a Delayed Trigger pulse will be generated at the rear panel and simultaneously will feed upward on the Schematic into

$\overline{\text{Display}}$ is generated when neither the Output nor Record modes of operation are selected. This is controlled by gate MH-3. The Output mode is selected when the flip-flop MF-4 has been triggered such that pin 12 is at the high level. Output is obtained only upon the request from the external interface. When Output is requested, pin 19 of the rear panel connector is pulled to a low level. This raises pin 14 of MF-4 to a high state, such that when the signal on pin 1 of MF-4 goes to a low level, the flip-flop will be set such that pin 12 is high. If we assume that the unit is operating in the Display mode such that $\overline{\text{Record}}$ is at a low level, we can talk our way through the circuit description. Under these conditions the signal $A\text{-}2^7$ is occuring every 512 microseconds (the total cycle time of the memory). If at some arbitrary time the Output Request signal signal is pulled low, then within a period of 512 microseconds $A\text{-}2^7$ will transmit a negative going edge to pin 1 of MF-4. This will cause the flip-flop to be set, and at that time the Output Enable signal on pin 21 of the rear panel connector will go to the high level. This is a signal to the output device that the Output Request signal can now be returned to its normal high level. At the same time that Output goes high then a negative pulse is generated at pin 6 at MH-3. This negative pulse appears as a positive pulse on pin 1 of MJ-2, the Flag flip-flop. The trailing edge of the positive pulse on pin 1 of MJ-2 causes the Flag signal on pin 12 to go high. The positive transition of Flag signal should be utilized by the interface device to strobe data from the model 810-D into buffer storage of the peripheral device.

When the peripheral device is ready for the next word of information, the $\overline{\text{Command}}$ signal should go to the low level. This leading edge of the negative going $\overline{\text{Command}}$ signal generates a pulse in the two gates of MJ-1 to clear the Flag flip-flop. The Flag signal will go to the low level upon the leading edge of $\overline{\text{Command}}$. Also on the leading edge of $\overline{\text{Command}}$ a new word of information will be clocked from the memory as described in the earlier description of the clock drive circuit. Approximately 100 nanoseconds after the leading edge of $\overline{\text{Command}}$ a Memory Drive occuring on pin 10 of MH-3 will clock the Flag signal back to the high level, indicating to the interface device that new data is available. This process of $\overline{\text{Command}}$-Flag is known as a hand shake routine and can continue word for word until all 256 words of data have been clocked from the 810-D. At that time, the most significant address bit $A\text{-}2^7$ will go low on pin 1 of MG-4, and will be transmitted as a negative going signal on pin 1 of the Output flip-flop MF-4. This will return the Output Enable to the low level and place the unit back into the Display mode.

the start-stop circuit through pin 10 of MF-7. As described earlier a signal on this pin occuring in synchronization with A=0 will terminate the record process. When Record goes low, the Delay Counter will stop counting because Record on pin 10 of MG-6 prevents the gate from transmitting Time Base signals to the counter.

It is important to keep in mind that once the recording process has been started, valid data is in the memory at all times. The Trigger merely tells the unit when to stop recording. This is the reverse operation from many conventional instruments. However, it is very significant to point out again that the model 810-D has the capability of looking in front of the Trigger signal and thereby achieving a negative time delay. When we select a delay we are in effect determining the amount of data to be observed prior to or in front of the Trigger. If a Delay of 7/8 is selected then this is interpreted as a desire to have 7/8 of the recorded data in front of the Trigger. Consequently, upon receipt of a trigger 32 Time Base pulses will be counted before the Delayed Trigger signal is generated to stop the recording process. Likewise if a delay of 1/2 is selected then 1/2 of the data recorded is before the trigger occured and the trigger allows 128 time base pulses to be recorded before stopping the recording process. Similarly, if a Delay of 1/8 is selected, then only 1/8 of the stored data occured prior to the trigger and 224 time base pulses are counted after the Trigger. The Delayed Trigger is routed to the rear panel of the unit to be used for multiple unit connections. It normally is not used when a single unit is being operated. The Delayed Trigger as described earlier stops the recording process by feeding through gate MF-7 and MF-6 to reset the record flip-flop. Trigger on pin 45 of the rear panel connector is available for this function. The digital trigger is normally held at a high level and upon going to a low level activates the Delay Counter. From this point, the Delay Counter functions in an identical manner as described above.

When the recording process is stopped by means of the Manual Trigger, the delay circuit is bypassed. This bypass feature is intentionally provided for slow recording speeds where the operator may see a pattern of interest on the CRT display and make the decision to stop data recording. With the delay eliminated he does not have to take into consideration the additional data recording that would otherwise occur if the Delay Counter was active.

7.27 Output Circuit (Schematic Part 3, Page 58)

The Output Circuit is used only when an interface device is used in conjunction with the model 810-D to transfer the contents of the 810-D to an external device. First, note that at the left portion of the Output Circuit the signal

NOTE: In the previous discussion two significant items were omitted. 1) After the external interface has detected Output Enable going to the high state, a period of no longer than 500 microseconds must elapse before the first Command signal is generated. Furthermore, there must not be a period greater than 500 microseconds elapse between successive Command signals. Should the time between these signals become greater than the specified period, the output data may not be valid. 2) Once the output mode has been entered, a minimum of 256 Command pulses must be generated. Otherwise, the unit will be left in the output mode with no way to exit this mode, other than by means of pushing the Record pushbutton which generates Arm signal on pin 2 of the Output flip-flop thereby resetting this flip-flop.

A second mode of operation would occur if the Output Request is initiated during the Record process. This would be used in those conditions where an automatic data outputting process is to be initiated each time the device is triggered. If we assume that the Record is in process then the Record signal on pins 2 and 5 of MG-4 is at a low level. In addition, pin 14 of MF-4 is assumed to be at the high level because the Output Request line is being held low. Finally, $A\text{-}2^7$ will either be in the low state or will go to the low state just prior to ending the record process. In either case pin 4 of MG-4 will be high when Record on pin 5 goes high. This will cause a negative transition at pin 6 at MG-4 and pin 1 of MF-4 forcing the Output flip-flop to change to the Output mode. From this time on, the circuit functions as described earlier and at the end of Output the unit will revert to the Display mode.

7.28 Time Base (Schematic Part 4, Page 59)

The Time Base Circuit of the unit provides both the periodic clock for circulating the memory in the Display mode of operation which is fixed at 2 microseconds per word and the selectable clock rate used for strobing data into the memory. Before describing the Time Base circuit it should be noted that dynamic shift registers have both a high frequency and a low frequency limitation. In the model 810-D the memory devices that are utilized have a guaranteed upper frequency of operation of 10MHz, and this is the upper rate at which these devices are used in the instrument. The low frequency limitation however, does not allow the instrument to run as slowly as might be desireable for some applications. Under these conditions the memory must be clocked at a much higher rate than the rate at which new data is input to the memory. For this unit we define two types of recording: 1. Interlace recording - Interlace recording occurs when the data input rate is slower than the

actual clock rate. This occurs at data rates that occur below the minimum specified operating frequency of the shift register memory. The model 810-D utilizes devices which are guaranteed to operate as slowly as 1 Khz.
2. Non-interlaced recording - This applies to recording rates at which the memory is clocked at precisely the same frequency at which new data is entered into storage. This occurs for all clock intervals shorter than 1 millisecond.

As we shall see in section 7.29, the Address Counter does not operate at the non-interlace recording speeds and consequently there is no data display on the CRT monitor attached to the unit. Referring to the Time Base Circuit, it will be noted that the basic clock is derived from a 10MHz crystal oscillator connected into a feedback circuit utilizing two parts of gate MK-1. The 1 μsec Time Base and the 2 μsec Time Base are derived by dividing the 10 MHz crystal oscillator down to 1MHz by decade divider MK-2. This produces a 1MHz time base signal at pin 11 at MK-2 which is further divided by a factor of 2 by the binary counter MG-3. The signal on pin 12 of MG-3 is the 2 μsec time base utilized for clocking the memory at all Interlace recordings speeds and in the Display mode.

Referring to the switch decoding circuit shown in the middle of sheet 4, it will be observed that a very simple decoding scheme is utilized whereby 3 signals for multiplication factors of 10 are derived - these are called 1/10, 1/1, and 10. Three additional signals are generated for intermediate ranges, and these are called X1, X2, and X5. Under any internal selected conditions, two of these 6 signals will be in the high state. The other four will be in a low level. The signals which tell the unit to interlace or not to interlace are also derived from the Sample Interval switch in conjunction with the multiplier switch for microseconds or milleseconds operation. The decoding for the Interlace control is such that the Interlace signal on pin 3 of MJ-6 is at a high level when the microseconds/milliseconds switch is in the milliseconds position and the interval switch is in any position other than .1, .2 or .5.

For purposes of illustration let us take an example whereby the clock is selected to operate at 5 microseconds clock intervals. Under these conditions the signals X1/1 and X 5 will be true and Interlace will be low. We can trace a signal path from pin 6 of MK-1, the oscillator buffer gate; through MK-2 pin 11 where the frequency has been divided down to 1MHz; through MJ-3 pin 11 where we maintain the 1MHz rate. We will note in passing that the

1MHz rate is divided down by MK-4, MK-5 and MK-6 to a 1Kz rate on pin 9 of MJ-6. However, this signal is gated off with the microseconds multiplier switch grounding pin 10 of MJ-6. However, the millisecond position on pin 1 of MJ-3 is pulled high by the resistor on the front panel and allows the 1MHz signal on pin 11 of MJ-3 to be gated through to pin 3 of MJ-3. At this point the signal has three possible paths only one of which we have selected. That is the route through the ÷ 5 portion of MJ-4 into pin 10 of MJ-5. The positive signal on pin 9 corresponds to our selection of 5 microsecond intervals. The Time Base signal on the common outputs of MJ-5 represents a pulse-train at the selected time interval. As we have seen in other parts of this circuit description, this signal is used for clocking the memory and strobing data into the input data latches. If we revise our example to select 5 millisecond time intervals rather than 5 microsecond time intervals, we will find that the signal at the common pin 3, pin 8 connection of the MJ-6 will be exactly 1,000 times slower than earlier. This occurs because the signal from MJ-3 pin 6, 8 and 11 is routed through the three decade counters, MK-4, MK-5 and MK-6 back into MJ-6.

If an external clock rate is selected by means of the front panel Clock Interval selector, then the input goes from the front panel to pin 5 of MJ-5. Pin 4 will be at the high level due to the selection of the External rate. At the leading edge of the External Time Base signal, Time Base will go low and after 1 additional gate delay will strobe data into the input Data Latches (Section 7.21). It is important to remember that the leading or positive going edge of the External clock is the activating edge for that signal. It is also important to note that the microseconds/milliseconds switch must be used properly with the External clock. If the clock interval is less than 1 millisecond than the multiplier switch should be at the microseconds position. If the interval is greater than 1 millisecond than the switch should be set to the milliseconds. As seen earlier this will determine whether or not the unit operates in the Interlace or Interlace mode.

For further discussion on the operation during recording refer to Section 7.31.

7.29 Address Counter (Schematic Part 4, Page 59)

A shift register memory when fed back from output to input has no well defined starting point. Consequently, when keeping track of information it is necessary to utilize a separate counter. In the model 810-D this separate counter is called the Address Counter. The Counter consists

of two 4-bit binary counters, MG-10 and MJ-8. Together they comprise an 8 bit binary counter of 256 words. Note that A=0 (address =0) on pin 6 of MH-7 is generated when all 8 bits of the binary counter are in their low level. This signal is at the high level for 1 and only 1 position among the total 256 possible states of the Address Counter. It will also be noted that a second diode gate network is used to generate the Z and $\overline{Z}$ signals used for external blanking with a CRT and also for driving the X-Ramp circuit. Note that the first two bits of the address counter are not used in the diode gate feeding pin 9 and 10 of MH-7. Consequently, pin 8 of MH-7 will go to the low state for 4 consecutive addresses (zero through 3) and in all other times be high. The Z signal is the inverse of the $\overline{Z}$ signal and consequently goes to the high state for these same four address locations. Note also that the nor gate MG-9 holds the address counter reset to zero during the Record, non-interlace mode of operation. As we shall see a bit later, holding the address counter to the reset condition prohibits the display operation. If we assume that the unit is operating in the display mode, then the address counter is being advanced each 2 microseconds. This advance pulse is the Memory Clock signal which is derived from the Clock Drive Circuit on Sheet 2 of the Schematic. The counter will cycle through its full range each 512 microseconds. Each time it goes to address zero, the A=0 signal on pin 6 of MH-7 will go high. The $\overline{Z}$ signal on MH-7 pin 8 will go low each time the counter reaches the contents of 252 and will stay low for 4 consecutive address locations. As long as the Display mode is maintained, this process will continue and the $\overline{Z}$ signal will synchronize the X-Ramp to the Address Counter. The most significant bit of the Address Counter on pin 11 of MJ-8 is $A\text{-}2^7$. It will be recalled that this signal is used in entering and leaving the Output mode of operation.

In Record-Interlace mode the operation of the address counter is somewhat more complex than in the other modes. In this mode the three flip-flops located directly beneath the Address Counter are utilized. Let us assume that the input data rate is quite slow and that between each data input to memory there is time for the address to completely cycle several times. When a Time Base signal occurs, data will be strobed into the Data Latch circuit. The Time Base signal likewise will set pin 5 of flip-flop MF-9 to the high state, because the D input to that flip-flop, Record, is high. Nothing further will happen until A=0 goes high. A=0 is normally in the low state and being applied to the direct clear inputs of both sections of flip-flop MF-8 will hold them in their reset conditions. When A=0 goes to the high state this reset is eliminated. The next occurance of the 1 μsec Time Base following A=0 going

to the high level will transfer the high level on pin 5 of MF-9 to pin 12 of MF-8. When pin 12 of MF-8 goes high, pin 13 goes low and acts to inhibit the Memory Clock signal from adding a count to the Address Counter. The second occurance of the 1 μsec Time Base will cause pin 9 of MF-8 to go high such that now both outputs on pin 9 and 12 of the two sections of the MF-8 are both high. When pin 8 of MF-8 goes low, MF-9 is returned to its original condition. The third occurance of the 1 μsec Time Base will reset both sections of MF-8 to their original state. The net result of all of this effort is to force the Address Counter to stay in the Zero condition for two consecutive Memory Clock pulses each time data is put into the memory.

If we recall in the description on the Start-Stop circuit that the Insert signal which provides new data being input to the memory is only valid when A=0 we can understand why this mode of operation was chosen. Visualize that the counter is running and that the address currently identified as Zero is in fact the next location to which data will be inserted. When this data is actually inserted at that position, the Address Zero position is slipped one position in the memory. Thereby aligning itself just behind the previuos location where we inserted data, which is in fact the next location where new data must be inserted. If one monitors the signal A=0 during a Record-Interlace mode of operation it will be observed that A=0 is normally two microseconds in duration and occasionally is extended to four microseconds. It also helps in understanding this particular circuit to recall that the 1μsec Time Base and the 2μsec Time Base which generates the Memory Clock signal are firmly locked together.

7.210 X-Ramp (Schematic Part 4, Page 59)

The X-ramp is a linearly increasing voltage synchronized with the Address Counter in the model 810-D for the purpose of providing X deflection in an XY CRT display. It consists of a current source Q5 driving a capacitor C24. The reference end of the capacitor goes to the emitter of a "grounded base" transistor stage, Q4. The base of Q4 goes to the Horizontal Position control located on the front panel such that the emitter of Q4 is raised or lowered and the base voltage is changed, thereby changing the origin of the X ramp. The ramp is allowed to charge linearly up to the address 252 at which time the $\overline{Z}$ signal coupling through MF-7 pin 11 turns on Q3, discharging C24. C24 is held in the discharge state until the end of the $\overline{Z}$ signal or until address zero occurs. At which time Q3 is turned off and the linear charging process begins. The amplitude of the ramp is controlled by R181 in the

emitter of Q5. This potentiometer controls the amount of current being dumped into the capacitor. The origin as described earlier is controlled by the voltage on Q4 which is derived from the front panel position control. Q6 is an emitter follower providing the X ramp drive to the output on the rear panel (via the front panel) and serves to prevent loading on the C24. During those times when the address counter is not being used, C24 charges up to the point where Q5 saturates. This produces a voltage of approximately 7.5 volts and drives the display on the XY CRT unit off scale to the right.

The ramp voltage at Q6 is normally adjusted to an amplitude of approximately 5 volts. This signal is transmitted to the front panel multiplier control where under normal conditions the signal is attenuated by a factor of 5 so as to produce a 1 volt linear ramp at the rear panel. When the X5 expansion is selected the attenuation is removed and a 5 volt ramp would be generated at the rear panel were it not for the clamp diodes which limit the actual voltage swing between approximately $\pm$ 1.5 volts. The clamp circuits are utilized to protect the CRT device from excessive drive voltage. The horizontal position control when utilized in the X 5 position moves any portion of the 5 volt ramp to within the $\pm$ 1.5V region for linear deflection of the CRT.

7.3 Operating Modes

This section will provide a description of the series or sequence of events that occur in each mode. By necessity some things will be omitted. However, it is hopeful that this section will lend itself to a more fundamental understanding of the way the model 810-D operates.

7.31 Record-Internal Time Base Non-Interlace

If we assume that the instrument has previously been operating in a Display mode, the Record mode starts when the manual Record button is pushed. Pushing the button generates a non-bouncing signal in the start-stop circuit at pin 6 of MF-6 which together with the A=0 signal sets the unit into record via ME-5 pin 6. There will be a latency of up to 512 microseconds before the A=0 occurs. As long as the switch is depressed the $\overline{\text{Arm}}$ signal will be at the low level and this signal will hold the Delay Counter reset to its zero condition via pin 2 of MG-6 into the clear input of the flip-flop. Since the slowest interval in the non-interlaced mode is .5 milliseconds, the time to cycle through 256 words of memory is only 128 milliseconds. The manual hold-off on the trigger flip-flop virtually insures that all old data in the memory from a previous recording operation will be flushed out.

We are now in the Record mode and data is being inserted into the memory with each Time Base signal. The time base will be as selected by the front panel Clock Interval Switch. The Address Counter is being held reset to its zero condition by MG-9, and the horizontal ramp is inoperative such that no display is available on a CRT. The Record indicator on the front panel will be eliminated as the only indication that the unit is functioning. This process will continue indefinitely, and at any point in time there are 256 previous data words in the memory. The Clock Drive Circuit which is providing clocks to the memory is being controlled by MH-2 pin 6 which is a pulse occuring at the rate of the Time Base. It is worth repeating that in this mode the Address Counter is being held at zero, and as indicated by the Start-Stop circuitry the Insert signal under these conditions is always true. This insures that new data is constantly being input to the memory. When a Trigger pulse occurs the Delay Counter starts a count down process. It counts at the rate of the Time Base. When the preselected number of counts have been accumulated in the Delay Counter, an output pulse called Delayed Trigger is produced. This pulse feeds back to the Start-Stop circuit and terminates the Record process immediately since the A=0 signal is already present. Assuming that an Output Request has not been made during the Record time the Display mode will be entered immediately. This mode is further described in Section 7.34. It is important to remember that the recording process will continue until stopped by a Trigger. Furthermore, the Delay Counter functions to provide a control of the amount of data stored prior to the Trigger. This allows the operator by means of the CRT display to actually see the timing conditions of the 8 inputs prior to the condition that provided the Trigger.

7.32 Record-Internal, Interlaced

In the Interlace mode of recording,the Start-Stop process is identical to the non-interlaced. Once recording the difference is that the memory is clocked at a constant rate of 500Kz and the Address Counter is operating. A display is provided in this mode of operation. If a CRT is utilized, data will appear to enter the CRT on the right hand side of the screen and move to the left hand side at which point it disappears. This mode of operation is available only for clock intervals longer than .5 milliseconds.

Data is strobed into the input Data Latches on each occurance of the Time Base signal. This data will be written into the memory at some time following the time base

signal but within a period of 512 microseconds. Since another time base cannot occur sooner than 1 millisecond there will always be the opportunity to store the data in memory prior to strobing new data into the input Data Latches. The Address Counter is functioning and the address, A=0, is used as a marker signal to indicate the next address at which new data will be inserted. When data is inserted into this particular address the signal A=0 is allowed to slip one position with respect to the memory such that it now aligns itself with the next slot in memory after the one just filled. This is the next location in which new data will be inserted. This process likewise continues until a trigger is received. At this time the Delay Counter again begins to count down from the Time Base signal until the selected number of counts has been accumulated at which time the Record process is ended. Again, however, waiting until the signal A=0 occurs. A=0 must occur each 512 microseconds and since the time base signal cannot occur more often than each millisecond in the Interlace mode of operation there is no danger of failing to recognize the end of the delay. When the Record flip-flop is reset the Display mode is entered as described earlier.

7.33 External Time Base

When utilizing this instrument with an external time base it is essential that the time base signal be continuous. It must be a pulse train which starts before the Record push button is activated and which continues beyond the time when Record ends. The unit is not intended to be used with discontinuous clocks. It should also be remembered that when utilizing the external time base that the microseconds/milliseconds switch must be used properly to insure valid data storage. Clock rates faster than 10MHz are prohibited, and for clock rates below 1Kz the milliseconds range must be selected. Failure to select the milliseconds range with low speed clocks may result in garbled data being stored. The External Time Base signal is gated into the common output gate MJ-5 on pin 6 of that gate. Once the signal is at this point it is indistinguishable from an internally generated time base signal,and the recording mode proceeds in an identical manner to that described above for the internal time base. The only difference is that now the time base can be of any frequency within the specified operating ranges and not at a precise 1, 2 or 5 multiple of the fundamental crystal frequency. The unit is instructed to be in the Interlace or Non-Interlace modes depending upon the position of the milliseconds/microseconnds range switch. It is possible to violate the input conditions by having the range switch in the wrong position relative to the clock

frequency being used. For example, if a clock frequency of greater than 1Kz is used in conjunction with the milliseconds range position then the instrument will be instructed to interlace by the range switch while the time base is too high for proper interlacing to occur. In this case bad data storage would result. Likewise as mentioned earliear if a rate slower than 1Kz is used with the range switch in the microseconds position bad data can also be the result. Beyond this one consideration of matching the input rate with the range selector, recording does proceed identical to that described under the internal operation.

7.34 Display Mode

The Display mode is the normal mode of operation occuring at the end of the Record mode. It is the mode which provides for a CRT display of the memory contents and is the mode most likely to be used for data interpretation. During Display the memory is clocked at a constant rate of a clock each 2 microseconds, providing a complete memory cycle each 512 microseconds. An X ramp is generated by the X ramp circuit illustrated on sheet 4 of the Schematic and this synchronizes the CRT with the data being read from memory. Each clock represents 8 new bits of information at the rear panel. However, since most CRT devices are signal beam devices it would be impossible with such a device to see 8 simultaneous traces. Consequently, a mode has been devised such that the data bits are sequentially displayed. The rate of display is sufficiently high such that flicker does not occur. Sequential display is provided by a 1 of 8 decoder located in position MG-2 on the circuit board. Each bit of memory information is displaced vertically by means of a digital to analog converter operating in conjunction with the binary counter MG-3 which selects the respective bit from the memory. In order to accomodate conventional oscilloscopes which have duty cycle limitations, the stair step function is forced to remain in its lowest level for two consecutive memory cycles. This is scarcely observable in normal operation with the only effect being to show bit 8 (on the lowest level) at a slightly greater intensity than the other seven bits.

Once entered the display mode will continue until either a new recording sequence is started or the Output mode is selected.

7.35 Output Mode

The Output mode is selected to transmit digital information stored in the model 810-D to the outside world by means of an interface or peripheral device. Data is clocked from the 810-D asynchronously to the interface.

The technique used is called a "hand-shake" routine. By this technique the output device first requests an Output mode,and this is acknowledged by the 810-D with an Output Enable signal. At the time that the enable signal appears, the request line can be returned to its normal condition. Simultaneously, with providing the Output Enable a Flag signal will also be generated by the 810-D signifying that valid data from the first word of memory is on the output lines in the rear panel connector. The interface should utilize the positive transition of the Flag signal as a data strobe. Each successive word following the first word must be requested by the interface by means of a $\overline{\text{Command}}$ signal. The signal is normally at a high level and must be driven to the low level in order to request new data. The $\overline{\text{Command}}$ signal is utilized internally in the 810-D to advance the memory by 1 location providing new data on the output and also to generate a new Flag command. The sequence would be that with the Flag high from the first word the $\overline{\text{Command}}$ signal would cause the Flag to go low immediately. Within approximately 100 nanoseconds of the $\overline{\text{Command}}$ signal the Flag would return to its high level signifying that valid data from the second word is now available on the output lines. Flag going high can be used also by the interface as a signal to remove the $\overline{\text{Command}}$ signal. However, this latter operation of removing the command is not essential to the proper operation of the device. There are two restraints involved in using the Output mode. First, $\overline{\text{Command}}$ pulses following the positive transition of the Flag signal can have a latency of no more than 500 microseconds. A delay of longer than 500 microseconds may result in bad data output. This limitation occurs because of the low frequency limitation upon the clock rate of the MOS shift register memories used in the device; secondly, the Output mode with $\overline{\text{Commands}}$ must continue until the Output Enable signal is returned to its low level. The 810-D depends upon dumping all data once the Output mode is selected. In the event that all 256 data words are clocked out of the 810-D then the Output Enable will go back to its normal low state and the device will revert to the Display mode of operation. If however, the Output Request has never been taken away, then after 512 microseconds the Output mode will again be generated and the process must be repeated. Therefore, it is important that the interface designer take these items into consideration in order to properly utilize the Output mode of the 810-D.

7.36 Multiple Unit Operation

It will sometimes be necessary to synchronize two or more model 810-D units together in order to capture sufficient data to solve the measurement problem. This cap-

ability has been provided for on the rear panels of the model 810-D by means of 2 BNC connectors. These connectors are labeled Time Base I/O and Delayed Trigger I/O. They are intended to be used only when connecting 1 model 810-D to another model 810-D and not as a normal inputs from pulse generators, computer interfaces, etc. In operation, two short coaxial cables would be used to connect two units together. The Delayed Trigger between the two units should be connected together and the Time Base between the two units should be connected together. One of the units should be selected as the master unit and the other unit as a slave unit. The slave unit should have its Clock Interval switch set to the external position. However, no input should be provided to this unit. It will receive its time base signal through the Time Base I/O interconnection between units. NOTE: The μsec/msec switch must be set correctly by the slave unit. If the clock interval provided by the Master unit is less than 1 msec, then μsec is selected by the Slave; and if the interval is greater than 1msec, the msec position must be selected. The master unit can be selected to operate on either internal or external time base as desired. It will operate in the normal mode as described earlier in this section. The recording process is started manually or remotely on both units. The recording process between the two units will function as described in the manual. One or both of the units can be configured to select a trigger. Whenever either unit detects a Trigger signal and its respective Delay Counter provides a Delayed Trigger this signal connected common to both units will stop the recording process.

If the Manual trigger is utilized, there is no provision to feed this signal to the second unit, such that the manual triggering of 1 unit will have no effect on the other unit.

In order to achieve a satisfactory CRT display of the contents of two units, it will be necessary to configure a 3-pole 2-position switch circuit to allow the contents of the respective units to be switched on to the CRT monitor. Or, conversely, two independent monitors could be utilized. By this technique, it is relatively easy to combine two units into a system to monitor 16 data bits, a common peripheral and computer configuration.

SECTION VIII

Maintenance Procedures

8.1 Maintenance

This section covers maintenance and disassembly procedures for trouble-shooting and repair of the Model 810-D. Repair is performed with the aid of a trouble-shooting procedure for the unit, the technical description, and the schematic diagram.

Waveform photographs have been included with the schematics to aid service personnel who wish to trouble-shoot to the component level. Additional assistance in a particular problem can be obtained by contacting the Customer Service Department at the factory: Phone (408) 255-9500 TWX 910 338-0226.

In summary, there are two methods of service available:

1. Return the entire unit to the factory or service center for repair.

2. Trouble-shoot the problem to the component level with the aid of the trouble-shooting procedure and schematics or with the aid of factory personnel.

8.2 Trouble-shooting Procedure

The following test equipment will be required to conduct the trouble-shooting procedure:

1. A pulse generator capable of fast rise time(< 5ns) variable width pulses or square waves over the frequency range of .10 Hz to 5.0 MHz and with a variable output of up to 10 volts peak-to-peak into a 50 ohm load.

2. An oscilloscope: 2 channel DC to 100MHz input bandwidth.

If a display device is not normally used with the Model 810-D, an additional oscilloscope or CRT display will be required during the testing period. This latter oscilloscope need only have a 2MHz input bandwidth. Connect the display device to the 810-D outputs as shown in Figure 4.3 Page 19.

8.3 Power Supply

The Power Supply is located on a removable regulator PC Board assembly, mounted to the rear panel. To remove the regulator assembly from the unit, unscrew the (5) five, #4 screws from the top and bottom flanges of the heat sink. Lift the heat sink and pull out of the chassis. The transformer and primary supply filter capacitors are mounted to the chassis and to the main PC Card.

There are four power supplies used in the Model 810-D. They are +15 V, -15 V, -5V and +5 Volts. These power supplies are all series regulated units; utilizing grounded-collector, series-pass transistors and integrated circuit regulators. All four power supplies are equipped with a current limiting feature. If the output of the power supply is shorted or the amount of current flow exceeds that normally used in the Model 810-D, the power supply output voltage drops to zero. During normal operation, the following currents are supplied by the power supplies:

+15 V @126MA	NOTE: Unit in display mode.
-15 V @116MA	During record at fast clock
-5 V @ 72MA	rates, current will increase
+5 V @1.32A	on +5 and -5 supplies.

Voltage adjustments are provided on the +15V and -15V power supplies. The +5 V power supply is referenced to the +15 V power supply and no adjustment of the +5 V is necessary since the two power supplies will track each other. The -5 V power supply is a fixed voltage power supply in that fixed resistors are used to set the output level. Approximately 500MA of current can be drawn from the rear panel connector +5 Volt output without causing an overload.

8.4 Front Panel

The front panel assembly consists of a PC card assembly mounted directly to the front panel. The entire front panel can be removed for service by removing the (4) four #6 nuts from the studs on the front panel. However, a more practical approach is to remove the THRESHOLD, CLOCK INTERVAL, DISPLAY position and TRIGGER LEVEL knobs. Then remove the (6) six #6 screws (3 top and 3 bottom) from the PC card. Remove just the PC card from the unit for service. There are no active components on the front panel assembly and the interconnecting cable plugs into sockets at the top left corner of the PC card. When removing the PC card from the front panel, care must be exercised not to damage the LEDs or the connecting wire to the external clock BNC connector. The input BNC connectors are mounted to a separate bracket which is bolted directly to the chassis.

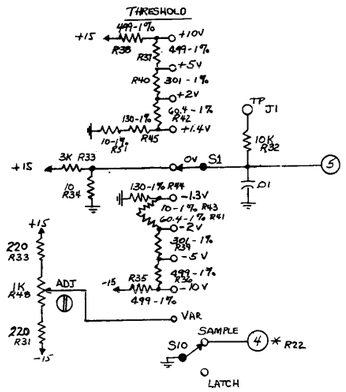
8.5 Main PC Assembly

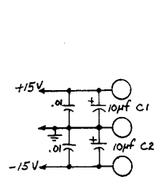
The Main PC assembly is the heart of the 810-D. All data storage and control functions are performed on this card. It is recommended that this card not be removed for service. In order to trouble-shoot the main PC assembly it is recommended that the service personnel determine whether the problem is located in the data section or the control section. Once this determination has been made refer to the technical description and the waveform photographs on the schematics for trouble-shooting.

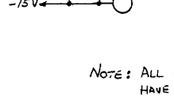
SECTION IX

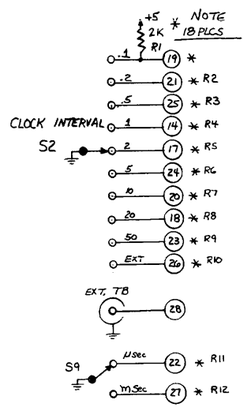
Schematics and Assembly Drawings

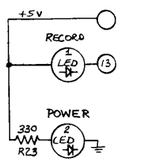
9.0 List of Drawings

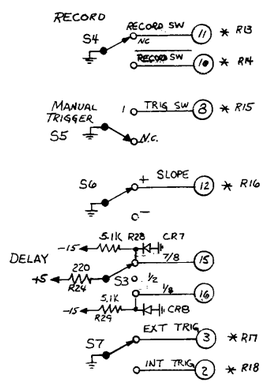


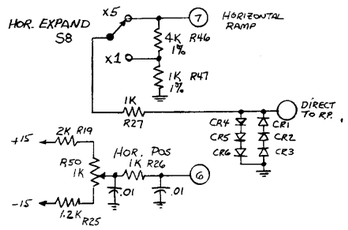






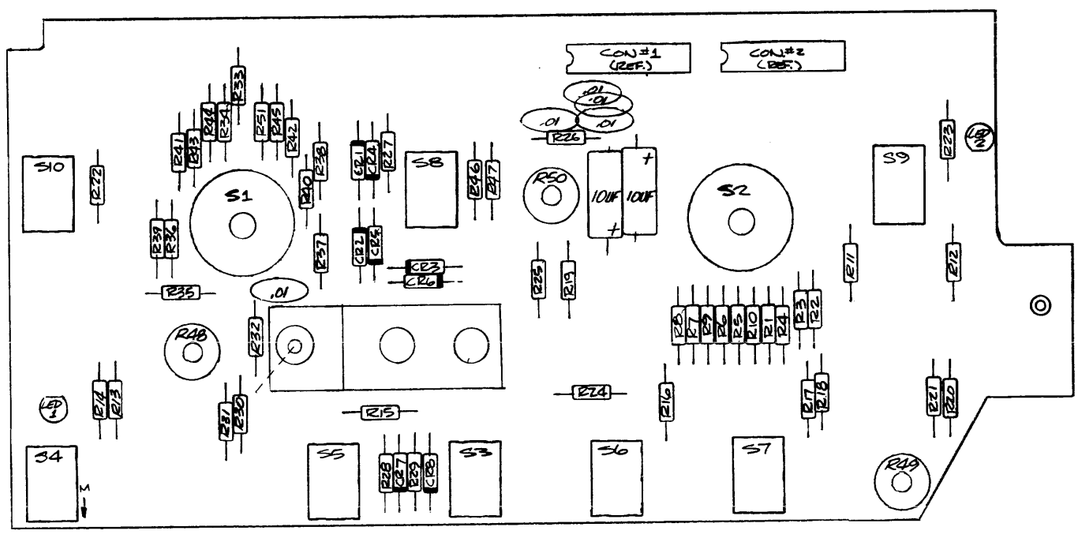


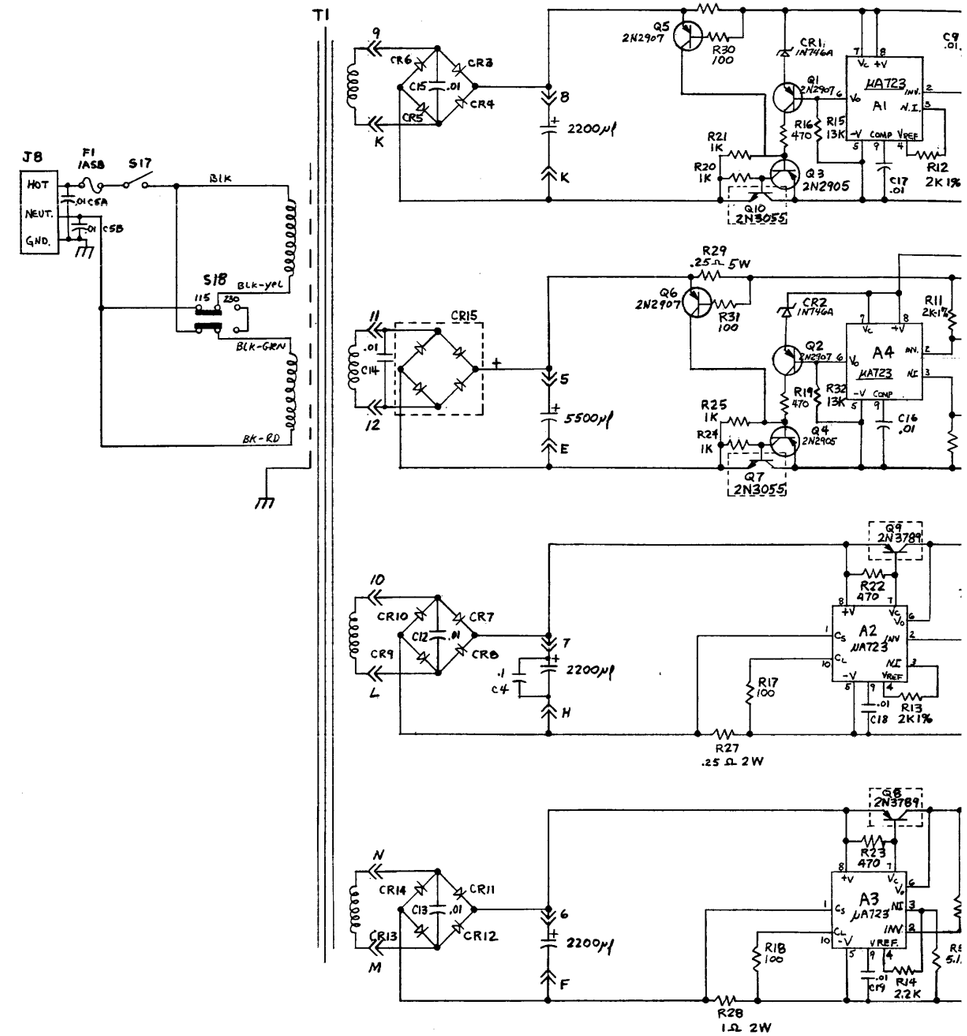


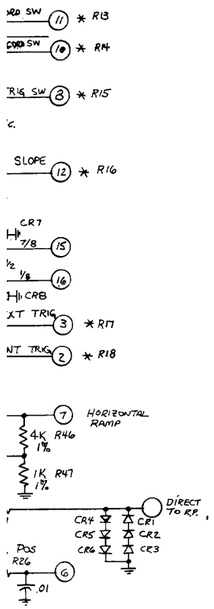


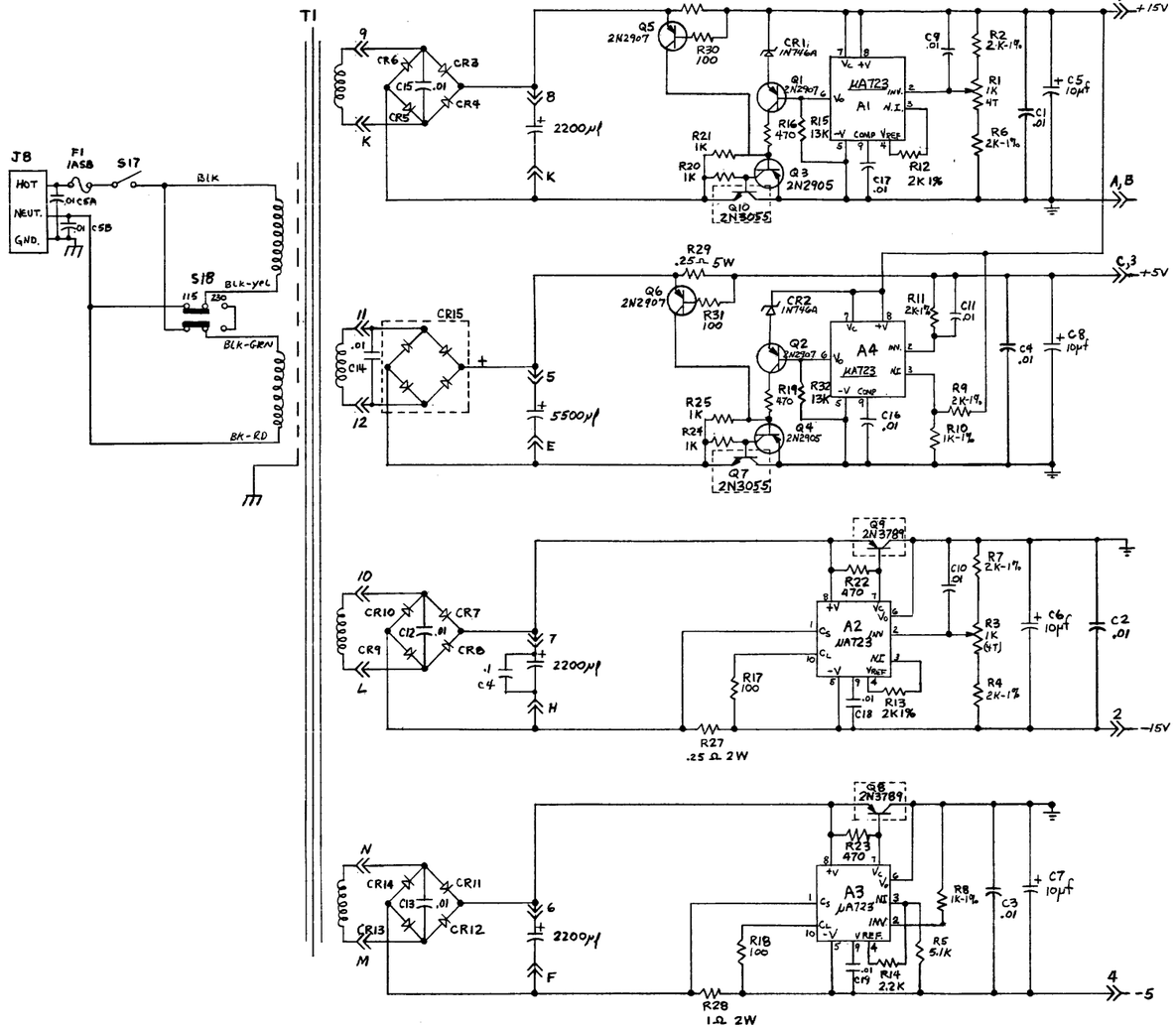
NOTE: ALL LOCACTIONS MARKED * (19 PLACES) HAVE 2K PULL-UP RESISTORS TO +5V.

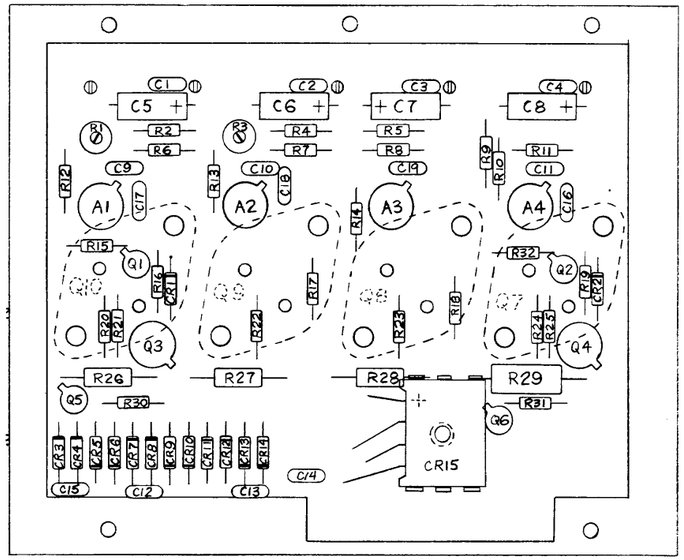
ALL PIN NUMBERS REFER TO MOTHER BOARD

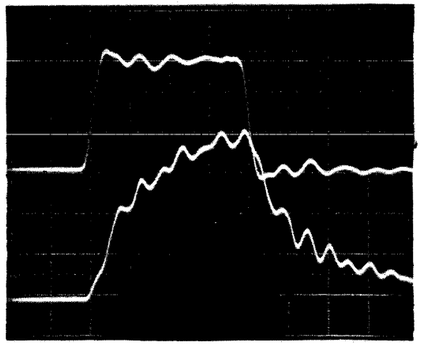




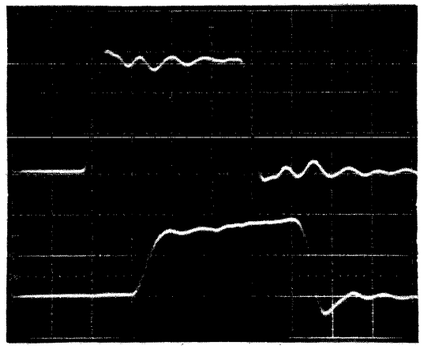

RD SW
11
* R13
CORD SW
10
* R14
RIG SW
8
* R15
SLOPE
12
* R16
CR7
7/8
15
1/2
1/8
16
CR8
XT TRIG
3
* R17
NT TRIG
2
* R18
7
HORIZONTAL RAMP
4K R46 1%
1K R47 1%
DIRECT TO RP
CR4
CR5
CR6
CR1
CR2
CR3
POS
R26
6
.01


T1
J8
HOT
NEUT.
GND.
F1
1ASB
.01 CSA
.01 CSB
S17
BLK
S18
115
230
BLK-YEL
BLK-GRN
BK-RD
9
CR6
CR3
C15 .01
CR5
CR4
K
8
2200μf
K
R26
1Ω 2W
Q5
2N2907
R30
100
CR1
1N746A
Q1
2N2907
R16
470
R15
13K
R21
1K
R20
1K
Q3
2N2905
Q10
2N3055
μA723
A1
C9
.01
R2
2K-1%
R1
1K
6T
R6
2K-1%
C1
.01
C5
10μf
R12
2K 1%
C17
.01
1
+15V
A,B
R29
.25Ω 5W
Q6
2N2907
R31
100
CR2
1N746A
Q2
2N2907
R19
470
R32
13K
R25
1K
R24
1K
Q4
2N2905
Q7
2N3055
μA723
A4
C11
.01
R11
2K-1%
R9
2K-1%
R10
1K-1%
C16
.01
C4
.01
C8
10μf
C,3
+5V
11
CR15
C14
.01
12
5
5500μf
E
10
CR10
CR7
C12 .01
CR9
CR8
L
7
2200μf
.1
C4
H
Q9
2N3789
R22
470
μA723
A2
C10
.01
R7
2K-1%
R3
1K
6T
R4
2K-1%
C6
10μf
C2
.01
2
-15V
R17
100
R13
2K1%
C18
R27
.25Ω 2W
N
CR14
CR11
C13 .01
CR13
CR12
M
6
2200μf
F
Q8
2N3789
R23
470
μA723
A3
R8
1K-1%
C3
.01
C7
10μf
R18
100
R14
2.2K
R5
5.1K
C19
R28
1Ω 2W
4
-5

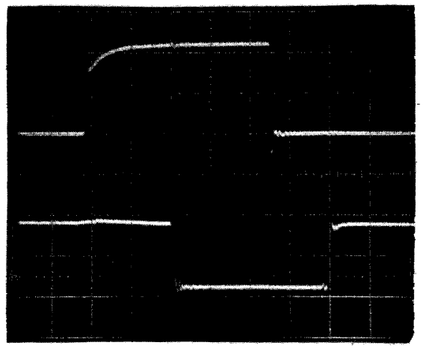

C1
C5
C2
C6
C3
C7
C4
C8
R1
R3
R2
R4
R5
R6
R7
R8
R9
R10
R11
R12
C9
C10
C18
C19
C17
C16
A1
A2
A3
A4
R13
R14
R15
Q1
R16
CR1
R32
Q2
R19
CR2
R20
R21
R22
Q3
R23
CR3
R24
R25
CR4
Q4
R26
R27
Q5
R30
R28
Q6
R31
R29
Q10
Q9
Q8
Q7
CR5
CR6
CR7
CR8
CR9
CR10
CR11
CR12
CR13
CR14
C15
C12
C13
C14
CR15



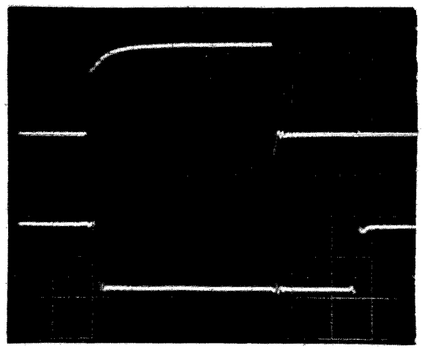
1. Scope: Vert. CH1 1v/div CH2 2v/div
   Horz. .01μ sec/div
   Trigger: Int CH1 + slope
   Puse generator: 2V + pulse 40ns wide



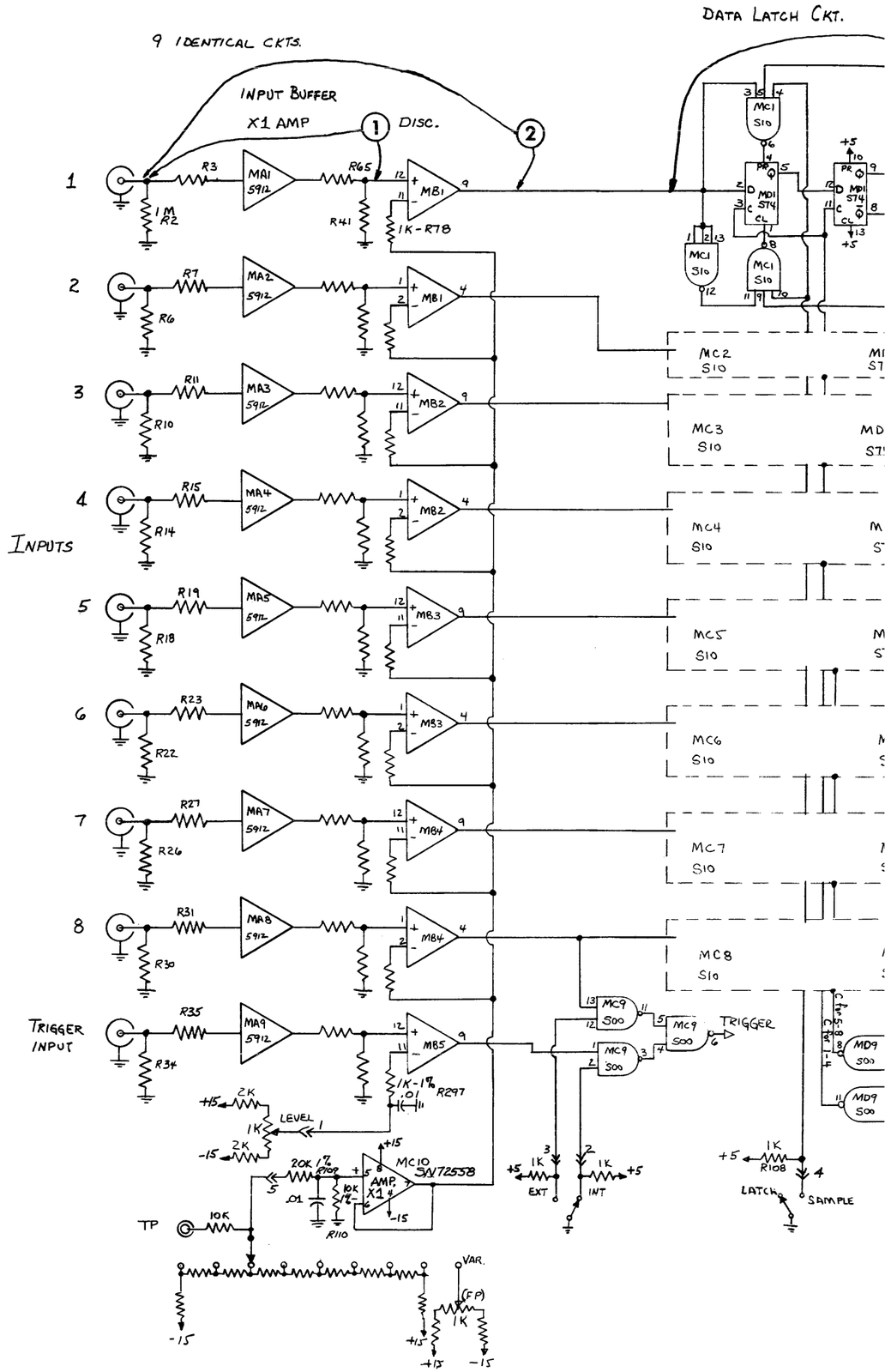
2. Scope: Vert. CH1 1v/div CH2 2v/div
   Horz. .01μ sec/div
   Trigger: Int CH1 + slope
   Pulse generator: 3V + pulse 40ns wide

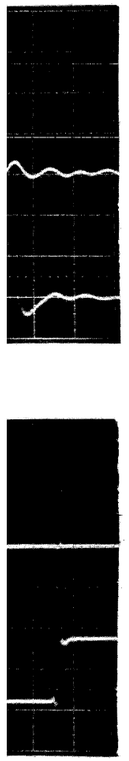


3. Scope: Vert. 2v/div Horz. .1μ sec/div
   Trigger: Int CH1 + slope
   Puse generator: 3V + pulse 40ns wide
   810-D: Sample mode, in record, clock
   interval .1μ sec.



4. Scope: Vert. 2v/div Horz. .1μ sec/div
   Trigger: Int CH1 + slope
   Pulse generator: 3V + 40 nsec side
   810-D: Latch mode, in record, clock
   interval .1μ sec.





9 IDENTICAL CKTS.

INPUT BUFFER

X1 AMP

DISC.

DATA LATCH CKT.

INPUTS

TRIGGER INPUT

DATA 1

DATA 2

DATA 3

DATA 4

DATA 5

DATA 6

DATA 7

DATA 8

TO MEMORY INPUT LOGIC

TRIGGER

TIME BASE

LEVEL

TP

VAR. (FP)

EXT

INT

LATCH

SAMPLE

MC10 SN72558 AMP. X1

DETAIL of BUFFER & DISCRIMINATOR

NE521

TO LATCH

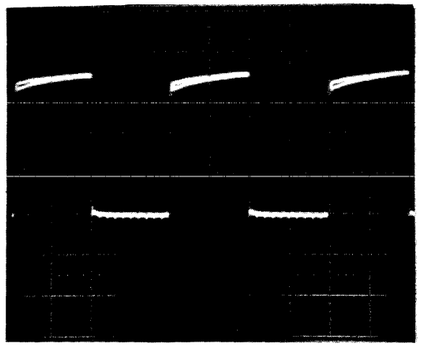
TO BIAS

TO BUFFER

NOTE - SYMBOL ⏚ INDICATES WIRE TO FRONT OR REAR PANEL.

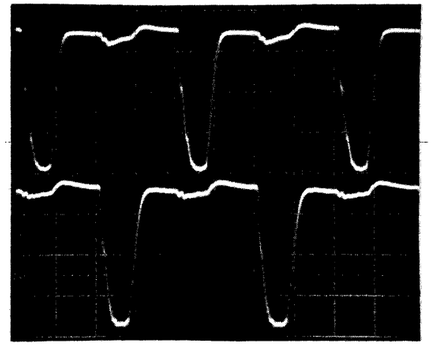
SCHEMATIC - MAIN PC BOARD

PART 1 of 4 PAGE 56

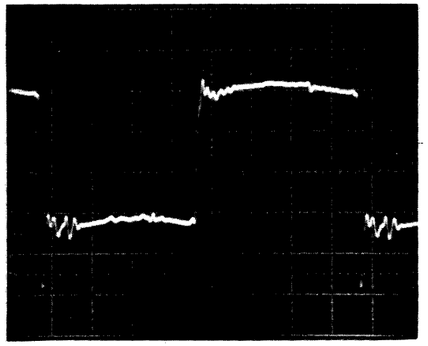


1. Scope: Vert. 1v/div Horz. .5μ sec/div
   Trigger: Int + slope
   810-D: In display mode

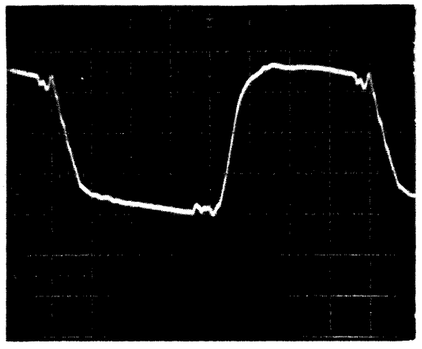
2. Scope: Vert. 1v/div Horz. .1μ sec/div
   Trigger: Int CH1 + slope
   810-D: In Record, clock Int. .2μ sec.



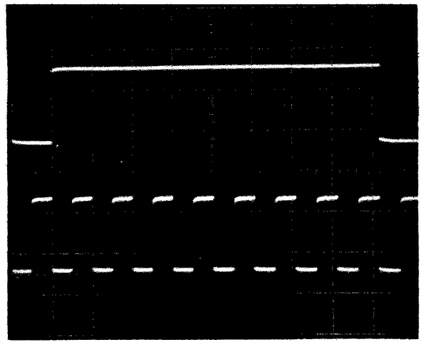
3. Scope: Vert. 5v/div Horz. .1μsec/div
   Trigger: Int CH1 + slope
   810-D: in record, clock int. .2μ sec.



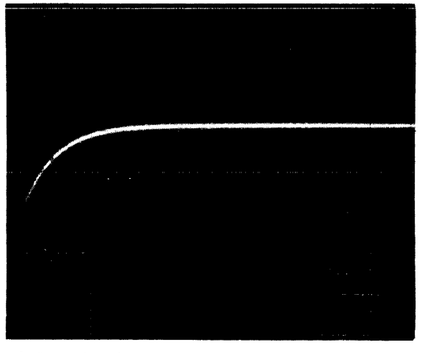
4. Scope: Vert. 1v/div Horz. .05μsec/div
   Trigger: Int - slope
   810-D: In record, clock int. .2μsec, TB
   out connected to CH1 input.



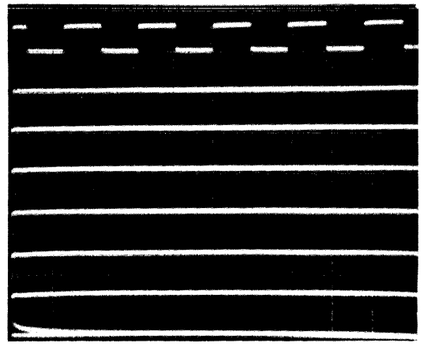
5. Scope: Vert. 1v/div Horz. .05μsec/div
   Trigger: int - slope
   810-D: in record, clock int. .2μsec, TB
   out connected to CH1 input.



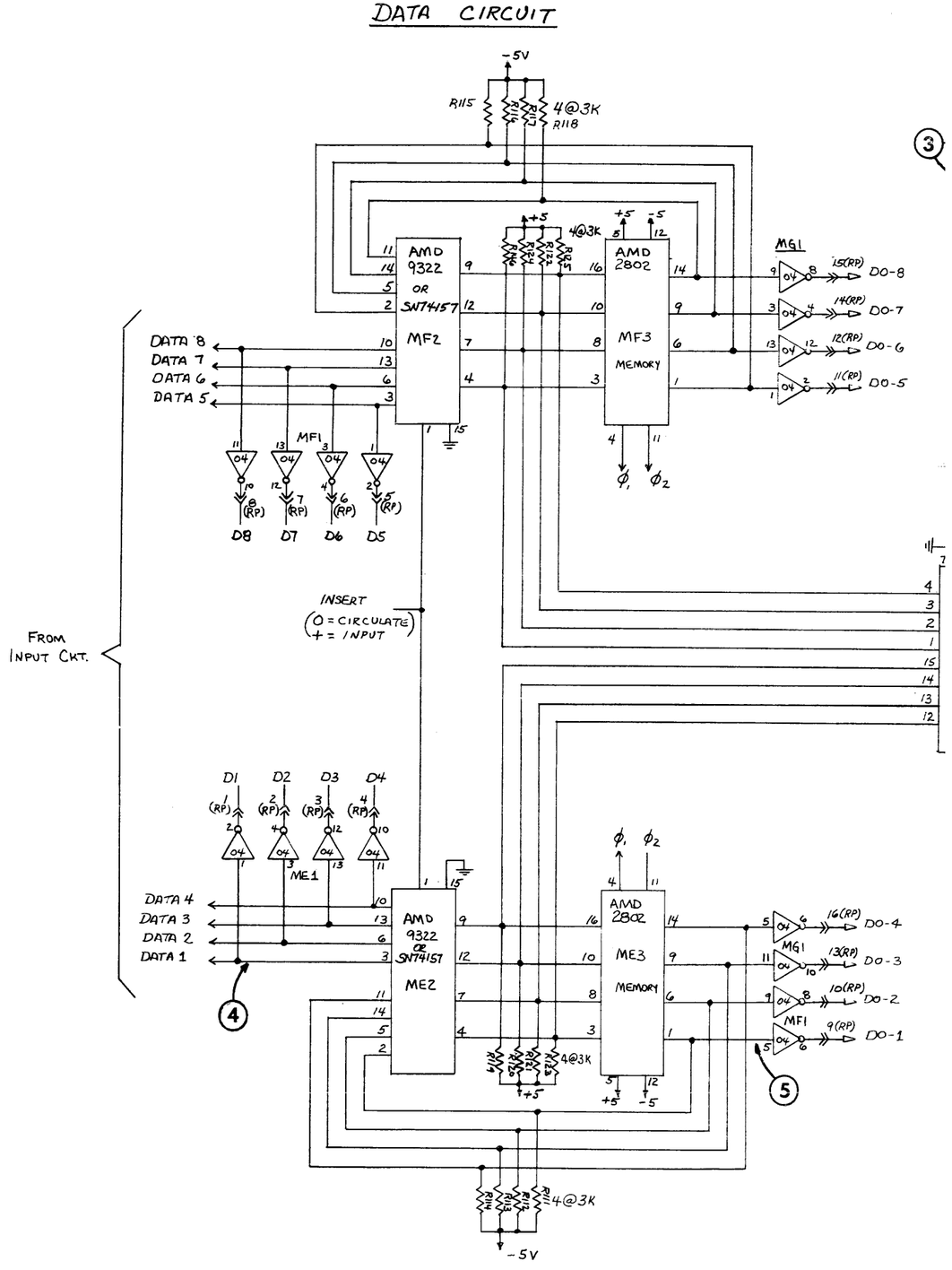
6. Scope: Vert. 2v/div Horz. .5msec/div
   Trigger: Int CH1 - slope
   810-D: In display mode



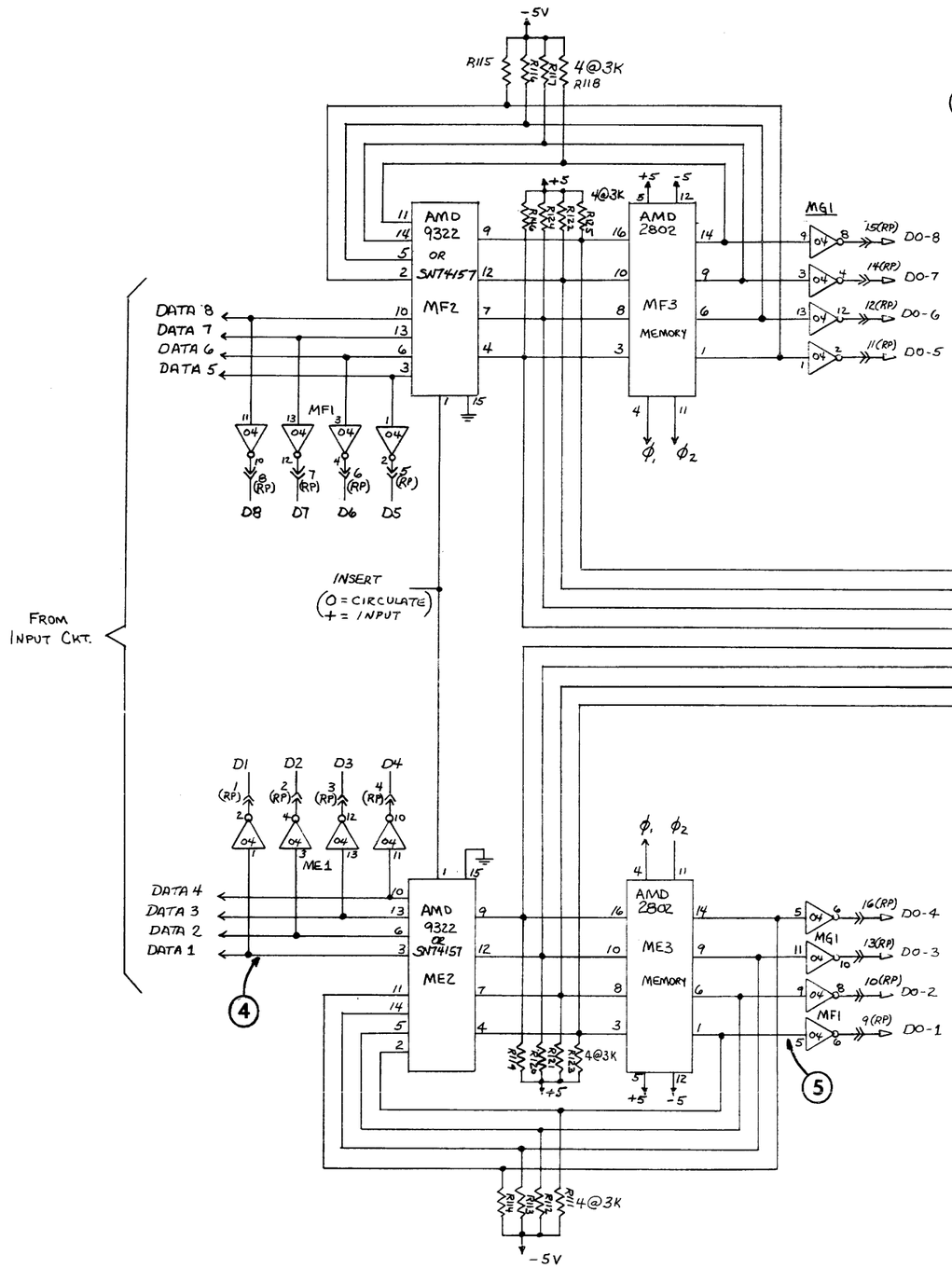
7. Scope: Vert. 1v/div Horz. 1μsec/div
   Trigger: Int. - slope
   810-D: in Display Mode



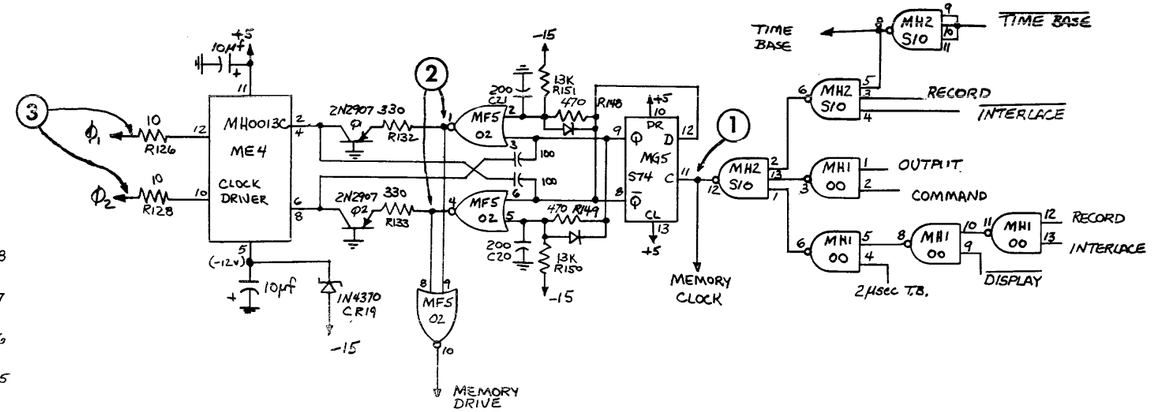
8. Scope: Vert. .1v/div Horz. 50 μsec/div
   Trigger: on "Z" output
   810-D: in Display. Data stored in CH1



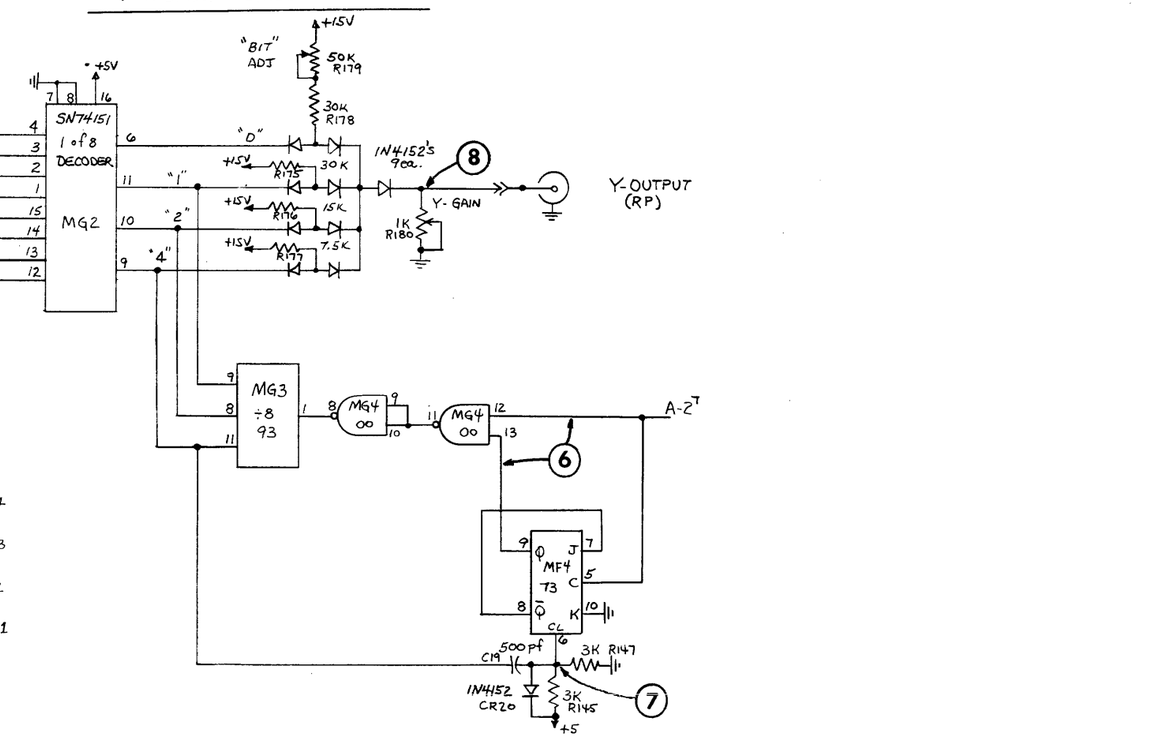
DATA CIRCUIT

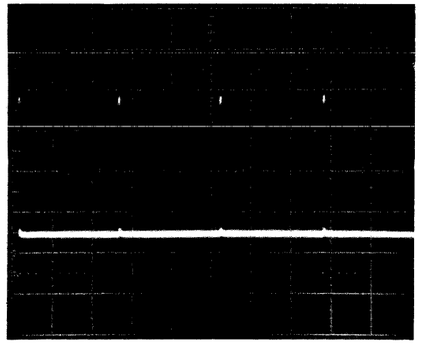


CLOCK DRIVE CIRCUIT

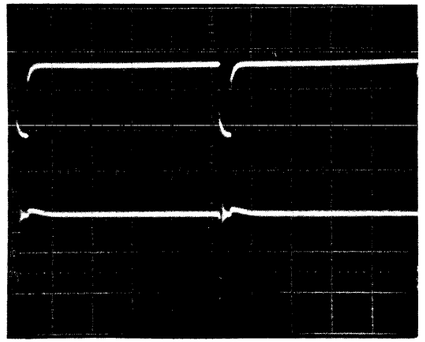


Y-DISPLAY CIRCUIT

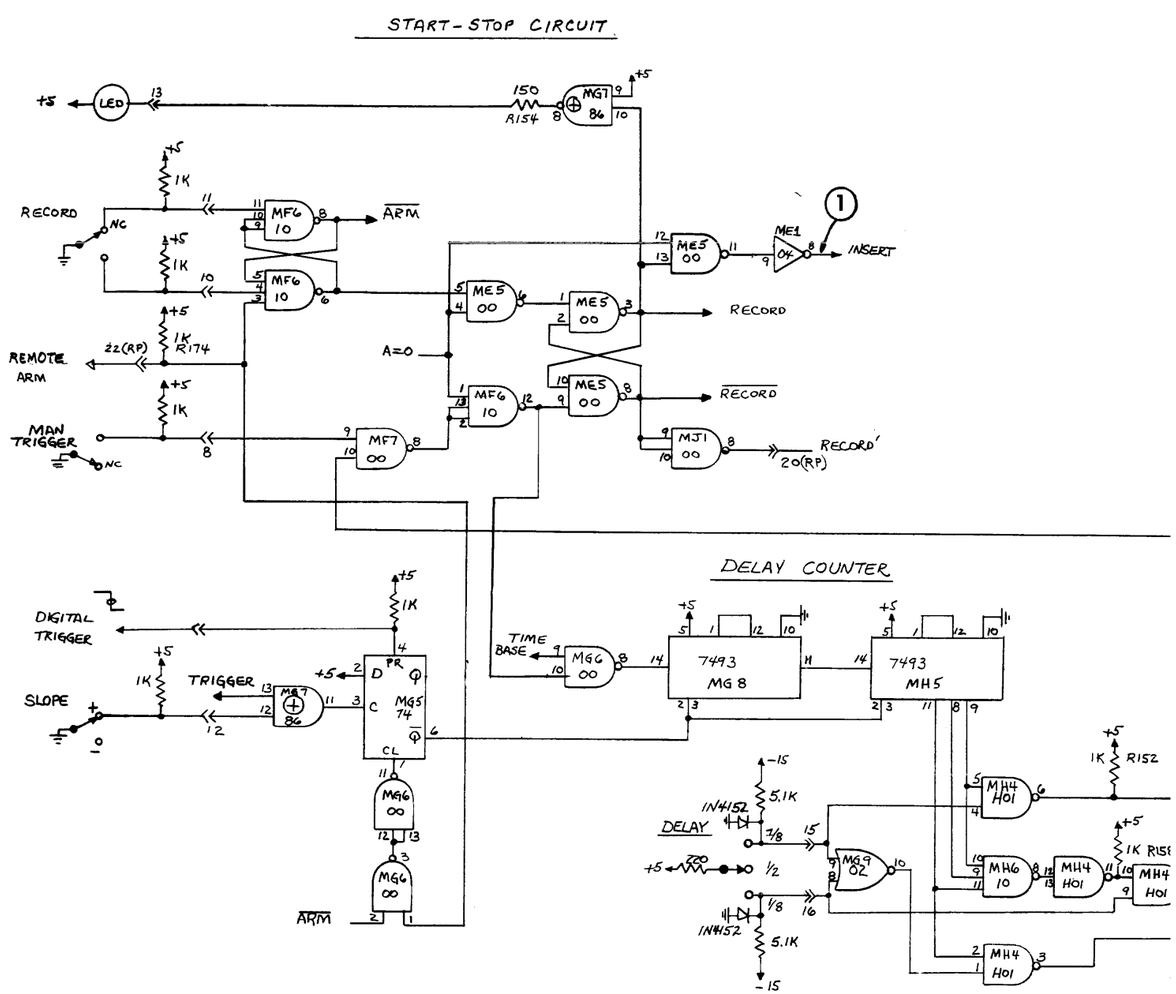




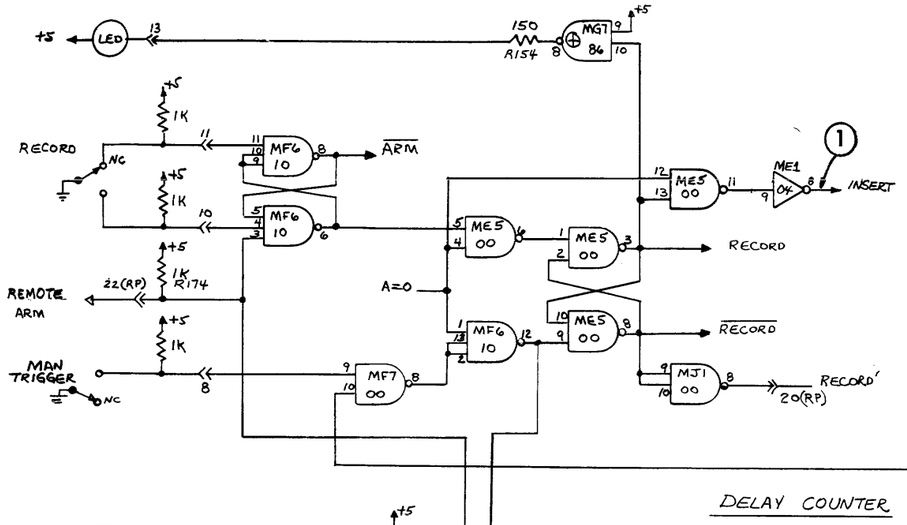
1. Scope: Vert. 1v/div Horz. .2msec/div
   Trigger: Int + slope
   810-D: In record, clock int. lmsec



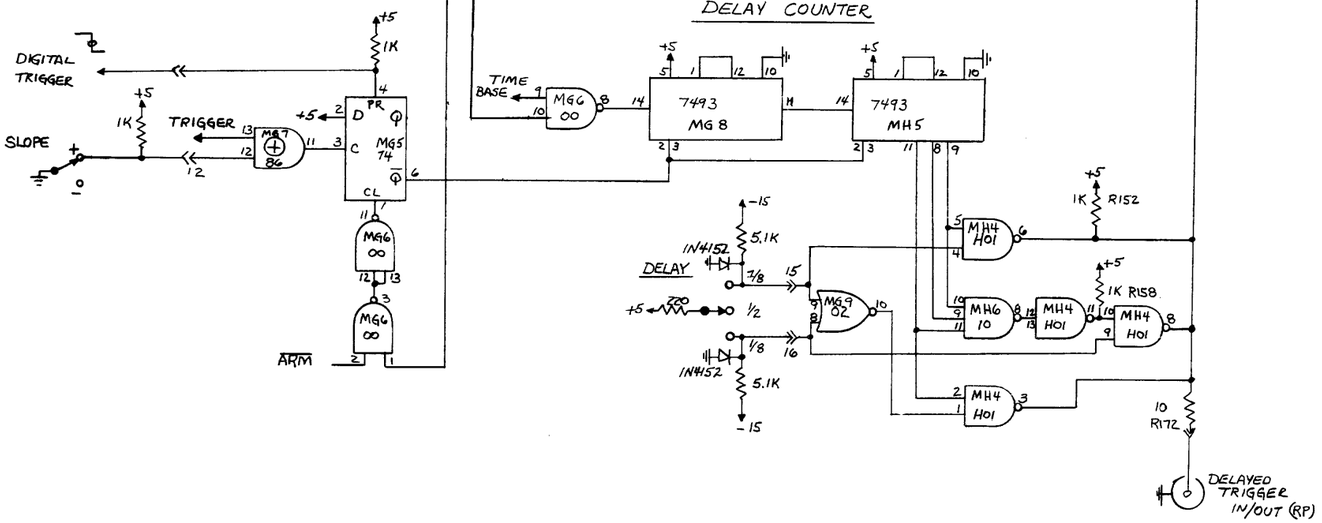
2. Scope: Vert. 2v/div Horz 2µsec/div
   Trigger: Int + slope
   810-D: in output. "Output request" grounded CMD rate 10µsec.



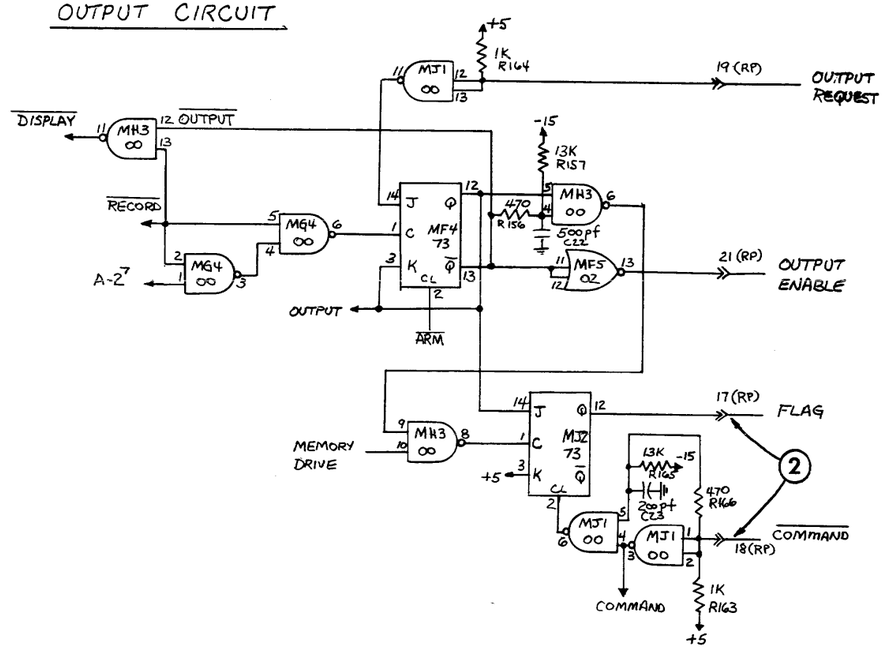
START-STOP CIRCUIT

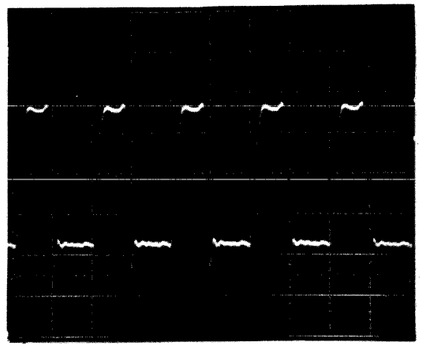


DELAY COUNTER

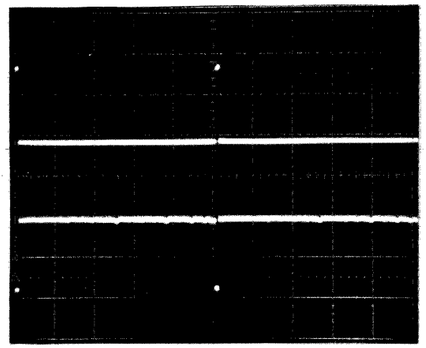


OUTPUT CIRCUIT

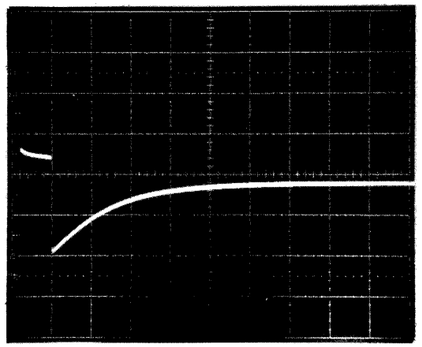




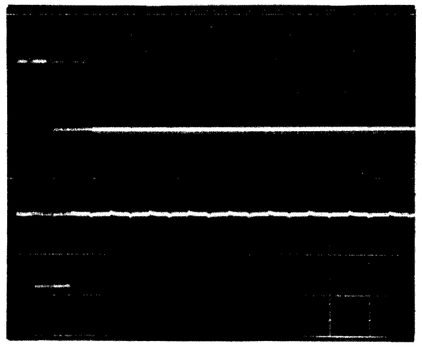
1. Scope: Vert. 1v/div Horz. .05μsec/div
   Trigger: Int + slope



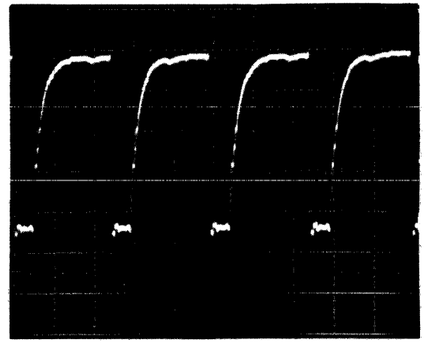
3. Scope: Vert. 2v/div Horz. .1msec/div
   Trigger: Int CH1 + slope
   810-D: in Display Mode.



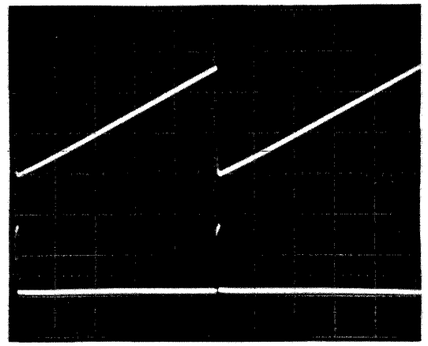
5. Scope: Vert. 1v/div Horz. 10μsec/div
   Trigger: Int + slope
   810-D: In display mode



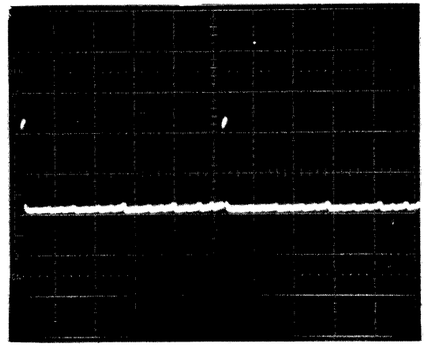
7. Scope: Vert 2v/div Horz. 2μsec/div
   Trigger: CH1 + slope
   810-D: in Record. Clock int. 1msec.



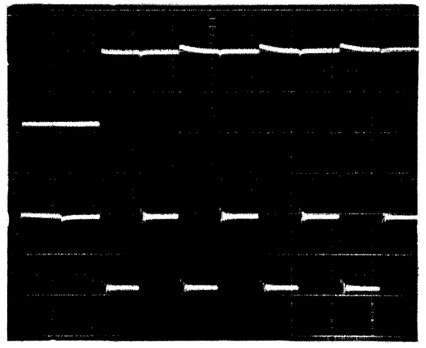
2. Scope: Vert. 1v/div Horz. .2msec/div
   Trigger: Int - slope
   810-D: Clock inteval .5μsec.



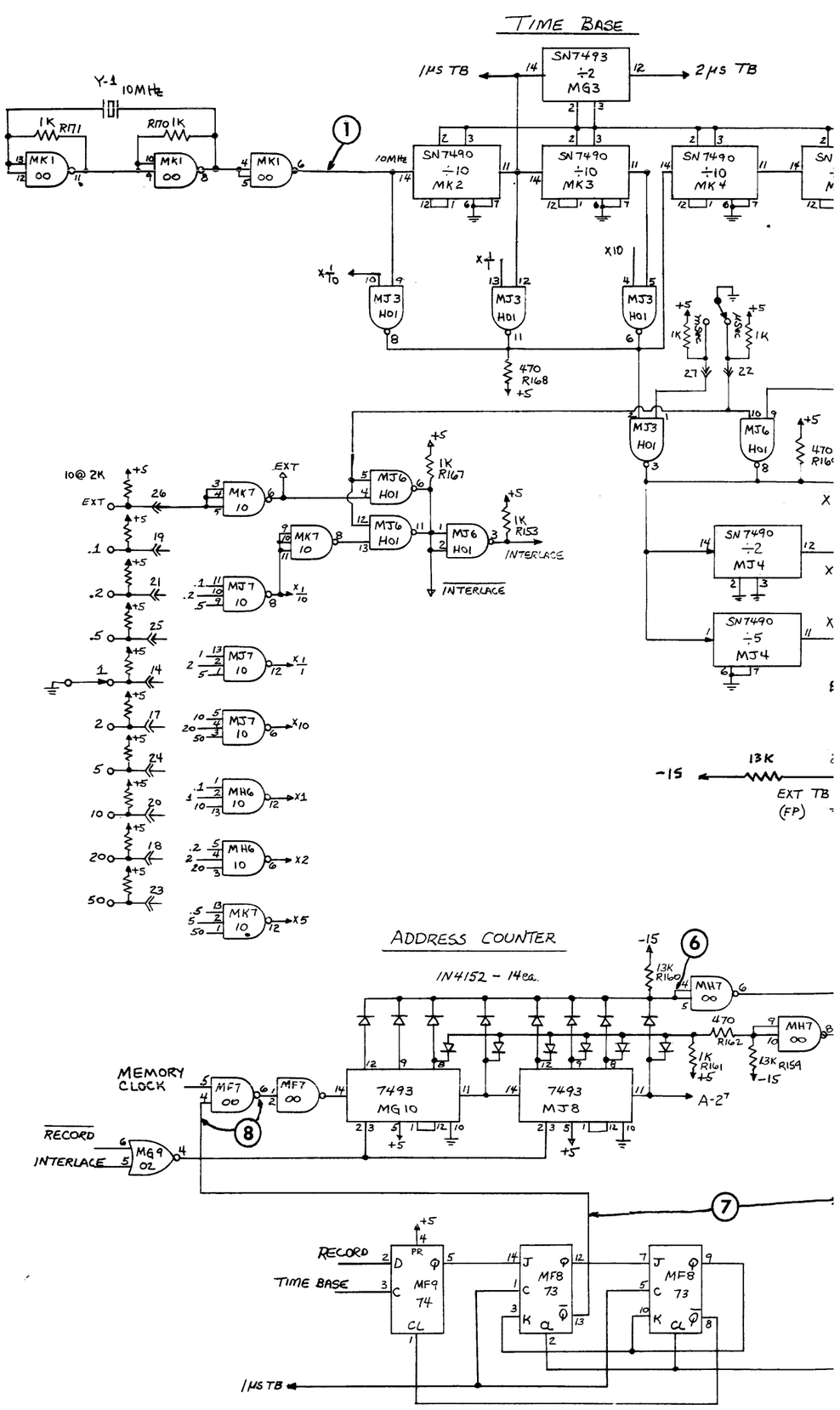
4. Scope: Vert. 2v/div Horz. .1msec/div
   Trigger: Int CH2 + slope
   810-D: in Display Mode

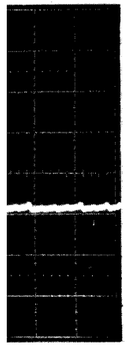


6. Scope: Vert. 1v/div Horz. .1msec/div
   Trigger: Int + slope
   810-D: in display

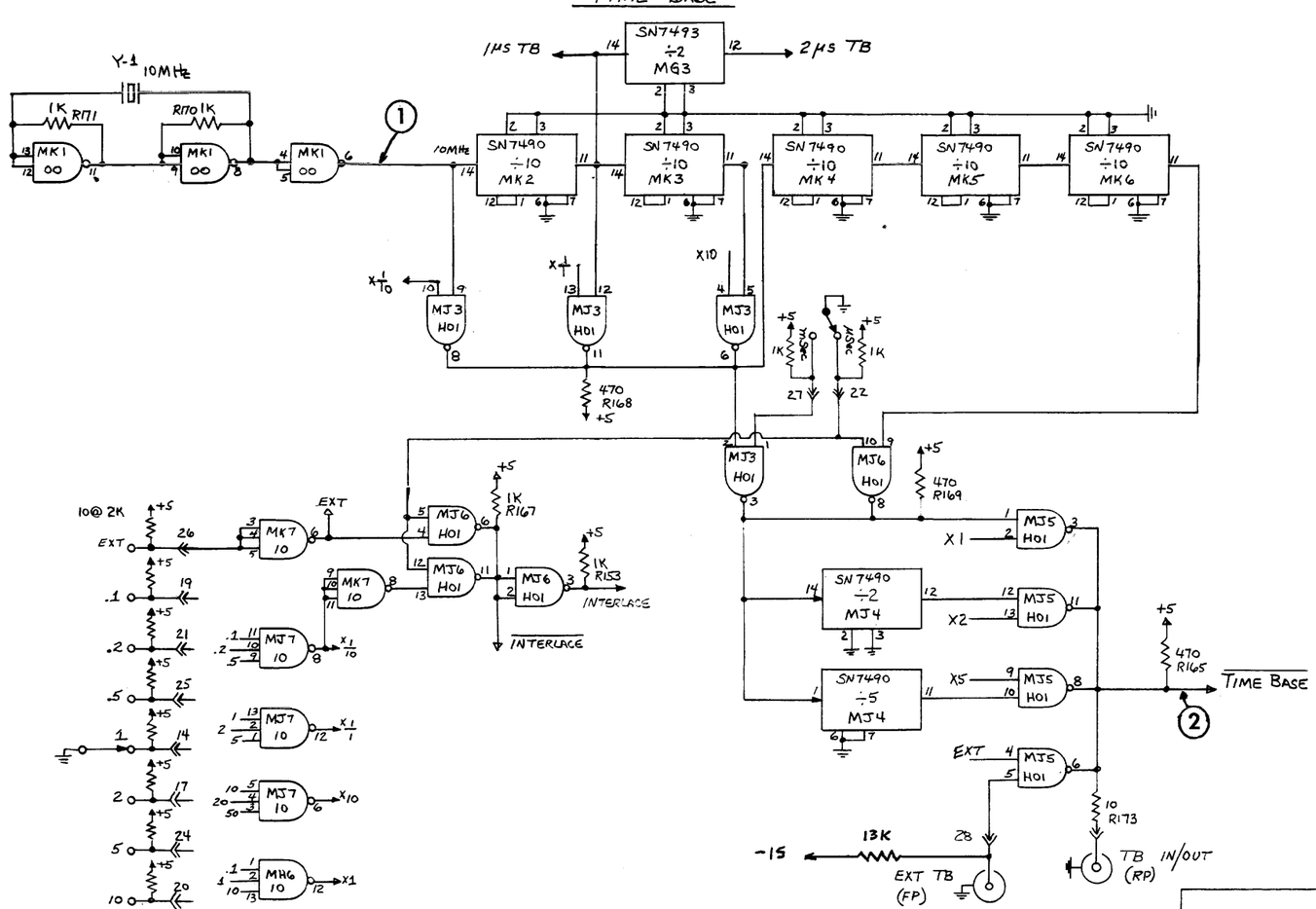


8. Scope: Vert. 2v/div Horz. 1μsec/div
   Trigger: Int. CH1 - Slope
   810-D: In record, clock Int. 1msec.

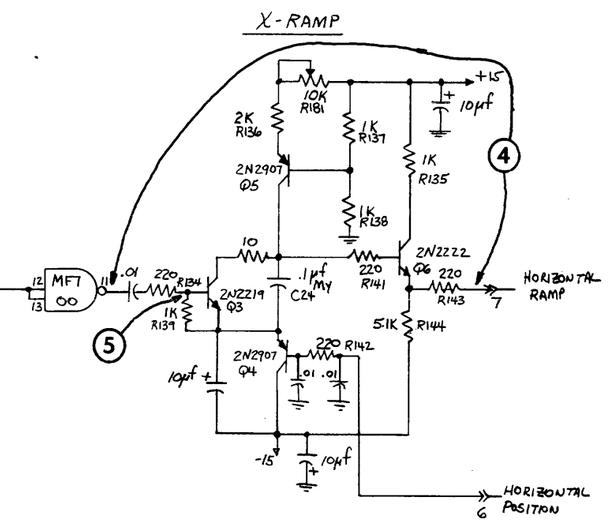




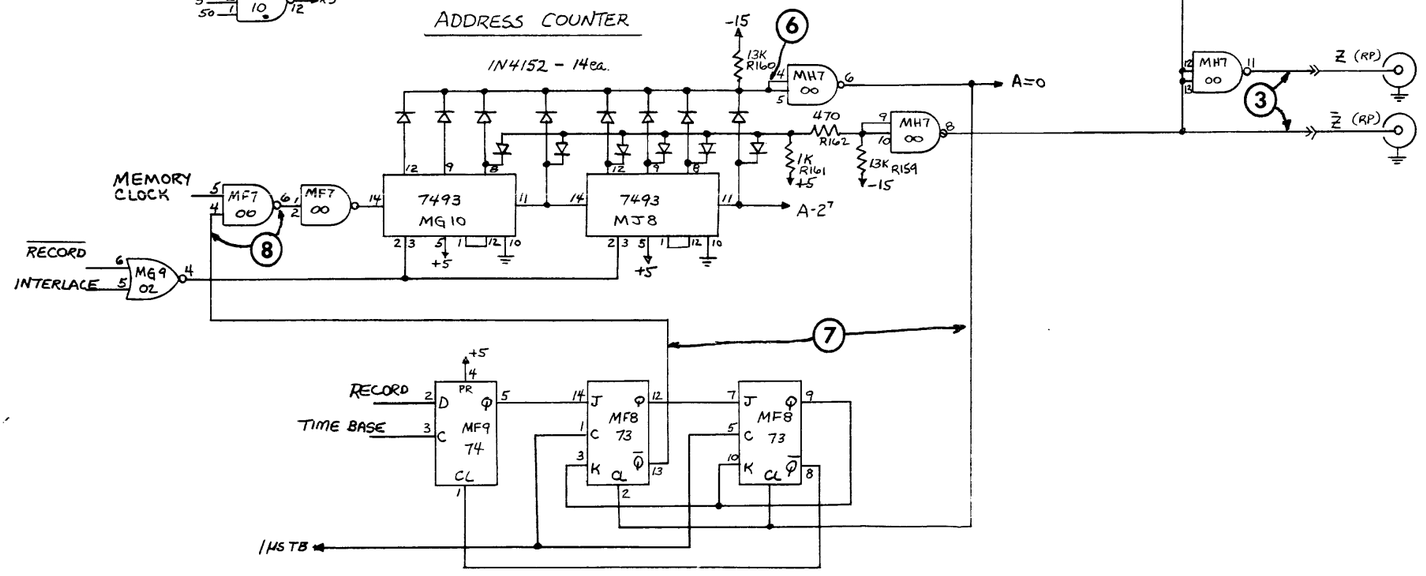
TIME BASE

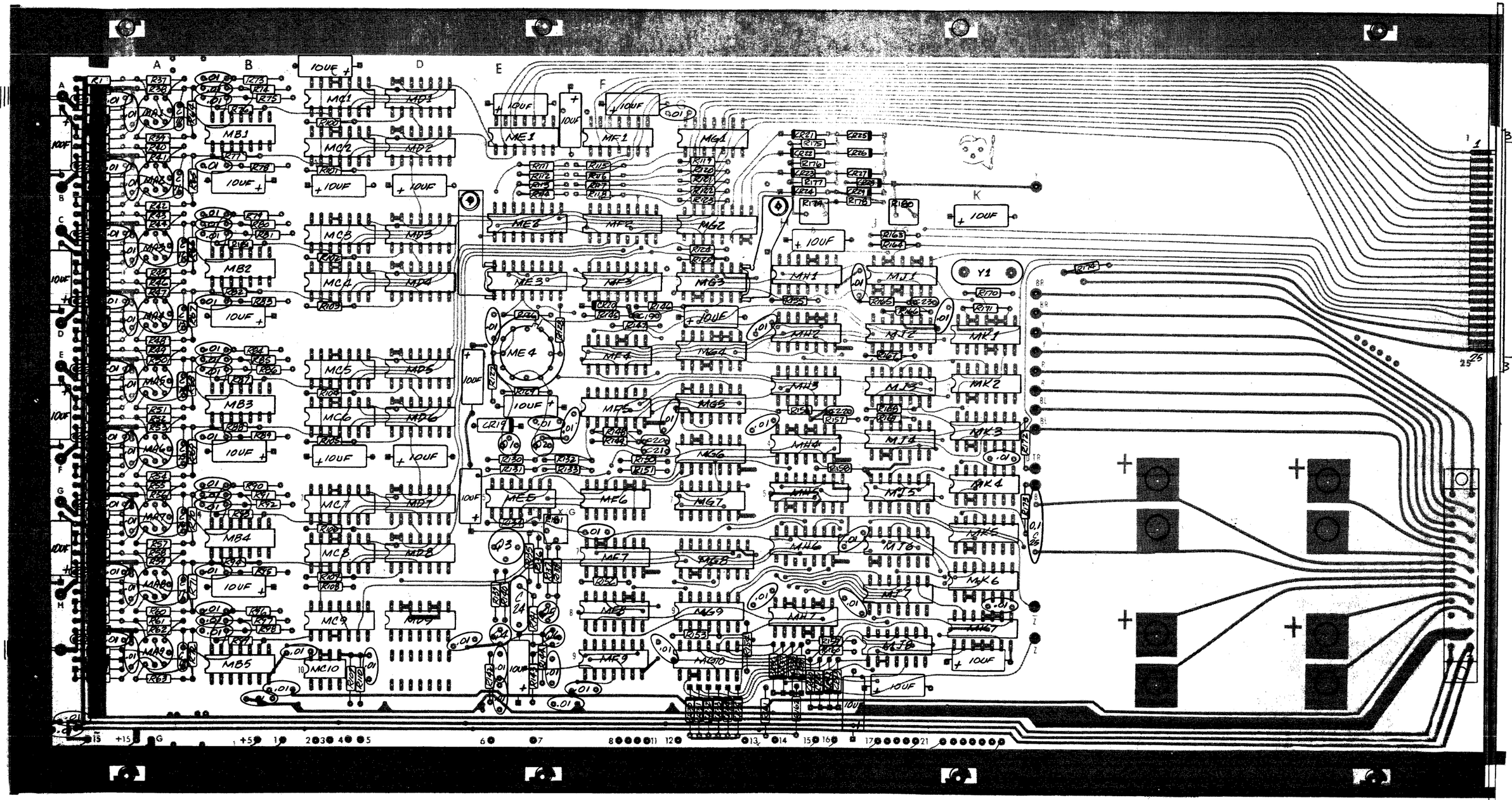


X-RAMP



ADDRESS COUNTER





ASSEMBLY - MAIN PC BOARD