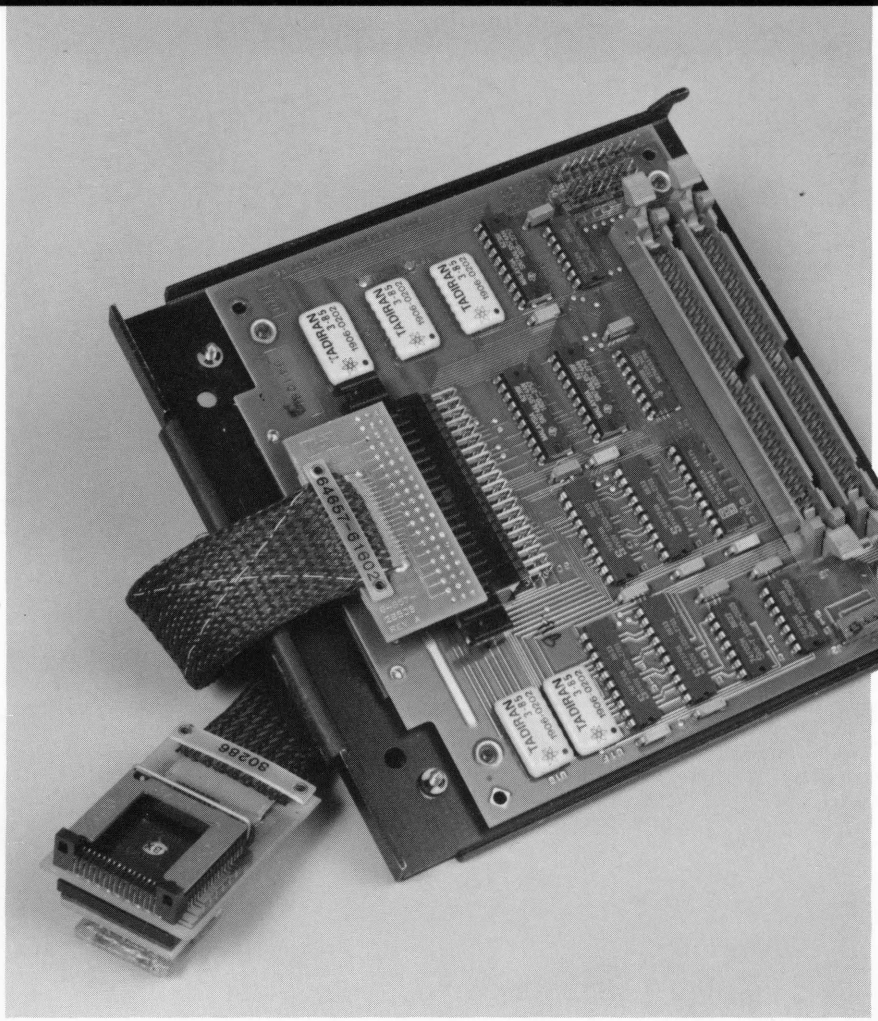
HP 10312D
Intel 80286 Preprocessor
for the HP 1650A and HP 16510A Logic Analyzers

Operating Manual



HEWLETT PACKARD

HP 10312D
Intel 80286 Preprocessor
Operating Manual

for the HP 1650A and HP 16510A Logic Analyzers

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Pages	Effective Date

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Analyzing the Intel 80286 1

Introduction

The HP 10312D Preprocessor Interface Module, when installed in the HP 10269C General Purpose Probe Interface, provides a complete interface between an 80286 target system and the HP 1650A or HP 16510A Logic Analyzer. The interface module connects the signals from the 80286 target microprocessor to the logic analyzer inputs and generates all status and clock signals required by the software for inverse assembly of the 80286 instruction set.

The 80286 Interface Module operates in the bus mode. In the bus mode, all bus cycles, including prefetches, are sent to the logic analyzer as they occur. All coprocessor (80287) cycles on the local bus will also be captured.

The 80286 configuration software on the flexible disc sets up the format specification of the logic analyzer for compatibility with the 80286 microprocessor. It also loads the inverse assembler routine for obtaining displays of 80286 data in assembly language mnemonics. The interface module specifications are given in chapter 2.

Installation Overview

1. Install the 80286 Preprocessor (HP 10312D) into the HP 10269C Probe Interface (see page 1-4).

2. Connect the 80286 preprocessor cable to the target system (see page 1-6).

3. Plug the logic analyzer probes into the probe interface as follows:

HP 1650A and 16510A Pod	(into)	HP 10269C Connector
1		1
2		2
3		3

4. Load the logic analyzer configuration and inverse assembler by loading the file C80286_I from the inverse assembler disc (see page 1-12).

Equipment Supplied

The HP 10312D Preprocessor and Inverse Assembler consists of the following:

- The preprocessor hardware, which includes the interface circuit card and cable assembly;
- The inverse assembly software on a 3.5-inch disc; and
- This operating manual.

Equipment Required

The minimum hardware for state analysis of a 80286 target system consists of the following:

- An HP 1650A or HP 16510A Logic Analyzer;
- The HP 10269C General Purpose Probe Interface, which connects the preprocessor to the logic analyzer; and
- The 80286 Preprocessor and Inverse Assembler (HP 10312D).

Installing the HP 10312D in the HP 10269C

The HP 10269C routes the signals from the HP 10312D Preprocessor and provides the correct mechanical connections for the logic analyzer probes. To install the HP 10312D to the HP 10269C:

1. Install the HP 10312D Interface Module Card on the underside of the HP 10269C General Purpose Probe Interface Pod (see figure 1-1).

2. Insert the metal tabs of the interface card in the slots of the pod.

3. Connect the two pod internal cables to the interface card.

4. Gently fold the interface card into the pod and fasten the cable end of the interface card to the pod with the two captive screws on the interface card.

CAUTION

To prevent equipment damage, be sure to remove power from both the logic analyzer and the target system whenever the interface module or microprocessor is being connected or disconnected.

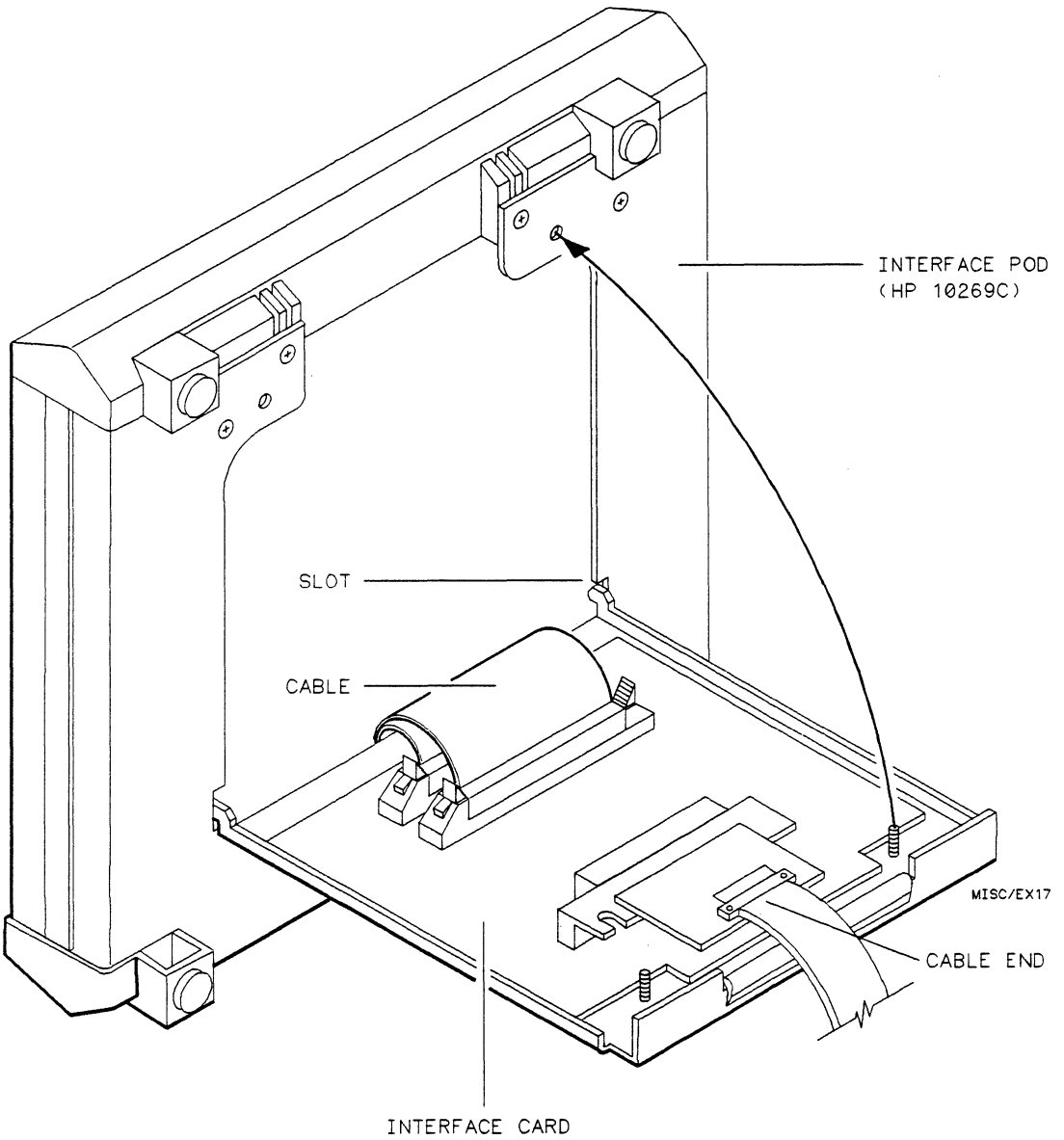

Figure 1-1. Installing the HP 10312D in the HP 10269C

Connecting to the Target System

The interface cable microprocessor connector will connect directly to a PGA socket on the target system or, with the adapter supplied, connect to an LCC style socket.

CAUTION

PROTECT AGAINST STATIC DISCHARGE

The interface module contains devices that are susceptible to damage by Electrostatic Discharge (ESD). Therefore, precautionary measures should be taken before handling the microprocessor connector attached to the end of the interface cable in order to avoid damaging the internal components of the interface module with static electricity.

Do not install the microprocessor connector of the interface module in the target microprocessor socket when power is applied to the target system. The interface module may be damaged if power is not removed from the target system prior to installation.

Installing the Interface Cable in a PGA Socket Assembly.

To connect the microprocessor connector to the target system:

1. Remove the 80286 microprocessor from the target system microprocessor socket.

2. Store the microprocessor in a protected environment.

3. Place the interface connector (see figure 1-2), attached to the end of the cable from the interface module, in the target system microprocessor socket.

CAUTION

Take care to align the interface connector with the target system socket so that all microprocessor contacts are making contact. Also, take care to note the position of pin 1 on both the connector and socket prior to inserting the connector in the socket.

Note

If necessary, the socket protectors may be removed from the top and bottom of the interface connector to reduce capacitance or to improve clearance by providing a lower profile. Their removal, however, increases the risk of damaging a pin or trace on the interface connector, so remove the connectors only when absolutely necessary.

4. Place the microprocessor in the socket pins on top of the interface connector.

Note

For easier installation and removal of the microprocessor chip, first install a 68-pin 11-by-11 ZIF socket in the socket pins on top of the interface connector. Then install the microprocessor chip in the ZIF socket.

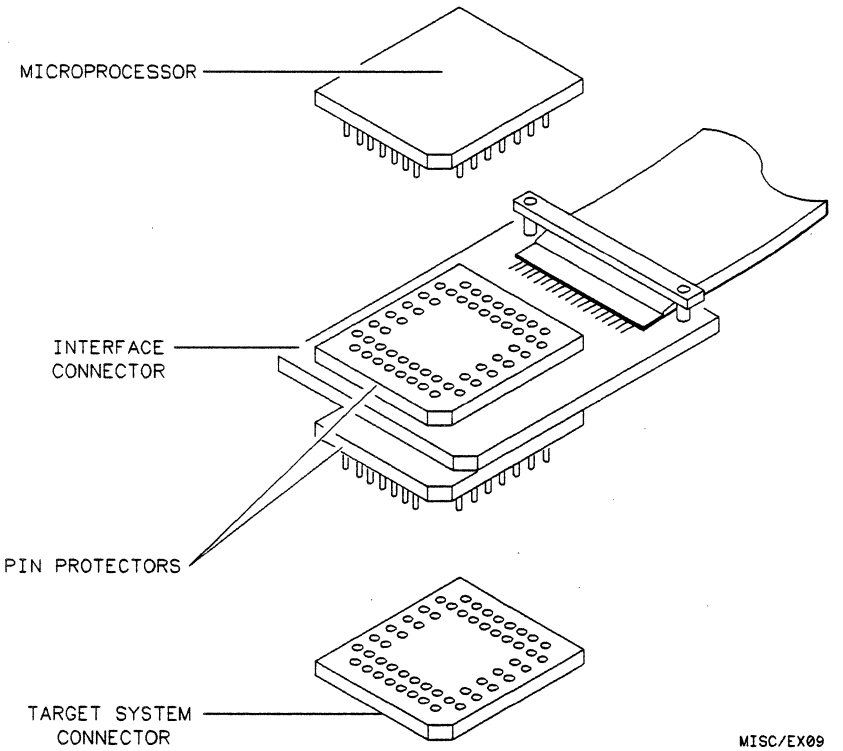

Figure 1-2. Installing the Interface Cable in the PGA Socket

Installing the Interface Cable in an LCC Socket Assembly.

The LCC adapter supplied with the interface is designed to plug into an IDT 3M Textool socket assembly (part no. 268-5400-52) or equivalent socket assembly.

To connect the microprocessor connector to the target system LCC socket assembly:

1. Remove the 80286 microprocessor from the target system microprocessor socket.

2. Store the microprocessor in a protected environment.

3. Place the LCC adapter in the target system microprocessor socket (see figure 1-3).

CAUTION

Take care to align the interface connector with the adapter and the adapter with the target system socket so that all microprocessor contacts are making contact. Also, take care to note the position of pin 1 on the interface connector, LCC adapter, and target system socket prior to connecting them.

4. Install the U-shaped IC retainer on top of the bottom board of the LCC adapter and secure it by swinging the swivel lock up and over the end of the U-shaped IC retainer.

5. Place the interface connector, attached to the end of the cable from the interface module, in the LCC adapter socket.

6. Place a PGA style 80286 microprocessor on top of the interface cable connector.

Note

If a PGA style 80286 microprocessor chip is unavailable, an LCC style device can be installed by first installing the LCC socket, supplied with the HP 10312D, in the top of the interface connector. If the plastic orientation indicator pin isn't already cut off of the LCC socket (part no. 1200-1138), cut it off so that the LCC socket can be flush mounted on the top of the connector. Then install the LCC style 80286 microprocessor in the LCC socket. Install the heatsink, supplied with the HP 10312D, in place of the U-shaped IC retainer that goes on top of the microprocessor. The additional socket adds capacitance to the circuit, but shouldn't affect the performance of the microprocessor chip.

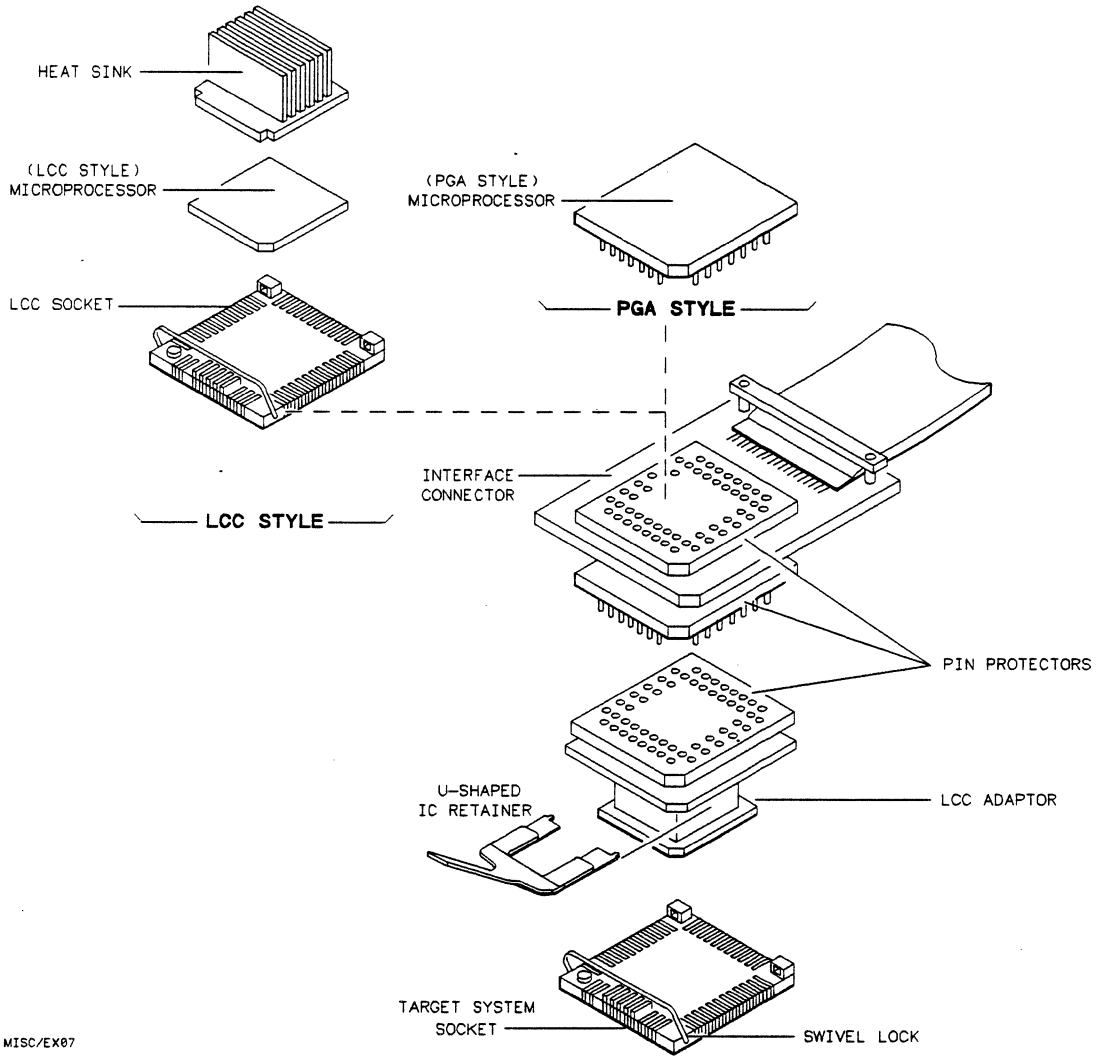

Figure 1-3. Installing the Interface Cable in an LCC Socket

Connecting to the HP 10269C

Connect the HP 1650A or HP 16510A Logic Analyzer pods to the HP 10269C General Purpose Probe Interface as follows:

HP 1650A and 16510A Pod	(into)	HP 10269C Connector
1		1
2		2
3		3

Setting Up the Analyzer from the Disc

The logic analyzer can be configured for 80286 analysis by loading the appropriate configuration file from the flexible disc. Loading this file will also load the inverse assembler file. To load the configuration and inverse assembler:

1. Install the flexible disc labeled "80286 Inverse Assembler for use with: HP 1650A and HP 16510A" in the front disc drive of the logic analyzer.

2. Select one of the following menus:

- For the HP 1650A, select the I/O Disc Operations menu;
- For the HP 16510A, select the System Front Disc menu.

3. Configure the menu to "Load" the analyzer from the file "C80286_I."

4. Execute the load operation to load the file into the HP 1650A or HP 16510A Logic Analyzer.

Format Specification

The 80286 Inverse Assembler file contains predefined format specifications (see figure 1-4). These format specifications include all labels for monitoring the 80286 microprocessor and any coprocessors connected directly to the microprocessor.

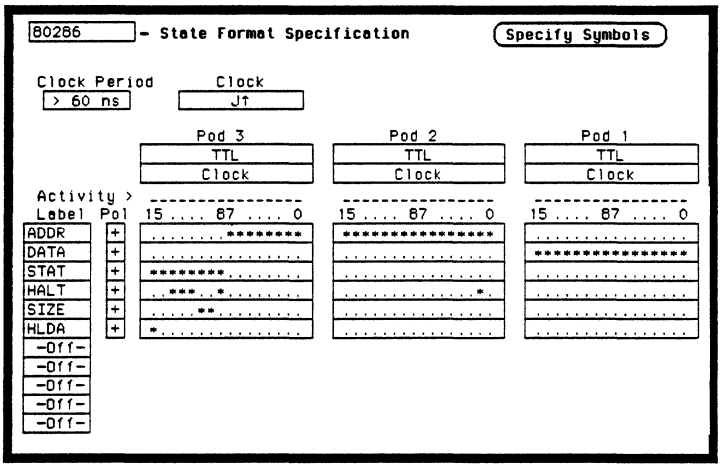

Figure 1-4. 80286 Format Specification

Note

The Clock Period field in figure 1-4 should remain in the current selection (> 60 ns) for proper HP 10312D operation. For more information on the Clock Period field, refer to the reference manual for your logic analyzer.

Symbols

The Symbol Table of the format specification menu is set up with names to identify values of the status label (see figure 1-5).

Additional labels have been defined in the format specification to make triggering on specific 80286 cycles easier. Labels that may be of interest are:

- The "SIZE" label which indicates the size of the transfer on the DATA bus (byte or word transfer) and which byte of a byte transfer is valid.

- The "HALT" label which differentiates between a halt cycle caused by executing the HALT instruction and a shutdown cycle caused by an execution while attempting to process a double fault exception.

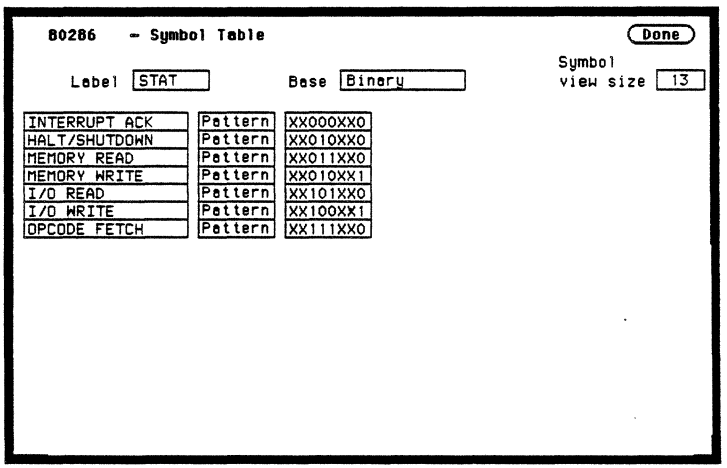

Figure 1-5. Symbol Table for the 80286

Slow Clock

If you have the interface module hooked up and running and observe a slow clock or no activity from the interface board, the +5 V supply coming from the analyzer may not be getting to the interface board.

To check the +5 V supply coming from the analyzer, disconnect one of the logic analyzer cables from the HP 10269C and measure across pins 1 and 2 or pins 39 and 40 (see figure 1-6).

- If +5 V isn't observed across these pins, check the internal preprocessor fuse on the HP 1650A or HP 16510A Logic Analyzer. For information on checking this fuse, refer to the HP 1650A or HP 16510A service manuals.

- If +5 V is observed across these pins and you feel confident that the +5 V is getting to the interface module, contact your nearest Hewlett-Packard Sales/Service Office for information on servicing the board.

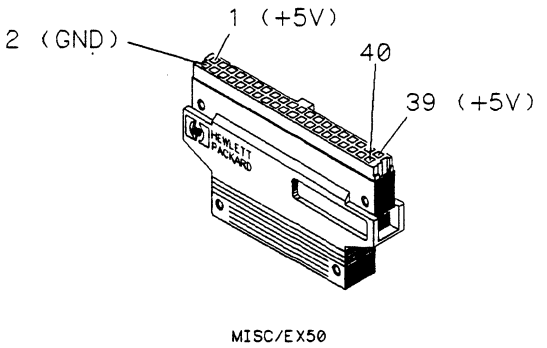

Figure 1-6. Pinout for the Logic Analyzer Cable

Listing Menu

Captured data is displayed as shown in figure 1-7. The inverse assembler is constructed so the mnemonic output closely resembles the actual assembly source code.

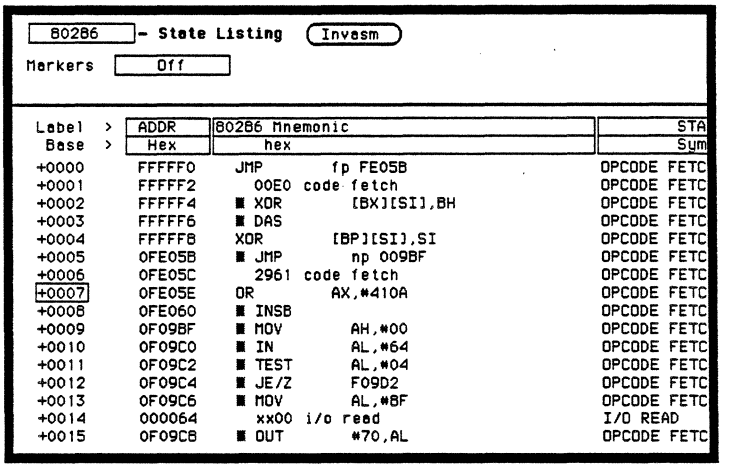

Figure 1-7. Listing Menu for the 80286

The 80286 Inverse Assembler

The 80286 inverse assembler has been designed to support the 80286 microprocessor with or without coprocessors. The following paragraphs explain the operation of the inverse assembler and the results you can expect in certain situations.

The 80286 can fetch instructions up to two bytes (16 bits) wide in a single bus cycle. However, the microprocessor does not provide enough status information to discriminate between the first code fetch cycle of an instruction and subsequant code fetch cycles. You must point to the state that contains the first byte of an instruction fetch. Once synchronized, the inverse assembler will disassemble from this state through the end of the screen.

To do this:

1. Select a line on the display that you know is the first state of a code fetch.

2. Roll this line to the top of the listing.

3. Select the "Invasm" field at the top of the display. The listing will inverse assemble from the top line down. Any data before this screen is left unchanged.

Rolling the screen up will inverse assemble the lines as they appear on the bottom of the screen. If you jump to another area of the screen by entering a new line number, you must re-synchronize the inverse assembler by repeating steps 1 through 3.

Note

Each time you inverse assemble a block of memory, the analyzer will keep that block in the inverse assembled condition. You can inverse assemble several different blocks in the analyzer memory, but the activity between those blocks will not be inverse assembled.

Interpreting Data

Unless followed by a lower-case letter, all numeric output from the inverse assembler is in hexadecimal format. A lower-case "o" following a numeric value indicates an octal representation (the ESC instruction for example). Decimal values are indicated by a lower-case "d" (as in the INT instruction).

Two instructions may be displayed for a single analyzer state because the 80286 fetches a word with two instruction bytes from program memory. If the least significant byte of this word contains a single-byte instruction, the next sequential instruction begins in the upper byte. In this case, the two instructions displayed on a single line are separated by the delete symbol (▌). Since instructions may begin in either the lower or upper byte, the last byte of a multiple-byte instruction may also occur in the lower byte, with a second instruction beginning in the upper byte. In this instance, the delete symbol is displayed in the left-most position of the mnemonic display field. Thus, the following definition: Any instruction appearing to the right of the delete symbol begins in the upper byte of the fetched word.

Examples:

PUSH DX▌ADC BX,DX	(PUSH occupies the lower byte; ADC begins in the upper byte.)
▌CMP AX,#53E6	(An instruction shown on a previous line uses the lower byte; CMP begins in the upper byte.)
JO OFLOW_CTL	(JO begins in the lower byte and uses the upper byte as well.)

Asterisks (*) in the inverse assembler output indicate a portion (or portions) of an instruction was not captured by the analyzer. Missing opcodes occur frequently and are primarily due to microprocessor prefetch activity. Storage qualification, or the use of storage windows, can also lead to such occurrences.

The 80286 microprocessor can perform word transfers as well as byte transfers between microprocessor registers and memory. Furthermore, byte transfers may occur on either the upper eight bits or the lower eight bits of the 16-bit data bus. The inverse assembler makes a distinction between these conditions by displaying "xx" (don't care) for the byte of the transfer that was ignored by the microprocessor. In this way, it is possible to determine exactly which byte was used by the microprocessor:

28B3 memory write	(word transfer)
xxB3 memory write	(byte transfer on lower 8 bits)
28xx memory write	(byte transfer on upper 8 bits)

The 80286 instruction set contains four groups of instructions defining the instruction type in the second opcode, rather than in the first. In this case, if the second opcode is not stored in analyzer memory, only the group where an instruction resides can be determined. Therefore, the group name, rather than an instruction mnemonic, is displayed in the mnemonic display field. These group names are defined as follows:

- Immed - Contains the following instructions when used with immediate source operands:

ADD	AND
OR	SUB
ADC	XOR
SBB	CMP

- Shift - Contains the following logical and arithmetic shifts and rotates:

ROL	SHL/SAL
ROR	SHR
RCL	SAR
RCR	

- Grp_1 - Contains the following instructions:

TEST	IMUL
NOT	DIV
NEG	IDIV
MUL	

Note: The TEST instruction is included only when the instruction concerns an immediate source operand.

- Grp_2 - Contains the following three groups of instructions:

INC DEC	when the instruction concerns memory operands on 8-bit registers
CALL JMP	indirect operand
PUSH	when the instruction concerns 16-bit memory operands

- 2-byte - Contains the following instructions or groups of instructions:

LAR	2 byte Grp1 (see below)
LSL	2 byte Grp2 (see below)
CLTS	

The 80286 instruction set contains two groups of instructions where the instruction type is defined in the third byte. In this case, if the third byte is not stored in analyzer memory, only the group where an instruction resides can be determined. Therefore, the group name, rather than an instruction mnemonic, is displayed in the mnemonic display field. These groups are defined as follows:

- 2 byte Grp1 - Contains the following instructions:

SLDT	LTR
STR	VERR
LLDT	VERW

- 2 byte Grp2 - Contains the following instructions:

SGDT	LGDT
SIDT	LIDT
SMSW	LMSW

Listed below are several abbreviations for normal programming syntax that have been adopted to reduce the width of the inverse assembler display field.

dwp	- DWORD PTR
wp	- WORD PTR
bp	- BYTE PTR
fp	- FAR PTR
np	- NEAR PTR
s	- SHORT

Note that these symbols are displayed only if the operation size cannot be determined from the instruction itself.

To further reduce the field width of the inverse assembler, LOCK and REPeat prefixes appear on the line before the instruction to which they apply.

Physical, rather than logical addresses, are used to perform symbolic address mapping. Most instructions, however, specify a 16-bit intrasegment offset and may indicate a segment different from the default segment for that particular instruction. Since the physical address cannot be determined from this information alone, the inverse assembler must attempt to locate the resulting bus cycle so that the physical address may be obtained. If a bus cycle of the type indicated by the initiating instruction is not found, the physical address cannot be determined and an unmapped logical address (segment override, if any, and the 16-bit intrasegment offset) is displayed instead of a mapped physical address.

Coprocessor Support

The HP 10312D Interface Module fully supports the 80287 coprocessor. The 80287 instructions are inverse assembled and all 80287 operand transfers are decoded as I/O reads and writes.

Instruction Decoding

The HP 10312D Interface Module will send all bus transactions by both the microprocessor and coprocessor to the logic analyzer, and the time count will accurately reflect when the bus cycles occurred. No distinction is made between instructions that are executed and those that are only prefetched by the microprocessor. Typically, there will be several states separating the memory (or I/O) transfer from the instruction that caused the transfer. The logic analyzer is clocked on the falling edge of the microprocessor input clock. This occurs at the end of the next bus state following the last Tc state. The next bus state could be a Ts or a Ti state.

Status Encoding

Each of the eight bits in the STATUS label are described below. Table 1-1 lists the precise value of each bit for all types of 80286 microprocessor cycles. Bit 0 is the least significant bit of the 8-bit field.

- Bit 0 is the device status bit LS1.
- Bit 1 is the device status bit BHE.
- Bit 2 is the device address bit A0.
- Bit 3 is the device status bit LS0.
- Bit 4 is the device status bit M/LIO.
- Bit 5 is the device status bit COD/LINTA.
- Bit 6 is the device status bit LLOCK.
- Bit 7 is the device status bit HLDA.

Table 1-1. Status Field Encoding

80286	Status Bit 7 6 5 4 3 2 1 0
Cycle Type	
Interrupt Acknowledge	x x 0 0 0 x x 0
Halt/Shutdown	x x 0 1 0 x x 0
Memory Read	x x 0 1 1 x x 0
Memory Write	x x 0 1 0 x x 1
I/O Read	x x 1 0 1 x x 0
I/O Write	x x 1 0 0 x x 1
Opcode Fetch	x x 1 1 1 x x 0
Valid bytes in Transfer (from BHE and A0)	
Word (both bytes valid)	x x x x x 0 0 x
Low Byte	x x x x x 0 1 x
High Byte	x x x x x 1 0 x
Other Cycle Information	
Lock	x 0 x x x x x x
Hold Acknowledge	1 x x x x x x x

Note: x = don't care

General Information 2

Interface Module Specifications

Microprocessor Compatibility:	Intel 80286 and all microprocessors made by other manufacturers that comply with Intel 80286 specifications.
Microprocessor Package:	68-contact PGA
	68-contact LCC (with supplied adapter)
Accessories Required:	HP 10269C and HP 10312D
Maximum Clock Speed:	10 MHz clock output (20 MHz clock input)
Signal Line Loading:	1 "F" ALS load plus approximately 40 pF on the following lines:
	A0-A23, LBHE, M/LIO, COD/LINTA, LLOCK
	1 "F" TTL load plus approximately 40 pF on the following lines:
	HLDA, D0-D15, CLK
	2 ALS TTL load plus approximately 40 pF on the following lines:
	LS0, LS1, LREADY, RESET
	All other lines, no load and approximately 12 pF capacitance.

Microprocessor Operations Displayed:	Memory Read/Write I/O Read/Write Opcode Fetch Interrupt Acknowledge Halt Hold Acknowledge Lock Transfer to 80287 Coprocessor	
Power Requirements:	0.66 A at +5 Vdc maximum, supplied by the logic analyzer.	
Logic Analyzer Required:	HP 1650A or HP 16510A	
Environmental Temperature:	Operating:	0 to +55 degrees C (+32 to +131 degrees F)
	Nonoperating:	-40 to +75 degrees C (-40 to +167 degrees F)
Altitude:	Operating:	4600 m (15,000 ft)
	Nonoperating:	15,300 m (50,000 ft)
Humidity:	To 90% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation within the instrument.	

Interface Description

The primary function of an interface module is to connect the target microprocessor to the logic analyzer through the probe interface, and to perform any functions unique to that particular microprocessor. The HP 10312D Interface Module performs this primary function by:

1. Latching and buffering the address, status, and data bus of the 80286 microprocessor so that address, status, and data can be sent to the logic analyzer at the same time; and

2. Generating the logic analyzer clock from the appropriate 80286 microprocessor signals and bus conditions. See figure 2-1 for a block diagram of the interface module.

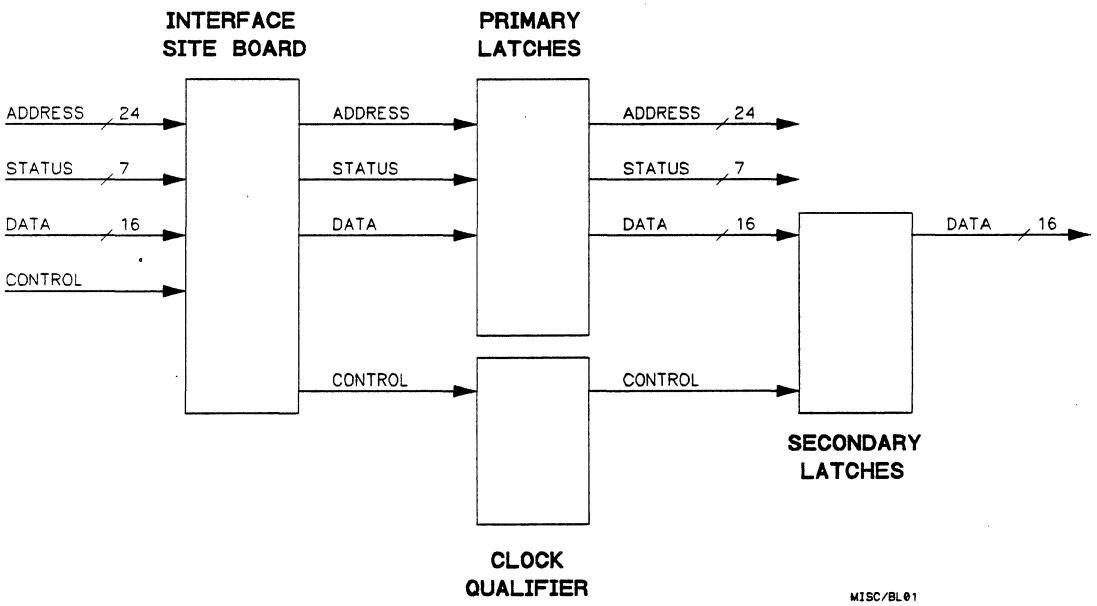

Figure 2-1. 80286 Interface Block Diagram

The preprocessor detects the start of an 80286 bus cycle when the LS0 or LS1 status line goes true. The interface latches address and status at the end of the Ts state of the bus cycle. At the end of the first Tc state of the bus cycle, the interface samples the READY signal and, if found true, the bus cycle is terminated and the logic analyzer is clocked at the end of the next bus state. If the READY signal is not sampled true at the end of the first Tc state, it is sampled at the end of each subsequent Tc state until found true (each extra Tc state is equivalent to adding one wait state). Since the 80286 microprocessor has a 10 ns setup, 5 ns hold specification for data reads, the interface module samples data on every clock cycle. If the data is later determined to be good (if READY was also sampled true), the data is transferred to a set of secondary latches. Address and status in the primary latches and data in the secondary latches are transferred to the logic analyzer at the end of the bus state following the last Tc state of the bus cycle.

Table 2-1 lists the 80286 signals and their corresponding lines to the logic analyzer.

Interface Requirements

The HP 10312D Preprocessor Interface Module operates with an 80286 microprocessor clocked at rates up to 20 MHz. The card adds one "F" load to the data, CLK, LS0, LS1, and HLDA lines, and one ALS TTL load to A0-A23, LBHE, M/LIO, COD/LINTA, LLOCK, RESET, and LREADY.

Testing and Troubleshooting

There are no automatic performance tests or adjustments for the HP 10312D Preprocessor Interface Module. If a failure is suspected in the HP 10312D Preprocessor Interface Module, contact your nearest Hewlett-Packard Sales/Service Office for information on servicing the board.

Table 2-1. 80286 Signal List

CPU Signal	CPU Pin	Label	HP 1650A and 16510A	
			Pod	Bit
A0	34	ADDRESS	2	0
A1	33	ADDRESS	2	1
A2	32	ADDRESS	2	2
A3	28	ADDRESS	2	3
A4	27	ADDRESS	2	4
A5	26	ADDRESS	2	5
A6	25	ADDRESS	2	6
A7	24	ADDRESS	2	7
A8	23	ADDRESS	2	8
A9	22	ADDRESS	2	9
A10	21	ADDRESS	2	10
A11	20	ADDRESS	2	11
A12	19	ADDRESS	2	12
A13	18	ADDRESS	2	13
A14	17	ADDRESS	2	14
A15	16	ADDRESS	2	15
A16	15	ADDRESS	3	0
A17	14	ADDRESS	3	1
A18	13	ADDRESS	3	2
A19	12	ADDRESS	3	3
A20	11	ADDRESS	3	4
A21	10	ADDRESS	3	5
A22	8	ADDRESS	3	6
A23	7	ADDRESS	3	7

Table 2-1. 80286 Signal List (Continued)

CPU Signal	CPU Pin	Label	HP 1650A and 16510A	
			Pod	Bit
D0	36	DATA	1	0
D1	38	DATA	1	1
D2	40	DATA	1	2
D3	42	DATA	1	3
D4	44	DATA	1	4
D5	46	DATA	1	5
D6	48	DATA	1	6
D7	50	DATA	1	7
D8	37	DATA	1	8
D9	39	DATA	1	9
D10	41	DATA	1	10
D11	43	DATA	1	11
D12	45	DATA	1	12
D13	47	DATA	1	13
D14	49	DATA	1	14
D15	51	DATA	1	15
LS1	4	STATUS	3	8
BHE	1	STATUS	3	9
A0	34	STATUS	3	10
LS0	5	STATUS	3	11
M/LIO	67	STATUS	3	12
COD/LINTA	66	STATUS	3	13
LLOCK	68	STATUS	3	14
HLDA	65	STATUS	3	15
PANLCLK*	--	CLOCK	1	J CLK

* This signal is a combination of several microprocessor signals.

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