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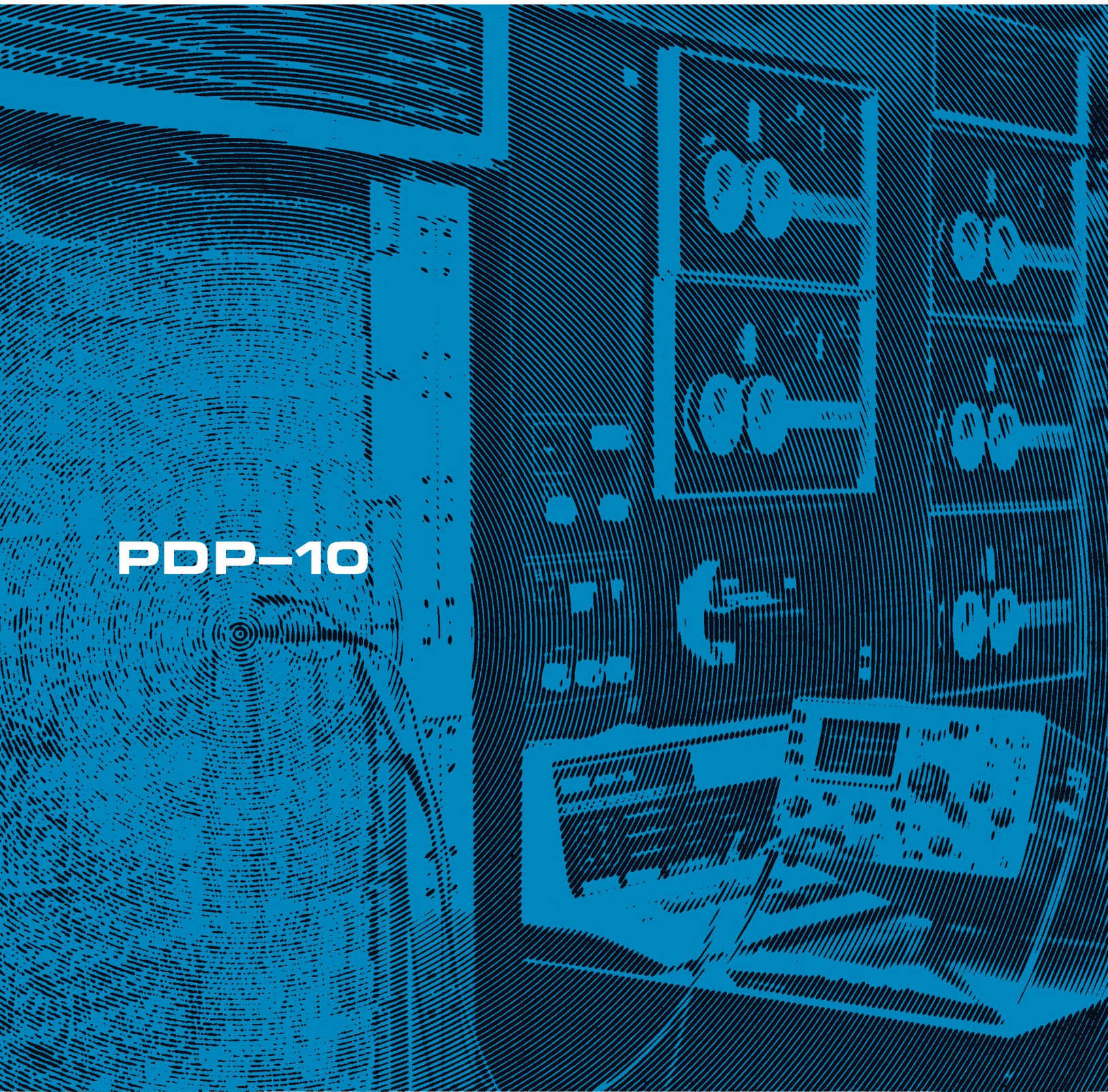
DA10 PDP-8/9 INTERFACE



DEC-10-IACA-D

DA10

PDP-8/9 INTERFACE INSTRUCTION MANUAL

June 1968

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

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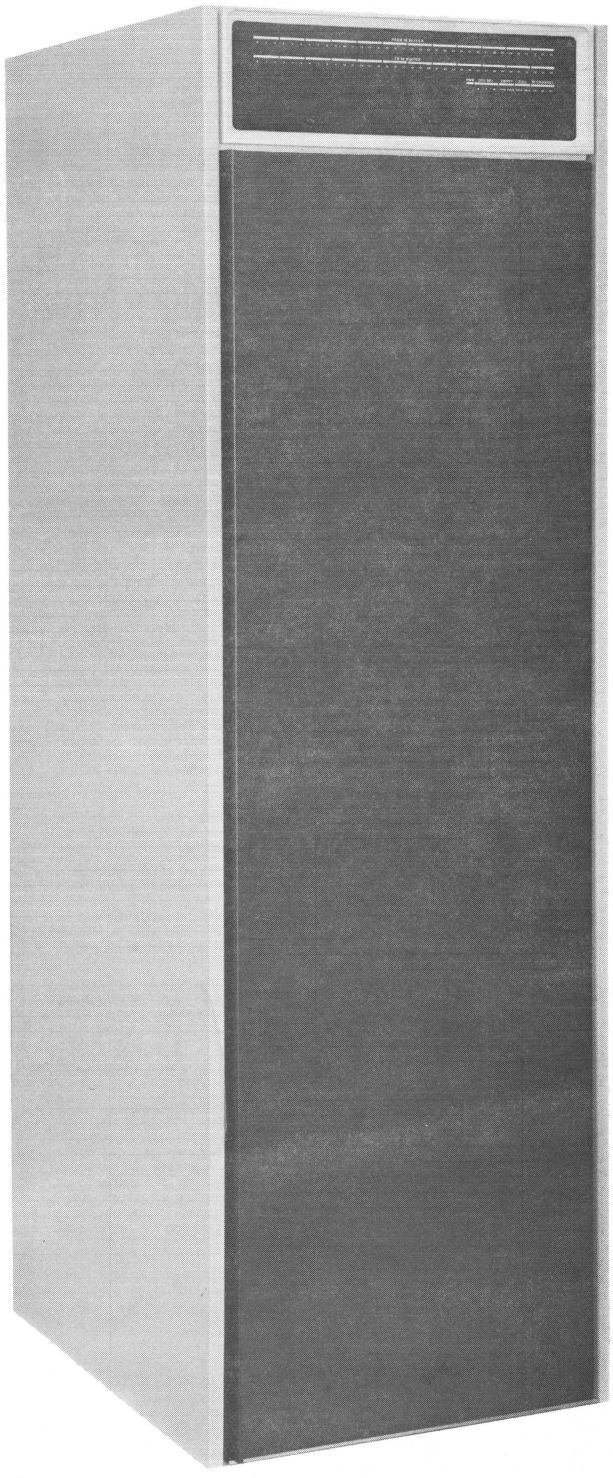


DA10 PDP-8/9 Interface

CHAPTER 1
INTRODUCTION

The DA10 Interface is an optional unit available with the PDP-10 System, manufactured by Digital Equipment Corporation (DEC) Maynard, Massachusetts. The interface allows data and control information to be transferred in both directions between the PDP-10 processor and either a PDP-8 processor or a PDP-9 processor.

This manual and the documents referenced herein provide the necessary information for the installation, operation and mainteance of the DA10 Interface Unit. The level of discussion in this manual assumes the reader is familiar with the logic symbology used by DEC, and the general operations of the PDP-8, PDP-9, and PDP-10 processors.

1.1 REFERENCED PUBLICATIONS

Table 1-1 lists the publications which are available to supplement the information in this manual. These documents can be obtained from the nearest DEC regional office or by writing to:

Digital Equipment Corporation
146 Main Street
Maynard, Massachusetts 01754

Table 1-1
Available Publications

Title	Document No.	Description
Digital Logic Handbook	C-105	Description and specifications of the standard FLIP CHIP modules. Simplified explaination of the selection and use of the modules.
PDP-10 Maintenance Manuals		
Volume 1	DEC-10-HMAA-D	Complete information on the internal operation of the KA10 Processor memory, basic I/O, and options.
Volume 2	DEC-10-HMBA-D	The engineering drawings associated with the KA10 Processor.
Volume 3	DEC-10-HMCA-D	Description, schematics and specifications of the special modules used in the PDP-10 System.

Table 1-1 (Cont)
Available Publications

Title	Document No.	Description
PDP-10 Peripheral Device Engineering Drawing Set (Volume 4)	DEC-10-I6DA-D	Logic block diagrams and other pertinent engineering drawings for BA10 and DA10 options.
PDP-8 Maintenance Manual	F-87	Complete information on the PDP-8 processor operation and available options.
PDP-9 Maintenance Manuals		
Volume 1	F-97	Complete information on the PDP-9 Processor and available options.
Volume 2	F-97	Logic block diagrams and other pertinent engineering drawings for the PDP-9.
DA10 Interface Test	MAINDEC-10-D8A0-D	A description and listing of the program used to detect and diagnose malfunctions in the DA10.
PDP-10 System Reference Manual	DEC-10-HGAA-D	Programming and operating information on the PDP-10 Processor and options.

1.2 GENERAL DESCRIPTION

The DA10 Unit allows the interconnecting of the Input/Output (I/O) Bus from the KA10 Processor to the I/O bus of either a PDP-8 or PDP-9 Processor. Because of the differences in word length and I/O signals of the three devices, the DA10 interface assembles 12-bit words from the PDP-8 or 18-bit words from the PDP-9 into a 36-bit word for transfer to the PDP-10 Processor, or divides a 36-bit word from the PDP-10 into the required length for transfer to the associated processor. Figure 1-1 is a typical system diagram using the DA10 Interface. During input and output operations the DA10 receives both data and control information.

1.3 EQUIPMENT SPECIFICATIONS

Figure 1-2 shows the assemblies mounted in the front and rear of the DA10 Unit which consists of a standard 19 in. cabinet, Type CAB-9B, which is contructed with welded steel frames and sheet aluminum covering. Access doors are mounted on the front and rear of the cabinet and are held closed by magnetic latches. The power control and dc power supply are mounted inside the rear

access door on a plenum door that is latched by a spring-loaded pin at the top. Module mounting panels are mounted behind the front door with the wiring side facing outward. Access to the modules for removal, replacement and/or adjustment is gained through the rear of the cabinet. A fan at the bottom of the cabinet draws cooling air into the cabinet through a dust filter, and a fan assembly mounted in the logic rack passes the cooling air over the modules. The air is exhausted through an opening at the top of the cabinet. Table 1-2 contains the general specifications of the DA10A and DA10B units.

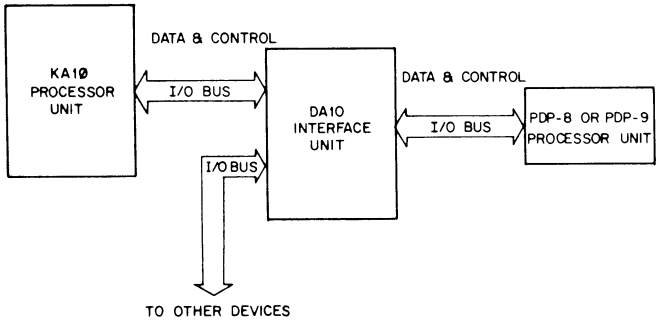


Figure 1-1 DA10 Interface, Typical System Diagram

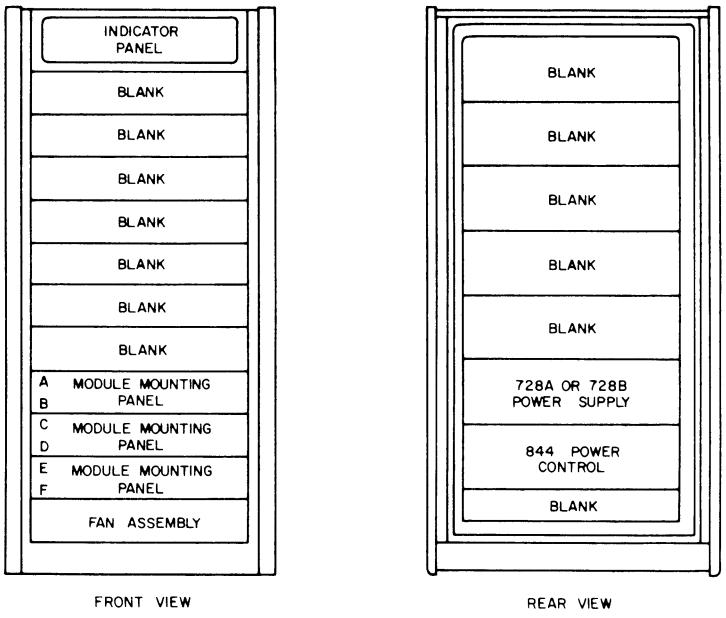


Figure 1-2 DA10 Interface, Assembly Locations

Table 1-2
DA10 General Specifications

Voltage ac	Current (A) Nominal 115V	Power Dissipation (W)	Heat Dissipation (Btu/hr)	Dimensions (in.)	Service Clearance (in.)	Weight (lb)	Maximum Cable Lengths (ft)
See Notes 1 and 2	2.0	230	800	Height: 69 Width: 21-1/4 Depth: 27	Front 36 Rear 36	300	PDP-8: 20 PDP-9: 100 PDP-10: 150 (I/O Bus)

Note 1: PDP-10 Systems normally operate from 3-phase (WYE connected), 115V ± 10%, 60 Hz ± 2 Hz, or 230V ± 10%, 50 Hz ± 2 Hz phase to neutral. Individual devices have separate power cords using 3-wire 30A (single phase) Hubbel Twistlock connectors. An earth/ground connection must be supplied through the power cord in addition to the ground bus requirements.

Note 2: Equipment for use within North America will have the 3-wire Hubbel #3331 (mates with Hubbel #3330) power cord cap (male plug) supplied on the end of a 25 ft line cord.

Equipment for use outside of North America will have a pressure-type terminal strip suitable for 8 to 18 gage wire enclosed within the equipment's power control.

Two configurations of the DA10 are available. The Type DA10A is a 60 Hz configuration and the Type DA10B is a 50 Hz configuration. With the exception of the power supply and power wiring, both configurations are similar. A 728 power supply is used with the DA10A and a 728A power supply is used with the DA10B. The differences in the power wiring of the two configurations are shown on drawing D-IC-DA10-0-3.

CHAPTER 2

OPERATION AND PROGRAMMING

The following paragraphs provide the information and programming notes needed to operate the DA10 Interface with either a PDP-8 or PDP-9 Processor. For the detailed programming information refer to the PDP-10 System Reference Manual, DEC-10-HGAA-D.

2.1 INDICATOR PANEL

The indicator panel (Figure 2-1) is mounted on the top front of the DA10 cabinet. It contains the indicators listed in Table 2-1 and displays the contents and status of the registers and flip-flops in this interface unit.

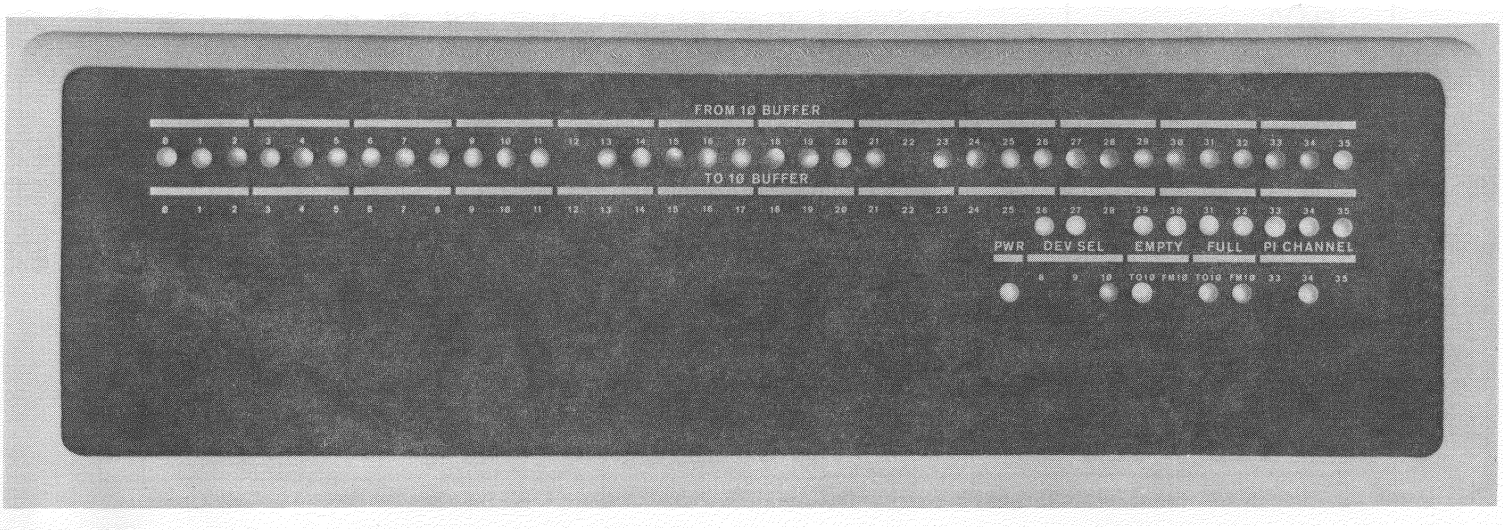


Figure 2-1 DA10 Interface, Indicator Panel

Table 2-1
DA10 Indicator Panel

Indicator	Function
FROM 10 BUFFER (0 through 35)	Indicates the contents of the FM10 Buffer, bits 0 through 35.
TO 10 BUFFER (0 through 35)	Indicates the contents of the TO10 Buffer, bits 0 through 35.

Table 2-1 (Cont)
DA10 Indicator Panel

Indicator	Function
PWR	Lights to indicate that dc power is applied to the logic rack.
DEV SEL	
8	Lights to indicate that DA10 is selected by the PDP-8 Processor.
9	Lights to indicate that DA10 is selected by the PDP-9 Processor.
10	Lights to indicate that DA10 is selected by the PDP-10 Processor.
EMPTY	
TO10 (STAT BUFD)	Lights to indicate that the 36-bits in the TO10 Buffer have been transferred to the PDP-10 or that bit IOB32 is set to a 1 during a CONO instruction.
FM10 (STAT BUFB)	Lights to indicate that the last byte of the FM10 Buffer has been transferred to the PDP-8 or PDP-9 or that IOB28 is set to a 1 during a CONO instruction.
FULL	
TO10 (STAT BUFC)	Lights to indicate that the last byte from a PDP-8 or PDP-9 which loads the TO10 Buffer has been received or that bit IOB30 is set to a 1 during a CONO instruction.
FM10	Lights to indicate that 36-bits from the PDP-10 have been loaded into the FM10 Buffer or that bit IOB26 is set to a 1 during a CONO instruction.
PI CHANNEL (33 through 35)	Indicates the binary configuration of the PI Channel selected.

2.2 POWER CONTROL PANEL

The Type 844 Power Control Panel (Figure 2-2) is mounted on the plenum door at the rear of the cabinet. This panel contains the switches and indicators (listed in Table 2-2) that are used to control the main ac power and select the local and remote modes of operation.

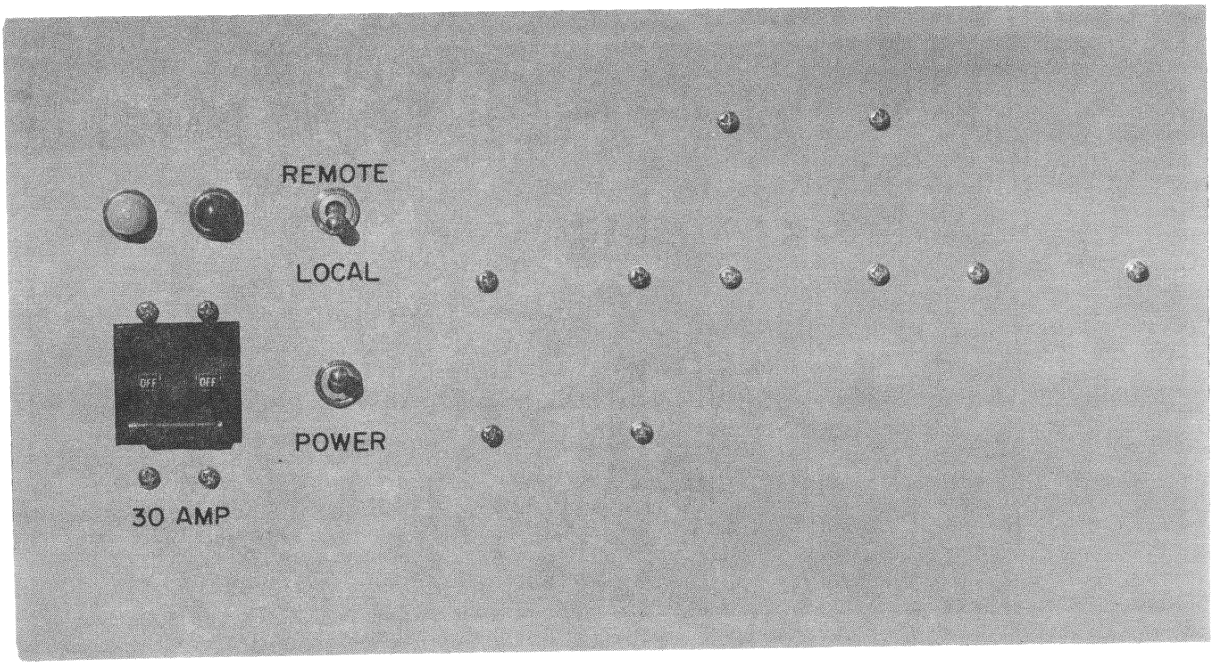


Figure 2-2 Type 844 Power Control Panel

Table 2-2
Power Control Panel, Switches and Indicators

Switch/Indicator	Function
White indicator	Lights to indicate that 115 Vac or 230 Vac line power is applied.
Red indicator	Lights to indicate wrong polarization of the ac line or when 230 Vac is applied.
30 AMP (Circuit Breaker)	Controls the line power to the convenience outlets and protects the input line.
REMOTE/LOCAL (Switch)	Selects either LOCAL or REMOTE mode of operation. (Refer to Paragraph 2.2.1.)
POWER (Switch)	Controls line power to the dc power suppliers and DA10 system.

2.2.1 Power Application

The DA10 has two power application modes selectable by the REMOTE/LOCAL switch on the power control panel. In the remote mode, power to the DA10 is controlled by the POWER switch on the control panel of the KA10 Processor when the following conditions are met.

a. The PDP-10 remote turn-on bus is connected to the DA10 power control.

b. The REMOTE/LOCAL switch on the power control panel of the DA10 is in the REMOTE position.

c. The circuit breaker and POWER switch on the DA10 power control panel are in the up position.

The local mode is in effect when the REMOTE/LOCAL switch is in the LOCAL position. This allows the 30A circuit breaker and POWER switch to control power to the unit.

2.3 DEVICE SELECTION

The DA10 is selected via the I/O busses of the PDP-8 or PDP-9 or the PDP-10 central processors. Each central processor selects the DA10 in an independent manner, therefore, each method is explained separately in this section. For additional information on device selection, refer to Chapter 3, Installation.

2.3.1 PDP-10 Device Selection

The DA10 is selected by bits 3 through 9 of the I/O instructions from the PDP-10 central processor. Seven complementary pairs of signals representing IOS3 through IOS9 are sent to the DA10 via the I/O bus. The IOS lines necessary to select code 014_8 ($000\ 001\ 1_2$) are connected to an AND gate shown on drawing D-BS-DA10-0-CS. When this code appears on the I/O bus, the AND gate is enabled and its output conditions the DATAO enable, DATAI enable, CONO enable, and CONI enable gates.

2.3.2 PDP-9 Device Selection

The PDP-9 central processor uses bits 6 through 13 of IOT instructions for device selection. These eight levels form a 6-bit device selection code, DS0 through DS5, and two subdevice selection codes, SD0 and SD1. The PDP-9 device code 22_8 ($010\ 010_2$) has been assigned to the DA10. When this code is present on the device selection lines of the I/O bus, it is decoded by the decoder shown on drawing D-BS-DA10-0-SI. The subdevice codes SD0 and SD1 are ANDed with the appropriate IOP signals to generate buffer clear and data transfer signals as shown on drawing D-BS-DA10-0-DTL.

2.3.3 PDP-8 Device Selection

The PDP-8 central processor uses bits 3 through 8 of the IOT instructions for device selection. These lines are connected to a pair of W990 modules located in card slots D04 and D05, as shown on drawing D-BS-DA10-0-SI. Jumpers are inserted on the W990 modules to obtain the outputs that are

used for decoding, and the decoders are shown in the upper left-hand corner of the drawing. The PDP-8 codes assigned to the DA10 are as follows; 70_8 ($111\ 000_2$), 71_8 ($111\ 001_2$), and 72 ($111\ 010_2$). In the event that these codes conflict with another peripheral device in a particular system, they can be changed by modifying the jumpers on the W990 modules. It must be noted that the codes cannot overlap octal triads (i.e., the most significant octal bit must be the same for all selected codes). Refer to Paragraph 3.4.1 for additional information on jumper placement.

2.4 PROGRAMMING NOTES

2.4.1 PDP-10 Instructions

The DA10 responds to the standard PDP-10 I/O instructions. It requires one I/O device number (standard: 014) and provides program interrupt requests on one PI channel. Data, status, and control are transferred via the assigned I/O instructions. Various aspects of the I/O instructions are described below.

2.4.1.1 CONO (Conditions Out) - Control information is transferred to the DA10 via the right 18-bits of a CONO instruction. Figure 2-3 shows specifically which bits are used and the respective functions that are performed if the specific bit is a 1 during the performance of the CONO instruction. The CONO instruction is completed in two parts. First, the CONO clear pulse is sent to the DA10, and 1 μs later, the CONO SET pulse is sent. Since the PI channel (bits 33 through 35) is cleared by the CONO clear pulse, the PI channel assignment must be placed on bits 33 through 35 whenever a CONO instruction is performed to set the PI channel.

Clear Self Check Enable 23	Set Self Check Enable 24	Clear FM10 Full Flag 25	Set FM10 Full Flag 26	Clear FM10 Empty Flag 27	Set FM10 Empty Flag 28	Clear TO10 Full Flag 29	Set TO10 Full Flag 30	Clear TO10 Empty Flag 31	Set TO10 Empty Flag 32	Set PI Channel 33	34	35

Figure 2-3 CONO Data Word

2.4.1.2 CONI (Conditions In) - The status of the DA10 is transferred to the central processor by a CONI instruction. Figure 2-4 shows specifically which bits are transferred and their respective function. A 1 in any bit except bits 33 through 35 indicates that the associated flag is set. References to the CONI instruction include the CONSO and CONSZ instructions.

	Self Check Enable		FM10 Full Flag		FM10 Empty Flag		TO10 Full Flag		TO10 Empty Flag	PI Channel		
23	24	25	26	27	28	29	30	31	32	33	34	35

Figure 2-4 CONI Data Word

2.4.1.3 DATAO (Data Out) - The DATAO instruction is performed in two parts. First the DATAO clear pulse is sent to the DA10, and 1 μs later, the DATAO SET pulse is sent. In the case of the DA10, the DATAO clear pulse performs the following functions: clears the FM10 buffer conditioning it for a data transfer; and clears the FM10 EMPTY flag removing the PI request to the PDP-10. The DATAO set pulse performs the following functions: strobes the data on the PDP-10 I/O bus into the FM10 buffer; and sets the FM10 FULL flag enabling the PI gate in the DA10 which sends a PI request to the PDP-8 or PDP-9. References to the DATAO instruction in this manual include the appropriate functions of the BLKO instruction.

2.4.1.4 DATAI (Data In) - When the DATAI instruction is performed, commands to the DA10 will transfer the contents of the TO10 buffer to the central processor via the 36 data lines of the I/O bus, clear the TO10 FULL flag, and set the TO10 EMPTY flag. The clearing of the TO10 FULL flag removes the PI request from the PDP-10, and the setting of the TO10 EMPTY flag sends a PI request to the PDP-8 or PDP-9. The references to DATAI instructions in this manual include the appropriate functions of the BLKI instruction.

2.4.2 PDP-9 Programming

The DA10 is assigned device code 22_8 for the PDP-9. Both data and control to the DA10 pass via the assigned device codes. The PDP-9 receives a PI request when either the FM10 FULL flag or the TO10 EMPTY flag is set.

The DA10 status can be tested with the following instructions.

Instruction	Test
702221	Skip one if the TO10 EMPTY flag is set.
702241	Skip one if the TO10 FULL flag is set.

A 702201 instruction will clear the TO10 buffer and the TO10 EMPTY flag.

The following instructions will load the TO10 buffer.

Instruction	Function
702204	Transfers the contents of the PDP-9 accumulator to bits 0 through 17 of the TO10 buffer.
702224	Transfers the contents of the PDP-9 accumulator to bits 18 through 35 of the TO10 buffer; and set the TO10 FULL flag.

The following instructions will read the FM10 buffer.

Instruction	Function
702212	Clears and loads the PDP-9 accumulator with bits 0 through 17 of the FM10 buffer.
702232	Clears and loads the PDP-9 accumulator with bits 18 through 35 of the FM10 buffer, clears the FM10 FULL flag and sets the FM10 EMPTY flag.

2.4.3 PDP-8 Programming

The PDP-8 device selection codes 70, 71, 72 have been assigned to the DA10. Both data and control pass via the assigned selection codes. The PDP-8 receives a PI request when either the FM10 FULL flag or the TO10 EMPTY flag is set. The DA10 status can be tested with the following instructions.

Instruction	Test
6701	Skip one if the TO10 EMPTY flag is set.
6721	Skip one if the FM10 FULL flag is set.

The 6701 instruction will clear the TO10 buffer and the TO10 EMPTY flag.

The following instructions load the TO10 buffer.

Instruction	Function
6704	Transfers the contents of the PDP-8 accumulator to bits 0 through 11 of the TO10 buffer.
6714	Transfers the contents of the PDP-8 accumulator to bits 12 through 23 of the TO10 buffer.
6724	Transfers the contents of the PDP-8 accumulator to bits 24 through 35 of the TO10 buffer, and sets the TO10 FULL flag.

The following instructions read the contents of the FM10 buffer.

Instruction	Function
6702	Loads the PDP-8 accumulator with the contents of bits 0 through 11 of the FM10 buffer (inclusive OR).
6712	Loads the PDP-8 accumulator with the contents of bits 12 through 23 of the FM10 buffer (inclusive OR).
6722	Loads the PDP-8 accumulator with the contents of bits 24 through 35 of the FM10 buffer (inclusive OR), clears the FM10 FULL flag and sets the FM10 EMPTY flag.

CHAPTER 3
INSTALLATION

The information necessary to connect the DA10 unit to the PDP-10 processor and to either a PDP-8 or PDP-9 processor is provided in the following section. It includes the special module and buffer wiring instructions and adjustment procedures required for a standard installation.

3.1 POWER REQUIREMENTS

The DA10 unit connects to the ac line as specified in Table 1-2.

3.2 ENVIRONMENTAL CONDITIONS

The operating environment for the DA10 unit is the same as that required for the PDP-10 processor. Refer to the appropriate section in the PDP-10 Maintenance Manual, Volume I for specific environmental limits.

3.3 SPACE REQUIREMENTS

The DA10 cabinet can be installed at any location provided that the specified cable and power cord lengths are used. The dimensions of the cabinet and the minimum service area are illustrated in Figure 3-1.

3.4 DEVICE SELECTION WIRING

Since a conflict with another peripheral device could occur, the PDP-8 device selection lines are sent to the PDP-8 device selection decoder through a pair of device selection cards. A brief description of these cards and the wiring information follow.

3.4.1 PDP-8 Device Selection Cards

In the DA10, the PDP-8 device selection lines connect to the device selection cards located in slots D04 and D05. Jumpers located on these selection cards can be arranged so the DA10 will respond to three device selection codes within the PDP-8 repertoire. If special device selection codes have not been specified by the customer, the strapping on the device selection cards is connected so that the DA10 will respond to standard device selection codes of 70, 71, and 72.

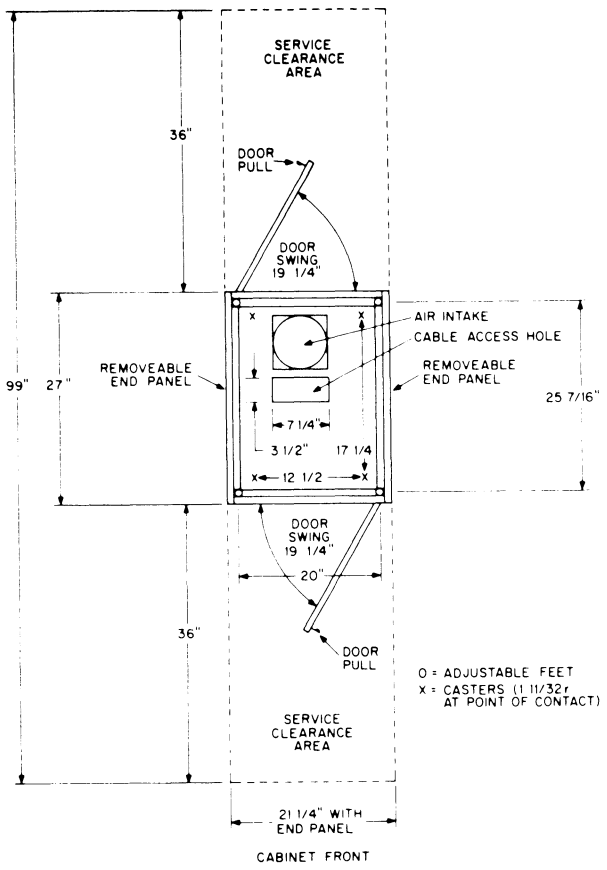


Figure 3-1 DA10 Area Requirements

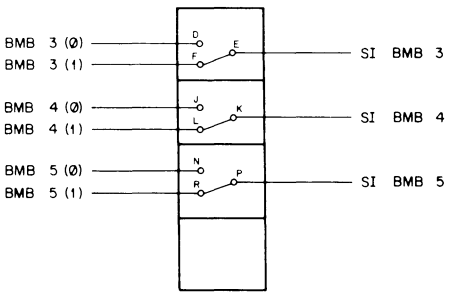
Figure 3-2 is provided to aid the maintenance personnel in understanding the PDP-8/DA10 device selection cards. A table at the top of the figure shows the condition of bits 3 through 8 for standard device selection codes. A schematic representation and a pictorial representation of the device selection cards show the jumper placement for the standard device selection codes. When different device selection codes are utilized by the DA10, the table at the bottom of the figure may be used to determine the new strapping requirements. It is important that the software must reflect any change from the standard device selection codes.

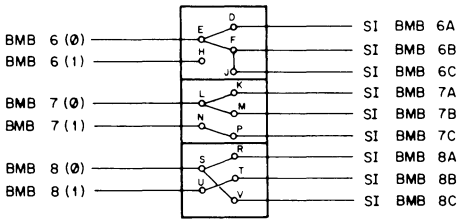
3.5 DATA TRANSFER PULSE MIXERS

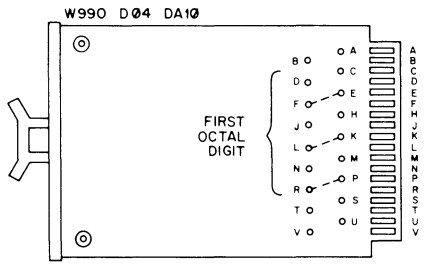
The DA10 is capable of transferring 12-bit words to and from a PDP-8 central processor and 18-bit words to and from a PDP-9 central processor. To fulfill these functions, a data transfer pulse mixer (a jumper network) has been designed into the DA10. Two W990 modules located in slots B23 and A09 contain the jumper network. When the DA10 is shipped, the data transfer pulse mixer is

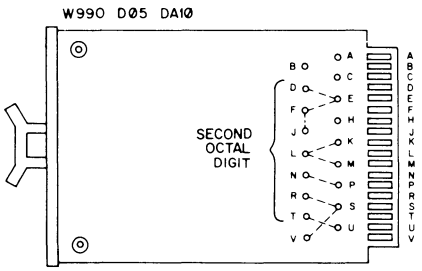
strapped for the central processor that is specified by the user. During installation, however, the data transfer pulse mixer modules should be checked to assure that the strapping is correct. The following discussions, which describe the data transfer pulse mixer, are intended to explain why the data transfer pulse mixer is required, describe its operation when strapped for the different central processors, and provide guidelines for changing the strapping, if required.

DEVICE SELECTION CODE	FIRST OCTAL DIGIT			SECOND OCTAL DIGIT		
	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7	BIT 8
70	1	1	1	0	0	0
71	1	1	1	0	0	1
72	1	1	1	0	1	0









	BIT NO.	DØ4 JUMPERS	
		FROM	TO
FIRST OCTAL DIGIT	BIT 3 = 1	E	F
	BIT 3 = Ø		D
	BIT 4 = 1	K	L
	BIT 4 = Ø		J
	BIT 5 = 1	P	R
	BIT 5 = Ø		N

	BIT NO.	DØ5 JUMPERS					
		FIRST DEVICE SEL. CODE		SECOND DEVICE SEL. CODE		THIRD DEVICE SEL. CODE	
		FROM	TO	FROM	TO	FROM	TO
SECOND OCTAL DIGIT	BIT 6 = 1	D	H	F	H	J	H
	BIT 6 = Ø		E		E		E
	BIT 7 = 1	K	N	M	N	P	N
	BIT 7 = Ø		L		L		L
	BIT 8 = 1	R	U	T	U	V	U
	BIT 8 = Ø		S		S		S

Figure 3-2 PDP-8/DA10 Device Selection Cards

When a PDP-9 reads the FM10 buffer, data must be present on its I/O bus for approximately 1 μs to complete the data transfer. To complete a data transfer to a PDP-8, only the leading edge

transition of the data is required. In order to fulfill both of these requirements, a 100 ns DTL 8 READ A pulse (and DTL 8 READ D) and a 1 μs DTL 9 READ A pulse (and DTL 9 READ D) are generated in the data transfer logic and sent to the data transfer pulse mixer. The strapping on the data transfer pulse mixer is varied as explained below to select the appropriate pulse. (Refer to drawing D-BS-DA10-0-DTPM (sheets 1 and 2).)

Sheet 1 of drawing D-BS-DA10-0-DTPM shows the strapping for the PDP-8 configurations. When a PDP-8 is interfaced with the DA10, three sequential READ pulses that are generated under program control are required to transfer three 12-bit bytes out of the FM10 buffer and onto the PDP-8 I/O bus. Three sequential LOAD pulses are also required to load three 12-bit data words into the TO10 buffer via the PDP-8 I/O bus.

When the first byte is to be read, the DTL 8 READ A pulse is generated and sent to pin D of module A09 generating the DTPM READ AX pulse. The DTPM READ AX pulse is returned to the data transfer logic and is used to generate the DTL READ A pulse that enables the output gates for bits 00 through 11 of the FM10 buffer gating the first byte onto the PDP-8 I/O bus. When the second byte is to be read, the DTL READ MID pulse is generated and sent to pins K and S of module A09 generating the DTPM READ B and DTPM READ C pulses. The DTPM READ B pulse enables the output gates for bits 12 through 17 and the DTPM READ C pulse enables the output gates for bits 18 through 23. With bits 12 through 23 enabled, the second byte is gated onto the PDP-8 I/O bus. The last byte is transferred in a way similar to the first byte. The DTL 8 READ D pulse is sent to pin L of module A09 generating the DTPM READ DX pulse. It is returned to the data transfer logic generating the DTL READ D pulse that enables the output gates for bits 24 through 35 of the FM10 buffer.

When the first data word from the PDP-8 is to be loaded into the TO10 buffer, the DTL LOAD A pulse is sent directly to the input gates for bits 00 through 11 of the TO10 buffer gating the data into the TO10 buffer. To load the second data word, the DTL LOAD MID pulse is generated and sent to pins K and S of module B23 generating the DTPM LOAD C pulses which enable the input gates for bits 12 through 23 of the TO10 buffer. The last data word is loaded by the DTL LOAD D pulse that is sent directly to the input gates for bits 24 through 35 of the TO10 buffer.

If the DA10 is to be interfaced with a PDP-9, the A09 and B23 modules require different strapping because of the 18-bit word length of the PDP-9. The PDP-9 configuration of the data transfer pulse mixers is shown on sheet 2 of drawing D-BS-DA10-0-DTPM. When the first 18-bit byte is read from the FM10 buffer, the DTL 9 READ A pulse is sent to pin F of module A09 generating the DTPM READ AX pulse. The DTPM READ AX pulse is used to generate the DTL READ A pulse that enables the output gates for bits 00 through 11 of the FM10 buffer; and after being applied to pin H of module A09, generates the DTPM READ B pulse that enables the output gates for bits 12 through 17 of the FM10 buffer. With output gates 00 through 17 enabled, the 18-bit byte is gated onto the PDP-9 I/O bus.

The second 18-bit byte from the FM10 buffer is gated onto the PDP-9 I/O bus in a similar manner except the DTL 9 READ D pulse initiates the data transfer by generating the DTPM DX pulse. The DTPM READ DX pulse is used to generate the DTL READ D pulse that performs the following data transfer functions: enables the output gates for bits 18 through 23. With the output gates for bits 18 through 35 enabled, the second byte is placed on the PDP-9 I/O bus.

To load the TO10 buffer, the PDP-9 performs two 18-bit data transfers. During the first data transfer, the DTL LOAD A pulse enables the input gates for bits 00 through 11 and generates the DTPM LOAD C pulse enabling the input gates for bits 18 through 23. With the input gates enabled, the data on the PDP-9 I/O bus is loaded into bits 18 through 35 of the TO10 buffer.

A comparison of sheets 1 and 2 of drawing D-BS-DA10-0-DTPM will show the differerences in the data transfer pulse mixer strapping. When a PDP-8 is interfaced with the DA10, the strapping shown on sheet 1 is utilized; sheet 2 shows the strapping required for interfacing a DA10 with a PDP-9.

3.6 FM10 BUFFER OUTPUT MIXER

As stated in the discussion of the data transfer pulse mixer, the 36-bits of data stored in the FM10 buffer are read in the following manner: three 12-bit words are strobed onto the PDP-8 I/O bus; or two 18-bit words are strobed onto the PDP-9 I/O bus. The DA10 is made compatible with either the PDP-8 or PDP-9 by the strapping arrangment on the FM10 buffer output mixer, a jumper network contained on five W990 modules located in slots C10, C11, D10, D11 and E12. To illustrate the strapping arrangements for the PDP-8 and PDP-9, Figures 3-3 and 3-4 show a simplified view of output mixer along with the FM10 buffer output gates and the I/O busses.

As shown on Figure 3-3, bits 00 through 11 are strobed directly onto the PDP-8 I/O bus when the DTL READ A pulse reads the first byte. When the second byte is read, the DTPM READ B pulse storbes bits 12 through 17 and the DTPM READ C pulse strobes bits 18 through 23. The data on lines IOB 12A through IOB 17A and IOB 00O through IOB 05O are placed on the PDP-8 I/O bus via the strapping of the output mixer. To read the third byte, the DTL READ D pulse strobes the data onto lines IOB 06O through IOB 17O sending the data to the PDP-8 I/O bus via the strapping on the output mixer.

When a PDP-9 is interfaced with the DA10, the output mixer strapping is changed so that the DA10 will accommodate the 18-bit word length of the PDP-9. Figure 3-4 shows a simplified view of the PDP-9 strapping. When the first 18-bit byte is read, bits 00 through 11 are strobed directly onto the associated bits of the PDP-9 I/O bus by the DTL READ A pulse, and bits 12 through 17 are strobed onto lines IOB 12A through IOB 17A by the DTPM READ B pulse. Then, bits 12 through 17 are placed on the associated bits of the PDP-9 I/O bus via the output mixer strapping. To read the second byte,

the DTPM READ C pulse strobes bits 18 through 23 and the DTL READ D pulse strobes bits 24 through 35. The data on IOB 00O through IOB 17O is placed on the appropriate line of the PDP-9 I/O bus via the output mixer strapping.

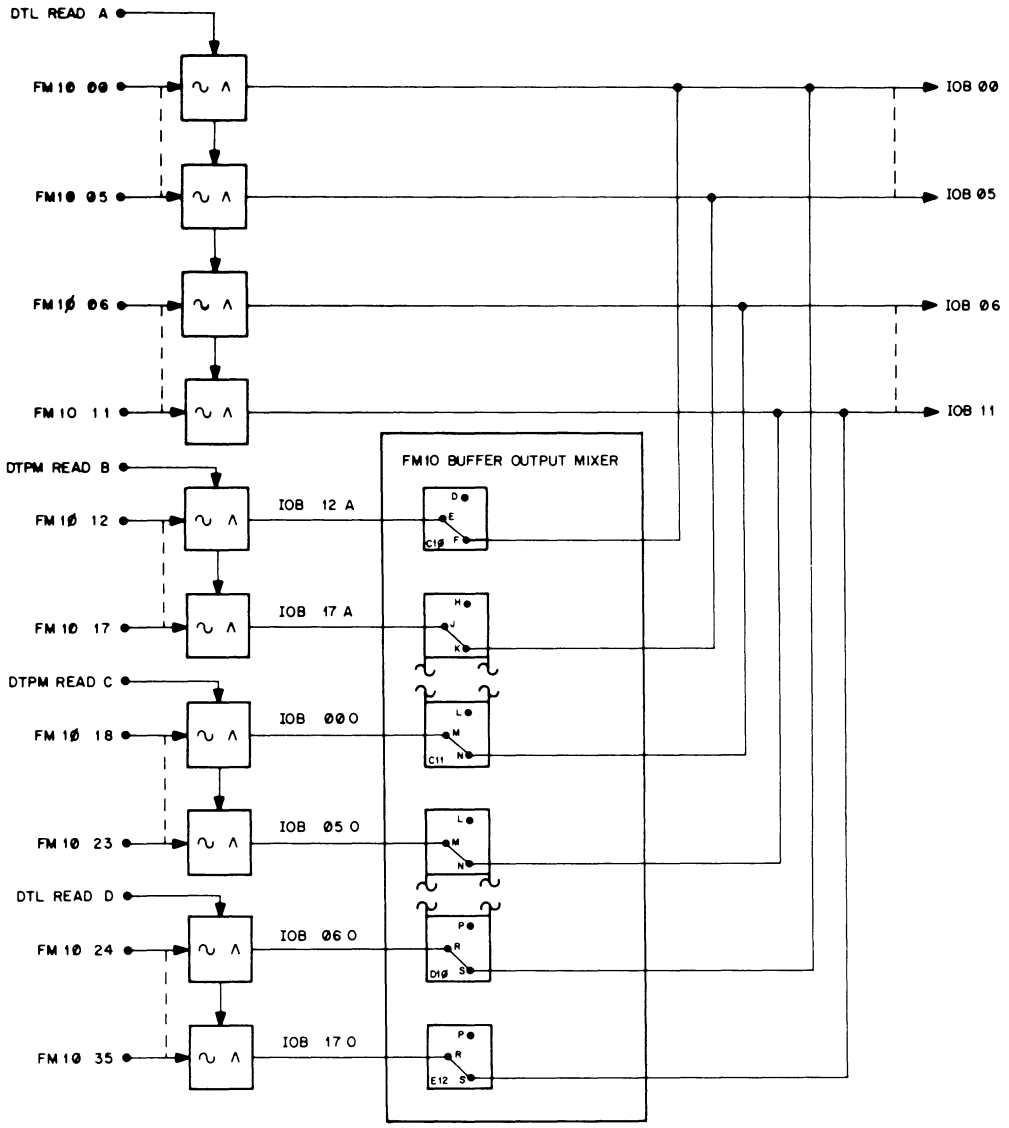


Figure 3-3 FM10 Buffer Output Mixer - PDP-8 Strapping

Figures 3-3 and 3-4 show only a portion of the jumper network that is contained in the output mixer, but they do show the key jumpers that are required to understand the output mixer operation. For the complete strapping arrangement, refer to drawing D-BS-DA10-0-FBOM (sheets 1 and 2). Sheets

1 and 2 show the strapping required by a PDP-8 and PDP-9 respectively. The input signal names to the mixer (IOB 12A - IOB 17A, etc.) shown in Figures 3-3 and 3-4 should be prefixed with FTB 9 to obtain the signal names shown on drawing D-BS-DA10-0-FBOM. When the equipment is shipped, the output mixer is strapped for operation with the central processor specified by the user. To assure that the strapping arrangement is correct, check the output mixer modules when the equipment is installed.

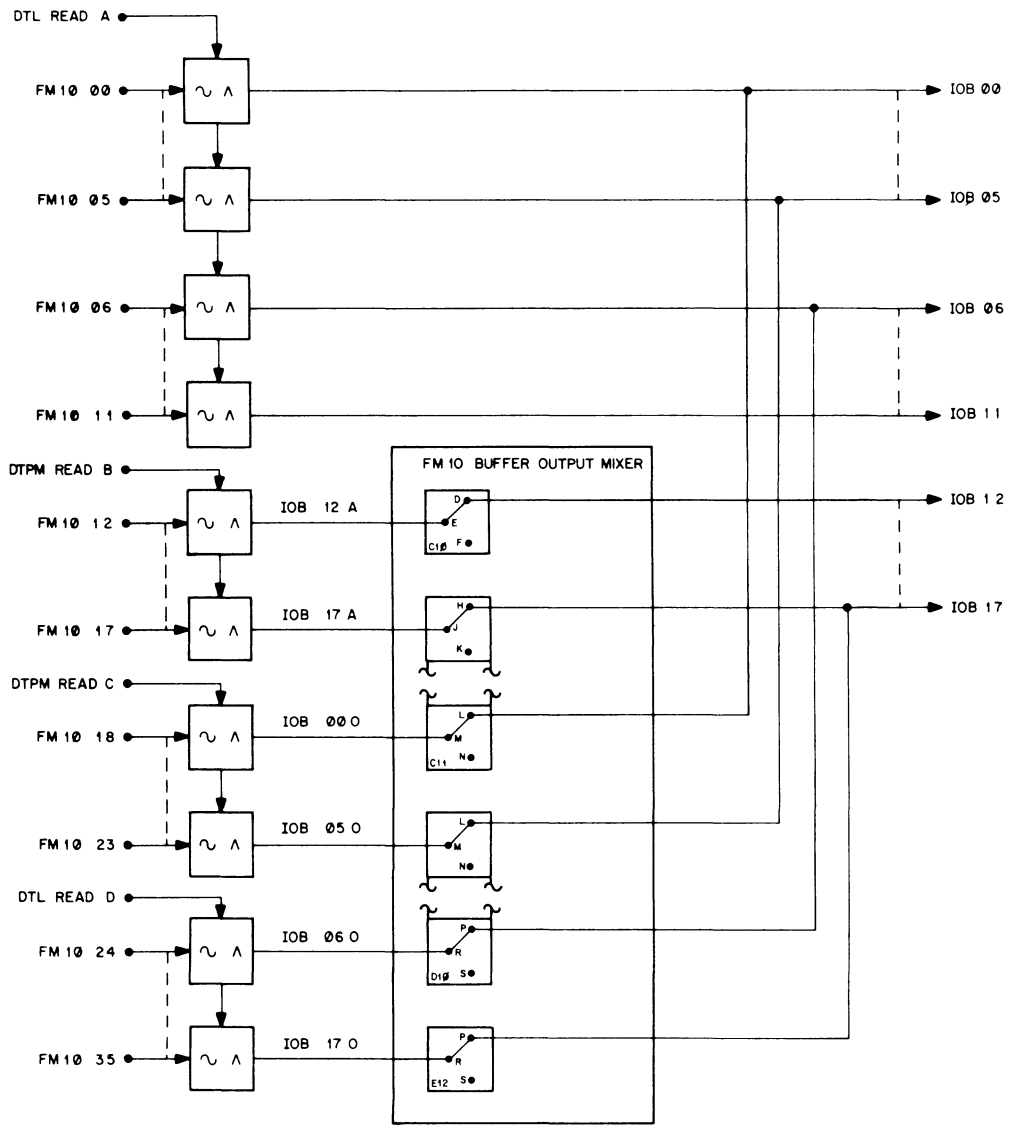


Figure 3-4 FM10 Buffer Output Mixer - PDP-9 Strapping

3.7 TO10 BUFFER INPUT MIXER

The TO10 buffer input mixer, a jumpering network, is contained on five W990 modules that are located in slots C12, C13, D12, D13, and F12. By varying the strapping arrangement of the input mixer, the DA10 is conditioned for operation with a PDP-8 or PDP-9. Figures 3-5 and 3-6 illustrate the two strapping arrangements in simplified block diagram form. As explained in the discussion of the data transfer pulse mixer, the 36-bit TO10 buffer is loaded in one of two ways described below.

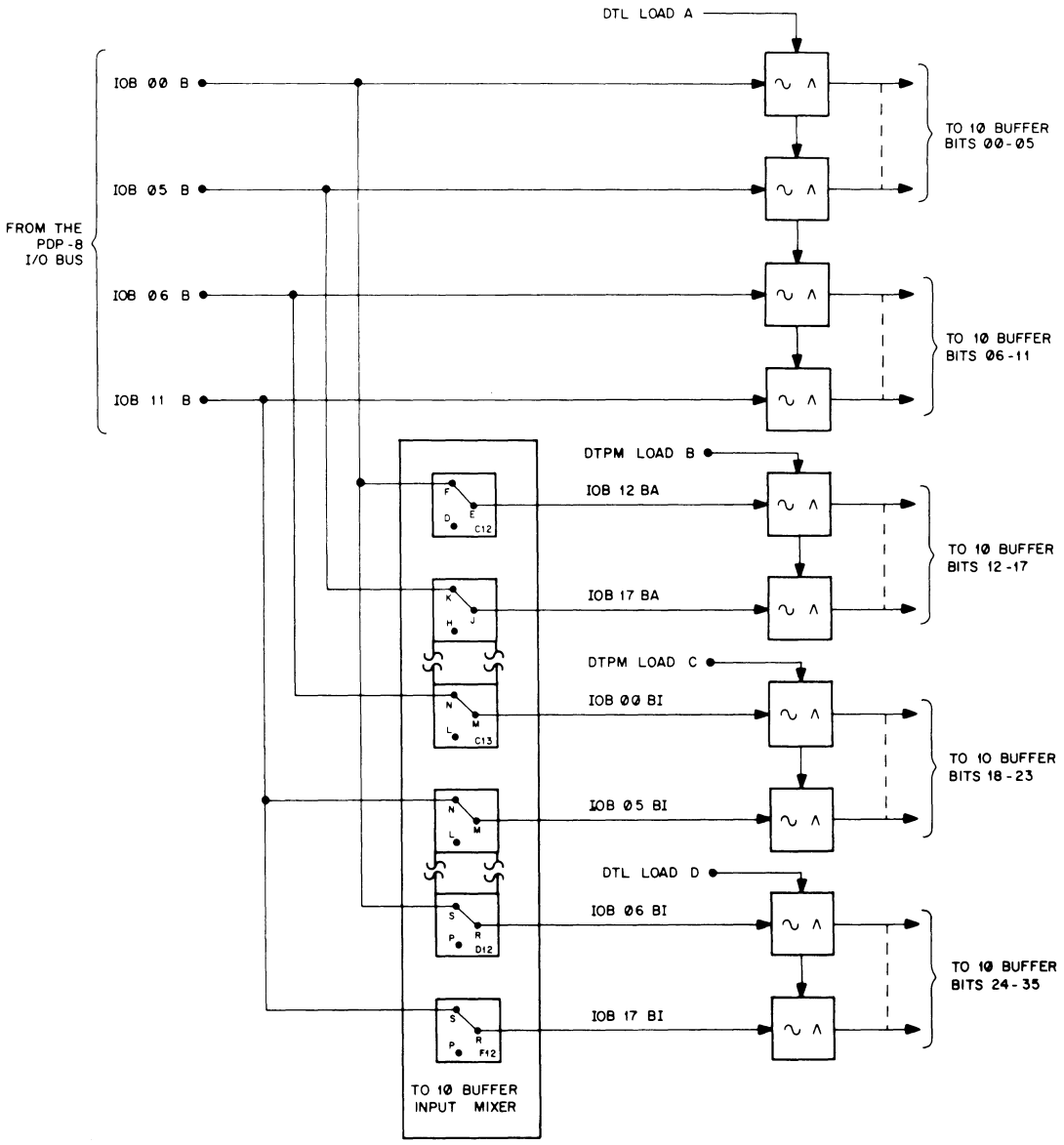


Figure 3-5 TO10 Buffer Input Mixer - PDP-8 Strapping

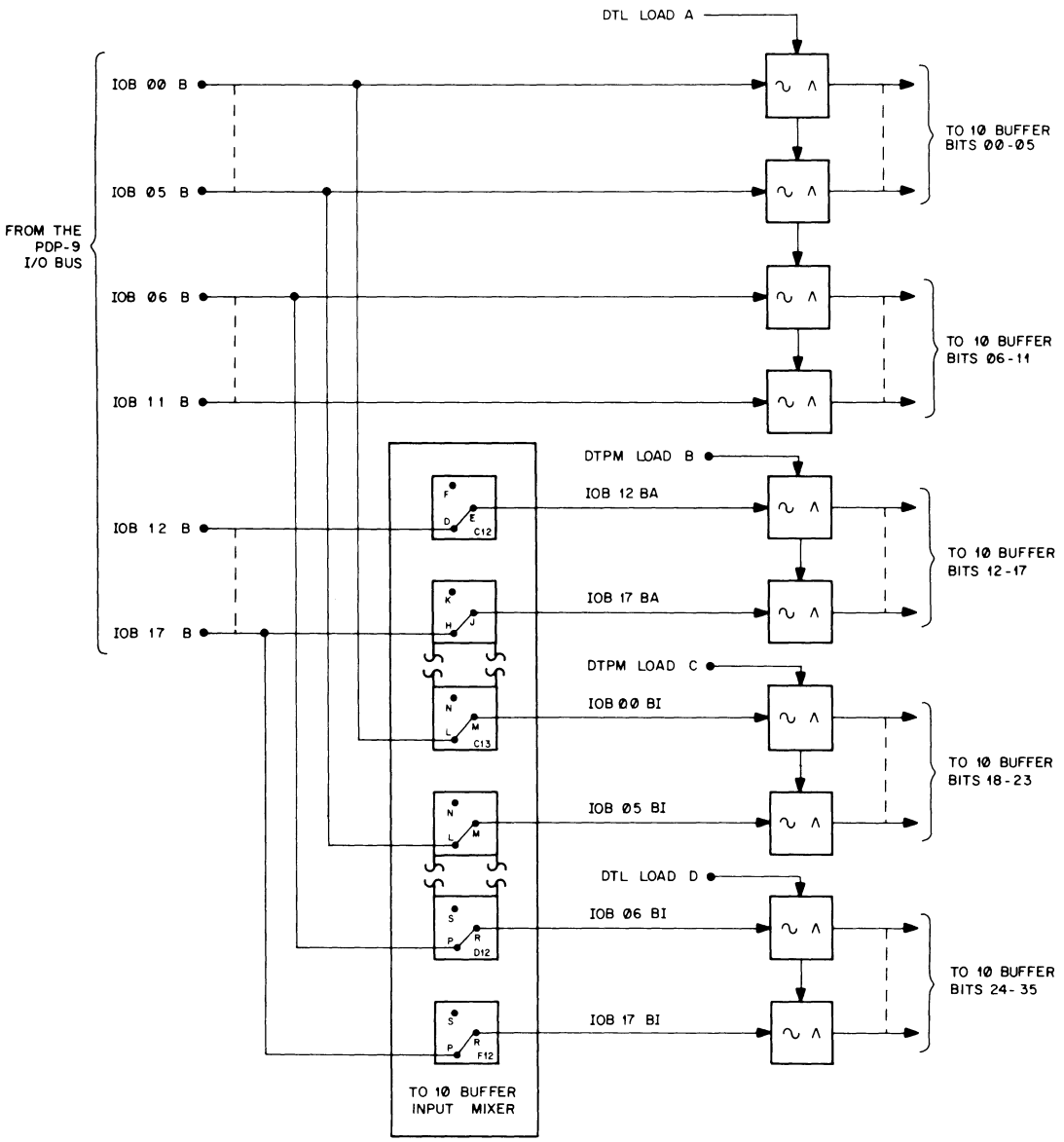


Figure 3-6 TO10 Buffer Input Mixer - PDP-9 Strapping

A PDP-8 performs three 12-bit transfers; or a PDP-9 performs two 18-bit transfers. The input mixer strapping is one of the items which must be varied to make the DA10 compatible with either a PDP-8 or PDP-9. Both strapping arrangements are explained in the following discussions.

Figure 3-5 shows that data from the PDP-8 I/O bus is sent directly to the input gates for bits 00 through 11 of the TO10 buffer. Also, it can be seen that the data from the PDP-8 I/O bus is sent to the input gates for bits 12 through 23 and bits 24 through 35 via the input mixer strapping. To complete the first transfer, the DTL LOAD A pulse enables the input gates for bits 12 through 23; the data on lines IOB 12BA through IOB 17BA is loaded into the TO10 buffer by the DTPM LOAD B pulse;

and the data on lines IOB 00BI through IOB 05BI is loaded by the DTPM LOAD C pulse. The third data word is placed on the I/O bus and sent to lines IOB 06BI through IOB 17BI via the input mixer strapping. Then, the DTL LOAD D pulse gates the data on the lines into bits 24 through 35 of the TO10 buffer.

Figure 3-6 shows the input mixer strapping arrangement used when the DA10 is interfaced with a PDP-9. The data on lines IOB 00B through IOB 11B is sent to the input gates for bits 00 through 11 and to the input gates for bits 18 through 29 via the input mixer strapping. The data on lines IOB 12B through 17B is sent to the input gates from bits 12 through 17 and 30 through 35 via the input mixer strapping. When the PDP-9 transfers the first data word, the DTL LOAD A and DTPM LOAD B pulses enable the input gates for bit 00 through 17 gating the data into the TO10 buffer. During the transfer of the second word, the DTPM LOAD C and DTL LOAD D pulses enable the input gates for bits 18 through 35 and gates the second PDP-9 data word into bits 18 through 35 of the TO10 buffer.

Only a portion of the input mixer is shown in Figures 3-5 and 3-6. Refer to drawing D-BS-DA10-0-TBIM (sheets 1 and 2) for the complete strapping arrangement. Sheets 1 and 2 show the strapping required for use with a PDP-8 and a PDP-9 respectively. The output signal names from the input mixer (IOB 12BA, IOB 17A, etc.) shown in Figures 3-5 and 3-6 should be prefixed with TBIM 9 to obtain the signal names shown on the drawing. When the equipment is shipped, the input mixer is strapped to operate with the central processor specified by the user. During installation, the input mixer strapping arrangement should be checked to assure that it is is correct.

3.8 I/O BUS CONNECTIONS

The DA10 is connected to the PDP-10 central processor via the PDP-10 I/O bus and to either the PDP-8 or PDP-9 via their I/O busses. The I/O bus cables for each system are looped from the central processor through the options that operate from the specific I/O bus. These cables are ended with connector modules that are inserted into connector blocks on the module mounting panels. To insert the cables, access is gained through the rear of the DA10 cabinet. Drawing D-MU-DA10-0-2 (sheet 2) shows where the I/O bus cables are inserted. Drawing D-IC-DA10-0-IOBI (3 sheets) shows the I/O bus interface for the three systems as follows: sheet 1 shows the PDP-9; sheet 2 shows the PDP-10; and sheet 3 shows the PDP-8. Since the DA10 is a part of the three I/O bus systems, the maximum I/O bus cable lengths are as follows: 20 ft for the PDP-8; 100 ft for the PDP-9; and 150 ft for the PDP-10.

3.8.1 PDP-10 I/O Bus Cables

Each PDP-10 bus cable is terminated by two W851 connector modules joined by mechanical hardware to form a cable assembly. Since the I/O bus is looped between the PDP-10 I/O devices, the

I/O bus cable assemblies from a preceding device are connected to the DA10 and the DA10 I/O bus cable assemblies are connected to the next device in the loop. The connections are completed by screwing the connector assemblies into the appropriate card slots. The margin cable and remote turn-on cable are also looped between the PDP-10 options to complete the margin and remote turn-on circuits. Table 3-1 indicates the location of the PDP-10 I/O bus cables in the DA10.

Table 3-1
PDP-10 I/O Bus Cables

I/O Bus Cable Assembly	Connector Module	DA10 Card Slots	
1	1A and 1B	EF25	EF29
	1C and 1D	EF26	EF30
2	2A and 2B	EF27	EF31
	2C and 2D	EF28	EF32

3.8.2 PDP-9 I/O Bus Cables

Each PDP-9 I/O bus cable is terminated by two W850 connector modules joined by mechanical hardware to form a cable assembly. A set of PDP-9 I/O bus cables are required to interface the PDP-9 to the DA10. The connections are completed by screwing the connector assemblies into the appropriate DA10 card slots shown in Table 3-2.

Table 3-2
PDP-9 I/O Bus Cables

I/O Bus Cable Assembly	Connector Module	DA10 Card Slots	
1	1A and 1B	EF13	EF17
	1C and 1D	EF14	EF18
2	2A and 2B	EF15	EF19
	2C and 2D	EF16	EF20

3.8.3 PDP-8 I/O Bus Cables

Each PDP-8 I/O bus cable is terminated by a W021 connector module. A set of cables are required to interface the PDP-8 to the DA10. The connection is completed by inserting the connector module into the appropriate card slot shown in Table 3-3.

Table 3-3
PDP-8 I/O Bus Cables

Connector No.	DA10 Card Slots	
1	E01	E07
2	E02	E08
3	E03	E09
4	E04	E010
5	E05	E011
6	E06	F06
7	F01	F07
8	F02	F08
9	F03	F09
10	F04	F10
11	F05	F11

3.9 ONE-SHOT ADJUSTMENT

The DA10 contains two one-shots as a part of the test logic. They are located on an R302 Delay module mounted in card slot A10. Because these one-shots are a part of the test logic, they do not affect the data transfer operation. If the one-shots are adjusted incorrectly, they could cause the self-test to fail. During factory checkout, the trimpots on the delay modules are adjusted to the maximum clockwise position (looking at the back of the module) and should remain in that position after shipment. When the DA10 is installed, the adjustment of the trimpots should be checked for correct adjustment before self-test is performed.

CHAPTER 4
THEORY OF OPERATION

A functional description of the DA10 Interface on a simplified block diagram level is presented in the following paragraphs. This is followed by detailed theory information referencing both detailed block diagrams and the logic block diagrams that are contained in the Peripheral Device Engineering Drawing Set, Volume IV, Doc. No. DEC-10-I6DA-D.

4.1 FUNCTIONAL DESCRIPTION

Figure 4-1 is a simplified block diagram of the DA10 Interface connected to a PDP-8 or PDP-9 processor. The DA10 contains two 36-bit buffers (FM10 and TO10), five status flags (located in the status register), and the control logic necessary for device selection and data transfer. To simplify the following discussion, all PDP-10 instructions and IOT instructions are performed by the central processor under program control.

Since data can be transferred through the DA10 in either direction, a data transfer from a PDP-10 is discussed first. When a transfer from a PDP-10 is to be executed, the PDP-10 central processor performs a DATAO instruction, during which the following events occur: a 36-bit data word is sent to the FM10 buffer via the I/O bus and the input buffering circuits; the FM10 buffer is cleared; the data from the input buffering circuits is loaded into the FM10 buffer; and the FM10 FULL flag is set. When the FM10 FULL flag is set, a program interrupt request (PI RQ) signal is sent to the PDP-8 or PDP-9 central processor.

After receiving the PI RQ signal, the PDP-8 or PDP-9 central processor enters a programmed routine to sequentially check the status flags connected to the PI line by performing a series of IOT instructions. When the IOT instruction that checks the FM10 FULL flag is performed, the skip logic generates a skip request (SKIP RQ) signal and program control is transferred to the appropriate service routine.

The PDP-8 or PDP-9 central processor completes the service routine by performing a series of IOT instructions. Each IOT instruction enables the data transfer logic to generate a READ pulse that is sent to the FM10 buffer. Each READ pulse transfers a portion of the data in the 36-bit FM10 buffer to the PDP-8 or PDP-9 central processor via the I/O bus. In the case of a PDP-9, the read request gate generates a RD RQ signal that is required by the PDP-9 during a data transfer.

When a PDP-8 is connected to the DA10, three IOT instructions are performed to fetch three 12-bit data words. When a PDP-9 is connected to the DA10, two IOT instructions are performed to fetch two 18-bit data words.

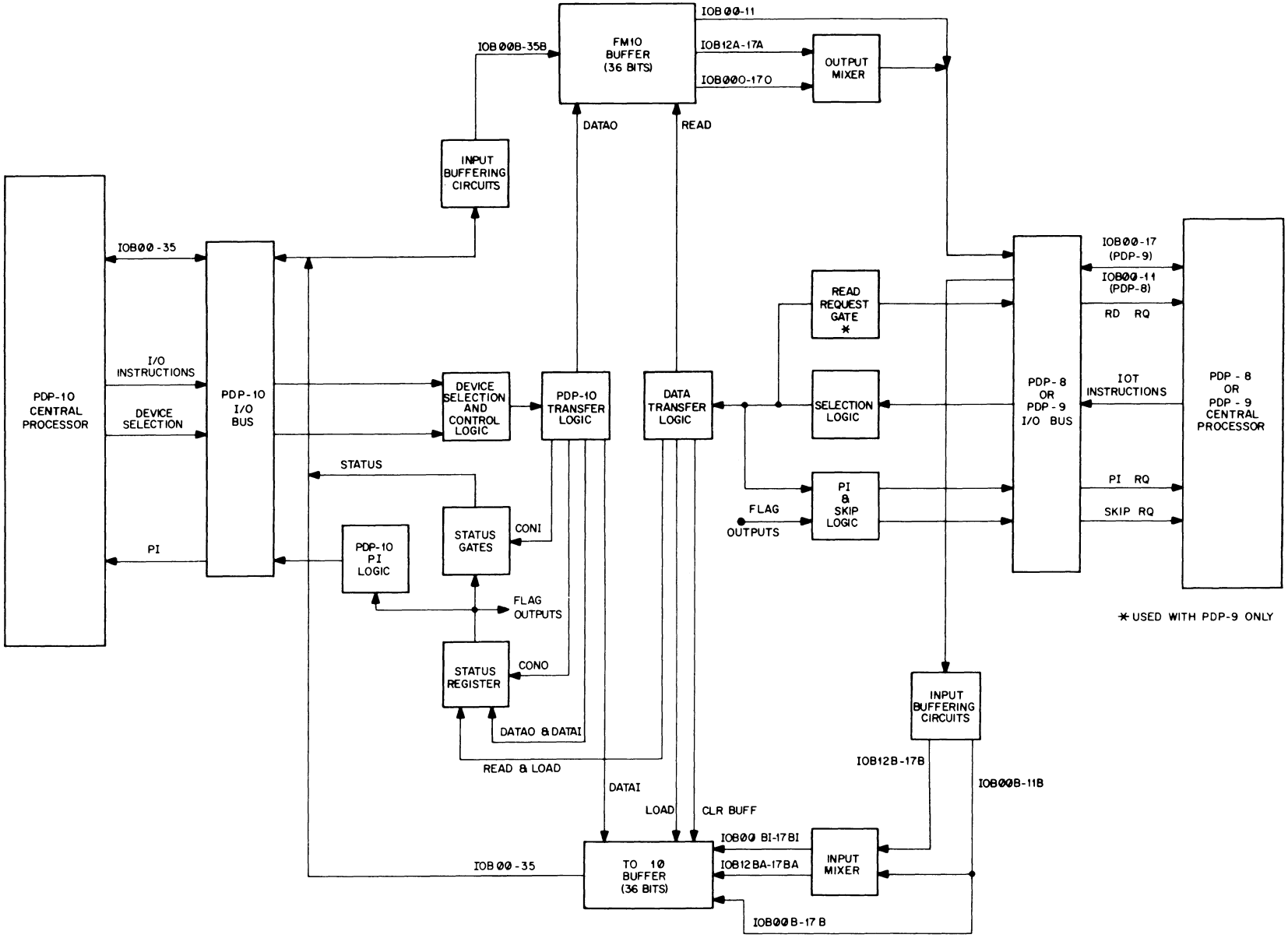


Figure 4-1 DA10 Interface - Simplified Block Diagram

During the last IOT instruction, the READ pulse is sent to the status register to set the FM10 EMPTY flag and clear the FM10 FULL flag. The FM10 EMPTY flag enables the PDP-10 PI logic and a program interrupt request (PI) signal is sent to the central processor.

The PDP-10 central processor performs a CONI instruction to fetch the status information via the I/O bus and detects that the FM10 EMPTY flag is set. If the PDP-10 central processor has additional data to be transferred, it places the next data word on the I/O bus and performs a DATAO instruction as explained above. These data transfers continue until the PDP-10 central processor has no additional data for the PDP-8 or PDP-9 central processor. At this time, the PDP-10 central processor may perform a CONO instruction to clear the status flags and remove the PI signal.

To perform a PDP-8 or PDP-9 data transfer to the PDP-10, the central processor performs a series of IOT instructions to load the TO10 buffer. Prior to a data transfer, an IOT instruction is performed to generate a clear buffer (CLR BUFF) pulse. The CLR BUFF pulse clears the 36 flip-flops in the TO10 buffer and clears the TO10 EMPTY flag. Then, the IOT instructions during which the data is transferred are performed.

During each data transfer, the PDP-8 or PDP-9 central processor places a data word on the I/O bus and sends the control signals to the DA10. In the data transfer logic, a LOAD pulse is generated and sent to the TO10 buffer. The LOAD pulses gate the data word into the 36-bit TO10 buffer. Three 12-bit data words are transferred to fill the TO10 buffer when a PDP-8 is connected to the DA10 and two 18-bit data words are transferred when the PDP-9 is connected.

The TO10 FULL flag is set by the last LOAD pulse and the TO10 FULL flag enables the PDP-10 PI logic sending a PI signal to the central processor. After receiving the PI signal, the PDP-10 central processor performs a CONI instruction to fetch the status information. From the status information, the PDP-10 central processor determines that the TO10 buffer is loaded and performs a DATAI instruction to gate the 36-bits of data out of the TO10 buffer and into the central processor via the I/O bus. During DATAI instruction the TO10 EMPTY flag is set and the TO10 FULL flag is cleared.

At this time, the PI signal is removed from the PDP-10 central processor and a PI RQ signal is sent to the PDP-8 or PDP-9 central processor. The PDP-8 or PDP-9 central processor enters a routine to sequentially check the status flags connected to the PI line by performing a series of IOT instructions. When the TO10 EMPTY flag is located in the set condition, program control is transferred to the appropriate service routine and the TO10 buffer is loaded. This action is repeated until the PDP-8 or PDP-9 has completed the necessary transfer of data.

4.2 DETAILED DESCRIPTION

The transfer of data and control information is discussed as data from the PDP-10 to a PDP-8 or PDP-9 and from a PDP-8 or PDP-9 to the PDP-10 processor.

4.2.1 Data Transfer to a PDP-8 (Figure 4-2)

When data is transferred to a PDP-8, the PDP-10 central processor places up to 36-bits of data on data lines IOB 10, IOB 00 through IOB 10, IOB 35; places the DA10 device selection number (014_8) on the device selection lines IOS 3(0) through IOS 9(1) and performs a DATAO instruction. The central processor performs the DATAO instruction in two parts: the IOB 10 DATAO CLR pulse is sent to the DA10 and 1 μs later, the IOB 10 DATAO SET pulse is sent.

The device selection number is decoded in the PDP-10 device selection decoder and the resultant signal, 014 SEL, conditions the DATAO clear enable gate, DATAO set enable gate, and a number of other enable gates. When the IOB 10 DATAO CLR signal is sent to the DA10, the DATAO clear enable gate is enabled generating the DATAO CLR pulse. The DATAO CLR pulse conditions the FM10 buffer to receive the data transfer by clearing the 36 flip-flops in the buffer. If the STAT BUF B flip-flop is set causing a program interrupt request to the PDP-10, the DATAO CLR pulse also removes the program interrupt request by clearing the STAT BUF B flip-flop.

One microsecond later, the IOB 10 DATAO SET signal is sent to the DATAO set enable gate. Since the 014 SEL signal is still true, the DATAO set enable gate is conditioned and the DATAO SET pulse is generated. The DATAO SET pulse performs two major functions. It enables the input gates loading the data on the data lines into the FM10 buffer and sets the STAT BUF A flip-flop.

At this time, the 36 bits of data are loaded into the FM10 buffer and the data is ready to be transferred to the PDP-8 central processor. Since the PDP-8 has a word length of 12 bits, three 12-bit data transfers must be performed to unload the FM10 buffer.

The data transfers from the FM10 buffer to the PDP-8 central processor are performed in the following manner. When the STAT BUF A flip-flop is set, the set side of the flip-flop enables the PI gate sending a program interrupt request (PI RQ) signal to the PDP-8. After receiving the PI RQ signal, the PDP-8 central processor performs a series of IOT instructions to sequentially check the status flags of the various devices connected to its I/O bus.

One of these IOT instructions is IOT 721. When IOT 721 is performed, the signals on lines BMB 3(0) through BMB (1) are decoded, thus generating the 72 SEL signal. The IOP 1 signal, which is a part of IOT 721, is ANDed with the 72 SEL signal and the set side of STAT BUF A flip-flop to generate a skip request (SKIP RQ) signal that is sent to the PDP-8 central processor. After the PDP-8 central processor detects the SKIP RQ signal, program control is transferred to a service routine during which IOT 702, 712, and 722 are performed.

When IOT 702 is performed, the 70 SEL signal is generated in the selection logic and sent to the data transfer logic. In the data transfer logic, the 70 SEL and IOP 2 signals are ANDed and generate the READ A pulse. The READ A pulse enables the output gates for bits 00 through 11 and gates the data to the PDP-8 accumulator register via the PDP-8 I/O bus.

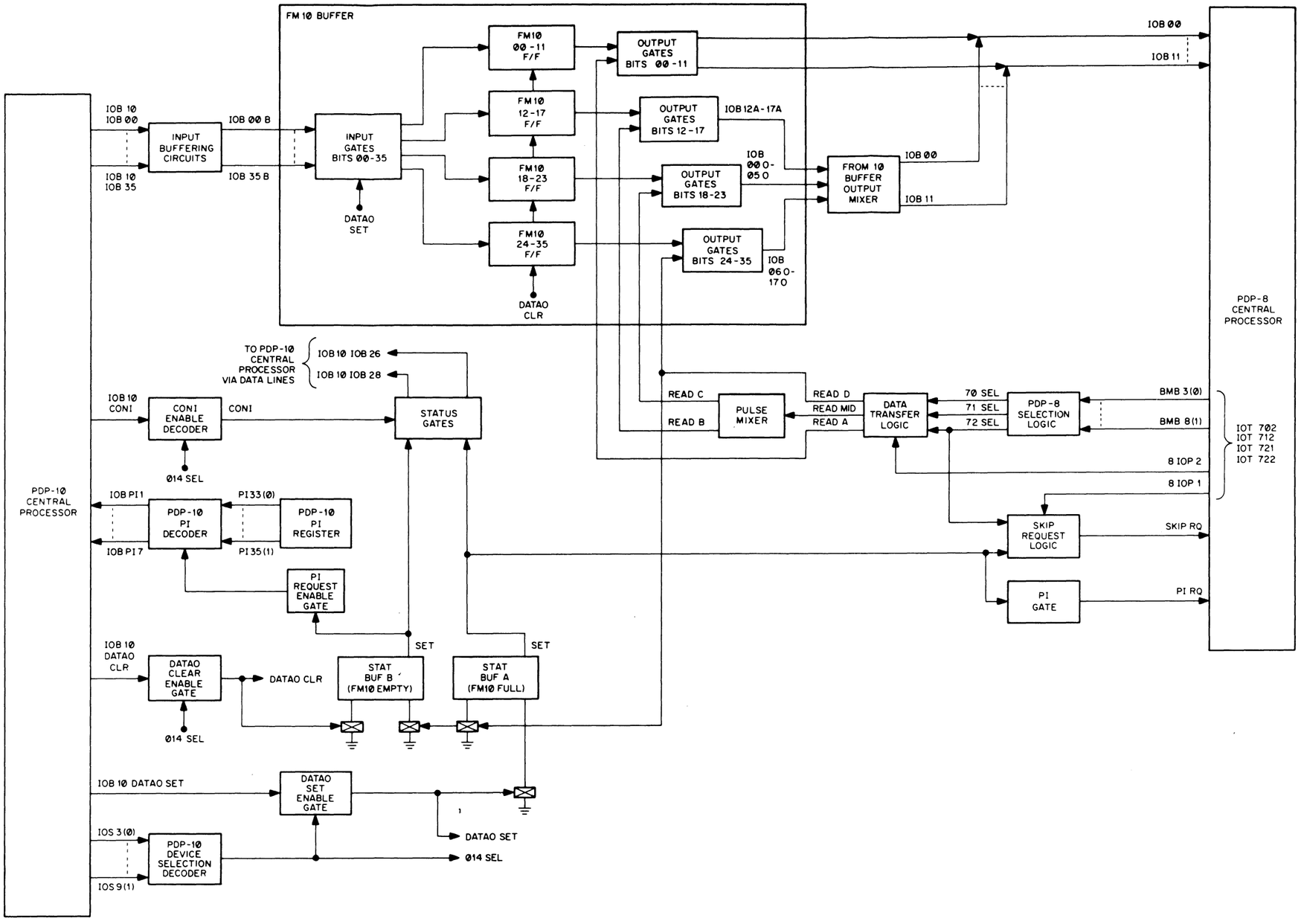


Figure 4-2 Data Transfer from PDP-10 to PDP-8, Simplified Block Diagram

Next, the PDP-8 central processor performs an IOT 712 instruction. The 71 SEL signal is generated in the selection logic and is ANDed with the IOP 2 signal in the data transfer logic generating the READ MID pulse. The READ MID pulse is applied to the pulse mixer, a jumper network, and the READ B and READ C pulses are generated. The READ B pulse enables the output gates for bits 12 through 17 and the READ C pulse enables the output gates for bits 18 through 23. With the output gates enabled, the data in bits 12 through 23 are gated to the PDP-8 accumulator register via the FM10 buffer output mixer and PDP-8 I/O bus.

To perform the last transfer, the PDP-8 central processor performs an IOT 722 instruction. The 72 SEL signal is generated and ANDed with the IOP 2 signal generating the READ D pulse. The READ D pulse enables the output gates for bits 24 through 35 gating the data to the PDP-8 accumulator register via the FM10 buffer output mixer and the PDP-8 I/O bus. At the same time, the READ D pulse clears the STAT BUF A flip-flop and sets the STAT BUF B flip-flop. The set side of the STAT BUF B flip-flop is applied to the PI request enable gate and the PDP-10 PI decoder is enabled. The PI channel assignment number that is stored in the PDP-10 PI register is decoded, and a PI request is sent to the PDP-10 central processor via the assigned line.

The PDP-10 services the PI request by performing a CONI instruction. The DA10 is selected and the 014 SEL signal that conditions the CONI enable gate is generated. When the IOB 10 CONI signal is applied to the CONI enable gate, the CONI signal is generated enabling the status gates. The status information is sent to the PDP-10 central processor via the assigned data lines of the I/O bus. In this case, the significant bit of status information is contained on IOB 10, IOB 28. With this bit a 1, the PDP-10 central processor is provided with an indication that the FM10 buffer is empty and ready to receive the next data transfer. Additional data transfers are performed in an identical manner as explained above.

4.2.2 Data Transfer to a PDP-9

If the DA10 is connected to a PDP-9 instead of a PDP-8, the PDP-10 central processor loads the FM10 buffer in the same manner as it did when a PDP-8 was connected. There are differences in the data transfer from the FM10 buffer to the PDP-9 because the IOT instructions and the word length are different. In this section, the differences in data transfer are explained in detail, and the functions that are the same are only discussed. If additional detail is required to understand the PDP-10 operation, refer to Paragraph 4.2.1.

Reference to Figure 4-3 will help to clarify much of the following discussion. Figures 4-2 and 4-3, show that the PDP-10 interface connections to the DA10 are identical when either a PDP-8 or PDP-9 central processor is connected to the DA10. The PDP-10 central processor places the data and the device selection number on the I/O bus and performs a DATAO instruction to load the data

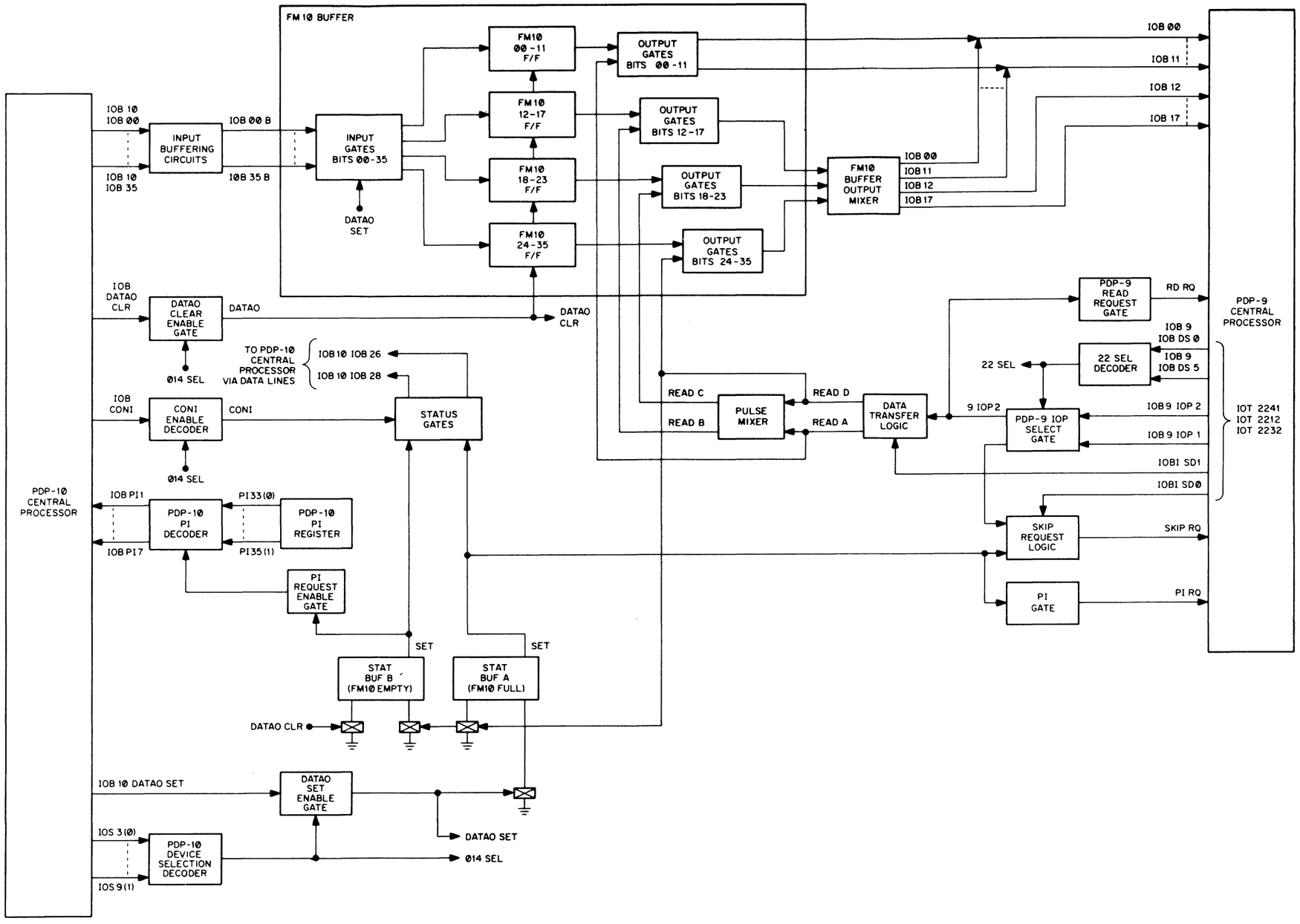
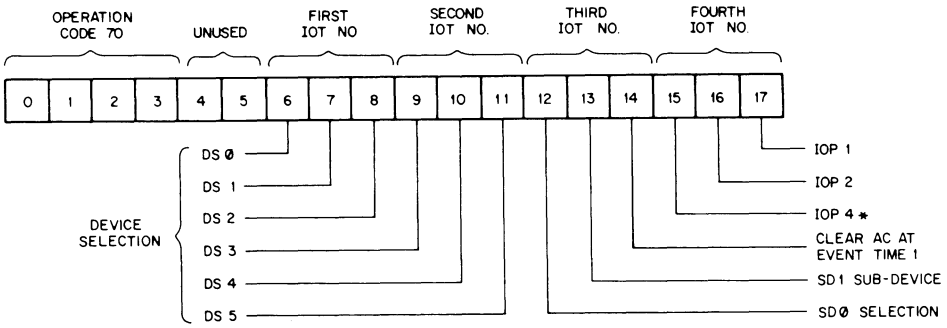


Figure 4-3 Data Transfer from PDP-10 to PDP-9, Simplified Block Diagram

into the FM10 buffer. The DATAO instruction also clears the STAT BUF B flip-flop and sets the STAT BUF A flip-flop. The set side of the STAT BUF A flip-flop is connected to the PI gate and a PI RQ signal is sent to the PDP-9 central processor.

The PDP-9 central processor services the PI request by performing a series of IOT instructions to sequentially check the status flags of the various devices connected to its I/O bus. Refer to Figure 4-4 for the PDP-9 IOT instruction format.



*IOP4 is assigned to this bit because of its binary relationship to the other IOP bits. There is no IOP3.

Figure 4-4 PDP-9 IOT Instruction Format

When the PDP-9 central processor performs IOT 2241, the 22 SEL signal is generated by decoding the signals on the device selection lines IOB 9, IOB DS0 through IOB DS5. The 22 SEL signal enables the IOP select gate generating the 9 IOP 1 signal. The set side of the STAT BUF A flip-flop, the 9 IOP 1 signal and the IOB 1 SD0 signal (a 1 during this instruction) are ANDed in the skip request logic generating the SKIP RQ signal.

After the central processor detects the SKIP RQ signal, program control is transferred to a service routine during which the central processor performs IOT 2212 and IOT 2232.

When IOT 2212 is performed, the PDP-9 central processor clears its accumulator register and places the necessary control signals on the I/O bus. The 22 SEL signal is decoded and ANDed with the IOB 9 IOP 2 signal in the IOP select gate generating the 9 IOP 2 signal. The 9 IOP 2 signal performs two major functions: first, it is applied to the PDP-9 read request gate generating the read request (RD RQ) signal, a 1 μs pulse that is required to complete the data transfer; second, it is ANDed with IOB 1 SD1 (a 0 during this instruction) generating the READ A pulse. The READ A pulse is sent to the pulse mixer to generate the READ B pulse.

The READ A pulse enables the output gates for bits 00 through 11 and the READ B pulse enables the output gates for bits 12 through 17. The data in bits 00 through 11 are placed directly on the

I/O bus, and the data in bits 12 through 17 are placed on the I/O bus via the FM10 buffer output mixer. A brief review of conditions up to this point show that the PDP-9 accumulator register has been cleared, the RD RQ signal has been sent to the PDP-9 central processor, and the data has been placed on the data line of the I/O bus. The PDP-9 central processor allows the data to settle and then strobes the data into the accumulator register to complete the transfer of the first 18-bits of data.

Then, the PDP-9 central processor performs the IOT 2232 instruction to fetch the second 18-bits of data stored in bits 18 through 35 of the FM10 buffer. During the IOT 2232 instruction, the PDP-9 central processor clears the accumulator register and places the necessary control signal on the I/O bus. Again, the 22 SEL signal is decoded and ANDed with the IOB 9 IOP 2 signal in the IOP select gate generating the 9 IOP 2 signal. The 9 IOP 2 signal causes the RD RQ signal to be generated and the READ D pulse to be generated after the 9 IOP 2 signal is ANDed with the IOB 1 SD 1 signal (a 1 during this instruction). The READ D pulse is sent to the pulse mixer to generate the READ C pulse. The READ C pulse then enables the output gates for bits 18 through 23 and the READ D pulse enables the output gates for bits 24 through 35. With the 18 output gates enabled, the second 18 bits of data are gated onto the PDP-9 I/O bus via the FM10 buffer output mixer. After the PDP-9 central processor has allowed time for the data on the I/O bus to settle, it strobes the data into the accumulator register to complete the transfer.

The READ D pulse also clears the STAT BUF A flip-flop to remove the PI RQ signal from the PDP-9; and it sets the STAT B flip-flop to send a PI request to the PDP-10. The PDP-10 services the PI request by performing a CONI instruction to fetch the status information via the data lines. As it was in the case of a PDP-8, IOB 10 IOB 28 is the significant bit of status information because it indicates that the FM10 buffer is empty. Additional data transfers are completed in an identical manner as controlled by the PDP-10 central processor until the required data has been transferred.

4.2.3. Data Transfer From a PDP-8 to a PDP-10

The PDP-8 central processor performs a service routine consisting of a series of IOT instructions to transfer data to a PDP-10 central processor via the DA10. To transfer a full 36-bits of data, the PDP-8 central processor performs the following IOT instructions: IOT 701 to clear the TO10 buffer IOT 704 to load bits 00 through 11; IOT 714 to load bits 12 through 23; and IOT 724 to load bits 24 through 35 and set the STAT BUF C flip-flop. If only a partial transfer is to be performed, IOT 724 must be included to set the STAT BUF C flip-flop and send a PI request to the PDP-10 central processor. (Figure 4-5 should be referenced while reading the following functional description.)

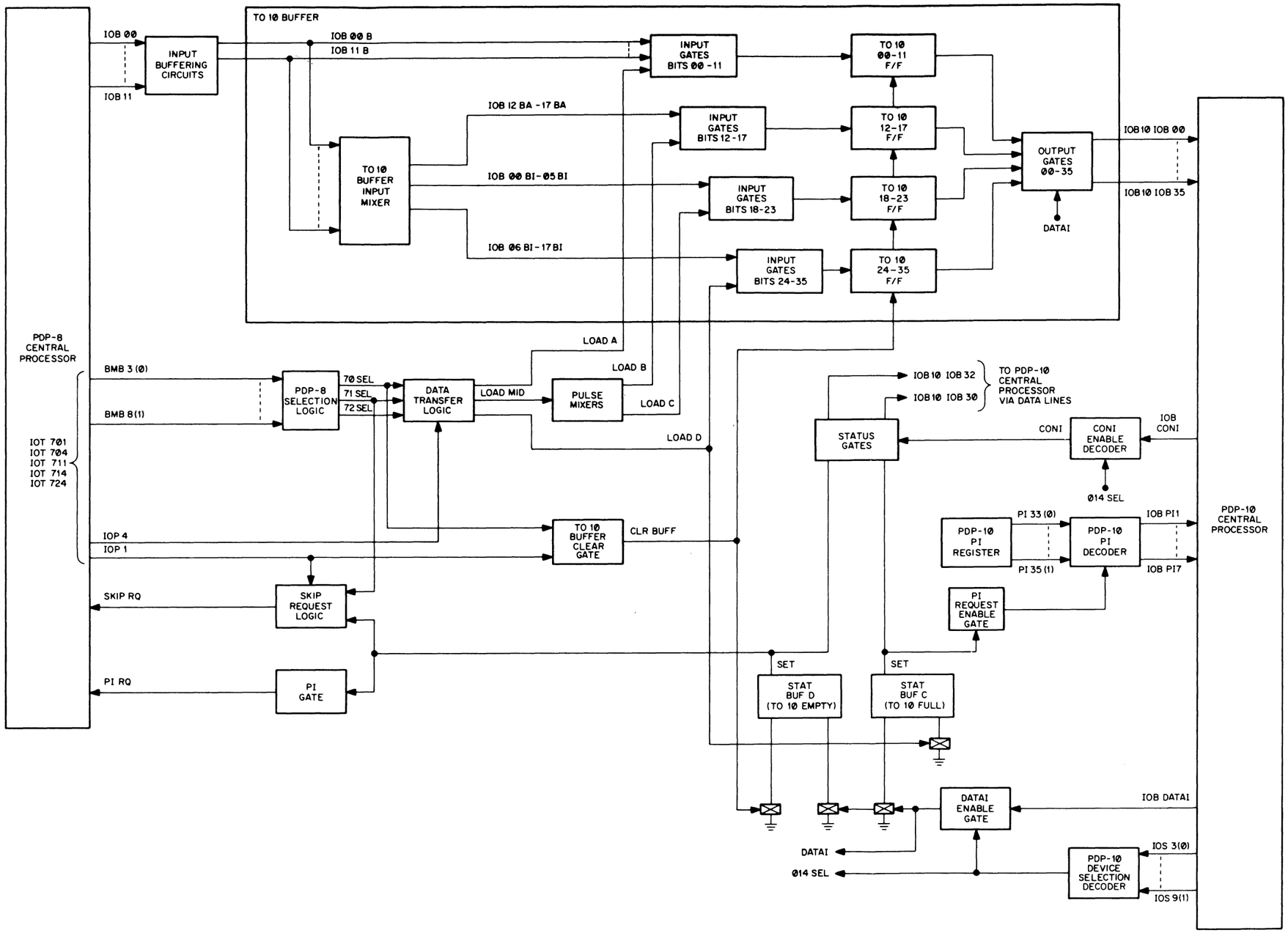


Figure 4-5 Data Transfer from PDP-8 to PDP-10, Simplified Block Diagram

When IOT 701 is performed, the signals on the device selection lines BMB 3(0) through BMB 8(1) are decoded in the selection logic generating the 70 SEL signal. The 70 SEL and IOP 1 signals are ANDed in the TO10 buffer clear gate generating the CLR BUFF pulse. The CLR BUFF pulse performs two major functions. It clears the 36 flip-flops in the TO10 buffer, and it clears the STAT BUF D flip-flop (the STAT BUF D flip-flop will be set if the PDP-8 central processor has received a previous PI RQ signal).

The DA10 is now ready to accept data from the PDP-8. When an IOT 704 instruction is performed, the PDP-8 places 12 bits of data on data lines IOB 00 through IOB 11 and sends the necessary control signals to the DA10. The 70 SEL signal is generated and ANDed with the IOP 4 signal in the data transfer logic generating the LOAD A pulse. When the LOAD A pulse is generated, the input gates for bits 00 through 11 are enabled and the data is loaded into bits 00 through 11.

To load bits 12 through 23, the PDP-8 central processor performs an IOT 714 instruction. The PDP-8 central processor places 12 bits of data on the data lines and the data is routed to input gates 12 through 23 via the input buffering circuits and the TO10 buffer input mixer. When the control signals are sent out, the 71 SEL signal is decoded and ANDed with the IOP 4 signal generating the LOAD MID pulse. The LOAD MID pulse is sent to the pulse mixers to generate the LOAD B and LOAD C pulses.

The LOAD B pulse enables the input gates for bits 12 through 17 and the LOAD C pulse enables the input gates for bits 18 through 23. When the input gates are enabled, the data is loaded into bits 12 through 23.

To complete the loading of the TO10 buffer, the PDP-8 central processor performs an IOT 724 instruction. Again, the data is sent from the PDP-8 to the input gates via the input buffering circuits and the TO10 buffer input mixer. The 72 SEL signal is generated and ANDed with the IOP 4 signal generating the LOAD D pulse. The LOAD D pulse enables the input gates for bits 24 through 35 and loads the data into bits 24 through 35, and it sets the STAT BUF C flip-flop.

When the STAT BUF C flip-flop is set, the PI request enable gate is enabled and the PDP-10 PI decoder is enabled. The PI channel assignment number stored in the PDP-10 PI register is decoded sending a PI request to the PDP-10 central processor via the assigned PI line. The PDP-10 central processor performs a CONI instruction to fetch the DA10 status information. At this time, IOB 10 IOB 30 is a 1 indicating the presence of data in the TO10 buffer.

To fetch the data, the PDP-10 central processor performs a DATAI instruction. The DA10 device number is decoded and the resultant signal, 014 SEL, enables the DATAI enable gate generating the DATAI signal. The DATAI signal enables the output gates for bits 00 through 35 and gates the data onto the PDP-10 I/O bus; it clears the STAT BUF C flip-flop removing the PI request to the PDP-10; and it sets the STAT BUF D flip-flop. The set side of the STAT BUF D flip-flop is applied to the PI gate and a PI RQ signal is sent to the PDP-8 central processor.

The PDP-8 enters a routine during which it checks the status flags of its assigned I/O devices. When IOT 711 is performed, the skip request logic generates a SKIP RQ signal and program control is transferred to the service routine that loads the TO10 buffer. This action is repeated until the PDP-8 central processor has completed the required data transfers.

4.2.4 Data Transfer From a PDP-9 to a PDP-10

To transfer data from a PDP-9 to a PDP-10 via the DA10, the PDP-9 central processor performs a service routine consisting of a series of IOT instructions. Since the PDP-9 word length and IOT instructions are different from those of the PDP-8, there are differences between this transfer and a PDP-8 data transfer. In this section, the complete transfer is discussed but only the differences between PDP-8 and 9 data transfers are explained in detail.

When 36-bits of data are to be transferred to the PDP-10 central processor via the DA10, the PDP-9 central processor performs the following IOT instructions: IOT 2201 to clear the TO10 buffer; IOT 2204 to load bits 00 through 17; and IOT 2224 to load bits 18 through 35 and set the TO10 FULL flag. If only a partial transfer is to be performed, IOT 2224 must be included to set the TO10 FULL flag sending a PI request to the PDP-10 central processor. (Refer to Figure 4-6 while reading the following functional description.

When IOT 2201 is performed, the signals on the device selection lines IOB 9, IOB DS0 through IOB DS5 are decoded generating the 22 SEL signal. The 22 SEL signal is ANDed with the IOB 9 IOP 1 signal in the IOP select gate generating the IOP 1 signal. The IOP 1 signal, then, is ANDed with the IOB 1 SD0 and IOB 1 SD1 signals (both 0 during this instruction) generating the CLR BUFF pulse. The CLR BUFF pulse clears the 36 flip-flops in the TO10 buffer and clears the STAT BUF D flip-flop (STAT BUF D flip-flop will be set if the PDP-9 central processor has received a previous PI RQ signal).

At this time, the DA10 is ready to accept data from the PDP-9. When IOT 2204 is performed, the PDP-9 central processor places up to 18-bits of data on data lines IOB 00 through IOB 17 and sends the necessary control signals to the DA10. The data on line IOB 00 through IOB 11 are sent to the input gates for bits 00 through 11 via the input buffering circuits and to the input gates for bits 18 through 29 via the input buffering circuits and the TO10 buffer input mixer. Data on lines IOB 12 through IOB 18 are sent to the input gates for bits 12 through 17 and bits 30 through 35 via the input buffering circuits and the TO10 buffer input mixer.

The signals on device selection lines are decoded generating the 22 SEL signal. The 22 SEL signal is ANDed with the IOB 9 IOP 4 signal in the IOP select gate generating the IOP 4 signal. Then, the IOP 4 signal is ANDed with the IOB 1 SD1 (a 0 during this instruction) generating the LOAD A

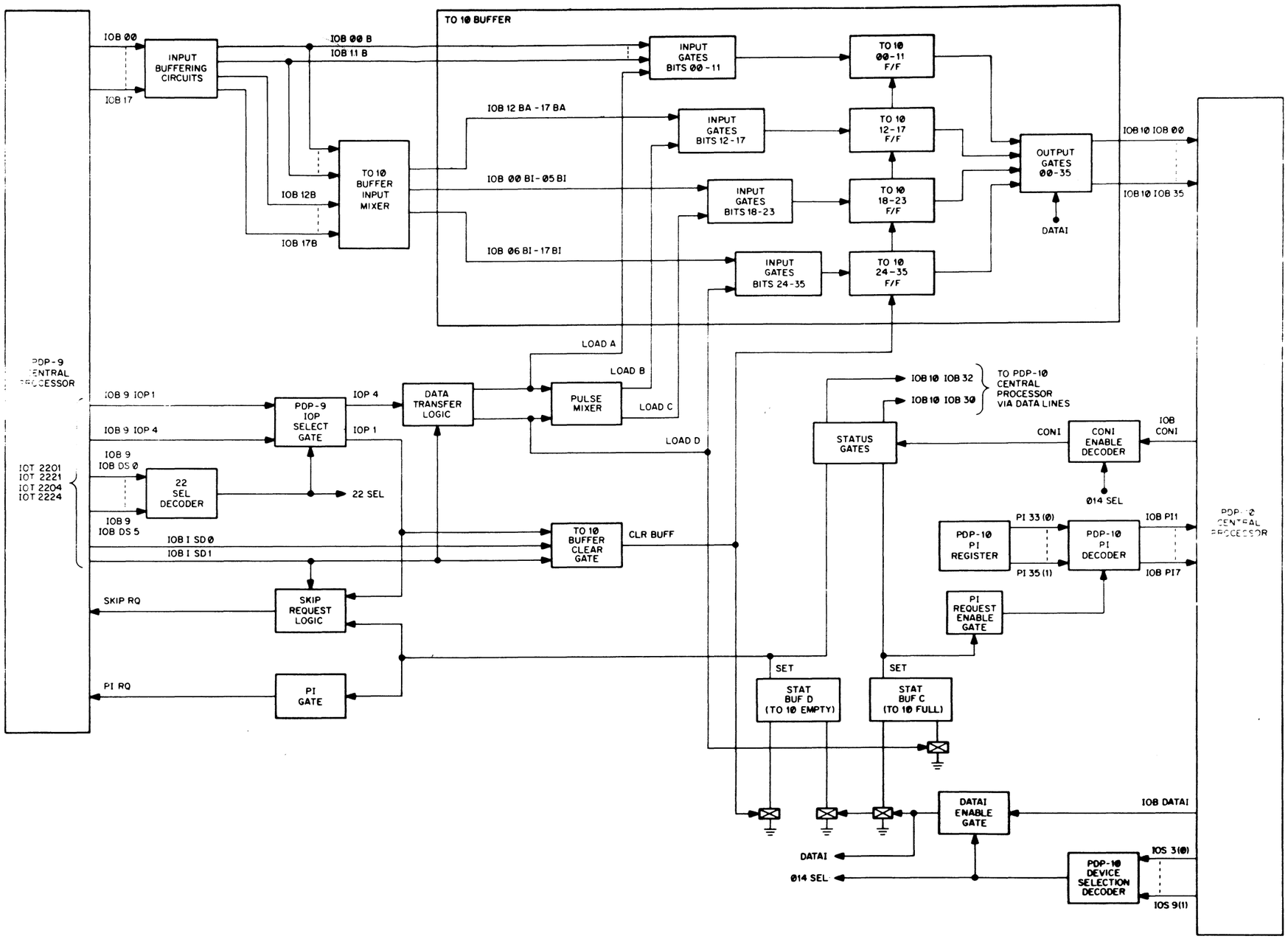


Figure 4-6 Data Transfer from PDP-9 to PDP-10, Simplified Block Diagram

pulse. The LOAD A pulse is applied to the pulse mixer to generate the LOAD B pulse. To load the data on the data lines into the TO10 buffer, the LOAD A pulse enables input gates 00 through 11 and the LOAD B pulse enables input gates 12 through 17. When the input gates are enabled, bits 00 through 17 are loaded into the TO10 buffer.

To load bits 18 through 35, the PDP-9 central processor performs an IOT 2224 instruction. The data is placed on the data lines and the control signals are sent to the DA10. Data is routed to input gates 18 through 35 via the TO10 buffer input mixer. When the control signals are received by the DA10, the 22 SEL signal is generated and ANDed with the IOB 9 IOP 4 signal in the IOP select gate generating the IOP 4 pulse. The IOP 4 pulse is ANDed with the IOB 1 SD1 signal (a 1 during this instruction) in the data transfer logic generating the LOAD D pulse. The LOAD D pulse is divided in the pulse mixer generating the LOAD C pulse. When the LOAD C pulse is generated, input gates for bits 18 through 23 are enabled and the data is loaded into bits 18 through 23. The LOAD D pulse enables input gates for bits 24 through 35 loading the data into bits 24 through 35; and sets the STAT BUF C flip-flop.

The PI request enable gate is enabled by the set side of the STAT BUF C flip-flop enabling the PDP-10 PI decoder. The contents of the PDP-10 PI register is decoded and a PI request is sent to the PDP-10 central processor via the assigned PI line.

To service the PI request, the PDP-10 central processor performs the same instructions that were performed when the PDP-8 was connected to the DA10. A CONI instruction is performed to fetch the status information that indicates the presence of data in the TO10 buffer. Then, a DATAI instruction is performed to fetch the data from the TO10 buffer. At the same time the data is fetched, STAT BUF D is set sending a PI RQ signal to the PDP-9 central processor. After receiving the PI RQ signal, the PDP-9 central processor enters a routine which checks the status flag of its assigned I/O devices. When IOT 2221 is performed, the skip request logic generates a SKIP RQ signal that is sent to the PDP-9 central processor. If the PDP-9 has additional data to be transferred, program control is transferred to a service routine that loads the next data into the TO10 buffer. This action is repeated until the PDP-9 central processor has completed the required data transfers.

4.3 SELF-CHECK OPERATION

The self-check program, Part A of diagnostic program MAINDEC-10-D8A0-D, checks the DA10 operation without the use of the PDP-8 or PDP-9 central processor. During the self-check mode, all the I/O busses are used and are not available for data transfer. The PDP-8 or PDP-9 I/O bus cables are disconnected at the DA10 before the self-check is performed.

In the following discussion, it has been assumed that the strapping in the pulse mixers, the FM10 output mixer and the TO10 input mixer are set for operation with a PDP-8 central processor. If a PDP-9 central processor is connected to the DA10, self-check operation would be similar except the READ MID and LOAD MID pulses would not be used to transfer data. (Refer to Figure 4-7 while reading the following discussion.)

When the DA10 self-check logic is enabled, a loop is closed that starts at and returns to the PDP-10 central processor via the I/O bus. First, the DA10 internal control functions are checked to assure normal operation. A series of known data words, then, are transferred through the loop. The first data is loaded into the FM10 buffer via the PDP-10 I/O bus, transferred from the FM10 buffer to the TO10 buffer via the DA10 internal bus wiring (called the DATA BUS during the discussion), and returned to the PDP-10 central processor. The returned data is compared with the original data to detect errors. This action is repeated with the next data until data has been transferred or an error is detected.

The DA10 internal control functions (DATAO, DATAI, READ D, etc.,) are checked and the data transfers are performed under program control. Because each data transfer is similar, a typical data transfer is explained. To enable the self-check logic, the PDP-10 central processor performs a CONO instruction with a 1 on IOB 24. When the CONO SET pulse is received, the STAT BUF E flip-flop is set conditioning the gates in the self-check logic.

The PDP-10 central processor performs a DATAO instruction. The DATAO CLR pulse clears the FM10 buffer and the STAT BUF B flip-flop. Next, the DATAO SET pulse enables the input gates of the FM10 buffer gating the data lines into the FM10 buffer and sets the STAT BUF A flip-flop.

When the STAT BUF A flip-flop is set, a chain reaction is started which transfers the data from the FM10 buffer to the TO10 buffer. The 1 side of the STAT A flip-flop enables the TLC gate generating the TLC signal. The TLC signal is applied to a pulse amplifier generating the CLR BUFF pulse. When the CLR BUFF pulse is generated, the TO10 buffer is cleared and the TLD gate is disabled. The trailing edge of the CLR BUFF pulse enables the TLD gate and the TLD pulse goes true.

When the TLD pulse goes true, it is applied to a pulse amplifier generating the READ A pulse. The output gates for bits 00 through 11 are enabled by the READ A pulse gating the first byte onto the data bus and the data is allowed to settle. Then, the trailing edge of the READ A pulse enables the TLE gate.

When the TLE gate is enabled, the TLE pulse goes true and is applied to a pulse amplifier generating the LOAD A pulse. The LOAD A pulse enables the input gates for bits 00 through 11 gating the data on the data bus into bits 00 through 11 of the TO10 buffer. At the same time, the LOAD A pulse starts the TLF delay which allows the first data transfer to be completed before the second byte is placed on the data bus.

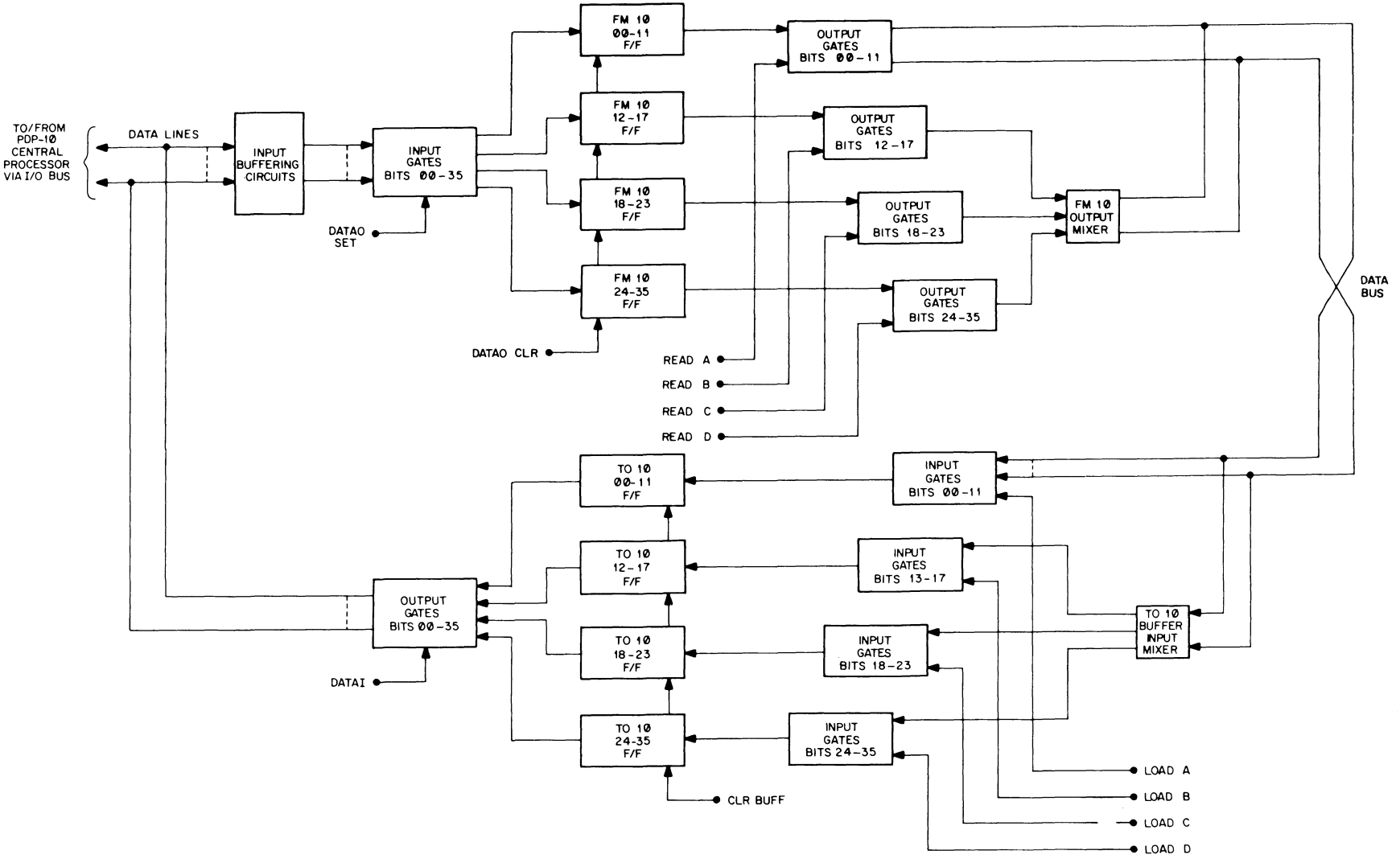


Figure 4-7 DA10 Self-Check Block Diagram (Part 1)

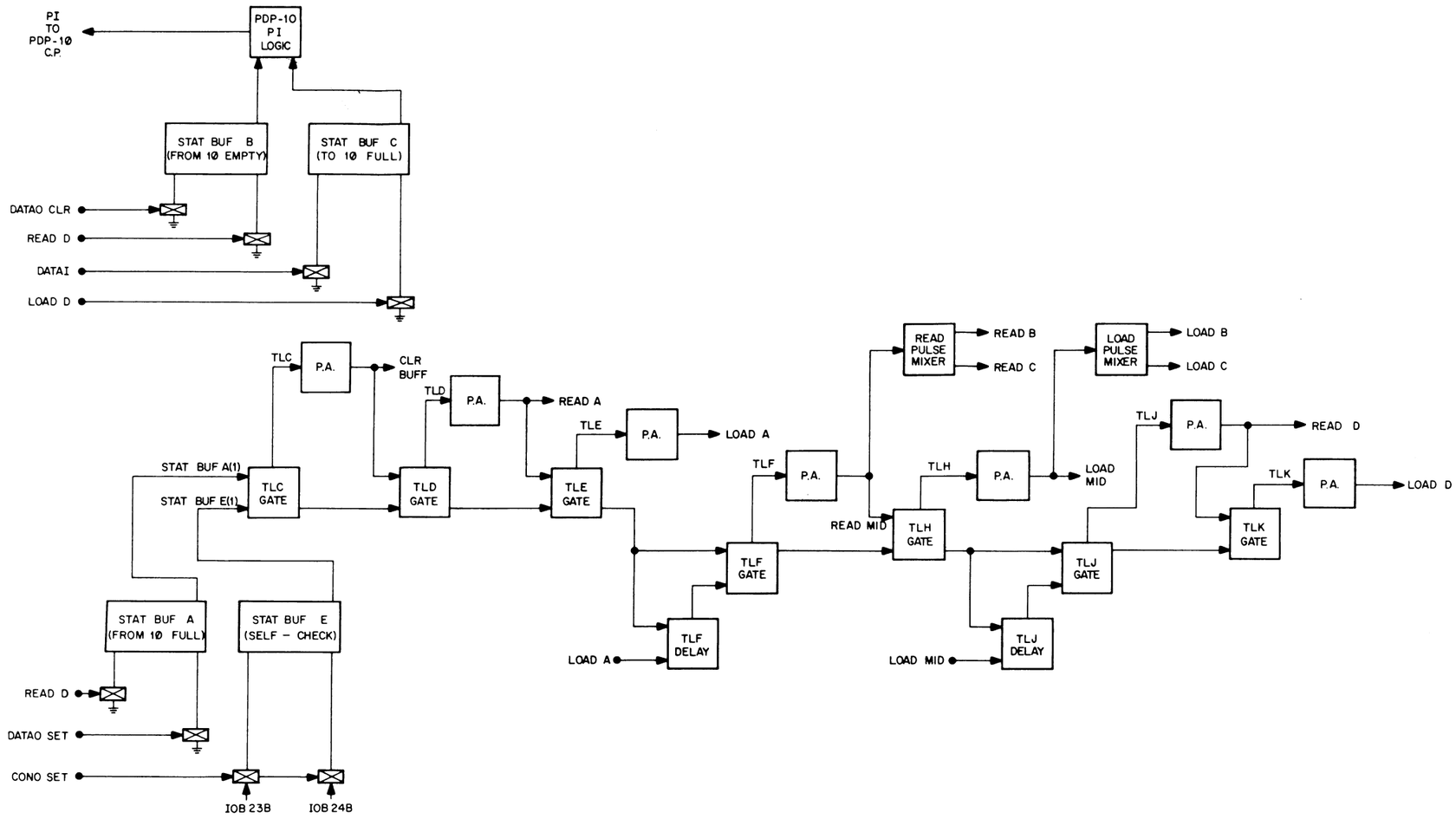


Figure 4-7 DA10 Self-Check Block Diagram (Part 2)

Approximately 400 ns after the TLF delay was started, the output signal from the delay enables the TLF gate causing the TLF pulse to go true. The TLF signal is applied to a pulse amplifier generating the READ MID pulse. The READ MID pulse is applied to the read pulse mixer generating the READ B and READ C pulses. The READ B pulse enables the output gates for bits 12 through 17 and the READ C pulse enables the output gates for bits 18 through 23. With the output gates enabled, the second byte, bits 12 through 23, is gated onto the data bus.

The trailing edge of the READ MID pulse enables the TLH gate generating the TLH pulse. The TLH pulse is applied to a pulse amplifier generating the LOAD MID pulse. When the output of the pulse amplifier is applied to the load pulse mixer, the LOAD B and LOAD C pulses are generated. The LOAD B pulse enables the input gates for bits 12 through 17 and the LOAD C pulse enables the input gates for bits 18 through 23. With the input gates enabled, the data on the data bus is gated into bits 12 through 23 of the TO10 buffer.

The LOAD MID pulse also starts the TLJ delay. Approximately 400 ns later, the output signal from the delay enables the TLJ gate generating the TLJ pulse. The TLJ pulse is applied to a pulse amplifier generating the READ D pulse. When the READ D pulse is applied to the output gates for bits 24 through 35, the third byte is gated onto the data bus. The READ D pulse also clears the STAT BUF A flip-flop and sets the STAT BUF B flip-flop.

The trailing edge of the READ D pulse enables the TLK gate and the TLK pulse goes true. The TLK pulse is sent to a pulse amplifier generating the LOAD D pulse. When the LOAD D pulse is generated, two major functions are performed: the input gates for bits 24 through 35 are enabled gating the third byte into the TO10 buffer; and the STAT BUF C flip-flop is set.

At this time, the data from the FM10 buffer has been transferred to the TO10 buffer and is ready to be fetched by the PDP-10 central processor. Since the STAT BUF C flip-flop is set, the PDP-10 decoder is enabled sending a PI signal to the central processor.

The PDP-10 central processor performs a CONI instruction to fetch the status information and detects the presence of data in the TO10 buffer. To fetch the data, the PDP-10 central processor performs a DATAI instruction during which the following functions are performed: the output gates of the TO10 buffer are enabled gating the data to the PDP-10 central processor via the I/O bus; and the STAT BUF C flip-flop is cleared.

The PDP-10 central processor checks for erroneous data by comparing the data from the TO10 buffer with the data that was sent to the FM10 buffer and causes a printout to be generated. If an error(s) has been detected, the printout is useful in relating the failure to the program listing.

After the printout is completed, the program enters a routine suitable for scoping, and maintenance personnel may perform troubleshooting procedures to locate the malfunction(s). After repairs have been completed, the self-check may be repeated to assure normal operation.

4.4 POWER TURN-ON AND INITIALIZATION

Figure 4-8 is a simplified block diagram of the power turn-on circuits and the CONO instruction.

When power is applied to the Type 844 Power Control, it is applied to the DA10 logic, but a normally closed (NC) contact in the power control remains in the NC position for 4s. During the 4s delay, the output signal from the NC contact, CONTRL OFF, holds the five STAT BUF flip-flops and the three PI register flip-flops in the cleared condition.

During the 4s delay, the PWR UP one-shot returns to the 0 state. The output signal from the PWR UP one-shot is sent to a pulse amplifier generating the CONO CLR pulse. The CONO CLR pulse is sent to the direct clear inputs of the PI register (PI 33 through PI 35) flip-flops clearing the register.

When input power to the power control is lost or turned-off, the NC contact in the power control closes and power to the DA10 logic remains on for 4s. With the NC contact closed, the CONTROL OFF signal is true and is used to clear the STAT BUF flip-flop and the PI register.

The DA10 may be conditioned under program control during a PDP-10 CONO instruction (i.e., the STAT BUF flip-flops may be set or cleared and/or the PI channel assignment number may be loaded into the PI storage register). During the CONO instruction, DA10 device selection number from the PDP-10 is decoded conditioning the CONO clear and CONO set enable gates; the input gates to the STAT BUF flip-flops are conditioned by signal sent over data lines 23 through 32 (e.g., IOB 23 is a 1 if STAT BUFF E is to be cleared, IOB 28 is a 1 if STAT BUF B is to be set); the PI channel assignment number is placed on data lines 33 through 35; the CONO CLR pulse is sent to the DA10; 1 μs after the CONO CLR pulse, the CONO SET pulse is sent.

When the IOB 10 CONO CLR pulse is sent, the CONO CLR pulse is generated and the PI register is cleared. One microsecond later, the input gates that were conditioned are enabled by the CONO SET pulse. At this time, the STAT BUF flip-flops are set or cleared according to the signals on the data lines and the PI channel assignment number is strobed into the PI register.

The last function shown on Figure 4-8 is the IOB RESET. The PDP-10 central processor generates the IOB RESET pulse in any of several ways (e.g., during PDP-10 power turn-on or turn-off) and places it on its I/O bus. In the DA10, the IOB RESET pulse is applied to the direct set input of the STAT BUF flip-flops clearing the five flip-flops and is used to generate the CONO CLR pulse. The CONO CLR pulse is used to clear the PI register.

4.5 LOGIC BLOCK DIAGRAMS

The logic block diagrams for the DA10 interface are contained in Volume IV of the Peripheral Device Engineering Drawing Set, Doc. No. DEC-10-I6DA-D. These drawings contain mnemonics and

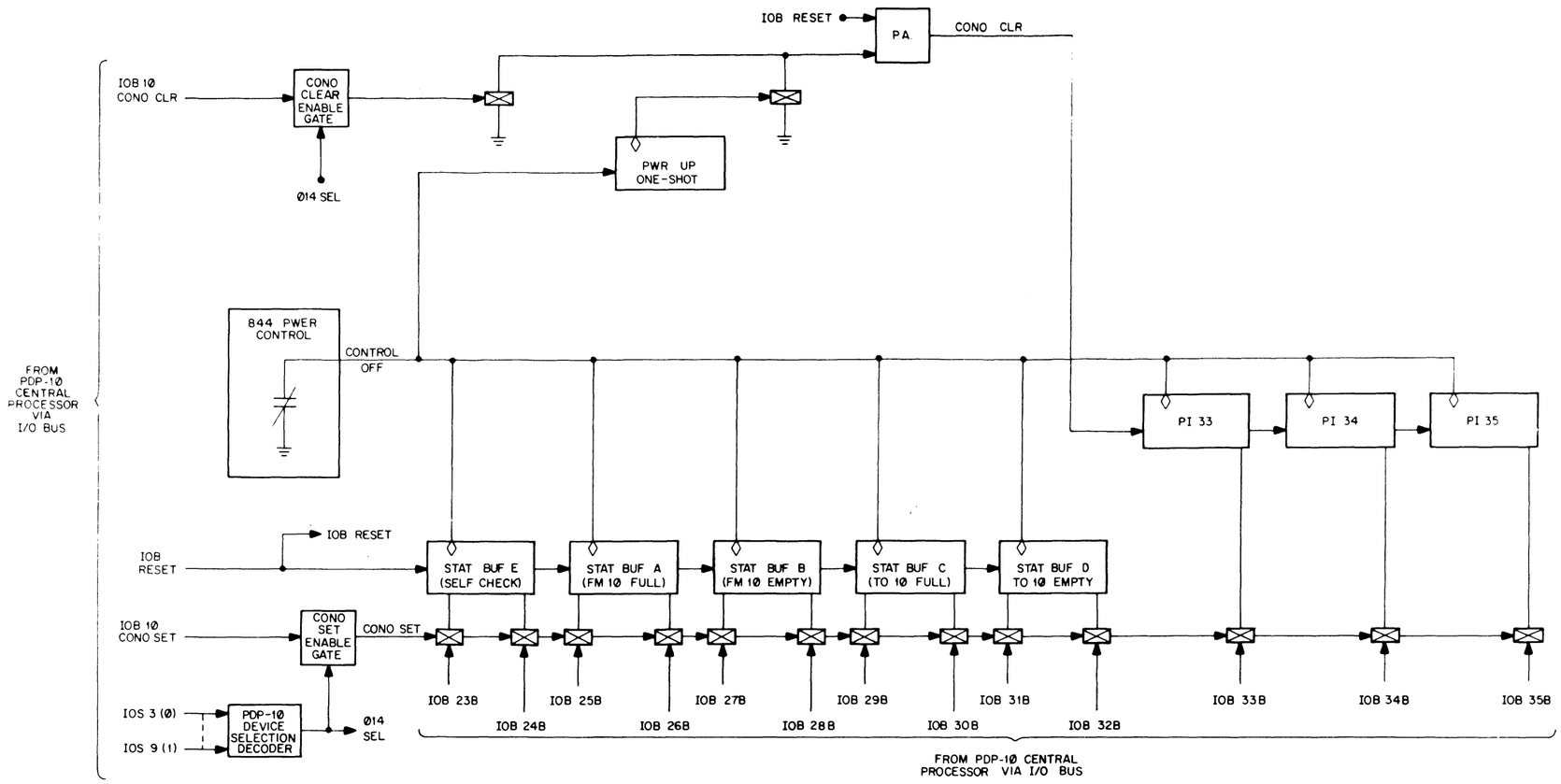
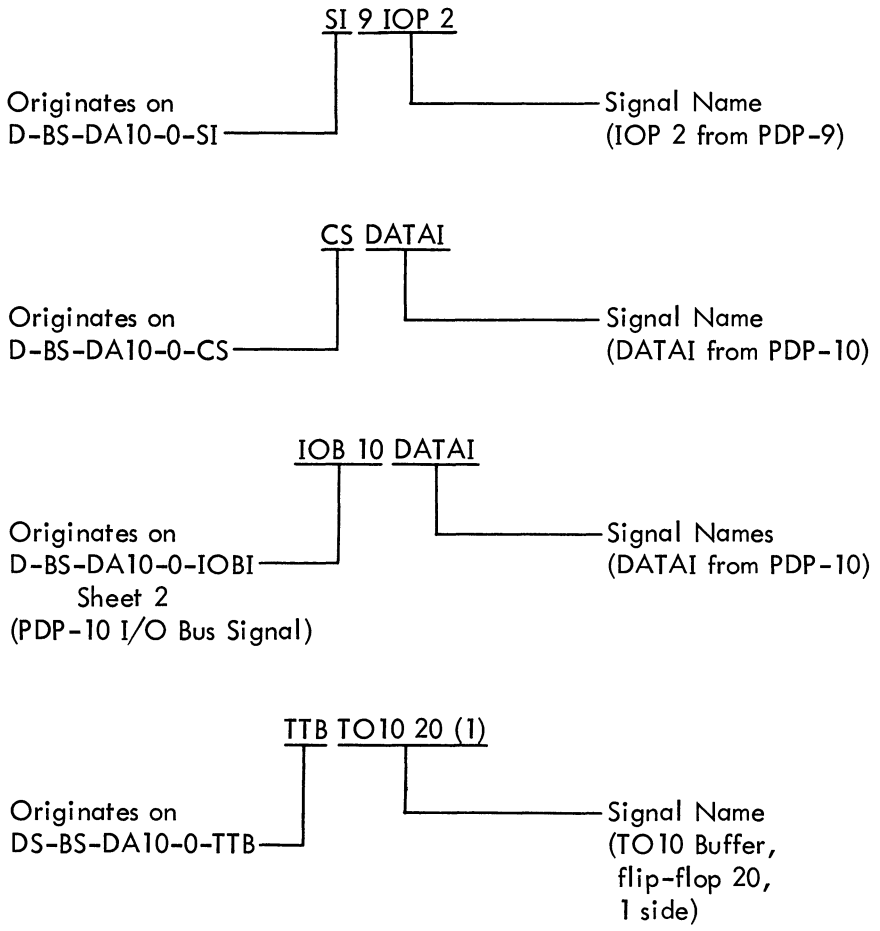


Figure 4-8 Power Up and CONO Instruction, Simplified Block Diagram

codes which are used to identify signal origins, module types, and module locations. The detailed descriptions, schematic diagrams, and specifications of the special modules used in the DA10 are in Volume III of the PDP-10 Maintenance Manual, Doc. No. DEC-10-HMCA-D.

4.5.1 Signal Mnemonics

The signal name is prefixed by a series of letters or numbers. This prefix is the drawing title abbreviation of the engineering drawing where the signal originated. To allow input signals to be traced to their point of origin, an example of the signal name system is as follows.



4.5.2 Logic Functions

The following paragraphs describe the logic functions contained on the drawings listed in parentheses in the paragraph title.

4.5.2.1 Control and Selection (D-BS-DA10-0-CS) - This drawing shows the logic circuits that receive the PDP-10 signals. In the upper left-hand corner, the PDP-10 device selection decoder is shown. The 36 I/O bus receiver circuits that make up the input buffering circuits are shown at the top of the drawing. Then, DATAO, DATAI, CONO, and CONI enable gates are shown at the bottom.

4.5.2.2 Data Transfer Logic (D-BS-DA10-0-DTL) - The data transfer logic that reads the FM10 buffer and loads the TO10 buffer is shown on this drawing along with the power-up circuit. The TO10 buffer clear gate at the top of the drawing is enabled during a PDP-8 IOT 701 instruction or during a PDP-9 IOT 2201 instruction. The READ pulses are generated by the logic shown in the middle of the drawing. These pulses are generated as follows: a PDP-8 IOT 702 instruction or a PDP-9 IOT 2212 instruction generates the READ A pulse; a PDP-8 IOT 712 instruction generates the READ MID pulse; and a PDP-8 IOT 722 instruction or a PDP-8 IOT 2232 instruction generates the READ D pulse. During the PDP-9 IOT 2212 and PDP-9 IOT 2232 instructions, the SI 9 IOP 2 signal enables the PDP-9 read request gate (shown on the right-hand side of the drawing) generating the RD RQ signal required by the PDP-9 central processor.

When data is transferred to a PDP-9, the data must be on the PDP-9 I/O bus for approximately 1 μs. To fulfill this requirement, the DTL READ A pulse is applied to the W640 module located in slot A17 generating the 1 μs wide DTL 9 READ pulse. After passing through the data transfer pulse mixer, the resultant pulse (DTPM READ AX) is used to generate the DTL READ A pulse. The DTL READ A pulse enables the FM10 buffer output gates for bits 00 through 17 and places the data on the PDP-9 I/O bus for 1 μs. The DTL READ D pulse is used in a similar manner to generate the DTL READ D pulse that places the data in bits 18 through 35 on the PDP-9 I/O bus for 1 μs.

The LOAD pulses are generated by the logic shown at the bottom of the drawing. These pulses are generated in the following manner: when a PDP-8 is interfaced with the DA10, IOT 704 generates LOAD A, IOT 714 generates LOAD MID, and IOT 724 generates LOAD D; when a PDP-9 is interfaced with the DA10, IOT 2204 generates LOAD A and IOT 2224 generates LOAD D.

4.5.2.3 Data Transfer Pulse Mixers [D-BS-DA10-0-DTPM (2 Sheets)] - This two-sheet drawing shows the strapping arrangement of the pulse mixer. Sheets 1 and 2 show the PDP-8 and PDP-9 configurations respectively. For a detailed discussion of the strapping for data transfer pulse mixers, see Paragraph 3.5.

4.5.2.4 FM10 Buffer Output Mixer [D-BS-DA10-0-FBOM (2 Sheets)] - On this two-sheet drawing, the strapping arrangements of the FM10 buffer output mixer are shown. Sheets 1 and 2 show the PDP-8 and PDP-9 configurations, respectively. For a detailed discussion of the strapping for the FM10 buffer output mixer, refer to Paragraph 3.6.

4.5.2.5 FM10 Buffer [D-BS-DA10-0-FTB (2 Sheets)] - The 36 flip-flops of the FM10 buffer, the 36 input gates and the 36 output gates are shown on this drawing. The buffer is loaded by the DATAO SET pulse from the PDP-10 and is read in the following manner: bits 00 through 11 by the READ A pulse; bits 12 through 17 by the READ B pulse; bits 18 through 23 by the READ C pulse; and bits 24 through 35 by the READ D pulse.

4.5.2.6 DA10 Indicators (D-BS-DA10-0-IND) - This drawings shows the signals on the seven indicator cables. Each signal name identifies the signal and the location of its origin.

4.5.2.7 I/O Bus Interface [D-BS-DA10-0-IOBI (3 Sheets)] - The I/O bus signals from the three central processors are shown on this drawing. Sheet 1 shows the PDP-9 I/O bus signals, sheet 2 shows the PDP-10 I/O bus signals, and sheet 3 shows the PDP-8 I/O signals.

4.5.2.8 Selection and IOT (D-BS-DA10-0-SI) - This drawing contains the logic for a number of PDP-8 and PDP-9 selection and control functions. The three device selection decoders contained in the PDP-8 selection logic are shown in the upper-left hand corner. The input signals to the PDP-8 decoders come from the two PDP-8 device selection cards shown in the lower right-hand corner. Paragraph 3.4.1 presents a detailed discussion of the PDP-8 device selection cards. In the upper right-hand corner, there are 18 I/O bus receiver circuits. When a PDP-8 central processor is connected to the DA10, the first 12 bus receiver circuits act as input buffers for the PDP-8 I/O bus signal and all 18 bus receiver circuits are used when the PDP-9 is interfaced with the DA10. The 22 SEL decoder that decodes the signals on the PDP-9 device selection lines is shown in the lower left-hand corner. When the PDP-9 sends out a 22_8 over its device select lines, the output signals from the 22 SEL decoder enables the three IOP selection gates shown just above and to the right of the decoder. The remaining logic shown on this drawing are six inverters at the bottom center of the drawing and two OR circuits that generate an indicator signal when a PDP-8 or PDP-9 has selected the DA10.

4.5.2.9 SKP and I/O Status Logic (D-BS-DA10-0-SISL) - This drawing contains the DA10 status logic and the PDP-8/PDP-9 skip request logic. Seven of the eight status gates are shown at the top of the drawing. These status gates are enabled during the performance of a PDP-10 CONI instruction, and the status information is sent to the PDP-10 central processor via the data lines of the PDP-10 I/O bus. The DA10 status register is shown in the center of the drawing. The status register consists of four status flags and the PDP-10 PI register, the PDP-10 PI decoder and the PI request enable gate. The status flags (STAT BUF A through STAT BUF D) are set and/or cleared during the data transfers to indicate the condition of the FM10 and/or TO10 buffers. These flags may also be set or cleared under

the PDP-10 program control during the performance of a PDP-10 CONO instruction. The PDP-10 PI channel assignment number may be loaded into the PDP-10 PI register (PI 33 through PI 35) during the performance of a PDP-10 CONO instruction. When the FM10 EMPTY or TO10 FULL flags are set, then the PI request enable gate enables the PDP-10 PI decoder (DC DR) sending a PI request to the central processor via the assigned PI channel of the PDP-10 I/O bus. The last major functions shown at the bottom of this drawing is the PDP-8 and PDP-9 skip request logic. A SKIP RQ signal is sent to the PDP-8 central processor under the following conditions: if an IOT 711 instruction is performed when the TO10 EMPTY flag is set; or if an IOT 721 instruction is performed when the FM10 FULL flag is set. A SKIP RQ signal is sent to the PDP-9 central processor if an IOT 2221 is performed when the TO10 EMPTY flag is set; or if an IOT 2241 is performed when the FM10 FULL flag is set.

4.5.2.10 TO10 Buffer [D-BS-DA10-0-TTB (2 Sheets)] - This drawing shows the 36 input gates and the 36 output gates. The TO10 buffer is loaded in the following manner: bits 00 through 11 are loaded by the LOAD A pulse; bits 12 through 17 are loaded by the LOAD B pulse; bits 18 through 23 are loaded by the LOAD C pulse; and bits 24 through 35 are loaded by the LOAD D pulse. To fetch the data in the TO10 buffer, the PDP-10 central processor performs a DATAI instruction enabling the output gates and placing the data on the data lines of the PDP-10 I/O bus.

4.5.2.11 TO10 Buffer Input Mixer [D-BS-DA10-0-TBIM (2 Sheets)] - The strapping arrangements of the TO10 buffer input mixer are shown on this drawing. Sheets 1 and 2 show the PDP-8 and PDP-9 configurations respectively. Refer to Paragraph 3.7 for a detailed discussion of the strapping for the TO10 buffer input mixer.

4.5.2.12 Test Logic (D-BS-DA10-0-TL) - This drawing contains the test logic that is utilized during the self-check mode. The self-check enable flip-flop (STAT BUFF E) can be set or cleared under PDP-10 program control. When the flip-flop is set, a loop is closed that starts at and returns to the PDP-10 central processor via the PDP-10 I/O bus. Refer to Paragraph 4.3 for a detailed discussion of the self-check logic. The eighth status gate is shown in the lower middle of this drawing. This gate is enabled during a PDP-10 CONI instruction indicating the condition of the self-check enable flip-flop.

CHAPTER 5
MAINTENANCE

This section contains the general maintenance information for the DA10 Interface. The maintenance information is grouped into preventive and corrective procedures. The corrective maintenance procedures refer to the diagnostic program MAINDEC-10-D8A0-D which exercises the interface and indicates on a printer the area and content of the error.

5.1 PREVENTIVE MAINTENANCE

The DA10 requires standard test equipment, hand tools, cleaners, standard test cables and probes that are considered a part of every well-equipped maintenance activity.

Preventive maintenance consists of tasks performed prior to the initial operation of the DA10 and periodically during its life to insure that the equipment is in satisfactory operating condition. Performance of these tasks forestalls possible future failures by correcting minor damage and discovering progressive deterioration at an early stage. A log book used to record data found during the performance of each preventive maintenance task will indicate the rate of circuit deterioration and provide information which will enable maintenance personnel to determine when components should be replaced to prevent failure of the equipment. All preventive maintenance tasks should be performed as a function of conditions at the installation site, including average usage of the DA10, and the down-time limitations of the equipment. Perform the mechanical checks at least once each month or as often as required to maintain efficient functioning of the cooling equipment. All other tasks should be performed on a regular schedule, at an interval determined by the average usage and the reliability requirements of the system. For a typical application, a schedule of every four months or 1000 equipment operating hours, whichever occurs first, is suggested.

5.1.1 Mechanical Checks

The following steps should be performed during a mechanical check, and the indicated corrective action should be performed, if a substandard condition is located.

a. Clean the exterior and the interior of each equipment cabinet by using a vacuum cleaner or clean cloths that are moistened in nonflammable, nonconductive solvent. Be sure the solvent is not harmful to paint.

b. Clean dirt from the blower assemblies using care not to damage cable assemblies or modules.

c. Visually inspect the equipment for completeness and general condition. Repaint any scratched or corroded areas.

d. Inspect all wiring and cables for cuts, breaks, fraying, deterioration, kinks, strain, and mechanical security. Tape, solder, or replace any defective wiring.

e. Inspect each row of modules to assure that each module is securely seated in its connector.

f. Verify that the proper I/O bus cables and all other interconnecting cables are firmly seated in their respective connectors.

g. Inspect power supply capacitors for leaks, bulges, or discoloration. Replace any capacitors showing these signs of malfunction.

5.1.2 DEC Type 728 Power Supply

Check the two output voltages from the 728 Power Supply at the logic end. These voltages are not adjustable, so if the output voltage or ripple content is not within the tolerance specified, the supply is considered defective and troubleshooting procedures should be performed.

Check the +10V output between the red (+) and black (-) wires to assure that it is between +9.5 to +11.0V with less than 800 mV rms ripple. Check the -15V output between the blue (-) and black (+) wires to assure that it is between -14.5 and -16.0V with less than 100 mV rms ripple. Note that the black wires are common with the power supply chassis.

5.1.3 Margin Checks

Margin checks are performed to aggravate borderline conditions within the logic circuits, thereby revealing solid observable faults. In this way, marginal conditions can be corrected to forestall equipment downtime. Margin checks can also be used as a troubleshooting aid for locating marginal or intermittent components. Checks may be performed by varying the logic voltages manually at the margin control panel of the central processor while performing the diagnostic procedure.

5.2 CORRECTIVE MAINTENANCE

In this section, corrective maintenance procedures for the DA10 control and data transfer logic are detailed. Corrective maintenance procedures for the central processor are contained in the maintenance manuals for the central processor so they are not repeated here.

The DA10 control and data transfer logic is constructed of highly reliable transistorized modules and standard circuits. Use of these circuits and performance of the preventive maintenance tasks insure minimum equipment downtime due to failure. Should a malfunction occur, the condition should be analyzed and corrected as indicated in the procedures that are described in the following paragraphs. The specific circuit modules are described in the DEC Logic Handbook and Volume III of the PDP-10 Maintenance Manual, the engineering drawings are contained in Volume IV of the

PDP-10 Peripheral Engineering Drawing Set and the location of mechanical and electrical components are described in Chapter 1 of this manual.

Diagnosis and remedial action for a malfunction are performed in the following phases:

a. Preliminary investigation to gather all information and to determine the mechanical and electrical security of the card reader and its control logic.

b. System troubleshooting through the use of the diagnostic program to isolate the malfunction to a module; if the malfunction is not located during the diagnostic program, signal tracing and/or aggravation techniques may be used.

c. Module troubleshooting to locate defective components within a module.

d. Repairs to correct the cause of the malfunction.

e. Validation test to assure that the malfunction has been corrected.

f. Log entry to record pertinent data.

5.2.1 Preliminary Investigation

Before beginning troubleshooting procedures, explore every possible source of information. Evaluate all possible information concerning any unusual function of the system prior to the malfunction and all possible program information, such as the routine in progress, the condition of the indicators, etc. Search the maintenance log to determine whether this type of malfunction has occurred before or if there is any cyclic history of this type of malfunction, and determine how this condition was corrected previously. When the entire DA10 control logic fails, perform a visual inspection to determine the mechanical and electrical integrity of all power sources, cables, connectors, etc. Assure that the power supplies are operational by performing the power supply checks as described under Preventive Maintenance.

5.2.2 System Troubleshooting

Do not attempt to troubleshoot the DA10 logic without first gathering all information possible concerning the malfunction, as outlined under Preliminary Investigation.

Commence troubleshooting by repeating the operation during which the malfunction was initially observed, using the same conditions. Thoroughly check the operating conditions for proper control settings and note the operation of all indicators before and at the time of malfunction. Careful checks should be performed to assure that the system is actually at fault before continuing the corrective maintenance procedures. Loose or faulty cable connections can often give indications very similar to those caused by internal malfunctions. Faulty ground connections between pieces of equipment are a source of trouble. The central processors and the DA10 logic must be properly grounded to prevent high voltage transients.

If the malfunction has been determined to lie within the DA10 logic, but cannot be localized to a specific logic function, perform the DA10 diagnostic program. When the malfunction has been isolated to a specific logic element, continue troubleshooting to locate the defective module or component by means of signal tracing. If the malfunction is intermittent, a form of aggravation test should be employed to locate the malfunction.

5.2.2.1 Diagnostic Program - The most efficient means of troubleshooting the DA10 control and data transfer logic makes use of the diagnostic program described in MAINDEC-10-D8A0-D. This program requires that all processor diagnostic tests and the console teletype test have been run previously and all equipment is in operational condition. The diagnostic program is performed in two parts: Part A, self-test, checks all DA10 control and data transfer logic except the PDP-8 or PDP-9 skip logic under PDP-10 program control (the PDP-8 or PDP-9 is disconnected); Part B uses a program in the PDP-10 and another program in either the PDP-8 or PDP-9 to test all of the control and data transfer logic. Refer to DA10 Interface Test MAINDEC-10-D8A0-D for the diagnostic operating procedure.

Part B of the diagnostic is performed to check system operation and perform margin checks. When it has been determined that the malfunction is within the DA10, Part A of the diagnostic program is performed to locate the malfunction.

Error messages are printed on the console teletype or the line printer. The error printout contains the program counter number, the accumulator register number, the contents of the error word, and the error number. The program counter number is useful in relating the failure to the listing. Upon completion of the printout, the program will enter a routine suitable for scoping.

5.2.2.2 Signal Tracing - When a malfunction is detected and the computer enters into a loop, an oscilloscope may be used to trace signal flow through the suspected logic element. The oscilloscope sweep may be synchronized with DA10 control signals by connecting the trigger input of the oscilloscope to the appropriate module terminal. The signal tracing method can be used to determine with certainty the quality of pulse amplitude, duration, rise time, and the correct timing sequence of the signal. If an intermittent malfunction occurs, signal tracing should be combined with an appropriate form of aggravation test.

5.2.2.3 Intermittent Malfunctions - Intermittent malfunctions caused by poor wiring connections can often be revealed by tapping the modules while running a repetitive routine, such as the diagnostic program. Often, wiping the handle of a screwdriver across the back of a suspect row of modules is a useful technique. By repeatedly starting the program and vibrating fewer and fewer modules, the

malfunction can be localized to within one or two modules. After isolating the malfunction in this manner, check the seating of the modules in the connector, the module connector for wear, misalignment, and malfunction, and then check the module for a poor connection.

5.2.3 Module Troubleshooting

The procedure followed for troubleshooting and correcting the cause of a malfunction within modules and power supplies depends upon the down-time limitations. Where downtime must be kept at a minimum, it is suggested that a replacement parts program be adapted to maintain at least one spare module or power supply which can be inserted into the cabinet when system troubleshooting procedures have traced the fault to a particular component. A list of modules and power supplies can be compiled from the engineering drawings contained in Volume IV of the PDP-10 Peripheral Engineering Drawing Set. A list of recommended spares for the DA10 is contained in Table 5-1.

CAUTION

The primary ac power is present in the DA10 power control even though the logic power is turned off.

5.2.3.1 On-Line Dynamic Tests - Where downtime is not critical, the contents of the spare parts list can be reduced and signal tracing techniques can be utilized to troubleshoot modules. This type of procedure consists of removing the suspected module, inserting the module extender into the module connector, inserting the suspected module into the module extender, and performing the signal tracing procedure with an oscilloscope while the equipment is operated in a routine which exercises the module circuits.

5.3 REPAIR

For minimum system downtime, replace the defective modules and/or system components that have been detected during system troubleshooting procedures. When system downtime is not critical and module troubleshooting procedures are employed, perform the repairs by using good shop practices. Remove defective components by cutting the component leads and removing the leads from the printed board with a solder sucker. When soldering semiconductor devices, use a heat sink and the smallest soldering iron that is adequate for the work. Perform all soldering operations in the shortest possible time to prevent damage to components. Replace defective components with components of equal or greater quality or closer tolerance.

5.3.1 Type R302 Module Replacement

When the R302 Delay module located in card slot A10 is replaced, the trimpots on the new module should be adjusted to the maximum clockwise position (looking at the back of the module). Incorrect trimpot adjustment will not affect data transfer operation, but it may cause the self-test to fail.

5.4 VALIDATION TEST

Following the replacement of any electrical component, a test should be performed to assure the correction of the malfunction and to make necessary adjustments. This test should be taken from the preventive maintenance procedure most applicable to the portion of the system in which the malfunction occurred. Normally, the diagnostic program serves this purpose.

When time permits, it is suggested that the entire preventive maintenance task be performed as a validation test. The reasons for this are other components may be marginal; and while the equipment is down and available, preventive maintenance can be performed and need not be rescheduled for the normal period.

5.5 LOG ENTRY

Corrective maintenance procedures are not completed until they are recorded in the maintenance log. Record all the data that indicate the symptoms given by the malfunction, the method of malfunction location, and any other information which would be helpful in maintaining the equipment in the future.

5.6 SPARE PARTS LIST

Table 5-1 is a list of the spare parts recommended by DEC for the maintenance of the DA10. It is provided to aid the user with maintenance planning and is not intended to limit the stocking of spare parts that the user may feel are needed for effective maintenance.

Table 5-1
Recommended Spare Parts for DA10

MODULES

Type	Quantity	Type	Quantity
B133	1	S107	1
B134	1	S111	1
B152	1	S203	3
B163	2	W005	3
B685	1	W010	1
R001	1	W011	1
R002	1	W012	1
R201	2	W021	1
R302	1	W107	2
R303	1	W640	1
R601	1	W850	1
R602	2	W851	7
R613	1	W990	2

TRANSISTORS

DEC 3639C	7	2N 3605	2
DEC 4258	4	DEC 2844-2B	2
DEC 3009B	1	6534 - D	1

MISCELLANEOUS

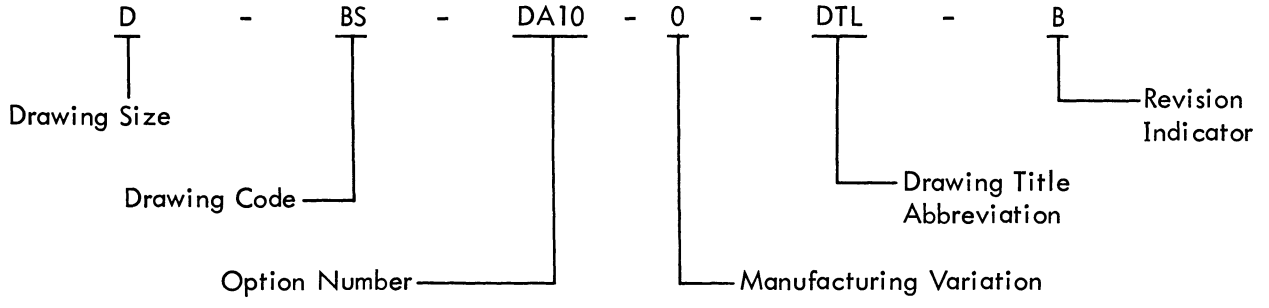
Type	Quantity	Part No.
Diode	10	D662
Diode	10	D664
Indicator Light	10	12-550
Trim Pot	2	A-13-5395

CHAPTER 6
ENGINEERING DRAWINGS

The engineering drawings are contained in Volume IV of the PDP-10 Peripheral Device Engineering Drawing Set and are in addition to a complete set of drawings supplied with each system. Should any discrepancy exist between the drawing in Volume IV and those supplied with the equipment, assume that the latter drawings are correct.

6.1 DRAWING TERMINOLOGY

The engineering drawing numbers for the DA10 contain six fields of information, separated by hyphens. A typical example of a drawing number is shown below.

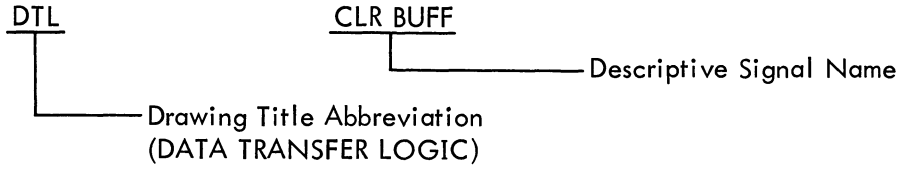


The drawing size, option number, and the drawing title abbreviation are self-explanatory. The manufacturing variation letter identifies the variation that the drawings reflect. For example: 0 reflects drawing applicable to all variations; A reflects the 60 Hertz equipment; etc. The drawing code identifies the type of drawing. A list of the common drawing codes follows.

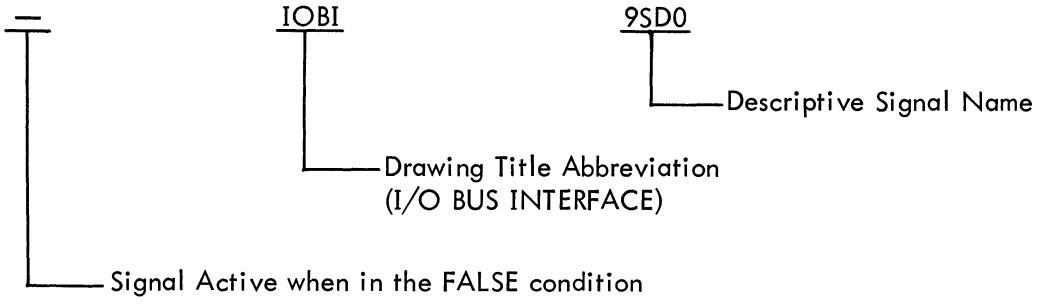
1. BS -- Block Schematic or Logic Diagram
2. CL -- Cable List
3. CS -- Circuit Schematic
4. FD -- Flow Diagram
5. IC -- Interconnection Drawing
6. KS -- Key Sheet
7. MU -- Module Utilization
8. RS -- Replacement Schematic
9. SD -- System Diagram
10. PL -- Parts List

Signal names on the drawings cross reference the signal to the drawing where the signal originates. Two typical examples of signal names are shown below.

Example 1:



Example 2:



6.2 LOGIC SYMBOLS

The DEC standard logic symbols are shown at the input of most circuits to specify the enabling condition required to produce a desired output. These symbols represent either standard DEC logic levels or standard DEC pulses.

Typical engineering symbols are shown in Figure 6-1.

6.3 LOGIC LEVELS

All logic signals are either standard DEC logic levels or standard DEC pulses. A standard DEC logic level is either a ground (0 to -0.5V) or -3V (-2.5 to -4.0V). Logic signals are generally given mnemonic names which indicate the condition represented by assertion of the signal. An open diamond (——◇) indicates that the signal is a level and that ground presents assertion; a solid diamond (——◆) indicates that the signal is a level and that -3V represents assertion.

All logic levels applied to the conditioning-level inputs of capacity-diode gates must be present either 100 or 400 ns (depending on the module used) before an input triggering pulse is applied to the gate.

The standard DEC negative pulse is indicated by a solid triangle (——▶) and goes from ground (0 to -0.5) to -3V (-2.5 to -4.0V). The standard DEC positive pulse, indicated by an open triangle (——▷) goes from -3V to ground. The width of the standard pulses used in this equipment is either 100 or 400 ns, depending on the module and application.

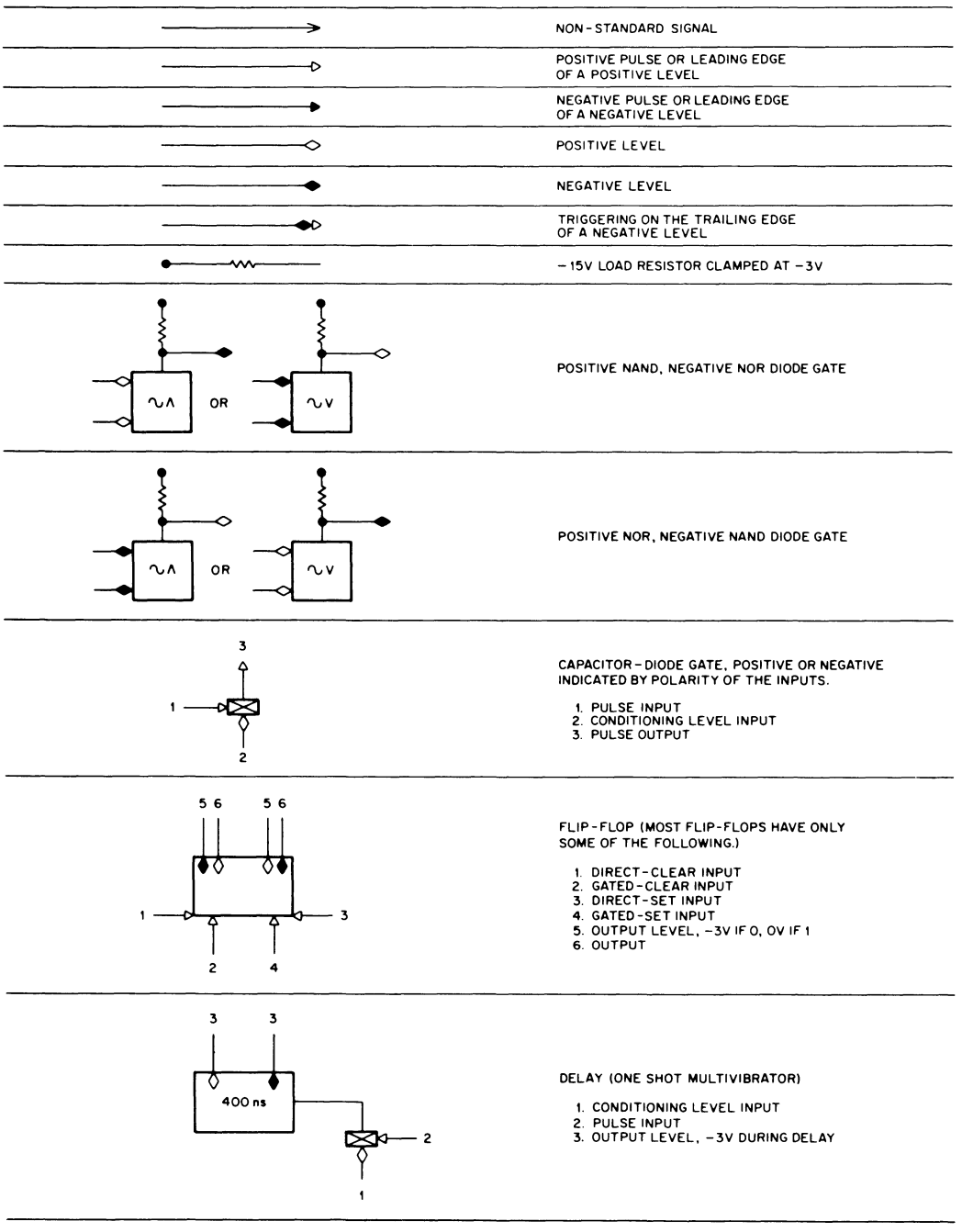


Figure 6-1 DEC Standard Logic Symbols

Occasionally, the trailing edge transition of a level is used at an input where a standard pulse is otherwise expected and a composite symbol (——◆▷) is drawn to indicate this fact. The triangle is drawn solid if the negative (ground to -3V) transition triggers circuit action. The shading of the diamond is opposite that of the triangle to indicate triggering on the trailing edge.

Any other signal is nonstandard and is indicated by an arrowhead (⟶) pointing in the direction of signal flow.

6.4 FLIP CHIP PULSES

FLIP CHIP circuit operation in the DA10 uses the DEC R-, S-, and B-series pulses. The pulse produced by the R-series or S-series modules start at -3V, goes to ground (-0.2V) for 100 or 400 ns, then returns to -3V. The rise time of the loading edge from 10% to 90% should be less than 60 ns. An idealized pulse is shown in Figure 6-2.

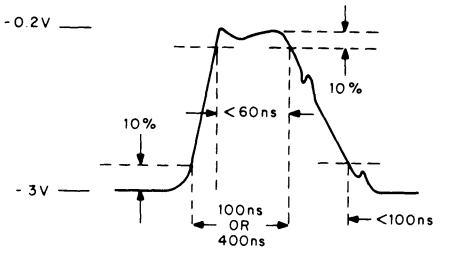


Figure 6-2 R-Series and S-Series Pulses

The B-series pulse starts at 0V, goes to -3V and returns to 0V. The pulse width must be between 30 and 40 ns at the -1V level and greater than 15 ns at the -2V level. Glitches on the bottom of the pulse should not be more positive than -2.5V, overshot should not exceed +4.0V, and no ring should be below -0.5V. The B-series pulse is idealized in Figure 6-3.

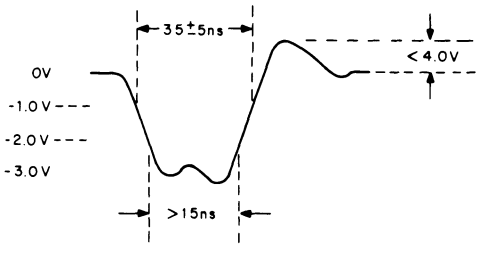


Figure 6-3 B-Series Pulse

6.5 ENGINEERING DRAWING LIST

Table 6-1 lists the engineering drawings that are supplied with the DA10. A copy of each drawing will be found in Volume IV of the PDP-10 Peripheral Engineering Drawing Set.

Table 6-1
DA10 Engineering Drawings

Drawing Number	Title
D-MU-DA10-0-2	Module Utilization List
D-IC-DA10-0-3	50 & 60 Hz AC and DC Power Wiring
D-BS-DA10-0-CS	Control and Selection
D-BS-DA10-0-DTL	Data Transfer Logic
D-BS-DA10-0-DTPM	Data Transfer Pulse Mixer
D-BS-DA10-0-FBOM	From 10 Buffer Output Mixer
D-BS-DA10-0-FTB	From 10 Buffer
D-BS-DA10-0-IND	DA10 Indicators
D-BS-DA10-0-IOBI	I/O Bus Interface
D-BS-DA10-0-SI	Selection and IOPS
D-BS-DA10-0-SISL	SKP and I/O Status Logic
D-BS-DA10-0-TTB	TO10 Buffer
D-BS-DA10-0-TL	Test Logic

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