DL11-W
serial line unit/real-time clock option
operator's manual

digital

EK-DL11W-OP-001

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serial line unit/real-time clock option
operator's manual

digital equipment corporation • maynard, massachusetts

1st Edition, May 1977

Printed in U.S.A.

This document was set on DIGITAL's DECset-8000 computerized typesetting system.

CONTENTS

		Page
CHAPTER 1	**INTRODUCTION**	
1.1	SCOPE	1-1
1.2	ENGINEERING DRAWINGS	1-1
1.3	GENERAL DESCRIPTION	1-2
1.3.1	DL11-W Teletype Control	1-3
1.3.2	DL11-W EIA Terminal Control	1-5
1.3.3	Line Time Clock	1-6
1.4	PHYSICAL DESCRIPTION	1-6
1.5	SPECIFICATIONS	1-7
1.6	CABLES	1-8
CHAPTER 2	**CONFIGURATION, INSTALLATION, AND TESTING**	
2.1	CONFIGURATION	2-1
2.1.1	Baud Rates	2-1
2.1.2	Address and Vector Selection	2-2
2.1.3	Address Selection Modes	2-2
2.1.4	Active and Passive Modes	2-3
2.1.5	Data Format	2-4
2.2	INSTALLATION	2-8
2.2.1	Mounting	2-8
2.2.2	Connections	2-9
2.3	INSTALLATION TESTING	2-12
CHAPTER 3	**PROGRAMMING INFORMATION**	
3.1	SCOPE	3-1
3.2	DEVICE REGISTERS	3-1
3.3	INTERRUPTS	3-5
3.4	TIMING CONSIDERATIONS	3-6
3.4.1	Receiver	3-6
3.4.2	Transmitter	3-6
3.4.3	Break Generation Logic	3-6
3.4.4	Line Clock	3-6
APPENDIX A	**ADDRESS SELECTION**	
APPENDIX B	**VECTOR ADDRESSING**	

FIGURES

Figure No.	Title	Page
1-1	DL11-W (M7856)	1-2
1-2	DL11-W Teletype Control	1-4
1-3	DL11-W Terminal Control	1-5
1-4	Line Clock Block Diagram	1-6
2-1	Address and Vector Selection	2-2
2-2	DL11-W Data Format	2-4
2-3	Typical Switch Settings	2-6
2-4	DD11-C, -P Backplanes	2-8
2-5	DL11-W Cable Connections	2-9
3-1	Receiver Status Register Bit Format	3-2
3-2	Receiver Data Buffer Bit Format	3-3
3-3	Transmitter Status Register Bit Format	3-4
3-4	Transmitter Data Buffer Bit Format	3-4
3-5	Clock Status Register Bit Format	3-5

TABLES

Table No.	Title	Page
1-1	DL11-W Operating Specifications	1-7
2-1	DL11-W Baud Rates	2-1
2-2	Address and Mode Selection	2-3
2-3	Switch Settings	2-3
2-4	Data Format Switches	2-5
2-5	DL11-W Switch Functions	2-6
2-6	Pin Connections	2-10
2-7	Input/Output Signals	2-11
2-8	7008360 Connections	2-11
2-9	7008519 Connections	2-12
2-10	BC05C Connections	2-12
3-1	Standard DL11-W Register Assignments	3-1

PREFACE

This manual describes the DL11-W Serial Line Unit/Real-Time Clock Option (M7856). Complete understanding of its contents requires that the user have a basic understanding of PDP-11 computers. The *PDP-11 Processor Handbook*, the *PDP-11 Peripherals Handbook*, the *PDP-11 Paper Tape Software Handbook*, and the appropriate system user's manual will be valuable as references.

CHAPTER 1
INTRODUCTION

1.1 SCOPE

This manual is divided into three major chapters: Introduction; Configuration, Installation, and Testing; and Programming. Although control signals and data are transferred between the interface and the Unibus and between the interface and the communications device, this manual is limited to coverage of the interface itself.

The purpose of this manual is to present the user with information necessary to understand normal system operation of the DL11-W. This information will be useful when analyzing trouble symptoms and determining corrective action. However, presentation of detailed troubleshooting techniques is beyond the scope of the manual.

1.2 ENGINEERING DRAWINGS

A complete set of engineering and circuit schematics is provided in a companion volume to this manual entitled *DL11-W SLU/RTC Option Engineering Drawings*. The general logic symbols used on these drawings are described in the *DIGITAL Logic Handbook*. Specific symbols and conventions are also included in certain PDP-11 system manuals. The following paragraphs describe the signal nomenclature convention used on the drawing set.

Signal names in the DL11-W print set are given in the following basic form:

SOURCE SIGNAL NAME POLARITY

SOURCE indicates the drawing number of the print set where the signal originates. The drawing number of a print is located in the lower right corner of the print title block (DL-1, DL-2, DL-3, etc.). SIGNAL NAME is the proper name of the signal. The names used on the print set are also used in this manual. POLARITY is either H or L to indicate the voltage level of the signal. H means +3 V; L means ground. As an example, the signal:

DL-1 RCVR DONE H

orignates on sheet 1 of the M7856 module drawing and is read, "When RCVR DONE is true, this signal is at +3 V."

Unibus signal lines do not carry a SOURCE indicator. These signal names represent a bidirectional wire-ORed bus; as a result, multiple sources for a particular bus signal exist. Each Unibus signal name is prefixed with the word BUS.

1.3 GENERAL DESCRIPTION

The DL11-W Serial Line Unit/Real-Time Clock Option provides two distinct functions. First, the DL11-W is a character-buffered communications interface designed to assemble or disassemble the serial information required by a communications device for parallel transfer to or from the PDP-11 Unibus. Second, the DL11-W is a line frequency clock which can provide timed interrupts, allowing a program to measure the passage of time. The DL11-W consists of a single integrated circuit quad board (Figure 1-1) containing two independent communications units (receiver and transmitter) that are capable of simultaneous 2-way communication, and an independent line frequency real-time clock. Note that a quad board has four connectors (groups of fingers).

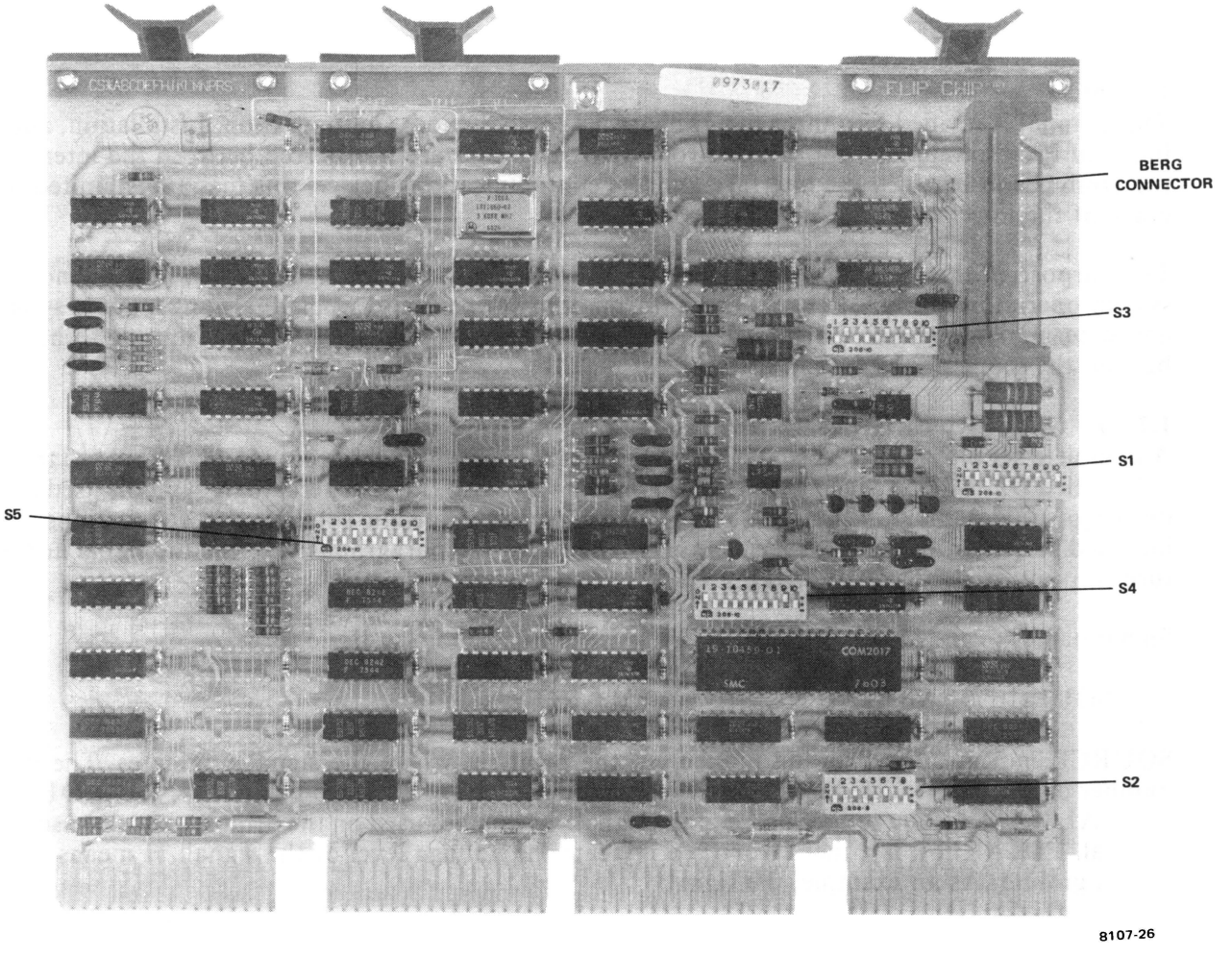

Figure 1-1 DL11-W (M7856)

The DL11-W interface provides the logic and buffer registers necessary for program-controlled transfer of data between a PDP-11 system requiring parallel data and an external device requiring serial data. The interface also includes status and control bits that may be controlled by the program, the interface, or an external device for command, monitoring, and interrupt functions.

The DL11-W interface provides the flexibility needed to handle a variety of terminals. For example, the user can use a DL11-W as a Teletype® control; or, in conjunction with another serial line interface, the DL11-W can be used as a communications link between two processor systems. The DL11-W provides the user with a choice of line speeds (baud rates), character size, stop code length, parity selection, and status indications.

The DL11-W can replace DL11-A, DL11-B, DL11-C, and DL11-D modules in most applications. However, the DL11-E is still required for use with communications data sets such as Bell Model 103 or 202. All of the features of the DL11-A through DL11-D modules are combined on the DL11-W and are switch-selectable to allow for interchangeability.

As a receiver of serial data, the interface converts an asynchronous serial character from an external device into the parallel character required for transfer to the Unibus. This parallel character can then be gated through the bus to memory, a processor register, or some other device. When the DL11-W is used as a transmitter, a parallel character from the bus is converted to a serial character for transmission to an external device. Because the two data transfer units (receiver and transmitter) are independent, they are capable of simultaneous 2-way communication. The receiver and transmitter each operate through two related registers: a control and status register for command and monitoring functions and a data buffer register for storing data prior to transfer to the bus or external device. The line frequency clock uses a signal derived from the ac input voltage by the power supply to generate timed interrupts. The clock portion utilizes a register for command and monitoring functions.

Typically, the DL11-W is operated in one of two functionally different configurations. The DL11-W used as a Teletype control and the DL11-W used with EIA level converters will be discussed individually in the following paragraphs. The real-time clock functions will also be described.

1.3.1 DL11-W Teletype Control

The DL11-W (Figure 1-2) can be used to interface to Model 33, Model 35, and Model 38 Teletypes, and to the LA36.

Serial information read or written by the Teletype unit is assembled or disassembled by the DL11-W interface for parallel transfer to or from the Unibus. When the processor puts an address on the bus, the DL11-W interface decodes the address to determine if the Teletype is the selected external device and, if selected, whether it is to perform an input or output operation.

If, for example, the Teletype has been selected to accept information for printout, parallel data from the Unibus is loaded into the DL11-W transmitter (punch) buffer. At this point, the XMIT RDY flag drops because the transmitter (punch) logic has been activated. (The flag comes back after a fraction of a bit time if the transmitter is not presently active.) The interface generates a START bit, shifts the data from the buffer into the Teletype one bit at a time, resets the XMIT RDY flag (as soon as the holding register of the double-buffer is empty, even though the shift register is active), and then puts out the required number of STOP bits.

®Teletype is a registered trademark of Teletype Corporation.

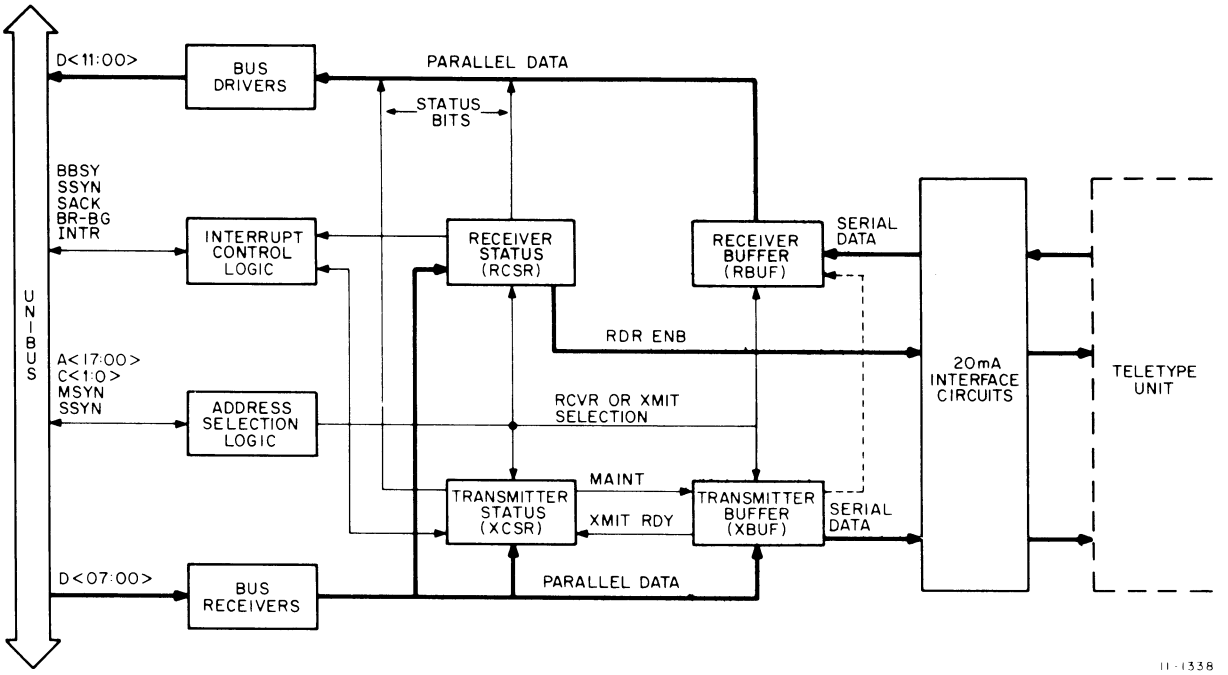

Figure 1-2 DL11-W Teletype Control

Thus, if the DL11-W is interfaced to a Model 33 Teletype, the 8-bit parallel bus data is converted to the 11-bit serial input required by the Teletype. Note that whenever a series of characters is to be output to the Teletype, the XMIT RDY flag is set prior to generation of the STOP bits and the shifting out of the character in the holding register, thus allowing another character to be loaded from the bus as soon as the transmitter holding buffer is empty. The XMIT RDY flag is used with XMIT INT ENB to initiate an interrupt sequence, informing the processor that the interface is ready to accept another character for transfer to the Teletype for printing.

When receiving data from the Teletype unit, the operation is essentially the reverse. The START bit of the Teletype serial data activates the interface receiver logic, and data is loaded one bit at a time into the reader buffer register. When buffer loading is complete, the buffer contents are transferred to the holding register and the interface sets the RCVR DONE flag, indicating to the program that a character has been assembled and is ready for transfer to the bus. If RCVR INT ENB is also set, the RCVR DONE flag initiates an interrupt sequence, thereby causing a vectored interrupt.

The DL11-W has a reader enable (RDR ENB) bit that can be set to advance the paper tape reader in the Teletype. When set, this bit clears the RCVR DONE flag. As soon as the Teletype sends another character, the START bit clears the RDR ENB bit, thus allowing just one character to be read.

The DL11-W also has a receiver active (RCVR ACT) bit, which indicates that the DL11-W interface is receiving data from the Teletype. This bit is set at the center of the START bit, which is the beginning of the input serial data, and is cleared by the leading edge of the RCVR DONE bit. The DL11-W also has a BREAK bit which can be switch-enabled. This bit can be set by the program to transmit a continuous space to the Teletype.

The DL11-W can be operated in a maintenance mode, which is program-selected by setting the MAINT bit in the transmitter status register. When in this mode, special logic is used to perform a closed loop test of interface logic circuits. A character from the bus is loaded into the transmitter (punch) buffer register. The serial output of the register enters the receiver (reader) buffer register, where it is converted back into parallel data and transferred to the bus. In the maintenance mode, the data is not transmitted to the Teletype. If the DL11-W is functioning properly, the character in the reader buffer (RBUF) is identical to the character loaded into the transmitter buffer (XBUF).

1.3.2 DL11-W EIA Terminal Control

The DL11-W also provides the control logic required for interfacing EIA terminals such as the VT06 display or the Model 37 Teletype (Figure 1-3).

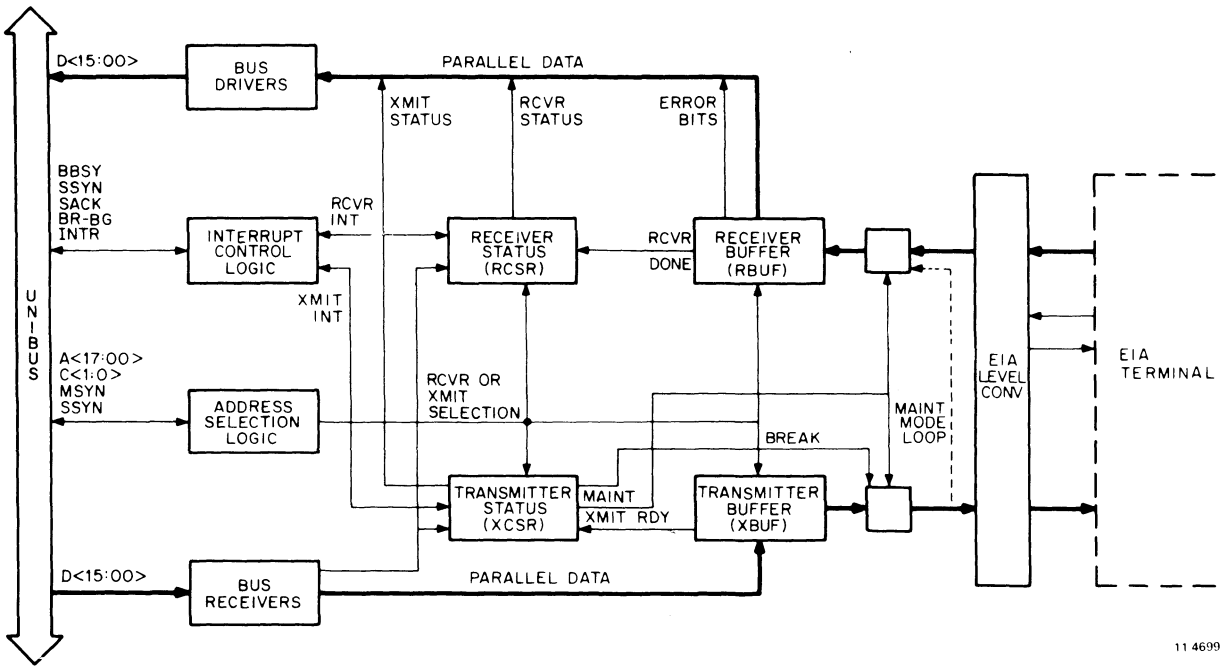

Figure 1-3 DL11-W Terminal Control

Functionally the EIA terminal control configuration is nearly identical to the Teletype control configurations. In the EIA terminal control configuration, EIA level converters on the DL11-W are used to change bipolar serial input data to TTL logic levels and TTL logic level serial output to the bipolar signals required by EIA terminals. EIA level outputs for the signals DATA TERMINAL RDY and REQ TO SEND are permanently strapped on. However, RDR ENB has no EIA level equivalent.

1.3.3 Line Time Clock (Figure 1-4)

A signal generated from the ac input line voltage by the power supply is received by the DL11-W. This signal is a square wave identical in frequency to the ac line voltage. A monitor bit (LTC MONITOR) on the line clock status register (LKS) is set once for each cycle by the hardware but must be cleared by the program. By monitoring this bit, the program can count unit time intervals of 16-2/3 ms (60 Hz) or 20 ms (50 Hz). If the LTC INT ENB bit is set, a vectored interrupt will be generated on each cycle.

The terms real-time clock (RTC) and line clock (LTC) are used interchangeably in other contexts, but line clock will be used generally in this manual for consistency.

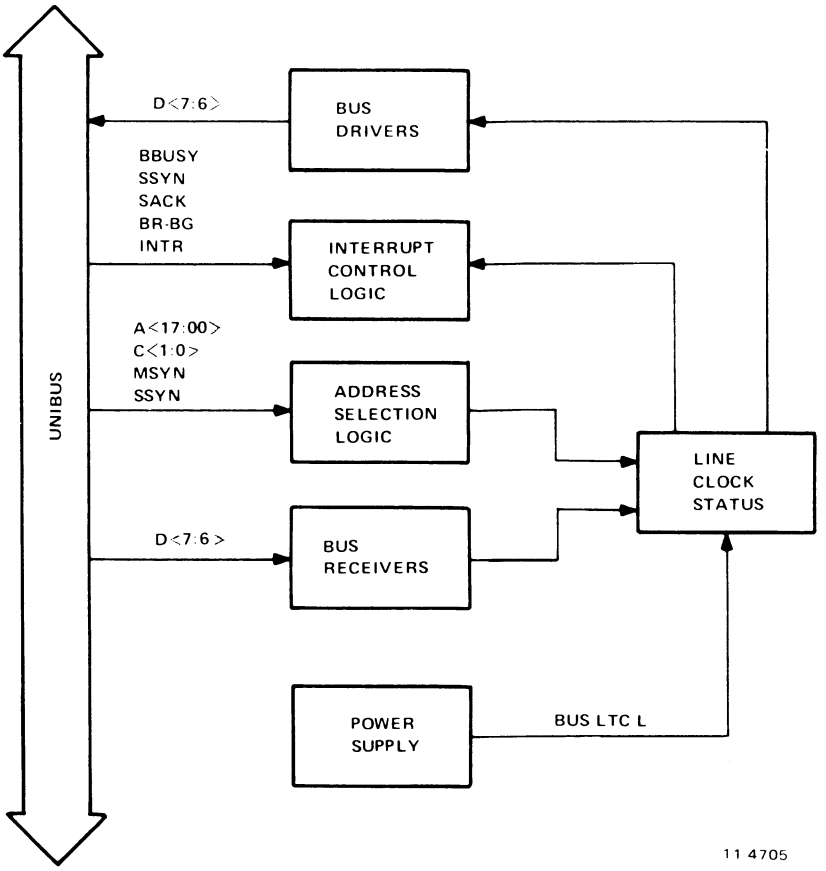

Figure 1-4 Line Clock Block Diagram

1.4 PHYSICAL DESCRIPTION

The DL11-W SLU/RTC option is packaged on a single M7856 quad integrated circuit module that can easily be plugged into a small peripheral controller slot in the processor or one of the slots in a DD11-D peripheral mounting panel.

Power is applied to the logic through the power harness already provided in the BA11 mounting box. The required current is approximately 2.0 A at +5 V and 150 mA at -15 V. If the EIA level outputs are used, then 50 mA of current, at a level between +9 V and +15 V, is also required.

The M7856 module has a Berg connector for all user input/output signals. The specific signals fed to this connector depend on the external device interfaced to, and the specific cable used. Mounting, cabling, and connector information is given in Chapter 2.

Figure 1-1 shows the position of the Berg connector and the five switch packs.

1.5 SPECIFICATIONS

Operating and physical specifications for the DL11-W Serial Line Unit/Real-Time Clock are given in Table 1-1.

Table 1-1 DL11-W Operating Specifications

Specification	Description
Registers	Receiver Status Register (RCSR) Receiver Buffer Register (RBUF) Transmitter Status Register (XCSR) Transmitter Buffer Register (XBUF) Line Clock Status Register (LKS)
Register Addresses	RCSR 777560 RBUF 777562 When used as console device XCSR 777564 XBUF 777566 LKS 777546 Valid when SLU is used as console or DL11-W is used as a line clock only. (See Appendix A for addresses other than console device).
Interrupt Vector Address	060 Receiver when used as console 064 Transmitter 100 Line Clock Floating Vectors (Appendix B)
Priority Level	BR4 SLU BR6 RTC
Interrupt Types	Transmitter Ready (XMIT RDY) Receiver Done (RCVR DONE) Line Clock Monitor

Table 1-1 DL11-W Operating Specifications (Cont)

Specification	Description
Commands	Receiver Interrupt Enable (RCVR INT ENB) Transmitter Interrupt Enable (XMIT INT ENB) Line Clock Interrupt Enable (LKS INT ENB) Reader Enable (RDR ENB) Maintenance Mode (MAINT) Break (BREAK)
Status Indicators	Receiver Active (RCVR ACT) Transmitter Ready (XMIT RDY) Receiver Done (RCVR DONE) Line Clock Monitor Error (ERROR) Overrun (OR ERR) Framing Error (FR ERR) Parity Error (P ERR)
Data Input/Output	Serial data, 20 mA active current loop Serial data, 20 mA passive current loop Serial data, conforms to EIA and CCITT specifications.
Data Format	One START bit; 5-, 6-, 7-, or 8-bit DATA character; PARITY bit (odd, even, or unused); 1 or 2 STOP bits with 6, 7, 8 DATA bits selected; 1 or 1.5 STOP bits with 5 DATA bits selected.
Data Rates	Baud rates may be 110, 150, 300, 600, 1200, 2400, 4800, or 9600. Any split speed combination possible (transmitter and receiver speeds may differ).
Bit Transfer Order	Low-order bit (LSB) first
Parity	Computed on incoming data or inserted on outgoing data, depending on type of parity (odd or even) used. Parity may be odd, even, or unused.
Size	Consists of a single quad module (M7856) that occupies a slot in a DD11-C, DD11-D, or DD11-P backplane.
Power Required	2.0 A at +5 V 150 mA at -15 V 50 mA at level between +9 V and +15 V.
Temperature Range	10° to 50° C.

1.6 CABLES

The DL11-W comes in a package with a 7008360 cable for use when interfacing via a 20 mA currrent loop; this kit is called the DL11-WA. The DL11-W also comes with a BC05C cable for interfacing to EIA level devices; this kit is the DL11-WB. The Berg connector will accept either cable.

CHAPTER 2
CONFIGURATION, INSTALLATION, AND TESTING

2.1 CONFIGURATION

The DL11-W consists of an M7856 quad module with five dip-mounted switch packs. Each pack contains either eight or ten individual slide or toggle switches. The packs are labeled S1 through S5 on the board; each switch on the packs is numbered 1 through 8 or 10. Positions for on and off are clearly indicated on the hardware. "SX-Y" is the convention used in this manual to refer to specific switches where X indicates the switch pack number and Y indicates the particular switch on that switch pack. For example, "S2-9" refers to switch number 9 on switch pack 2.

Switch selections on the DL11-W interface provide the flexibility needed to handle a variety of functions. For example, the user can set up switches so that the DL11-W can interface to a Teletype or to a high-speed CRT terminal. The user has a choice of speeds, character size, stop code length, parity, error detection, 20 mA current loop or EIA, addresses and vectors, active or passive modes, and the specific type of interface which the DL11-W is to replace.

2.1.1 Baud Rates

Table 2-1 lists the eight different baud rates available on the DL11-W. Completely independent split speed operation is provided so that the receiver and transmitter may operate at different rates. The user should be careful to set the correct speeds when replacing other interface modules (DL11-A, DL11-B, etc.).

Table 2-1 DL11-W Baud Rates

Baud Rate	Transmit			Receive		
	S4-10	S3-1	S3-4	S3-2	S3-3	S3-5
110	ON	ON	ON	OFF	OFF	OFF
150	OFF	ON	ON	ON	OFF	OFF
300	ON	OFF	OFF	OFF	ON	ON
600	ON	OFF	ON	OFF	ON	OFF
1200	ON	ON	OFF	OFF	OFF	ON
2400	OFF	OFF	OFF	ON	ON	ON
4800	OFF	OFF	ON	ON	ON	OFF
9600	OFF	ON	OFF	ON	OFF	ON

2.1.2 Address and Vector Selection

The DL11-W interface is addressed through the address selection logic, and its interrupt vector is determined by the interrupt control logic. Each DL11-W interface within a system has a unique address and a unique vector. These are determined by the switches on the module. However, the line clock address and vector are fixed at 777546 and 100, respectively. Figure 2-1 shows the relation of specific switches to the address and vector of the device used (Teletype, etc.).

Thus, for address selection, switch S5-3 corresponds to address bit 10, and it indicates a logical 1 when turned off. For vector selection, on the other hand, switch S2-3 corresponds to vector bit 5, and it indicates a logical 1 when it is on.

All PDP-11 systems have enough I/O addresses reserved to handle up to 47 devices. Each one of these devices could be a DL11-W. However, only one DL11-W per system is allowed to have the LTC enabled. The LTC sections of other DL11-Ws can be disabled by turning switches S5-9 on S5-10 off. See Appendix A for more specific address configuration information.

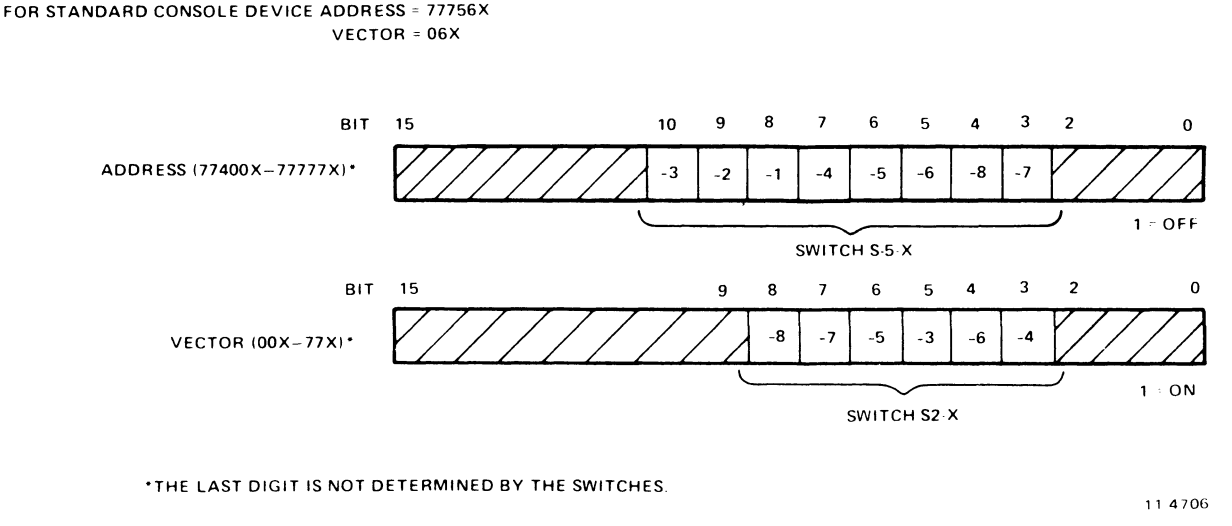

Figure 2-1 Address and Vector Selection

2.1.3 Address Selection Modes

The DL11-W can be operated in any of three different address selection modes. Normally, a DL11-W used as console terminal control would operate in the first mode, whereas additional DL11s would be operated in the second mode. The third mode is not normally used, but is discussed here for completeness.

Mode 1: Both the serial line unit and the line clock sections can be addressed. Due to common address selection logic, operation in this mode requires that the serial line unit addresses be restricted to 77756X. The line clock address is 777546.

Mode 2: Only the serial line unit section can be addressed. Address selection ranges from 774000 to 777776. The line clock is disabled and does not respond to address 777546.

Mode 3: Only the line clock section can be addressed at 777546. The serial line unit section does not respond to any address.

Table 2-2 indicates the correct switch setting for selection of the desired address and address mode.

Table 2-2 Address and Mode Selection

Address Bit	A10	A09	A08	A07	A06	A05	A04	A03	LTC	LTC
Switch	S5-3	S5-2	S5-1	S5-4	S5-5	S5-6	S5-8	S5-7	S5-9	S5-10
Mode 1	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	ON
Mode 2*	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	OFF
Mode 3	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	ON	ON

*Address 77756X is selected for the serial line interface. Other addresses may be selected using switches shown in Figure 2-1, where OFF = 1 and ON = 0.

2.1.4 Active and Passive Modes

Two switch-selectable modes of operation are available for the 20 mA current loop. In the active mode, the DL11-W is the source for the 20 mA of current; in the passive mode, the external device must provide the current. As an example, two processing systems could be connected using two DL11-Ws via the 20 mA current loop. One DL11-W would be the active device. The other DL11-W would be passive. Table 2-3 shows appropriate switch settings. Normal configuration is in the active mode.

Table 2-3 Switch Settings

	Transmitter				
	S1-1	S1-2	S1-3	S1-6	S1-7
Active	ON	ON	OFF	OFF	ON
Passive	OFF	OFF	ON	ON	OFF
	Receiver				
	S3-6	S3-7	S3-8	S3-9	S3-10
Active	ON	OFF	ON	OFF	ON
Passive	OFF	ON	OFF	ON	OFF
	Paper Tape Reader Enable				
	S1-4	S1-5	S1-8	S1-9	S1-10
Active	ON	OFF	ON	OFF	ON
Passive	OFF	ON	OFF	ON	OFF

2.1.5 Data Format

The data format (Figure 2-2) consists of a START bit, five to eight DATA bits, a PARITY bit or no PARITY bit, and one, one and one-half, or two STOP bits.

When less than eight DATA bits are selected, the hardware justifies the bits into the least significant bit positions for characters received by the interface. When transmitting characters, the program provides the justification into the least significant bits. The PARITY bit may be either on or off; when on, it can be selected for checking either odd or even parity when receiving and for providing an extra PARITY bit during transmission.

All variable items within any data format are selected by switches on the DL11-W module. None of the variables can be controlled by the program. These switches are listed in Table 2-4.

Figure 2-3 shows typical switch settings for a DL11-W when interfacing with a standard DIGITAL terminal (console device only).

Table 2-5 gives a complete listing of the switches and their functions.

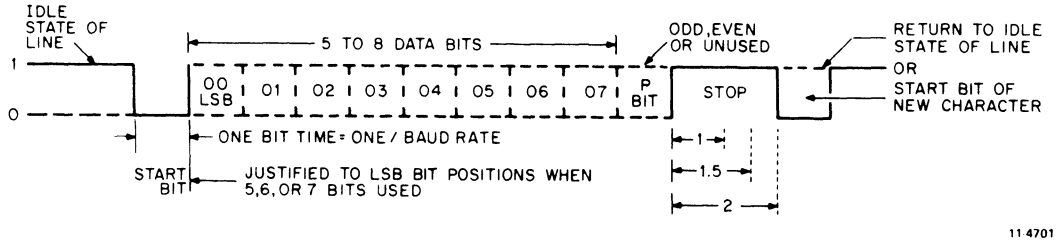

Figure 2-2 DL11-W Data Format

Table 2-4 Data Format Switches

Name	Switch	UART Pin No.	Function
No Parity	S4-6	35	Enables or disables the parity bit in the data character. When enabled, the value of the parity bit is dependent on the type of parity (odd or even) selected by the even parity select (S4-2) switch. When disabled, the STOP bits immediately follow the last DATA bit during transmission. During reception, the receiver does not check for parity. Switch ON - parity enabled Switch OFF - parity disabled
Even Parity	S4-2	39	Determines whether odd or even parity is to be used. The receiver checks the incoming character for appropriate parity; the transmitter inserts the appropriate parity value. Switch ON - odd parity Switch OFF - even parity
STOP Bit	S4-5	36	Selects the desired number of stop bits. Switch ON - One STOP bit. Switch OFF - Two STOP bits, but if five DATA bits are selected, one and one-half STOP bits will be selected.
Number of DATA bits	S4-3 S4-4	38 37	These two switches are used together to provide a code that selects the desired number of DATA bits in the character.

S4-4	S4-3	No. of DATA Bits
ON	ON	5
ON	OFF	6
OFF	ON	7
OFF	OFF	8

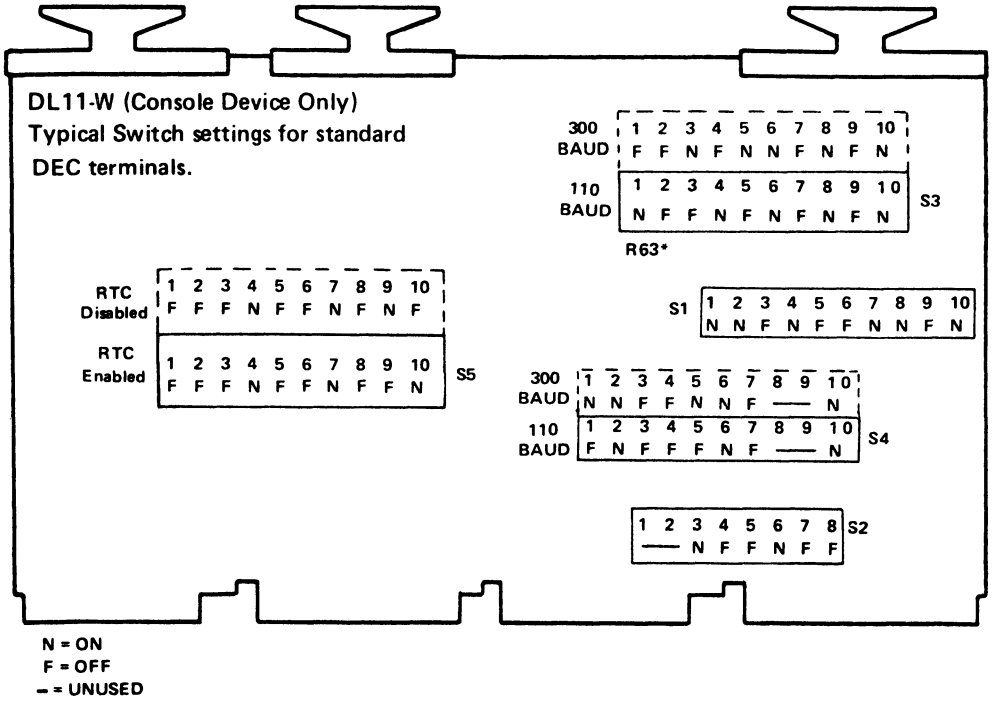

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Figure 2-3 Typical Switch Settings

Table 2-5 DL11-W Switch Functions

Switch Pack	Switch No.	Function
1	1, 2, 3	Transmitter (active/passive mode of 20 mA loop)
	4, 5	Reader enable (active/passive mode of 20 mA loop)
	6, 7	Transmitter (active/passive mode of 20 mA loop)
	8, 9, 10	Reader enable (active/passive mode of 20 mA loop)
2	1, 2	Not functional
	3, 4, 5, 6, 7, 8	Vector address

Table 2-5 DL11-W Switch Functions (Cont)

Switch Pack	Switch No.	Function
3	1	Transmitter baud rate
	2, 3	Receiver baud rate
	4	Transmitter baud rate
	5	Receiver baud rate
	6, 7, 8, 9, 10	Receiver (active/passive mode of 20 mA loop)
4	1	Break enable
	2	Parity select (odd or even)
	3, 4	Number of DATA bits
	5	Number of STOP bits
	6	Parity enable
	7	Error bit enable
	8, 9	Not functional
	10	Transmitter baud select
5	1, 2, 3, 4, 5, 6, 7, 8	Device address
	9, 10	Line clock enable

2.2 INSTALLATION

2.2.1 Mounting

The DL11-W interface can be mounted in either a small peripheral controller slot in the PDP-11 processor (DD11-C) or an SPC slot in a DD11-D or a DD11-P. Figure 2-4 shows the configuration of the DD11-C and DD11-P backplanes.

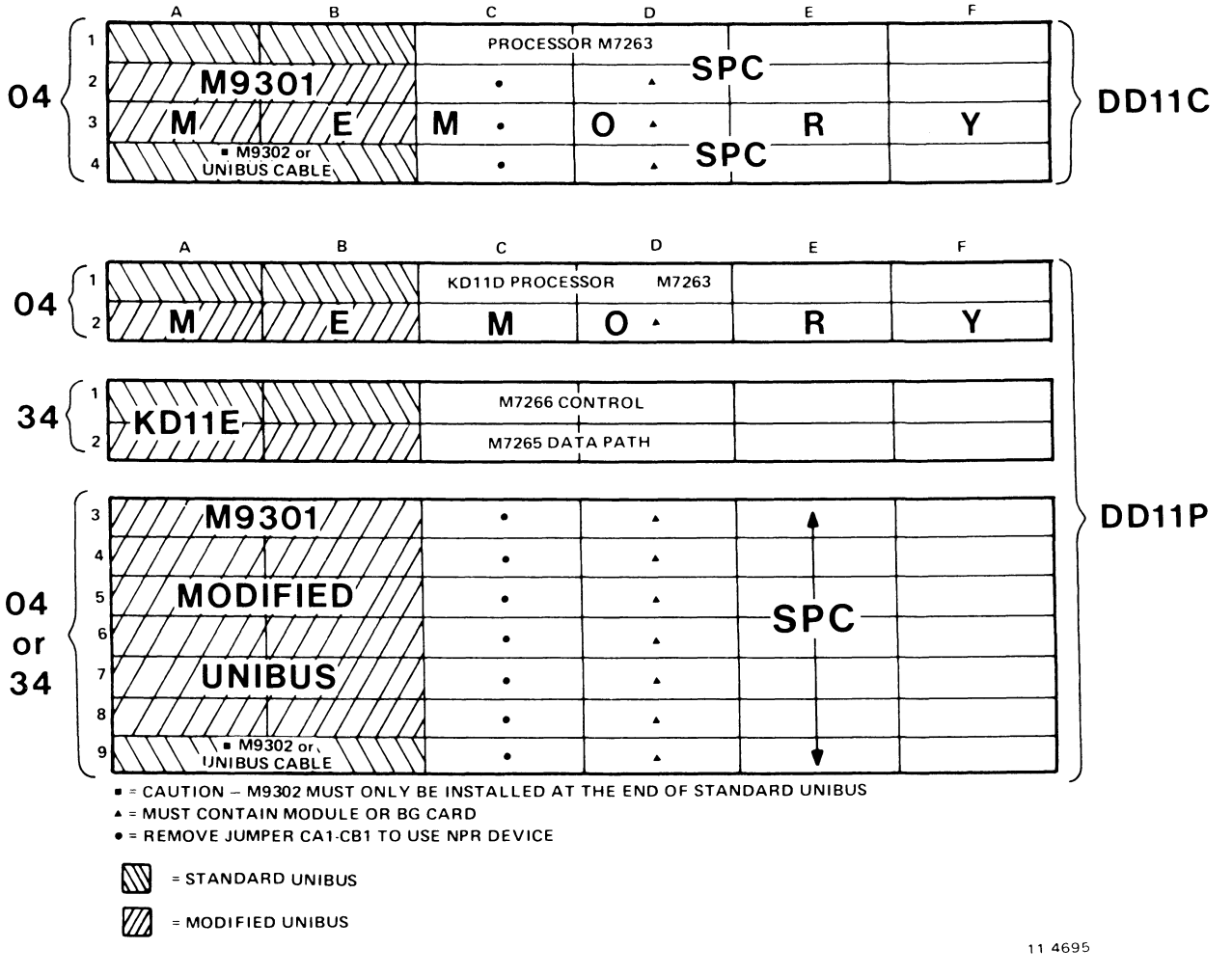


Figure 2-4 DD11-C, -P Backplanes

2.2.2 Connections

Once the M7856 module has been installed, an appropriate cable must be connected. Figure 2-5 shows the method of connecting cables between the DL11-W and various external devices.

Table 2-6 lists the signal names and associated pins on the Berg connector mounted on the M7856 module. This table also lists the signals supplied on the 7008360 and BC05C cables.

Table 2-7 provides a quick reference of M7856 input/output signals for TTL, EIA, and 20 mA current loop devices.

Table 2-8 lists connector pin numbers and signals for the 7008360 cable.

Table 2-9 lists connector pin numbers and signals for the 7008519 cable which is used in conjunction with the 7008360 cable.

Table 2-10 lists connector pin numbers for the BC05C cable connectors.

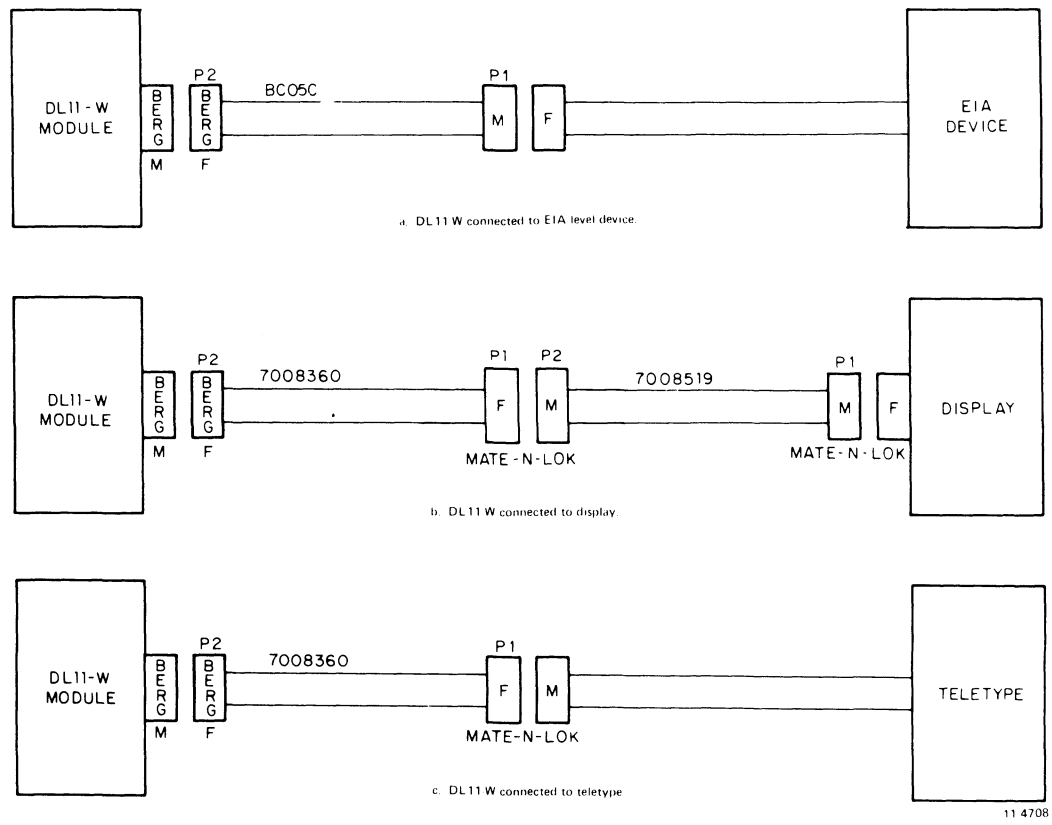


Figure 2-5 DL11-W Cable Connections

Table 2-6 Pin Connections

Berg Pin	M7856 Module	BC05C Modem Cable	7008360 Cable
A	Ground	Ground	Ground
B	Ground	Ground	
C		Force Busy	
D		Secondary Clear to Send	
E	Serial Input (TTL)	Interlock In	Interlock In
F	Serial Output (EIA)	Transmitted Data	
H	20 mA Interlock		Interlock Out
J	Serial Input (EIA)	Received Data	
K	+Serial Input (20 mA)		+Received Data
L		External Clock	
M	EIA Interlock	Interlock Out	
N		Serial Clock Xmit	
P		Secondary Request to Send	
R		Serial Clock Receiver	
S	-Serial Input (20 mA)		-Received Data
T		Clear to Send	
U			
V	Request to Send (EIA)	Request to Send	
W		-Power	
X		Ring	
Y		+ Power	
Z		Data Set Ready	
AA	+Serial Output (20 mA)		+Transmitted Data
BB		Carrier	
CC			
DD	Data Terminal Ready (EIA)	Data Terminal Ready	
EE	-Reader Run (20 mA)		-Reader Run
FF		202 Secondary Transmit	
HH			
JJ		202 Secondary Receive	
KK	-Serial Output (20 mA)		-Transmitted Data
LL		EIA Secondary Transmit	
MM		Signal Quality	
NN		EIA Secondary Receive	
PP	+Reader Run (20 mA)		+Reader Run
RR		Signal Rate	
SS			
TT	+5 V		
UU	Ground	Ground	Ground
VV	Ground	Ground	Ground

Table 2-7 Input/Output Signals

Type	Signals		Pin No.
TTL Signals	INPUT	Serial Data	E
20 mA Current Loop Signals	INPUT	+Serial Data	K
		−Serial Data	S
	OUTPUT	+Serial Data	AA
		−Serial Data	KK
		+Reader Run	PP
		−Reader Run	EE
EIA Signals	INPUT	Serial Data	J
	OUTPUT	Serial Data	F
		Request to Send	V
		Data Terminal Ready	DD

Table 2-8 7008360 Connections

Twisted Pair	Color	Mate-N-Lok Connector P1 (To Device)	Berg Connector P2 (To DL11)	Signal
Black/Red	Black	2	KK	−Transmitted Data
	Red	3	S	−Received Data
Black/White	Black	3	EE	−Reader Run
	White	5	AA	+Transmitted Data
Black/Green	Black	6	PP	+Reader Run
	Green	7	K	+Received Data
			E	Interlock In
			H	Interlock Out

NOTES:

1. Connector on ASR Teletype uses all pins (2–7).
2. Connector on KSR Teletype does not use pins 4 or 6 (Reader Run, - and +).

Table 2-9 7008519 Connections

7008360 Mate-N-Lok Connector P1	Mate-N-Lok Connector P2 (To 7008360)	Color	Mate-N-Lok Connector P1 (To Device)	Signal
2	2	Black	2	−Transmitted Data
3	3	Red	3	−Received Data
5	5	White	5	+Transmitted Data
7	7	Green	7	+Received Data

Table 2-10 BC05C Connections

Color	Cinch Connector P1 (To Device)	Berg Connector P2 (To DL11)	Signal
Blue/White	1	A	Ground
		VV	Ground
White/Blue	2	F	Transmitted Data
Orange/White	3	J	Received Data
White/Orange	4	V	Request to Send
Green/White	5	T	Clear to Send
White/Green	6	Z	Data Set Ready
Brown/White	7	B	Ground
		UU	Ground
White/Brown	8	BB	Carrier
Slate/White	9	Y	+Power
White/Slate	10	W	−Power
Blue/Red	11	FF	202 Secondary Transmit
Red/Blue	12	JJ	202 Secondary Receive
Orange/Red	13	D	Secondary Clear to Send
Slate/Red	14	LL	EIA Secondary Transmit
Slate/Green	15	N	Serial Clock Transmit
Red/Brown	16	NN	EIA Secondary Receive
Slate	17	R	Serial Clock Receive
Red/Slate	18	O	Unassigned
Blue/Black	19	P	Secondary Request to Send
Black/Blue	20	DD	Data Terminal Ready
Orange/Black	21	MM	Signal Quality
Black/Orange	22	X	Ring
Green/Black	23	RR	Signal Rate
Brown/Red	24	L	External Clock
Red/Orange	25	C	Force Busy
		E	Interlock In
		M	Interlock Out

2.3 INSTALLATION TESTING

Installation testing should be performed by running diagnostic test DZDLD-A to check out both the serial line unit and the real-time clock.

CHAPTER 3
PROGRAMMING INFORMATION

3.1 SCOPE

This chapter presents general programming information for software control of the DL11-W Serial Line Unit/Real-Time Clock Option. For more detailed information on programming in general, refer to the *Paper-Tape Software Programming Handbook* (DEC-11-GGPB-D).

This chapter is divided into three major portions: device registers, interrupts, and timing considerations.

3.2 DEVICE REGISTERS

All software control of the DL11-W SLU/RTC Option is performed by means of five device registers. These registers have been assigned bus addresses and can be read or loaded (with the exceptions noted) using any PDP-11 instruction which refers to their addresses. Address assignments can be changed by altering the setting of switches on the address selection logic to correspond to any address within the range of 774000 to 777777. However, register addresses for the DL11-W normally fall within the range of 775610 to 776176 or 776500 to 776670. An explanation of the addressing scheme is offered in Appendix A of this manual. For the remainder of this discussion, it is assumed that the DL11-W is being used as a console terminal control.

The five device registers and associated bus addresses are listed in Table 3-1.

Table 3-1 Standard DL11-W Register Assignments

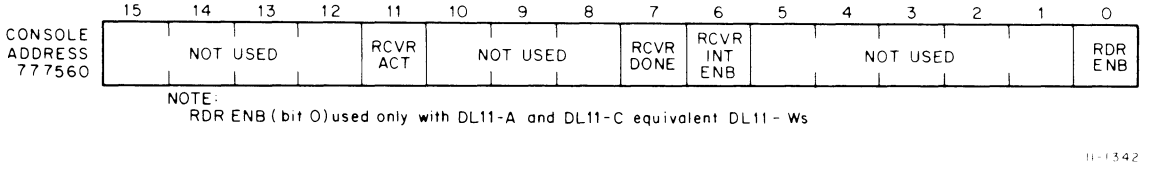
Register	Mnemonic	Address*
Receiver Status	RCSR	777560
Receiver Buffer	RBUF	777562
Transmitter Status	XCSR	777564
Transmitter Buffer	XBUF	777566
Line Clock Status	LKS	777546†

*These addresses are only for a DL11-W used as console terminal control. For other address assignments for these registers, refer to Appendix A.

†This address is valid only on a DL11-W used as a console terminal. On any other DL11-Ws used in a system, this register should be disabled.

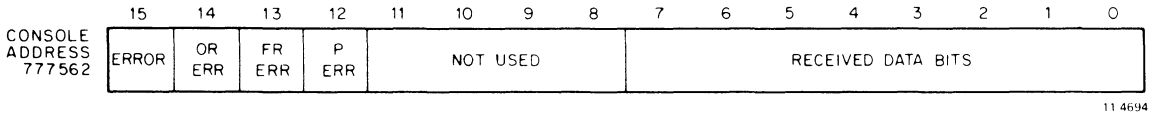
Figures 3-1 through 3-5 show the bit assignments for the device registers. The unused and write-only bits are always read as 0s. Writing unused or read-only bits has no effect on the bit position but is not considered good programming practice. The mnemonic INIT refers to the initialization signal issued by the processor. Initialization is caused by one of the following: issuing a programmed RESET instruction, pressing the START switch on the processor console, or the occurrence of a power-up or power-down condition on the processor power supply.

In the descriptions accompanying the figures, "transmitter" refers to those registers and bits involved in accepting a parallel character from the Unibus for serial transmission to the external device. "Receiver" refers to those registers and bits involved with receiving serial information from the external device for parallel transfer to the Unibus.



Bit	Meaning and Operation
15–12	Unused
11	Receiver Active – Read-only. When set, this bit indicates that the receiver interface is active. This bit is set at the center of the start bit, which is the beginning of the input serial data from the device, and cleared by the leading edge of Receiver Done. Also may be cleared by INIT.
10–8	Unused
7	Receiver Done – Read-only. Set when an entire character has been received and is ready for transfer to the Unibus. Cleared by setting Reader Enable, addressing (read or write) RBUF, or INIT. Starts an interrupt sequence when receiver interrupt enable (bit 6) is also set.
6	Receiver Interrupt Enable – Read/write. Cleared by INIT. Starts an interrupt sequence when Receiver Done is set.
5–1	Unused
0	Reader Enable – Write-only. Cleared by INIT or at the middle of a START bit. Advances paper tape reader of ASR Teletypes. Clears Receiver Done. The 20 mA current loop circuit output is associated with this bit.

Figure 3-1 Receiver Status Register Bit Format



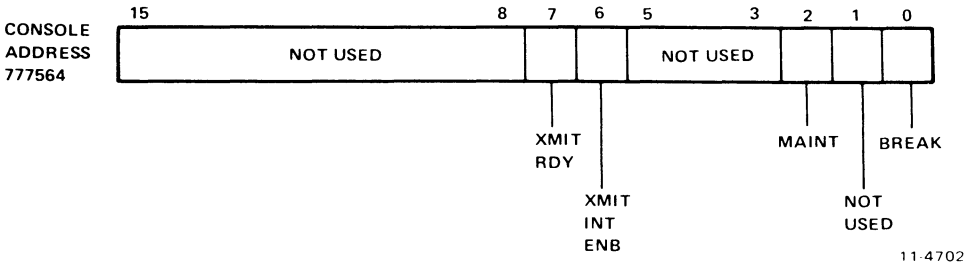
Bit	Meaning and Operation
15	Error – Read-only. Logical OR of Overrun, Framing Error, and Parity Error. Cleared by removing the error conditions. Error is not tied to the interrupt logic.
14	Overrun – Read-only. Set if previously received character is not read (Receiver Done not reset) before the present character is received.
13	Framing Error – Read-only. Set if the character read has no valid STOP bit. Also used to detect Break.
12	Receive Parity Error – Read-only. Set if received parity does not agree with the expected parity. Always 0 if no parity is selected.

NOTE

Error conditions remain until the next character is received, at which time the error bits are updated. INIT does not necessarily clear the error bits. Error bits may be disabled altogether via a switch, but not individually.

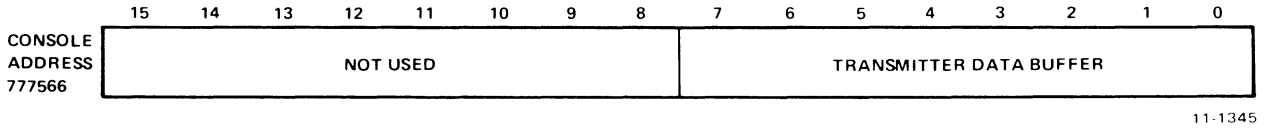
11–8	Unused
7–0	Received Data Bits – Read-only. These bits contain the character just read. If less than 8 bits are selected, the data will be right-justified into the least significant bits, and the higher unused bit or bits will be read as 0s. Not cleared by INIT.

Figure 3-2 Receiver Data Buffer Bit Format



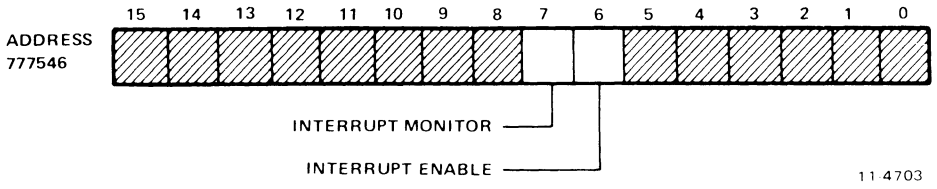
Bit	Meaning and Operation
15–8	Unused
7	Transmitter Ready – Read-only. Set by INIT. Cleared when XBUF is loaded; set when XBUF can accept another character. When set it will start an interrupt sequence if Transmitter Interrupt Enable is also set.
6	Transmitter Interrupt Enable – Read/write. Cleared by INIT. When set it will start an interrupt sequence if Transmitter Ready is also set.
5–3	Unused
2	Maintenance – Read/write. Cleared by INIT. When set, it disables the serial line input to the receiver and sends the serial output of the transmitter into the serial input of the receiver. Forces receiver to run at transmitter speed.
1	Unused
0	Break – Read/Write. Cleared by INIT. When set, it transmits a continuous space. May be disabled via a switch.

Figure 3-3 Transmitter Status Register Bit Format



Bit	Meaning and Operation
15–8	Unused
7–0	Transmitted Data Buffer – Write-only. If less than eight bits are selected, the character must be right-justified into the least significant bits.

Figure 3-4 Transmitter Data Buffer Bit Format



Bit	Meaning and Operation
15–8	Unused
7	Line Clock Monitor – Read/clear. Set by the line frequency clock signal and cleared only by the program. Set by INIT.
6	Line Clock Interrupt Enable – Read/write. Cleared by INIT. When set, starts an interrupt sequence if Line Clock Monitor is also set. An interrupt sequence will also be initiated upon the reception of the line frequency clock signal if the Line Clock Monitor bit is set from a previous clock signal.
5–0	Unused

Figure 3-5 Clock Status Register Bit Format

3.3 INTERRUPTS

The DL11-W interface uses BR interrupts to gain control of the bus to perform a vectored interrupt, thereby causing transfer of control to a handling routine. The DL11-W has three interrupt channels: one for the receiver section, one for the transmitter section, and one for the line clock section. These three channels operate independently. However, if simultaneous interrupt requests occur, the line clock has highest priority, followed by the receiver. The transmitter is last.

A line clock interrupt can occur only if the LKS interrupt enable bit (bit 6) in the line clock status register is set. With LKS interrupt enable set, falling edges of the signal LTC IN L will generate interrupt requests. The signal LTC IN L is derived from the ac power input by the power supply and is a square wave of the same frequency as the ac input voltage.

A transmitter interrupt can occur only if the interrupt enable (XMIT INT ENAB) bit in the transmitter status register is set. With XMIT INT ENAB set, setting the transmitter ready (XMIT RDY) bit initiates an interrupt request. When XMIT RDY is set, it indicates that the transmitter buffer is empty and ready to accept another character from the bus for transfer to the external device.

A receiver interrupt can occur only if the interrupt enable (RCVR INT ENB) bit in the receiver status register is set. Setting the receiver done (RCVR DONE) bit initiates an interrupt request. When RCVR DONE is set, it indicates that an entire character has been received and is ready for transfer to the bus.

The interrupt priority level is 6 for the line clock and 4 for the receiver and transmitter.

The vector address for the line clock is fixed at 100, whereas floating vector addresses are used for the receiver and transmitter of nonconsole DL11-Ws. The receiver vector is XX0 and the transmitter vector is XX4, where XX is assigned according to Appendix A. If the DL11-W is used as console terminal interface, then the receiver and transmitter vector addresses will be 60 and 64, respectively. The vector address can be changed by resetting switches in the interrupt control logic.

All DIGITAL programs and other software which refer to the standard vector addresses must also be changed if the vector addresses are changed.

3.4 TIMING CONSIDERATIONS

When programming the DL11-W SLU/RTC option, it is important to consider the timing of certain functions in order to use the system in the most efficient manner. Timing considerations for the receiver, transmitter, break generation logic, and line clock are discussed in the following paragraphs.

3.4.1 Receiver

The RCVR DONE flag (bit 7 in the RCSR) sets when the universal asynchronous receiver/transmitter (UART) has assembled a full character. This occurs at the middle of the first STOP bit. Because the UART is double-buffered, data remains valid until the next character is received and assembled. This permits one full character time for servicing the RCVR DONE flag.

3.4.2 Transmitter

The transmitter section of the UART is also double-buffered. The XMIT RDY flag (bit 7 in the XCSR) is set after initialization. When the buffer (XBUF) is loaded with the first character from the bus, the flag clears but then sets again within a fraction of a bit time. A second character can then be loaded which clears the flag again. The flag then remains cleared for nearly one full character time.

3.4.3 Break Generation Logic

When the BREAK bit (bit 0 in the XCSR) is set, it causes transmission of a continuous space. Because the XMIT RDY flag continues to function normally, the duration of a break can be timed by the pseudo-transmission of a number of characters. However, because the transmitter section of the UART is double-buffered, a null character (all 0s) should precede transmission of the break to ensure that the previous character clears the line. In a similar manner, the final pseudo-transmitted character in the break should be null.

3.4.4 Line Clock

An initial synchronization period will be required when the LKS interrupt is initially turned on. In other words, the interval from setting LKS interrupt enable to the first interrupt will be some fraction of an ac power cycle period. All subsequent interrupts will occur at the proper intervals, depending on the ac power frequency.

APPENDIX A
ADDRESS SELECTION

The address selection logic decodes the incoming address information from the bus to determine if the DL11-W has been selected for use, and provides the signals that determine which register has been selected and whether it is to perform an input or output function. Switches on the logic can be altered so that the module responds to any address within the range of 774000 to 777777. However, standard address assignments for the DL11-W normally fall within the ranges of 775610 to 776177 or 776500 to 776677.

The standard address assignments for DL11-W module are listed in Table A-1.

When the DL11-W is to be used as a console terminal control, switches are arranged so that the serial line section responds only to the standard device register addresses 777560, 777562, 777564, 777566, and, if the LTC is enabled, 777540. Although these addresses have been selected by DIGITAL as the standard assignments for the DL11-W when used as a console terminal control, the user may change the switches to assign any address desired, within the range of the address switches. However, the serial line address must be 77756X in order for the LTC and the SLU to both be used on the same DL11-W. Any MAINDEC program or other software that references the DL11-W standard assignments must be modified accordingly if other than the standard assignments are used.

Table A-1 DL11-W Standard Address Assignments

Unit	Address	Remarks
Console	777560	Receiver Status Register (RCSR)
	777562	Receiver Data Buffer (RBUF)
	777564	Transmitter Status Register (XCSR)
	777566	Transmitter Data Buffer (XBUF)
1	776500	RCSR unit 1
	776502	RSUF unit 1
	776504	XCSR unit 1
	776506	XBUF unit 1
2	776510	RCSR unit 2
	776512	RBUF unit 2
	776514	XCSR unit 2
	776516	XBUF unit 2
		NOTE **Address space in the range 776500–776676 is reserved for DL11-A and -B equivalent devices.**
16	777670	RCSR unit 16
	777672	RBUF unit 16
	777674	XCSR unit 16
	777676	XBUF unit 16
		NOTE **For DL11-C and -D equivalent devices, address as follows.**
1	775610	RCSR
	775612	RBUF
	775614	XCSR
	775616	XBUF
		NOTE **Unit numbers in the first column are only for showing address sequencing. DL11-A, -B, -C, and -D equivalent DL11-Ws may be mixed in any manner as long as they remain in their respective address space.**
31	776170	RCSR
	776172	RBUF
	776174	XCSR
	776176	XBUF

APPENDIX B
VECTOR ADDRESSING

Because the DL11-W SLU/RTC option is basically a communications device, interrupt vectors must be assigned according to the floating vector convention used for all communications devices. These vector addresses are assigned in order from 300 to 777, according to a specific method that ranks the types of devices in a particular PDP-11 system.

The first vector address (300) is assigned to the first DC11 Serial Asynchronous Line Interface in the system. The next DC11 (if used) is then assigned vector address 310, etc. The vector addresses are assigned consecutively to each unit of the second-ranked device type (KL11, DL11-A, DL11-R, or DL11-W), then to the third-ranked device (DB11), and so on in accordance with the following list:

1. DC11 Asynchronous Line Interface
2. KL11 Teletype Control (or DL11-A, DL11-B, or DL11-W)
3. DP11 Synchronous Serial Modem Interface
4. DM11 Asynchronous Serial Line Multiplexer
5. DN11 Automatic Calling Unit
6. DM11-BB Modem Control
7. DR11-A Device Registers
8. DR11-C General Device Interface
9. DT11 Bus Switch
10. DL11-C Asynchronous Line Interface or DL11-W
11. DL11-D Asynchronous Line Interface or DL11-W
12. DL11-E Asynchronous Line Interface

If any of these devices is not included in a system, the vector address assignments move up to fill the vacancy. If a device is added to an existing system, its vector address must be inserted in the normal position and all other addresses must be moved accordingly. If this procedure is not followed, DIGITAL software cannot test the system.

Note that while the floating vectors range from addresses 300 to 777, addresses 500 through 534 are reserved for special bus testers. In addition, address 1000 is used for the DS11 Synchronous Serial Line Multiplexer.

An address map is shown in Figure B-1 and a list of the vector addresses is given in Table B-1. It should be noted that the system Teletype (KL11) is not part of the floating vector scheme and is assigned vector addresses 060 and 064; therefore, if a DL11-W is used as a control for the system Teletype console, it should be assigned addresses 060 and 064. All other DL11-Ws would follow the floating vector conventions

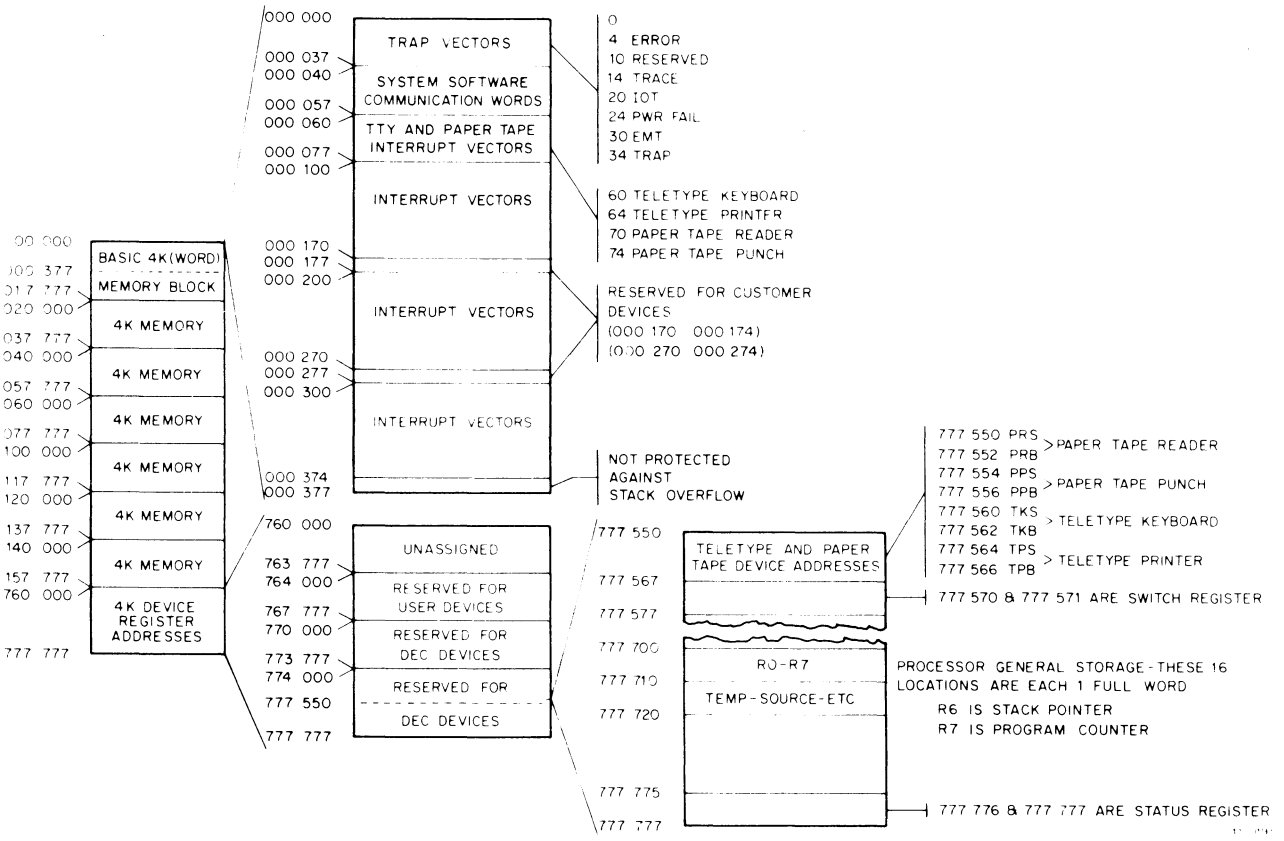


Figure B-1 Address Map

Table B-1 Interrupt Vectors

Address	Assignment
000	Reserved
004	Error Trap
010	Reserved Instruction Trap
014	Debugging Trap
020	IOT Trap
024	Power Fail Trap
030	EMT Trap
034	"Trap" Trap
040	System Software Communication Words
044	System Software Communication Words
050	System Software Communication Words
054	System Software Communication Words
060	Teletype In or DL11-W Console Interface
064	Teletype Out or DL11-W Console Interface
070	PC11 High-Speed Reader
074	PC11 High-Speed Punch
100	KW11-L Line Clock or DL11-W Line Clock
100	KW11-P Programmable Clock
110	DR11-A (Request A)
114	DR11-A (Request B)
120	XY11 X-Y Plotter
124	DR11-B
130	AD01
134	AFC11
140	AA11-A, -B, -C, -E Scope
144	AA11 Light Pen
150	
154	
160	
164	
170	User Reserved
174	User Reserved
200	LP11 Line Printer Control
204	RF11 Disk Control
210	RC11 Disk Control
214	TC11 DECtape Control
220	RK11 Disk Control
224	TM11 Magtape Control
230	CR11 Card Reader Control
234	UDC11
240	PDP-11/45 PIRQ
244	FPU Error
250	
254	RP11 Disk Pack Control
260	
264	
270	User Reserved
274	User Reserved
300	Floating vectors start at this address.

Table B-1 Interrupt Vectors (Cont)

Address	Assignment
304	
310	
314	
320	NOTE
324	**Floating vectors start at address 300 and are assigned in the**
330	**following order:**
334	
340	**1. All DC11s**
344	**2. All KL11s***
350	**3. All DP11s**
354	**4. All DM11s**
360	**5. All DN11s**
364	**6. All DM11-BBs**
370	**7. All DR11s**
374	**8. All DT11s**
400	**9. All DL11-Cs†**
404	**10. All DL11-Ds†**
410	**11. All DL11-Es**
414	
420	
424	
430	
434	
440	
444	
450	
454	
460	
464	
470	
474	
500	Special Bus Testers
504	Special Bus Testers
510	Special Bus Testers
514	Special Bus Testers
520	Special Bus Testers
524	Special Bus Testers
530	Special Bus Testers
534	Special Bus Testers
540	
544	
550	
554	
560	
564	
570	
574	
600–774	Floating vectors end here.
1000	DS11

*Or DL11-As, DL11-Bs, DL11-Ws
†Or DL11-Ws

Reader's Comments

DL11-W Serial Line Unit/
Real-Time Clock Option
Operator's Manual
EK-DL11W-OP-001

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