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DMC11 IPL synchronous line unit maintenance manual

digital

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DMC11 IPL
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CHAPTER 1

INTRODUCTION

1.1 SCOPE

This manual provides the information necessary to install, operate and maintain the DMC11 Line Unit. It is organized into five chapters and one appendix as follows.

Chapter 1 - Introduction

Chapter 2 - Installation

Chapter 3 - Register Descriptions and Programming Information

Chapter 4 - Detailed Description

Chapter 5 - Maintenance

Appendix A - Integrated Circuit Descriptions

This chapter provides a general description of the two basic variations of the DMC11 Line Unit. They are the remote unit (M8201) and the local unit (M8202). Some background material on Cyclic Redundancy Checking (CRC) methods is presented also.

1.2 DMC11 LINE UNIT GENERAL DESCRIPTION

The DMC11 Network Link consists of a synchronous line unit that is controlled by a microprocessor. The DMC11 is used to interconnect PDP-11 computers in local and remote network applications.

This manual covers four models of the line unit. They all contain circuitry to accommodate DDCMP and Bit Stuffing protocols. However, they are controlled by the DMC11-AD Microprocessor which handles only DDCMP.

DMC11-DA and DMC11-FA Line Units (Remote)

The module designation for both these line units is M8201. It contains modem control and level conversion logic that is compatible with both EIA/CCITT V24 and CCITT V35 interfaces. The DMC11-DA is shipped with a cable that accommodates only the EIA/CCITT V24 interface. This line unit has a maximum speed of 19.2K bps. The DMC11-FA is shipped with a cable that accommodates only the CCITT V35 interface and has a maximum speed of 56K bps.

DMC11-MA and DMC11-MD Line Units (Local)

Both of these line units have built-in modems. The module designation for the DMC11-MA option is M8202-YA. It operates at a speed of 1M bps over coaxial cable up to a maximum distance of 6000 feet. The module designation for the DMC11-MD option is M8202-YB. It operates at a speed of 56K bps over coaxial cable up to a maximum distance of 18,000 feet. The coaxial cable is not included with either option.

1.3 DMC11 LINE UNIT SPECIFICATIONS

DMC11-MA and DMC11-MD Line Units (Local)

Operating Mode	Half duplex (single cable), full duplex (two cables)
Data Format	Synchronous serial by bit, LSB first

Character Size	8 bits
Block Check	16 bit polynomials: CRC-16 and modified CRC-CCITT
Data Rate	1,000,000 bps (DMC11-MA), 56,000 bps (DMC11-MD)
Maximum Distance	6,000 feet (DMC11-MA), 18,000 feet (DMC11-MD)
Modulation	Diphase (double freq.) NRZ
Transmitter Timing	RC Osc., trimmable ±5%
Receiver Timing	From received signal
Line interface	Transformer coupled
Common Mode Rejection	500 to 1
Transmitter Signal	4 volts P-P (min.)
Receiver Signal	150 mV (min.) P-P
Cable Type	Belden 8232 or equivalent (not supplied)
Connector Type	AMP 20606X series
Mounting Space	One hex SPC slot (DD11B, C or D), cut-out permits use in end slots of backplane as well, provided the Unibus in/out slots contain low height (≤ 2.5 in.) modules like the M930.
Power Consumption	3.0 A at +5 V .046 A at -15 V .018 A at +15 V

DMC11-DA and DMC11-FA Line Units (Remote)

Operating Mode	Full or half duplex
Communications Channel	Private wire or switched
Data Format	Synchronous, serial by bit, LSB first
Character Size	8 bits

Block Check	16 bit polynomials: CRC-16 and modified CRC-CCITT
Data Rate	Up to 19,200 bps (DMC11-DA) Up to 56,000 bps (DMC11-FA)
Interface	RS232C or CCITT V.24 compatible (DMC11-DA), CCITT V35 compatible (DMC11-FA)
Modems	Bell 208, 209 or equivalent (DMC11-DA)
Signals Supported	BA transmit data DB serial clock transmit (SCT) BB receive data DD serial clock receive (SCR) CC data set ready CD data terminal ready CA request to send CB clear to send CE ring
Cable	25 foot with EIA connector supplied
Mounting Space	One hex SPC slot (DD11B, C or D), cutout permits use in end slots of backplane as well, provided the Unibus in/out height (≤ 2.5 in.) modules like the M930.
Power Consumption	3.2 A at +5 V .31 A at -15 V .03 A at +15 V

1.4 GENERAL DESCRIPTION

1.4.1 Introduction

This section provides a general description of the M8201 and M8202 Line Units. A more detailed description at the function level is contained in Chapter 4 Detailed Description.

The DMC11 Line Units (M8201 and M8202) perform the standard functions associated with a synchronous communications device. They are:

- Parallel to serial data conversion.
- Serial to parallel data conversion.
- SYNC character detection.
- Leading SYNC character stripping.

In addition, the line units can perform the following functions.

- Modem control and monitoring
- Cyclic redundancy character testing.
  - Zero bit stuffing
  - Zero bit stripping
- Automatic flag transmission.
- Automatic flag recognition.
- Automatic abort sequence transmission.
- Automatic abort sequence recognition.
- Automatic pad character transmission.

1.4.2 Operating Modes

The line units may operate in either of two microprogrammable modes. The modes are:

1. DDCMP mode - This is an 8-bit byte mode of operation. It is designed for the highly efficient byte oriented. Digital Data Communications Message Protocol (DDCMP) using the CRC-16 polynomial.

2. Bitstuff mode - This is a bit oriented mode of operation. It is designed for the bit oriented message protocols using the flag and abort sequences and the modified CRC-CCITT polynomial.

The line unit provides a data path between the microprocessor and a data set (or local link) and vice versa.

1.4.3 Microprocessor - Line Unit Data Path

The following discussion is keyed to the block diagram shown in Figure 4-1.

The microprocessor and line unit communicate through two unidirection data paths. Signals ALU 0-7 comprise the data path from the microprocessor to the line unit. The line unit appears to the microprocessor as 8 registers. The data is passed to the correct register by control signals CROM 0-3. Signal OBW is the strobe.

The line unit communicates with the microprocessor through the Line Unit In Bus (LU IBUS). The microprocessor controls all reading of the line unit registers.

Various maintenance signals are passed to the Maintenance and Miscellaneous logic. These signals control the functioning of the receiver and transmitter in the maintenance mode.

1.4.4 Transmitter

The transmitter portion of the line unit consists of three functional groups of logic. They are:

1. Out Data Silo
2. Transmitter Control
3. Transmitter CRC Logic

This logic performs specific parts of the transmission function. The functions are explained below.

The Out Data Silo is seen as a write only register to the microprocessor. The Transmitter Control logic sees it as a buffer. The silo is a 64 word deep data path between the microprocessor and the Transmitter Control logic.

The hardware implementation of this silo is through the use of FIFO (First In/First Out) devices. The silo effect is necessary because of the speed difference between the serialization process and the data available from the microprocessor. Because of the speed with which the microprocessor could load characters (conceivably, one character every 300 nanoseconds) and the speed at which the characters can be serialized (using dial up facilities, approximately one character every 160 microseconds), there must be a multicharacter buffer. Additionally, in order to relieve the microprogram of the need to have timers in order to know when to load another message

or when to end a message, the transmitter control bits (SOM - Start of Message and EOM - End of Message) are siloed also.

A typical sequence of operation is:

1. Microprogram loads SOM into the Out Control register.
2. Microprogram loads data into the Out Data Silo.
3. The Transmitter detects SOM at the silo output.
4. Request to send is asserted by the transmitter, automatically.
5. Clear To Send and Data Set Ready come true.
6. The transmitter is enabled. Serialization begins.

As long as the SOM bit is true, the data being serialized is not included in the CRC computation.

When the Tx Control detects a character available from the silo without the SOM bit set, it includes that character, and all the characters following it, in the CRC computation.

When EOM is detected, the Tx Control transmits the CRC Check Character (called the BCC). If more data follows the EOM, a new CRC computation is begun.

1.4.5 Receiver

The receiver portion of the line unit consists of three functional groups of logic. They are:

1. In Data Silo
2. Receiver Control
3. Receiver CRC Logic

This logic performs specific parts of the receive function. The functions are explained below.

The In Data Silo is seen by the microprocessor as a read only register. The Rx Control sees it as an output buffer. The silo is a 64 word deep data path between the Rx Control and the microprocessor.

The hardware implementation of the silo is similar to that used in the transmitter. Input to the In Data Silo is controlled by the Rx Control while output is controlled by the microprogram. The silo is present for the same reasons mentioned in the discussion of the transmitter.

A typical sequence of operations is:

1. The receiver becomes active after detecting the first data character preceded by two or more synchronizing sequences (one flag sequence in the case of Bit Stuff mode).

2. The data character is included in the CRC computation automatically.

3. The data character is loaded into the silo by the Receive Control.

4. The microprogram detects (by bit testing) both In Active and In Ready (bits 6 and 4, respectively, of the In Control register).

5. The microprogram reads the In Data Silo.

6. The silo presents In Rdy with each subsequent character.

7. The microprogram, having determined when the message ends, checks the BCC Match bit (bit 0 of the In Control register). If the bit is set, the message had no detected errors.

8. In Bit Stuff mode, the Block End bit (Bit 1 of R12) is set with the BCC Match bit, if no errors were detected.

1.4.6 Signal Conversion and Maintenance Logic

The signal conversion and maintenance logic provide automatic modem control, clock sources for the transmitter and receiver, and the receiver data source.

1.5 BASICS OF CYCLIC REDUNDANCY CHECKING

1.5.1 Mathematical Background

A cyclic code message consists of a specific number of data bits and a Block Check Character (BCC) that is computed by the CRC logic. Let n equal the total number of bits in the message and k equal the number of data bits; then n-k equals the number of bits in the BCC.

The code message is derived from two polynomials which are algebraic representations of two binary words, the generator polynomial P(X) and the message polynomial G(X). The generator polynomial is the type of code used (CRC-12, CRC-16, CRC-CCITT etc.); the message polynomial is the string of serial data bits. The polynomials are usually represented algebraically by a string of terms in powers of X such as X^n...+ X^3 + X^2 + X + X^0 (or 1). In binary form, a 1 is placed in each position that contains a term; absence of a term is indicated by a 0. The convention followed in this manual is to place the least significant bit (X^0) at the right. For example, if a polynomial is given as X^4 + X + 1 its binary representation is 10011 (3rd and 2nd degree terms are not present).

Given a message polynomial G(X) and a generator polynomial P(X), the objective is to construct a code message polynomial F(X) that is evenly divisible by P(X). It is accomplished as follows:

a. Multiply the message G(X) by X^{n-k} where n-k is the number of bits in the BCC.

b. The resulting product X^{n-k} [G(X)] is divided by the generator polynomial P(X).

c. The quotient is disregarded and the remainder C(X) is added to the product to yield the code message polynomial F(X), which is represented as X^{n-k} [G(X)] + C(X).

The division is performed in binary without carries or borrows. In this case, the remainder is always one bit less than the divisor. The remainder is the BCC and the divisor is the generator polynomial; therefore, the bit length of the BCC is always one less than the number of bits in the generator polynomial.

A simple example is explained below.

1. Given:

   Message polynomial $G(X)=110011$ $(X^5 + X^4 + X + X^0)$

   Generator polynomial $P(X)=11001$ $(X^4 + X^3 + 1)$

   $G(X)$ contains 6 data bits

   $P(X)$ contains 5 bits and will yield a BCC with 4 bits;

   therefore, $n-k=4$

2. Multiplying the message $G(X)$ by X^{n-k} gives:

   $$X^{n-k}\,[G(X)]=X^4\,(X^5 + X^4 + X + X^0)=X^9 + X^8 + X^5 + X^4$$

   The binary equivalent of this product contains 10 bits and is 1100110000.

3. This product is divided by $P(X)$

```
                    100001  <-- quotient
P(X)-->11001  | 1100110000  <-- X^(n-k) [G(X)]
              |
              11001
                 10000
                 11001
                  1001  <-- Remainder=C(X)=BCC
```

4. The remainder C(X) is added to X^{n-k} [G(X)] to give F(X)=1100111001.

The code message polynomial is transmitted. The receiving station divides it by the same generator polynomial. If there is no error, the division will produce no remainder and it is assumed that the message is correct. A remainder indicates an error. The division is shown below.

```
                    100001
P(X)-->11001  | 1100111001  <-- F(X)
              |
              11001
                 11001
                 11001
                 00000  <-- no remainder
```

1.5.2 Hardware Implementation of CRC

The BCC is computed and accumulated in a shift register during transmission. Another shift register is used during reception to examine the received data and BCC. In each register, the number of stages is equal to the degree of the generating polynomial. In the line unit, the registers have 16 stages because 16 degree generating polynomials are used. SDLC uses code CRC-CCITT whose generator

polynomial is $X^{16} + X^{12} + X^5 + 1$. DDCMP uses code CRC-16 whose generator polynomial is $X^{16} + X^{15} + X^2 + 1$.

Both the transmitter and receiver CRC registers have control logic that allows the registers to be configured for the selected CRC code.

When a message and accompanying BCC character have been received, the CRC logic only indicates whether the message is in error or not. It does not correct errors nor does it even enumerate or locate errors. Under protocol discipline, the sending station is requested to re-transmit the message.

1.5.3 CRC Operation in DDCMP Protocol

Under DDCMP protocol control, CRC operation is exactly like that described in Paragraph 1.3.4.1 Mathematical Background.

The transmitter and receiver CRC registers are initialized to all 0s. At the sending station, the transmitter CRC register accepts the information being transmitted and accumulates the BCC. When the last bit of information has been transmitted, the contents of the transmitter CRC register are transmitted.

At the receiving station, the information plus the 16 bit BCC is examined by the receiver CRC register. At the end of the message (information plus BCC), the contents of the receiver CRC register should read 0 if the message is errorless. The CRC error detection logic asserts a flag if the register reads 0. If an error is present, the register reads non 0 and the flag is not asserted. The

line unit does not count characters so it is the program's responsibility to look for the CRC error flag at the proper time.

1.5.4 CRC Operation in SDLC Protocol

Under SDLC protocol control, CRC operation is slightly different than that described in Paragraph 1.3.4.1 Mathematical Background. The differences are:

1. The factor X^k $(X^{15} + X^{14}...+ X + 1)$ is added to $X^{n-k}[G(X)]$ which corresponds to initializing the transmitter CRC register to all 1s. This function is equivalent to inverting the first 16 bits of G(X). This allows detection of the addition or deletion of 0s at the leading end of the message due to erroneous flag characters.

2. The accumulated BCC, which is called Frame Check Sequence (FSC) in the SDLC mode, is complemented before being transmitted. This results in a unique non-0 remainder (016417_8) at the receiver. This allows detection of the erroneous addition or deletion of 0s at the trailing edge of the message due to errors.

3. At the receiving station, the receiver CRC register is initialized to all 1s. The information plus the FCS constitutes the message and it is added to X^k $(X^{15} + X^{14}...+ X + 1)$ and divided by P(X) to give 016417_8, if the transmission is errorless. If an error is present, the flag is asserted.

CHAPTER 2

INSTALLATION

2.1 SCOPE

This chapter provides information for installation and checkout of the M8201 and M8202 line units.

2.2 UNPACKING AND INSPECTION

The line unit comes in four versions which are described below.

DMC11-DA (For EIA/CCITT V24 Interface)

- M8201 - Line Unit Module
- BC08R-1 or BC08S-1 - Interconnect Cable
- BC05C-25 - Modem Cable
- H325 - Test Connector

DMC11-FA (For CCITT V35 Interface)

- M8201 - Line Unit Module
- BC08R-1 or BC08S-1 Interconnect Cable
- BC05Z-25 - Modem Cable
- H - Test Connector

DMC11-MA (Local 1M bps)

- M8202-YA - Line Unit Module
- BC08R-1 or BC08S-1 Interconnect Cable
- 12-12528 - Coaxial Test Connector

DMC11-MD (Local 56K bps)

- M8202-YB - Line Unit Module
- BC08R-1 or BC08S-1 - Interconnect Cable
- 12-12528 - Coaxial Test Connector

Inspect these parts for visible damage. Report any damage or shortage immediately to the shipper and the DEC representative.

2.3 PRE-INSTALLATION SETUP PROCEDURES

NOTE

The line unit cannot function without the DMC11-AD Microprocessor (M8200). It is assumed that the DMC11-AD has been installed and checked out in accordance with Chapter 2 Installation of the Microprocessor manual (EK-DMCUP-MM-001).

Before installing the line unit, check the jumpers and switches to be sure that they are in the normal configuration.

1. Jumpers

   The M8201 Line Unit contains five jumpers (W1-W5). The M8202 Line Unit contains six jumpers (W1-W6). Refer to the components location drawing in the print set to locate the jumpers. The normal jumper configurations are described in Table 2-1 for the M8201 and Table 2-2 for the M8202.

2. Switch Packs No. 2 and No. 3.

   Switch packs no. 2 and no. 3 are both 8 switch DIPs. Switch pack no. 2 is Register 15 and is installed in location E87 on the M8201 Line Unit and in location E90 on the M8202 Line Unit. Switch pack no. 3 is Register 16 and is installed in location E88 on the M8201 Line Unit and in location E91 on the M8202 Line Unit.

Table 2-1

M8201 Jumper Configurations

Jumper Number	Normal Configuration	Function
W1	Installed	With this jumper installed, the transmitter CRC character is not inverted by the CRC register output gate. This jumper must be in to ensure proper operation of codes CRC-16 and CCITT under the discipline of DDCMP and Bit Stuff protocols. If the user removes this jumper for some special reason, the Transmitter CRC character is inverted by the CRC register output gate. The diagnostic will fail also.
W2	Installed	Jumpers W2 and W3 are used together.
W3	Removed	With W2 installed and W3 removed, the modem Data Set Ready line controls the state of signal D16 MODEM RDY H. With W3 installed and W2 removed, signal D16 MODEM RDY H is always asserted. This feature accommodates modems that require Data Set Ready to be on continuously.
W4	Installed	Jumpers W4 and W5 are used together.
W5	Removed	With W4 installed and W5 removed, signal D15 DTR H controls the state of the modem Request to Send line. With W5 installed and W4 removed, the Request to Send line is on continuously. This feature accommodates modems that require this condition.

Table 2-2

M8202 Jumper Configurations

Jumper Number	Normal Configuration	Function
W1	Installed	With this jumper installed, the transmitter CRC character is not inverted by the CRC register output gate. This jumper must be in to ensure proper operation of codes CRC-16 and CCITT under the discipline of DDCMP and Bit Stuff protocols. If the user removes this jumper for some special reason, the Transmitter CRC character is inverted by the CRC register output gate. The diagnostic will fail also.
W2, W3	Removed	When installed, the modem receiver protection transformer is disabled. Installation is not recommended.
W4, W5	Removed	When installed, the modem transformer protection transformer is disabled. Installation is not recommended.
W6	Removed	Installed for 1-wire half-duplex operation only.

When the line unit module is shipped, all switches in both packs are OFF. This is the default status (377_8).

These switches are a function of the down-line loading feature of the DMC11. After installation, the switches can be positioned to accommodate the users requirements. For details, refer to Chapter 3 in the microprocessor manual.

3. Switch Pack No. 1

Switch pack no. 1 is an 8 switch DIP that is installed in location E26 on the M8201 Line Unit and in location E29 on the M8202 Line Unit.

For the M8201, all switches except no. 5 are used. For the M8202, all switches except no. 4, 5, and 8 are used. The ON and OFF positions and the switch numbers are marked on the package. The switches are the rocker type and are pushed to the desired position.

Table 2-3 describes the normal configuration for switch pack no. 1.

2.4 INSTALLATION AND CHECKOUT

The M8201 and M8202 Line Units are hex modules. They do not interface with the Unibus so module edge connectors A and B are not required. As a result, the corner of the module in the vicinity of the A and B

Table 2-3

Configuration of Switch Pack No. 1

Switch Number	Normal Position	Function
1	OFF	With S1 OFF, signal D14 GRTP is low which enables the following ROMs. Transmitter Function Decode ROM Transmitter Data Decode ROM Receiver Decode ROM Receiver Function ROM During servicing with the automatic module tester, if S1 is ON, signal D14 GRTP is high which disables these ROMs.
2	OFF	With S2 OFF, signal D14 NO CRC is low, which allows the CRC function to be enabled. With S2 ON, the CRC function is inhibited.
3	OFF	With S3 OFF, signal D14 SEC MODE is low which inhibits operation of the line unit in the secondary mode. This mode is applicable only in the Bit Stuff protocols.
* 4	OFF	With S4 OFF, Received Data, Modem Receive Clock, and Modem Transmit Clock are presented to the line unit through the EIA/CCITT V24 interface. With S4 ON, these signals are received through the CCITT V35 interface. This switch is used only on the M8201 Line Unit.
5		Not Used

Table 2-3 (Cont)

Configuration of Switch Pack No. 1

Switch Number	Normal Position	Function
6	OFF	Signal D14 SECURE is associated with this switch. It is bit 0 of the Modem Control Register. This bit is reserved and is read only.
7	Module Dependent	Signal D14 SW is associated with this switch. It is read only bit 1 of the Modem Control Register. It is read by the diagnostics and indicates the type of line unit. With an M8201 Line Unit, S7 should be ON (D14 SW is low). With an M8202 Line Unit, S7 should be OFF (D14 SW is high).
8	ON	With S8 ON, the internal RC clock is sent to the modem cable connector (J1) on the M8201 Line Unit. During servicing with the H325 test connector installed on the modem cable, the RC clock is sent back to the line unit as the transmit and receive clocks. During normal operation, the switch should remain ON. This switch is used only on the M8201 Line Unit.

connectors has been removed. This allows the M8201 or M8202 to be installed in the end slots of the DD11-B, C, or D System Interfacing Units. The module plugs into connectors C, D, E, and F and fits over the Unibus cable connectors and short length (approx. 2-1/2 in.) Unibus terminator that are installed in connectors A and B.

Proceed with the installation and checkout as follows.

1. Install the M8201 or M8202 Line Unit.

2. Interconnect the line unit and the microprocess using cable BC08R-1 or BC08S-1 which is a one-foot long 40 conductor flat mylar cable with H856 female connectors on each end. The mating connector on the microprocessor and line unit is an H854 male connector. On the microprocessor this connector is designated J1. On the M8201 Line Unit it is designated J2 and on the M8202 Line Unit it is J1.

3. On the M8201 Line Unit, install the BC05C-25 cable to connector J1. On the other end of this cable, connect the H325 test connector.

   On the M8202 Line Unit, install the 12-12528 coaxial test connector which ties the two coaxial pig-tails together. These two 3-foot cables are soldered to the M8202.

4. Run MAINDEC-11-DZDME and DZDMF to verify correct line unit operation.

5. Run MAINDEC-11 DZDMG to verify correct line unit/microprocessor system operation.

6. Remove the test connector from the line unit.

M8201 - Connect the BC05C-25 Cinch connector to the customer supplied modem.

M8202 - Connect the coaxial pig-tails to the customer supplied coaxial cables.

CAUTION

The maximum allowable length for the BC05C or BC05Z cable is 50 feet.

2.5 JUMPER AND SWITCH CHECKLIST

Table 2-4 represents a concise checklist of the M8201 and M8202 Line Unit switch settings and jumper configuration as shipped.

Table 2-4

Jumper and Switch Checklist

Jumper Configuration

Jumper Desig.	DMC11-DA M8201	DMC11-FA M8201	DMC11-MA/MD M8202
W1	IN	IN	IN
W2	IN	IN	OUT
W3	OUT	OUT	OUT
W4	IN	IN	OUT
W5	OUT	OUT	OUT
W6	NA	NA	IN FOR HD
Settings For Switch Pack No. 1			
S1	OFF	OFF	OFF
S2	OFF	OFF	OFF
S3	OFF	OFF	OFF
S4	OFF	ON	OFF
S5	OFF	OFF	OFF
S6	OFF	OFF	OFF
S7	ON	ON	OFF
S8	ON	ON	OFF
Settings for Switch Pack Nos. 2 and 3			
S1-S8	OFF	OFF	OFF

NOTES:

1. Switch Pack Locations

   SP1-E26 on M8201 and E29 on M8202
   SP2-E87 on M8201 and E90 on M8202
   SP3-E88 on M8201 and E91 on M8202

2. All switches OFF in SP2 and SP3 represents the default status. Reference the DMC11 Microprocessor Manual for details on the use of these switches.

2.6 LOCAL LINK CABLE

This section discusses the selection, installation, and maintenance of the local link cable. This cable must serve two purposes. The link cable must deliver the generated signal to the receiver with sufficient amplitude to exceed the receiver threshold and it must shield the signal from external electrical noise.

2.6.1 Selection

For use in the DMC11, Digital recommends the Belden 8232 double shielded (triaxial) cable, or its equivalent. The electrical characteristics are listed below. The nominal specifications are given unless otherwise stated.

Inductance	0.097 microhenrys/ft (.318 microhenrys/meter)
Capacitance	17.3 pF/ft (56.7 pF/meter)
Vel. of Prop.	78%
Impedance	75 ohms
Attenuation (MHz)	dB/ft
1	.25
10	.8
50	1.8
100	2.7
Voltage Rating	175 Vrms
Sweep Test	22 dB min.
Conductor DC resistance	34.5 ohms/1000 ft (111.5 ohms/km)
Shield DC resistance (each shield)	2.6 ohms/1000 ft (8.53 ohms/km)

The required physical characteristics are:

Triaxial
Cellular polyethylene insulation
20 AWG center conductor

The Belden 8232 cable meets all of these requirements. The cable provides the required 75 ohm match to the line unit transmitter and receiver circuits. Its double shield provides excellent noise rejection. The combination of the 20 AWG center conductor and cellular polyethylene dielectric provide low signal loss and distortion. The polyethylene jacket has excellent weather and abrasion resistance, very good chemical resistance, fair flexibility and it does not contaminate the other dielectric. Other typical communications cable types (i.e., typical RG 59/u coax with 22 AWG conductor) using a solid polyethylene dielectric and single shield cannot be used for a 6000 foot connection.

When selecting cable, several factors must be considered in determining cable attenuation. The value given by the cable vendor is for room temperature and is nominal, being subject to deviation up to 20%. The attenuation increases with temperature at approximately 0.20%/^{o} C (0.11%/^{o} F). At 50^{o} C (122^{o} F) an additional loss of 5% over the room temperature specification can be expected. Finally, use at elevated temperatures causes aging at a faster than normal rate, and after 5 years, could produce yet another permanent 10% increase in attenuation. Thus the initial nominal 2.6 dB/1000 ft loss could become, after 5 years use at high temperature, 5.2 dB/1000 ft worst case.

2.6.2 Installation

The characteristics of the local link cable should be measured prior to installation. In particular there are two parameters that the user should measure and note for future reference. These are the propagation time delay, which can be measured with a pulse generator and an oscilloscope, and the dc resistance of the cable with the far end of the center conductor shorted to the inner shield. For the Belden 8232, these parameters can be expected to be nominally 1.30 ns/ft and 32 ohms/1000 ft. Once the cable is installed, and both ends are therefore not available at the same place, the latter parameter can still be measured easily, and the former can be measured by use of the TDR method described in Paragraph 2.6.3.

While installing the cable, make a complete map of its layout, showing the position of the cable with respect to buildings, equipment and so forth, and also the locations of all access points, including not only splices and in-line connectors, but pull boxes also. Carefully measure and record cable lengths between landmarks. Such a map will greatly facilitate maintenance.

The user must take the following factors into account when installing the local link cable.

TEMPERATURE - The polyethylene used as the dielectric material in most coaxial and triaxial cables begins to soften above 80^{o} C. As the conductor moves off center, variations in cable characteristics

occur. If installed under tension with sharp bends, the conductor may short to the shield. Additionally, the open circuit resistance should be measured after installation to ensure against shorts incurred during installation. This resistance should be $\geqslant$ 20K ohms. The closed circuit resistance should be 36.1 ohms/ft.

MOISTURE - Moisture or moisture-related impurities may enter the cable through cuts or scratches in the outer jacket or through improperly installed connectors. Minute amounts of water vapor will condense into water, which can migrate along the braid. Water condensed from a polluted atmosphere can contaminate the entire length of cable, shorten its lifetime, and seriously degrade performance.

PULLING TENSION - For most environmental conditions it is generally preferred that the cable be installed in conduit, through which the cable must be pulled. During installation, the total pulling tension on the 20 AWG center conductor must not exceed 12 pounds (8N).

For ease in maintenance it is best to divide the cable into sections. For long cable runs in conduit, it is convenient to have a pull box every 100 feet or equivalent. A 90 degree conduit bend is equal to 30 feet of straight level conduit. It is recommended that an antifriction agent be used during pulling, provided the agent is compatible with the cable jacket material.

SPLICES AND CONNECTORS - The cable layout should provide access points for test purposes and for replacing defective sections. (See Paragraph 2.6.2.1.) Strain relief must be provided at all splices and in-line connectors.

RECOMMENDED WIRING PRACTICES - Chapter 8, Article 800 of the National Electric Code defines wiring rules for communications circuits. These rules must be observed for safe operation of the DMC11. In particular, note these provisions of the code:

"Communication conductors shall not be placed in a raceway, compartment, outlet box, junction box or similar fitting with conductors for light and power. . ."

"Communication conductors may be run in the same shaft with conductors for light and power provided the conductors of the two systems are separated by at least two inches."

"Suitable protective devices must be employed for wiring between buildings."

SURGE WITHSTAND CAPABILITY - The receiver has no provision for protection against normal mode voltage surges exceeding 30 V. If surge withstand is required, the user must install a separate circuit to condition signals to the receiver.

NOISE - The M8202 is designed to operate with a common mode rejection ratio $\geq$ 500:1. Cable selection, installation grounding and noise suppression are means of reducing line error rates.

2.6.2.1 Connectors - The following components are recommended for use in joining cable sections and also for connecting the cable to the M8202 pigtails. All of these components which are shown in Figure 2-1, are manufactured by AMP Inc., Harrisburg, Pennsylvania.

Component	Digital Part Number	AMP Part #
Cable clamp	12-11430	206062-1
Male housing	12-12527	206152-1
Male pin	12-12001	66536-2
Female housing	12-12526	206060-1
Female pin	12-12000	66594-2

The connectors are installed by crimping the pins to the cable; the recommended crimper is the AMP Type V1, 90293-1. It is very unlikely that one can install a set of connectors without requiring the use of an ejector, to remove pins that have been inserted incorrectly; the proper ejector for the above pins is the AMP 305183.

The pin holes in the housing and receptacle are numbered. When working with a connector, always orient it so that hole 1 is at the top, then hole 4 is at the bottom, and the holes on either side are 2 and 3.

TO BE SUPPLIED

Figure 2-1 Local Link Cable Connectors

1. The cable clamp assembly is supplied as a shell, two screws, and three clamps, of which the one for the largest cable size should be used. Slide the shell onto the cable.

2. Dress the center conductor back enough so it will fit into a pin with the pin crimped to its insulation as well as to the conductor. Dress both shields back about another half inch, and taper the final half inch of the inner insulation so that its tip fits into the pin, and about a quarter inch fits into the connector, along with the center conductor. Crimp the pin to both the conductor and its insulation, and insert the pin in hole 1.

3. Separate the inner shield into two parts, attach pins to them, and insert the pins into holes 2 and 3.

4. Pull the outer shield together, insulate it from the inner shield, crimp a pin to it, and insert the pin in hole 4.

5. Screw the shell into the housing, and screw the clamp to the shell.

6. After male and female connectors have been plugged together, screw the other ring of the female housing over the male housing.

Both M8202 pigtails have female connectors, therefore, the local link cable must have a male connector. The connectors at the ends of the cables are installed in the same manner described above except that at the ends the outer shield must be grounded as described in Paragraph 2.6.2.2. The male connector shown in Figure 2-1 is made up for the computer connection. The wire sticking out the back end of the connector is the outer shield.

2.6.2.2 Grounding - The outer braided shield of the cable must be grounded near, but not to, the computer system chassis. The grounding conductor should be connected to a water pipe electrode, or if none is available, to the power service conduit, service equipment closure, or grounding electrode conductor where the grounding conductor of the power service is connected to a water pipe electrode at the building.

When neither of the above means of grounding is available, it is permissible to connect the grounding conductor to the service conduit, service equipment enclosure, grounding electrode conductor, or grounding electrode of the power service of a multigrounded neutral power system.

If it is impossible to ground the cable shield by one of the above methods, connect the grounding conductor to one of the following:

1. A concrete-encased electrode of not less than 20 feet of bare copper conductor, no smaller than 4 AWG, encased in at least 2 inches of concrete, and located within and near the bottom of a concrete foundation footing that is in direct contact with the earth.

2. An effectively grounded metal structure.

3. A continuous and extensive underground gas-piping system, where acceptable to both the servicing gas supplier and to the authority having jurisdiction.

4. A ground rod or pipe driven into permanently damp earth.

WARNING

Under no circumstances shall the grounding conductor be connected to a steam or hot water pipe, a lightning rod conductor, or pipe or rod electrodes grounding other than multiground neutral power circuits.

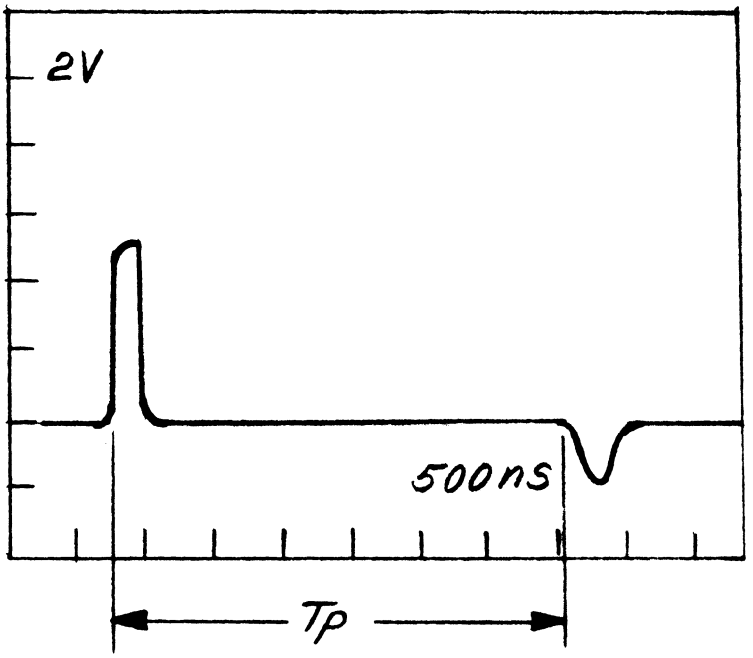
2.6.3 Maintenance

For maintenance purposes, the user should keep a record of the initial cable characteristics, particularly the propagation time delay and short circuit line resistance as indicated at the beginning of Paragraph 2.6.2. Once the system is operational, record the received signal amplitude at the M8202. Then repeat this measurement at every

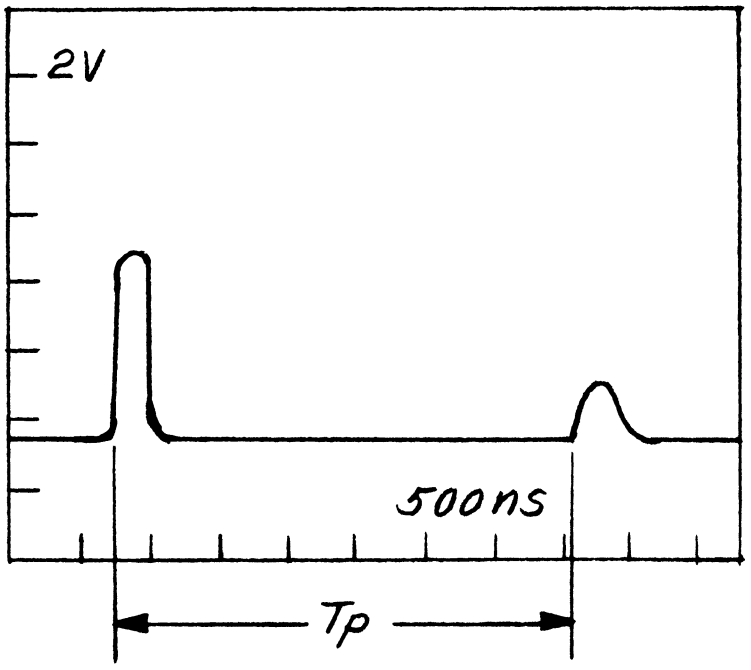
scheduled PM date (at least four times per year). If a deviation of 20 percent is observed in the signal amplitude, disconnect both ends of the cable from the M8202 and measure both the open circuit and short circuit resistance of the line. If the measured open circuit resistance is less than 20 megohms, inspect the cable for contamination of the dielectric, and for adverse effects of sharp bends or stress points, elevated temperatures, or aging. If the line resistance with a shorted end increases above the value measured at installation, inspect the cable for loose connectors, contaminated connectors, and excessive tension.

LOCATING A DEFECTIVE SECTION - An ohmmeter can be used to diagnose an open line or a low impedance shorted line, by checking one section at a time until the faulty section is located. If the cable is not partitioned into small enough sections, the distance to the fault can be measured by making use of time domain reflectometry (TDR).

Although TDR cable testers are available from Tektronix and others, a pulse generator and oscilloscope can be used for approximate measurements. Disconnect both ends of the cable, and drive one end with a 5 V peak, 100 ns wide pulse with a repetition rate below 10 kHz. Measure the time interval between the leading edge of the driven pulse and the leading edge of the first reflection. The reflected pulse will be in the 10 mV to 1 V range. It will be normal for a line open, but inverted for a line short. Figure 2-2 shows typical oscilloscope traces for both cases. The time interval represents the propagation time delay for a round trip from the signal



SHORTED LINE



OPEN LINE

Figure 2-2 Signal Reflections from a Line Fault

generator to the fault and back again. The distance D to the fault in feet (meters) is

$$D = T_p/2p$$

Where T_p is the measured time delay in nanoseconds, and p is the propagation time in nanoseconds per foot (meter) recorded before the cable was installed.

2.7 FULL DUPLEX/HALF DUPLEX OPERATION

The DMC11 is capable of either full-duplex or half-duplex operation. The microprogram controls the transmitter-receiver interaction in half-duplex mode in order to minimize the line control contention problems.

While there are few considerations required when selecting half-duplex operation of the DMC11-DA or DMC11-FA Line Units, careful thought should be given to the selection of full or half-duplex operation of the DMC11-MA-DMC11-MD Line Units.

Full- or half-duplex operation of the DMC11-DA/FA requires selecting the proper data set and informing the microprogram that half-duplex mode has been selected.

Operation of the DMC11-MA/MD Line Units require hardware considerations. Full-duplex opeation requires two separate local link cables. Half-duplex operation requires only one. The two cable requirement for full-duplex operation cannot be eliminated through the use of a dual Coax/Triax cable.

While full-duplex operation requires two cables, it also provides full throughput potential. Half-duplex operation implies half the throughput potential but requires only one cable. The following factors should be considered when selecting full-duplex or half-duplex operation.

1. Traffic Flow - Is most of the data going one way or is data flow nearly equal in both directions?

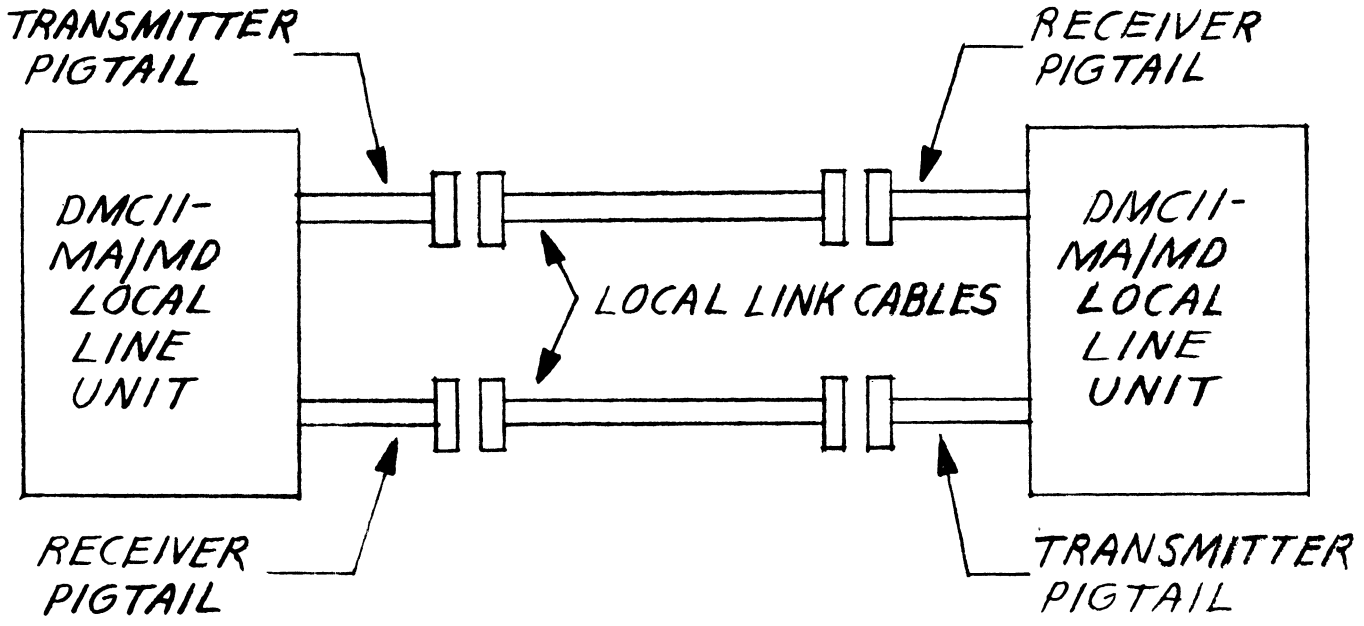
2. Data Rate - Is it necessary to use maximum data rate now and in the foreseeable future?

3. Cable Expense - Is the two cable full-duplex operation worth the expense?

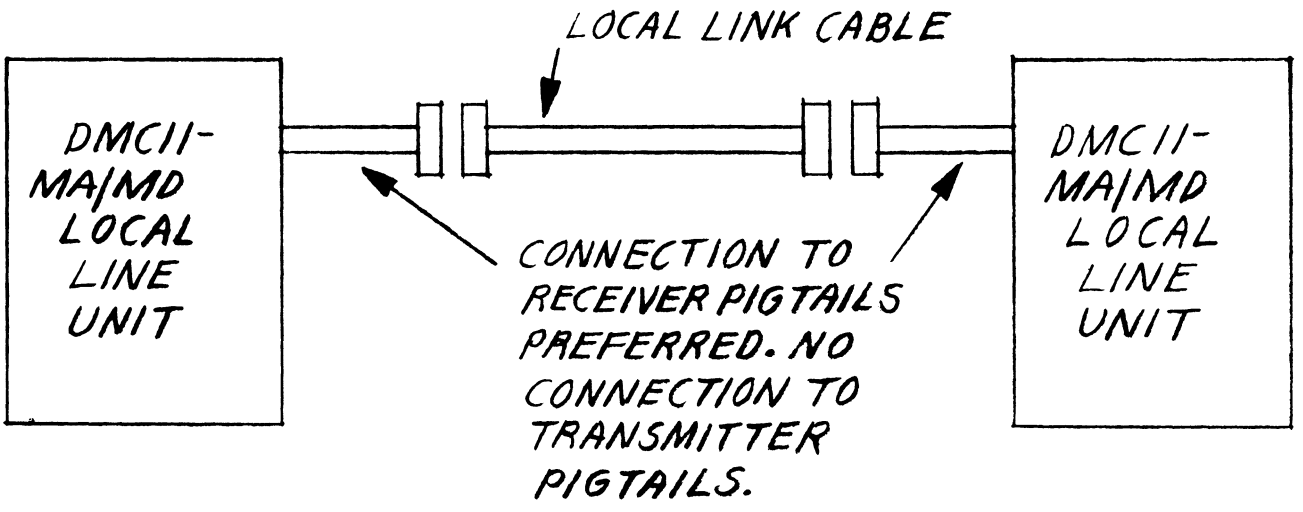
The local link line units (DMC11-MA/MD) require installation of the W6 jumper for half-duplex operation. This allows either line unit pigtail to be used as the output connection to the local link cable.

The connection to the local link cable is made so that the local transmitter pigtail is connected to the distant receiver pigtail through the local link cable (Figure 2-3).

In the case of half-duplex operation, the connection to the local link cable is made with either of the pigtails (Figure 2-3).



FULL DUPLEX



HALF DUPLEX

Figure 2-3 Full-Duplex/Half-Duplex Connections

CHAPTER 3

PROGRAMMING

3.1 INTRODUCTION

This chapter contains general programming information. It is divided into two sections: one lists the register bit functions and the other discusses programming procedures.

3.2 REGISTERS AND DEVICE ADDRESS SELECTION

The nine registers used in the line unit are shown in Table 3-1. They are all 8 bit registers.

The DMC11 (microprocessor plus line unit) is assigned a device address in the floating address space which includes addresses 760010 through 764000. The device address selection logic is located physically on the microprocessor module. The line unit registers are selected by four address signals from the microprocessor.

3.3 REGISTER BIT ASSIGNMENTS

Bit assignments for all the registers are shown in Figure 3-1. If applicable, the register is described by showing a bit assignment illustration and an accompanying table that discusses each bit in detail.

The cable that connects the line unit and the microprocessor contains two buses. The IN BUS (IBUS) carries information from line unit to the microprocessor. The OUT BUS (OBUS) carries information from the microprocessor to the line unit.

Table 3-1

Line Unit Registers

Name	Address	Comments
In Data Silo	10	Read only
Out Data Silo	10	Write only
Out Control Register	11	Read/write
In Control Register	12	Read/write
Modem Control Register	13	Read/write
Sync Register	14	Read/write
Register 15	15	Bits are switch selectable. Read only.
Register 16	16	Bits are switch selectable. Read only.
Maintenance Register	17	Read/write

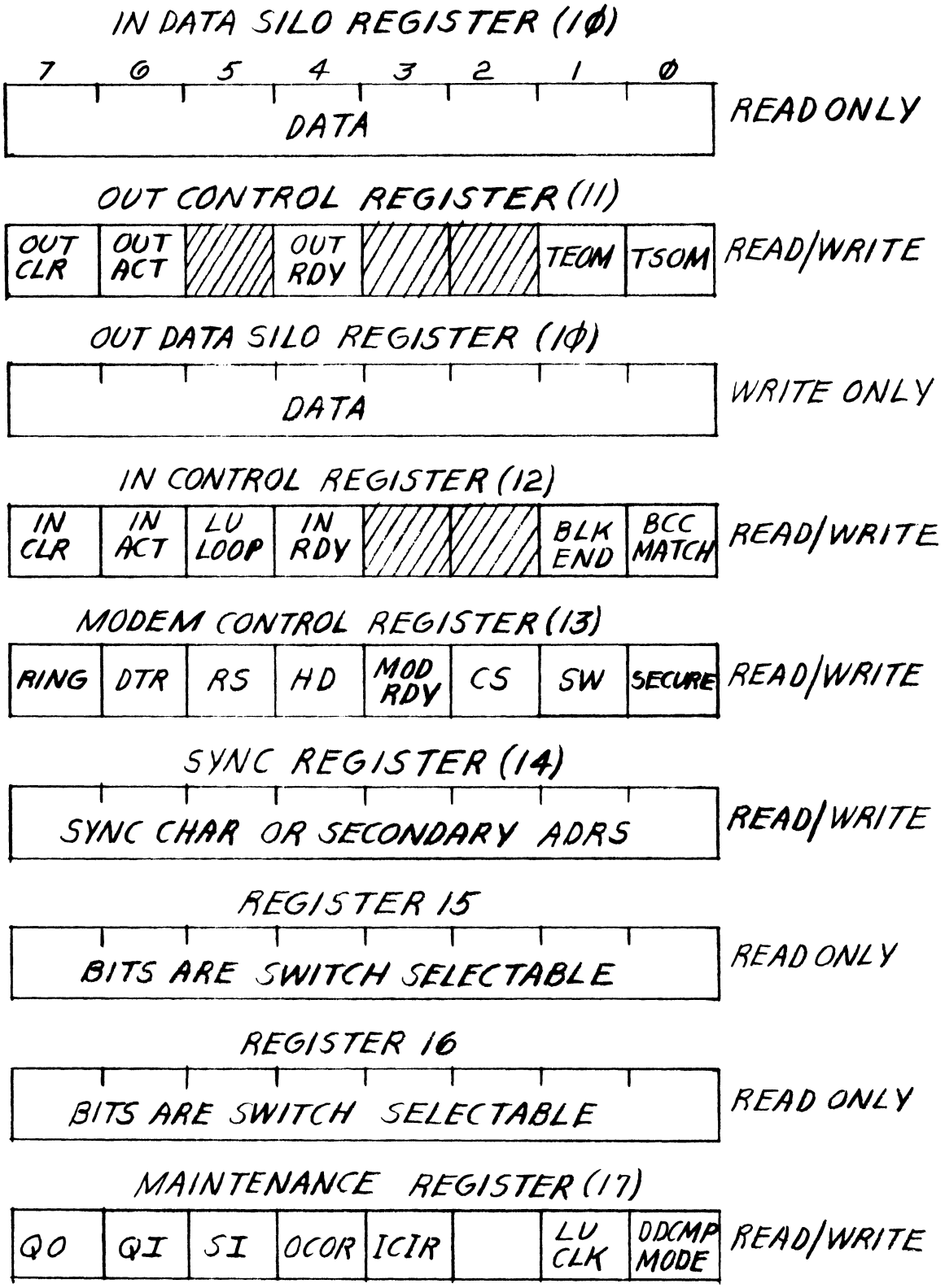


Figure 3-1 Line Unit Register Configurations and Bit Assignments

3.3.1 Data Silo Registers

The line unit contains two data silo registers. They are the In Data Silo which is read only and the Out Data Silo which is write only. The two buses (In Bus and Out Bus) that interconnect the line unit and microprocessor allow these registers to share the same address (10 octal). When register 10 is selected on the In Bus, the data in the In Data Silo is read by the microprocessor. This is an 8-bit data character from the receiver. When register 10 is selected on the Out Bus, the microprocessor writes data into the Out Data Silo. This is an 8-bit data character to be transmitted.

Both silos are 64 x 12 bit FIFOs. The In Data Silo and Out Data Silo each contain 8 bits (0-7 of the silo). In each case, the remaining 4 bits (8-10) belong to another register. For the In Data Silo, these are bits 0-3 of the In Control Register (11 octal). For the Out Data Silo, these are bits 0-3 of the Out Control Register (12 octal).

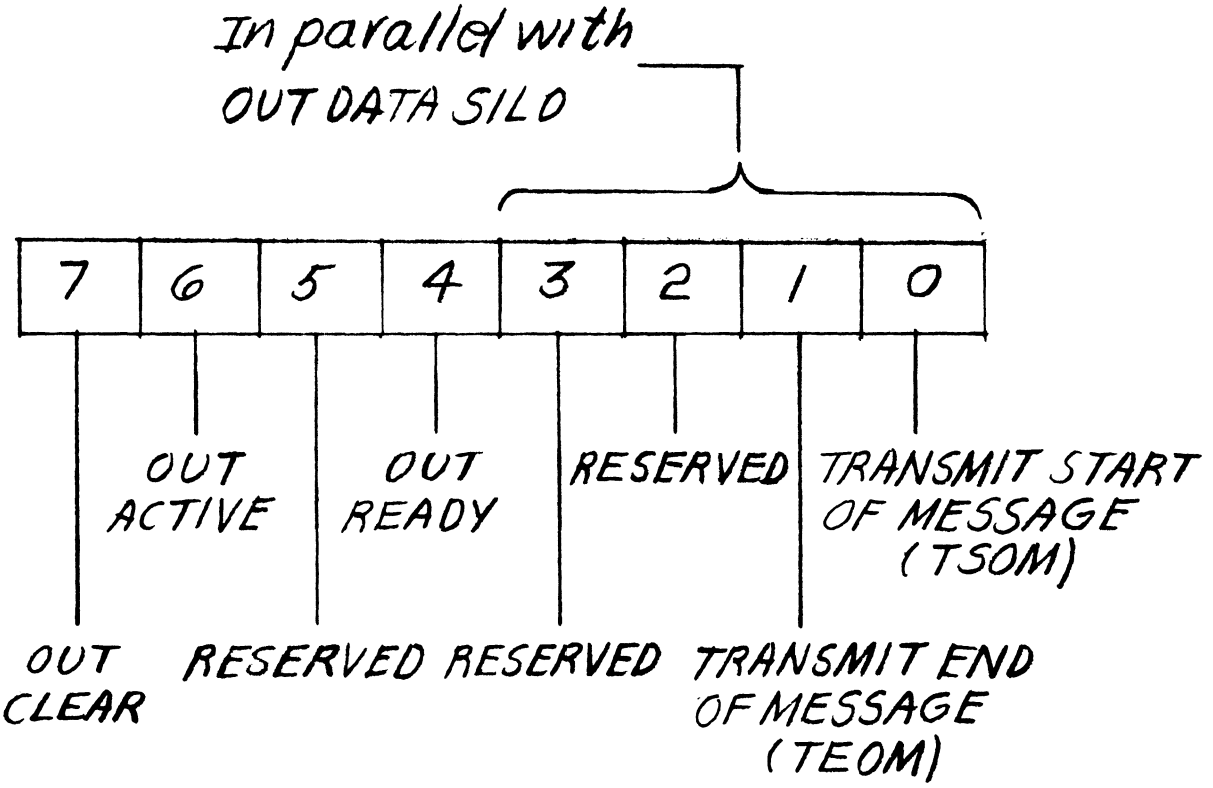
In Control Register bits 0-4 are updated every time register 10 is read. Therefore, they must be read before register 10 is read or they will be lost.

Out Control Register bits 0-4 are passed to the transmitter through the silo every time register 10 is written into. Therefore, if control information is to be passed, these bits must be written into before register 10 is written into.

3.3.2 Out Control Register (Figure 3-2)

Bit	Name	Description
0	TSOM (Transmit Start of Message)	This bit is used to initiate the start of a new message. DDCMP Mode: The Sync character must be loaded into the Out Data Silo along with the TSOM bit. This character is transmitted as the Sync character until TSOM is cleared. Until it is cleared, the characters are not included in the CRC accumulation. When TSOM is cleared, the present Sync character is transmitted and is followed by data. All data is included in the CRC accumulation, if CRC is enabled. Once TSOM has been set, the CRC accumulation cannot be inhibited unless the line unit is initialized. Bit Stuff Mode: When TSOM is set, a flag character is automatically transmitted. The character that is loaded with the TSOM bit is lost. Flag characters are automatically transmitted as long as TSOM is set. When data is to be transmitted, TSOM is cleared and data is loaded into the Out Data Silo. At the completion of the current flag character, the actual transmission of data begins. All information to be transmitted is included in the CRC accumulation, if the CRC function is enabled.

Bit	Name	Description
		This bit is program write only. It is cleared by the initialization logic and by the fact that data was loaded into the Out Data Silo. This bit is loaded into the silo and passed to the transmitter through the silo.
1	TEOM (Transmit End of Message)	This bit is used to terminate the message in progress and control the transmission of the CRC character, if the CRC function is enabled. DDCMP Mode: When TEOM is set, the CRC character is transmitted. If no more messages are pending (TSOM cleared), the transmitter is shut down. Bit Stuff Mode: When TEOM is set, the character loaded with it is lost. The CRC character is transmitted. If no more messages are pending, the transmitter is shut down by having a second TEOM in the silo. This generates a single terminating or inter-message flag. This bit is program write only. It is cleared by the initialization logic and by



NOTE

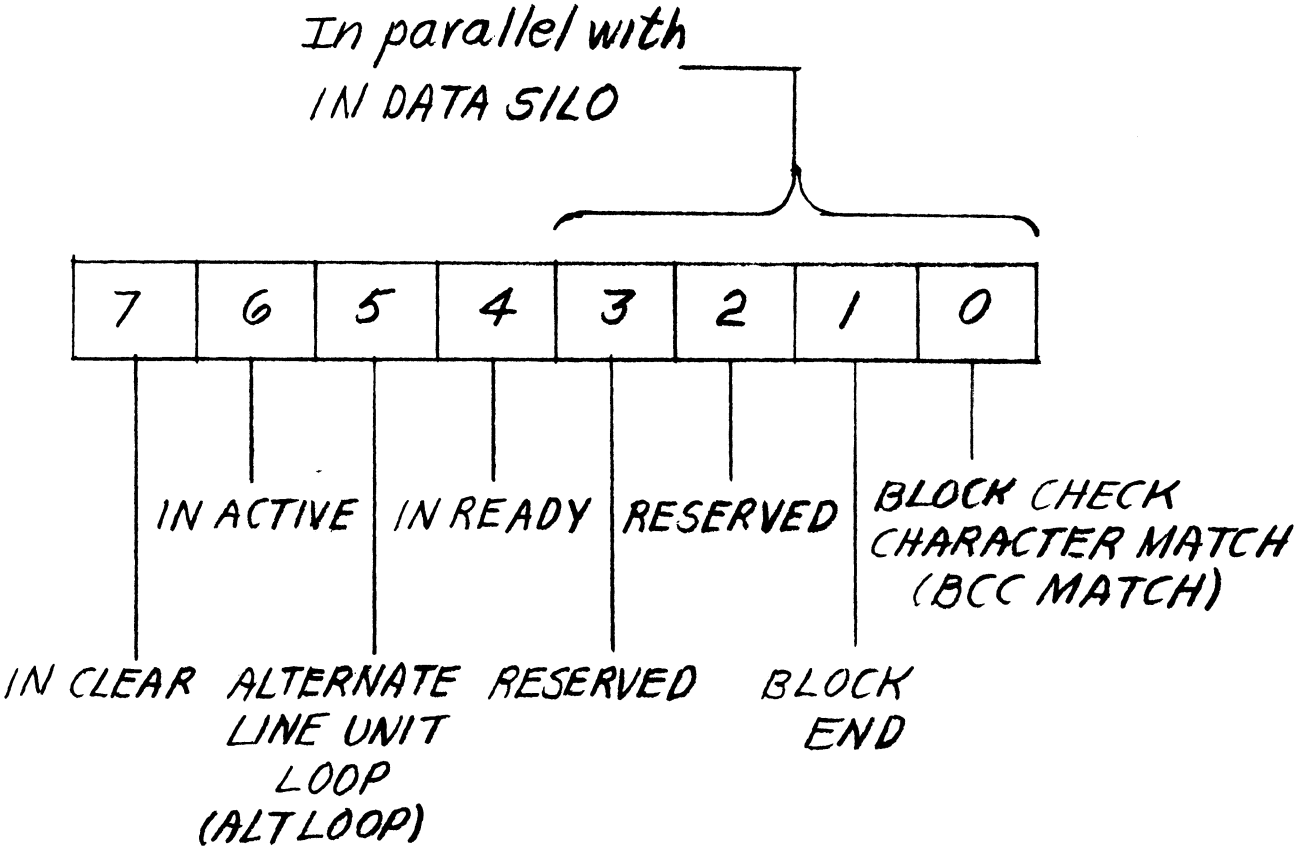
Bits Ø-3 are passed to the transmitter through the silo every time register 1Ø is written into. Therefore, if control information is to be passed, these bits must be written into before register 1Ø is written into.

Figure 3-2 Out Control Register Format

Bit	Name	Description
		the TSIP flip-flop which is set whenever data is loaded into the Out Data Silo. This bit is loaded into the silo and passed to the transmitter through the silo.
2 and 3	Reserved	These bits are program write only. They are cleared by the initialization logic and by the TSIP flip-flop which is set whenever data is loaded into the Out Data Silo.
4	OUT RDY (Out Ready)	When asserted, this bit informs the microprocessor that the transmitter is ready to accept data. It indicates that space is available in the Out Data Silo. The microprocessor loads the Out Data Silo and then reads OUT RDY. The speed of the microprocessor allows OUT RDY to be read and interpreted as true before the silo has loaded the data. Therefore, one cycle must elapse between loading the silo and reading OUT RDY. This bit is read only.
5	Reserved	Read only. This bit is switch selectable.
6	OUT ACTIVE	OUT ACTIVE informs the microprocessor of the status of the transmitter. When it is set, the transmitter is active. This bit is read only. It is set by the hardware and cleared by the initialization logic.
7	OCLRP (Out Clear)	This bit is used to clear all the transmitted functions. OCLRP is program write only.

3.3.3 In Control Register (Figure 3-3)

Bit	Name	Description
0	BCC MATCH (Block Check Character Match)	BCC MATCH is the output of the receiver CRC error logic that monitors the contents of the CRC register. With the CRC function enabled, BCC MATCH is asserted at the end of an errorless message. In the DDCMP protocol, the contents of the Receiver CRC Register equals zero when an errorless message has been received. In the SDLC protocol, the contents of the Receiver CRC Register equal 016417. This bit is read only and is updated every time register 10 is read.
1	BLOCK END	BLOCK END is used to inform the microprocessor, in SDLC mode, that a terminating flag has been received. This flag may be the leading flag for the next message. The BLOCK END bit is loaded with the high byte of the CRC character; therefore, the BLOCK END bit along with the BCC MATCH bit should be used to indicate reception of a good message. This bit is read only and is not used in the DDCMP mode. It is updated every time register 10 is read.
2 and 3	Reserved	Read only.
4	IN RDY (In Ready)	When asserted, this bit informs the microprocessor that received data is ready for processing. It indicates that data is available at the output of the In Data Silo. This bit is read only.



NOTE

Bits 0-3 are updated every time register 10 is read. Therefore, they must be read before register 10 is read or they will be lost.

Figure 3-3 In Control Register Format

Bit	Name	Description
5	ALT LU LOOP (Alternate Line Unit Loop)	During maintenance, this bit is set to loop the receiver on the transmitter with no connection to the modem control lines. This bit is program read/write.
6	IN ACTIVE	When asserted, this bit informs the microprocessor that the receiver is in the data reception mode; that is, it is receiving data or CRC characters. DDCMP Mode: IN ACTIVE is asserted upon receipt of the first non-sync character. SDLC Mode: IN ACTIVE is asserted upon receipt of the first data character.
7	ICLRP (In Clear)	This bit is used to clear all the receiver functions. ICLRP is program write only.

3.3.4 Modem Control Register (Figure 3-4)

Bit	Name	Description
0	SECURE	The function of this bit is reserved for future use. This read only bit is selected by a switch. SECURE is asserted when the switch is OFF (open).
1	SW	The function of this bit is reserved for future use. This read only bit is selected by a switch. SW is asserted when the switch is OFF (open).

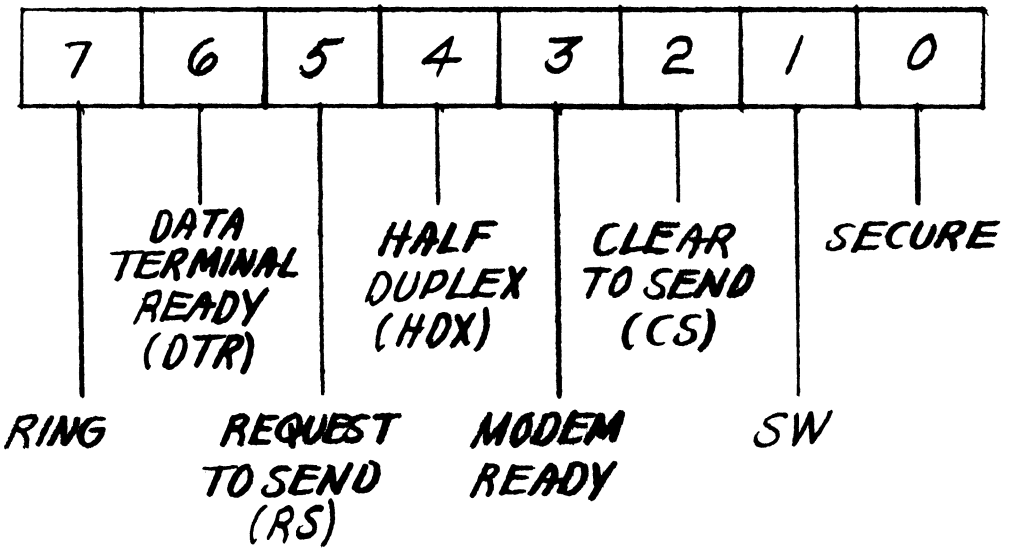


Figure 3-4 Modem Control Register Format

Bit	Name	Description
2	CS (Clear to Send)	The CS bit informs the microprocessor of the state of the modem Clear to Send line. This bit and MODEM RDY (bit 3) must be asserted simultaneously to generate SEND which is the transmitter enabling signal. This bit is read only.
3	MODEM RDY (Modem Ready)	The MODEM RDY bit informs the microprocessor of the state of the Modem Ready line. On the M8201 Line Unit, this signal can be held asserted permanently through the use of a jumper. On the M8202 Line Unit, this signal is asserted when power is turned on. This bit is read only.
4	HDX (Half Duplex)	The HDX bit is used to put the line unit in the half-duplex mode. When this bit and the Request to Send bit are asserted, the receiver clock is inhibited which blinds the receiver during operation in the half-duplex mode. This bit is program read/write and can be directly cleared by the clear signal from the microprocessor.
5	RS (Request to Send)	The RS bit informs the microprocessor of the state of the modem Request to Send line. This bit is controlled by the line unit logic and not by the microprocessor. It is cleared by absence of data or by the initialization logic. This bit is read only.

Bit	Name	Description
6	DTR (Data Terminal Ready)	The DTR bit enables the modem via the Data Terminal Ready line. This bit is program read/write. It is directly set by the initialization logic but it can be cleared only by writing a 0 into it.
7	RING	The RING bit informs the microprocessor of the state of the modem Ring line. RING is inhibited on the M8202 Line Unit. This bit is read only.

3.3.5 Sync Register

The Sync Register is an 8-bit program read/write register.

DDCMP Mode: The register is loaded with a program selectable sync character.

SDLC Mode: In the secondary mode, this register is loaded with secondary station address. This 8 bit character follows the initial flag in the SDLC message format.

3.3.6 Switch Selectable Registers (R15 and R16)

Both of these registers are DIPs containing eight switches each. The program determines the function of both registers.

3.3.7 Maintenance Register (Figure 3-5)

Bit	Name	Description
0	MODE	The MODE bit selects the protocol (DDCMP or SDLC families). When set, DDCMP is selected; when cleared, SDLC is selected. During initialization, the CLEAR signal from the microprocessor sets this bit to

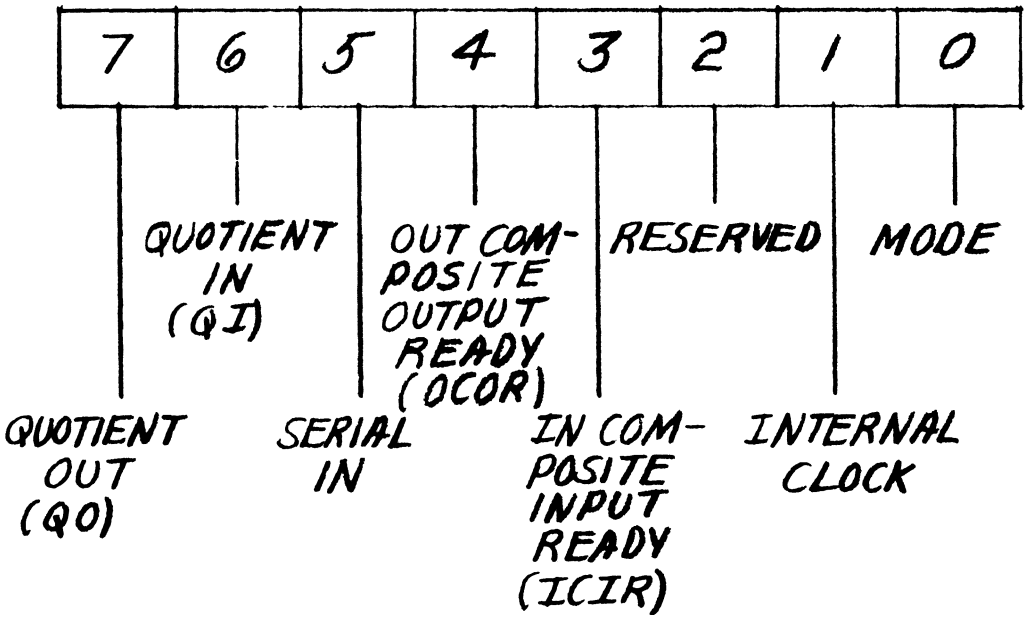


Figure 3-5 Maintenance Register Format

Bit	Name	Description
		select DDCMP. This bit can be cleared (SDLC selected) only by writing a 0 into it. This bit is read/write.
1	ECS (Internal Clock)	ECS is the output of the internal RC clock (approximately 10 KHz). This bit is read only.
2	Reserved	Read only.
3	ICIR (In Composite Input Ready)	When asserted, this bit indicates that the In Data Silo is ready to accept data. This bit is read only.
4	OCOR (Out Composite Output Ready)	When asserted, this bit indicates that data is ready at the output of the Out Data Silo. This bit is read only.
5	SI (Serial Input)	SI is the serial input data from the modem. This bit is read only.
6	QI (Quotient In)	QI is the least significant bit of the Receiver CRC Register. This bit is read only.
7	QO (Quotient Out)	QO is the least significant bit of the Transmitter CRC Register. This bit is read only.

3.4 PROGRAMMING PROCEDURES

The following programming procedures must be used to ensure proper operation of the line unit.

1. Transmit Start of Message (TSOM) and Transmit End of Message (TEOM) are bits 0 and 1 of the Out Control Register. TSOM and TEOM are loaded into this register by the microprocessor. These bits are sent from the Out Control Register to the Transmitter Buffer when the microprocessor loads a character (sync, data, etc.) into the Out Data Silo Register. If set, the control bit (TSOM or TEOM) goes along with the character. However, the Load signal for the Out Data Silo also clocks the TSIP flip-flop which clears the TSOM and TEOM bits in the Out Control Register.

   Therefore, always load the TSOM or TEOM bit into the Out Control Register before loading the Out Data Silo. The control information is cleared from this register automatically as the Out Data Silo accepts the data.

2. In the SDLC mode, the data written into the Out Data Silo with either TSOM or TEOM is lost. This is an internal function that is performed automatically by the transmitter control logic. Physically, this is accomplished by inhibiting the loading of the Transmitter Data Shift Register.

   In place of the shift register output, the transmitter control logic transmits a flag character when TSOM is set and it sends the transmitter CRC check character when TEOM is set. If both TEOM and TSOM are set, 16 zeroes are sent.

3. BCC MATCH and BLOCK END are bits 0 and 1 of the In Control Register. Physically, they are part of the 3341 FIFOs that constitute the In Data Silo. When the 8 data bits of the In Data Silo are read by the microprocessor, BCC MATCH and BLOCK END are lost. These bits are read as part of the In Control Register.

   Therefore, always read the In Control Register before reading the In Data Silo.

4. In the DDCMP mode, the BCC MATCH flag is presented with the CRC check character that produced the match information.

   In the Bit Stuff mode, the BLOCK END bit is asserted when the terminating flag has been received. This bit is loaded with the high byte of the CRC Check Character. Therefore, the BCC MATCH bit along with the BLOCK END bit should be used to indicate reception of an errorless message.

CHAPTER 4

DETAILED DESCRIPTION

4.1 INTRODUCTION

This chapter providse a two level discussion of the DMC11 line unit. A functional description is presented first. It discusses the line unit logic in major functional groups at the block diagram level (Figure 4-1). The second level of discussion is the detailed description that covers the complete line unit logic at the circuit schematic level as shown in the line unit print set.

NOTE

There are two versions of the line unit. The M8202 high speed line unit is intended for local network applications and contains an integral modem that operates at 1M bps or 56K bps. The M8201 low speed line unit is intended for remote network applications. It has no integral modem. The M8201 contains level conversion logic to interface with EIA RS232C/CCITT V24 compatible modems at speeds up to 19.2K bps or CCITT V35 modems at speeds up to 56K bps.

The DMC11 line unit is not a stand-alone device. It must be used with a DMC11 microprocessor. A separate manual (EK-DMCUP-MM-001) covers the microprocessor.

The first M8200 microprocessors to be shipped

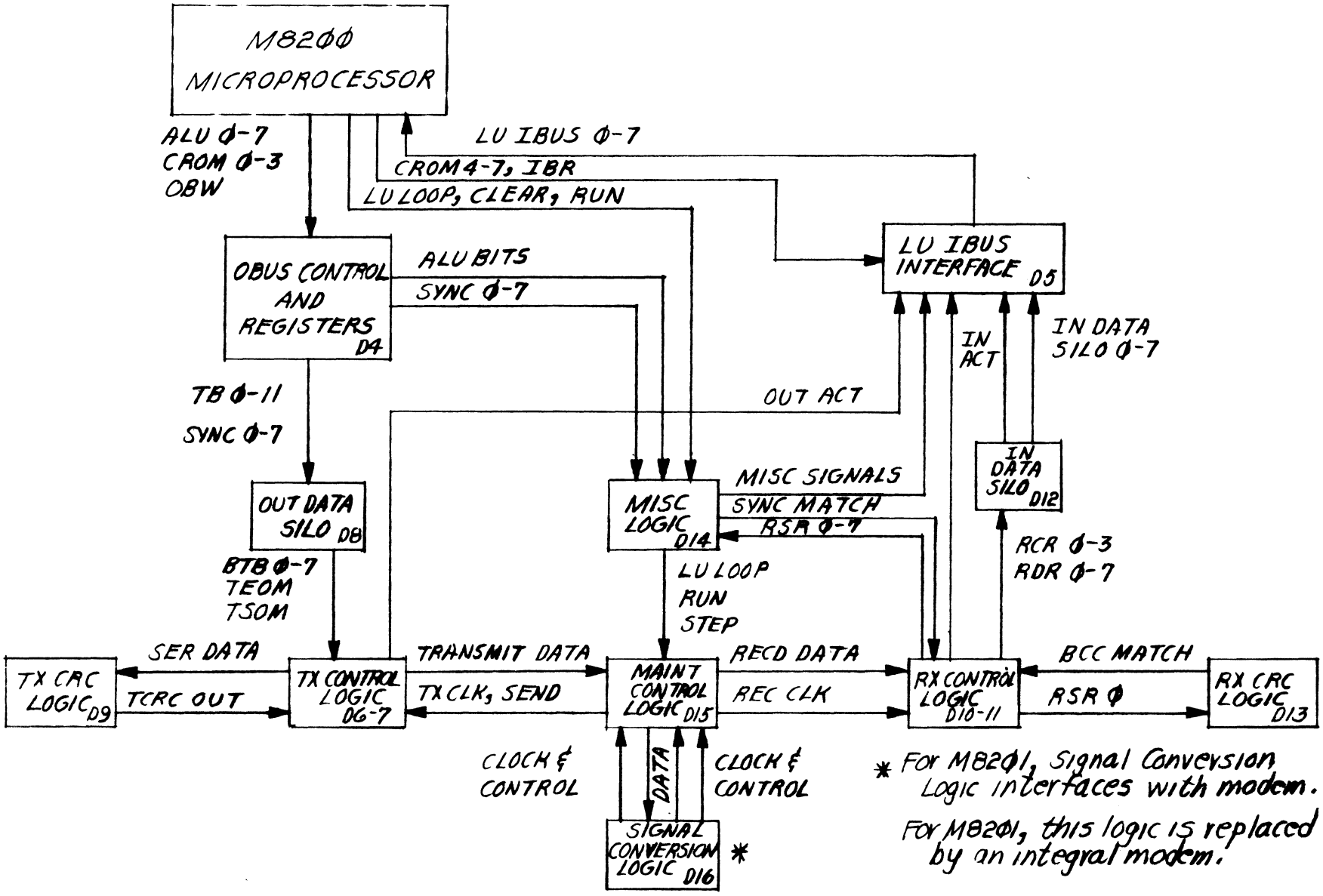


Figure 4-1 Line Unit Simplified Block Diagram

have their ROMs configured to operate with the DDCMP protocol. A subsequent version will have ROMs configured to operate with the SDLC protocol. The M8201 and M8202 line units can operate with both protocols.

4.2 FUNCTIONAL DESCRIPTION

4.2.1 Logic Description

For the functional discussion, the line unit logic is divided into 10 major sections as shown below.

Title	Para. No.
Registers	4.2.1.1
Out Control Logic	4.2.1.2
In Control Logic	4.2.1.3
Transmitter Control Logic	4.2.1.4
Receiver Control Logic	4.2.1.5
CRC Logic	4.2.1.6
*Data Set Interface Logic	4.2.1.7
Maintenance Logic	4.2.1.8
Initialization Logic	4.2.1.9
**Integral Modem	4.2.1.10

*M8201 only

**M8202 only

4.2.1.1 Registers

The eight line unit registers are discussed below. They are all 8 bit registers.

In Data Silo Register

The In Data Silo is loaded with 8 bits of received data from the Receiver Data Register. When the microprocessor performs a read operation on this register, the data is presented to the IBUS. This register uses address 10 (octal) and is read only.

Out Data Silo Register

The Out Data Silo is loaded with 8 bits of data to be transmitted and sends it to the Transmitter Shift register. This register uses address 10 (octal) and is write only.

Out Control Register

This register contains the control and status information pertaining to transmitter operation. It controls the start and end of a message and indicates the status of the Out Data Silo.

In Control Register

This register contains the control and status information pertaining to receiver operation. It also contains the receiver CRC error bit and a bit that controls looping of the receiver on the transmitter during maintenance.

Modem Control Register

This register contains the status information pertaining to the modem control/status lines.

Sync Register

The Sync Register is read/write and is loaded with a program selectable sync character in the DDCMP mode. It is loaded with the secondary station address during secondary station operation in the Bit Stuff mode.

Switch Selectable Registers R15 and R16.

These registers are DIPs containing eight switches each. The program determines the function of both registers.

Maintenance Register

This register contains status information of use during the maintenance mode. It monitors to output of the internal RC clock and serial data from the modem. It also contains the bit that controls the choice of protocol.

4.2.1.2 Out Control Logic - The out control logic interfaces with the microprocessor output bus (OBUS) which is used by the microprocessor to send information to the line unit. The out control logic consists of the Out Data Silo, Sync Register, four bits of the Out Control Register and the register decoder.

If the information from the microprocessor is part of a message to be transmitted, it is temporarily stored in the Transmitter Data Buffer. If the information is the line unit secondary station address (Bit Stuff protocol) or the sync character (DDCMP protocol), it is stored in the Sync Register.

4.2.1.3 In Control Logic - The in control logic interfaces with the microprocessor input bus (IBUS) which is used by the microprocessor to obtain information from the line unit. All eight registers in the line unit can be read by the microprocessor. Eight 8-input multiplexers are used to perform this function.

4.2.1.4 Transmitter Control Logic

The transmitter control logic controls the transmission of 8 bit characters with no restrictions on message length or format imposed by the line unit. The network protocol determines the message format. The logic consists of seven functional units that are described below.

ROMs and ROM Sync Buffer

Three read-only memories (ROMs) are the major controlling elements for the transmitter.

The Function Decode ROM (FDR) decodes the microprocessor inputs and controls the setting of TX DONE. This information along with the current state of the logic determines the next event on a character basis.

Six control signals, including three from the FDR, are stored in the ROM Sync Buffer. After the flag or sync characters have been sent, the buffer is clocked only at the end of a character. This allows the logic to set up for the next character during the present

character while not affecting the outputs of the buffer.

The [redacted] Control ROM (DPCR) formats the Bit Stuff control characters and controls transmitter data path multiplexing.

The [redacted] ROM (DDR) multiplexes the data received from the TX shift register, TX CRC register and DPCR. It also controls the timing of transfers from the Out Data Silo to the TX shift register.

Clock Logic

In the user mode, the transmitter clock logic uses the modem transmitter clock to derive a group of clock signals for the transmitter control logic. Separate maintenance logic allows the modem transmitter clock to be replaced by the internal RC clock or the single-stepped clock.

TD Flip-Flop and 1s Counter

The serialized information that is to be transmitted comes from the output of the DDR and is loaded into the TD flip-flop. The output of this flip-flop goes to the TDS flip-flop to be synchronized with the modem transmitter clock. The output of the TDS flip-flop is converted to EIA logic levels and then on to the modem. The output of the TD flip-flop is also sent to the 1s Counter.

The 1s Counter keeps track of the number of consecutive 1s transmitted. In the Bit Stuff mode, this information is used to make protocol decisions when transmitting control characters and to maintain data transparency. Two outputs of the counter are fed back to the DPCR as decision making signals. Counting consecutive

1s allows the transmitter control logic to decide whether a character is an abort character, flag character or five consecutive 1s in the data stream. When five consecutive 1s appear in the data stream, the logic stuffs a 0 as the next bit to prevent the sending of a flag configuration (01111110) in the data stream. The receiving station automatically removes the stuffed 0s.

TCSC Counter

The TCSC counter counts the number of bits in each data character that is transmitted, exclusive of stuffed 0s. It also counts the number of bits in a control character. It counts to 16 for a CRC character and to 8 for all others. At the last bit of a character, it generates pulse TCSC MAX H that synchronizes the current action of the transmitter data path to the microprocessor.

SACT, DONE and DATA LATE Flip-Flops

The SACT flip-flop informs the microprocessor of the status of the transmitter. When it is set, the transmitter is active.

The transmitter logic sets the DONE flip-flop to ensure continuous data. It sets it when a character has been loaded into the Transmitter Shift register when SACT is set, or when the transmitter is cleared.

During transmission, if DONE is still set at the end of the current character, the hardware sets the DATA LATE flip-flop. This indicates that the Out Data Silo had not been loaded with the next character in time for it to propagate through the silo.

Shift Register

The shift register is loaded in parallel from the Out Data Silo with the information (8 bit character) to be transmitted. This includes data, Bit Stuff control characters and DDCMP sync characters. The register serializes the character starting with the LSB. The serial data (TX SER OUT) from the shift register goes to the Data Decode ROM and CRC logic.

4.2.1.5 Receiver Control Logic - The receiver logic controls the reception of 8 bit characters in accordance with the network protocol. The logic consists of six functional units that are described below.

ROMs and RCS Flip-Flop

Two read-only memories (ROMs) are the major controlling elements for the receiver.

The Decode ROM decodes the protocol selected, recognizes sync characters, flag characters, and stuffed 0s. It controls the enabling of the Receiver Shift Register clock.

The Function ROM interprets the state of the receiver and controls the timing for loading characters in the Receiver Buffer Register.

The Receiver Control Synchronization (RCS) flip-flop stores three signals from the Function ROM and synchronizes them with the modem receiver clock. One signal, IN ACTIVE, is fed back and is stored as DELAYED ACTIVE.

Clock Logic

In the user mode, the receiver clock logic uses the modem receiver clock to derive a group of clock signals for the receiver control logic. Separate maintenance logic allows the modem receiver clock to be replaced by the internal RC clock or the single-stepped clock.

1s Counter and Enabling Logic

The 1s Counter (R1BC) is enabled by the CFF flip-flop. This flip-flop looks at the received data before it is shifted into the 1s Counter. During Bit Stuff protocol operation, the switch from the idle state to the active state must start with a 0 to signal the first bit of the Bit Stuff flag character (01111110). The [redacted] enables the 1s Counter only if this action occurs. This action locks the CFF flip-flop in the set state where it remains until it is directly cleared only when the receiver is cleared. [redacted] flip-flop is set.

The 1s Counter counts consecutive 1s and is cleared when a received 0 is detected. The state of some of its outputs are used as inputs to the Decode ROM to recognize a flag character (six consecutive 1s), an abort character (eight consecutive 1s), or a stuffed 0 (five consecutive 1s). This counter provides no function during DDCMP protocol operation.

Shift Register Counter

The Receiver Shift Register Counter (RSRC) counts the number of bits in a character, exclusive of stuffed 0s (Bit Stuff mode). At the last bit, it generates signal RSRC MAX H that goes to the Function ROM as a control input to indicate that the In Data Silo should be loaded with a character.

Shift Register and Data Buffer

Physically, the Shift Register consists of two separate but interrelated registers. Received serial data is sent to the first register and its 8-bit parallel output is sent to the ADDRS + SYNC comparator to check for a sync character (DDCMP protocol) or the line unit secondary address (SDLC protocol).

The same serial data is sent from the LSB of the first register to the second one which is called the Extended Receiver Shift Register. The 8-bit parallel output of the extended register is sent to the Receiver Data Buffer. From this buffer, the data goes to the In Data Silo and on to the microprocessor.

In Data Silo

The In Data Silo is loaded with received data from the Receiver Data Buffer and presents this data to the IBUS where it is read by the microprocessor. Because this register is constructed with 3341 FIFOs, its inputs and outputs are completely independent.

4.2.1.6 CRC Logic - The CRC logic is the circuit implementation of the cyclic redundancy checking method of encoding and decoding messages for error detection. It consists of a Transmitter CRC

Register, Receiver CRC Register, and error detection logic that is associated with the Receiver CRC Register. The Bit Stuff mode uses a modified CCITT code and the DDCMP mode uses code CRC-16. Both codes generate 16 bit CRC check characters.

In a typical operation, the sending station's transmitter CRC register looks at the information being transmitted and accumulates a CRC check character. This character is transmitted at the end of the message. The receiving stations receiver CRC register looks at the received message plus the CRC check character. At this point, the contents of the receiver CRC register determine if the message has been received without an error. For the DDCMP mode, the register must read 0. For the Bit Stuff mode, the register must read 016417. If the message is errorless, a flag (BCC STATE) is asserted by the error detection logic.

This logic only indicates that the message is or is not in error. It does not detect or correct specific errors. If the message is in error, as indicated by non-assertion of the flag, the protocol requests retransmission of the message.

4.2.1.7 Data Set Interface Logic

The data set interface logic is used only with the low speed line unit (M8201). It allows program control of the initiation of communications with the modem and allows monitoring of status signals from the modem. It also provides logic level conversion for all signals between the line unit and the modem. The data set uses EIA logic levels and the line unit uses TTL logic levels.

This logic supports two different interfaces. One is EIA/CCITT V24 which uses single ended signals. The other is CCITT V35 which uses double ended or differential signals.

Maintenance Logic

The maintenance logic consists of an RC clock and two multiplexers to select the proper source for data, clock, and control signals during servicing of the line unit.

Although not part of the maintenance logic, the outputs of the Request to Send (RS) and Half Duplex (HDX) flip-flops are used to inhibit the receiver clock when the half-duplex mode of operation is selected.

Initialization Logic

The initialization logic is used to clear the receiver section and the transmitter section separately or simultaneously. This logic is controlled by the microprocessor.

4.2.2 Major Operating Features

4.2.2.1 Introduction - This paragraph discusses the major operating features of the line unit at the functional level. The discussion is divided into three sections as shown below.

Title	Para. No.
Modem Control	4.2.2.2
Transmitter Section	4.2.2.3
Receiver Section	4.2.2.4

4.2.2.2 Modem Control - This paragraph applies to the low speed line unit (M8201) that is used for remote network applications using Bell 208, 209, or equivalent modems.

The modem control and status lines are monitored by the microprocessor. Only Data Terminal Ready (DTR) can be controlled. All others are automatically controlled by the line unit.

In some systems, handshaking is not necessary. The transmitter is simply enabled and transmission starts when the TSOM bit is detected by the transmitter. The receiver starts searching for synchronization without first having received a Ring indication.

The flow of data is interlocked with signals received from the modem. When modem control is being used in a system, the microprocessor must monitor the control signals from the modem.

All clock signals used in conjunction with data received from or transmitted to the modem must emanate from the modem and be in accordance with EIA RS334. No external clock to the modem is supplied by the line unit.

4.2.2.3 Transmitter Section - The transmitter section performs the following functions.

1. Buffers and serializes data to be transmitted.
2. Generates CRC check characters.
3. Creates transparent data stream.
4. Transmits flag, sync and abort/PAD characters.

This discussion includes basic functional descriptions of transmitter operation in the DDCMP and SDLC modes. A related flowchart is shown in sheet 2 of the circuit schematic print set.

Transmitter Operation In DDCMP Mode

1. The microprocessor loads the selected sync character into the Out Data Silo. It then loads the Start of Message (SOM) bit in the Out Control Register. The SOM bit goes from the Out Control Register to the Out Data Silo.

2. The sync character and SOM bit are propagated through the Out Data Silo. The Out Composite Output Ready (OCOR) bit is asserted to indicate that data (the sync character in this case) and the control bits (the SOM bit in this case) are ready at the output of the Out Data Silo.

3. If both SOM and EOM are asserted simultaneously, the transmitter sends 16 zeros. If the SOM bit is not set but the End of Message (EOM) bit is set, the line unit hangs up.

4. With SOM and OCOR asserted, the transmitter logic causes Request to Send (RS) to be asserted in the modem control logic.

5. The line unit waits for the Clear to Send (CS) and Modem Ready (MR) signals to be turned on by the modem. With both of these signals ON, the line unit asserts SEND. This is the enabling signal for the transmitter.

6. As long as the SOM bit is set, the transmit CRC function is inhibited (transmit CRC register is cleared). The transmitted data is not included in the CRC computation.

7. If SOM is not set with a character loaded into the Out Data Silo, the CRC accumulation starts. If the NO CRC switch is OFF, the CRC function is selected and all subsequent data characters are included in the transmit CRC accumulation.

8. During transmission, if DONE is still asserted at the end of the current character, DATA LATE is asserted which indicates that the Out Data Silo has not been loaded with the next character. This results in the Request to Send line being turned off after 1s have been transmitted for one character time and the line unit reverts to the Idle state (transmits MARKs).

9. The normal ending sequence is initiated when the microprocessor sets the End of Message (EOM) bit. The EOM bit and a meaningless character are loaded into the Out Data Silo. This causes the 16 bit CRC character to be transmitted and the last character to be ignored.

10. If the assertion of EOM is not followed by the assertion of SOM and the loading of another character, the line unit goes to the Idle state. The transmitter is shut down by the clearing of Out Active and RS. SEND is cleared when the modem drops Clear to Send (CS).

    If the assertion of EOM is followed by the assertion of SOM, the transmitter remains active.

Transmitter Operation In Bit Stuff Mode

1. The microprocessor loads the Start of Message (SOM) bit into the Out Control register. It then loads a null character into the Out Data Silo.

2. The null character and SOM bit are propagated through the Out Data Silo. The Out Composite Output Ready (OCOR) bit is asserted to indicate that data is ready at the output of the Out Data Silo.

3. If the SOM bit is not set but the End of Message (EOM) bit is set, the line unit hangs up. If both SOM and EOM are asserted simultaneously, the transmitter sends 16 zeros.

4. With SOM and OCOR asserted, the transmitter logic causes Request to Send (RS) to be asserted in the modem control logic.

5. The line unit waits for the Clear to Send (CS) and Modem Ready (MR) signals to be turned on by the modem. With both of these signals ON, the line unit asserts SEND. This is the enabling signal for the transmitter.

6. As long as the SOM bit is set, the transmit CRC function is inhibited (transmit CRC register is cleared).

7. For each SOM loaded into the silo, one flag character (01111110) is transmitted. When the microprocessor loads a character without SOM, that character is data. If the NO CRC switch is OFF, the CRC function is selected and all data characters are included in the transmit CRC accumulation.

8. Zero stuffing is performed on all characters except the flags and aborts. Zero stuffing consists of inserting a 0 following five consecutive 1s to preserve the identity of the flag and abort characters.

9. During transmission, if DONE is still asserted at the end of the current character, DATA LATE is asserted which indicates that the Out Data Silo has not been loaded with the next character. This results in the Request to Send line being turned off after transmitting an Abort character (seven or more 1s) and the line unit reverts to the Idle state (transmits MARKs).

10. The normal ending sequence is initiated when the microprocessor sets the End of Message (EOM) bit twice. The EOM bit and a meaningless character are loaded into the Out Data Silo twice. This causes the 16 bit CRC character to be transmitted followed by the terminating flag character.

11. When the terminating flag has been transmitted, the Out Active bit is cleared (transmitter deactivated) provided another message is not pending. If another message is pending, the first data character is transmitted following the terminating flag of the previous message. If the SOM bit is asserted following the double assertion of EOM, a second flag is transmitted.

Transmitter CRC Character Generation

The NO CRC switch must be off to enable the CRC logic. Two cyclic redundancy checking (CRC) codes are used. The DDCMP family protocols use code CRC-16 and the Bit Stuff type family protocols use code CCITT.

With the CRC function enabled, the transmitter CRC register looks at all data to be transmitted and accumulates a CRC check character. This 16 bit character is transmitted at the end of the message. In the SDLC mode, stuffed 0s are not included in the calculation of the CRC check character.

In the DDCMP mode, the transmitter CRC register reads all 0s when initialized (cleared). The register is cleared right after the CRC check character has been transmitted. This is necessary because the next character may be part of a sequence that requires computation of another CRC character.

In the Bit Stuff mode, the transmitter CRC register reads all 1s when initialized. This allows detection of the addition or deletion of 0s at the leading end of the message due to erroneous flag characters. The CRC check character is complemented before being transmitted. This allows detection of the erroneous addition or deletion of 0s at the trailing edge of the message. As in the DDCMP mode, the register is cleared right after the CRC check character has been transmitted.

4.2.2.4 Receiver Section - The receiver section performs the following functions.

1. Buffers and converts received serial data to parallel data.

2. Interprets transparent data stream in SDLC mode (removes stuffed 0s).

3. Recognizes flag and abort sequences.

4. Recognizes secondary station address (SDLC mode) and SYNC characters (DDCMP mode).

5. Detects CRC errors.

This discussion includes basic functional descriptions of receiver operation in the DDCMP and SDLC modes. A related flow chart is shown in sheet 2 of the circuit schematic print set.

Receiver Operation In DDCMP Mode

1. The microprocessor loads the network sync character into the Sync Register. The output of this register goes to one branch of the ADRS+SYNC comparator. The other branch of the comparator comes from the output of the Receiver Data Register. The comparator looks at the output of the Receiver Data Register on a bit by bit basis searching for a sync character.

2. Reception of the first sync character causes FRAME to be asserted. If a second consecutive sync character is not received, FRAME is cleared and the search for sync characters starts over again. When at least two consecutive sync characters have been received, the

receiver logic is considered to be synchronized and MESG ACT is set. The first non-sync character received following MESG ACT being set is assembled as an 8-bit data character.

3. The IN ACTIVE bit is asserted by the receiver control logic. This informs the microprocessor that the receiver is in the data reception mode. When the first data character reaches the output of the In Data Silo, IN RDY is asserted which informs the microprocessor that received data is ready for processing.

4. The CRC function is enabled when IN ACTIVE is asserted, provided that the NO CRC switch is off. The receiver CRC register examines all data and the 16 bit CRC check character at which point the register reads 0 if the message contains no errors. The BCC MATCH flag is asserted if the register reads 0.

5. The microprocessor decides when the message ends, when the BCC MATCH flag is valid, and when the receiver should be cleared.

Receiver Operation In Bit Stuff Mode

1. In the Bit Stuff mode, the line unit can operate as a primary or secondary station. The primary and secondary modes are switch selectable.

   In the primary mode, all received messages are presented to the microprocessor. In the secondary mode, the only

messages that are presented to the microprocessor are those that are preceded by the line units' secondary address. This address is an 8 bit character that follows the initial flag character.

The secondary address is loaded into the Sync Register by the microprocessor. From the Sync Register, it goes to the ADRS+SYNC comparator which examines the received data in order to detect the line unit secondary address.

2. The receiver searches for the initial flag character. In the primary mode, IN ACTIVE is asserted upon reception of the first data character. In the secondary mode, the line units secondary address must be received before IN ACTIVE is asserted.

   In the primary mode, all data subsequent to the flag character is presented to the microprocessor. In the secondary mode, all data subsequent to the secondary address is presented to the microprocessor.

3. The assertion of IN ACTIVE informs the microprocessor that the receiver is in the data reception mode. When the first data character reaches the output of the In Data Silo, IN RDY is asserted which informs the microprocessor that received data is ready for processing.

4. During data reception, the receiver automatically removes all stuffed 0s.

5. The assertion of IN ACTIVE enables the CRC function, provided that the NO CRC switch is off. The receiver CRC register examines all data and the 16 bit CRC check character at which time the register reads 016417 if the message contains no errors. In this case, the BCC MATCH bit is asserted.

   BLOCK END is asserted when the terminating flag is received and is loaded with the high byte of the CRC check character. Thus, the microprocessor should look for the simultaneous assertion of BLOCK END and BCC MATCH to indicate reception of an errorless message. The receiver is automatically cleared by BLOCK END.

Receiver CRC Character Checking

As in the case of the transmitter, the NO CRC switch must be off to enable the receiver CRC logic. The same cyclic redundancy checking (CRC) codes are used: code CRC-16 for the DDCMP family protocols and code CCITT for the SDLC family protocols.

The receiver CRC register examines all data and the 16 bit CRC character. In the SDLC mode, this includes all information between

the initial and terminating flags and excludes intermessage flags and stuffed 0s.

In the DDCMP mode, after reception of the CRC check character, the receiver CRC register reads 0 if the message contains no errors. In the SDLC mode, the register reads 016417 if the message contains no errors.

4.3 DETAILED DESCRIPTION

4.3.1 Introduction

The detailed description is divided into 10 major sections as shown below.

Description	Para. No.
Registers	4.3.2
Out Control Logic	4.3.3
In Control Logic	4.3.4
Transmitter Control Logic	4.3.5
Receiver Control Logic	4.3.6
CRC Logic	4.3.7
*Data Set Interface Logic	4.3.8
Maintenance Logic	4.3.9
Initialization Logic	4.3.10
**Integral Modem	4.3.11

*M8201 only

**M8202 only

The discussion is keyed to the circuit schematics in the print set. Supplementary illustrations are included in the text.

4.3.2 Registers

The line unit contains nine registers and they are discussed in the order shown below.

Register	Para. No.
In Data Silo Register	4.3.2.1
Out Data Silo Register	4.3.2.2
Out Control Register	4.3.2.3
In Control Register	4.3.2.4
Modem Control Register	4.3.2.5
Sync Register	4.3.2.6
Reserved Registers (2)	4.3.2.7
Maintenance Register	4.3.2.8

This discussion primarily covers the logical implementation and functional operation of the registers. A description of each bit is contained in Chapter 3 DEVICE REGISTERS.

4.3.2.1 In Data Silo Register - The In Data Silo Register is loaded with received data from the Receiver Data buffer and presents this data to the IBUS where it is read by the microprocessor.

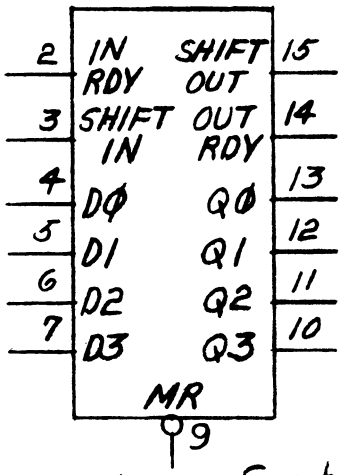
The received data is in the form of 8-bit characters. Physically, the silo contains 12 bits. The other four bits are part of the In Control Register and are discussed in Paragraph 4.3.2.4.

The In Data Silo is comprised of three 3341 64 word-by-4 bit propagatable registers called silos or FIFOs (first in/first out). At this point, the discussion digresses to explain the operation of the 3341 FIFO.

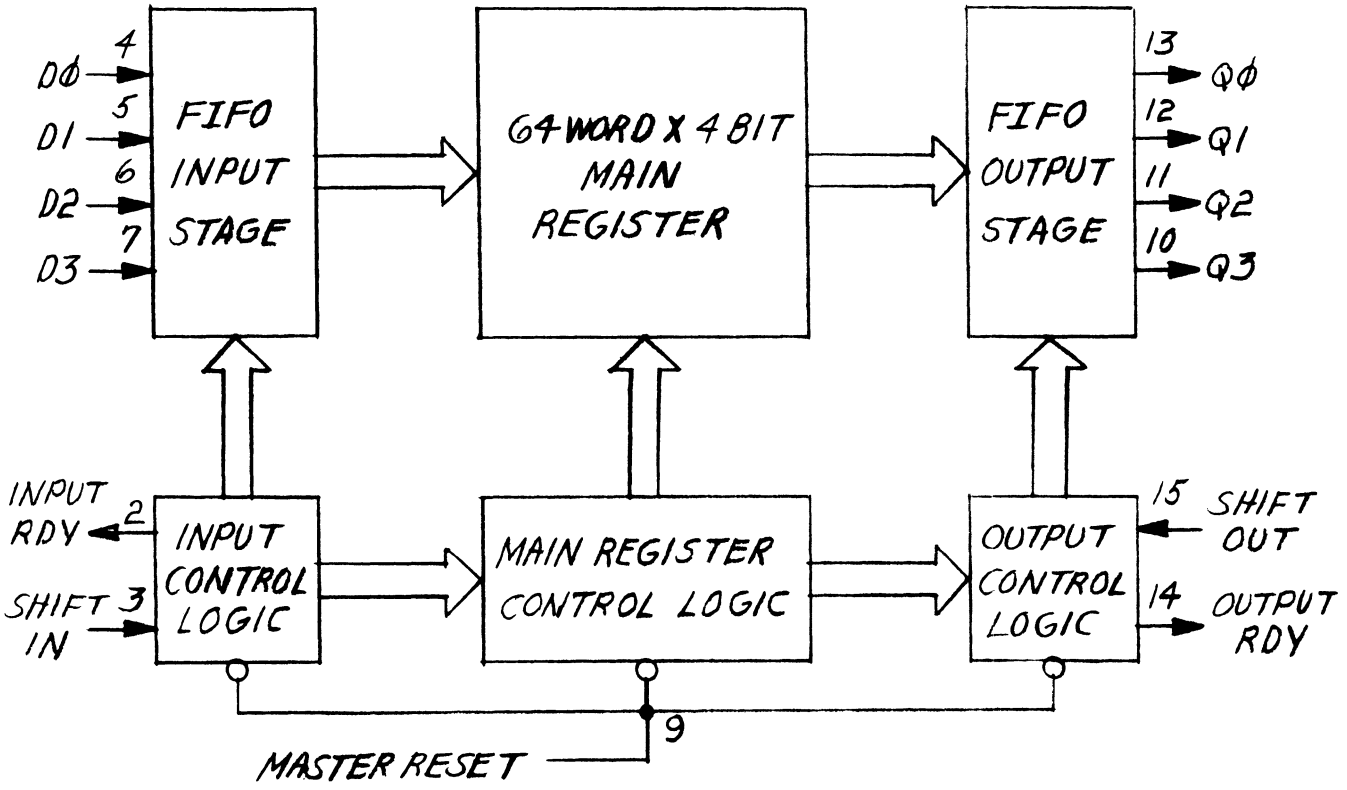
The logic symbol for the silo is shown in Figure 4-2. The inputs are D0-D3 and the outputs are Q0-Q3. There is no common clock so the inputs and outputs are completely independent. SHIFT IN is a control signal that is sent to the silo and INPUT READY is generated by the silo when space is available. When INPUT READY and SHIFT IN are high, the input is loaded into the top word position. INPUT READY goes low and when SHIFT IN goes low, the 4-bit word propagates to the second word position (if empty) and on to the bottom of the silo by internal control signals.

When data has reached the bottom of the silo, OUTPUT READY goes high to indicate the presence of valid data. When OUTPUT READY and SHIFT OUT are high, the bottom word is transferred out of the silo. This causes OUTPUT READY to go low but the word is maintained in the output stage until SHIFT OUT goes low also. At this point, the word in the adjacent position is transferred into the bottom position which causes OUTPUT READY to go high again but the data does not change. If the silo has been emptied, OUTPUT READY stays low.

In this application, three 3341s are connected to provide a register 64 words deep by 12 bits wide (Figure 4-3). Two devices (8 bits) represent the In Data Silo and one device (4 bits) represents bits 0-3 of the In Control register. The discussion now returns to the



Logic Symbol



Equivalent Logic Block Diagram

Figure 4-2 Logical Representation of 3341 FIFO

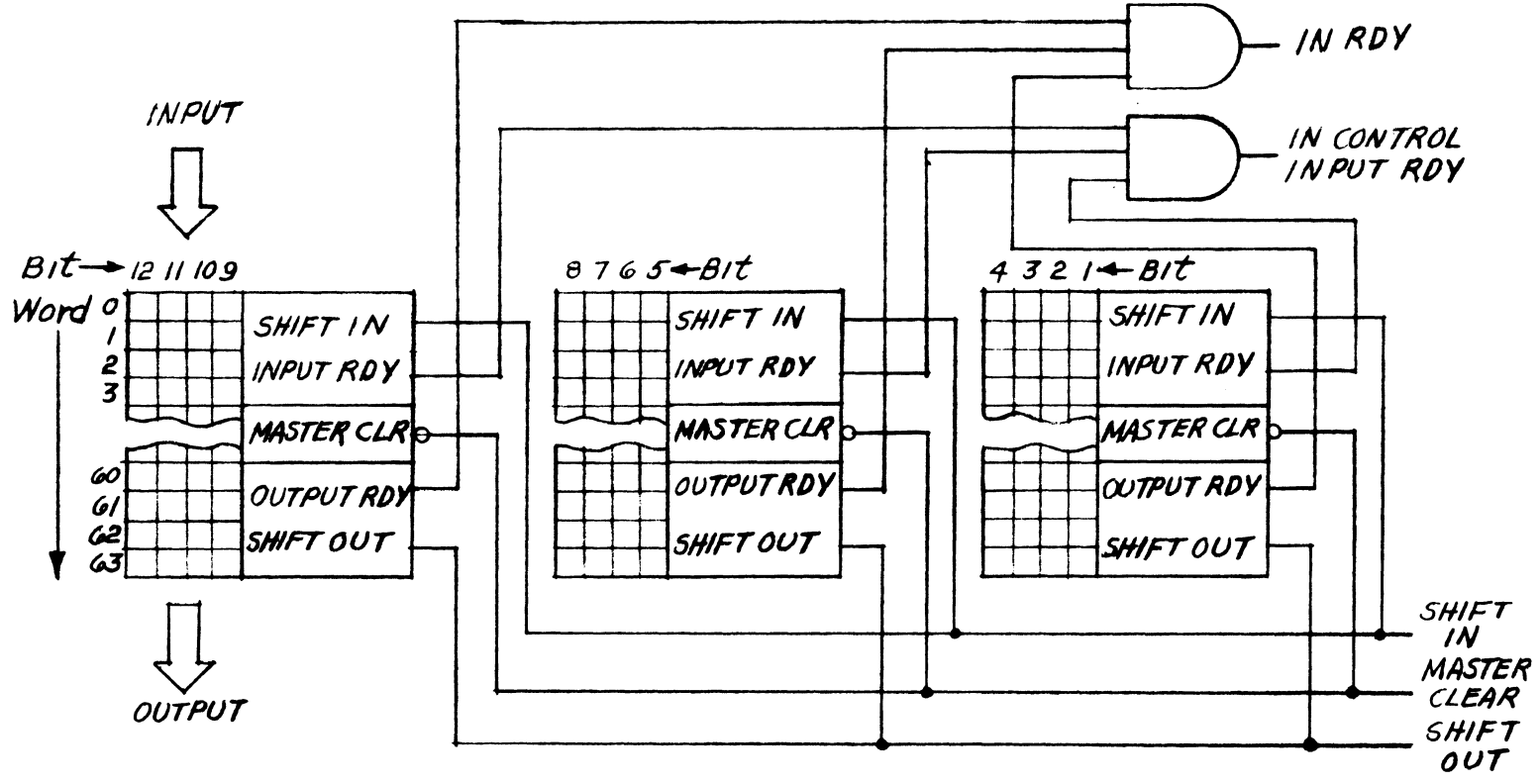


Figure 4-3 Architecture of In Data Silo

description of the In Data Silo and associated logic as shown in circuit schematic D12.

The Smith Super Silo is our name for this unique application of the 3341 FIFO.

The In Data Silo Register contains the 8 bits of received data that are to be read by the microprocessor. Physically, it is composed of three 3341 FIFOs to form a 12 bit register that is 64 words deep. The additional 4 bits are In Control Register bits 0-3. Although functionally separate, the In Data Silo and In Control Register bits 0-3 are loaded and shifted out together. (The In Control register is described in Paragraph 4.3.2.4.)

The inputs to the In Data Silo Register are D11 RDR 0 H - D11 RDR 7 H from the Receiver Data register. They represent the received data. The INPUT RDY outputs of the three FIFOs are ANDed to produce signal D12 ICIR H at a 74S11 3-input AND gate. This flag indicates that the silo is ready to accept an input. It is bit 3 of the Maintenance register. The SHIFT IN inputs of the three FIFOs are connected to D11 RSIP H (Receive Shift In Pulse) which is asserted by the receiver control logic when a received character has been assembled. The width of this pulse is dependent on the speed of the 3341 FIFO. The common SHIFT OUT signal comes from the 1 output of the RSO flip-flop. The D-input of this flip-flop is connected to +3 V so it is always set when clocked. The clock signal is D5 RDACP H (Receive Data Accepted Pulse) which is asserted when the In Data Silo has been read. This pulse is approximately 60 ns wide. The RSO flip-flop is clocked by the positive-going edge of this

negative pulse. The OUT RDY outputs of the three FIFOs are ANDed to produce signal D12 INRDY H at a 74S11 gate. This flag informs the microprocessor that received data is available at the silo output. It is bit 4 of the In Control register. Signal D12 INRDY H goes to the CLEAR input of the RSO flip-flop. When data is not ready at the silo output, D12 INRDY H is low which directly clears the RSO flip-flop and inhibits the shift out operation.

The MASTER RESET inputs of the three FIFOs are connected to D14 ICLRP L. When this signal goes low, the silo is cleared. D14 ICLRP L is controlled by the microprocessor to clear the receiver specifically or to clear it as part of the device reset function.

4.3.2.2 Out Data Silo Register - In this discussion, the Out Data Silo Register is considered to be an 8-bit register that accepts information to be transmitted and sends it to the Transmitter Shift register.

Physically, it is composed of three 3341 FIFOs to form a 12-bit register that is 64 words deep. The architecture and basic operation of the Out Data Silo is similar to the In Data Silo which is described in Paragraph 4.3.2.2.

Bits 8-11 of the Out Data Silo are associated with bits 0-3 of the Output Control register which are described in Paragraph 4.3.2.3.

The Out Data Silo and associated logic are shown in print D8. The inputs are D4 TB0 H-D4 TB7 H and they come from the microprocessor via a buffer. The outputs are D8 BTB0 H - D8 BTB7 H and go to the Transmitter Shift register. The 3341 inputs and outputs are completely independent because the FIFO has no common clock.

Some FIFO functions are controlled by the devices internal logic; hence, they are not evident from examining the logic print (D8).

A typical load/unload sequence is described in detail.

1. Initial Conditions

   It is assumed that the silo contains 62 characters; therefore, the top two positions (0 and 1) are empty. When space is available, the INPUT RDY output goes high as an internal FIFO function. There is data at the bottom of the silo so the OUTPUT RDY output goes high as an internal FIFO function.

   Assume that the TSIP flip-flop is cleared so the SHIFT IN input is low. Also assume that the TSOP flip-flop is cleared so the SHIFT OUT input is low.

   NOTE

   The silo is described as a functional unit with one set of inputs. Actually, it is composed of three FIFOs.

The silo has indicated that space is available for loading a character and valid data is available for unloading. In this discussion, a character is to be loaded first and then a character is to be unloaded.

2. Loading a Character

With the INPUT RDY output high, a character can be loaded by driving the SHIFT IN input high. The SHIFT IN input is connected to the 1 output of the TSIP flip-flop. When TSIP is set, SHIFT IN goes high. When it is desired to load the Out Data Silo, the microprocessor selects signal D4 R10 SEL L. This 60 ns negative pulse is sent to the clock input of the TSIP flip-flop. The positive-going trailing edge clocks TSIP and sets it because its D input is permanently connected to +3 V. SHIFT IN goes high and a character is loaded into the top of the silo.

After the character has been loaded, INPUT RDY goes low as an internal FIFO function. In turn, this drives D8 OUT RDY H low which directly clears the TSIP flip-flop via a 7408 2-input AND gate. This drives the SHIFT IN input low. Now, with both SHIFT IN and INPUT RDY low, the loaded character propagates to the second word position under the control of internal signals. The top position is empty, so INPUT RDY goes high again. If the character that was loaded had filled the silo, INPUT RDY would have remained low.

3. Unloading a Character

With the OUTPUT RDY output high, a character can be unloaded from the bottom of the silo by driving the SHIFT OUT input high. SHIFT OUT is connected to the 1 output of the TSOP flip-flop. When TSOP is set, SHIFT OUT goes high. At the end of a character, pulse D7 LOAD L is generated by the transmitter control logic. The positive-going trailing edge of this pulse clocks TSOP. This sets TSOP because its D input is permanently connected to +3 V. SHIFT OUT goes high and a character is unloaded from the silo. Now, OUTPUT RDY goes low as an internal FIFO function; however, the character is maintained in the bottom position until SHIFT OUT goes low also. When OUTPUT RDY goes low, D8 OCOR H goes low and directly clears the TSOP flip-flop. This drives the SHIFT OUT input low. At this point, the character in the adjacent position is transferred into the bottom position which causes OUTPUT RDY to go high again. This action is controlled by FIFO internal signals. If the character that was unloaded had emptied the silo, OUTPUT RDY would have remained low and the data would have remained at the silo output.

4.3.2.3 Output Control Register

Bits 0-3 (Print D8)

Bits 2 and 3 are reserved, but 0 is Transmit Start of Message (TSOM), and bit 1 is Transmit End of Message (TEOM). They are all write only bits. The logic required to generate these bits is shown in Figure 4-4.

Bits 0-3 are stored in a flip-flop register that is called the OUT CONT REG (print D4). The register inputs are connected to OBUS lines D3 BALU 0 L - D3 BALU 3 L from the microprocessor. The register outputs go to bits 8-11 of the Out Data Silo buffer (print ~~D4~~ D8).

This buffer and the OUT CONT REG are described in Paragraph 4.3.3 entitled Out Control Logic.

Buffer outputs D4 TB8 H - D4 TB 11 H go to the Out Data Silo (right 3341 on print D8). Reserved bits 2 and 3 are available at 3341 output pins 11 and 10, respectively.

Output pin 13 Siloed Transmit Start of Message (STSOM) goes to a 2-input NAND gate and is high when true. The other input of this gate goes high when the silo OUTPUT RDY signals are high. This drives the gate output low. This signal is inverted to assert D4 TSOM H which is used in the transmitter control logic.

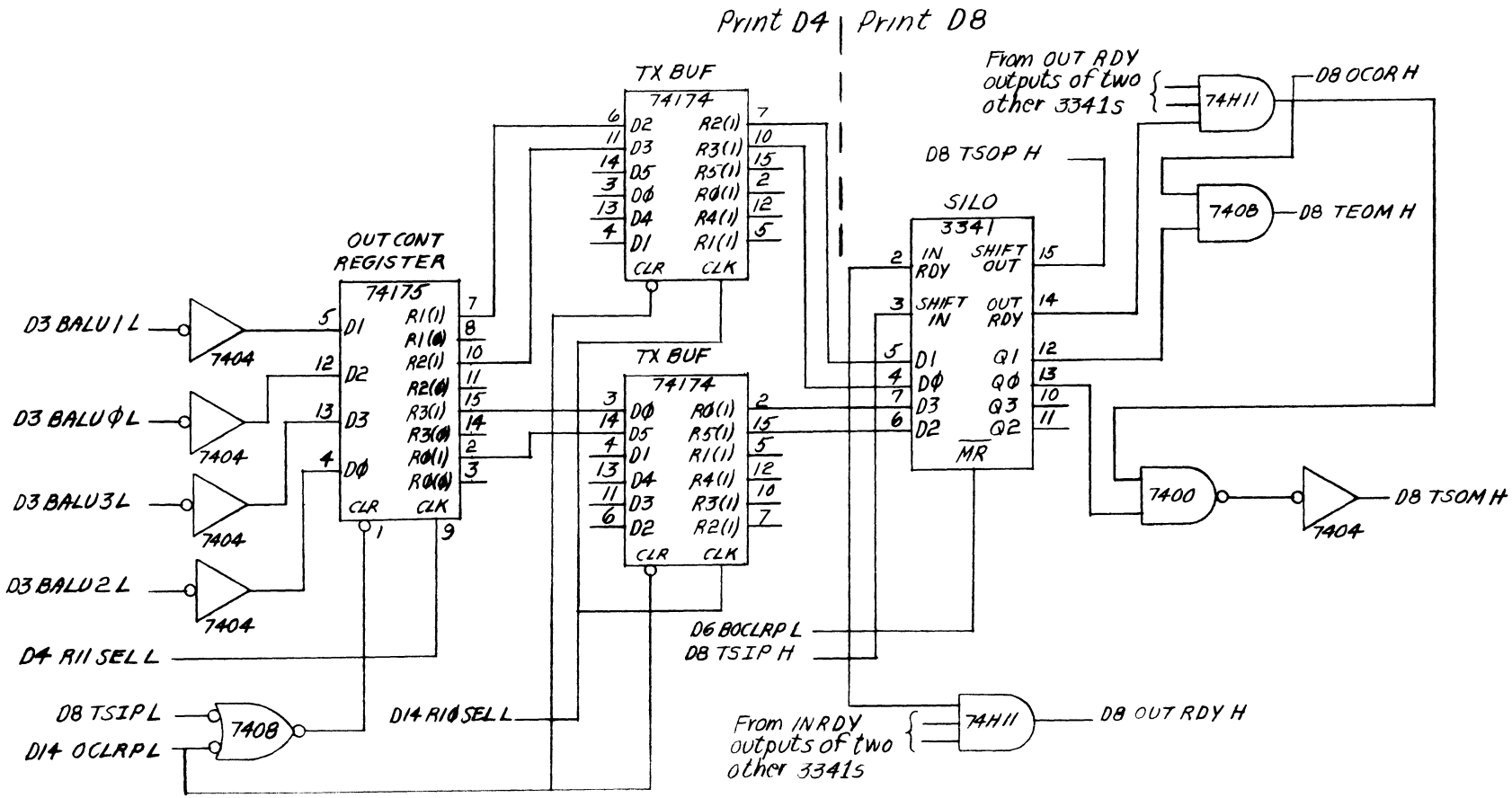


Figure 4-4 Logic for Output Control Register Bits 0-4

Output pin 12 Siloed Transmit End of Message (STEOM) goes to one input of 2-input AND gate and is high when true. The other input of this gate goes high when the three OUTPUT RDY signals are high. This drives the output high and asserts D8 TEOM H which is used in the transmitter control logic.

Bit 4 (Print D8)

Bit 4 is Out Ready (OUT RDY) and is read only. When asserted, it indicates to the microprocessor that space is available in the Out Data Silo. It is the AND function of the three INPUT RDY outputs from the Out Data Silo. This bit is identified as D8 OUT RDY H and is asserted at the output of a 74 H 11 AND gate when all three INPUT RDY signals are high (Figure 4-4).

Bit 5 (Reserved)

This read only bit is reserved for future use.

Bit 6 (print D6)

Bit 6 is OUT ACTIVE and is read only. It is generated at the 1 output of the SACT flip-flop which is controlled by the transmitter control logic. The D input of this flip-flop is connected to D6 SENTXAC H which comes from the ROM SYNC BUFF. This signal is the stored state of ENTXAC from the transmitter FUNCTION DECODE ROM. The SACT flip-flop is clocked by the traillng edge of D6 TX CLK L. This flip-flop is directly cleared by D6 BOCLR P L. This signal is derived from D14 OCLRP H which is bit 7 of the Out Control register.

Bit 7 (Print D14)

Bit 7 is Out Clear and is write only. The actual signals generated when this bit is written into are D14 OCLRP H and D14 OCLRP L. OCLRP stands for Out Clear Pulse. They are the complementary outputs of a 74123 1-shot. See Figure 4-5. A negative-going edge at the 1-shot triggers it and asserts D14 OCLRP H and D14 OCLRP $\overline{\text{H}}$ which are complementary 400 ns pulses. The triggering action occurs under two circumstances. In one case, the 1-shot is triggered when the microprocessor generates D3 CLEAR L to initiate a device clear operation. The other case is specific and triggering occurs when the microprocessor selects the Out Control register (D4 R11 SEL L goes low) and D4 ALU 7 L goes low. Signal D4 ALU 7 L is the double inversion of D3 BALU 7 L from the microprocessor.

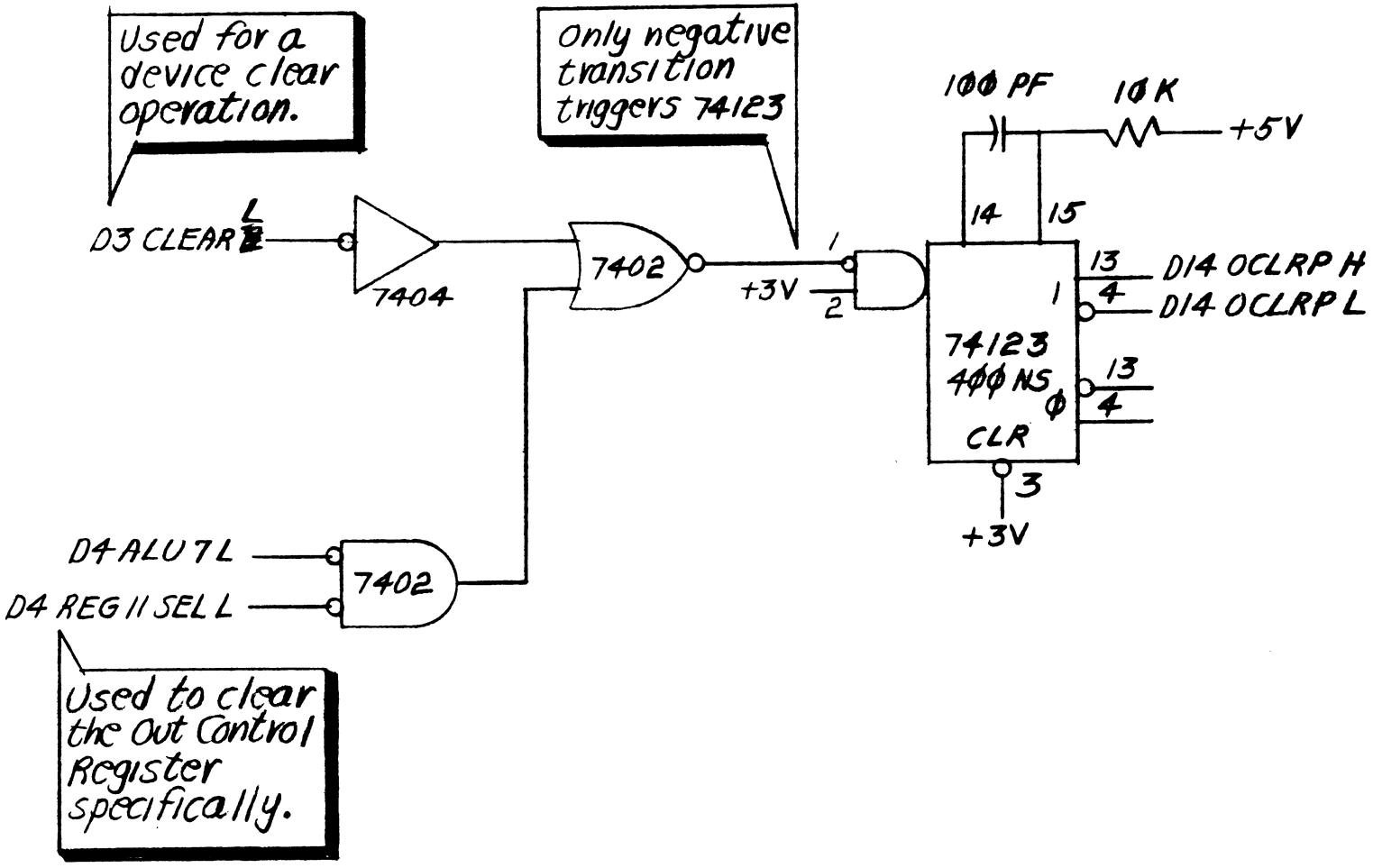


Figure 4-5 Logic for Output Control Register Bit 7

4.3.2.4 Input Control Register

Bits 0-3 (Print D12)

Bits 2 and 3 are reserved, bit 0 is Block Check Character Match (BCC MATCH), and bit 1 is IN BLOCK END. They are all read only bits.

These bits are picked off the output of the In Data Silo; specifically pins 10, 11, 12, and 13 of the left 3341 (print 12). The receiver control logic (prints D10 and D11) determines the state of bits 0 and 1. This logic is also shown in Figure 4-6.

Bit 0 (BCC MATCH) is asserted when the contents of the receiver BCC register equal zero in the DDCMP mode or 016417 in the Bit Stuff mode. The flag signal from the BCC logic is D13 BCC STATE H. It is clocked into the Receiver Data register (print D11) and on to the In Data Silo as D11 RCR 0 H. It comes out of the silo as D12 BCC MATCH H.

Bit 1 (IN BLOCK END) informs the microprocessor that a terminating flag character has been received. This function is useful only for the SDLC family of protocols. The state of this bit is determined by the receiver control logic (prints D10 and D11). In the SDLC primary mode, this bit is set when D10 FLG RECD H and D11 MESG ACT (1) H are both high. In the SDLC secondary mode, this bit is set when D10 FLG RECD H and D10 ADDRS+SYNC RECD H are both high. The bit is clocked into the Receiver Data register (print D11) by D11 REC DAT REG CLK H. This bit is also used to inform the microprocessor that an Abort signal has been received.

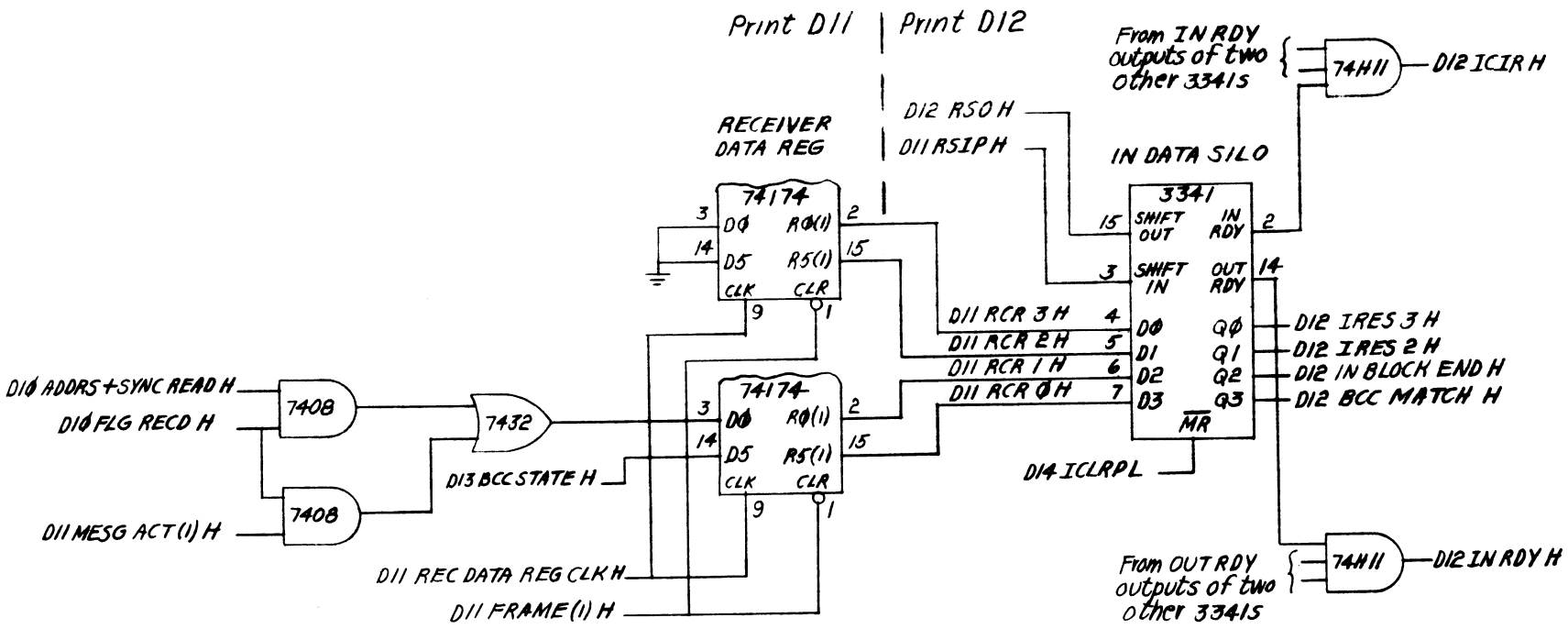


Figure 4-6 Logic for Input Control Register Bits 0-3

Bit 4 (Print D12)

Bit 4 is Input Ready (IN RDY) and is read only. When asserted, it indicates to the microprocessor that data is ready. It is the AND function of the three OUTPUT RDY signals from the In Data Silo. This bit is identified as D IN RDY H and is asserted at a 74S11 AND gate when all three OUTPUT RDY signals are high.

Bit 5 (Reserved)

This bit is reserved for future use. ? ALTERNATE LINE UNIT LOOP See D14

Bit 6 (Print D11)

Bit 6 is IN ACTIVE and is read only. This bit is identified as D11 IN ACTIVE (1) H and is stored in the Receiver Control Synchronization Buffer which is a 74175 quad D-type flip-flop. The input to this section of the flip-flop (pin 4) is D10 EN IN ACT H which is an output of the receiver control ROM.

Bit 7 (Print D14)

Bit 7 is In Clear (IN CLR) and is write only. It is used to control the receiver section of the line unit. When written into, this bit generates complementary 400 ns pulses from a 74123 1-shot. The pulses are identified as In Clear Pulses D14 ICLRP H and D14 ICLRP L (Figure 4-7) and are triggered by a negative-going pulse at 1-shot input pin 9. The triggering action occurs under two circumstances. In one case the 1-shot is triggered when the microprocessor generates D3 CLEAR L to indicate a device clear operation. The other case is specific and triggering occurs when the microprocessor selects the Input Control

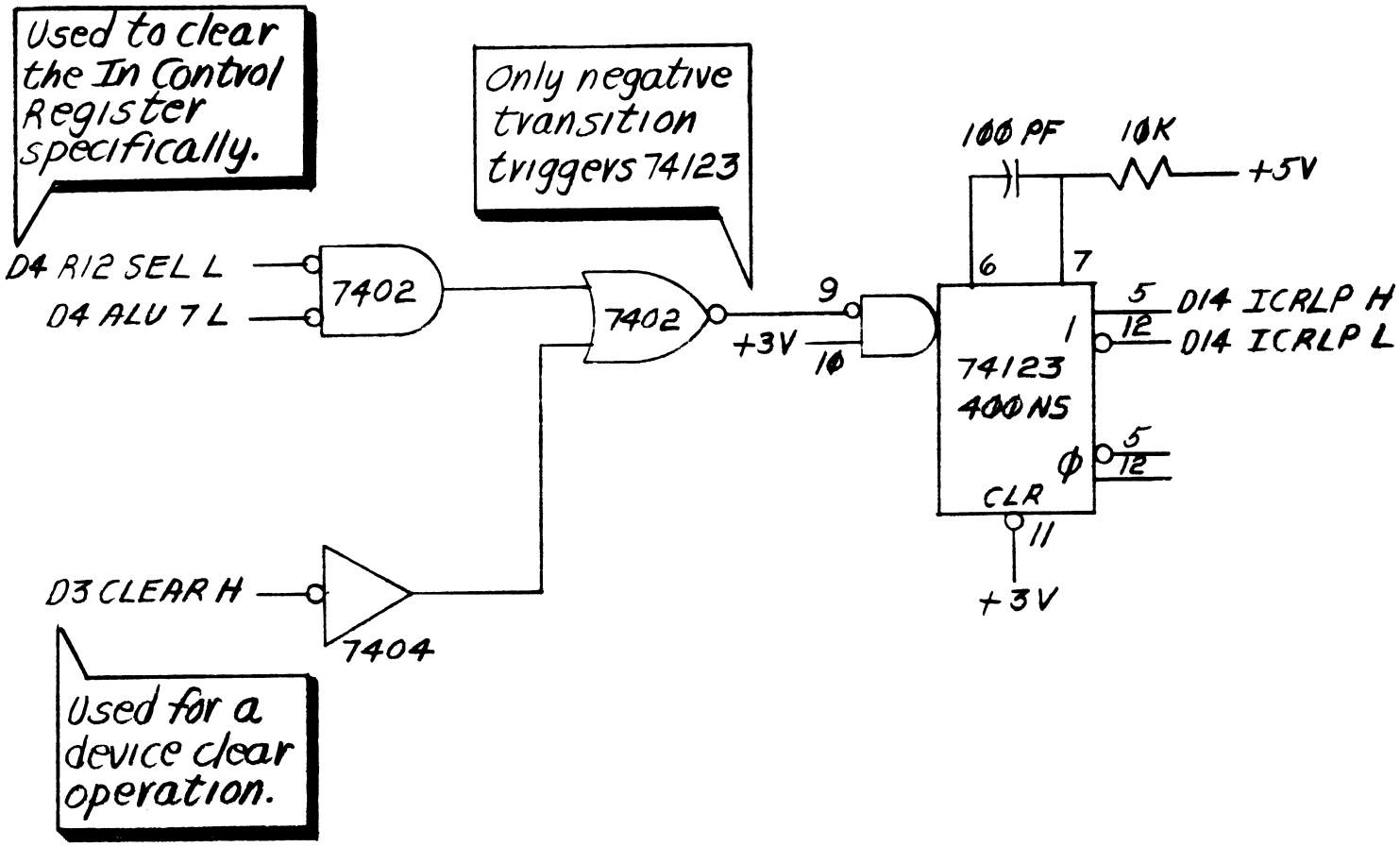


Figure 4-7 Logic for Input Control Register Bit 7

register (D14 R12 SEL L goes low)and D4 ALU 7 L goes low. Signal D4 ALU 7 L is the double inversion of D3 BALU 7 L from the microprocessor.

4.3.2.5 Modem Control Register

Bits 0 and 1 (Print D14)

These bits are reserved for future use. Physically, they are switches. One side is grounded and the other side is connected to +5 V through a resistor; therefore, the output is high when the switch is OFF (open).

Bits 2 and 3 (Print D16)

Bit 2 is Clear to Send (CS) and bit 3 is Modem Ready (MODEM RDY). Both bits are read only. Both signals come from the modem to 1489 receivers which convert the inputs from EIA logic levels to TTL logic levels. The signals are inverted during level conversion and are inverted again to become D16 CS H and D16 MODEM RDY H. The outputs of the 1489 receivers that are associated with these bits are ANDed at a negated-input AND gate. The output of this gate is D16 SEND F H (Send Function) which must be asserted to enable the transmitter.

Bit 4 (Print D15)

Bit 4 is Half Duplex (HDX) and is read/write. This bit is stored in the HDX flip-flop. The D input of this flip-flop is D4 ALU 4 H which comes from the microprocessor. It is clocked by the trailing edge of D4 R13 SEL L which is generated when the microprocessor selects the Modem Control register. When the flip-flop is set,

D15 HDX (1) H is asserted at its 1 output. This signal disables the receiver clock logic when the half duplex mode is selected. The HDX flip-flop is cleared by D3 CLEAR L.

Bit 5 (Print D15)

Bit 5 is Request to Send (RS) and is read only. This bit is stored in the RS flip-flop. The D input of this flip-flop is D8 SFG (1) H (Send Function Generator) which is the 1 output of the SFG flip-flop (print D8). The state of this flip-flop is determined by the 0 output of the DATA LATE flip-flop (print D6). A detailed discussion of the relationship between the DATA LATE and SFG flip-flops is covered in Paragraph 4.3.5.4. Figure 4-8 shows the RS flip-flop and associated line driver. The RS flip-flop is clocked by D15 TX CLOCK H and directly cleared by D14 OCLRP L. Inside the line unit, Request to Send is considered to be ON when the RS flip-flop is set. The corresponding state at the driver output which is EIA compatible, is high for the ON condition. This occurs when the Transmit Start of Message bit is set. Once set, it is cleared if the response time to the transmitter DONE bit is longer than one character time. This action sets the DATA LATE flip-flop and clears the SFG flip-flop which drives D8 SFG (1) H low at the D input of the RS flip-flop. This produces a low at the driver output (EIA RTS) which indicates that Request to Send is OFF.

The line unit is shipped with jumper W4 installed which allows the logic to control RS. In a private line application, W4 can be removed and W5 installed to keep RS on permanently.

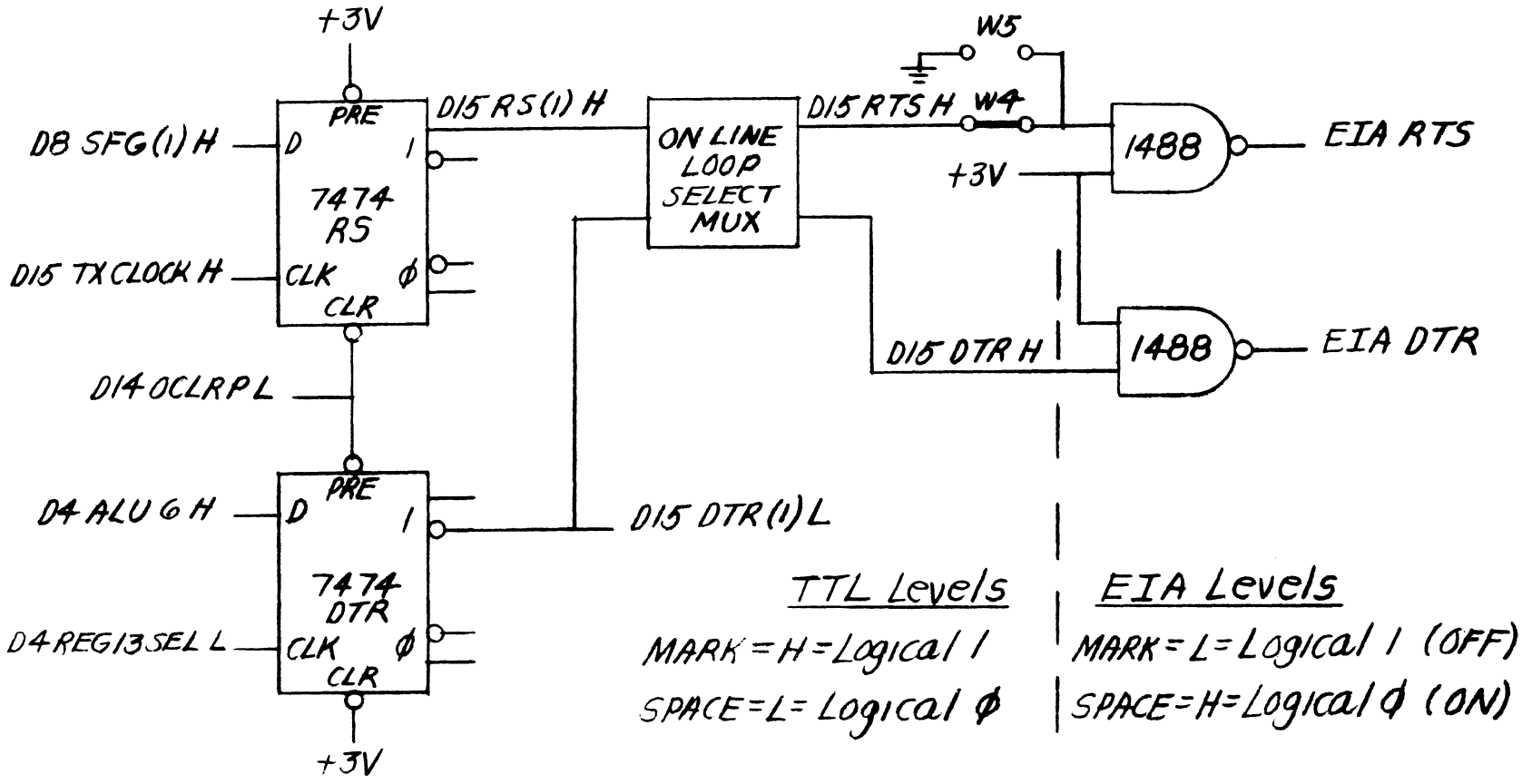


Figure 4-8 RTS and DTR Flip-Flops and Associated Drivers

Bit 6 (Print D15)

Bit 6 is Data Terminal Ready (DTR) and is read/write. This bit is stored in the DTR flip-flop. It is directly set by D14 OCLRP L which is generated under control of the microprocessor specifically or during a device clear operation. It can be written into (set or cleared) by the microprocessor using signal D4 ALU 4 H as the D input and D4 R13 SEL L as the clock input. D4 R13 SEL L is a negative pulse that is generated when the microprocessor selects the Modem Control register (13_8). The positive-going trailing edge of D4 R13 SEL L clocks the DTR flip-flop. The 0 output of the DTR flip-flop, D15 TR (1) L, goes to the ON LINE LOOP SELECT MUX and emerges as D15 DTR L. This signal is inverted by a 1488 driver (print D16) to generate EIA DTR. When the DTR flip-flop is set, EIA DTR is high which is the ON condition for this signal.

Bit 7 (Print D16)

Bit 7 is RING and is read only. This signal comes from the modem to a 1489 receiver which converts the signal from EIA logic levels to TTL logic levels. The signal is inverted during level conversion and is inverted again by a 7404 inverter to become D16 RING H.

4.3.2.6 Sync Register - The Sync register is described in Section 4.3.3 Out Control Logic.

4.3.2.7 Reserved Switch Registers (R15 and R16) - Two switch packs are used as switch selectable registers that are reserved for future use. Each pack contains eight switches. One side of each switch is grounded and the other side is connected to +5 V

through a resistor; therefore, the output is high when the switch is OFF (open). Register R15 outputs are D14 REG 15-0 H through D14 REG 15-7 H. Register D16 outputs are D14 REG 16-0 H through D14 REG 16-7 H.

4.3.2.8 Maintenance Register

Bit 0 (Print D14)

Bit 0 is MODE and is read/write. This bit is stored in a 7474 flip-flop. Its preset input is connected to signal D3 CLEAR L. When the microprocessor drives D3 CLEAR L low to initialize the line unit, the flip-flop is set which puts the line unit in the DDCMP mode. To put the line unit in the Bit Stuff mode, the flip-flop must be cleared by using its D input (D4 ALU 0 H) and clock signal D4 R17 SEL L which is generated when the microprocessor selects the Maintenance register (17_8).

NOTE

A Device Clear operation puts the line unit in the DDCMP mode. Therefore, when operating in the Bit Stuff mode, exercise caution when clearing the line unit.

Bit 1 (Print D15)

Bit 1 is the internal RC clock (ECS) and is read only. It is picked off the 1 output of the RCC ENABLE flip-flop. The signal is D15 ECS H and its frequency is approximately 10 KHz because the flip-flop divides the basic RC clock frequency by two.

Bit 2 (Reserved)

This bit is reserved for future use.

Bit 3 (Print D12)

Bit 3 is In Composite Input Ready (ICIR) and is read only. The actual signal is D12 ICIR H which is the output of a 3-input 74S11 AND gate. Functionally, it is the AND of the INPUT RDY output of the three 3341 FIFOs that make up the In Data Silo. When asserted, D12 ICIR H indicates that the silo is ready to accept data.

Bit 4 (Print D8)

Bit 4 is Out Composite Output Ready (OUT RDY) and is read only. The actual signal is D8 OCOR H which is the output of a 3-input 74S11 AND gate. Functionally, it is the AND of the OUTPUT RDY output of the three 3341 FIFOs that make up the Out Data Silo. When asserted, D8 OCOR H indicates that data is available to the transmitter.

Bit 5 (Print D10)

Bit 5 is Serial In (SI) and is read only. The actual signal is D10 SI which is the inversion of D15 RX DATA. This is the serial data to the receiver input (H = logical 1).

Bit 6 (Print D13)

Bit 6 is Quotient In (QI) and is read only. The actual signal is D13 QI H which is the output of the sixteenth bit of the receiver BCC register.

Bit 7 (Print D9)

Bit 7 is Quotient Out (QO) and is read only. The actual signal is D9 QO H which is the sixteenth bit of the transmitter BCC register.

4.3.3 Out Control Logic

The output bus (OBUS) and associated logic is shown in circuit schematic D4. The OBUS is used by the DMC11 microprocessor to send information to the line unit. If the information is part of a message to be transmitted, it is temporarily stored in the transmitter data buffer. If the information is the line unit secondary station address (Bit Stuff protocol) or the sync character (DDCMP protocol), it is stored in the Sync register.

The OBUS consists of eight lines identified as D3 BALU 0 L through D3 BALU 7 L. These eight bits are the buffered outputs of the ALU in the microprocessor. They are inverted to become D4 ALU 0 H through D4 ALU 7 H. These signals are sent to the Sync register and the Transmitter Buffer register.

The Sync register is composed of two 74175 quad D-type flip-flops. The eight D inputs in these two devices are connected to OBUS lines D4 ALU 0 H - D4 ALU 7 H. The common clock signal for these flip-flops is D4 R14 SEL L. This signal is generated by the 74S138 register decoder when the microprocessor selects the sync register. Signal R4 R14 SEL L is a negative pulse of 60 ns duration that clocks the Sync register on its trailing edge. The common clear signal for these devices is D3 CLEAR L. It comes from the microprocessor and is considered to be a master clear signal.

The output of the Sync register (D4 SYNC 0 H - D4 SYNC 7 H) is compared to the output of the Receiver Shift register (D11 RSR 0 H - D11 RSR 7 H). The comparator is comprised of eight

2-input 8242 exclusive-NOR gates (print D14). The outputs of these open-collector gates are wired-ORed and the resulting signal (D14 ADDRS+SYNC H) is pulled up via a 1K resistor connected to +5 V. The 8242 output goes high only when both inputs are identical. Because of the wired-OR connection, all 8242s must show a match condition before D14 ADDRS+SYNC H is asserted. In the DDCMP protocol, the comparator looks for a sync character. In the Bit Stuff protocol, it looks for the line units secondary address, provided it is operating in the secondary mode. Figure 4-9 is a block diagram that shows the interrelation among the OBUS Sync register and the Out Data Silo buffer.

This buffer contains 12 bits that all go to the Out Data Silo FIFOs. These bits are contained in two 74174 Hex D-type flip-flops. The inputs come from the OBUS lines as shown below.

OBUS Lines	Buffer Inputs
0	0 and 8*
1	1 and 9*
2	2 and 10*
3	3 and 11*
4	4
5	5
6	6
7	7

* 8-11 are flip-flop outputs and are not connected directly to OBUS lines

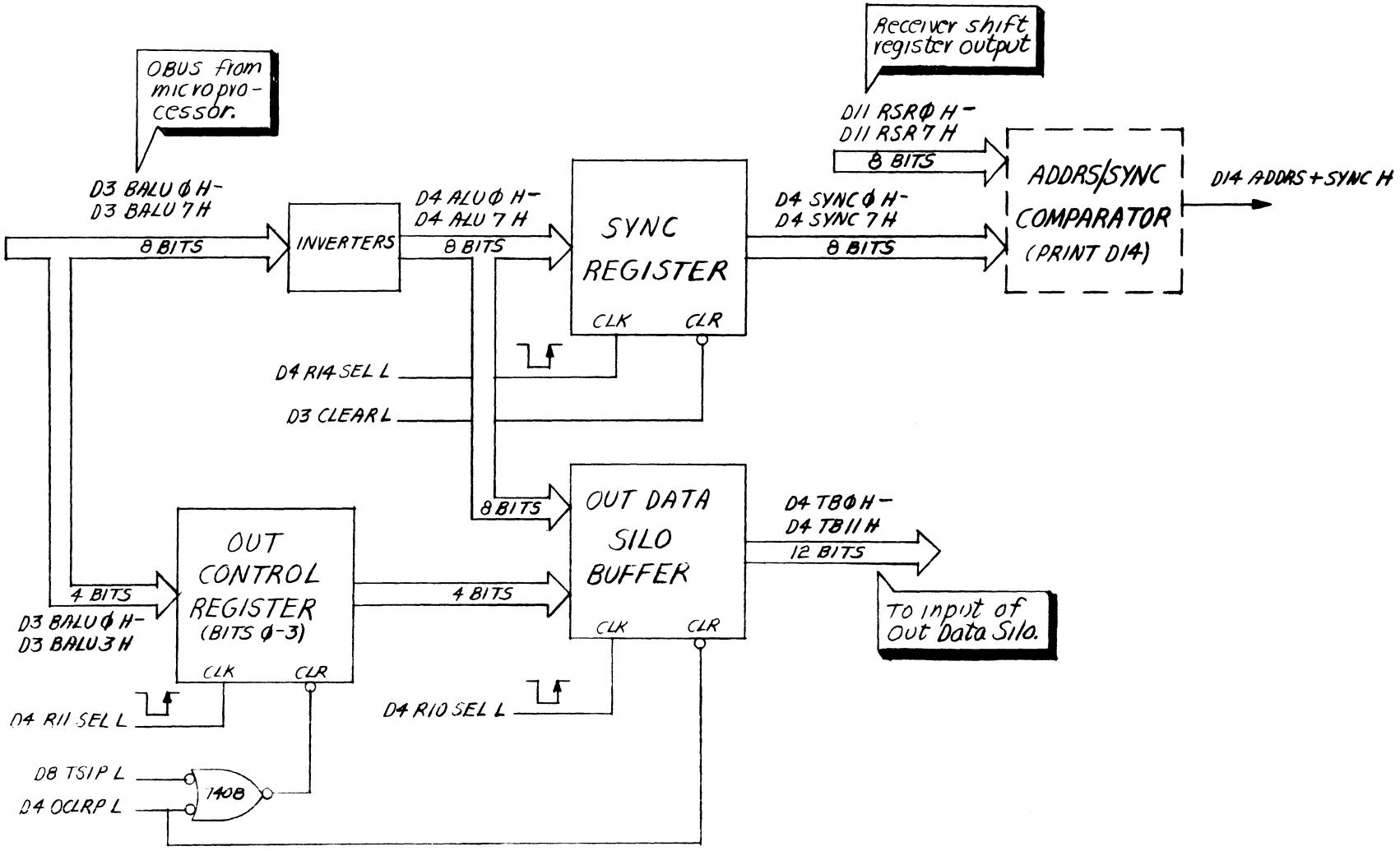


Figure 4-9 Block Diagram of OBUS and Associated Logic

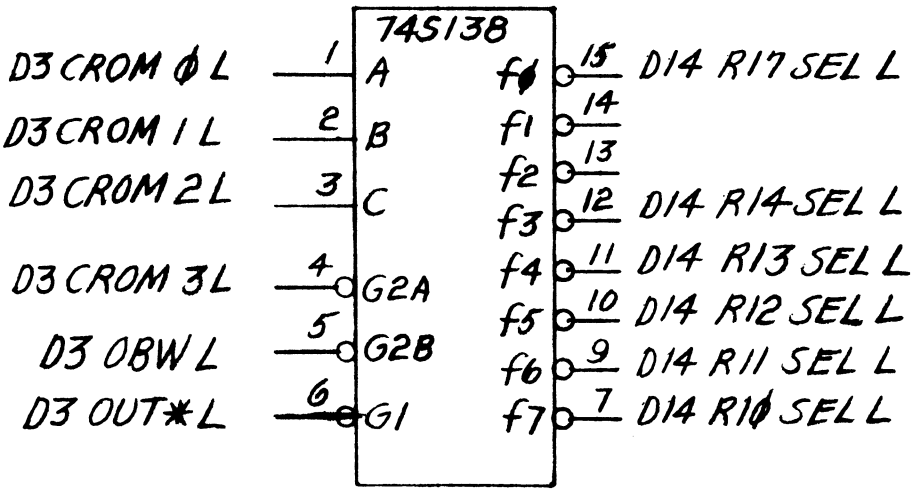
The buffer outputs are D4 TB 0 H - D4 TB 11 H; bits 0-7 are information bits and bits 8-11 are Out Control register bits. Signal D4 R10 SEL L is used to load this buffer and to shift its outputs into the Out Data Silo. This signal is generated by the register decoder which is controlled by the microprocessor. The designation R10 in this signal denotes the Out Data Silo (10_8). This silo can be written into only by the microprocessor; therefore, signal D4 R10 SEL L can be used to load the Out Data Silo.

The buffer is cleared by D14 OCLRP L which is asserted for 400 ns on demand by the microprocessor during a device clear operation. D14 OCLRP L can be also specifically selected by the microprocessor.

A 74175 quad D-type flip-flop contains bits 0-3 of the Out Control register. The inputs are connected to OBUS lines D4 ALU 0 H - D4 ALU 3 H and the outputs go to bits 8-11 respectively of the Out Data Silo buffer. These bits are loaded into the register by D4 R11 SEL L which is generated by the register decoder when the microprocessor selects the Out Control register. These bits are cleared by two signals. The first is D8 TSIP L which is generated when the Out Data Silo is loaded. The second is D14 OCLRP L which is controlled by the microprocessor to clear this register specifically or to clear it as part of the device clear function.

The remaining logic on print D4 is the register decoder. This device is a 74S138 3-to-8 line decoder that is controlled by the microprocessor. The decoder is enabled only when D3 CROM 3 L (pin 4) and D3 OBW L (pin 5) are both low and D3 OUT* H (pin 6) is high. Once enabled, the outputs are selected by the binary decoding

of inputs D3 CROM 0 L - D3 CROM 2 L (pins 1-3 respectively). The eight outputs are D4 R10 SEL L - D4 R17 SEL L. The selected output stays low for approximately 60 ns because enabling input D3 OBW* L is a 60 ns pulse. The decoder and a truth table are shown in Figure 4-10.



74S138 TRUTH TABLE

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2	C	B	A	f0	f1	f2	f3	f4	f5	f6	f7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

G2 IS G2A and G2B. Both low to enable.
X = irrelevant

Figure 4-10 Register Decoder

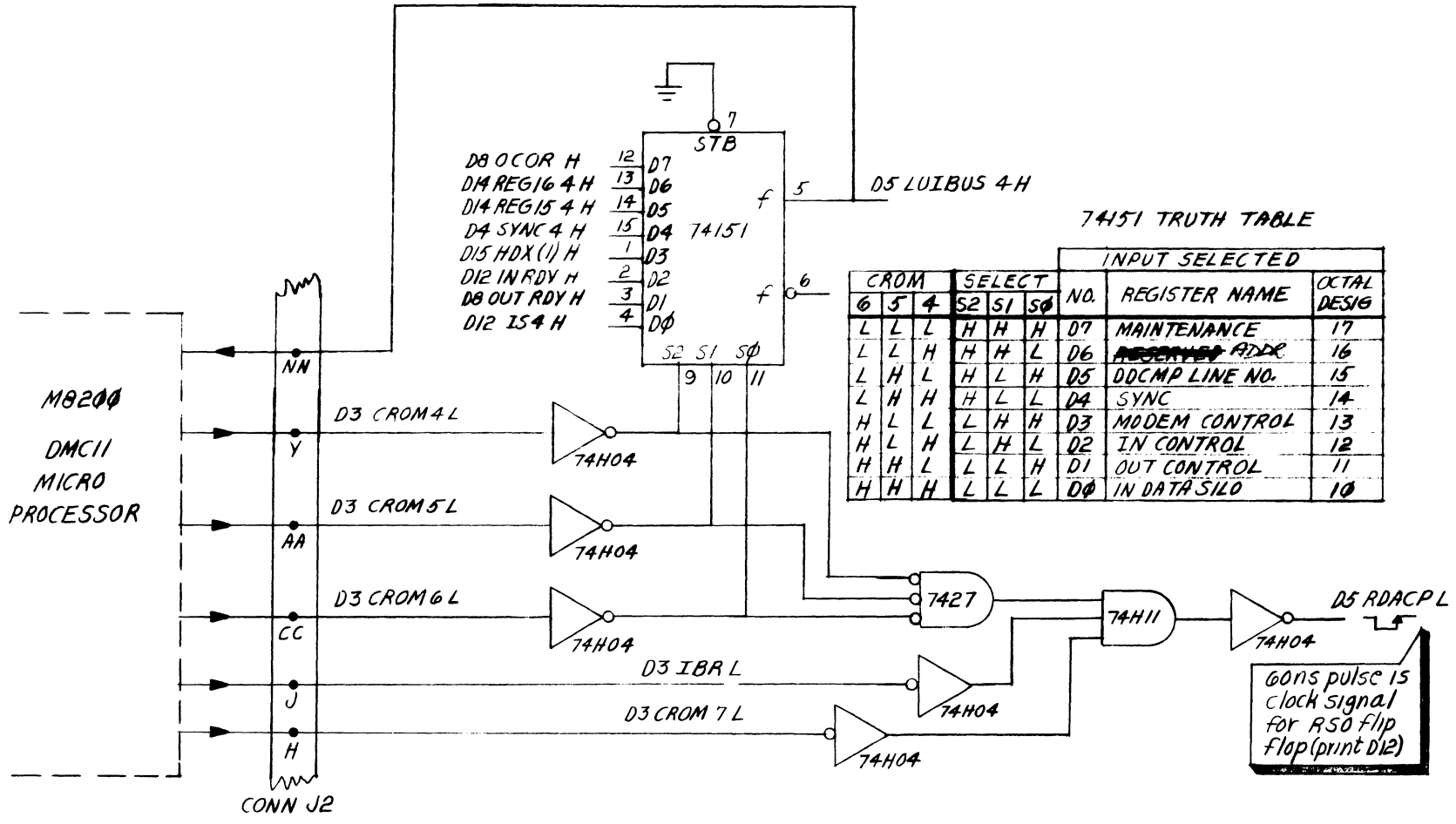
4.3.4 In Bus Control Logic

The input bus (IBUS) control logic is shown in circuit schematic sheet D5. It consists of eight multiplexers that are controlled by the DMC11 microprocessor to place the contents of any one of the eight line unit registers on the IBUS. The IBUS is used by the microprocessor to obtain information from the line unit.

A one-bit slice of the IBUS control logic is shown in Figure 4-11. A 74151 8 line-to-1 line multiplexer is used to handle one bit of all eight registers. Input (register) selection is performed by select inputs S2, S1, and S0 which are controlled by microprocessor signals D3 CROM 4 L, D3 CROM 5 L, and D3 CROM 6 L, respectively. A truth table for the 74151 multiplexer is also shown in Figure 4-11.

For example, if the select inputs are all high, the Maintenance Register (input D7) is selected. The output is D5 LUIBUS 4 H and, in this case, represents bit 4 of the Maintenance Register. The multiplexer has complementary outputs; however, in this application only the true output (pin 5) is used. The strobe input (pin 7) is permanently connected to ground to keep the multiplexer enabled.

The multiplexer outputs (D5 LUIBUS 0 H -- D5 LUIBUS 7 H) are sent through a connector (J2 on the M8201 and J1 on the M8202) and one-foot long cable to the microprocessor.



CROM			SELECT			INPUT SELECTED		
6	5	4	S2	S1	SØ	NO.	REGISTER NAME	OCTAL DESIG
L	L	L	H	H	H	D7	MAINTENANCE	17
L	L	H	H	H	L	D6	~~RECEIVER~~ ADDR	16
L	H	L	H	L	H	D5	DDCMP LINE NO.	15
L	H	H	H	L	L	D4	SYNC	14
H	L	L	L	H	H	D3	MODEM CONTROL	13
H	L	H	L	H	L	D2	IN CONTROL	12
H	H	L	L	L	H	D1	OUT CONTROL	11
H	H	H	L	L	L	DØ	IN DATA SILO	10

Figure 4-11 IBUS Control Logic (1-Bit Slice)

Circuit schematic D5 (and Figure 4-11) shows some additional logic that is associated with reading the In Data Silo register. When the In Data Silo is selected by the microprocessor, all three inputs of a 7427 NOR gate are low which drives its output high. This signal goes to one input of a 74H11 3-input AND gate. Control signal D3 CROM 7 L from the microprocessor is inverted and puts a high on the second input of this gate. When the silo is read by the microprocessor, D3 IBR L is inverted and puts a high on the third input. The output of the AND gate goes high and is inverted to generate D5 RDACP L. Signal D3 IBR L is a 60 ns pulse; therefore, D5 RDACP L is a negative pulse of 60 ns duration. The positive-going trailing edge of D5 RDACP L is used to clock the RSO flip-flop in the In Data Silo logic (print D12).

4.3.5 Transmitter Control Logic

The detailed discussion of the transmitter logic is divided into six parts as follows.

Discussion	Paragraph
ROMs and ROM Sync Buffer	4.3.5.1
Clock Logic	4.3.5.2
TD Flip-Flop and 1s Counter	4.3.5.3
TCSC Counter	4.3.5.4
SACT, DONE and DATA LATE Flip-Flops	4.3.5.5
Out Data Silo	4.3.5.6
Shift Register	4.3.5.7

4.3.5.1 ROMs and ROM Sync Buffer -- Three read-only memories (ROMs) are the major controlling elements for the transmitter. Each one is a 1024 bit TTL ROM (5603 or equivalent) that is organized as 256 words of 4 bits each. The ROMs are identified as shown below.

Name	Print No.
Function Decode ROM (FDR)	D6
Data Path Control ROM (DPCR)	D7
Data Decode ROM (DCR)	D7

Both enabling inputs (pins 13 and 14) are held low to keep the ROM enabled constantly while power is applied. The inputs represent an 8 bit binary coded address that selects any one of 256 words (decimal addresses 0 through 255). The most significant bit is pin 15 and the least significant bit is pin 5. Each word is pre-programmed and is unalterable. When addressed, a specific word always produces the same states at the four outputs.

As control elements, the ROMs act as compact logic arrays that replace a large amount of distributive logic.

A listing for each ROM is contained in the print set (drawing ? * The listing contains input/output binary equivalents for each address along with a brief note of what the address represents. Many addresses form combinations of inputs that are functionally meaningless or are not allowed. These addresses are defined as illegal.

The circuit schematic for the ROMs and associated logic is contained in prints D6 and D7. A simplified diagram is shown in Figure 4-12.

The data path control ROM has its enabling inputs (pins 13 and 14) connected directly to ground. The other two ROMs are enabled by signal D14 GR TEST POINT. This signal is the output of a 7404 inverter on print D14. The inverter input is connected to one side of a switch in switch pack SP3. This point is also connected to +5 V through a resistor. The other side of the switch is grounded. With the switch open (OFF), D14 GR TEST PT goes low and keeps the ROMs enabled. During maintenance, closing this switch can be used to simulate a disabled ROM.

In the following discussion, the source and destination of the signals associated with the ROMs and ROM sync buffer are described functionally. Some signals, specifically ROM inputs, have relevance only when viewed as a group during a specific point in a transmit operation.

Function Decode ROM

This ROM controls the setting of TX DONE and decodes the microprocessor inputs which in some cases are synchronized to the modem clock. This information along with the current state of the logic determines the next event on a character basis. The FDROM responds to the microprocessor, modem, and internal logic as shown in Table 4-1.

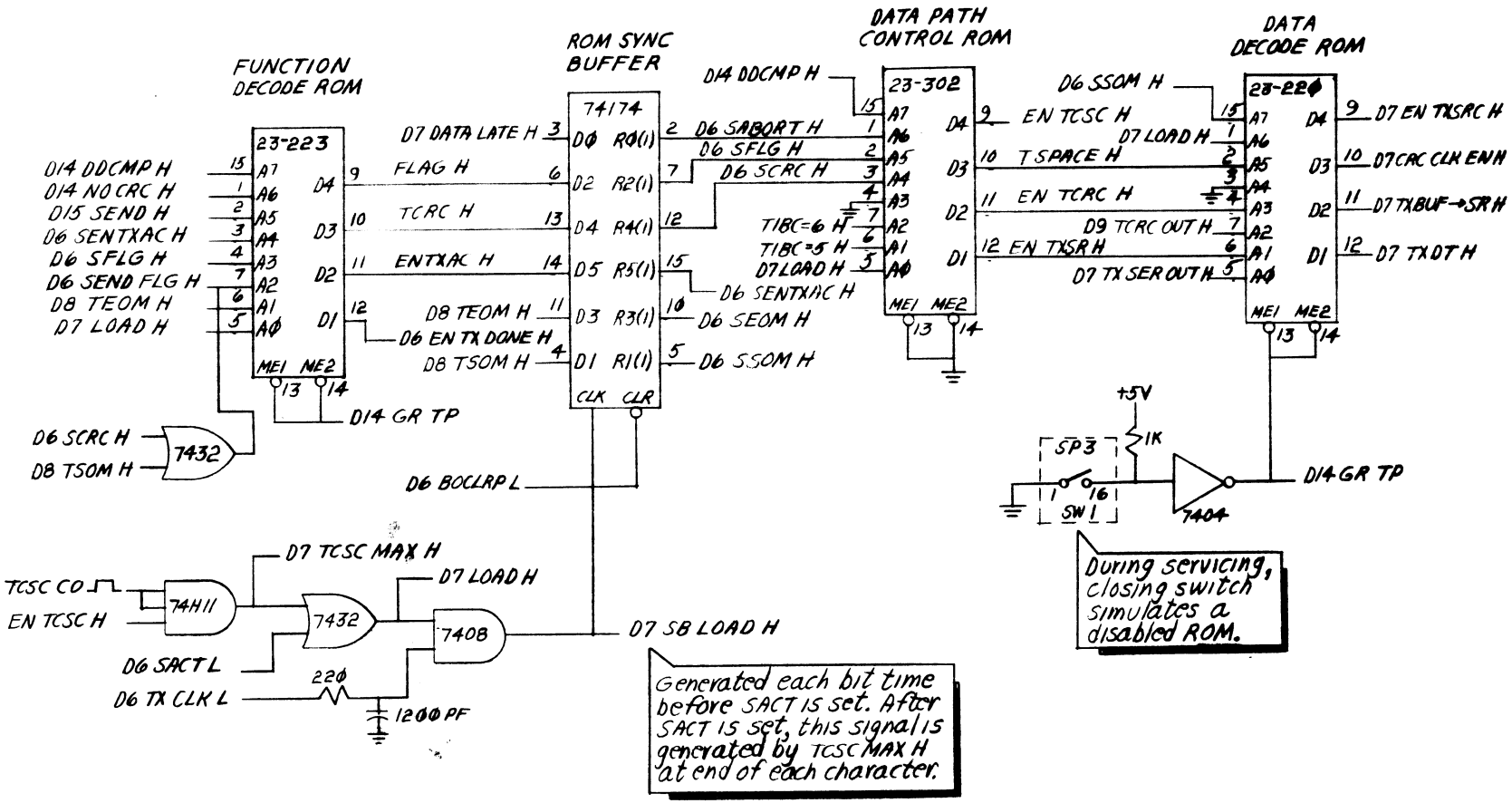


Figure 4-12 Transmitter ROMs and Associated Logic

Table 4-1

Transmitter Function Decode ROM Input Signals

Signal	Pin	Source
D14 DDCMP H	15	Microprocessor via bit 0 of Maintenance Register.
D14 NO CRC H	1	Hardware selectable using switch no. 1 in switch pack no. 1 (E26 on M8201 and E29 on M8202).
D16 SEND H	2	AND function of CLEAR TO SEND and DATA SET READY from the modem.
D6 SENTXAC H	3	Function Decode ROM via ROM Sync Buffer.
D6 SFLG H	4	
D6 SEND FLG H	7	OR function of D6 SCRC H and D6 SSOM H from ROM Sync Buffer.
D8 TEOM H	6	Microprocessor indirectly via bit 1 of Out Control Register. This is a silo bit.
D7 LOAD H	5	Transmitter control logic.

Three of the four outputs from the function decode ROM are sent to the ROM Sync buffer. These outputs are: D6 TFLG H, D6 TCRC H, and D6 ENTXAC H. The fourth output (D6 ENTXDNE H) goes to the preset input gating for the TX DONE flip-flop. This signal allows this flip-flop to be set directly at certain times during a transmit sequence.

ROM Sync Buffer

The ROM Sync buffer is a 74174 hex D type flip-flop that has a single-rail output (Q=H=1) for each input. The buffer provides storage for six transmitter control logic signals. After the flag or sync characters have been sent, the ROM Sync buffer is clocked only at the end of a character. This allows the logic to set up for the next character during the present character while not affecting the outputs of the buffer. It has common clock and clear inputs. Three inputs come from the FDROM. They are? TFLG H, TCRC H, and ENTXAC H. The corresponding outputs are D6 SFLG H, D6 CRC H and D6 SENTXAC H. The fourth and fifth inputs are: D8 TEOM H (Out Control register bit 1) and D8 TSOM H (Out Control register bit 0). TEOM and TSOM are silo bits. The corresponding outputs are: D6 SEOM H and D6 SSOM H. The sixth input is D6 DATA LATE (1) H, which is hardware controlled, and the corresponding output is D6 SABORT H.

Two gates and several signals are used to provide the clock signal for the ROM Sync buffer. During the idle state and up until the first bit of the sync character (DDCMP) or flag character (Bit

Stuff protocol) is transmitted, OUT ACTIVE is cleared. As a result, D6 SACT L is high. This signal goes to a 7432 OR gate and emerges as D7 LOAD H. Signal D7 LOAD H is ANDed with D6 TXCLK L which is a buffered and inverted transmitter clock from the modem. The result of this ANDing is D7 SB LOAD H. The buffer is actually clocked by the positive-going leading edge of D6 TX CLK L. As long as OUT ACTIVE is cleared, the ROM Sync buffer is clocked once each bit time.

When OUT ACTIVE is set, D6 SACT L goes low and drives D7 LOAD H low. D7 LOAD H goes high again for a short time only when the TCSC counter reaches the last bit of a character. At this time, the TCSC counter asserts positive pulse D7 TCSC MAX H. It is ANDed with D6 TX CLK L to generate D7 SB LOAD H which clocks the ROM Sync buffer. The D6 TX CLK L clock pulse in this case is the one associated with the last bit of the current character.

Except during the start up phase of transmission, the ROM Sync buffer is clocked only at the end of a character. This allows the microprocessor to change the FDROM inputs in anticipation of the next event without interferring with the current event thus synchronizing the line unit and modem.

The outputs of the ROM Sync buffer can change only when it is clocked. The outputs are considered to be synchronized to the modem transmitter clock because the buffer is clocked by D6 TX CLK L which is a derivative of the modem clock.

Data Path Control ROM

The data path control ROM (DPCROM) formats the Bit Stuff protocol control characters and controls transmitter data path multiplexing. The DPCROM inputs are shown in Table 4-2.

Table 4-2

Transmitter Data Path Control ROM Input Signals

Signal	Pin	Source
D14 DDCMP H	15	Microprocessor via bit 0 of Maintenance Register.
D6 SABORT H	1	Transmitter control logic.
D6 SFLG H	2	Function Decode ROM via ROM Sync buffer.
D6 SCRC H	3	
Ground	4	
D7 T1BC=6 H	7	T1BC Counter
D7 T1BC=5 H	6	
D7 LOAD H	5	Transmitter control logic.

Three of the four DPCROM outputs go to the data decode ROM. These outputs are: D7 TSPACE H, D7 ENTCRC H, and D6 ENTXSR H. The fourth output, D7 ENTCSC H, is the enabling signal for the TCSC counter. Signal D7 ENTCSC H must be high to allow the counter to count. This signal is not asserted (goes low) when a 0 is being stuffed into the transmitted data stream; therefore, the TCSC counter is inhibited to prevent the stuffed 0 from being counted (Bit Stuff mode only).

Data Decode ROM

The data decode ROM (DDROM) multiplexes the data received from the TX shift register, TX CRC register, and DPCROM. It also controls the timing of transfers from the Out Data Silo to the TX Shift register. The DDROM inputs are shown in Table 4-3.

The four DDROM outputs are: D7 ENTXSRC H, D7 CRC CLK EN H, D7 TXBUF⟶SR H, and D7 TXDT H.

Signal D7 ENTXSRC H is a qualifying input for the Transmitter Shift register clock. This register can be clocked only when D7 ENTXSRC H is asserted. This signal is not asserted during the following conditions: during transmission of Bit Stuff mode control character; CRC information; when a 0 is stuffed; and when D7 TXBUF⟶SR H is asserted.

Table 4-3

Transmitter Data Decode ROM Input Signals

Signal	Pin	Source
D6 SSOM H	15	ROM Sync Buffer.
D7 LOAD H	1	Transmitter control logic.
D7 TSPACE H	2	Data Path Control ROM.
Ground	3	
D7 ENTCRC H	4	Data Path Control ROM.
D9 TCRC OUT H	7	TXCRC Register.
D7 ENTXSR H	6	Data Path Control ROM.
D7 TX SER OUT H	5	TX Shift Register.

Signal D7 CRC CLK EN H is a qualifying input for the TX CRC register. This register can be clocked only when D7 CRC CLK EN H is asserted. This signal is not asserted when control or sync characters are being transmitted.

Signal D7 TXBUF —>SR H must be asserted to allow bits 0-7 of the Out ~~Control register~~ to be loaded into the TX Shift register. (This is information to be transmitted.)

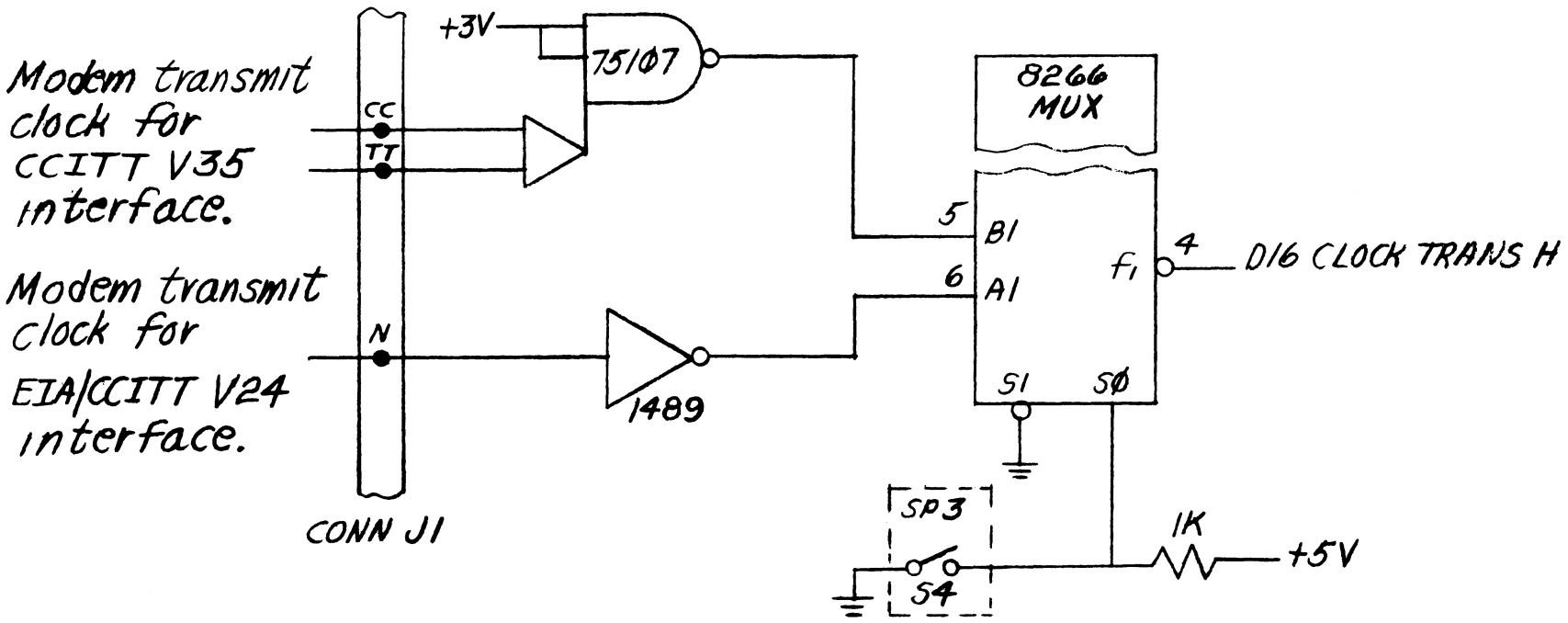
Signal D7 TXDT H from the Data Decode ROM represents data to be transmitted. It goes to the TD flip-flop which in turn goes to the TDS flip-flop. The output of the TDS flip-flop goes to the conversion logic (M8201) or the integral modem (M8202).

This arrangement ensures that the transmitted data is synchronized with the leading edge of the modem transmit clock to keep distortion at a minimum.

The TDS flip-flop is clocked by D15 TX CLOCK H which is offset from the modem clock by only 50 ns. Hence, the TDS flip-flop is considered to be synchronized to the modem transmit clock leading edge. Shortly after TDS clocks a data bit on the line, the TD flip-flop has captured the next bit to be transmitted.

4.3.5.2 TX Clock Logic - In the user mode, the transmitter clock is supplied by the modem. Special logic allows selection of an internal RC clock or single step clock during maintenance. This maintenance clock logic is discussed in Paragraph 4.3.9 Maintenance Logic.

The transmitter clock signal from the modem goes to a receiver in the level conversion logic. The logic is shown in print D16 and Figure 4-13. The signal goes to a 1489 receiver for an EIA/CCITT V24 interface or a 75107 two-channel receiver for a CCITT V35 interface. The outputs of these receivers go to an 8266 2-input 4-bit multiplexer. Select input S1 of this mux is connected to ground; therefore, the position of the switch connected to select input S0 determines which input is chosen. With the switch closed (ON), S0 is low and input B (CCITT V35) is selected. With the switch open (OFF), S0 is high and the inverse of input A (EIA/CCITT V24) is selected. The output of the mux is D16 CLOCK TRANS L. This signal is sent to one input of the CLK SRC MUX (print D15). The multiplexer output is D15 TX CLOCK H and can represent the modem transmitter clock single step clock, or internal RC clock as explained in Paragraph 4.3.9.



SELECT		SELECTED INPUT
S1	S0	
L	L	(B) CCITT V35
L	H	($\overline{A}$) EIA/CCITT V24

Figure 4-13 EIA Transmitter Clock Conversion Logic

Figure 4-14 shows the TX clock logic and associated timing diagram. Signal D15 TX CLOCK H clocks the TDS flip-flop. It is inverted to generate D15 TX CLK L which clocks the SACT flip-flop, TCSC counter, and ONES counter.

The positive-going edge of D15 TX CLOCK H triggers the TCP 1-shot (print D6) which generates 200 ns complementary pulses D6 TCP H (pin 5) and D6 TCP L (pin 12). Signal D6 TCP H clocks the TX Data Shift register. The positive-going edge of D6 TCP L triggers the DP 1-shot which generates 200 ns complementary pulses D6 DP H and D6 DP L. Signal D6 DP H clocks the TX BCC register. Signal D6 DP L clocks the TD flip-flop.

Signal D7 LOAD H is asserted at the output of a 7432 OR gate when pulse D7 TCSC MAX H is generated or D6 SACT L is high due to TX ACT being cleared. D7 LOAD H is inverted to generate D7 LOAD L which clocks the TSOP flip-flop. D7 LOAD H is ANDed with D6 TX CLK L, which is delayed approximately 70 ns, to generate D7 SB LOAD H at a 7408 AND gate. Signal D7 SB LOAD H clocks the ROM Sync Buffer.

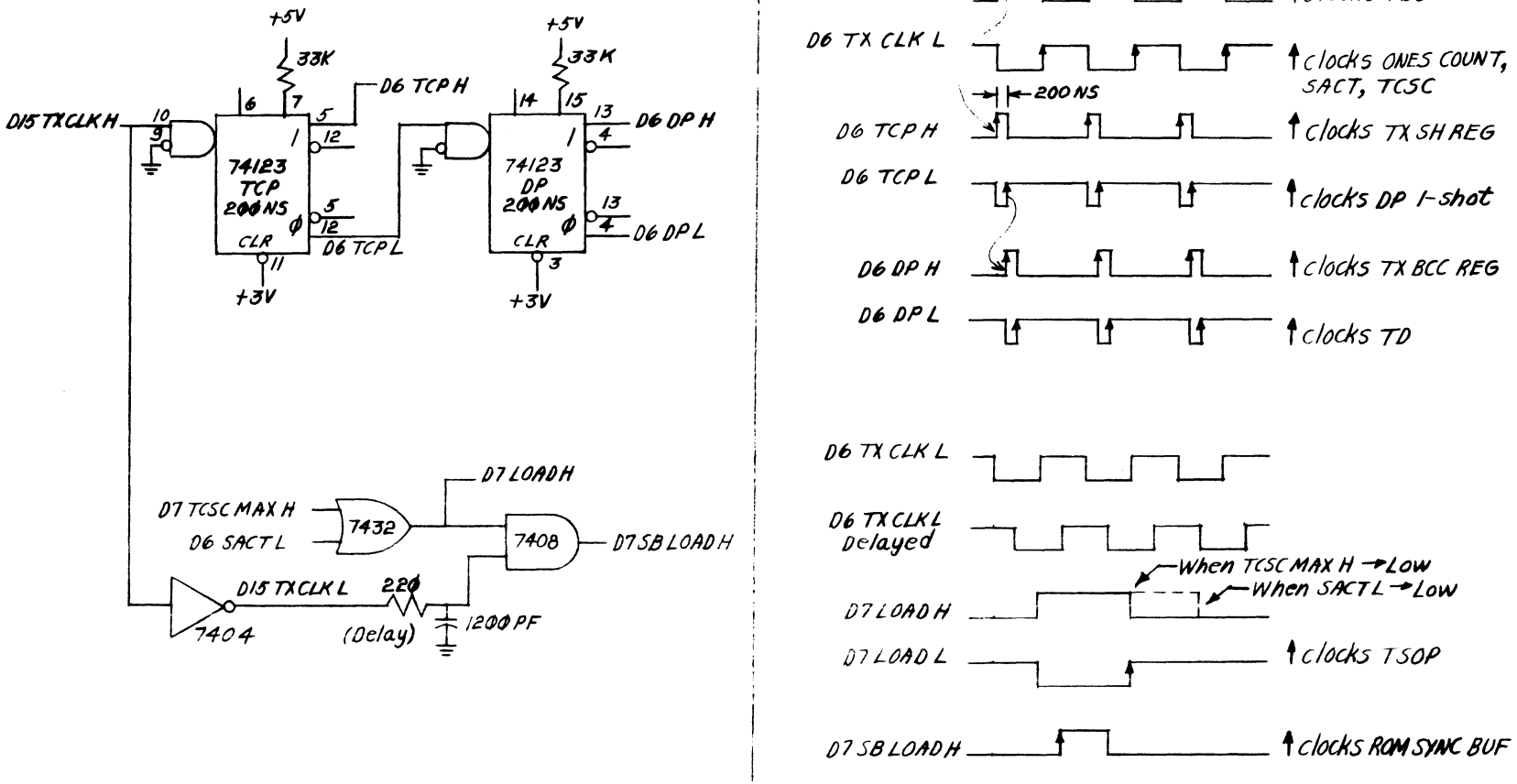


Figure 4-14 Transmitter Clock Logic and Timing Diagram

4.3.5.3 TD Flip-Flop and 1s Counter - The TD flip-flop and 1s counter are discussed together because they are closely related. The conversion of transmitter data from TTL to EIA logic levels is also discussed.

TD Flip-Flop

The TD flip-flop and associated logic is shown in print D7 and Figure 4-15. It is a D type (7474) and its D input is connected to the D7 TXDT H output (pin 12) of the Data Decode ROM. The logical state of signal D7 TXDT H is the same as the transmitted data at the output of the line unit after signal conversion (EIA XMIT DATA). The definitions for TTL and EIA logic levels are shown below.

Outside the line unit the reference point is the level converter output (EIA XMIT DATA).

SPACE=H=+6 V = logical 0

MARK=L=-6 V = logical 1

(For the 75110 two-output driver, a logical 0 exists when output A is negative with respect to output B; and a logical 1 exists when output A is positive with respect to output B.)

Inside the line unit the reference point is Data Decode ROM output pin 12 (D7 TXDT H).

SPACE=L=0 V = logical 0

MARK=H=+5 V = logical 1

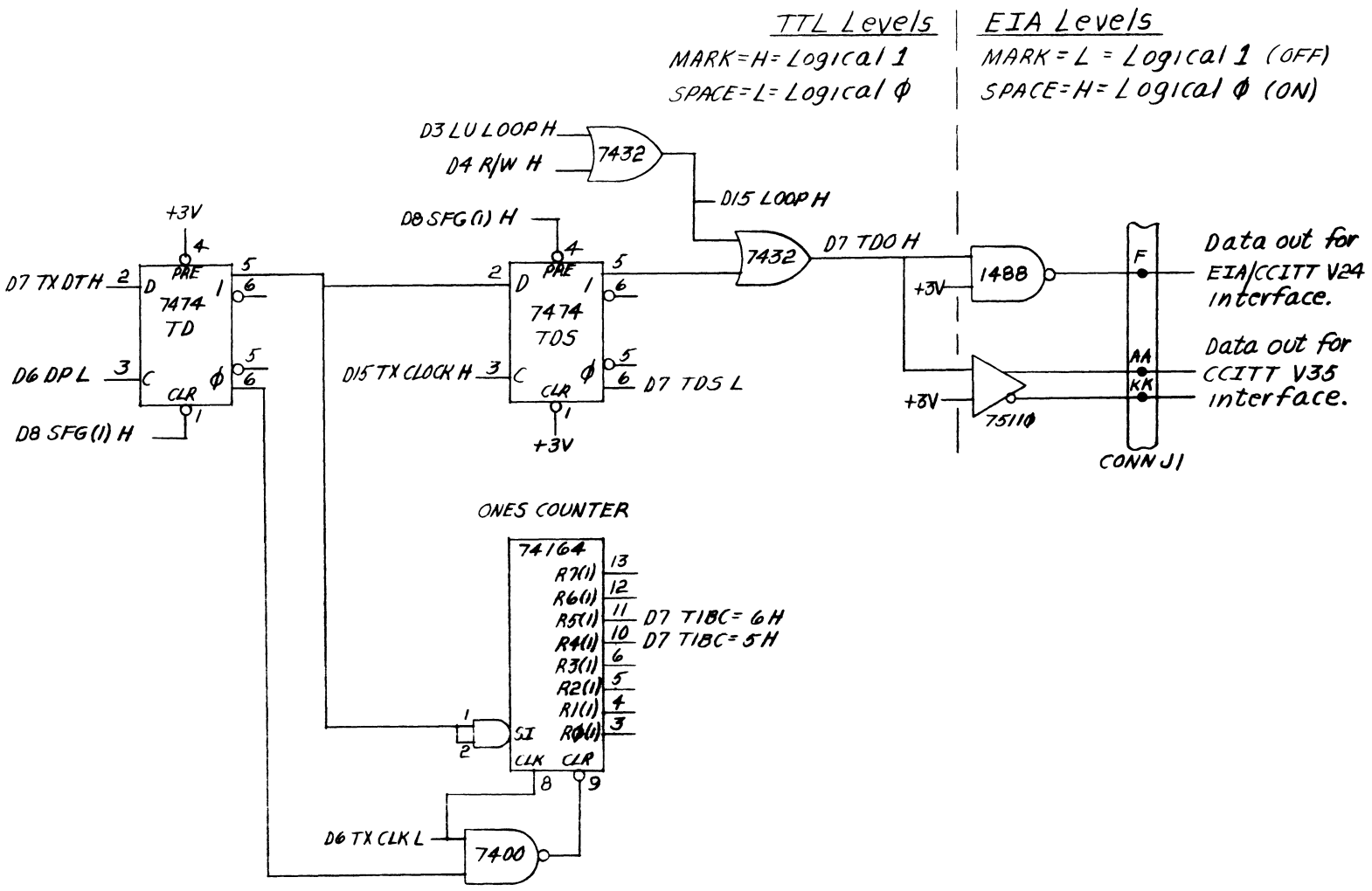


Figure 4-15 TD Flip-Flop and 1s Counter

Minimum distortion of the transmitted data is accomplished by clocking the data on the line with a clock that has minimum offset from the modem clock. The clock signal is D15 TX CLOCK H which is offset by approximately 50 ns due to propagation delays in passing through three devices. It is used to clock the TDS flip-flop which receives the data to be transmitted from the TD flip-flop. This flip-flop receives data from the Data Decode ROM (D7 TXDT H) which is clocked by signal D6 DP L. This clock signal is a derivative of D15 TX CLOCK H and occurs about 400 ns after the positive-going edge of D15 TX CLOCK H. The TDS flip-flop is synchronized to the modem transmitter clock. Shortly after TDS clocks a data bit on the line, the TD flip-flop has captured the next bit to be transmitted.

If the TX DONE bit is not serviced within the required time, signal D8 SFG (1) H goes low and the TD flip-flop is directly cleared and the TDS flip-flop is directly set. This signal also holds the flip-flop set and overrides the clocked data input. This keeps the EIA SMIT DATA line in the MARK state (idle or OFF condition) until a new message is initiated.

During servicing, the microprocessor puts the line unit in the maintenance loop mode by asserting D3 LU LOOP H. This puts the EIA XMIT DATA line in the MARK state.

1s Counter

Functionally, the 1s counter keeps track of the number of consecutive 1s transmitted. This information is used in the Bit Stuff mode to make protocol decisions when transmitting control characters and to maintain data transparency.

The 1s counter is a 74164 8-bit parallel-out serial shift register. Both serial inputs (pins 1 and 2) are connected to the 1 output of the TD flip-flop (Figure 4-15); therefore, with the flip-flop set a 1 is shifted in when the 1s counter is clocked by the positive-going edge of D6 TX CLK L. This clock signal is ANDed with the 0 output of the TD flip-flop at a 7400 NAND gate. When the TD flip-flop is cleared, its 0 output goes high. When the clock signal goes high, the NAND gate output goes low and the 1s counter is cleared. In this mode of operation, the 1s counter counts consecutive 1s and is cleared when a 0 is sensed at its serial input.

Only two of the eight outputs of the 1s counter are used. They are the 5th most significant output (pin 10) identified as D7 T1BC=5 H and the 6th most significant output (pin 11) identified as D7 T1BC=6 H. Signal D7 T1BC=5 H goes high when five consecutive 1s have been shifted in and D7 T1BC=6 H goes high when six consecutive 1s have been shifted in (D7 T1BC=5 H remains high).

These two signals are inputs to the Data Path Control ROM. During transmission of a flag character (Bit Stuff protocol) they control the selection of the 7th and 8th flag bits. During the transmission of all other characters, they force the insertion of a 0 after a series of five consecutive 1s.

The Bit Stuff protocol frame begins and ends with a flag character. All characters between flags must not contain a flag bit pattern. The transmitter inserts (stuffs) a 0 after a sequence of five contiguous 1s that occur within the frame so that a flag pattern (01111110) cannot be transmitted by chance. Under these conditions, when five consecutive 1s are detected, the 1s counter asserts D7 T1BC=5 H. The Data Path Control ROM responds by indicating that a 0 (SPACE) is to be sent next. When the 1s counter detects this 0, it is cleared.

4.3.5.4 Transmitter Character Serialization Counter (TCSC) - The TCSC counter counts the number of bits in each data character that is transmitted exclusive of stuffed 0s (Figure 4-16). It also counts the number of bits in a control character. It counts to 16 for a CRC character and to 8 for all others. At the last bit of a character, it generates pulse D7 TCSC MAX H that synchronizes the current action of the transmitter data path to the microprocessor.

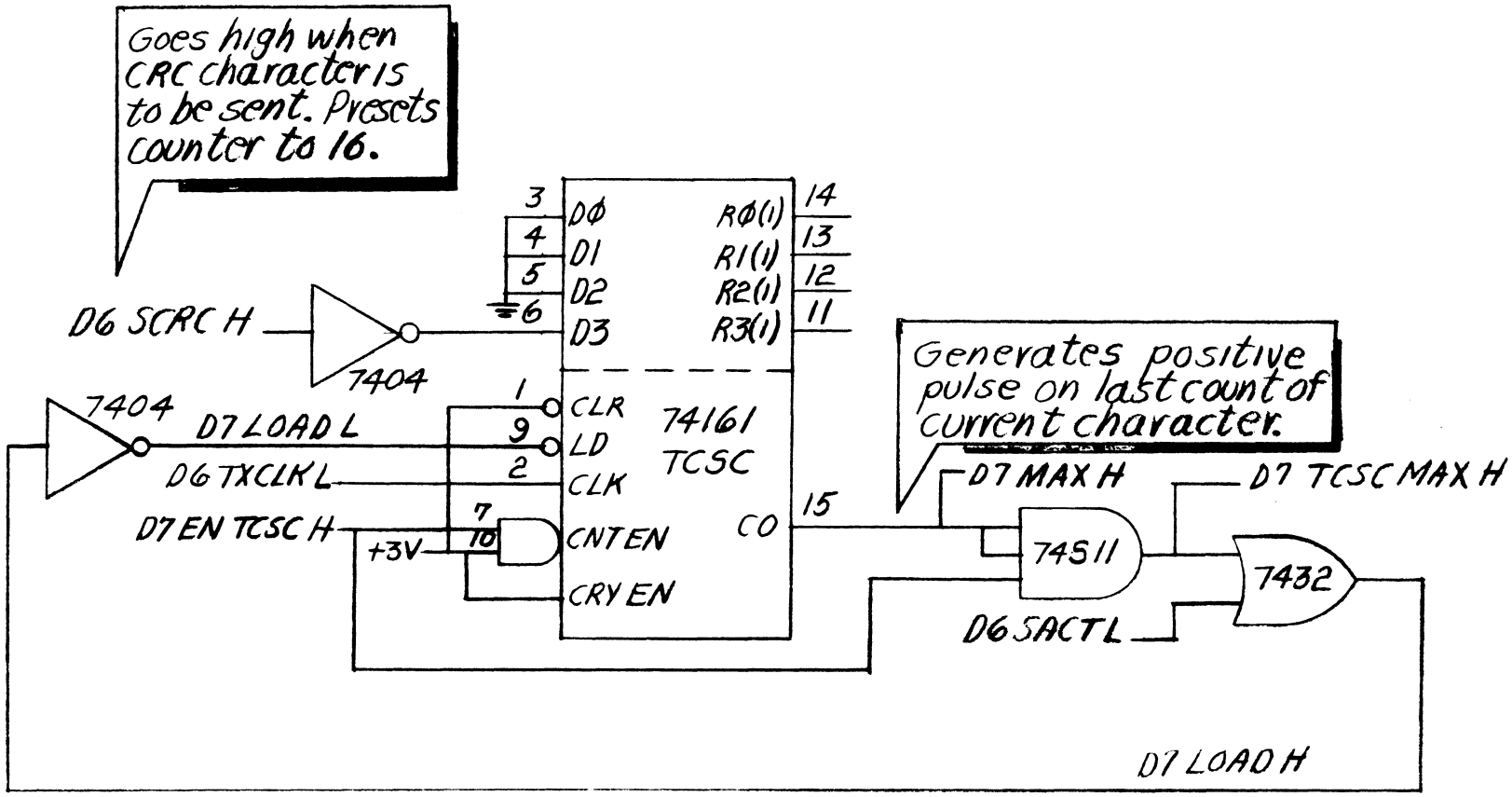


Figure 4-16 TCSC Counter

It is a 74161 synchronous 4-bit counter. Both count enable inputs, ENB CN (pin 7) and ENB CR (pin 10), must be high to enable the counter. ENBCR is permanently connected to +3 V and ENB CN is controlled by signal D7 ENTCSC H. The clear input (CLR) is inhibited by connecting it to +3 V. The counter data outputs are not used. A low signal on the load (LD) input inhibits incrementing the counter and causes the outputs to agree with the inputs after the next clock pulse. When the counter reaches its maximum count (all 1s or count 15), the carry out pulse D7 MAX H is generated. This positive pulse is of the same duration as the positive portion of the LSB output (pin 14). It times out when the next clock pulse arrives and the counter overflows (all outputs equal 0).

The counter can be preset during the load operation to count up to 8 or 16. The CRC character contains 16 bits and when it is coming up for transmission signal D6 SCRC H is high. This signal is inverted which puts a low on the counter MSB input (pin 6). The other three counter data inputs are always held low because they are connected to ground. In this case, when the LD input goes low, the counter is preset to 0 so it counts from 0 to 15 (16 counts) and then overflows.

During the transmission of other data characters, which are 8 bits long, signal D6 SCRC H is low and the counter MSB is high. Now, when the LD input goes low, the counter is preset to 8 so it counts from 8 to 15 (8 counts) and then overflows.

As previously mentioned, the counter is enabled when D7 ENTCSC H is high. This signal is controlled by the Data Path Control ROM. The counter is enabled (D7 ENTCSC H is asserted) during each data character bit exclusive of stuffed 0s. When a 0 is to be stuffed, the ROM drives D7 ENTCSC H low to inhibit the counter.

The counter is clocked by the positive-going edge of D6 TXCLK L which occurs once each bit time.

The LD signal for the counter is D7 LOAD L. When the counter finishes counting a character, it overflows and generates D7 TCSC MAX H. This signal is fed back to a 7432 OR gate and then inverted to generate D7 LOAD L. This signal presets the counter for the next data character. Signal D6 SACT L is the other input to the 7432 OR gate. When the transmitter is inactive, OUT ACTIVE is cleared and D6 SACT L is high which presets the counter.

4.3.5.5 SACT, DONE, and DATA LATE Flip-Flops - The SACT, DONE, and DATA LATE flip-flops represent a functional section of the transmitter control logic (print D6). These flip-flops and associated logic are shown also in Figure 4-17.

SACT Flip-Flop

The SACT flip-flop informs the microprocessor of the status of the transmitter. When SACT is set, the transmitter is active. The D input of the SACT flip-flop is connected to D6 SENTXAC H which comes from the ROM Sync Buffer. The state of this signal is

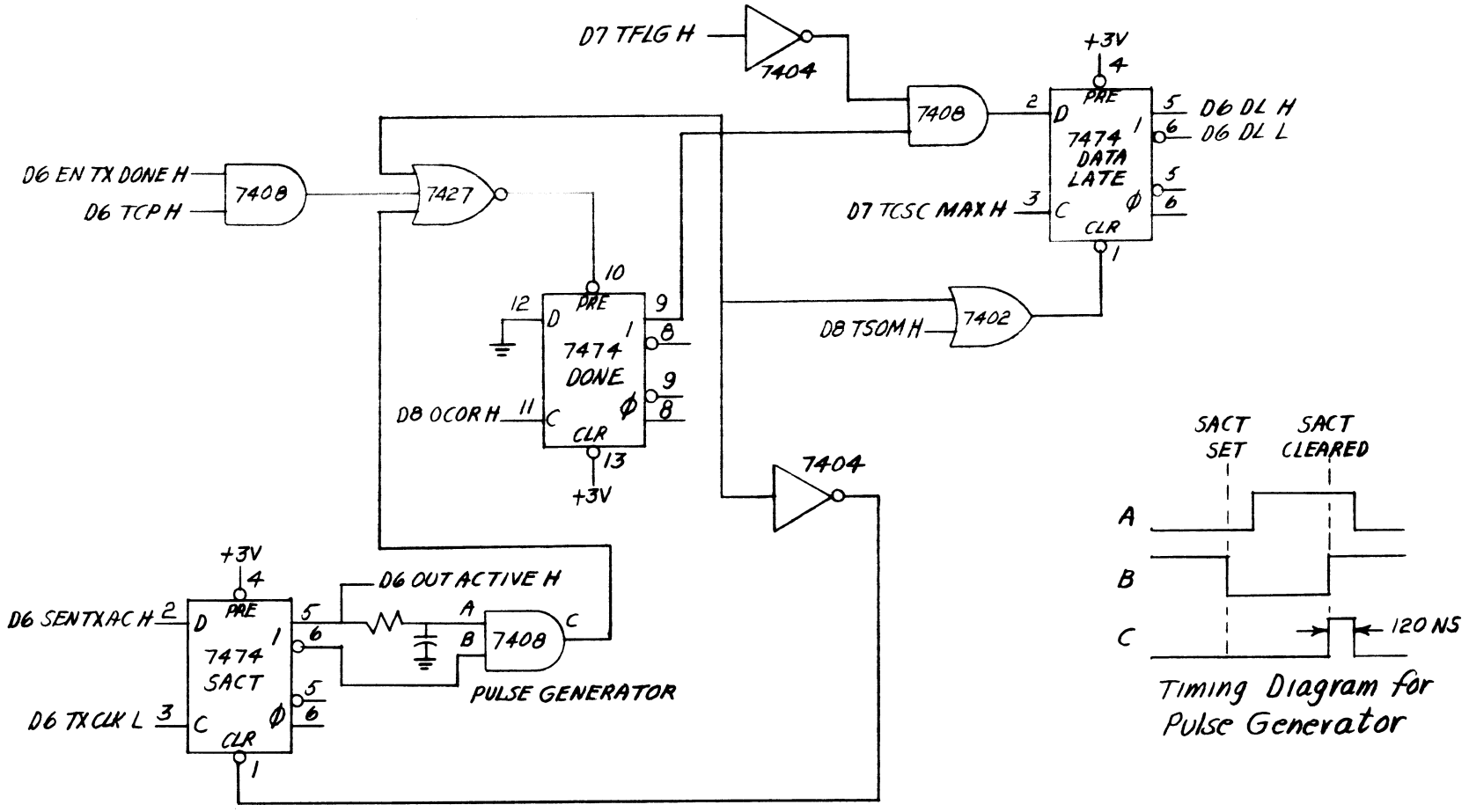


Figure 4-17 SACT, DONE and DATA LATE Flip-Flops

controlled by D6 ENTXAC H from the Function Decode ROM. The clock signal for this flip-flop is D6 TXCLK L and it is cleared by D6 BOCLRP L.

DONE Flip-Flop

The transmitter logic sets the DONE flip-flop when the transmitter has accepted data from the Out Data Silo.

The clear input of the DONE flip-flop (pin 13) is inhibited by connecting it to +3 V. The D input is connected to ground so it can be cleared only when the flip-flop is clocked by the positive edge that occurs when signal D8 OCOR H is asserted. This signal goes high when data from the Out Data Silo is available to the transmitter.

The preset input (pin 10) of the DONE flip-flop is connected to the output of a 7427 3-input NOR gate.

One input of this gate is connected to D14 OCLRP H; therefore, during initialization of the line unit the DONE flip-flop is set.

The second input is connected to the output of a 7408 2-input AND gate. This output represents the ANDing of D6 ENTXDNE H and D6 TCP H. During transmission of flag and data characters, the Function Decode ROM asserts D6 ENTXDNE H to indicate the acceptance of data and control information from the Out Data

Silo. Clock signal D6 TCP H is high for 200 ns during each bit time and, if D6 ENTXDNE H is asserted during this period, the DONE flip-flop is set.

The DONE flip-flop is set one half bit time after the last bit of the final message character, provided the SEND bit is cleared. This indicates the end of the message and the transmitter goes to the idle state (send MARKs). The transmitter logic clears the SACT flip-flop. The 1 and 0 outputs of this flip-flop go to a pulse generator comprised of a 7408 AND gate and an RC network. When the SACT flip-flop is cleared, a 40 ns pulse is generated at the AND gate output. This pulse is the third input of the 7427 NOR gate. This gate inverts the pulse and sets the DONE flip-flop.

DATA LATE Flip-Flop

During transmission, if DONE is still set at the end of the current character, the hardware sets the DATA LATE flip-flop. This indicates that data was not available in time from the Out Data Silo.

The preset input of the DATA LATE flip-flop is connected to +3 V; therefore, it can be set only through clocking action. Its D input is connected to the output of a 7408 2-input AND gate. One input of this gate comes from the 1 output of the DONE flip-flop which is high when DONE is set. The other input is the inversion of D7 TFLG H. This signal is high when a Bit Stuff protocol flag is being transmitted which puts a low on the D input of DATA LATE. Hence,

the DATA LATE flip-flop cannot be set if a flag character is being transmitted.

The DATA LATE flip-flop is clocked by the leading edge of D7 TCSC MAX H which is generated at the end of each character. If the DONE flip-flop is still set at this time, and a data or control character is being transmitted, the D input of DATA LATE is high. D7 TCSC MAX H clocks DATA LATE and sets it. This causes the SFG flip-flop (print D8) to be cleared at the next TCSC MAX time which in turn clears the Request to Send (RS) flip-flop (pring D15). This turns off the RS line to the modem. The line unit transmits MARKs (idle state) until the message is retransmitted.

4.3.5.6 Transmitter Shift Register (Print D7) - The transmitter shift register (TXSR) is a 74165 parallel-load 8-bit shift register that serializes the information to be transmitted (Figure 4-18). This includes data, BCC characters, Bit Stuff control characters, and DDCMP sync characters.

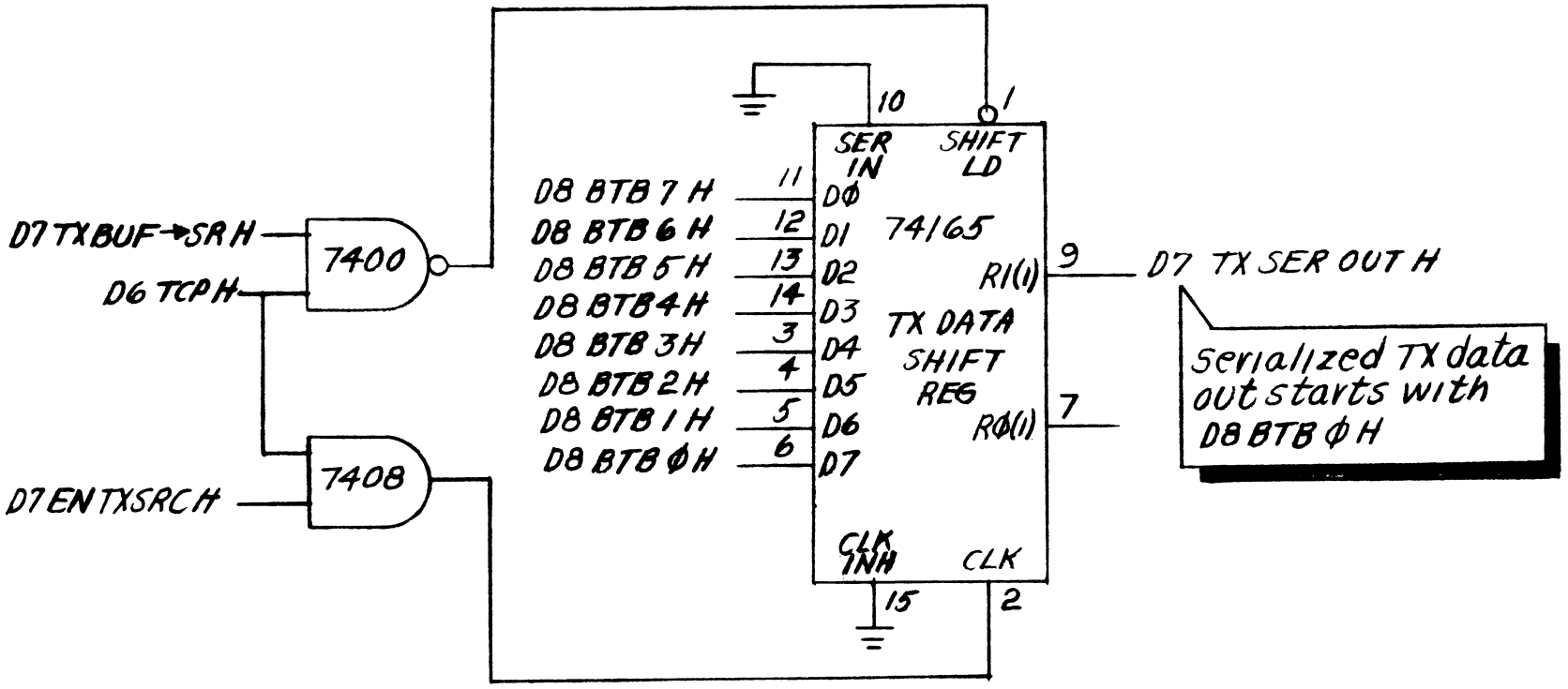


Figure 4-18 Transmitter Shift Register

The TXSR inputs are D8 BTB0 H - D8 BTB7 H which are the seven least significant bits of the Out Data Silo. The TXSR has complementary serial outputs; however, only the true output, D7 TXSER OUT H, is used. The serialized data out is picked off the TXSR least significant bit (pin 6) so the eight data bits are serialized starting with bit D8 BTB0 H.

The clock inhibit input (pin 15) is disabled by connecting it to ground so the clock cannot be inhibited except during loading. The TXSR is clocked by a positive-going edge at its clock input (pin 2). The clock input is connected to the output of a 7408 2-input AND gate. One input to this gate is D7 EN TXSRC H which is asserted by the Data Decode ROM when data is to be transmitted. The other input is clock signal D6 TCP H which is a 200 ns positive pulse that occurs once each bit time.

When the TXSR load input (pin 1) is low, the clock is inhibited and bits D8 BTB0 H - D8 BTB07 H are parallel loaded into the register. The load input is connected to the output of a 7400 2-input NAND gate. One input to this gate is D7 TXBUF$\longrightarrow$SR H which is asserted by the Data Decode ROM when the Out Data Silo is to be loaded. The other input is clock pulse D6 TCP H. When both of these signals are asserted, the load input goes low.

4.3.6 Receiver Logic

The detailed discussion of the receiver logic is divided into six parts as follows.

Discussion	Paragraph
ROMs and RCS Flip-Flop	4.3.6.1
Clock Logic	4.3.6.2
1s Counter and Enabling Logic	4.3.6.3
Shift Register Counter	4.3.6.4
Shift Register and Data Buffer	4.3.6.5
In Data Silo	4.3.6.6

4.3.6.1 ROMs and RCS Flip-Flop

Two read-only memories (ROMs) are the major controlling elements for the receiver. Each one is a 1024 bit TTL ROM (5603 or equivalent) that is organized as 256 words of 4 bits each. The ROMs are identified as shown below.

Name	Print No.
Decode ROM (DR)	D10
Function ROM (FR)	D10

Both enabling inputs (pins 13 and 14) are held low to keep the ROMs enabled constantly while power is applied. The inputs represent an 8 bit binary coded address that selects any one of 256 words (decimal addresses 0-255). The most significant bit is pin 15 and the least significant bit is pin 5. Each word is pre-programmed and is unalterable. When addressed, a specific word always produces the same states at the four outputs.

The circuit schematic for the ROMs and associated logic is contained in prints D10 and D11. A simplified diagram is shown in Figure 4-19.

Both ROMs are enabled by signal D14 GR TEST POINT which is described in Paragraph 4.3.5.1.

In the following discussion, the source and destination of the signals associated with the ROMs and RCS flip-flop are described functionally. Some signals specifically ROM inputs, have relevance only when viewed as a group during a specific point in a receive operation.

Decode ROM

This ROM decodes the protocol selected, recognizes sync characters, flag characters and stuffed 0s. It controls the enabling of the Receiver Shift register clock. The Decode ROM responds to the microprocessor and internal logic as shown in Table 4-4.

Two outputs of the Decode ROM, D10 EN FRM H and D10 ADDRS+SYNC$_{\wedge}$H (RECI), are sent directly to the Function ROM. The third output, D10 EN RSRC H, is an enabling signal for the clock for the receiver shift register and the RSRC counter. The fourth output, D10 FLG RCVD H, is ORed with D14 DDCMP H to provide a Function ROM input.

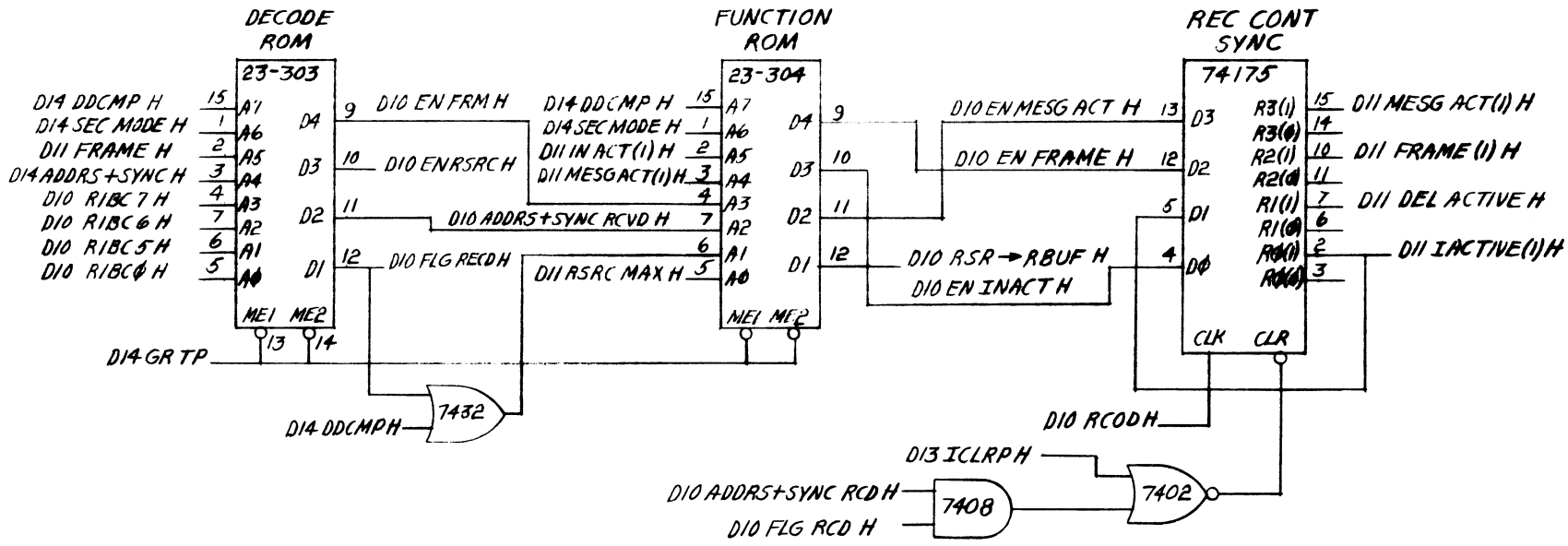


Figure 4-19 Receiver ROMs and Associated Logic

Table 4-4

Receiver Decode ROM Input Signals

Signal	Pin	Source
D14 DDCMP H	15	Microprocessor via bit 0 of Maintenance Register.
D14 SEC MODE H	1	Hardware selectable using a switch in switch pack no. 1.
D11 FRAME (1) H	2	From Function ROM via RCS flip-flop.
D14 ADDRS+SYNC H	3	Output of sync comparator.
D10 R1BC 7 H	4	Output of R1BC Counter.
D10 R1BC 6 H	7	
D10 R1BC 5 H	6	
D10 R1BC 0 H	5	

Function ROM

This ROM interprets the state of the receiver and controls the timing for loading characters in the Receiver Buffer register. The Function ROM responds to the microprocessor and internal logic as shown in Table 4-5.

Table 4-5

Receiver Function ROM Input Signals

Signal	Pin	Source
D14 DDCMP H	15	Microprocessor via bit 0 of Maintenance Register.
D14 SEC MODE H	1	Hardware selectable using a switch in switch pack no. 1.
D11 INACT (1) H	2	From Function ROM via RCS flip-flop.
D11 MESG ACT (1) H	3	
D10 EN FRM H	4	From Decode ROM
D10 ADDRS+SYNC RECD H	7	
Unlabeled	6	OR function of D10 FLG RECD H and D14 DDCMP H.
D11 RSRC MAX H	5	From RSRC Counter.

RCS Flip-Flop (Print D11)

The Receiver Control Synchronization (RCS) flip-flop is a 74175 quad D-type. It stores three signals from the Function ROM. They are: D10 EN FRAME H, D10 EN INACT H, and D10 EN MESG ACT H. Output pin 2 (D11 IN ACT (1) H is fed back to pin 5 as the fourth input). The clock signal for the RCS flip-flop is D10 RCOD L which is a derivative of the modem receiver clock. It is a 200 ns negative pulse that is generated once each bit time. Its positive-going trailing edge clocks the RCS flip-flop.

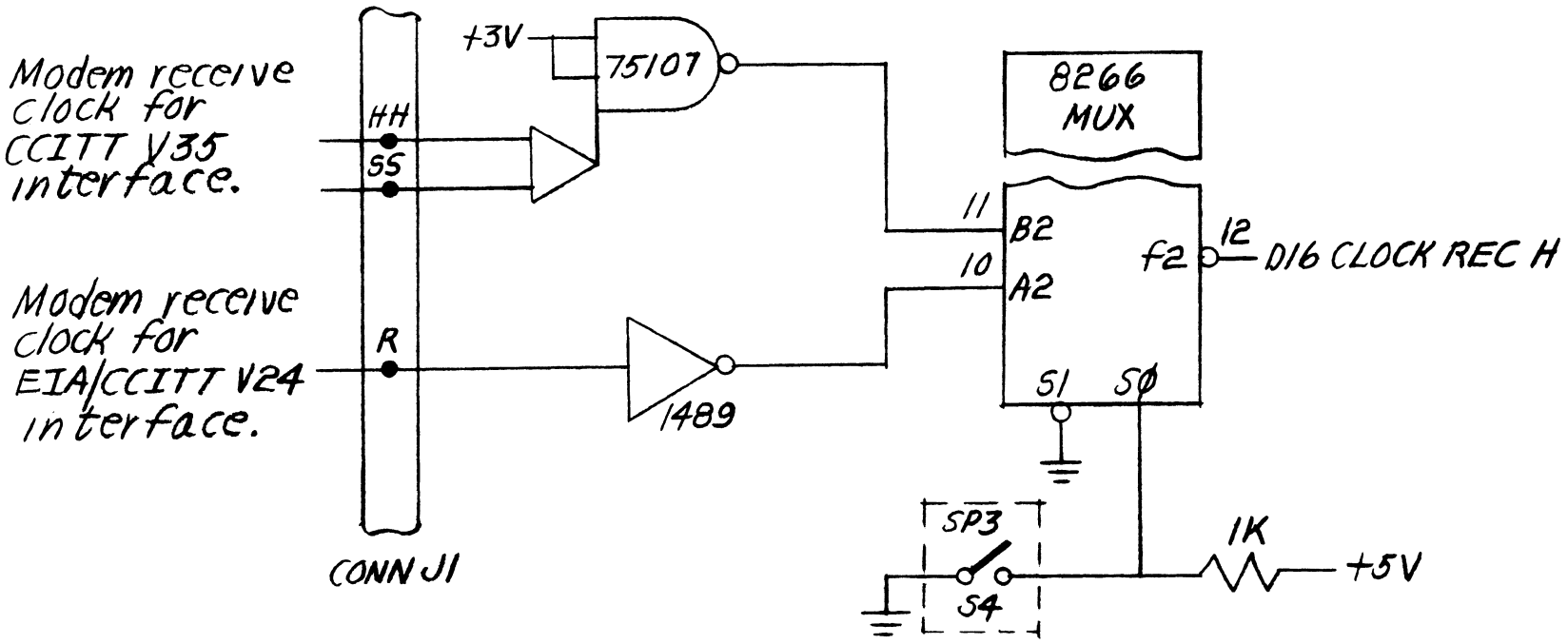
The RCS flip-flop is directly cleared by D14 ICLRP H via a 7402 OR gate. Signal D14 ICLRP H is asserted when the IN CLEAR bit of the In Control register is set or when the microprocessor initiates a general clearing of the line unit.

RCS can also be cleared by an error condition that exists when signals D10 ADDRS+SYNC RECD H and D10 FLG RECD H are asserted simultaneously. The AND function of these two signals appears at the output of a 7408 AND gate and is inverted to directly clear the RCS flip-flop. This condition exists when a Bit Stuff abort sequence (7 or more 1s) is received.

4.3.6.2 Clock Logic - In the user mode, the receiver clock is supplied by the modem. Special logic allows selection of an internal RC clock or single step clock during maintenance. This maintenance clock logic is discussed in Paragraph 4.3.9 Maintenance Logic.

The receiver clock signal from the modem goes to a receiver in the level conversion logic which is shown in print D16 and Figure 4-20. The signal goes to a 1489 receiver for an EIA/CCITT V24 interface or a 75107 two-channel receiver for a CCITT V35 interface. The outputs of these receivers go to an 8266 2-input 4-bit multiplexer. Select input S1 of the mux is connected to ground; therefore, the position of the switch connected to select input S0 determines which input is chosen. With the switch closed (ON), S0 is low and input B (CCITT V35) is selected. With the switch open (OFF), S0 is high and the inverse of input A (EIA/CCITT V24) is selected. The output of the mux is D16 CLOCK RECEIVE L. This signal is sent to one input of the CLK SRC MUX (print D15). The multiplexer output is D15 RX CLK H and can represent the modem receiver clock, single step clock, or internal RC clock as explained in Paragraph 4.3.9.

Figure 4-21 shows the RX clock logic and timing diagram. Clock signal D15 RX CLK L is generated at the output of a 7400 2-input NAND gate. One input of this gate is the clock signal that comes from the CLK SRC mux. The other input comes from the output of another 7400 NAND gate and is the AND function of D15 RS (1) H and D15 HDX (1) H. These two signals are used to blind the receiver by inhibiting the RX clock while transmitting in the half-duplex mode. Signal D15 RS (1) H is used as a qualifying signal because the modem requires the Request to Send (RS) line



SELECT		SELECTED INPUT
S1	S0	
L	L	(B) CCITT V35
L	H	(Ā) EIA/CCITT V24

Figure 4-20 EIA Receiver Clock Conversion Logic

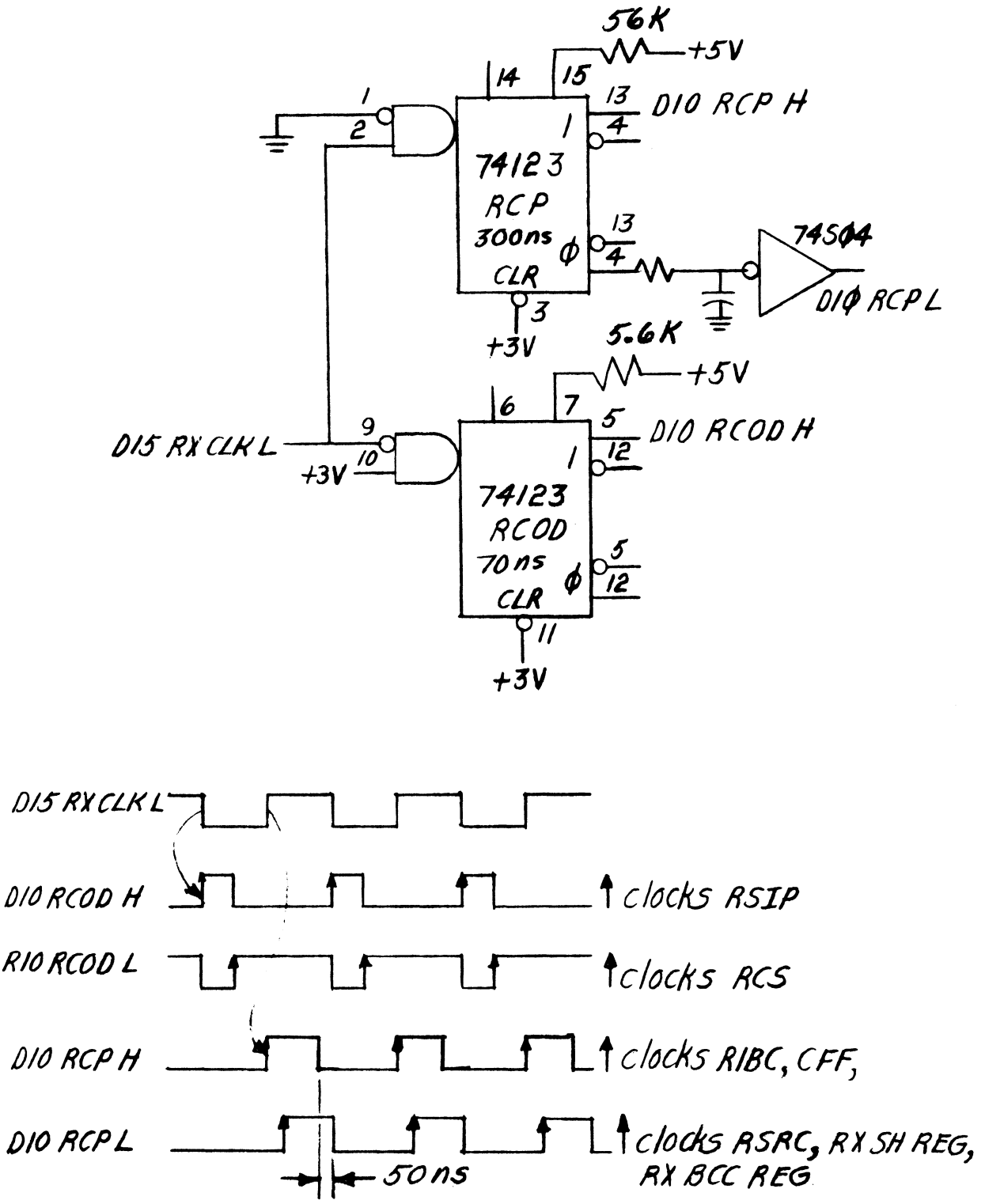


Figure 4-21 Receiver Clock Logic and Timing Diagram

to be on during transmission. This signal comes from the 1 output of the RS flip-flop and is high except when RS is cleared as a result of a data late condition or a CLR OUT condition. When it is desired to operate in the half-duplex mode, the HDX flip-flop is set by the microprocessor and D15 HDX (1) H is asserted. This, in turn, drives D15 RX CLK L high which inhibits the clock.

Clock signal D15 RX CLK L triggers two 74123 1-shots (print D10). The positive-going edge of D15 RX CLK L generates complementary pulses of 300 ns duration which are identified as D10 RCP H and D10 RCP L. The negative-going edge of D15 RX CLK L generates complementary pulses of 70 ns duration which are identified as D10 RCOD H and D10 RCOD L.

Signal D10 RCP H clocks the R1BC counter and the CFF flip-flop. Signal D10 RCPL clocks the RSRC Counter, RX BCC generator, and the Receiver Shift Register. Signal D10 RCOD H clocks the RSIP flip-flop. Signal D10 RCOD L clocks the RCS flip-flop.

4.3.6.3 CFF Flip-Flop and R1BC Counter (Print D10) - The R1BC Counter counts consecutive 1s and is cleared when a received 0 is detected. Some of its outputs are used as inputs to the Decode ROM. They are used to detect Bit Stuff flag characters and stuffed 0s.

The CFF flip-flop looks at the received data before it is shifted into the R1BC counter. From the idle (MARK) state in the Bit Stuff protocol the switch to active reception must start with a 0 to signal the first bit of the flag character (01111110). The CFF

flip-flop enables the R1BC counter only if this action occurs. The CFF flip-flop, R1BC, and associated logic is shown in print D10 and Figure 4-22.

Assume that the line unit is operating in the Bit Stuff protocol user mode and that the receiver line is in the idle state (sending MARKs) using a EIA/CCITT V24 interface.

The following definitions are provided to clarify the logic levels used in this discussion.

Outside the line unit. (Reference signal is EIA REC DATA at the input of 1489 receiver.

SPACE=H=+6 V = logical 0

MARK=L=-6 V = logical 1

Inside the line unit. (Reference signal is D16 REC DATA at the output of 1489 receiver.

SPACE=L=0 V = logical 0

MARK=H=+5 V = logical 1

In the MARK state, EIA REC DATA is low. It is inverted by the 1489 receiver and the 8266 mux. There is no state change through the On Line Loop Select Mux so it appears low as D15 RX DATA H at the D input of the CFF flip-flop. The CFF flip-flop starts cleared. It is clocked once each bit time by D10 RCP H but does

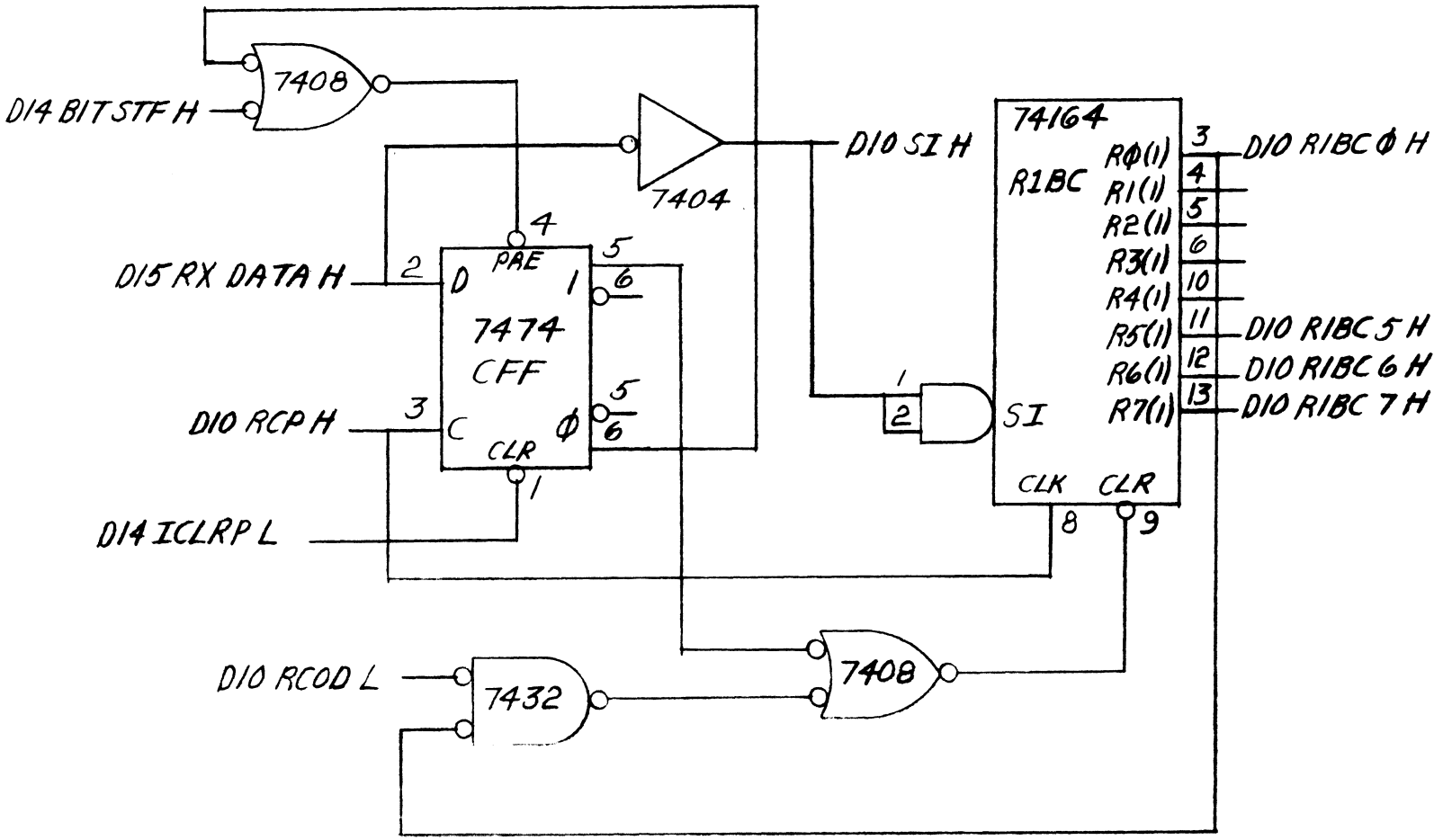


Figure 4-22 CFF Flip-Flop and R1BC Counter

not change state (remains cleared). D15 RX DATA H is inverted and sent to the serial input of the R1BC counter. This counter is a 74164 8-bit parallel-out shift register with a clear input. It is clocked also by D10 RCP H; however, a 1 is not shifted in because the counter is held clear via a 7408 AND gate by the low from the 1 output of the CFF flip-flop.

Assume that the transmitting station starts to send a flag (01111110). When the modem receive data goes to a 0 (SPACE), the D input of the CFF flip-flop goes high and the serial input of the R1BC counter goes low. When clock signal D10 RCP H comes along, both the CFF flip-flop and R1BC counter are clocked. The CFF flip-flop is set and the low from its 0 output is fed back to its preset input (pin 4) via a 7408 AND gate. This locks the flip-flop in the set state until it is directly cleared by D14 CLRP L going low which happens only on initialization or when it is desired to clear the receiver section.

D10 R1BC 0 H is low and D10 RCOD L is high at this time which puts a high on one input of the 7408 AND gate that is connected to the clear input of the R1BC counter. The 1 output of the CFF flip-flop puts a high on the other input of this gate. The output, which is high, inhibits the direct clear input of the R1BC counter. However, now D10 RCOD L comes along and drives the clear input low which directly clears the counter. Nothing happens because the counter is already clear. This action indicates that the R1BC counter is always cleared when a 0 is detected and the D10 RCOD L pulse is generated.

When the modem receive data goes to a 1 (the first 1 of the flag character), a 1 is shifted into the R1BC counter and D10 R1BC 0 H goes high. This inhibits the clear input of the R1BC counter and it is not enabled (driven low) when D10 RCOD L is generated.

Operating in this manner, the R1BC counter counts 1s to recognize a flag character and a 0 that is stuffed after five contiguous 1s.

4.3.6.4 Shift Register Counter - The Receiver Shift Register Counter (RSRC) counts the number of bits in a character, exclusive of stuffed 0s (Bit Stuff protocol). At the last bit, it generates signal D11 RSRC MAX H which goes to the Function ROM as a control input to indicate that the In Data Silo should be loaded with a character.

The RSRC counter is shown in print D11 and Figure 4-23.

The counter is actually a 74165 parallel-load 8 bit shift register. Its MSB is connected to +3 V and all other data inputs are connected to ground. When the load input (pin 1) goes low (FRAME cleared), the clock is inhibited and a 1 is loaded in the counters MSB position (pin 6). The clock inhibit input (pin 15) is connected to ground. The counter is clocked by a positive-going edge at its clock input (pin 2). Complementary serial outputs (pins 9 and 7) are picked off the MSB position. The true serial output (pin 9) is fed back externally to the serial input (pin 10). The serial input is fed internally to the LSB position (pin 11).

In operation, the loaded 1 is recirculated back through the counter and, after eight bits are counted, it resides in the MSB position again. At this time, it asserts D11 RSRC MAX H which is used in the Receiver Function ROM to indicate the end of a received character. D11 RSRC MAX H is actually asserted at the output of a 74S11 3-input AND gate. One input is the counter true output (pin 9). The other two inputs are D11 FRAME (1) H and D10 ENRSRC H and they must be asserted also.

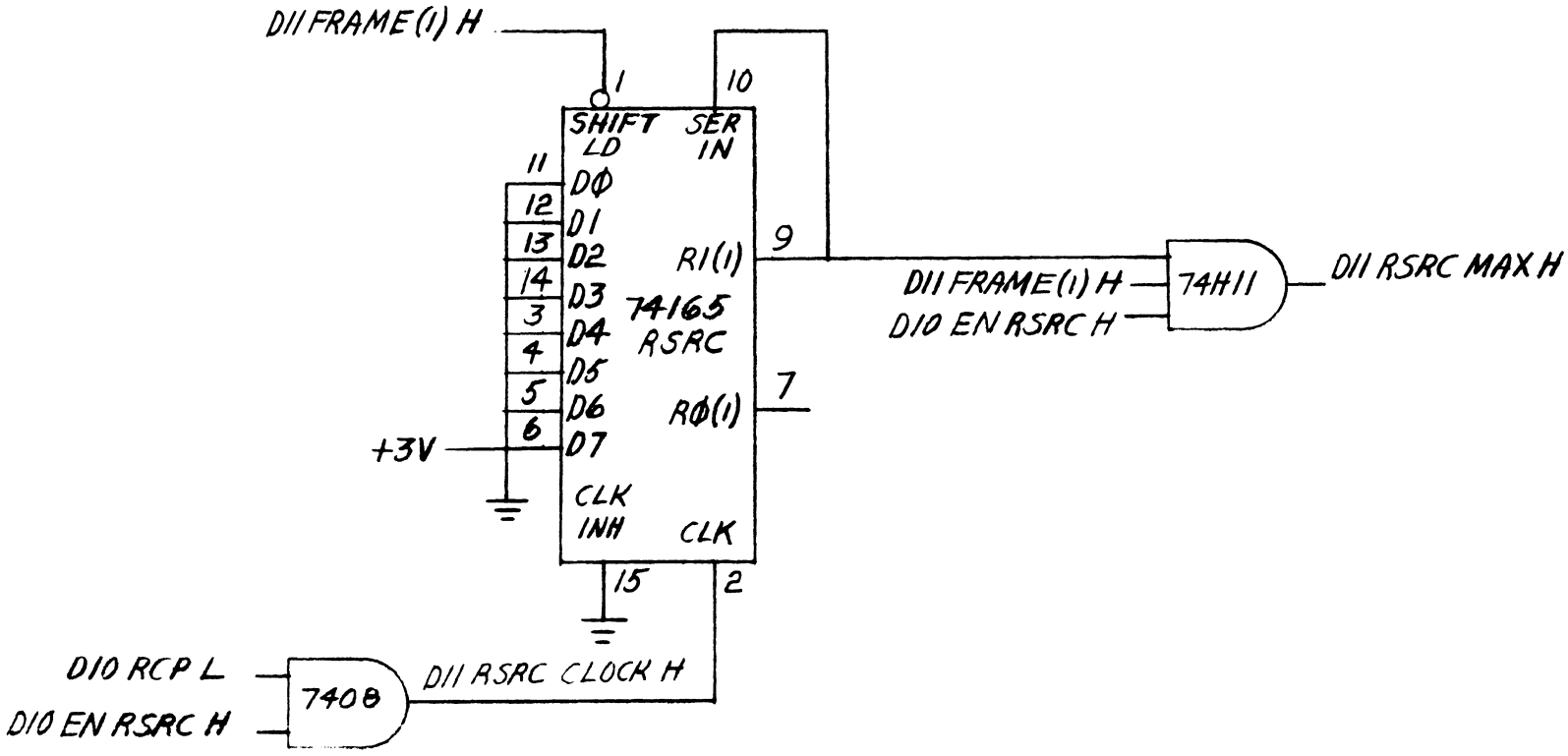


Figure 4-23 Receiver Shift Register Counter

The clock signal for the RSRC counter is D11 RSR CLK H. It is the AND function of D10 RCP L and D10 ENRSRC H. D10 RCP L is a clock signal that occurs once each bit time. D10 ENRSRC H comes from the Receiver Decode ROM. It is not asserted when the receiver logic detects a stuffed 0. By not clocking the RSRC counter when a stuffed 0 is detected, the stuffed 0 is not counted as part of the character.

A detailed discussion of the RSRC counter operation is given below.

1. Assume that the line unit receiver is in the idle state under Bit Stuff protocol discipline. The RCS flip-flop is cleared and D11 FRAME (1) H is low. As a result, the RSRC counter is loaded with a 1 and signal D11 RSRC MAX H is low.

2. The receive line goes active and a flag character is received. When the flag is recognized, the control logic asserts D11 FRAME (1) H. This releases the RSRC load function and activates the clock input. Signal D10 ENRSRC H is also asserted at this time. All three inputs of the 74S11 AND gate are high so D11 RSRC MAX H goes high to indicate the end of the first flag. The Receiver Function ROM recognizes the event but it does not assert D10 RSR→RBUF H which prevents the flag from being loaded into the Receiver Data register.

NOTE

In the Bit Stuff primary mode, all characters subsequent to the last

starting flag are presented to the program. In the Bit Stuff secondary mode, the character following the secondary address is the first character presented to the program.

3. When the first bit of the first data character is received, it is clocked into the shift register. The RSRC counter is also clocked. This moves the 1 from the MSB position (pin 6) to the LSB position (pin 11) which drives D11 RSRC MAX H low. The character is assembled bit by bit in the shift register and the 1 in the RSRC counter is shifted towards the MSB bit by bit. At the eighth bit, the 1 is in the MSB position and D11 RSRC MAX H goes high. This signal goes to the Function ROM which asserts D10 RSR→RBUF H which loads the assembled data character into the Receiver Data register. From here, the character goes to the In Data Silo. The microprocessor decides when to accept the character.

4.3.6.5 Shift Register and Data Buffer - The shift register, data buffer and associated logic is shown in print D11 and Figure 4-24.

The shift register is loaded in serial with an eight bit character. The 8 bit parallel output of the shift register is loaded into the data buffer and out to the microprocessor via the In Data Silo.

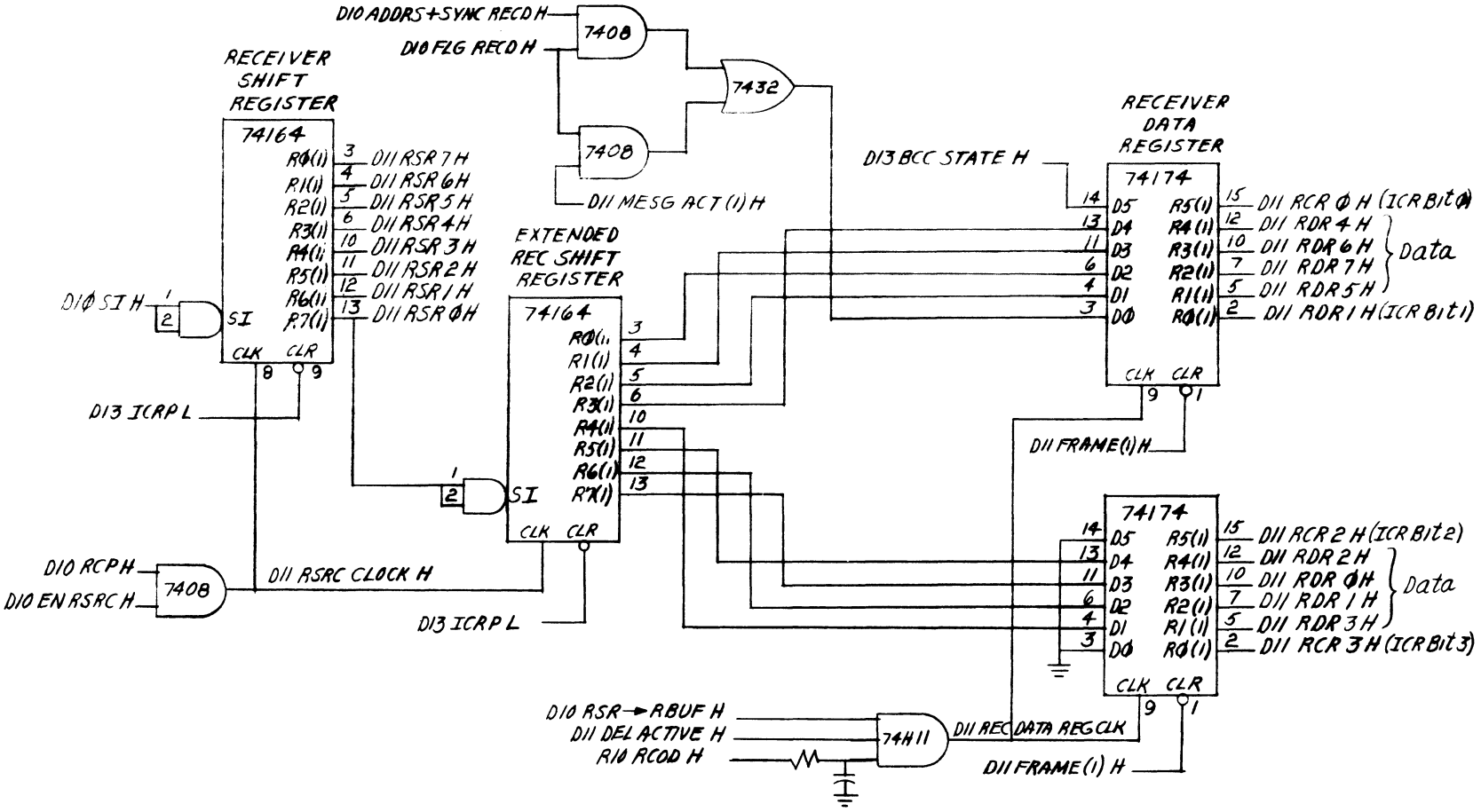


Figure 4-24 Receiver Shift Register and Data Buffer

Actually, two shift registers are used. Received information, as represented by signal D10 SI H, is sent to the serial input of the first shift register. The outputs of this shift register are D10 RSR 0 H - D10 RSR 7 H and they are sent to the comparator on print D14 to be compared with the contents of the Sync Register. This register contains either the sync character (DDCMP protocol) or the line unit secondary address (secondary mode in Bit Stuff protocol).

The 0 bit output of the first shift register (D11 RSR 0 H) is sent to the serial input of the second shift register which is called the extended shift register. This signal is also sent to the RX BCC generator. The outputs of this shift register are sent to the data buffer.

Both shift registers are clocked by D11 RSR CLK H which is the AND function of D10 EN RSRC H and D10 RCP L. Signal D10 EN RSRC H is an enabling signal asserted by the Receiver Decode ROM. Signal D10 RCP H is a derivative of the modem receiver clock and occurs once each bit time. Both shift registers are cleared by D14 ICLRP L which is generated during initialization or when it is desired to clear the receiver only. This is done through the use of the IN CLEAR bit.

The data buffer consist of two 74174 hex D-type flip-flops to provide storage for 12 bits. Eight bits are used for the received character and the remaining 4 are for bits 0-3 of the In Control register. The data buffer is clocked by D11 RX DATA REG CLK H which is the AND function of three signals. One signal is D10 RSR→RDBUF H which

is asserted by the Receiver Function ROM when the data buffer is to be loaded. The second signal is D11 DEL ACTIVE H which is asserted one bit time after D11 INACTIVE (1) H is asserted by the RCS flip-flop. The third signal is D10 RCOD H which is a derivative of the modem receiver clock and occurs about the mid point during each bit time. The data buffer is cleared by D11 FRAME (1) H. This signal comes from the RCS flip-flop and is controlled by the Receiver Function ROM. It is asserted when the receiver is framed.

The four bits of the In Control Register that are stored in the data buffer are identified as outputs D11 RCR 0 H - D11 RCR 3 H. Bits 2 and 3 are reserved for future use so the corresponding data buffer inputs are connected to ground. Bit 0 is BCC MATCH and is represented by signal D13 BCC STATE H from the RX BCC generator error detection logic. Bit 1 is BLOCK END and is used to inform the microprocessor that a terminating flag (Bit Stuff mode) or an abort has been received.

4.3.6.6 In Data Silo - The In Data Silo is one of the eight registers in the line unit. A detailed discussion of the operation of the In Data Silo is contained in Paragraph 4.3.2.2.

4.3.7 CRC Logic

4.3.7.1 General - This discussion covers the operation of the transmitter and receiver cyclic redundancy checking (CRC) logic. This discussion is divided into four sections that are covered in the order shown below.

1. Error detection logic.

2. Transmitter CRC register.

3. Receiver CRC register.

4. Typical transmitter and receiver CRC computations.

Some background information on cyclic redundancy checking is found in Chapter 1 INTRODUCTION.

4.3.7.2 Error Detection Logic - The CRC error detection logic is used only by the receiver; however, both the sending and receiving stations must have their CRC logic enabled. The sending station computes a CRC character for the message and transmits it at the end of the message. The receiving station examines the message plus its CRC character. At the end of the message, the receiving stations' CRC register must contain a specific value to indicate that the message has been received error free. For the DDCMP protocol, the receiver CRC register must read 0; for the Bit Stuff protocol, it must read 016417.

NOTE

To facilitate the use of different CRC codes in the DDCMP and Bit Stuff protocols, the definition of logical 0 and logical 1 are different for each protocol. They are defined as follows.

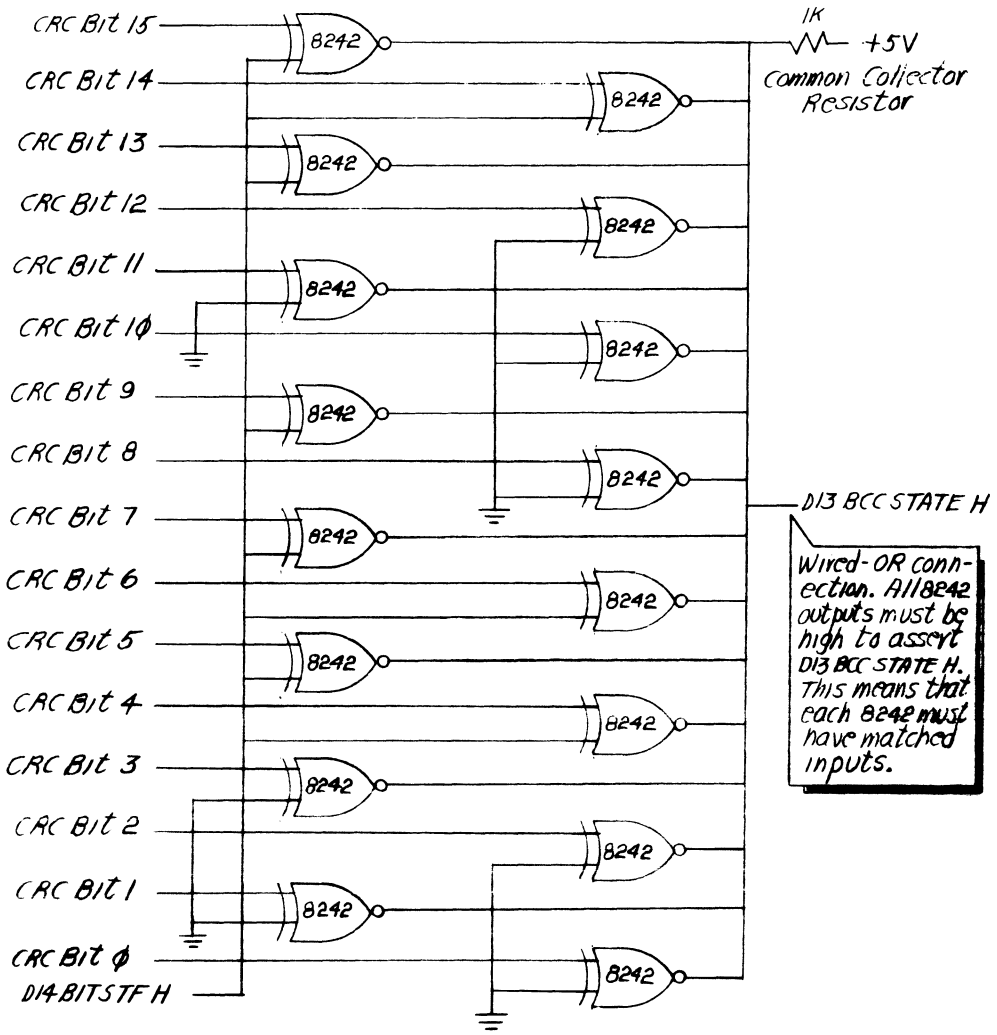
	DDCMP	Bit Stuff
High = +3 V	= Logical 1	Logical 0
Low = 0 V	= Logical 0	Logical 1

The CRC detection logic is shown in print D13 and Figure 4-25.

A comparator circuit is used to check the contents of the receiver CRC register at the end of a message. This circuit consists of 16 8242 2-input exclusive-NOR gates. The output of each 8242 goes high when its inputs match (both high or both low). The 8242 has a bare collector output that allows it to be used in a wired-OR configuration.

Each of the 16 outputs from the receiver CRC register goes to one input of an 8242. For bits, 12, 11, 10, 8, 3, 2, 1 and 0, the other input of the associated 8242 is connected to ground which is low. For bits 15, 14, 13, 9, 7, 6, 5 and 4, the other input of the associated 8242 is connected to signal D14 BIT STF H. This is bit 0 of the Maintenance Register. D14 BIT STF H is high in the SDLC protocol and low in the DDCMP protocol.

In the DDCMP protocol, one input of each 8242 is low because D14 BIT STF H is low. When the message and CRC character has been received, the receiver CRC register must be 0. In this case, both inputs of each 8242 are low so that all 8242 outputs go high. Signal D13 BCC STATE H goes high which indicates that the received message is errorless. If the message is in error, the register reads non-0. This means that at least one 8242 detects no match at its input so that its output goes low. This pulls the +5 V to ground through a common collector resistor and the last stage transistor in the 8242 with mismatched inputs. Now, signal D13 BCC STATE H goes low to indicate that an error exists in the received message. The micro-



Register Contents at End of Message Required to Assert D13 BCC STATE H Which Indicates No Errors.

Bit Stuff Protocol

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Bit No.
0	0	0	1	1	1	0	1	0	0	0	0	1	1	1	1	Binary
0		1		6			4			1			7			Octal

Logical ϕ = H
Logical 1 = L

With D14 BIT STF H signal high, bits 15, 14, 13, 9, 7, 6, 5 and 4 are ϕs. Bits 12, 11, 10, 8, 3, 2, 1 and ϕ are 1s because of ground connections.

DDCMP Protocol

Logical ϕ = L
Logical 1 = H

All bits are ϕ because of ground connections (low) and because signal D14 BIT STF H is low also.

Figure 4-25 CRC Error Detection Logic

indicate that an error exists in the received message. The microprocessor must determine the appropriate response to such a condition. Typically, it requests retransmission of the message. Refer to the Microprocessor Manual or protocol documents for details.

This logic only indicates that the received message is in error. It does not determine the number or location of the errors nor does it have error correcting capability.

In the Bit Stuff protocol, D14 BIT STF H is high; therefore, one input of the 8242 comparators associated with bits 15, 14, 13, 9, 7, 6, 5, and 4 is high. By definition, these inputs are logical 0s. The remaining 8242 comparators (bits 12, 11, 10, 8, 3, 2, 1, and 0), have one input at ground (low). By definition, these inputs are logical 1s. The binary coded octal equivalent of this binary representation is 016417 (bit 15 is MSB). In order to match these inputs, the contents of the receiver CRC register must be 016417 after receiving the message and CRC character. If a match occurs, signal D13 BCC STATE H is asserted to indicate that the received message is errorless.

4.3.7.3 Transmitter CRC Register

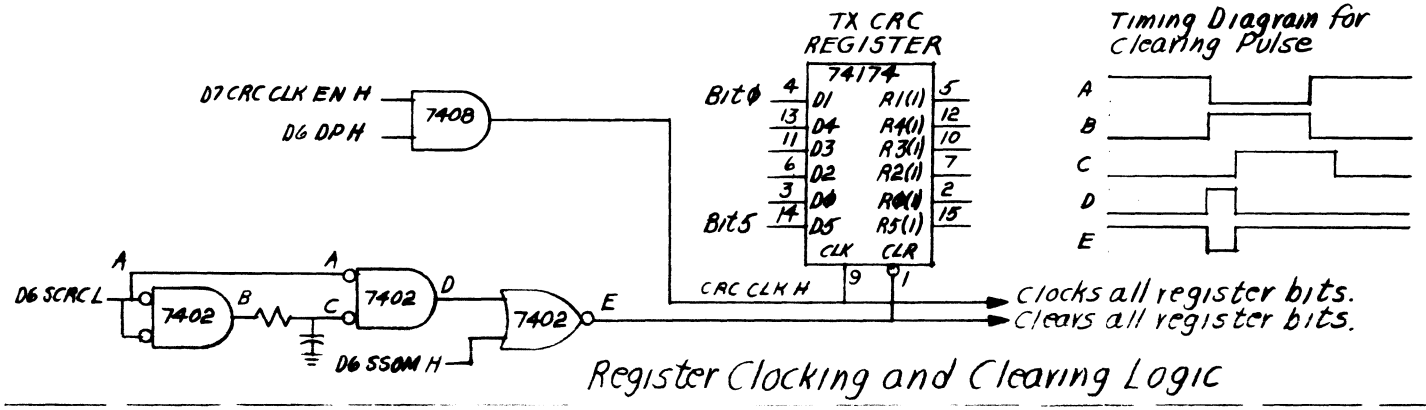
General

The transmitter CRC register consists of a 16 bit shift register, input/feedback logic, and the appropriate number of X-OR gates to operate with the selected CRC codes. Two codes are used: CRC-16 for the DDCMP protocol and CRC-CCITT for the Bit Stuff protocol. CRC-16 requires three X-OR gates; one each for the input (bit 0),

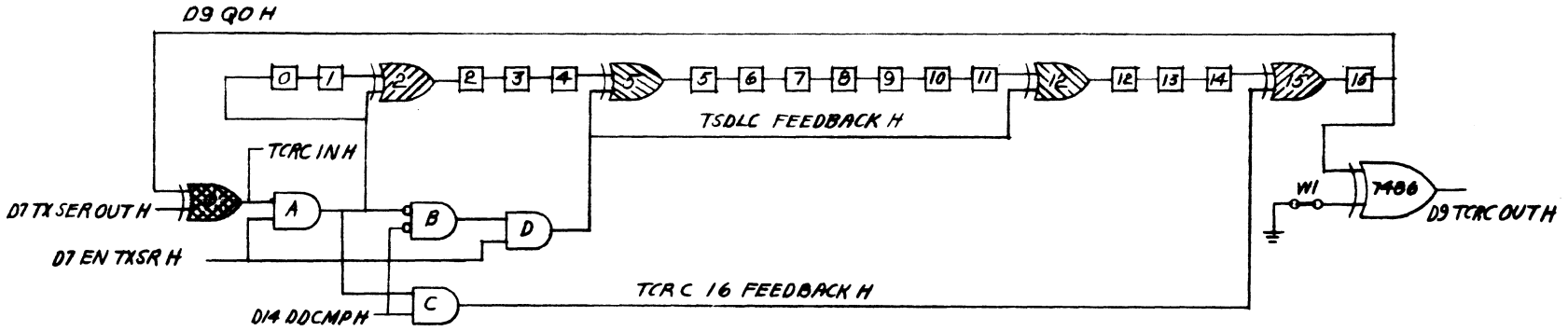
bit 2 and bit 15. CRC-CCITT also requires three X-OR gates; one each for the input (bit 0), bit 5, and bit 12. A total of five X-OR gates are used in the register. The one for the input is used by both protocols. For a given protocol, the input/feedback control logic selects the required X-OR gates to provide the feedback path. For example, in the Bit Stuff mode, the X-OR gates for the input, bit 5 and bit 12 provide X-OR functions. The X-OR gates for bits 2 and 15 act as non-inverting gates and only shift data from one stage to the next.

The transmitter CRC register is shown in print D9. It is also shown in Figure 4-26. In this illustration, the register stages are shown symbolically as numbered squares. Actually, they consist of three 74174 hex flip-flops that are clocked simultaneously and cleared simultaneously. The clock signal is D9 CRC CLK H which is the AND function of D7 CRC CLK EN H and D6 DP H. Signal D7 CRC CLK EN H is asserted by the Transmitter Data Decode ROM when the CRC logic is enabled. Signal D6 DP H is a 200 ns positive pulse that is derived from the modem transmitter clock. This pulse occurs once each bit time.

The clear signal is generated at the output of a 7402 2-input NAND gate that is shown as a logically equivalent negated-input AND gate. This signal is generated in two ways. At the start of a message, the program sets the Start of Message bit (TSOM) for a short time. When it is set, signal D6 SSOM H goes high at the 7402 gate. This gate inverts the signal which drives it low and clears the transmitter CRC register.



Register Clocking and Clearing Logic



NOTES

- Used for both DDCMP and Bit Stuff protocols.
- Feedback path for DDCMP.
- Feedback path for Bit Stuff.
- Register Stage.

Register Input and Feedback Logic

Figure 4-26 Transmitter CRC Register

Signal D6 SCRC is enabled by the Transmitter Function Decode ROM at the proper time during transmission, if a CRC computation is desired. This signal goes to the input of a pulse generator comprised of two 7402 gates, a resistor and capacitor. This pulse generator provides a 100 ns positive pulse at its output only on the negative-going transition of D6 SCRC. With D6 SCRC high, the pulse generator output is low. The other input of the 7402 gate is low also because TSOM is cleared very early in the transmission; that is, D6 SSOM H is low. With both inputs low, the output of the 7402 gate is high; therefore, the clearing signal is inhibited.

After the accumulated 16 bit CRC character has been transmitted, the transmitter logic clears signal D6 SCRC which generates a positive pulse at the pulse generator output. This pulse is inverted and clears the CRC register. In the DDCMP and Bit Stuff modes, it is necessary to force clear the CRC register at this time because the next character may be part of a sequence that should be included in another CRC computation.

Input/Feedback Control Logic (DDCMP Mode)

Operation of the input/feedback control logic in both modes (DDCMP and Bit Stuff protocol) is discussed using Figure 4-26. For ease of discussion, the X-OR gates are identified numerically (0, 2, 5, 12 and 15); and the other gates are identified alphabetically (A, B, C and D).

In the DDCMP mode, signal D14 DDCMP H is asserted. This puts a high on one input of AND gate C and negated-input AND gate B. The other input of gates B and C is the output of AND gate A which is the AND function of D7 EN TXSR H and D9 TCRC IN H. Signal D7 EN TXSR H is asserted by the Transmitter Data Path Control ROM when the CRC function is enabled. Therefore, the Transmitter CRC Register is active and is computing a CRC on the message being transmitted. Signal D9 TCRC IN H comes from exclusive-OR gate 0 and is the X-OR function of D9 TXSER OUT H and D9 TXCRC OUT H. Signal D9 TXSER OUT H is the output of the Transmitter Shift Register and is the data being transmitted. Signal D9 TXCRC OUT H is the output of the CRC register (bit 15). The X-ORed states of D9 TCRC IN H are sent to the first stage (bit 0) of the CRC register. They also pass through gates A and C to X-OR gates 2 and 15. The output of gate B, and hence the output of gate D, is held low by D14 DDCMP H. This inhibits the X-OR function of X-OR gates 5 and 12 and they act as non-inverting gates. When the CRC character has been accumulated and it is time to transmit the CRC character, D7 EN TXSR H goes low which drives the input of the CRC register low. Thus, the transmitter CRC is not active while its contents are being transmitted.

In summary, the CRC register starts cleared (all 0s) by the assertion of D6 SSOM (1) H. The state of D14 DDCMP H, which is high, sets up the X-OR gates so that the register accumulates a CRC character in accordance with code CRC-16. The feedback path is set up by D9 TCRC IN H prior to the register being clocked. When all the data

in the transmitted message has been operated on, the register contains the CRC character. At this point, the transmitter control logic drives D7 EN TXSR H low and the CRC character is transmitted after the last data character. Remember that while the data is being operated on by the CRC register to accumulate a CRC character, it is being transmitted simultaneously without alteration. The CRC character is transmitted by being serially shifted from the output of the CRC register to the Transmitter Decode ROM. All X-OR gates are disabled and the existing data is not altered during the process. When the CRC character has been transmitted, the high-to-low transition of D6 SCRC H clears the CRC register. The only contribution that the CRC register makes to the transmitted data is generation of the CRC character which the receiving station uses to determine whether or not the message has been received errorless.

Input/Feedback Control Logic (Bit Stuff Mode)

In the SDLC mode, D14 DDCMP H is low which qualifies gate B and disqualifies gate A. Qualification of gate B, with D7 EN TXSR H asserted, sets up the feedback path for operation with code CRC-CCITT by enabling X-OR gates 5 and 12. The low output from gate C goes to X-OR gates 2 and 15 and they operate as non-inverting gates.

The CRC register starts cleared (all 1s in the Bit Stuff mode). This allows detection of the addition or deletion of 0s at the leading end of the message due to erroneous flag characters. All bit positions except 0, 5, and 12 receive the data from the previous stage of the

CRC register without modification by the X-OR function. Except for the change in the feedback path, operation is the same as that described in the DDCMP example. The transmitter control logic complements the CRC character before sending it. This allows the detection of the erroneous addition or deletion of 0s at the trailing end of the message.

4.3.7.4 Receiver CRC Register - The configuration of the Receiver CRC Register is exactly like the Transmitter CRC Register, with respect to the X-OR feedback paths. The input/feedback logic, clocking logic, and clearing logic are different. The Receiver CRC Register is shown in print D13. It is also shown in Figure 4-27. For ease of discussion, the X-OR gates are identified numerically (0, 2, 5, 12 and 15); an- the other gates are identified alphabetically (A, B and C).

The clock signal for the CRC register is D11 RSR CLOCK H which is the AND function of D10 EN RSRC H and D10 RCP L. Signal D10 EN RSRC H is asserted by the Receiver Decode ROM when information is being received. Signal D10 RCP L is a 70 ns positive pulse that is derived from the modem receiver clock. This pulse occurs once each bit time.

The register is cleared by signal D11 IN ACTIVE (1) H which comes from the RCS flip-flop and is bit 6 of the Input Control Register. This bit is asserted by the receiver control logic when the line unit is in the data reception mode. This means that it is asserted

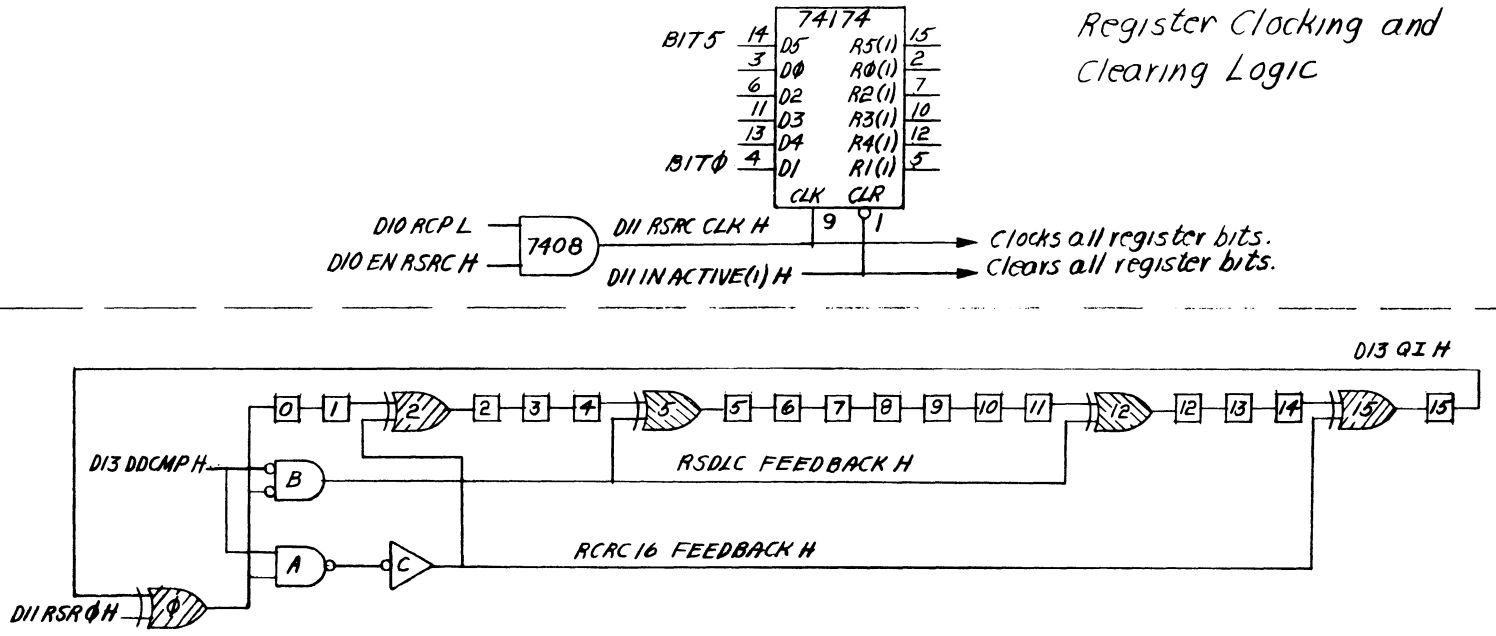


Figure 4-27 Receiver CRC Register

upon receipt of the first non-sync or non-flag character; therefore at the beginning of a message it is not asserted (low) and the Receiver CRC register is cleared.

Input/Feedback Control Logic (DDCMP Mode)

Operation of the input/feedback control logic in both modes (DDCMP and Bit Stuff) is discussed using Figure 4-27.

In the DDCMP mode, signal D14 DDCMP H is asserted. This puts a high on one input of NAND gate A and negated-input AND gate B. The output of gate B is held low which makes X-OR gates 5 and 12 perform as non-inverting gates. The output of gate A can be high or low depending on the state of D11 RSR 00 H. This allows X-OR gates 2 and 15 to perform the X-OR function. This sets up the feedback path for code CRC-16 in the DDCMP mode. The input to the register is D11 RSR 00 H which is the bit 0 output of the Receiver Shift Register.

In summary, the state of D11 DDCMP H conditions the input logic to set up the feedback path to conform to code CRC-16. All data and the received CRC character are included in the CRC computation. At the end of the message, the Receiver CRC Register should read all 0s. This indicates reception of an errorless message.

Input/Feedback Control Logic (Bit Stuff Mode)

In the Bit Stuff mode, D14 DDCMP H is low which qualifies gate B and disqualifies gate A. Qualification of gate B sets up the feedback path for operation with code CRC-CCITT by enabling X-OR gates 5 and

12. Disqualification of gate A, keep a low on input of X-OR gates 2 and 15 which makes them perform as non-inverting gates.

In summary, the state of D11 DDCMP H conditions the input logic to set up the feedback path to conform to code CRC-CCITT. All data and the CRC character (called the FCS character in SDLC protocol) are included in the CRC computation. The sending station complements the FCS character before transmitting it. After receiving the data and FCS character, the Receiver CRC Register must read 016417 to indicate an errorless message.

4.3.7.5 Typical CRC Accumulation - Figure 4-28 shows typical transmit and receive CRC accumulations in the Bit Stuff mode.

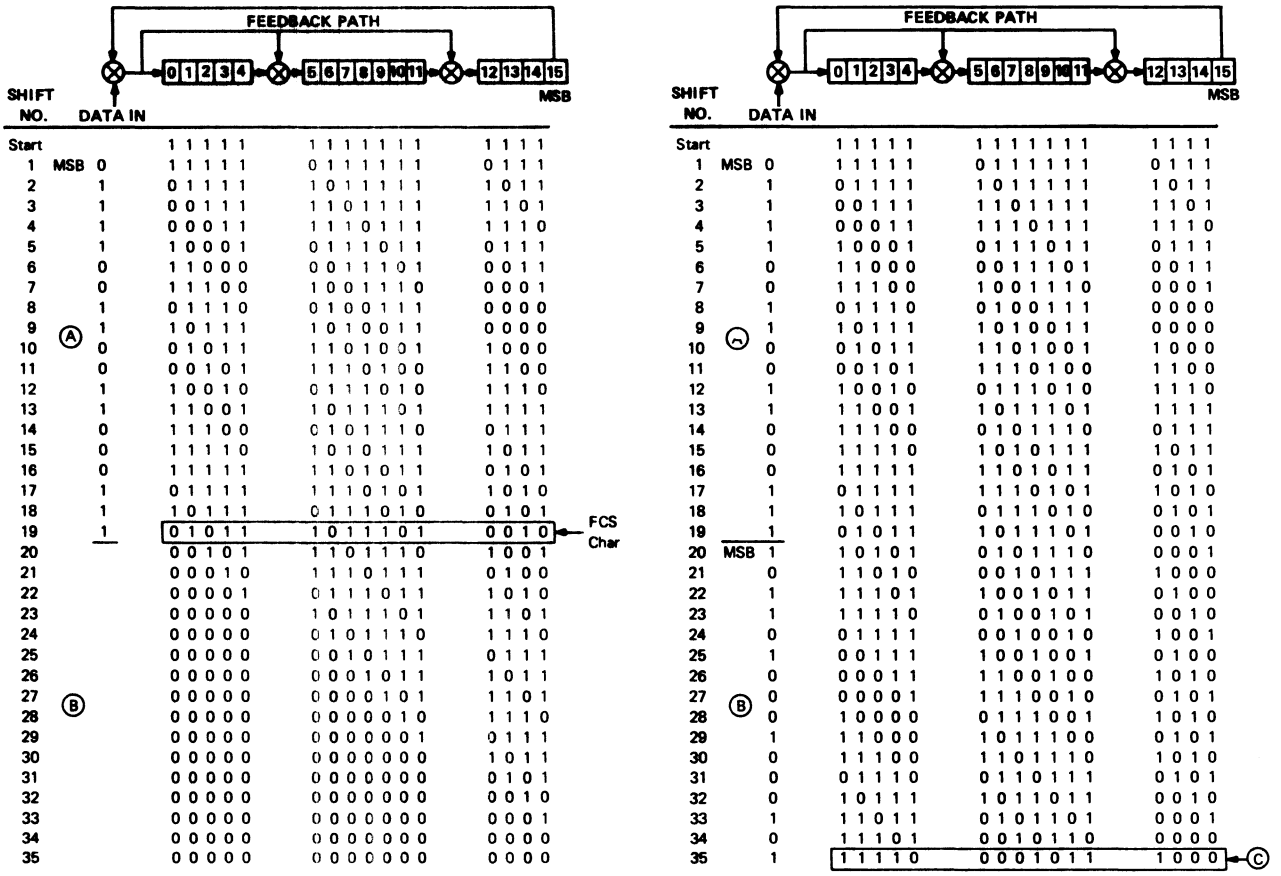
Remember the following facts concerning CRC operation in the Bit Stuff mode.

1. In the Receiver and Transmitter registers, a high signal represents logical 0 and a low signal represents logical 1.

2. Both registers start cleared (all 1s).

3. After the CRC check character (FCS) has been accumulated in the transmit mode, it is transmitted in complementary form.

4. In the receive mode, after reception of the data and FCS character, the Receiver CRC Register must read 016417 (LSB right justified) or else the message is in error.



Transmit CRC Accumulation (SDLC)

Receive CRC Accumulation (SDLC)

NOTES

(A) Transmission of 19 bit data character showing accumulated FCS character.

(B) Transmission of 16 bit FCS character showing 0s being shifted into register

NOTES

(A) Reception of 19 bit data character.

(B) Reception of complement of FCS character.

(C) Contents of register at end of message. Contents equal 016417_8 (LSB right justified).

Figure 4-28 Typical Transmit and Receive CRC Accumulation

4.3.8 Data Set Interface Logic (M8201 Only)

4.3.8.1 General

The data set interface logic performs signal conversion between the TTL logic levels used in the line unit and the EIA logic levels used outside the line unit. The logic levels are defined below.

TTL Levels (Inside the line unit.)

High = +5 V = logical 1

Low = 0 V = logical 0

EIA Levels (Outside the line unit.)

High = +6 V = logical 0

Low = -6 V = logical 1

This logic supports two different interfaces. One is EIA/CCITT V24 which uses single ended signals. The other is CCITT V35 which uses double ended or differential signals.

In the EIA/CCITT V24 interface, signals from the modem are handled by 1489 receivers. Each receiver has an external response control input, consisting of a resistor and capacitor, that sets the threshold for level conversion. The signals to the modem are handled by 1488 drivers.

In the CCITT V35 interface, signals from the modem are handled by 75107 two-channel receivers. Each receiver has differential inputs that are converted to a single output. The signals to the modem are handled by 75110 two-channel drivers. Each driver has a single input

that is converted to differential outputs.

The level conversion logic is shown in print D16.

4.3.8.2 Conversion of Signals from the Modem - The signals from the modem that are converted to TTL levels are shown in Table 4-6.

Table 4-6

Signals from the Modem

Signal	1489 Receiver	75107 Receiver
DATA SET READY	Yes	No
CLEAR TO SEND	Yes	No
RING	Yes	No
XMIT CLOCK	Yes	Yes
SERIAL DATA IN	Yes	Yes
REC CLOCK	Yes	Yes

The 1489 receiver inverts the signal that it is converting. For EIA control signals, a high state indicates an ON condition.

The outputs of the 1489 receivers for the DATA SET READY, CLEAR TO SEND, and RING signals are inverted again to produce D16 MODEM RDY H, D16 CS H, and D16 RING H, respectively. These signals are part of the Modem Control Register and they are read by the program to determine the status of the modem.

In addition, the outputs of the receivers for DATA SET READY and CLEAR TO SEND are ANDed at a negated-input AND gate to assert D16 SEND f H only when both these signals are ON (high). SEND is an enabling signal for the transmitter and must be asserted in order to turn on the transmitter. Two jumpers (W2 and W3) are provided in the output of the receiver associated with DATA SET READY (Figure 4-29). With W2 installed and W3 removed, D16 MODEM RDY H can be asserted or non-asserted. For those applications that require DATA SET READY to be permanently ON, W3 is installed and W2 is removed. This holds signal D16 MODEM RDY H asserted.

Signals XMIT CLOCK, SERIAL DATA IN, and REC CLOCK from the modem are each sent to a pair of receivers: 1489 for the EIA/CCITT V24 interface and 75107 for the CCITT V35 interface. An 8266 quad 2-input multiplexer is used to select between the two interfaces. For each of these signals, there are two possible outputs; one from the 1489 receiver and one from the 75107 receiver. The 1489 outputs go to the multiplexer A inputs and the 75107 outputs go to the multiplexer B inputs. Select input S1 is connected to ground; therefore, the position of the switch connected to select input S0 determines which input is chosen. With the switch closed (ON), S0 is low and input B (CCITT V35) is selected. With the switch open (OFF), S0 is high and the inverse of input A (EIA/CCITT V24) is selected. The inversion of A in the multiplexer compensates for the non-inverting action of the 75107 receiver.

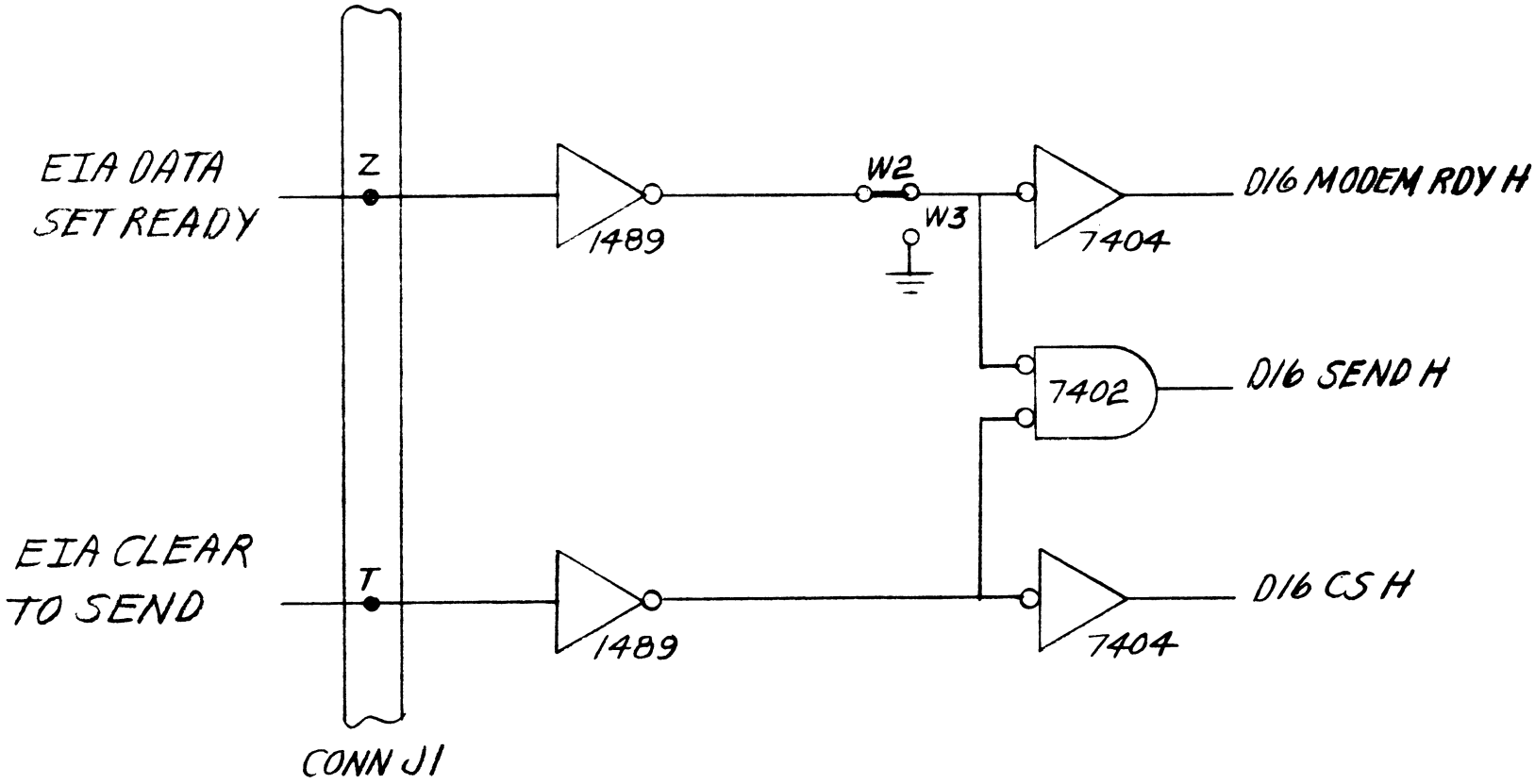


Figure 4-29 Conversion Logic for DSR and CS Signals

4.3.8.3 Conversion of Signals to the Modem - The signals to the modem that are converted to EIA levels are shown in Table 4-7.

Table 4-7

Signals to the Modem

Signal	1488 Driver	75110 Driver
D15 DTR H (Data Terminal Ready)	Yes	No
D15 RTS H (Request to Send)	Yes	No
D7 TDO H (Transmitter Data)	Yes	Yes
D15 SECS H (External Clock)	Yes	Yes

The drivers convert the signals to EIA logic levels. The 1488 drivers supply single-ended output signals and the 75110 drivers supply differential output signals.

Two jumpers (W4 and W5) are provided in the input to the RTS driver. With W4 installed and W5 out, assertion of the RTS signal is controlled by the RS flip-flop (print D15). With W5 installed and W4 out, the RTS signal is held asserted.

Signal D15 SECS H is the output of the internal RC clock that is used during servicing of the line unit. D15 SECS H is turned on and off by a switch in package SP3 (print D15).

4.3.9 Maintenance Logic

4.3.9.1 General - The line unit can be operated in three maintenance modes during servicing. The modes are described below.

1. Internal Maintenance Mode - This mode provides a means for analyzing ninety percent of the line unit without disconnecting it from the modem (M8201) or the coaxial cable (M8202). Level converters and the cable cannot be checked in this mode.

   Single step clocking is provided by the diagnostic program via the microprocessor.

2. System Test Mode - Clocking is supplied by the line unit RC clock. In this mode, the line unit may remain connected to the modem.

3. External Maintenance Mode - For the M8201 line unit, the modem must be disconnected and the H325 test connector must be connected to the BC05-25 cable. In this mode, the line unit plus the conversion logic and the modem cable are checked. Clocking is supplied by the 10 kHz internal clock which is turned around in the H325 test connector to simulate the modem transmit and receive clock.

For the M8202 line unit, the coaxial cables must be disconnected and the 12-12528 coaxial adapter must be used to connect the pig-tail coaxial cables together. Clocking is supplied by the integral modem.

The maintenance logic consists of an RC clock and two multiplexers to select the proper source for the data, clock, and control signals.

The logic is shown in print D15 and Figure 4-30.

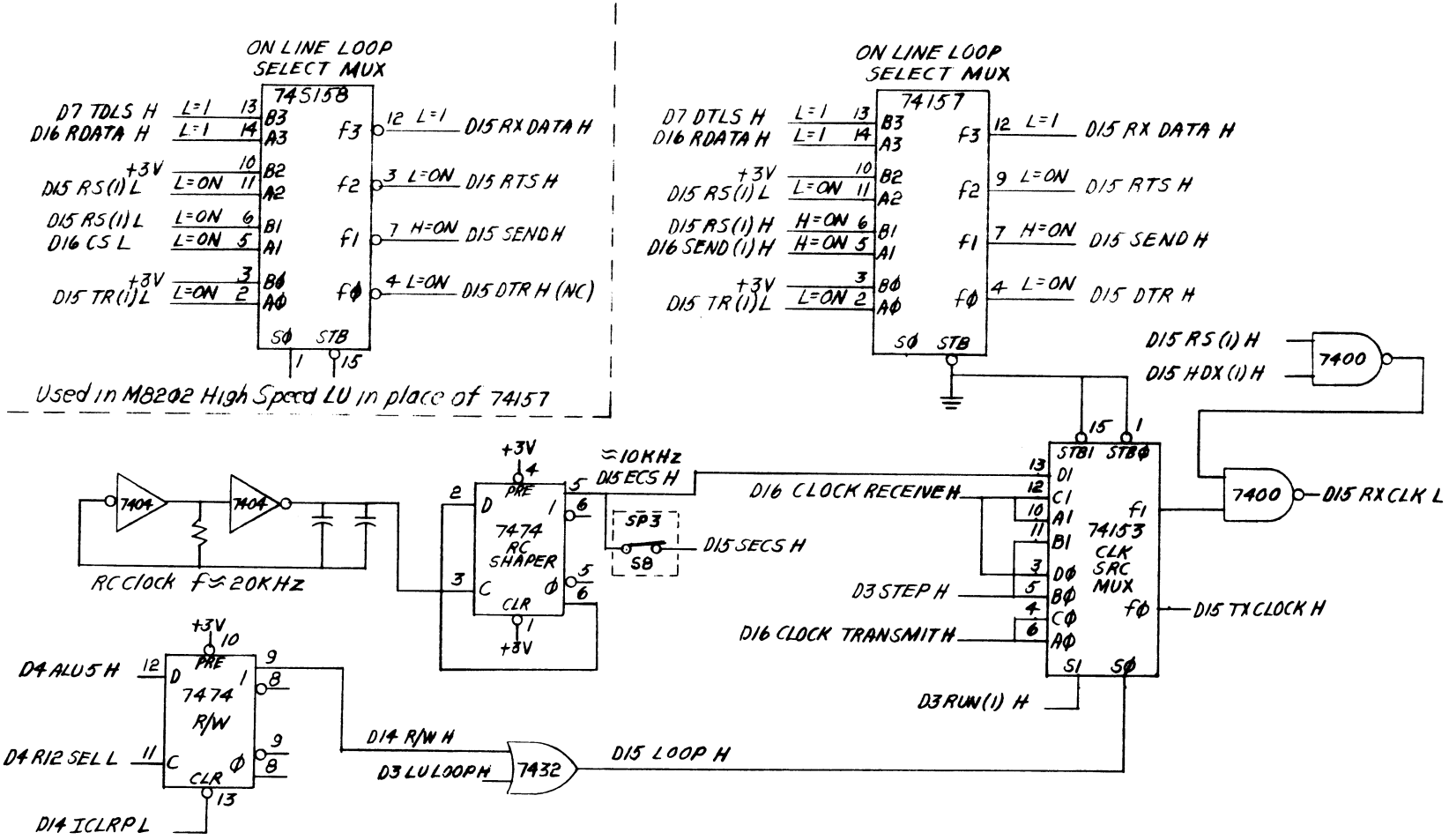


Figure 4-30 Maintenance Logic

4.3.9.2 RC Clock - The RC clock consists of two 7404 inverters and feedback capacitors and resistors. It is a free running 20K Hz clock that starts when power is applied to the line unit and stops only when power is removed.

The output of the RC clock goes to the clock input of the RCC SHAPER flip-flop. The 0 output of this flip-flop is connected to its D input so it divides the RC clock output by two. The flip-flop also shapes the RC clock output. The actual RC clock is the 1 output of the RCC SHAPER flip-flop which is a 10K Hz symmetrical square wave called D15 ECS H. This signal goes through a switch and on to the input of a 1488 driver and a 7510 driver. When the H325 test connector is installed for servicing, the output of the 1488 driver (EIA/CCITT V24 interface) is turned around and simulates the modem transmitter and receiver clock signals. A different cable and test connector are required for the CCITT V35 interface.

Signal D15 ECS H also goes to an input of the CLK SRC multiplexer.

4.3.9.3 Maintenance Multiplexers - Two multiplexers are used in the maintenance logic.

ON LINE LOOP SEL Multiplexer

The ON LINE LOOP SEL mux controls the source of received data to the receiver control logic and the state of three control signals: SEND, Request to Send (RTS) and Data Terminal Ready (DTR).

These four signals are outputs of the ON LINE LOOP SEL mux which is a 74157 quad 2-input multiplexer. The mux strobe input is connected to ground which keeps the mux enabled. The select input is connected to the output of a 7402 (7432) 2-input NOR gate; therefore, the input signals to this gate controls the selection of the mux inputs. These signals are D3 LU LOOP H and D14 R/W H. Signal D3 LU LOOP H is controlled by the microprocessor. The microprocessor asserts D3 LU LOOP H to put the line unit in the maintenance mode. Signal D14 R/W H is bit 5 of the In Control Register and can be used also to put the line unit in the maintenance mode. D14 R/W H comes from the 1 output of a 7474 flip-flop that is controlled by the microprocessor.

In the user mode, neither D14 R/W H nor D3 LU LOOP H are asserted so the S0 input of the ON LINE LOOP SEL mux is low which selects input A. The following events occur.

1. D16 SEND (1) H (input A1) is high because Data Set Ready and Clear to Send from the modem are ON (high). This asserts D15 SEND H at mux output f1. This signal must be high to activate the transmitter.

2. D15 RS (1) L (input A2) is low because the transmitter control logic has set the RS flip-flop. This drives D15 RTS H low at mux output f2. This signal is inverted by á 1488 driver to put a high on the EIA Request to Send line. This signal must be ON (high) to condition the modem for transmission.

3. D16 RDATA H (input A3) is selected. This is the received data from the modem. It becomes D15 RX DATA H at mux output f3. This signal goes to the receiver control logic.

4. D15 DTR (1) L (input A0) is low because the microprocessor has set the DTR flip-flop. This drives D15 DTR H low at mux output f0. This signal is inverted by a 1488 driver to put a high on the EIA Data Terminal Ready line. This signal must be ON (high) to prepare the modem to be connected to the communications channel.

In the maintenance mode, the processor asserts either D3 LU LOOP H or D14 R/W H. This drives the S0 input of the ON LINE LOOP SEL mux high which selects input B. The following events occur.

1. D15 RS (1) H (input B1) is high because the transmitter control logic has set the RS flip-flop. This asserts D15 SEND H at mux output f1 to activate the transmitter.

2. Input B2 is connected to +3 V which drives D15 RTS H high at mux output f2. This is the OFF state for the EIA Request to Send line.

3. Input B3 is connected to D7 TDLS H which is data to be transmitted. This means that the data to be transmitted (D7 TDLS H) is used as the received data (D15 RX DATA H at mux output f3).

4. Input B0 is connected to +3 V which drives D15 DTR H high at mux output f0. This is the OFF state for the EIA Data Terminal Ready line.

The above discussion covers the 74157 ON LINE LOOP SEL mux for the low speed line unit (M8201). A similar mux is used in the high speed line unit (M8202). It is a 74S158 mux that is functionally equivalent to the 74157 except that the outputs are inverted.

Because there is no level conversion logic in the M8202, there is NO SEND input to the mux. D15 SEND H is a mux output but its associated inputs (A1 and B1) are different. In the user mode, input A1 is selected. This is D16 CSL from the integral modem which is low. The mux inverts this signal to assert D15 SEND H. In the maintenance mode input B1 is selected. This is D15 RS (1) L from the RS flip-flop and it is low. The mux inverts this signal to assert D15 SEND H.

CLK SRC Multiplexer

The CLK SRC mux controls the source of the transmitter and receiver clocks during normal operation and servicing of the line unit. The CLK SRC mux is a 74153 dual 4 line-to 1 line multiplexer. Both strobe inputs are connected to ground which keep both sections of the mux enabled. Select input S0 (LSB) is controlled by D3 LU LOOP H or D14 R/W H. Select input S1 (MSB) is controlled by D3 RUN (1) H from the microprocessor. Output f0 is D15 TX CLOCK H which is the clock signal for the transmitter control logic. Output f1 goes to

one input of a 7400 2-input NAND gate. The other input of this gate represents (D15 RS (1) H) (D15 HDX (1) H). The output of the gate is D15 RX CLK L which is the clock signal for the receiver control logic. This gate inhibits the receiver clock only when half duplex operation is selected. A truth table for the CLK SCR mux is shown below.

RUN S1	LOOP/RW S0	INPUT SELECTED	OPERATING MODE
L	L	(A) Modem clocks D16 CLOCK TRANSMIT H and D16 CLOCK RECEIVE	User
L	H	(B) Single step clock D3 STEP H.	Internal Maintenance
H	L	(C) Modem clocks D16 CLOCK TRANSMIT H and D16 CLOCK RECEIVE simulated by RC clock.	*External Maintenance
H	H	(D) Internal RC clock D15 ECS H.	System Test

*Test connector H325 must be used. RC clock is used to simulate modem clocks.

4.3.10 Initialization Logic

The initialization logic is used to clear the receiver section and transmitter section separately or simultaneously. This logic is shown in print D14.

For each section, a 74123 one-shot generates complementary pulses that are the clearing signals. Each one-shot is triggered by a negative-going edge at its input. The output pulses are 400 ns in duration.

The microprocessor can clear the receiver and transmitter sections simultaneously by driving signal D3 CLEAR L. This signal is inverted by a 7404 inverter and sent to one input each of two 7402 NOR gates. The low outputs from these gates trigger the one-shots.

The microprocessor can clear the receiver section or the transmitter section separately by driving D4 ALU 7 L low and addressing the In Control Register for the receiver or the Out Control Register for the transmitter.

For example, assume that it is desired to clear the receiver section. The microprocessor drives signal D4 ALU 7 L low. This signal goes to one input of negated-input AND gate (7402). The microprocessor addresses the In Control Register and the register decoding logic drives D4 R12 SEL L low. This signal goes to the other input of this gate. The output of the gate goes high and is inverted by another NOR gate to trigger the one-shot that generates D4 ICLRP L.

4.3.11 Integral Modem (M8202 Only)

4.3.11.1 General Information - The DMC11-MA and DMC11-MD Line Units each contain an integral modem. The modem circuitry is located on the corner of the module above the cutout section.

The modem for the DMC11-MA version operates at 1M bps up to a distance of 6000 feet. The DMC11-MD version operates at 56K bps up to a distance of 18,000 feet. Each version requires Belden 8232 coaxial cable or equivalent.

The modem incorporates diphase (double frequency) modulation with non-return-to-zero (NRZ) coding. Transmitted or received data is identified by the number of signal transitions that occur during a bit time. A SPACE (logical 0) is identified by two transitions per bit time. A MARK (logical 1) is identified by one transition per bit time.

The transmitter clock is generated by an RC oscillator. The amplitude of the transmitted signal is 4V peak-to-peak.

The receiver clock is recovered from the received signal which should be 150 mV peak-to-peak minimum.

4.3.11.2 Functional Description - The functional description discusses the modem operation at the block diagram level. Figure 4-31 is a simplified block diagram of the modem.

Transmitter Section (Figure 4-31)

A free running RC oscillator supplies the transmitter clocking signal. The oscillator is adjustable within a tolerance of ±5% and contains a temperature compensation network to prevent drift. The oscillator frequency is twice that of the modem operating frequency.

The oscillator output is divided by two which produces a clean symmetrical square wave at the desired modem operating frequency. This signal plus the oscillator output and data to be transmitted are combined in the Clock Phase/Data Anding Network to generate the clocking signal for the OUT flip-flop. This clocking signal is a string of positive pulses that occur once or twice per bit time depending on whether the data is a 1 or a 0, respectively.

The OUT flip-flop is connected so that it is complemented by successive clock pulses. Therefore, its output executes one or two state transitions during one bit time depending on whether the data is a 1 or a 0.

The TTL output from the OUT flip-flop goes to a bipolar line driver that generates an ac signal with zero crossover points that coincide with the TTL input. In the 56K bps version, pulse shapers are included in the line driver to increase the amplitude of the ac signal at the crossover points.

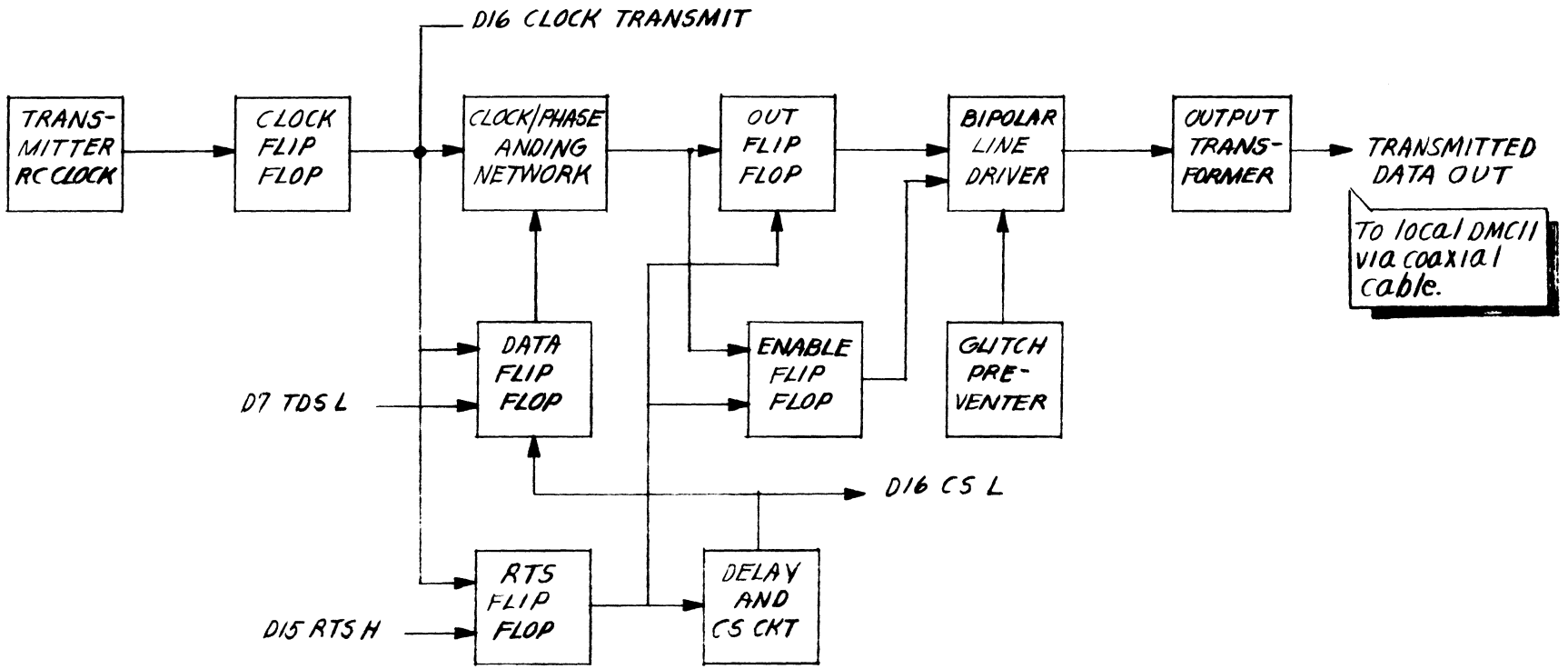


Figure 4-31 Simplified Block Diagram of Modem Transmitter

The output of the line driver goes to the protection transformer and on to the receiving station via the coaxial cable. The transformer protects the modem against damage by voltages up to 1500 V that may be picked up accidently by the cable.

Data to be transmitted is D7 TDS L which comes from the 0 output of the TDS flip-flop in the transmitter control logic. Signal D7 TDS L goes to the DATA flip-flop which is clocked at the modem operating frequency. The output of the DATA flip-flop goes to the Clock Phase/Data Anding Network.

Transmission cannot be initiated until the RTS flip-flop is set and the Delay and Clear to Send Circuit asserts signal D16 CS. Until these conditions have been satisfied, the transmit line remains in the MARK hold state. When the Request to Send (RS) flip-flop in the maintenance select logic (print D15) is set, D15 RTS H is asserted. Now, the RTS flip-flop in the modem is set. Seven bit times after RTS is set, signal D16 CS L goes low and is sent to the maintenance logic to assert D15 SEND H which is the enabling signal for the transmitter logic (print D6). After three additional bit times, transmission starts.

After the RTS flip-flop is set, the ENABLE flip-flop is set. The 1 output of this flip-flop goes to the Bipolar Line Driver. ENABLE must be set to allow the modem to leave the MARK hold state and transmit data as indicated by the state changes of the OUT flip-flop.

The Glitch Preventer senses +5 V and its output goes to the Bipolar Line Driver. During power-up, this circuit holds the modem in the MARK condition for several milliseconds to prevent the transmission of nonsense characters.

Receiver Section (Figure 4-32)

The received data is an ac signal that must exceed 150 mV peak-to-peak. It enters the modem through the input protection transformer.

From the transformer, the signal goes to a filter with a FET front end. It is a linear phase bandpass filter for 10 KHz to 2 MHz which eliminates low frequency noise from the input signal. The filter provides complementary signals to the input of the Zero Crossover Detector.

Two differential comparators are connected to form the Zero Crossover Detector. This circuit provides complementary outputs that are the inverse of the corresponding inputs. These output signals are TTL compatible and provide levels that are approximately 0 V for a low and 3.5 V for a high.

Each Zero Crossover Detector output is connected to the input of a 200 ns 1-shot. A positive-going edge from the detector triggers its associated 1-shot. The 1-shots do not retrigger nor are they triggered simultaneously; therefore, each one produces a string of 200 ns negative pulses. These two pulse strings are ORed and inverted to form a single string of positive 200 ns pulses. These

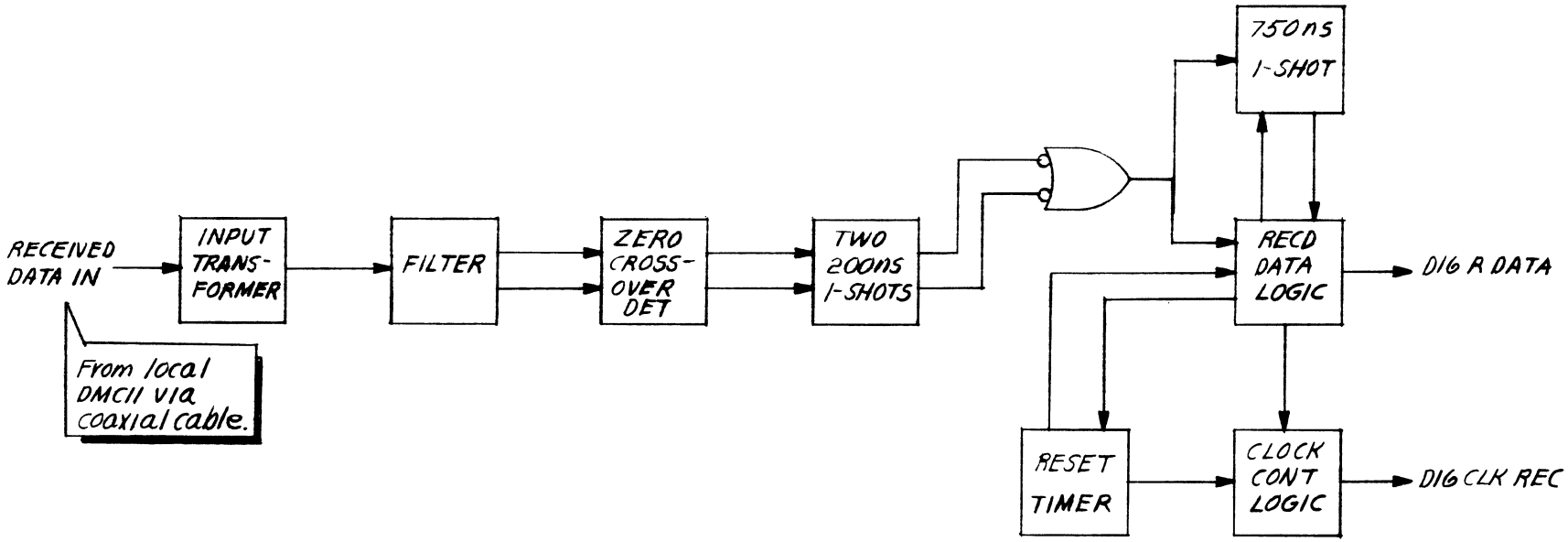


Figure 4-32 Simplified Block Diagram of Modem Receiver

pulses trigger the 750 ns Clock 1-shot which is not retriggerable. It produces a train of 750 ns pulses that are separated by 250 ns. This on-off cycle totals 1 µs which is the bit time for the 1M bps modem. Other speeds (56K, 250K and 500K bps) are obtained by changing component values in the modem circuitry. A component value table is shown in sheet D16 of the print set.

The output of the 750 ns Clock 1-shot goes to the Receiver Data logic. This logic responds to the 750 ns 1-shot plus the string of 200 ns pulses to produce a TTL data signal (D16 R DATA) which represents the state of the received data for one bit time (1 µs for the 1M bps modem). This signal goes to the On Line Loop Select mux (sheet D15), comes out as D15 RX DATA and is sent to the receiver control logic (sheet D10) as received data.

The output of the 750 ns Clock 1-shot also goes to the Clock Control logic to generate the receiver clock signal D16 CLOCK RECEIVE. This signal is a string of 250 ns positive pulses. The leading edge of each pulse occurs at the start of each bit time. Signal D16 CLOCK RECEIVE goes to the receiver clock logic (print D10) as the receiver clock.

The output of the 750 ns Clock 1-shot is constantly monitored by the Reset Timer. This device is a retriggerable 1-shot with a 1.5 µs pulse duration. As long as data, and hence the clock, is present the 1-shot remains enabled. If there is no clock for one and one half bit times (1.5 µs), the 1-shot times out and clears the Receiver Data Logic.

CHAPTER 5

MAINTENANCE

5.1 SCOPE

This chapter lists required test equipment and provides a complete description of the DMC11 Line Unit preventive and corrective maintenance procedures.

5.2 MAINTENANCE PHILOSOPHY

Basically, line unit maintenance consists of preventive and corrective maintenance procedures, diagnostic programs, and a maintenance log. The preventive maintenance procedures are performed regularly in an attempt to detect any deterioration due to aging and any damage caused by improper handling of the module. The corrective maintenance procedures are performed to isolate and repair faults in module circuitry only after it has been determined that the module is faulty. The maintenance log is used to record all maintenance activities for future reference and analysis; hopefully, the log will facilitate future maintenance action and aid in detecting any component failure pattern that may develop.

5.3 PREVENTIVE MAINTENANCE

Preventive maintenance consists of tasks performed at periodic intervals to ensure proper equipment operation and minimum unscheduled downtime. These tasks consist of running diagnostics, visual inspection and operational checks.

The preventive maintenance schedule depends on the environmental and operating conditions that exist at the installation site. Under normal conditions, recommended preventive maintenance consists of inspection and cleaning every 600 hours of operation of every 4 months, whichever occurs first. However, relatively extreme conditions of temperature, humidity, dust, and/or abnormally heavy work loads demand more frequent maintenance.

The diagnostic programs comprise the basic tool used by the technician to isolate faults. The diagnostics exercise the DMC11 in three distinct maintenance modes and provide printouts indicating the results. The printouts point the technician to a particular logic area such as the transmitter or receiver logic. The technician uses standard test equipment (scope and probe) to further isolate the fault to a specific circuit component.

5.4 TEST EQUIPMENT REQUIRED

Maintenance procedures for the line unit require the standard test equipment and diagnostic programs listed in Table 5-1, in addition to standard hand tools, cleaners, test cables, and probes.

5.5 CORRECTIVE MAINTENANCE

The corrective maintenance procedures are designed to aid the maintenance technician in isolating and repairing faults within the line unit module. Hence, the technician must be otherwise equipped to determine that the line unit is, in fact, at fault.

Table 5-1

Test Equipment Required

Equipment	Manufacturer	Designation
Multimeter	Triplett or Simpson	Model 630-NA or 260
Oscilloscope	Tektronix	Type 453
X10 Probes (2)	Tektronix	P6008
Module Extenders	DEC	W984 (Double) W987 (Quad) NOTE For a hex board use a double and a quad
Diagnostic Tapes	DEC	DZDME and DZDMF

5.5.1 Maintenance Modes

The line unit can be operated in three modes. They are:

1. Internal maintenance
2. System test
3. External maintenance

The modes are selected by two signals that come from the microprocessor. The signals are D3 LU LOOP H and D3 RUN (1) H. They control two multiplexers in the maintenance logic (print D15) to select the clocking source and to condition the interface logic (M8201 only) or the integral modem (M8202 only) for servicing.

5.5.1.1 Internal Maintenance - This mode checks about 90% of the line unit without disconnecting it from the modem (M8201) or the coaxial cable (M8202).

Signal D15 SEND H is asserted to keep the transmitter active. The transmitter output is looped around to become the receiver input. The Request to Send and Data Terminal Ready signals are held OFF.

The clocking source is D3 STEP from the microprocessor. It is single stepped by the diagnostic program.

5.5.1.2 System Test - This mode is set up similar to the internal maintenance mode except that the clock source is the 10 KHz internal RC clock.

5.5.1.3 External Maintenance Mode - This mode provides complete checking of the line unit including level conversion logic and associated cables.

For the M8201 line unit, the modem must be disconnected and the H325 must be connected to the BC05C-25 cable (Figure 5-1).

For the M8202 line unit, the coaxial cables must be disconnected and the 12-12528 coaxial adapter must be used to connect the pig-tail coaxial cables together. This tests all the transmitter and receiver logic as well as the integral modem and pig-tail cables.

Clocking for the M8201 line unit is supplied by the 10 KHz internal clock which is turned around in the H325 test connector to simulate the modem transmit and receive clocks.

Clocking for the M8202 is supplied by the integral modem clock.

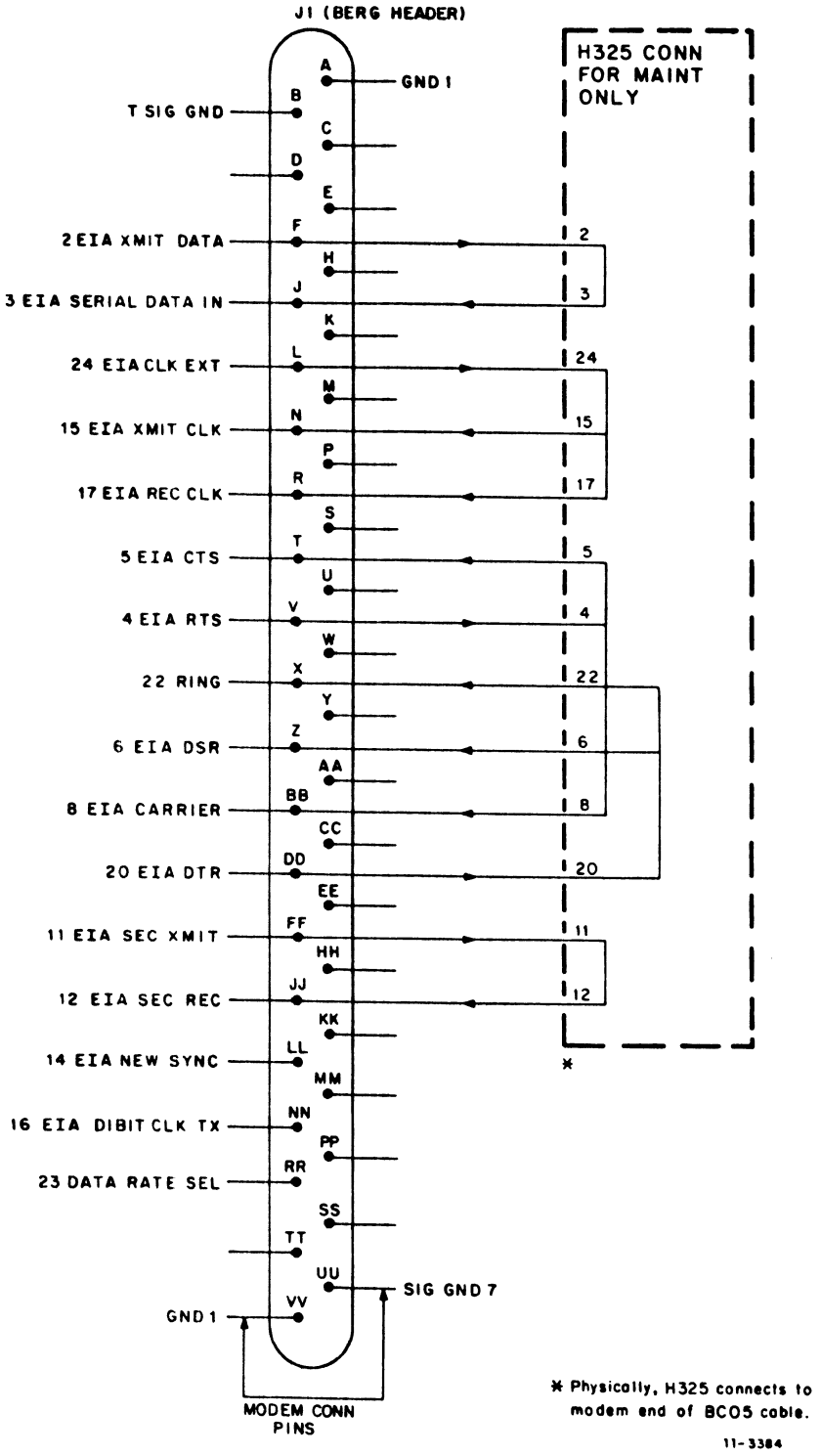


Figure 5-1 Schematic of H325 Test Connector

Also, for the M8201, the modem control signals are tested to ensure the proper level conversion and cable paths exist. The signals are turned around in the H325 test connector as follows.

Transmitted data is returned as received data.

Request to Send is returned as Clear to Send.

Data Terminal Ready is returned as Ring and Data Set Ready.

5.5.2 Diagnostics

Two diagnostic tapes are used to verify proper operation of the line unit. They are DZDME which tests under DDCMP control and DZDMF which tests under Bit Stuff protocol control.

Detailed discussions of the content, use and interpretation of each diagnostic tape is documented separately. The documents and tapes are shipped with the line unit.

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