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REV C H7606-0-0 DD B SIZE CODE

DRAWING NO.	NO OF SHTS	PART NO.	DESCRIPTION	REVISIONS											
				B1	C1	D1									
		M7606	KA630	A	B	C									
D-UA-M7606-0-0	1		KA630 UNIT ASSEMBLY	A	B	C									
K-PL-M7606-0-DBP	2		KA630 PARTS LIST	A	B	C									
K-PC-M7606-0-DBJ	1		P.C. DESIGN DATA BASE	E	E	E									
		5016523-01	ETCHED CIRCUIT BOARD	E1	E1	E1									
B-DD-5016523-0-0	1		DRAWING DIRECTORY	A	A	A									
B-CS-M7606-0-1	1		M7606 DRAWING DIRECTORY	-	B	B									
B-CS-M7606-0-2	1		MICROVAX II SYSTEM	-	B	B									
B-CS-M7606-0-3	1		KA630-UVAX ON Q22 BUS	-	B	B									
B-CS-M7606-0-4	1		UVAX & FPU	-	B	B									
B-CS-M7606-0-5	1		UVAX & FPU PINOUTS	-	B	B									
B-CS-M7606-0-6	1		ADDRESS LATCH/LOCAL MEMORY DECODE	-	B	B									
B-CS-M7606-0-7	1		MEMORY SUBSYSTEM	-	B	B									
B-CS-M7606-0-8	1		Q22 BUS INTERFACE GATE ARRAY	-	B	B									
B-CS-M7606-0-9	1		Q22 BUS INTERFACE GATE ARRAY	-	B	B									
B-CS-M7606-0-10	1		DC380 PAD ASSIGNMENT TOP VIEW LL5320 IN 144 PIN GRID ARRAY	-	B	B									
B-CS-M7606-0-11	1		REFRESH LOGIC/COUNTER	-	B	B									
B-CS-M7606-0-12	1		DIVIDE BY 12	-	B	B									
B-CS-M7606-0-13	1		SYNCHRONOUS 3 BIT COUNTER	-	B	B									
NOTES:				REVISION HISTORY	DATE	ECO NO.	REV	A	B	C					
					5/84			INIT							
					5/85			M001							
					6/85			M002							
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						CHK'D E. LANDRY	DATE 5/17/84	KA630							
						DES. ENG B. MASKAS	DATE 5/17/84	DOCUMENT NUMBER							
						RESP ENG B. MASKAS	DATE 5/17/84	SIZE B	CODE DD	NUMBER M7606-0-0	REV. C	SHEET 1 OF 4			
						MFG. ENG. B. SCHULTE	DATE 9/24/84								

DRB 128C
EN-01242-16-REVA(388)

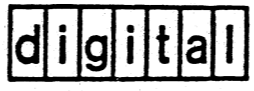
KA630-A

DRAWING NO.	NC OF SHTS	PART NO.	DESCRIPTION	REVISIONS																			
B-CS-M7606-0-14	1		VECTOR HACK	-	B	B																	
B-CS-M7606-0-15	1		INVERTING MUX LOGIC		B	B																	
B-CS-M7606-0-16	1		4 to 1 MUX		B	B																	
B-CS-M7606-0-17	1		Q-BUS SUPPORT LOGIC		B	B																	
B-CS-M7606-0-18	1		BLK MD CTR LOGIC		B	B																	
B-CS-M7606-0-19	1		TOGGLE FLOP		B	B																	
B-CS-M7606-0-20	1		Q-BUS SUPPORT LOGIC		B	B																	
B-CS-M7606-0-21	1		Q-BUS SUPPORT LOGIC		B	B																	
B-CS-M7606-0-22	1		Q-BUS SUPPORT LOGIC		B	B																	
B-CS-M7606-0-23	1		Q-BUS SUPPORT LOGIC		B	B																	
B-CS-M7606-0-24	1		POWER BUFFER MACRO		B	B																	
B-CS-M7606-0-25	1		BIDIRECT BUFFER		B	B																	
B-CS-M7606-0-26	1		MUX LOGIC		B	B																	
B-CS-M7606-0-27	1		TRANSLATION MAP GROUP		B	B																	
B-CS-M7606-0-28	1		KA630 Q-BUS INTERFACE		B	B																	
B-CS-M7606-0-29	1		UVAX INTERFACE GATE ARRAY		B	B																	
B-CS-M7606-0-30	1		DC179 PAD ASSIGNMENT TOP-VIEW LL3320 IN 144 PIN GRIP ARRAY		B	B																	
B-CS-M7606-0-31	1		UVAX INTERFACE GATE ARRAY DATA PATH		B	B																	
B-CS-M7606-0-32	1		UVDAL I/O BUFFERS, ADDR LATCHES		B	B																	

NOTES:

DATE	ECO NO.	REV.	REVISION HISTORY		
			A	B	C
5/84	INIT				
5/85	MLO01				
6/85	MLO02				

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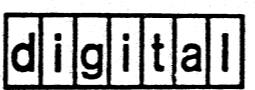
DRN. D. DROZD	DATE 5/17/84	TITLE	
CHK'D E. LANDRY	DATE 5/17/84	KA630	
DES. ENG. B. MASKAS	DATE 5/17/84	DOCUMENT NUMBER	
RESP. ENG. B. MASKAS	DATE 5/17/84	SIZE B DD	NUMBER M7606-0-0
MFG. ENG. B. SCHULTE	DATE 9/24/84	REV C	SHEET 2 OF 4

DRAWING NO.	NO OF SHTS	PART NO.	DESCRIPTION	REVISIONS																		
				1	2	3	4	5	6	7	8	9	10	11	12							
B-CS-M7606-0-33	1		ADDRESS DECODER	-	B	B																
B-CS-M7606-0-34	1		EXCEPTIONS AND INTERRUPTS	-	B	B																
B-CS-M7606-0-35	1		UVAX INPUTS AND I/O PINS	-	B	B																
B-CS-M7606-0-36	1		BOOT/DIAG REG., MEM ERR ADDR REG.	-	B	B																
B-CS-M7606-0-37	1		EPR BUS, X DAL BUS	-	B	B																
B-CS-M7606-0-38	1		INTERNAL DATA BUSES	-	B	B																
B-CS-M7606-0-39	1		MISC. CONTROL STROBES	-	B	B																
B-CS-M7606-0-40	1		RESET COUNTER, POWER UP/DOWN CTRL	-	B	B																
B-CS-M7606-0-41	1		MEMOK SYSTEM ERROR REGISTER	-	B	B																
B-CS-M7606-0-42	1		TIME OF YEAR (TOY) CLOCK	-	B	B																
B-CS-M7606-0-43	1		CONSOLE SERIAL LINE INTERFACE	-	B	B																
B-CS-M7606-0-44	1		LEDS AND CONFIGURATION CONNECTOR	-	B	B																
B-CS-M7606-0-45	1		DECOUPLING CAPACITORS	-	B	B																
B-CS-M7606-0-46	1		KA630 STATE MACHINES	-	B	B																
B-CS-M7606-0-47	1		UVAX CYCLE CONTROLLER	-	B	B																
B-CS-M7606-0-48	1		MEMORY SEQUENCER	-	B	B																
B-CS-M7606-0-49	1		MEMORY SEQUENCER SUPPORT	-	B	B																
B-CS-M7606-0-50	1		Q22 BUS STATE MACHINES	-	B	B																
B-CS-M7606-0-51	1		KA630 MEMORY ARBITER LISTING	-	B	B																

NOTES:

REVISION HISTORY	REV.	DATE	INITIALS		
			ECO NO.	INIT	ML001
	A	5/84			
	B	5/85			
	C	6/85			

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DRN.	D.DROZD	DATE	5/17/84	TITLE	KA630
CHK'D	E.LANDRY	DATE	5/17/84		
DES. ENG.	B.MASKAS	DATE	5/17/84	DOCUMENT NUMBER	
RESP. ENG.	B.MASKAS	DATE	5/17/84	SIZE	CODE
MFG. ENG.	B.SCHULTE	DATE	9/24/84	B	DD
				NUMBER	REV.
				M7606-0-0	C
				SHEET 3	OF 4

DRAWING NO.	NO OF SHTS	PART NO.	DESCRIPTION	REVISIONS								
B-CS-M7606-0-52	1		KA630 MEMORY SYSTEM ARBITER STATE FLOW DIAGRAMS	-	B	B						
B-CS-M7606-0-53	1		KA630 MEMORY SYSTEM ARBITER STATE FLOW DIAGRAMS	-	B	B						
B-CS-M7606-0-54	1		KA630 LOCAL I/O CONTROL MACHINE UL TESTING	-	-	-						
B-CS-M7606-0-55	1		KA630 LOCAL I/O BUS CONTROL	-	E	B						
B-CS-M7606-0-56	1		KA630 Q-BUS ARBITRATION CONTROL MACHINE LISTING	-	-	-						
B-CS-M7606-0-57	1		Q-BUS ARBITRATION CONTROLLER DETAILED CONTROL FLOW DIAGRAM	-	B	B						
B-CS-M7606-0-58	1		Q22 BUS MASTER CONTROL MACHINE LISTING	-	-	-						
B-CS-M7606-0-59	1		Q22 BUS MASTER CONTROL MACHINE FLOW DIAGRAM	-	B	B						
B-CS-M7606-0-60	1		Q22 BUS SLAVE CONTROL MACHINE LISTING	-	-	-						
B-CS-M7606-0-61	1		Q22 BUS SLAVE CONTROL MACHINE FLOW DIAGRAM	-	B	B						
B-CS-M7606-0-62	1		Q22 BUS SLAVE CONTROL MACHINE FLOW DIAGRAM	-	B	B						
B-CS-M7606-0-63	1		IKKL RAS DECODE FROM (ETS) LISTING	-	-	-						
B-CS-M7606-0-64	1		PALASM LISTING FOR PALISLSA DEVICES	-	-	-						
B-CS-M7606-0-65	1		MEMORIC DICTIONARY	-	-	-						
K-DO-M7606-0-0	24		M7606 CROSS REF LIST	-	A	A						

NOTES:

DATE	ECO NO.	REV.	A	B	C
5/84	INIT				
5/85	MLOO1				
6/85	MLOO2				

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DRN.	D.DROZD	DATE	5/17/84
CHK'D	E.LANDRY	DATE	5/17/84
DES. ENG.	B.MASKAS	DATE	5/17/84
RESP. ENG.	B.MASKAS	DATE	5/17/84
MFG. ENG.	B.SCHULTE	DATE	9/24/84

TITLE			
KA630			
DOCUMENT NUMBER			
SIZE	CODE	NUMBER	REV
B	DD	M7606-0-0	C
SHEET 4 OF 4			

LINE	ITEM	TOP DOCUMENT	PART NUMBER	MIN REV	DESCRIPTION	QTY PER VARIATION				REFERENCE DESIGNATOR
						AA	AC	AH	BA	
						D1	D1	D1	D1	
1	1	D-MD-5016523-0-0	5016523-01		CIRCUIT DRILL & ETCH	1	1	1	1	
2	2		1010279-01		.47 MFD 25V 20% CER	6	6	6	6	C30-C35
3	3		1012784-00		.047 MFD 50V +80-20% CER	7	7	7	7	C28,C1-C6
4	4		1013466-05		56.0 MMF 50V 5% CER	1	1	1	1	C67
5	5		1013466-07		220.0 MMF 50V 5% CER	1	1	1	1	C29
6	6		1014265-02		.33 MFD 50V +80-20% CER	58	58	58	58	C7-C27,C42-C66,C68,C69,C71-C80
7	7		1017472-00		10 MFD 35V +75-10% AL EL	3	3	3	3	C39-C41
8	8		1020446-05		22 MFD 16V +50-10% AL EL	2	2	2	2	C37,C38
9	9		1100114-00		PIV= 25 IO=135 MA	1	1	1	1	D9
10	10		1105275-00		PIV= 60 IO=300 MA -15NS	3	3	3	3	D2,D4,D3
11	11		1109977-00		VZ= 4.3 5% 1N749A	1	1	1	1	D1
12	12		1114117-00		PIV= 40 IO= 75 A - 4NS	3	3	3	3	D6-D8
13	13		1114136-02		LED 6.7MA 5V .2MCD GREEN	1	1	1	1	D14
14	14		1120964-01		LED ASSY 4 RED 5V 8MA	1	1	1	1	D10
15	15		1210929-02		FUSE, SUB-MINI 1.000A, 125V, A	2	2	2	2	F1,F2
16	16		1213113-03		HANDLE,MODULE	1	1	1	1	
17	17		1213506-04		PCB HEADER 09PIN(2X05).100CC 90D	1	1	1	1	J3
18	18		1213506-10		PCB HEADER 20PIN(2X10).100CC 90D	1	1	1	1	J2
19	19		1213506-13		PCB HEADER 50PIN(2X25).100CC 90D	1	1	1	1	J1
20	20		1215006-07		SKT,IC 28PIN DIP TIN SOLD	2	2	2	2	XE21,XE22
21	21		1300202-00		47.0 .25 W 5.0 % CF	3	3	3	3	R1,R2,R29
22	22		1300365-00		1.0 K .25 W 5.0 % CF	1	1	1	1	R3
23	23		1300447-00		4.70 K .25 W 5.0 % CF	1	1	1	1	R8
24	24		1300479-00		10.0 K .25 W 5.0 % CF	2	2	2	2	R11,R12
25	25		1301808-00		22.0 K .25 W 5.0 % CF	1	1	1	1	R4
26	26		1302388-00		2.0 K .25 W 5.0 % CF	1	1	1	1	R14
27	27		1302466-00		100.0 K .25 W 5.0 % CF	1	1	1	1	R16
28	28		1304837-00		24.0 K .25 W 5.0 % CF	1	1	1	1	R7
29	29		1314637-00		R NETWORK 3-22 1.0 % 6PIN	4	4	4	4	R31-R34
30	30		1316334-02		R NETWORK 9-10K 2.0 % 10PIN	2	2	2	2	R10,R23

REVISION HISTORY			BASIC PART NO: M7606			DRN: RONALD RHOADES DATE: 01-FEB-84			D I G I T A L				
ENG!	ECO NUMBER	REV	SECTION A OF C			CHK'D:	DAVID DROZD	DATE:	17-MAY-84	TITLE PARTS LIST			
---	INITIAL	A	SECTION VARIATION INDEX			CHK'D:	DAVID DROZD	DATE:	17-MAY-84	MAYFLOWER KA630			
BM	M7606-ML001	B	[A] AA,AC,AH,BA			DES.ENG.:	BARRY MASKAS	DATE:	22-MAY-84	DOCUMENT NUMBER			
BM	M7606-ML002	C	[B] BC,BH,CA,CC			RESP.ENG.:	BARRY MASKAS	DATE:	8-AUG-84	SIZE!	CODE!	NUMBER	REV
			[C] CH,DA,DC,DH			MFG.ENG.:	BILL SCHULTE	DATE:	22-MAY-84	K	PL	M7606-0-DBP	C
			[D]						RELEASE DATE: 19-JUN-85				
			[E]										
			[F]										
			[H]										
			[J]										
			[K]										
			[L]										
			[M]										
			[N]										
			ASSEMBLY NUMBER:			TOP DOCUMENT NUMBER:			FILE NAME:			EDIT #	
			D-UA-M7606-0-0			B-DD-M7606-0-0			Z8847C.PLS			37	

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LINE	ITEM	TOP DOCUMENT	PART NUMBER	MIN REV	DESCRIPTION	QTY PER VARIATION				REFERENCE DESIGNATOR
						AA D1	AC D1	AH D1	BA D1	
31	31		1316395-02		R NETWORK 9-1.0K 2.0 % 10PIN	1	1	1	1	R9
32	32		1317404-00		249.0 .25 W 1.0 % RN55D-F10	1	1	1	1	R13
33	33		1317558-01		R NETWORK 4-27 5.0 % 8PIN	2	2	2	2	R39,R40
34	34		1318110-00		R NETWORK 11-330 11-680 13PIN	4	4	4	4	R24-R27
35	35		1319610-01		750.0 K .25 W .10% RN55E-B 2	1	1	1	1	R17
36	36		1319645-01		487.0 K .25 W .10% RN55E-B 2	1	1	1	1	R18
37	37		1321144-01		R NETWORK 5-220 2.0% 10PIN	1	1	1	1	R28
38	38		1321218-01		R NETWORK 4-39 +-10HM 8PIN	4	4	4	4	R35-R38
39	39		1811660-05		*** THIS ITEM IS NOT USED ***	-	-	-	-	
40	40		1811660-62		OSCILLATOR,XTAL 614.4 KHZ	1	1	1	1	Y2
41	41		1814057-00		OSCILLATOR, XTAL 40.000 MHZ	1	1	1	1	Y3
42	42		1818800-00		OSCILLATOR,XTAL 32.768KHZ	1	1	1	1	Y1
43	43		1911469-B0		8640 BURNED-IN RECEIVER,B	1	1	1	1	E16
44	44		1912803-B0		LS04 BURNED-IN INVERTER G	1	1	1	1	E25
45	45		1913471-B0		LS367 BURNED-IN DRIVER,BUS	1	1	1	1	E41
46	46		1914140-01	LM	211P COMPARATOR,VOLTAGE	1	1	1	1	E29
47	47		1914987-00		8641-2 TRANSCEIVER,UNIBUS,QU	4	4	4	4	E5,E7,E19,E24
48	48		1915193-B0		LS244 BURNED-IN DRIVER,LIN	1	1	1	1	E28
49	49		1915219-B0		LS373 BURNED-IN FF-0 OCTAL	1	1	1	1	E1
50	50		1915415-B0		9636 BURNED-IN DRIVER,DUA	1	1	1	1	E23
51	51		1916028-B1		9643 BURNED-IN DRIVER,TTL	1	1	1	1	E15
52	52		1918868-B0		LS26 NAND GATE,2-IN,HIGH	1	1	1	1	E35
53	53		1919015-00	DC	021 BUS TRANSCEIVER,20PI	3	3	3	3	E11,E30,E36
54	54		1919542-B1		9639 RECEIVER,LINE,DUAL,P	1	1	1	1	E18
55	55		1919684-01	LM	385B2 PREC VOLT REF. 1.23	1	1	1	1	D5
56	56		1920441-B1		74F245 TRANSCEIVER,BI-DIREC	4	4	4	4	E52,E71,E85,E99
57	57		1920442-B1		74F374 FF-D,OCTAL,TRI-STATE	2	2	2	2	E8,E12
58	58		1920853-B1		LS646 BUS TRANSCEIVER/REGI	2	2	2	2	E9,E10
59	59		1921008-B1		74F240 BUFFER/LINE DRIVER,0	2	2	2	2	E80,E94
60	60		1921010-B1		74F373 OCTAL TRANSPARENT LA	5	5	5	5	E2,E6,E46,E53,E73
61	61		1921305-B1		74F00 NAND GATE,QUAD,2-IN,	1	1	1	1	E47
62	62		1921306-B1		74F02 NOR GATE,QUAD,2-IN,B	1	1	1	1	E38
63	63		1921307-B1		74F04 HEX INVERTER,BURNED	2	2	2	2	E32,E87
64	64		1921312-B1		74F32 OR GATE,QUAD,2-IN,BU	2	2	2	2	E37,E65
65	65		1921314-B1		74F74 FF-D,DUAL,BURNED-IN	2	2	2	2	E31,E34
66	66		1921321-B1		74F158 MUX,QUAD,2-IN,BURNED	3	3	3	3	E72,E93,E101
67	67		1921323-B1		74F174 FF-D,HEX,BURNED-IN	2	2	2	2	E17,E59
68	68		1921417-B1		74F521 COMPARATOR,IDENTITY,	1	1	1	1	E66
69	69		1922871-01		TRANSCEIVER,PARITY B	4	4	4	4	E58,E64,E92,E106
70	70		1923679-B1		74F537 DECODER/DEMUX,1-OF-1	1	1	1	1	E100
71	71		2117312-00		UART DL-11 SOFTWARE	1	1	1	1	E13
72	72		2118467-02		*** THIS ITEM IS NOT USED ***	-	-	-	-	
73	73		2118472-02		*** THIS ITEM IS NOT USED ***	-	-	-	-	
74	74		2118795-00		146818 CLOCK/CALENDAR/RAM	1	1	1	1	E14
75	75		2120887-01	DC	333 MICROVAX,32BIT 68PIN	1	1	1	1	E43
76	76		2121384-02		RAM 8KX8,STATIC 150	2	2	2	2	E3,E4
77	77		2121413-02		41256 RAM 256KX1,DYNAMIC 1	-	-	36	-	E48-E51,E54-E57,E60-E63,E67-E70, CONT E74-E77,E81-E84,E88-E91,E95-E98.

D	I	G	I	T	A	L	TITLE	MAYFLOWER	SECTION A	OF	C	SIZE	CODE	DOCUMENT NUMBER	REV
							KA630					K	PL	M7606-0-DBP	C

LINE	ITEM	TOP DOCUMENT	PART NUMBER	MIN REV	DESCRIPTION	QTY PER VARIATION				REFERENCE DESIGNATOR
						AA	AC	AH	BA	
						D1	D1	D1	D1	
78	78		2121415-02		81256-15 RAM 256KX1,DYNAMIC 1	-	36	-	-	CONT E102-E105 E48-E51,E54-E57,E60-E63,E67-E70, CONT E74-E77,E81-E84,E88-E91,E95-E98, CONT E102-E105
79	79		2122797-01		DC 337 MICROVAX FLOATING PO	1	1	1	-	E42
80	80		2123389-01		GATE ARRAY,3200 GATE	1	1	1	1	E45
81	81		2123413-01		DC379 CMOS GATE ARRAY,144PGA,320	1	1	1	1	E44
82	82		23007L3-00		L3-01	1	1	1	1	E39
83	83		23008L3-00		L3-01 FPLS	1	1	1	1	E20
84	84		23009L3-00		L3-01	1	1	1	1	E26
85	85		23010L3-00		L3-01	1	1	1	1	E33
86	86		23018E6-00		*** THIS ITEM IS NOT USED ***	-	-	-	-	
87	87		23019E6-00		*** THIS ITEM IS NOT USED ***	-	-	-	-	
88	88		23036L1-00		*** THIS ITEM IS NOT USED ***	-	-	-	-	
89	89		23115F2-00		*** THIS ITEM IS NOT USED ***	-	-	-	-	
90	90		23169J5-00		J5-03 PAL,LOGIC	1	1	1	1	E40
91	91		23170J5-00		J5-03 PAL,LOGIC	1	1	1	1	E78
92	92		23171J5-00		J5-03 PAL,LOGIC	1	1	1	1	E86
93	93		23E42F1-00		F1-05	1	1	1	1	E79
94	94		9000024-01		EYELET,ROLLED 0.1210DX0.192	4	4	4	4	
95	95		9009185-00		JUMPER, WIRE, INSULATED, BLACK B	3	3	3	3	W2,W4,W5
96	96		9907004-06		CARTON,DIE CUT,B,200PSI W/ARTWOR	1	1	1	1	
97	97		9907025-06		BAG,ANTISTATIC BUBBLE	1	1	1	1	
98	98		9907092-04		BAG,TRANSLUCENT,ESD PROTECTIVE	1	1	1	1	
99	99		23034E6-00		*** THIS ITEM IS NOT USED ***	-	-	-	-	
100	100		23035E6-00		*** THIS ITEM IS NOT USED ***	-	-	-	-	
101	101		23053L1-00		L1-01	1	1	1	1	E27
102	102		23062E6-00		E6-02 U	1	1	1	1	E22
103	103		23063E6-00		E6-02 U	1	1	1	1	E21

- 104 NOTE: M7606-AA IS THE PRIMARY VARIATION OF THE KA630 CPU.
- 105 NOTE: M7606-AC IS THE MODULE USING FUJITSU 256K RAMS.
- 106 NOTE: M7606-AH IS THE MODULE USING NEC 256K RAMS.
- 107 NOTE: M7606-BA IS THE AA VERSION WITHOUT FLOATING POINT.
- 108 NOTE: M7606-BC IS THE MODULE USING FUJITSU 256K RAMS.
- 109 NOTE: M7606-BH IS THE MODULE USING NEC 256K RAMS.
- 110 NOTE: M7606-CA IS THE AA VERSION USING 64K RAMS
- 111 NOTE: M7606-CC IS THE MODULE USING FUJITSU 64K RAMS.
- 112 NOTE: M7606-CH IS THE MODULE USING NEC 64K RAMS.
- 113 NOTE: M7606-DA IS THE CA VERSION WITHOUT FLOATING POINT.
- 114 NOTE: M7606-DC IS THE MODULE USING FUJITSU 64K RAMS.
- 115 NOTE: M7606-DH IS THE MODULE USING NEC 64K RAMS.

D	I	G	I	T	A	L	TITLE	SECTION A	OF	C	SIZE	CODE	DOCUMENT NUMBER	REV
							MAYFLOWER KA630				K	PL	M7606-0-DBP	C

LINE	ITEM	TOP DOCUMENT	PART NUMBER	MIN REV	DESCRIPTION	QTY PER VARIATION				REFERENCE DESIGNATOR
						BC	BH	CA	CC	
						D1	D1	D1	D1	
1	1	D-MD-5016523-0-0	5016523-01		CIRCUIT DRILL & ETCH	1	1	1	1	
2	2		1010279-01		.47 MFD 25V 20% CER	6	6	6	6	C30-C35
3	3		1012784-00		.047 MFD 50V +80-20% CER	7	7	7	7	C28,C1-C6
4	4		1013466-05		56.0 MMF 50V 5% CER	1	1	1	1	C67
5	5		1013466-07		220.0 MMF 50V 5% CER	1	1	1	1	C29
6	6		1014265-02		.33 MFD 50V +80-20% CER	58	58	58	58	C7-C27,C42-C66,C68,C69,C71-C80
7	7		1017472-00		10 MFD 35V +75-10% AL EL	3	3	3	3	C39-C41
8	8		1020446-05		22 MFD 16V +50-10% AL EL	2	2	2	2	C37,C38
9	9		1100114-00		PIV= 25 IO=135 MA	1	1	1	1	D9
10	10		1105275-00		PIV= 60 IO=300 MA -15NS	3	3	3	3	D2,D4,D3
11	11		1109977-00		VZ= 4.3 5% 1N749A	1	1	1	1	D1
12	12		1114117-00		PIV= 40 IO= 75/ A - 4NS	3	3	3	3	D6-D8
13	13		1114136-02		LED 6.7MA 5V .2MCD GREEN	1	1	1	1	D14
14	14		1120964-01		LED ASSY 4 RED 5V 8MA	1	1	1	1	D10
15	15		1210929-02		FUSE, SUB-MINI 1.000A, 125V, A	2	2	2	2	F1,F2
16	16		1213113-03		HANDLE,MODULE	1	1	1	1	
17	17		1213506-04		PCB HEADER 09PIN(2X05).100CC 90D	1	1	1	1	J3
18	18		1213506-10		PCB HEADER 20PIN(2X10).100CC 90D	1	1	1	1	J2
19	19		1213506-13		PCB HEADER 50PIN(2X25).100CC 90D	1	1	1	1	J1
20	20		1215006-07		SKT,IC 28PIN DIP TIN SOLD	2	2	2	2	XE21,XE22
21	21		1300202-00		47.0 .25 W 5.0 % CF	3	3	3	3	R1,R2,R29
22	22		1300365-00		1.0 K .25 W 5.0 % CF	1	1	1	1	R3
23	23		1300447-00		4.70 K .25 W 5.0 % CF	1	1	1	1	R8
24	24		1300479-00		10.0 K .25 W 5.0 % CF	2	2	2	2	R11,R12
25	25		1301808-00		22.0 K .25 W 5.0 % CF	1	1	1	1	R4
26	26		1302388-00		2.0 K .25 W 5.0 % CF	1	1	1	1	R14
27	27		1302466-00		100.0 K .25 W 5.0 % CF	1	1	1	1	R16
28	28		1304837-00		24.0 K .25 W 5.0 % CF	1	1	1	1	R7
29	29		1314637-00		R NETWORK 3-22 1.0 % 6PIN	4	4	4	4	R31-R34
30	30		1316334-02		R NETWORK 9-10K 2.0 % 10PIN	2	2	2	2	R10,R23

REVISION HISTORY			BASIC PART NO: M7606			DRN: RONALD RHOADES			DATE: 01-FEB-84			DIGITAL		
ENG	ECO NUMBER	REV	SECTION B OF C			CHK'D: DAVID DROZD			DATE: 17-MAY-84			TITLE PARTS LIST		
---	INITIAL	A	SECTION VARIATION INDEX			DES.ENG.: BARRY MASKAS			DATE: 22-MAY-84			DOCUMENT NUMBER		
BM	M7606-ML001	B	[A]	AA,AC,AH,BA	RESP.ENG.: BARRY MASKAS			DATE: 8-AUG-84			SIZE	CODE	NUMBER	REV
BM	M7606-ML002	C	[B]	BC,BH,CA,CC	MFG.ENG.: BILL SCHULTE			DATE: 22-MAY-84			K	PL	M7606-0-DBP	C
			[C]	CH,DA,DC,DH	ASSEMBLY NUMBER:			TOP DOCUMENT NUMBER:			FILE NAME:			EDIT #
			[D]		D-UA-M7606-0-0			B-DD-M7606-0-0			Z8847C.PLS			37
			[E]											
			[F]											
			[G]											
			[H]											
			[I]											
			[J]											
			[K]											
			[L]											
			[M]											
			[N]											

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LINE	ITEM	TOP DOCUMENT	PART NUMBER	MIN REV	DESCRIPTION	QTY PER VARIATION				REFERENCE DESIGNATOR
						BC D1	BH D1	CA D1	CC D1	
31	31		1316395-02		R NETWORK 9-1.0K 2.0 % 10PIN	1	1	1	1	R9
32	32		1317404-00		249.0 .25 W 1.0 % RN55D-F10	1	1	1	1	R13
33	33		1317558-01		R NETWORK 4-27 5.0 % 8PIN	2	2	2	2	R39,R40
34	34		1318110-00		R NETWORK 11-330 11-680 13PIN	4	4	4	4	R24-R27
35	35		1319610-01		750.0 K .25 W .10% RN55E-B 2	1	1	1	1	R17
36	36		1319645-01		487.0 K .25 W .10% RN55E-B 2	1	1	1	1	R18
37	37		1321144-01		R NETWORK 5-220 2.0% 10PIN	1	1	1	1	R28
38	38		1321218-01		R NETWORK 4-39 +-10HM 8PIN	4	4	4	4	R35-R38
39	39		1811660-05		OSCILLATOR, XTAL 33.330 MHZ	-	-	1	1	Y3
40	40		1811660-62		OSCILLATOR, XTAL 614.4 KHZ	1	1	1	1	Y2
41	41		1814057-00		OSCILLATOR, XTAL 40.000 MHZ	1	1	-	-	Y3
42	42		1818800-00		OSCILLATOR, XTAL 32.768KHZ	1	1	1	1	Y1
43	43		1911469-B0		8640 BURNED-IN RECEIVER, B	1	1	1	1	E16
44	44		1912803-B0		LS04 BURNED-IN INVERTER G	1	1	1	1	E25
45	45		1913471-B0		LS367 BURNED-IN DRIVER, BUS	1	1	1	1	E41
46	46		1914140-01	LM	211P COMPARATOR, VOLTAGE	1	1	1	1	E29
47	47		1914987-00		8641-2 TRANSCEIVER, UNIBUS, QU	4	4	4	4	E5, E7, E19, E24
48	48		1915193-B0		LS244 BURNED-IN DRIVER, LIN	1	1	1	1	E28
49	49		1915219-B0		LS373 BURNED-IN FF-0 OCTAL	1	1	1	1	E1
50	50		1915415-B0		9636 BURNED-IN DRIVER, DUA	1	1	1	1	E23
51	51		1916028-B1		9643 BURNED-IN DRIVER, TTL	1	1	1	1	E15
52	52		1918868-B0		LS26 NAND GATE, 2-IN, HIGH	1	1	1	1	E35
53	53		1919015-00	DC	021 BUS TRANSCEIVER, 20PI	3	3	3	3	E11, E30, E36
54	54		1919542-B1		9639 RECEIVER, LINE, DUAL, P	1	1	1	1	E18
55	55		1919684-01	LM	385B2 PREC VOLT REF. 1.23	1	1	1	1	D5
56	56		1920441-B1		74F245 TRANSCEIVER, BI-DIREC	4	4	4	4	E52, E71, E85, E99
57	57		1920442-B1		74F374 FF-D, OCTAL, TRI-STATE	2	2	2	2	E8, E12
58	58		1920853-B1		LS646 BUS TRANSCEIVER/REGI	2	2	2	2	E9, E10
59	59		1921008-B1		74F240 BUFFER/LINE DRIVER, 0	2	2	2	2	E80, E94
60	60		1921010-B1		74F373 OCTAL TRANSPARENT LA	5	5	5	5	E2, E6, E46, E53, E73
61	61		1921305-B1		74F00 NAND GATE, QUAD, 2-IN,	1	1	1	1	E47
62	62		1921306-B1		74F02 NOR GATE, QUAD, 2-IN, B	1	1	1	1	E38
63	63		1921307-B1		74F04 HEX INVERTER, BURNED	2	2	2	2	E32, E87
64	64		1921312-B1		74F32 OR GATE, QUAD, 2-IN, BU	2	2	2	2	E37, E65
65	65		1921314-B1		74F74 FF-D, DUAL, BURNED-IN	2	2	2	2	E31, E34
66	66		1921321-B1		74F158 MUX, QUAD, 2-IN, BURNED	3	3	3	3	E72, E93, E101
67	67		1921323-B1		74F174 FF-D, HEX, BURNED-IN	2	2	2	2	E17, E59
68	68		1921417-B1		74F521 COMPARATOR, IDENTITY,	1	1	1	1	E66
69	69		1922871-01		TRANSCEIVER, PARITY B	4	4	4	4	E58, E64, E92, E106
70	70		1923679-B1		74F537 DECODER/DEMUX, 1-0F-1	1	1	1	1	E100
71	71		2117312-00		UART DL-11 SOFTWARE	1	1	1	1	E13
72	72		2118467-02		8264-15 RAM 64K X1, 150NS 1	-	-	-	36	E48-E51, E54-E57, E60-E63, E67-E70, CONT E74-E77, E81-E84, E88-E91, E95-E98, CONT E102-E105
73	73		2118472-02		*** THIS ITEM IS NOT USED ***	-	-	-	-	
74	74		2118795-00		146818 CLOCK/CALENDAR/RAM	1	1	1	1	E14
75	75		2120887-01	DC	333 MICROVAX, 32BIT 68PIN	1	1	1	1	E43
76	76		2121384-02		RAM 8KX8, STATIC 150	2	2	2	2	E3, E4

D	I	G	I	T	A	L	TITLE	SECTION B OF C	SIZE	CODE	DOCUMENT NUMBER	REV
							MAYFLOWER KA630		K	PL	M7606-0-DBP	C

LINE	ITEM	TOP DOCUMENT	PART NUMBER	MIN REV	DESCRIPTION	QTY PER VARIATION				REFERENCE DESIGNATOR
						BC D1	BH D1	CA D1	CC D1	
77	77		2121413-02		41256 RAM 256KX1,DYNAMIC 1	-	36	-	-	E48-E51,E54-E57,E60-E63,E67-E70, E74-E77,E81-E84,E88-E91,E95-E98, E102-E105
78	78		2121415-02		81256-15 RAM 256KX1,DYNAMIC 1	36	-	-	-	E48-E51,E54-E57,E60-E63,E67-E70, E74-E77,E81-E84,E88-E91,E95-E98, E102-E105
79	79		2122797-01		DC 337 MICROVAX FLOATING PO	-	-	1	1	E42
80	80		2123389-01		GATE ARRAY,3200 GATE	1	1	1	1	E45
81	81		2123413-01		DC379 CMOS GATE ARRAY,144PGA,320	1	1	1	1	E44
82	82		23007L3-00		L3-01	1	1	1	1	E39
83	83		23008L3-00		L3-01 FPLS	1	1	1	1	E20
84	84		23009L3-00		L3-01	1	1	1	1	E26
85	85		23010L3-00		L3-01	1	1	1	1	E33
86	86		23018E6-00		*** THIS ITEM IS NOT USED ***	-	-	-	-	
87	87		23019E6-00		*** THIS ITEM IS NOT USED ***	-	-	-	-	
88	88		23036L1-00		*** THIS ITEM IS NOT USED ***	-	-	-	-	
89	89		23115F2-00		F2-03	-	-	1	1	E79
90	90		23169J5-00		J5-03 PAL,LOGIC	1	1	1	1	E40
91	91		23170J5-00		J5-03 PAL,LOGIC	1	1	1	1	E78
92	92		23171J5-00		J5-03 PAL,LOGIC	1	1	1	1	E86
93	93		23E42F1-00		F1-05	1	1	-	-	E79
94	94		9000024-01		EYELET,ROLLED 0.1210DX0.192	4	4	4	4	
95	95		9009185-00		JUMPER, WIRE, INSULATED, BLACK B	3	3	-	-	W2,W4,W5
			CONT			-	-	3	3	W2,W3,W6
96	96		9907004-06		CARTON,DIE CUT,B,200PSI W/ARTWOR	1	1	1	1	
97	97		9907025-06		BAG,ANTISTATIC BUBBLE	1	1	1	1	
98	98		9907092-04		BAG,TRANSLUCENT,ESD PROTECTIVE	1	1	1	1	
99	99		23034E6-00		*** THIS ITEM IS NOT USED ***	-	-	-	-	
100	100		23035E6-00		*** THIS ITEM IS NOT USED ***	-	-	-	-	
101	101		23053L1-00		L1-01	1	1	1	1	E27
102	102		23062E6-00		E6-02	U	1	1	1	E22
103	103		23063E6-00		E6-02	U	1	1	1	E21

- 104 NOTE: M7606-AA IS THE PRIMARY VARIATION OF THE KA630 CPU.
- 105 NOTE: M7606-AC IS THE MODULE USING FUJITSU 256K RAMS.
- 106 NOTE: M7606-AH IS THE MODULE USING NEC 256K RAMS.
- 107 NOTE: M7606-BA IS THE AA VERSION WITHOUT FLOATING POINT.
- 108 NOTE: M7606-BC IS THE MODULE USING FUJITSU 256K RAMS.
- 109 NOTE: M7606-BH IS THE MODULE USING NEC 256K RAMS.
- 110 NOTE: M7606-CA IS THE AA VERSION USING 64K RAMS
- 111 NOTE: M7606-CC IS THE MODULE USING FUJITSU 64K RAMS.
- 112 NOTE: M7606-CH IS THE MODULE USING NEC 64K RAMS.
- 113 NOTE: M7606-DA IS THE CA VERSION WITHOUT FLOATING POINT.
- 114 NOTE: M7606-DC IS THE MODULE USING FUJITSU 64K RAMS.

D	I	G	I	T	A	L	TITLE	MAYFLOWER KA630	SECTION B OF C	SIZE	CODE	DOCUMENT NUMBER	REV
										K	PL	M7606-0-DBP	C

LINE ITEM TOP DOCUMENT

MIN
PART NUMBER REV DESCRIPTION

QTY PER VARIATION

BC BH CA CC REFERENCE DESIGNATOR
D1 D1 D1 D1

VARIATION REVISION LEVEL:

115 NOTE: M7606-DH IS THE MODULE USING NEC 64K RAMS.

D I G I T A L	TITLE MAYFLOWER KA630	SECTION B OF C	SIZE K	CODE PL	DOCUMENT NUMBER M7606-0-DBP	REV C
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LINE ITEM	TOP DOCUMENT	PART NUMBER	MIN REV	DESCRIPTION	VARIATION REVISION LEVEL:	QTY PER VARIATION				REFERENCE DESIGNATOR
						CH D1	DA D1	DC D1	DH D1	
1	1	D-MD-5016523-0-0		5016523-01	CIRCUIT DRILL & ETCH	1	1	1	1	
2	2			1010279-01	.47 MFD 25V 20% CER	6	6	6	6	C30-C35
3	3			1012784-00	.047 MFD 50V +80-20% CER	7	7	7	7	C28,C1-C6
4	4			1013466-05	56.0 MMF 50V 5% CER	1	1	1	1	C67
5	5			1013466-07	220.0 MMF 50V 5% CER	1	1	1	1	C29
6	6			1014265-02	.33 MFD 50V +80-20% CER	58	58	58	58	C7-C27,C42-C66,C68,C69,C71-C80
7	7			1017472-00	10 MFD 35V +75-10% AL EL	3	3	3	3	C39-C41
8	8			1020446-05	22 MFD 16V +50-10% AL EL	2	2	2	2	C37,C38
9	9			1100114-00	PIV= 25 IO=135 MA	1	1	1	1	D9
10	10			1105275-00	PIV= 60 IO=300 MA -15NS	3	3	3	3	D2,D4,D3
11	11			1109977-00	VZ= 4.3 5% 1N749A	1	1	1	1	D1
12	12			1114117-00	PIV= 40 IO= 75 A - 4NS	3	3	3	3	D6-D8
13	13			1114136-02	LED 6.7MA 5V .2MCD GREEN	1	1	1	1	D14
14	14			1120964-01	LED ASSY 4 RED 5V 8MA	1	1	1	1	D10
15	15			1210929-02	FUSE, SUB-MINI 1.000A, 125V, A	2	2	2	2	F1,F2
16	16			1213113-03	HANDLE,MODULE	1	1	1	1	
17	17			1213506-04	PCB HEADER 09PIN(2X05).100CC 90D	1	1	1	1	J3
18	18			1213506-10	PCB HEADER 20PIN(2X10).100CC 90D	1	1	1	1	J2
19	19			1213506-13	PCB HEADER 50PIN(2X25).100CC 90D	1	1	1	1	J1
20	20			1215006-07	SKT,IC 28PIN DIP TIN SOLD	2	2	2	2	XE21,XE22
21	21			1300202-00	47.0 .25 W 5.0 % CF	3	3	3	3	R1,R2,R29
22	22			1300365-00	1.0 K .25 W 5.0 % CF	1	1	1	1	R3
23	23			1300447-00	4.70 K .25 W 5.0 % CF	1	1	1	1	R8
24	24			1300479-00	10.0 K .25 W 5.0 % CF	2	2	2	2	R11,R12
25	25			1301808-00	22.0 K .25 W 5.0 % CF	1	1	1	1	R4
26	26			1302388-00	2.0 K .25 W 5.0 % CF	1	1	1	1	R14
27	27			1302466-00	100.0 K .25 W 5.0 % CF	1	1	1	1	R16
28	28			1304837-00	24.0 K .25 W 5.0 % CF	1	1	1	1	R7
29	29			1314637-00	R NETWORK 3-22 1.0 % 6PIN	4	4	4	4	R31-R34
30	30			1316334-02	R NETWORK 9-10K 2.0 % 10PIN	2	2	2	2	R10,R23

REVISION HISTORY		BASIC PART NO: M7606		DRN: RONALD RHOADES	DATE: 01-FEB-84	D I G I T A L			
ENG	ECO NUMBER	REV	SECTION C OF C	CHK'D: DAVID DROZD	DATE: 17-MAY-84	TITLE PARTS LIST			
---	INITIAL	A	SECTION VARIATION INDEX	DES.ENG: BARRY MASKAS	DATE: 22-MAY-84	DOCUMENT NUMBER			
BM	M7606-ML001	B	[A] AA,AC,AH,BA	RESP.ENG.: BARRY MASKAS	DATE: 8-AUG-84	SIZE	CODE	NUMBER	REV
BM	M7606-ML002	C	[B] BC,BH,CA,CC	MFG.ENG.: BILL SCHULTE	DATE: 22-MAY-84	K	PL	M7606-0-DBP	C
			[C] CH,DA,DC,DH	ASSEMBLY NUMBER: D-UA-M7606-0-0	TOP DOCUMENT NUMBER: B-DD-M7606-0-0	RELEASE DATE: 19-JUN-85		FILE NAME: Z8847C.PLS	EDIT #: 37
			[D]						
			[E]						
			[F]						
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			[M]						
			[N]						

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LINE	ITEM	TOP DOCUMENT	PART NUMBER	MIN REV	DESCRIPTION	QTY PER VARIATION				REFERENCE DESIGNATOR
						CH	DA	DC	DH	
						D1	D1	D1	D1	
31	31		1316395-02		R NETWORK 9-1.0K 2.0 % 10PIN	1	1	1	1	R9
32	32		1317404-00		249.0 .25 W 1.0 % RN55D-F10	1	1	1	1	R13
33	33		1317558-01		R NETWORK 4-27 5.0 % 8PIN	2	2	2	2	R39,R40
34	34		1318110-00		R NETWORK 11-330 11-680 13PIN	4	4	4	4	R24-R27
35	35		1319610-01		750.0 K .25 W .10% RN55E-B 2	1	1	1	1	R17
36	36		1319645-01		487.0 K .25 W .10% RN55E-B 2	1	1	1	1	R18
37	37		1321144-01		R NETWORK 5-220 2.0% 10PIN	1	1	1	1	R28
38	38		1321218-01		R NETWORK 4-39 +-10HM 8PIN	4	4	4	4	R35-R38
39	39		1811660-05		OSCILLATOR, XTAL 33.330 MHZ	1	1	1	1	Y3
40	40		1811660-62		OSCILLATOR, XTAL 614.4 KHZ	1	1	1	1	Y2
41	41		1814057-00		*** THIS ITEM IS NOT USED ***	-	-	-	-	
42	42		1818800-00		OSCILLATOR, XTAL 32.768KHZ	1	1	1	1	Y1
43	43		1911469-B0		8640 BURNED-IN RECEIVER, B	1	1	1	1	E16
44	44		1912803-B0		LS04 BURNED-IN INVERTER G	1	1	1	1	E25
45	45		1913471-B0		LS367 BURNED-IN DRIVER, BUS	1	1	1	1	E41
46	46		1914140-01	LM	211P COMPARATOR, VOLTAGE	1	1	1	1	E29
47	47		1914987-00		8641-2 TRANSCEIVER, UNIBUS, QU	4	4	4	4	E5, E7, E19, E24
48	48		1915193-B0		LS244 BURNED-IN DRIVER, LIN	1	1	1	1	E28
49	49		1915219-B0		LS373 BURNED-IN FF-0 OCTAL	1	1	1	1	E1
50	50		1915415-B0		9636 BURNED-IN DRIVER, DUA	1	1	1	1	E23
51	51		1916028-B1		9643 BURNED-IN DRIVER, TTL	1	1	1	1	E15
52	52		1918868-B0		LS26 NAND GATE, 2-IN, HIGH	1	1	1	1	E35
53	53		1919015-00	DC	021 BUS TRANSCEIVER, 20PI	3	3	3	3	E11, E30, E36
54	54		1919542-B1		9639 RECEIVER, LINE, DUAL, P	1	1	1	1	E18
55	55		1919684-01	LM	385B2 PREC VOLT REF. 1.23	1	1	1	1	D5
56	56		1920441-B1		74F245 TRANSCEIVER, BI-DIREC	4	4	4	4	E52, E71, E85, E99
57	57		1920442-B1		74F374 FF-D, OCTAL, TRI-STATE	2	2	2	2	E8, E12
58	58		1920853-B1		LS646 BUS TRANSCEIVER/REGI	2	2	2	2	E9, E10
59	59		1921008-B1		74F240 BUFFER/LINE DRIVER, O	2	2	2	2	E80, E94
60	60		1921010-B1		74F373 OCTAL TRANSPARENT LA	5	5	5	5	E2, E6, E46, E53, E73
61	61		1921305-B1		74F00 NAND GATE, QUAD, 2-IN,	1	1	1	1	E47
62	62		1921306-B1		74F02 NOR GATE, QUAD, 2-IN, B	1	1	1	1	E38
63	63		1921307-B1		74F04 HEX INVERTER, BURNED	2	2	2	2	E32, E87
64	64		1921312-B1		74F32 OR GATE, QUAD, 2-IN, BU	2	2	2	2	E37, E65
65	65		1921314-B1		74F74 FF-D, DUAL, BURNED-IN	2	2	2	2	E31, E34
66	66		1921321-B1		74F158 MUX, QUAD, 2-IN, BURNED	3	3	3	3	E72, E93, E101
67	67		1921323-B1		74F174 FF-D, HEX, BURNED-IN	2	2	2	2	E17, E59
68	68		1921417-B1		74F521 COMPARATOR, IDENTITY,	1	1	1	1	E66
69	69		1922871-01		TRANSCEIVER, PARITY B	4	4	4	4	E58, E64, E92, E106
70	70		1923679-B1		74F537 DECODER/DEMUX, 1-OF-1	1	1	1	1	E100
71	71		2117312-00		UART DL-11 SOFTWARE	1	1	1	1	E13
72	72		2118467-02		8264-15 RAM 64K X1, 150NS 1	-	-	36	-	E48-E51, E54-E57, E60-E63, E67-E70, CONT E74-E77, E81-E84, E88-E91, E95-E98, CONT E102-E105
73	73		2118472-02		4164-3 MOS RAM 64K X1, 150	36	-	-	36	E48-E51, E54-E57, E60-E63, E67-E70, CONT E74-E77, E81-E84, E88-E91, E95-E98, CONT E102-E105
74	74		2118795-00		146818 CLOCK/CALENDAR/RAM	1	1	1	1	E14

D	I	G	I	T	A	L	TITLE	SECTION C OF C	SIZE	CODE	DOCUMENT NUMBER	REV
							MAYFLOWER KA630		K	PL	M7606-0-DBP	C

LINE	ITEM	TOP DOCUMENT	PART NUMBER	MIN REV	DESCRIPTION	QTY PER VARIATION				REFERENCE DESIGNATOR
						CH D1	DA D1	DC D1	DH D1	
75	75		2120887-01		DC 333 MICROVAX,32BIT 68PIN	1	1	1	1	E43
76	76		2121384-02		RAM 8KX8,STATIC 150	2	2	2	2	E3,E4
77	77		2121413-02		*** THIS ITEM IS NOT USED ***	-	-	-	-	
78	78		2121415-02		*** THIS ITEM IS NOT USED ***	-	-	-	-	
79	79		2122797-01		DC 337 MICROVAX FLOATING PO	1	-	-	-	E42
80	80		2123389-01		GATE ARRAY,3200 GATE	1	1	1	1	E45
81	81		2123413-01		DC379 CMOS GATE ARRAY,144PGA,320	1	1	1	1	E44
82	82		23007L3-00		L3-01	1	1	1	1	E39
83	83		23008L3-00		L3-01 FPLS	1	1	1	1	E20
84	84		23009L3-00		L3-01	1	1	1	1	E26
85	85		23010L3-00		L3-01	1	1	1	1	E33
86	86		23018E6-00		*** THIS ITEM IS NOT USED ***	-	-	-	-	
87	87		23019E6-00		*** THIS ITEM IS NOT USED ***	-	-	-	-	
88	88		23036L1-00		*** THIS ITEM IS NOT USED ***	-	-	-	-	
89	89		23115F2-00		F2-03	1	1	1	1	E79
90	90		23169J5-00		J5-03 PAL,LOGIC	1	1	1	1	E40
91	91		23170J5-00		J5-03 PAL,LOGIC	1	1	1	1	E78
92	92		23171J5-00		J5-03 PAL,LOGIC	1	1	1	1	E86
93	93		23E42F1-00		*** THIS ITEM IS NOT USED ***	-	-	-	-	
94	94		9000024-01		EYELET,ROLLED 0.1210DX0.192	4	4	4	4	
95	95		9009185-00		JUMPER, WIRE, INSULATED, BLACK B	3	3	3	3	W2,W3,W6
96	96		9907004-06		CARTON,DIE CUT,B,200PSI W/ARTWOR	1	1	1	1	
97	97		9907025-06		BAG,ANTISTATIC BUBBLE	1	1	1	1	
98	98		9907092-04		BAG,TRANSLUCENT,ESD PROTECTIVE	1	1	1	1	
99	99		23034E6-00		*** THIS ITEM IS NOT USED ***	-	-	-	-	
100	100		23035E6-00		*** THIS ITEM IS NOT USED ***	-	-	-	-	
101	101		23053L1-00		L1-01	1	1	1	1	E27
102	102		23062E6-00		E6-02	U 1	1	1	1	E22
103	103		23063E6-00		E6-02	U 1	1	1	1	E21

- 104 NOTE: M7606-AA IS THE PRIMARY VARIATION OF THE KA630 CPU.
- 105 NOTE: M7606-AC IS THE MODULE USING FUJITSU 256K RAMS.
- 106 NOTE: M7606-AH IS THE MODULE USING NEC 256K RAMS.
- 107 NOTE: M7606-BA IS THE AA VERSION WITHOUT FLOATING POINT.
- 108 NOTE: M7606-BC IS THE MODULE USING FUJITSU 256K RAMS.
- 109 NOTE: M7606-BH IS THE MODULE USING NEC 256K RAMS.
- 110 NOTE: M7606-CA IS THE AA VERSION USING 64K RAMS
- 111 NOTE: M7606-CC IS THE MODULE USING FUJITSU 64K RAMS.
- 112 NOTE: M7606-CH IS THE MODULE USING NEC 64K RAMS.
- 113 NOTE: M7606-DA IS THE CA VERSION WITHOUT FLOATING POINT.
- 114 NOTE: M7606-DC IS THE MODULE USING FUJITSU 64K RAMS.
- 115 NOTE: M7606-DH IS THE MODULE USING NEC 64K RAMS.

D	I	G	I	T	A	L	TITLE	SECTION C OF C	SIZE	CODE	DOCUMENT NUMBER	REV
							MAYFLOWER KA630		K	PL	M7606-0-DBP	C

KA630-AA, -AB, -AC, -AD (M7606) DRAWING DIRECTORY

DATA PATH

- 0 MICROVAX II SYSTEM
- 1 KA630 - uVAX on Q22 Bus
 - 1.1 uVAX & FPU
 - 1.1.1 uVAX & FPU PINOUTS
 - 1.2 ADDRESS LATCH/LOCAL MEMORY DECODE
 - 1.3 Memory Subsystem
 - 1.4 Q22 Bus Interface Gate Array
 - 1.4.1-1.4.2, 1.4.1.1-1.4.1.9
 - 1.5 Translation Map Group
 - 1.6 KA630 QBUS INTERFACE
 - 1.7 uVAX Interface Gate Array
 - 1.7.1-1.7.2, 1.7.2.1-1.7.2.10
 - 1.8 TOY CLOCK
 - 1.9 Console Serial Line Interface
 - 1.10 LEDS and Configuration Connector
 - 1.11 Decoupling Capacitors

CONTROL

- 2 KA630 State Machines
 - 2.1 uVAX Cycle Controller
 - 2.1.1 MEMORY SEQUENCER
 - 2.1.2 MEMORY SEQUENCER SUPPORT
 - 2.2 Q22 BUS STATE MACHINES

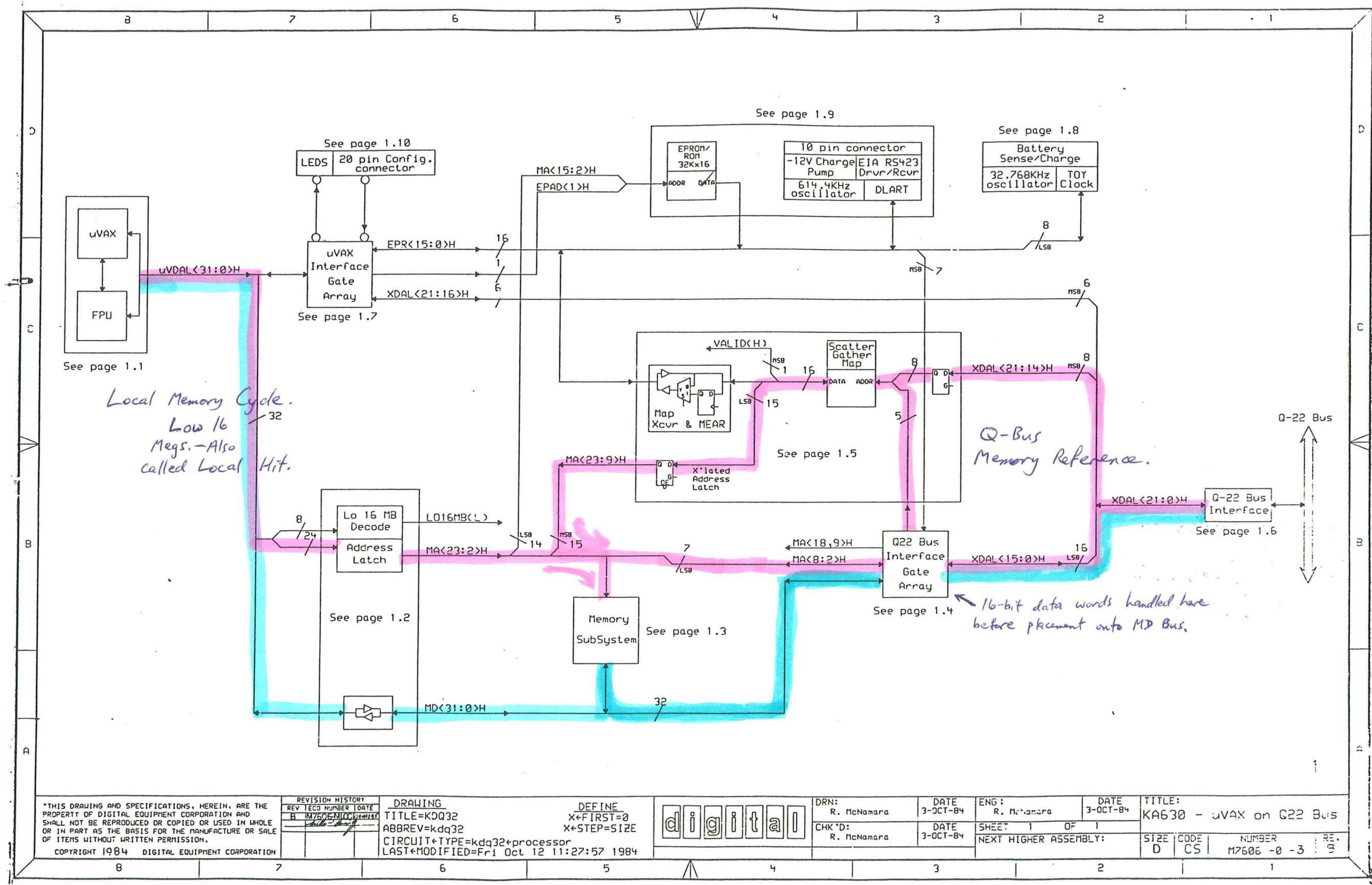
MISC.

- 3 KA630 MEMORY ARBITER LISTING
 - 3.1-3.2 KA630 MEMORY ARBITER FLOW DIAGRAM
- 4 KA630 LOCAL I/O CONTROL MACHINE LISTING
 - 4.1 KA630 LOCAL I/O CONTROL MACHINE FLOW DIAGRAM
- 5 Q22 BUS ARBITRATION CONTROL MACHINE LISTING
 - 5.1 Q22 BUS ARBITRATION CONTROL MACHINE FLOW DIAGRAM
- 6 Q22 BUS MASTER CONTROL MACHINE LISTING
 - 6.1 Q22 BUS MASTER CONTROL MACHINE FLOW DIAGRAM
- 7 Q22 BUS SLAVE CONTROL MACHINE LISTING
 - 7.1-7.2 Q22 BUS SLAVE CONTROL MACHINE FLOW DIAGRAM
- 8 1KX4 RAS DECODE PROM (E79) LISTING
- 9 PALASM LISTINGS FOR PAL16L8A DEVICES
- 10 MNEMONIC DICTIONARY

DRAWING DEFINE
 TITLE=DIRECTORY X+FIRST=0
 ABBREV=DIRECT X+STEP=SIZE
 CIRCUIT+TYPE=DOCUMENTATION
 LAST+MODIFIED=Sun Dec 9 16:50:34 1984

REVISION	Joe M. Muller
CHK	CHANGE NO
REV	REV
M7606M001 B	
JOE M. MULLIN	

digital	DRN	ENG	DATE	TITLE
	MASKAS & McNamara	MASKAS & McNamara	8-DEC-83	M7606 DRAWING DIRECTORY
USRA	DATE	BOARD LOCATION	SIZE	CODE
FIRST USED ON OPTION/MODEL	TOP DOCUMENT NUMBER:		D	CS
			M7605	-0 -1



*Local Memory Cycle.
Low 16
Megs. - Also
called Local Hit.*

*Q-Bus
Memory Reference.*

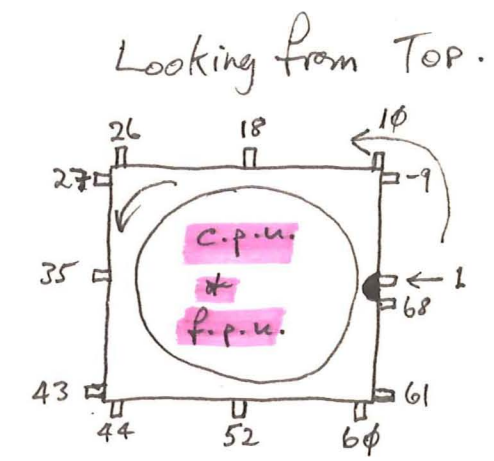
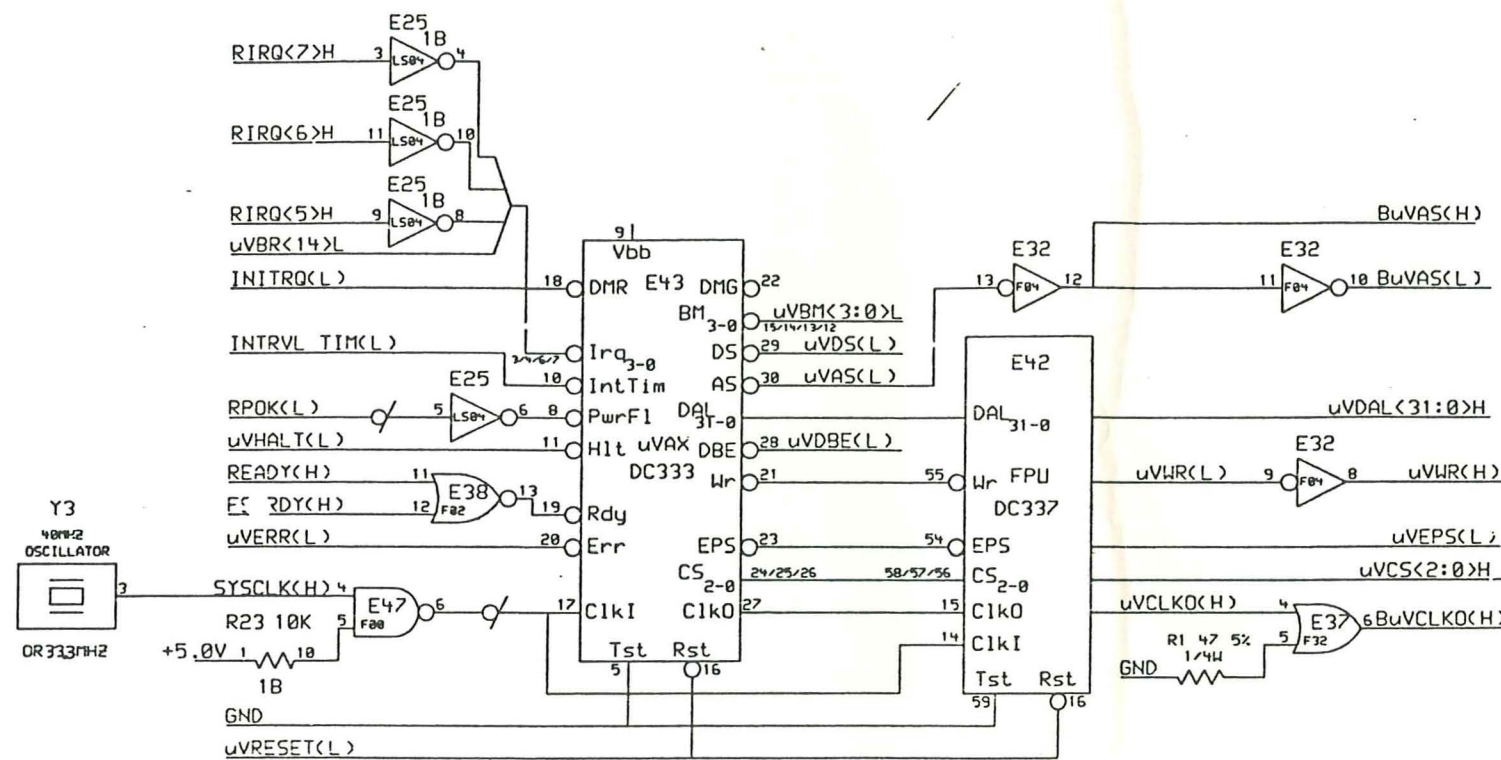
*16-bit data words handled here
before placement onto MD Bus.*

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REVISION HISTORY			DRAWING		DEFINE	
REV	ECO NUMBER	DATE	TITLE	ABBREV	X+FIRST=0	X+STEP=SIZE
B	11750	10/12/84	KDQ32	kdq32		
			CIRCUIT+TYPE=kdq32+processor			
			LAST+MODIFIED=Fri Oct 12 11:27:57 1984			

digital

DRN: R. McNamara	DATE 3-OCT-84	ENG: R. McNamara	DATE 3-OCT-84	TITLE: KA630 - uVAX on G22 Bus
CHK'D: R. McNamara	DATE 3-OCT-84	SHEET 1 OF 1	NEXT HIGHER ASSEMBLY:	SIZE CODE NUMBER RE. D CS M7606 -0 -3 10



uVAS<L> CYCLES

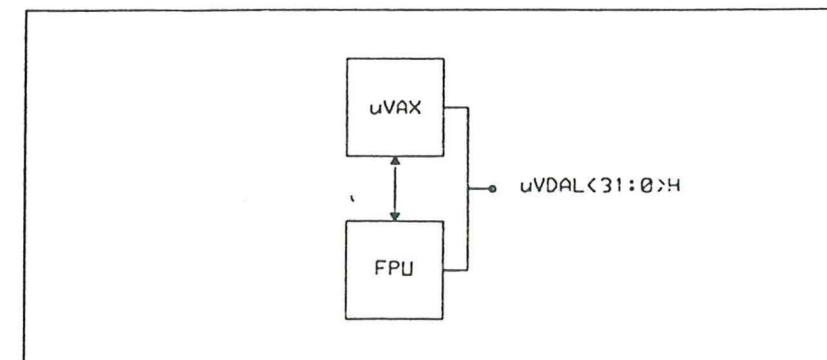
uVCS<2:0>H uVWR<L>

- LHH H interrupt acknowledge (IAK)
- HLH H read (1 - stream)
- HLH H read (lock)
- HHx H read (0 - stream)
- HLH L write (unlock)
- HHH L write (0 - stream)
- x => don't care

uVEPS<L> CYCLES

uVCS<2:0>H uVWR<L>

- HLH H read data
- HHH H read response (uVCS<2> pulled low by responder)
- HLL L write command (fpu)
- HLH L write data
- HHL L write command (non-fpu)



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REV	ECO	NUMBER	DATE
1			

DRAWING
TITLE=UVAX
ABBREV=UVAX+FPU
CIRCUIT+TYPE=UVAX/FPU
LAST+MODIFIED=Fri Nov 9 18:39:57 1984

DEFINE
X<FIRST=0
X<STEP=SIZE

digital

DRN:
BARRY MASKAS
CHK'D:
BARRY MASKAS

DATE
3-OCT-84
DATE
3-OCT-84

ENG:
BARRY MASKAS
SHEET 1 OF 1
NEXT HIGHER ASSEMBLY:

DATE
3-OCT-84

TITLE:
UVAX & FPU

SIZE CODE D ICS
NUMBER 17506-0-1
REV B



MM54HC245/MM74HC245 Octal TRI-STATE® Transceiver

General Description

These TRI-STATE bi-directional buffers utilize micro-CMOST™ Technology, 3.5 micron silicon gate P-well CMOS, and are intended for two-way asynchronous communication between data buses. They have high drive current outputs which enable high speed operation even when driving large bus capacitances. This circuit possesses the low power consumption and high noise immunity usually associated with CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits.

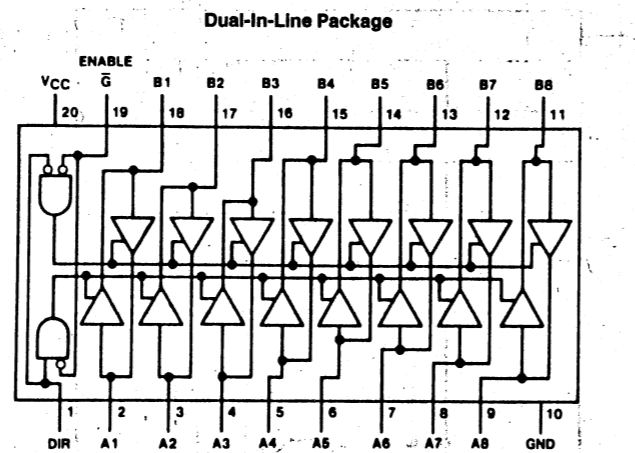
Each device has an active low enable input \bar{G} and a direction control input, DIR. When DIR is high, data flows from the A inputs to the B outputs. When DIR is low, data flows from the B inputs to the A outputs. The MM54HC245/MM74HC245 transfers true data from one bus to the other.

This device can drive up to 15 LS-TTL Loads, and does not have Schmitt trigger inputs. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 14 ns
- Wide power supply range: 2–6V
- Low quiescent current: 80 μ A maximum (74 HC)
- Tri-State outputs for connection to bus oriented systems
- High output drive: 6 mA (minimum)

Connection Diagram

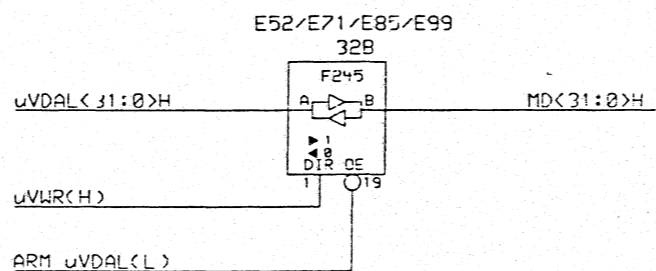
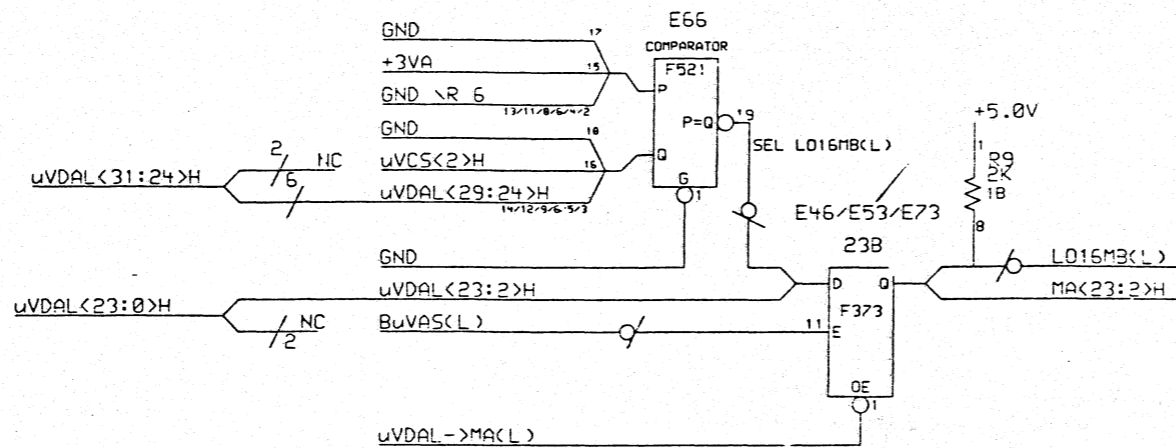


MM54HC245/MM74HC245
54HC245 (J) 74HC245 (J,N)

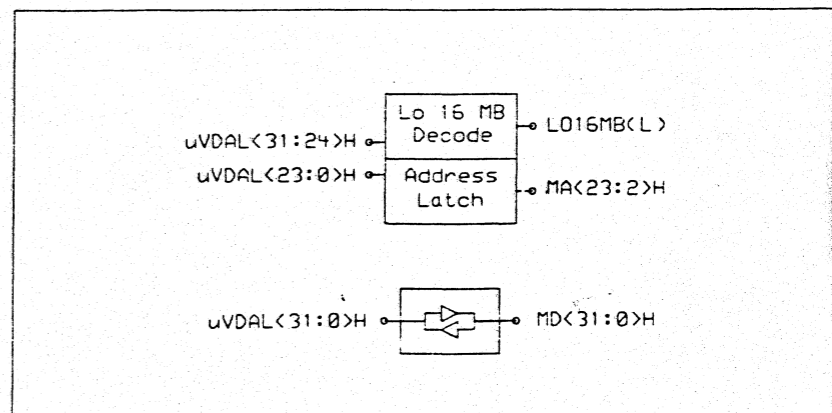
Truth Table

Control Inputs		Operation
\bar{G}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = high level, L = low level, X = irrelevant



1.2



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REVISION HISTORY	
REV	DATE
1	10/20/84

DRAWING
TITLE=ADDR LATCH
ABBREV=ADLATCH
CIRCUIT+TYPE=ADDR+LATCH
LAST*MODIFIED=Sat Oct 20 18:19:02 1984

DEFINE
X+FIRST=0
X+STEP=SIZE

DESIGNED BY: BARRY MASKAS
CHECKED BY: BARRY MASKAS

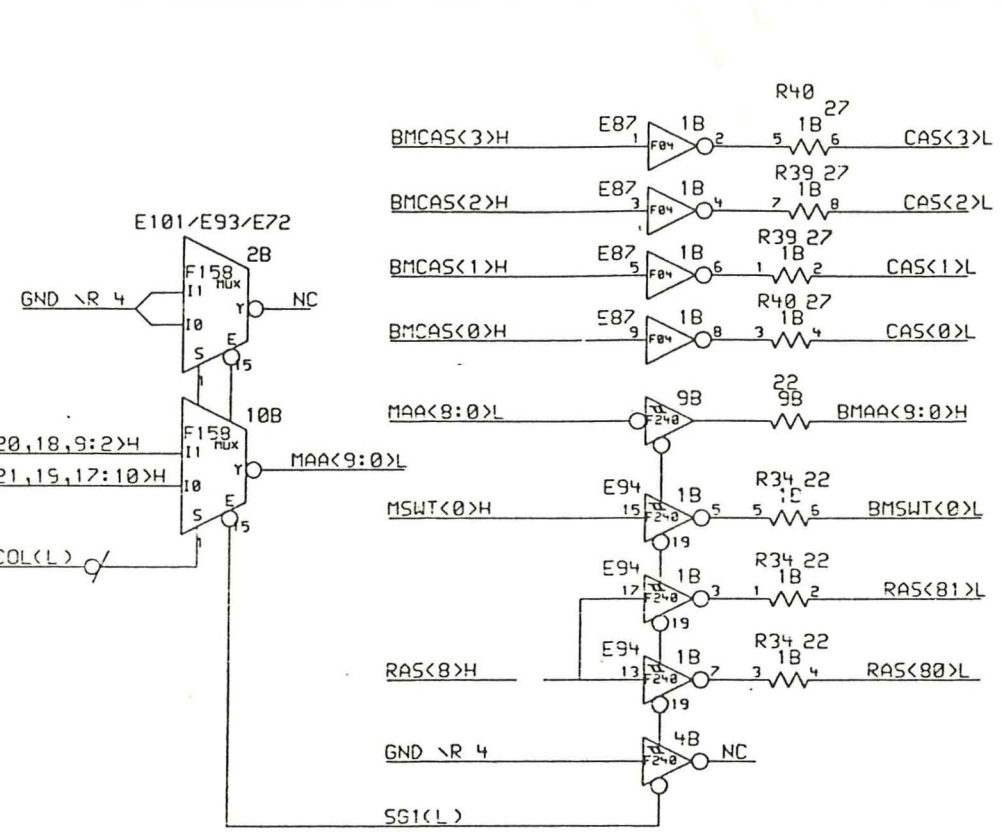
DATE: 3-OCT-84

ENGINEER: BARRY MASKAS
DATE: 3-OCT-84

SHEET 1 OF 1

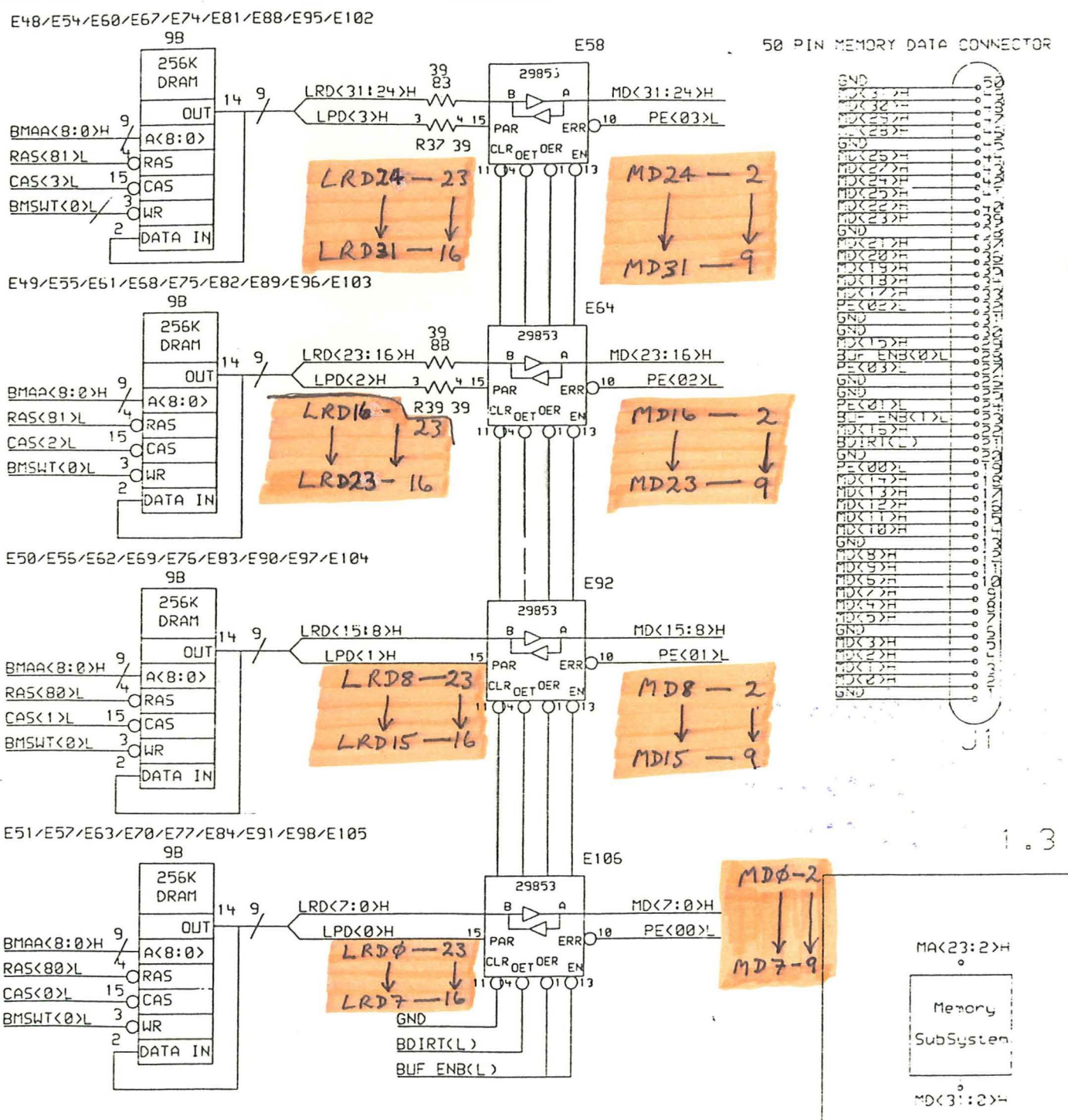
TITLE: ADDRESS LATCH/
LOCAL MEMORY DECODE
NEXT HIGHER ASSEMBLY:
SIZE: U CODE: CS NUMBER: M7525 -0 -3 REV: B

8 7 6 5 4 3 2



MODULE CD CONNECTORS

GND	1	C11	GND	1	D11
RAS<0>H	1	C12	RAS<6>H	1	D12
MSID<4>L	1	C13			
MAA<8>L	1	C14	BMCAS<3>H	1	D13
MAA<0>L	1	C15	BMCAS<2>H	1	D14
MAA<2>L	1	C16	BMCAS<1>H	1	D15
MAA<1>L	1	C17	BMCAS<0>H	1	D16
MSID<1>L	1	C18	RAS<2>H	1	D17
RAS<4>H	1	C19	RAS<3>H	1	D18
MSWT<1>H	1	C20	RAS<7>H	1	D19
MSID<0>L	1	C21	RAS<3>L	1	D20
BMCAS<1>H	1	C22	MAA<6>L	1	D21
RAS<1>H	1	C23	MAA<3>L	1	D22
BMCAS<0>H	1	C24	MAA<4>L	1	D23
RAS<5>H	1	C25	MAA<5>L	1	D24
GND	1	C26	GND	1	D25
MAA<9>L	1	C27	MAA<7>L	1	D26
+5.0V	1	C28	+5.0V	1	D27



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REVISION HISTORY
 REV. IECO NUMBER DATE
 H M7505-1100 1984

DRAWING TITLE=MEM ABBREV=MEM CIRCUI+TYPE=MEMEORY LAST+MODIFIED=Mon Oct 29 09:26:41 1984

DEFINE X+FIRST=0 X+STEP=SIZE

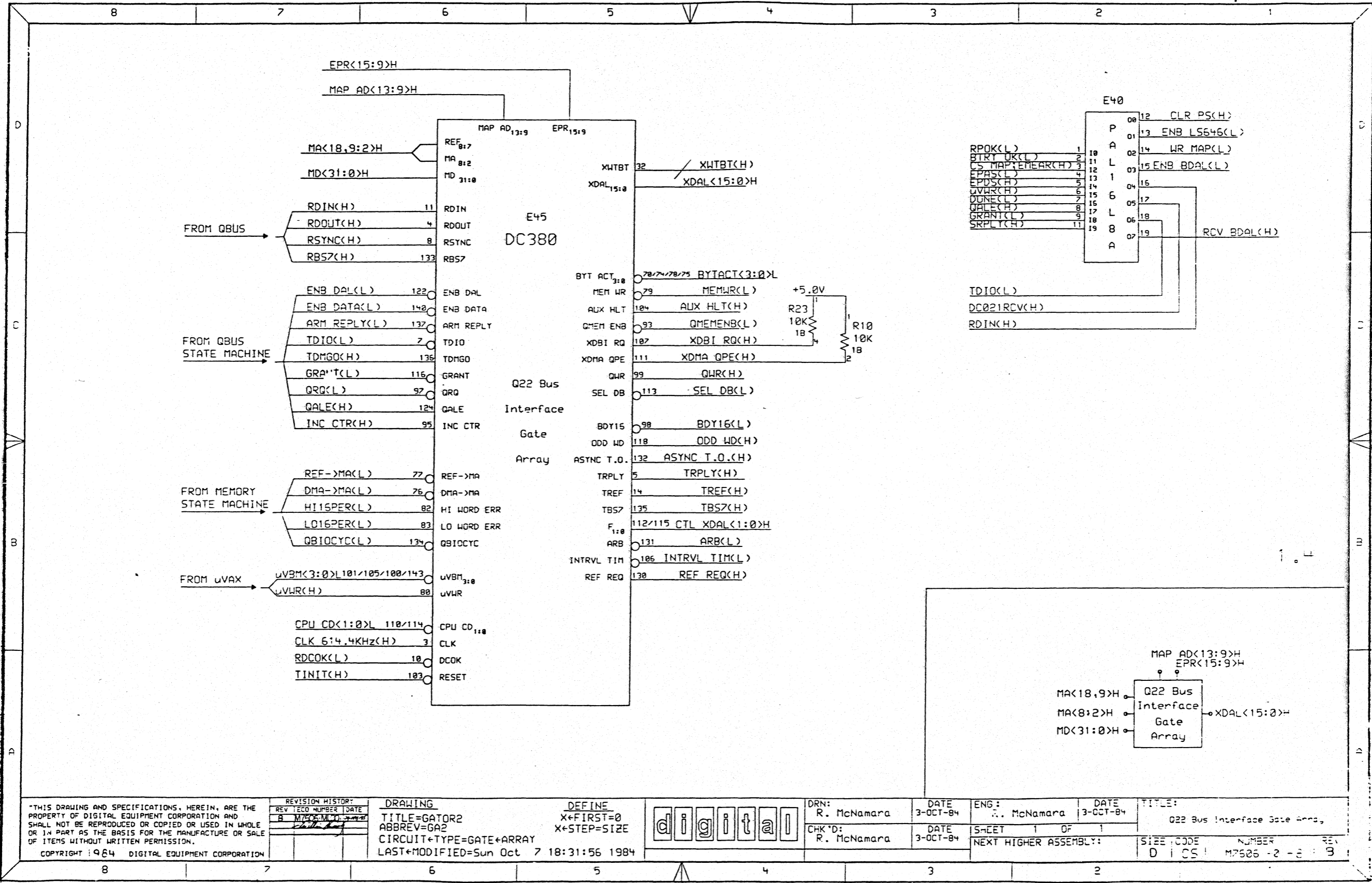
digital

DRN: BARRY MASKAS DATE 3-OCT-84 ENG: BARRY MASKAS DATE 3-OCT-84 TITLE: Memory SubSystem

CHK'D: BARRY MASKAS DATE 3-OCT-84 SHEET 1 OF 1 NEXT HIGHER ASSEMBLY:

SIZE CODE NUMBER REV
 D CS 17505-11-7 B

8 7 6 5 4 3 2



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REVISION HISTORY:		
REV	TECO NUMBER	DATE
A	M7505-2-2	3-84

DRAWING
 TITLE=GATOR2
 ABBREV=GA2
 CIRCUIT+TYPE=GATE+ARRAY
 LAST+MODIFIED=Sun Oct 7 18:31:56 1984

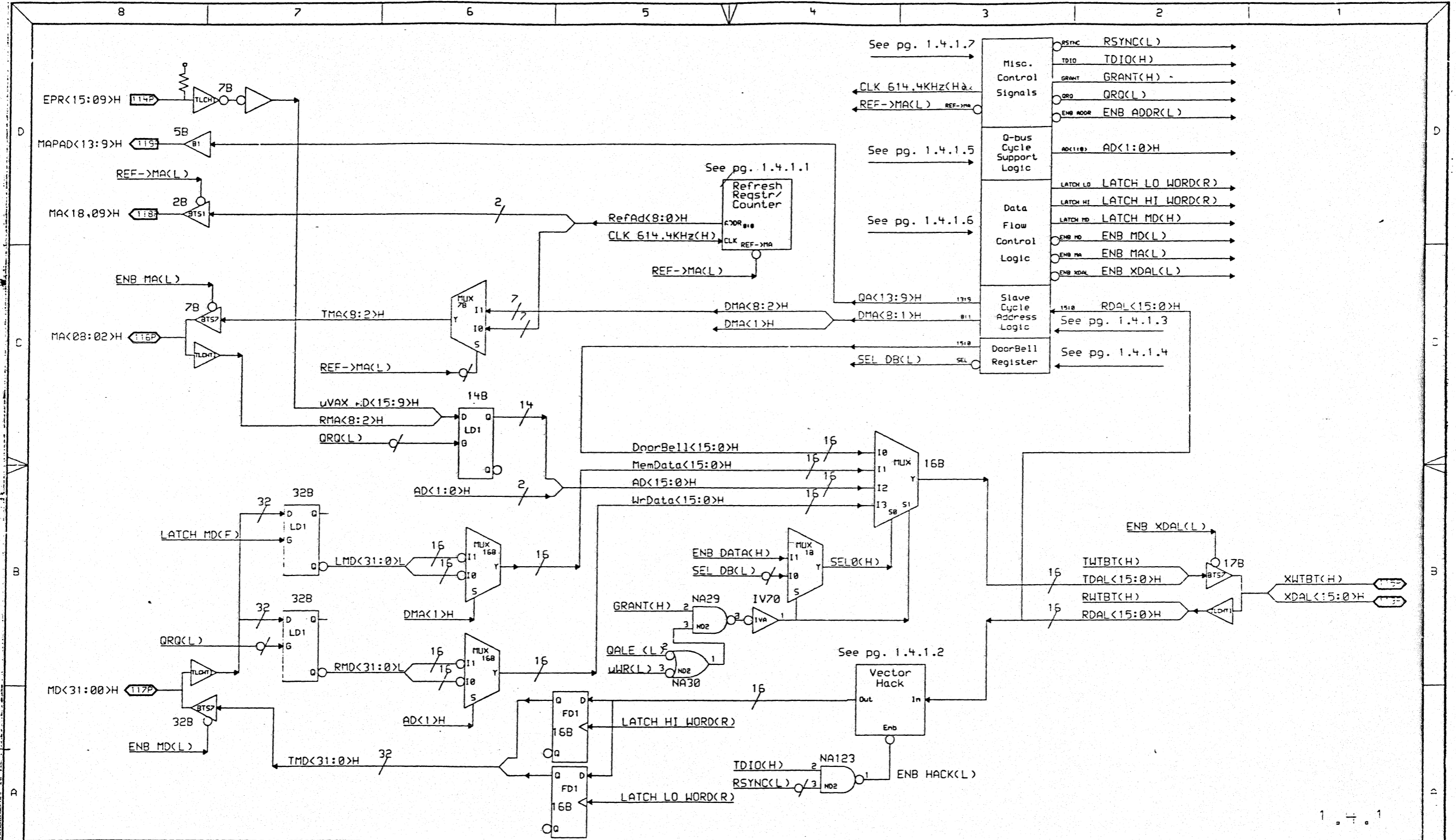
DEFINE
 X+FIRST=0
 X+STEP=SIZE

digital

DRN:
R. McNamara
 DATE
3-OCT-84
 CHK'D:
R. McNamara
 DATE
3-OCT-84

ENG:
R. McNamara
 DATE
3-OCT-84
 SHEET 1 OF 1
 NEXT HIGHER ASSEMBLY:

TITLE:
Q22 Bus Interface Gate Array,
 SIZE CODE NUMBER
 D | CS | M7505 -2 -2 | 3



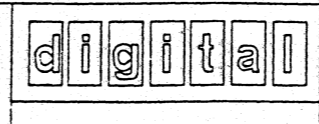
1.4.1

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REVISION HISTORY		
REV	ECO NUMBER	DATE
B	M752-MIC	10-21-84

DRAWING
 TITLE=GA2
 ABBREV=GA2
 LAST*MODIFIED=Tue Oct 9 14:46:23 1984

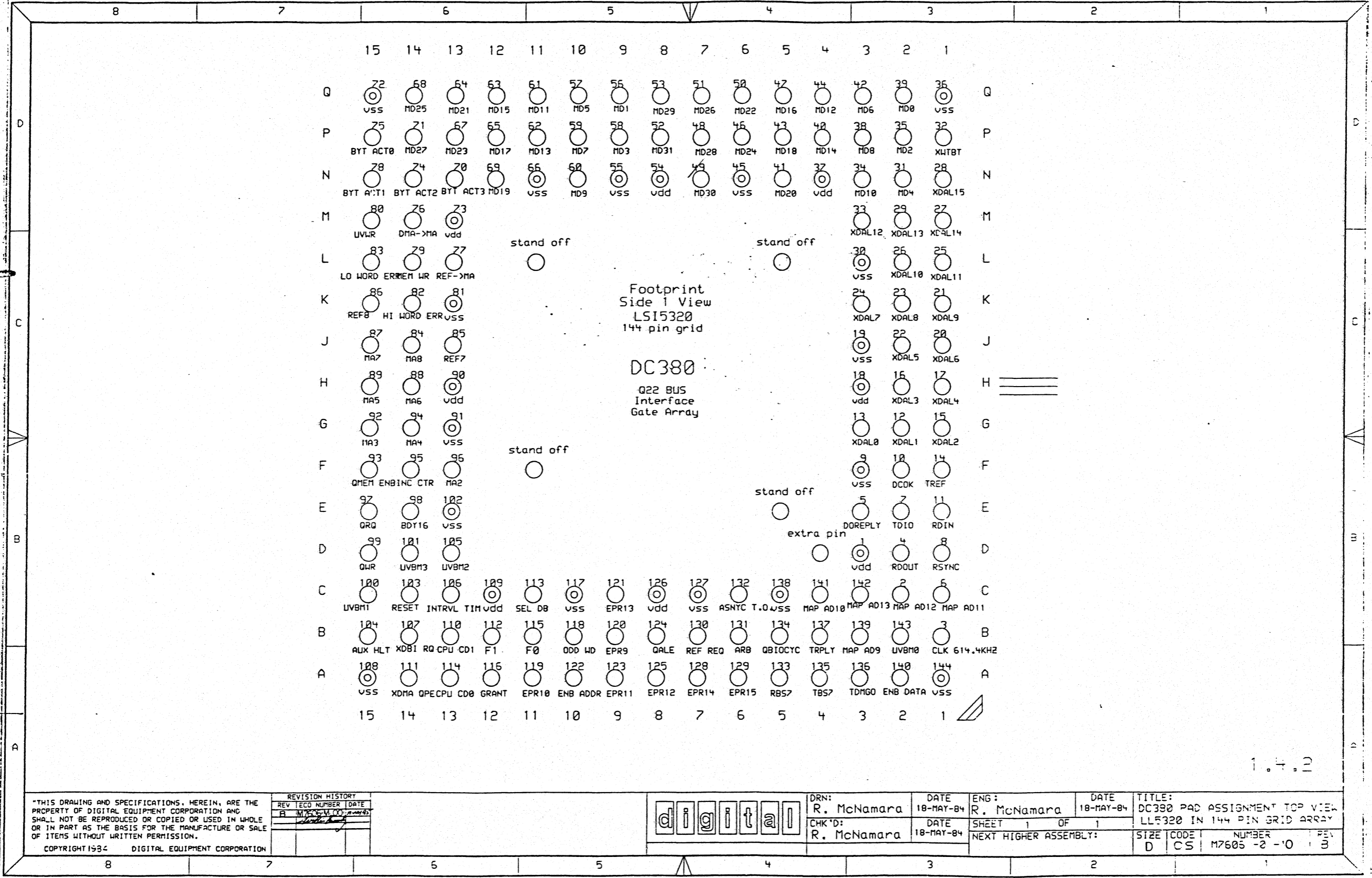
DEFINE
 X*FIRST=0
 X*STEP=SIZE



DRN: R. McNamara
 DATE: 15-DEC-83
 CHK'D: R. McNamara
 DATE: 15-DEC-83

ENG: R. McNamara
 DATE: 15-DEC-83
 SHEET 1 OF 1
 NEXT HIGHER ASSEMBLY:

TITLE: Q22 Bus Interface Gate Array
 SIZE: CODE D | cs
 NUMBER: 17505-0-3
 REV: 1



Footprint
Side 1 View
LSI5320
144 pin grid

DC380
Q22 BUS
Interface
Gate Array

1.4.2

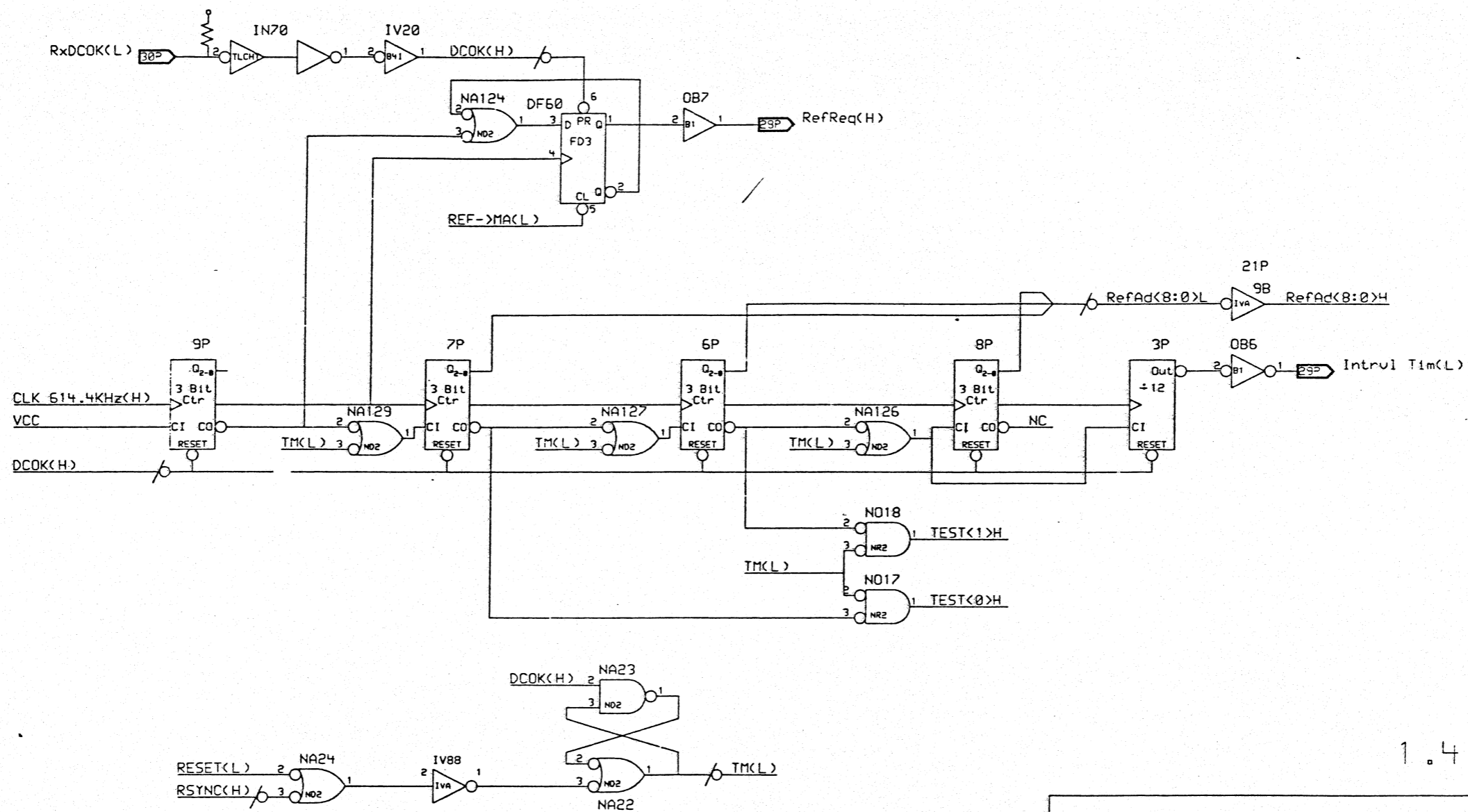
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REVISION HISTORY		
REV	ECO NUMBER	DATE
1		

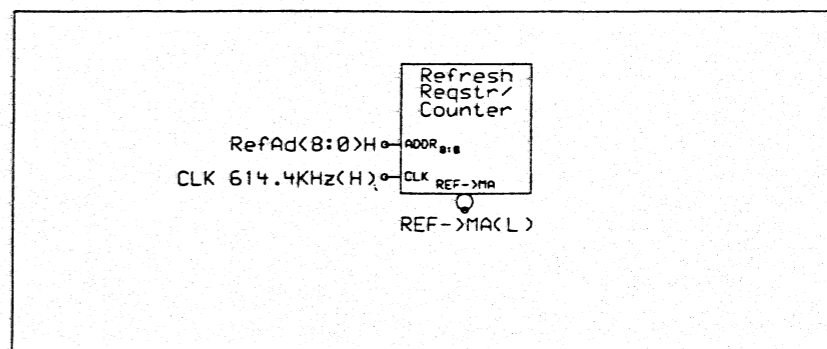
digital

DRN: R. McNamara	DATE 18-MAY-84	ENG: R. McNamara	DATE 18-MAY-84
CHK'D: R. McNamara	DATE 18-MAY-84	SHEET 1	OF 1
NEXT HIGHER ASSEMBLY:		SIZE CODE NUMBER D CS M7605 -2 -10 3	

TITLE: DC380 PAD ASSIGNMENT TOP VIEW LSI5320 IN 144 PIN GRID ARRAY			
SIZE D	CODE CS	NUMBER M7605 -2 -10	REV 3



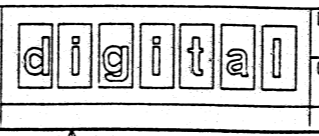
1.4.1.1



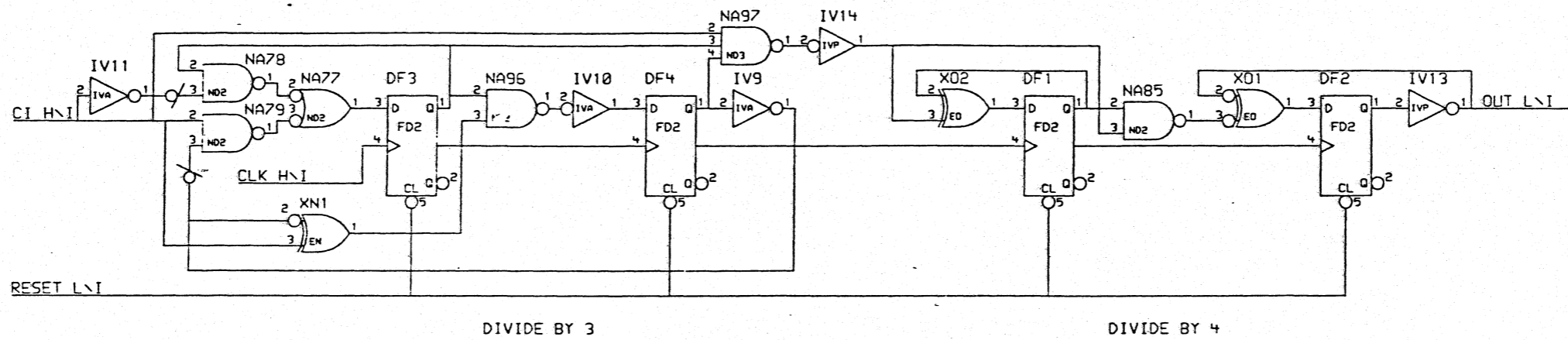
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REVISION HISTORY		
REV	ECO NUMBER	DATE
B	M7626-00-11	13-NOV-83

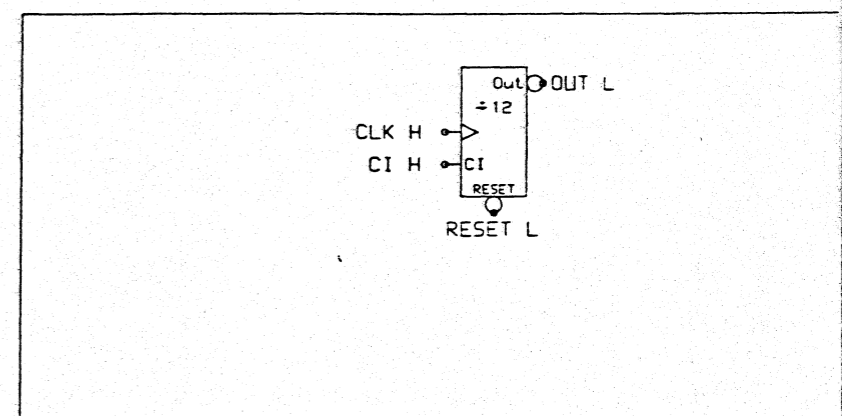
DRAWING
 LAST MODIFIED=Wed Oct 10 19:06:07 1984



DRN: R. McNamara	DATE 13-NOV-83	ENG: R. McNamara	DATE 13-NOV-83	TITLE: REFRESH LOGIC/COUNTER
CHK'D: R. McNamara	DATE 13-NOV-83	SHEET 1 OF 1	NEXT HIGHER ASSEMBLY:	SIZE D
				CODE CS
				NUMBER M7626 -0 -11
				REV B



1.4.1.1.1

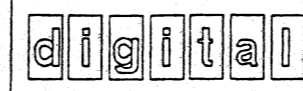


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REVISION HISTORY	
REV	ECO NUMBER DATE
1	11/13/83 R.McNamara

DRAWING
 TITLE=DIV BY 12
 ABBREV=DIV12
 LAST*MODIFIED=NOT WRITTEN

DEFINE
 X*FIRST=0
 X*STEP=SIZE

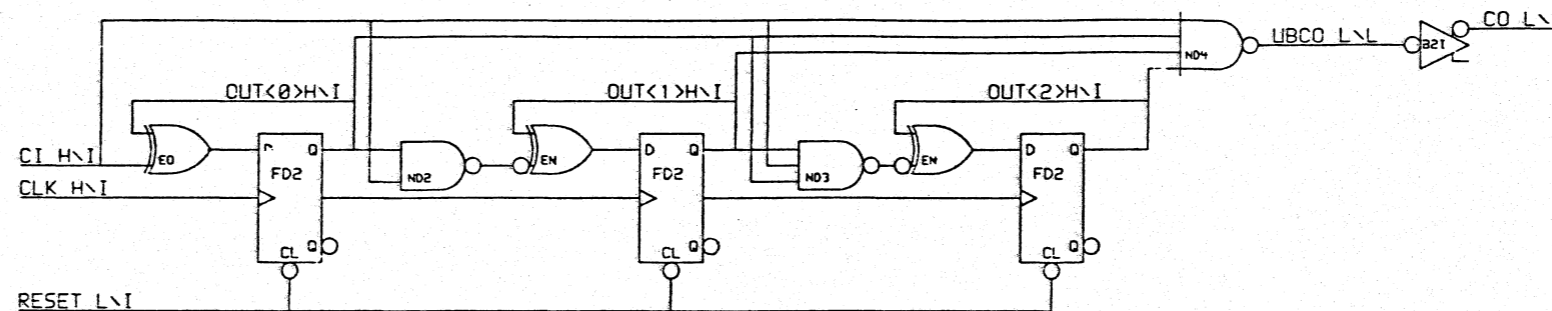


DRN:
 R. McNamara
 CHK'D:
 R. McNamara

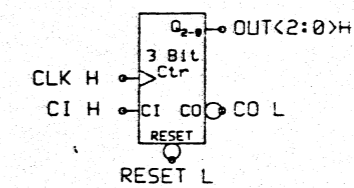
DATE
 13-NOV-83
 DATE
 13-NOV-83

ENG:
 R. McNamara
 SHEET 1 OF 1
 NEXT HIGHER ASSEMBLY:

TITLE:
 Divide by 12
 SIZE CODE NUMBER
 D 05 M7626 -2 -12
 REV. B



1.4.1.1.2



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REVISION HISTORY		
REV	ECO NUMBER	DATE
1	M7505-001	11/06/83

DRAWING
TITLE=3 BIT CTR
ABBREV=3BCTR
CIRCUIT+TYPE=3BITCTR
LAST*MODIFIED=Sat Oct 20 18:47:47 1984

DEFINE
X*FIRST=0
X*STEP=SIZE

digital

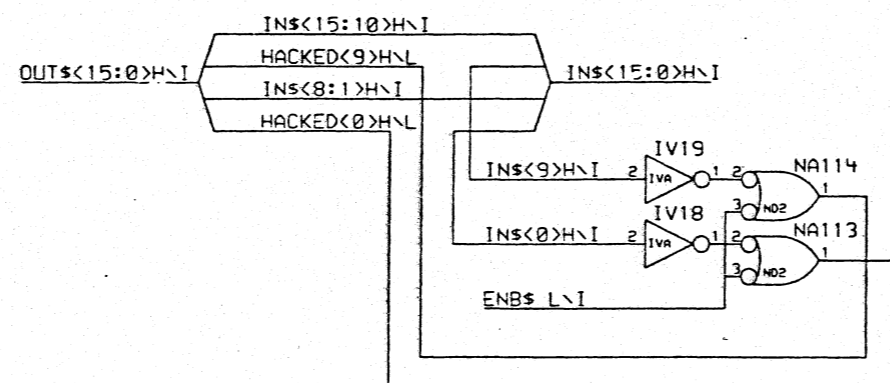
DRN:
R. McNamara
CHK'D:
R. McNamara

DATE
6-NOV-83
DATE
6-NOV-83

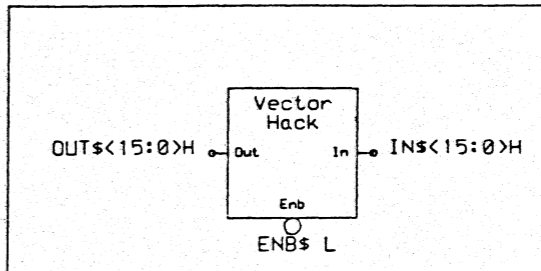
ENG:
R. McNamara
SHEET 1 OF 1
NEXT HIGHER ASSEMBLY:

TITLE:
Synchronous 3 Bit Counter

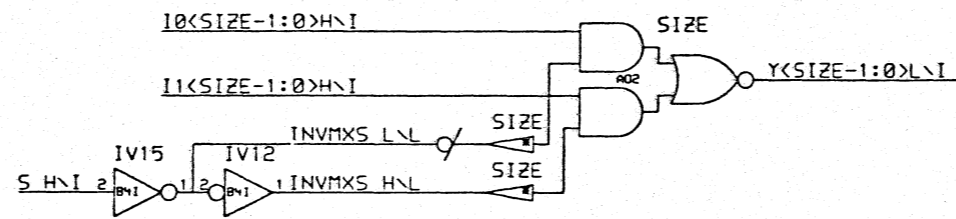
SIZE CODE NUMBER REV
D ICS M7505-0-3 E



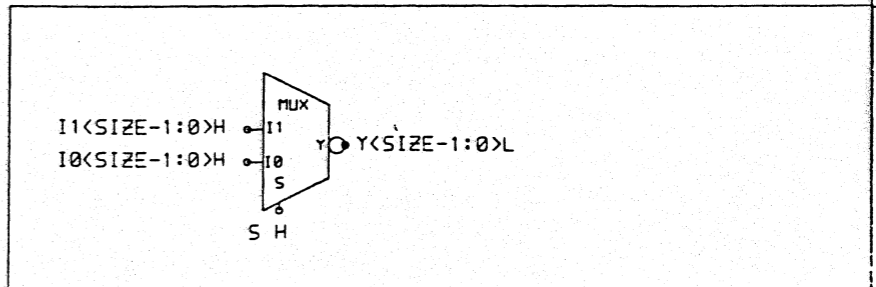
1.4.1.2



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	COPYRIGHT 1984 DIGITAL EQUIPMENT CORPORATION										



1.4.1.2A



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REVISION HISTORY		
REV	ECO NUMBER	DATE
B	IMVCS MOD	

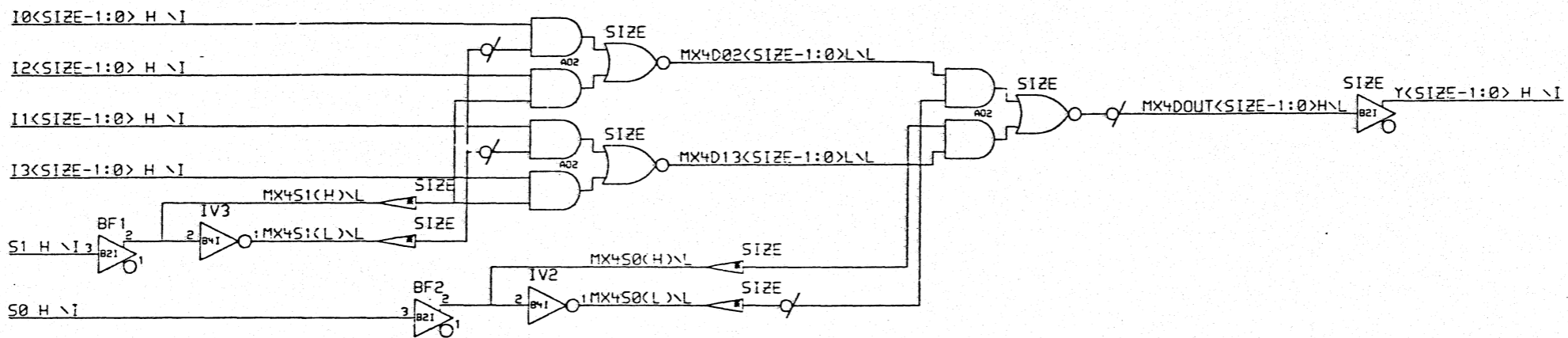
DRAWING
 TITLE=INV MUX
 ABBREV=INVMX
 LAST+MODIFIED=Wed Oct 10 19:20:46 1984

DEFINE
 X+FIRST=0
 X+STEP=SIZE
 digital

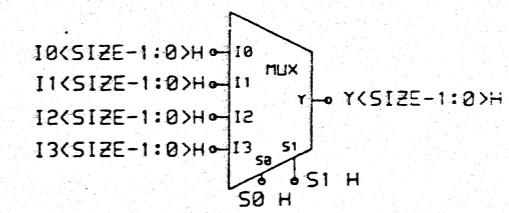
DRN:
R. McNamara
 CHK'D:
R. McNamara

DATE	ENG:	DATE
23-Jan-84	R. McNamara	23-Jan-84
DATE	SHEET	OF
23-Jan-84	1	1
NEXT HIGHER ASSEMBLY:		

TITLE:
Inverting MUX
Logic
 SIZE | CODE | NUMBER | REV
 D | CS | M7505 -0 -15 | B



1.4.1.2B



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REVISION HISTORY		
REV	ECO NUMBER	DATE
B	M7625-2-16	10-JAN-84

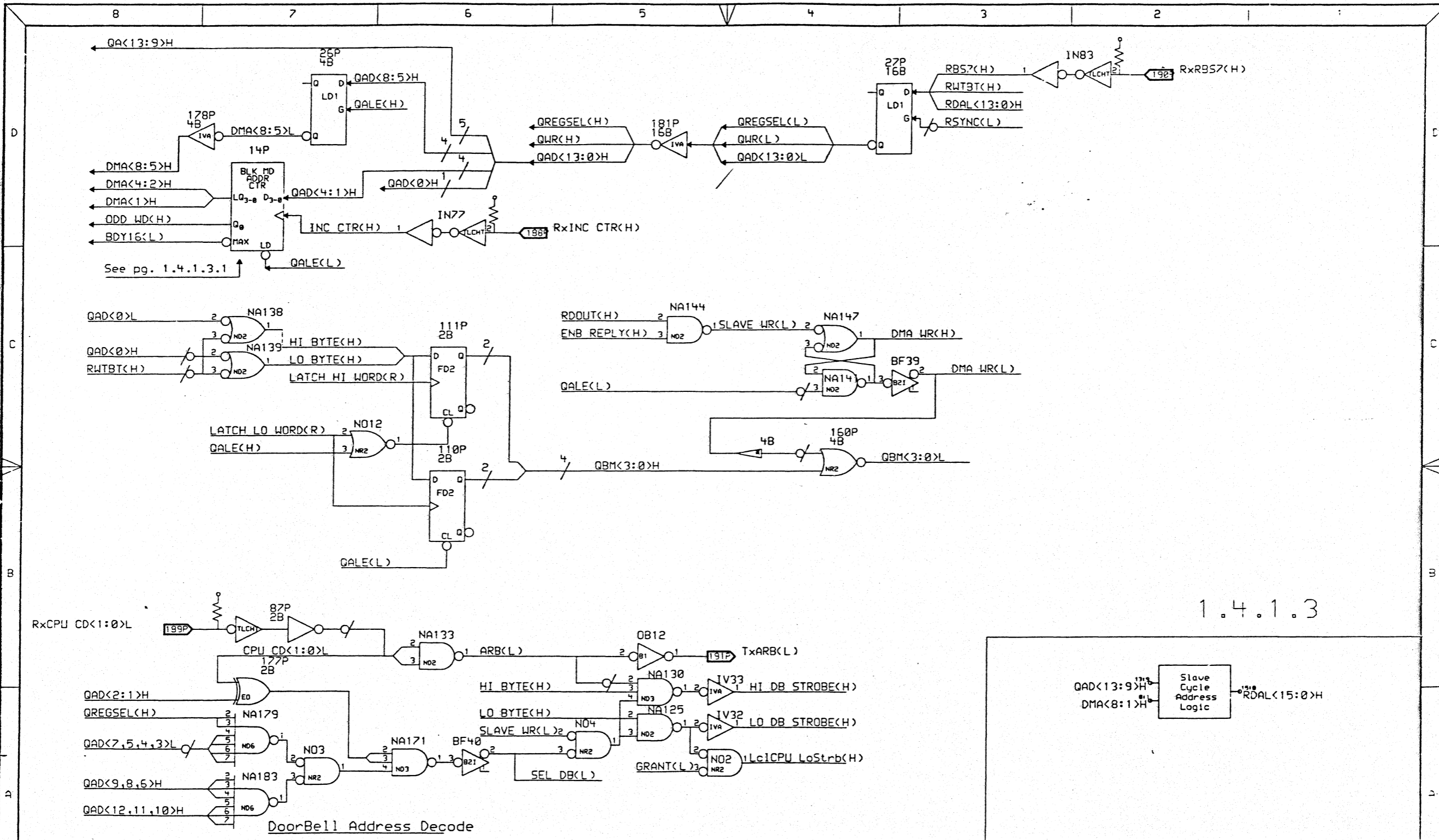
DRAWING TITLE=4MUX
ABBREV=4MX
LAST*MODIFIED=Wed Oct 10 19:23:47 1984

DEFINE
X*FIRST=0
X*STEP=SIZE
digital

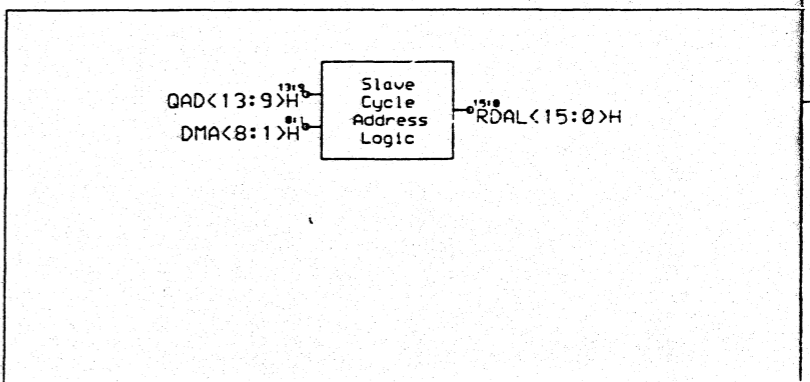
DRN: R. McNamara
CHK'D: R. McNamara

DATE 10-JAN-84
DATE 10-JAN-84
SHEET 1 OF 1
NEXT HIGHER ASSEMBLY:

ENG: R. McNamara
DATE 10-JAN-84
TITLE: 4 to 1 MUX
SIZE CODE: D | CS | NUMBER: M7625-2-16 REV: 5



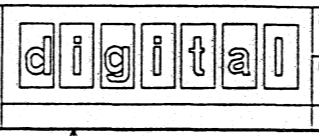
1.4.1.3



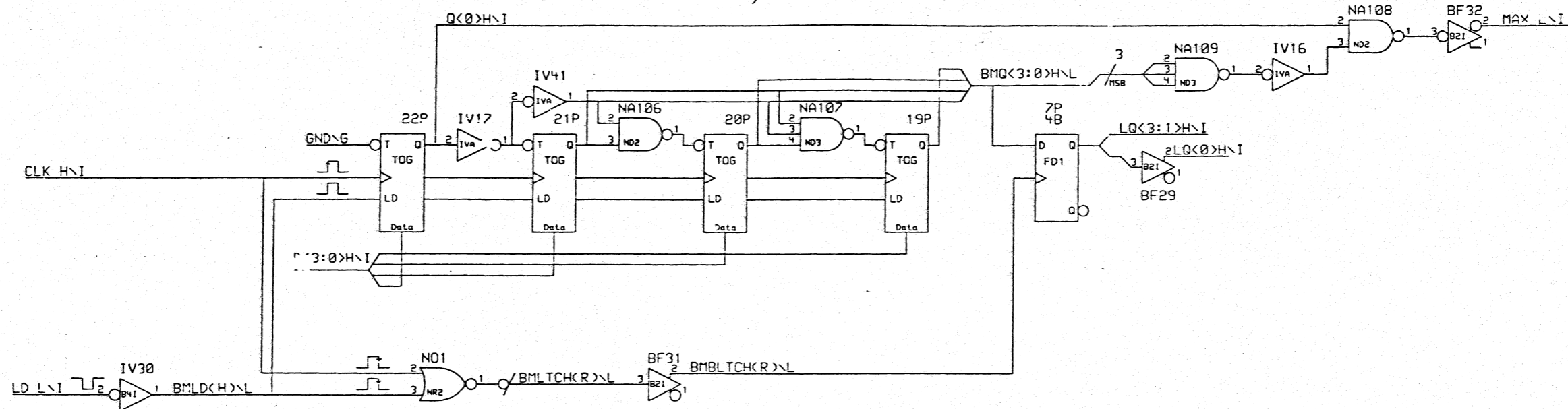
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REVISION HISTORY		
REV	TECO NUMBER	DATE
1	17205	10/10/84
2	17205	10/10/84

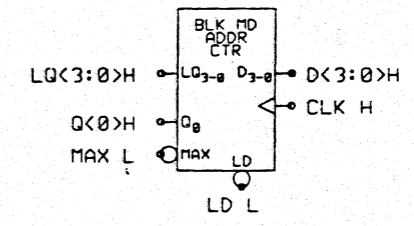
DRAWING
 LAST MODIFIED=Wed Oct 10 19:32:56 1984



DRN: R. McNamara	DATE 16-NOV-83	ENG: R. McNamara	DATE 16-NOV-83	TITLE: Q-bus Support Logic
CHK'D: R. McNamara	DATE 16-NOV-83	SHEET 1 OF 1	NEXT HIGHER ASSEMBLY:	SIZE CODE NUMBER REV D 35 M7605 -2 -17 B



1.4.1.3.1

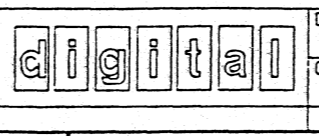


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REVISION HISTORY		
REV	ECO NUMBER	DATE
0		10/10/84

DRAWING
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ABBREV=BMCTR
CIRCUIT+TYPE=BLKMDCTR
LAST+MODIFIED=Wed Oct 10 19:28:01 1984

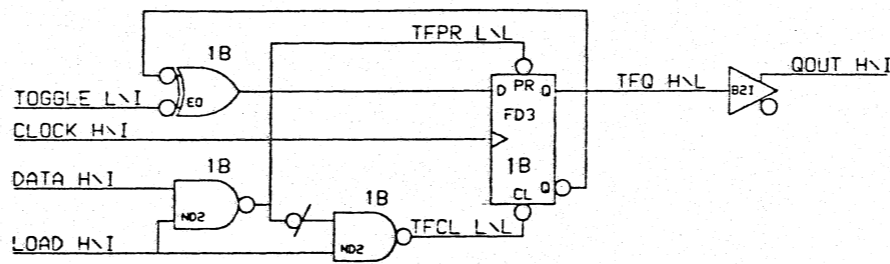
DEFINE
X+FIRST=0
X+STEP=SIZE



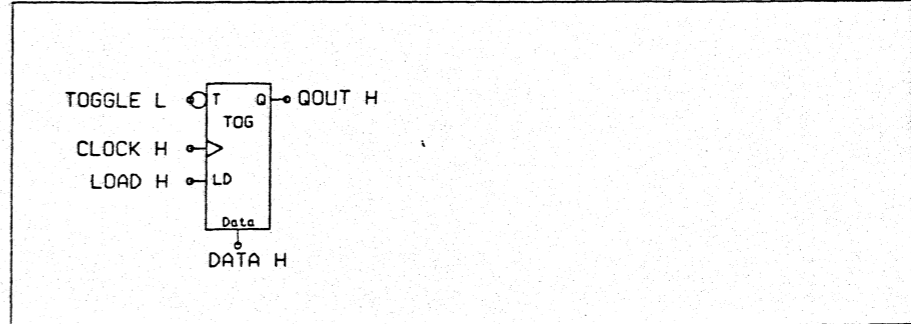
DRN:
R. McNamara
CHK'D:
R. McNamara

DATE
6-NOV-83
DATE
6-NOV-83
SHEET 1 OF 1
NEXT HIGHER ASSEMBLY:

TITLE:
BLK MD CTR LOGIC
SIZE CODE NUMBER
D CS M7505-0-18 REV F



1.4.1.3.1.1



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REVISION HISTORY		
REV	ECO NUMBER	DATE
A	1768-AL001	11/06/83

DRAWING
TITLE=TOG
ABBREV=TOG
LAST+MODIFIED=Wed Oct 10 19:57:28 1984

DEFINE
X+FIRST=0
X+STEP=SIZE

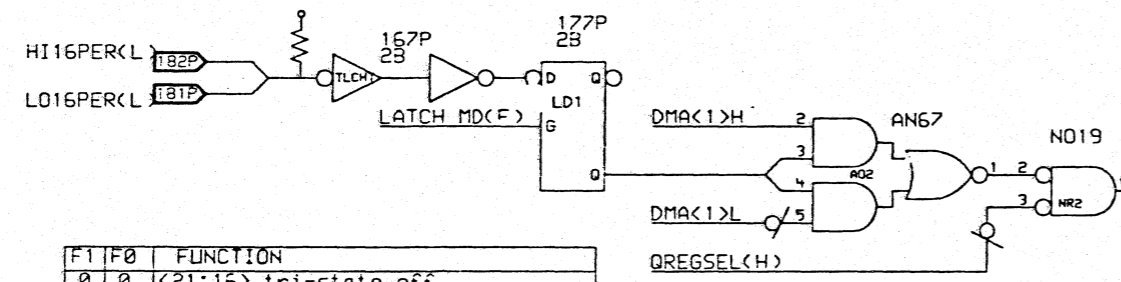
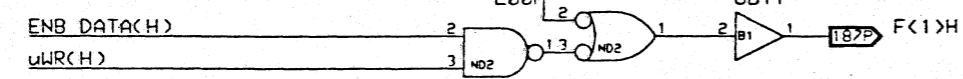
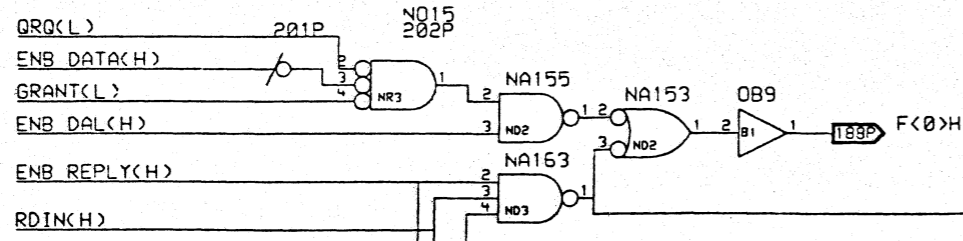
digital

DRN:
R. McNamara
CHK'D:
R. McNamara

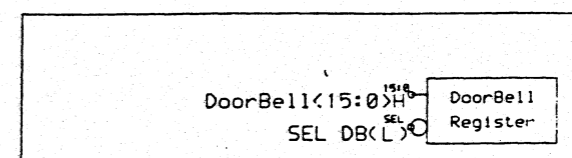
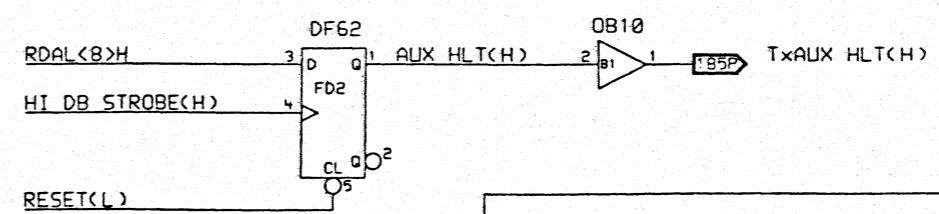
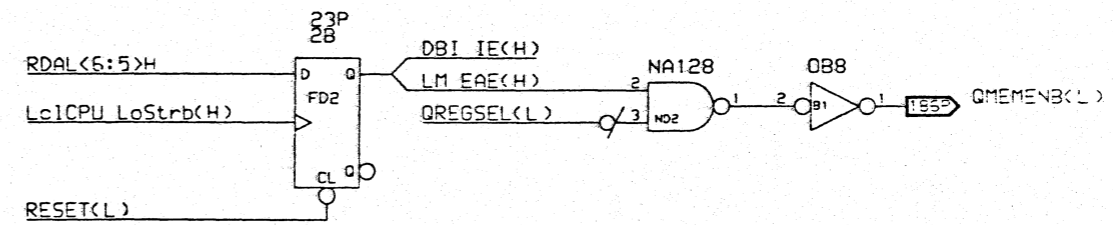
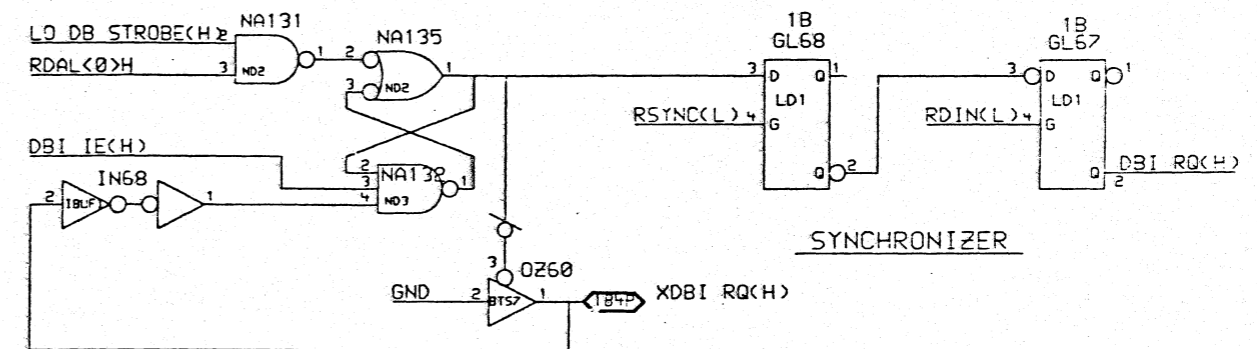
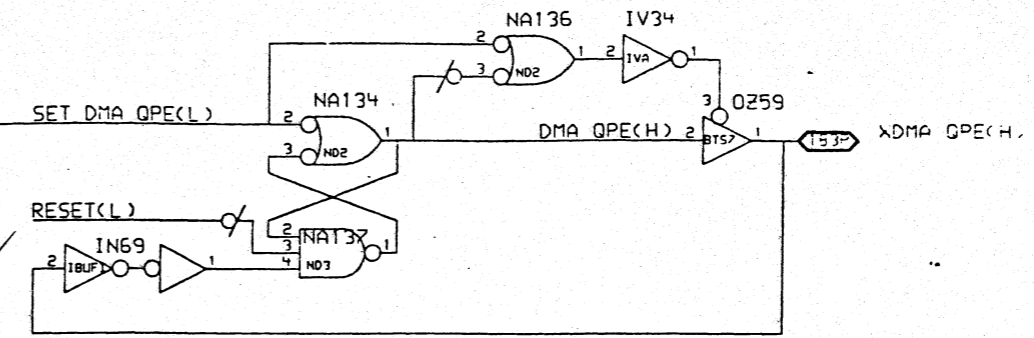
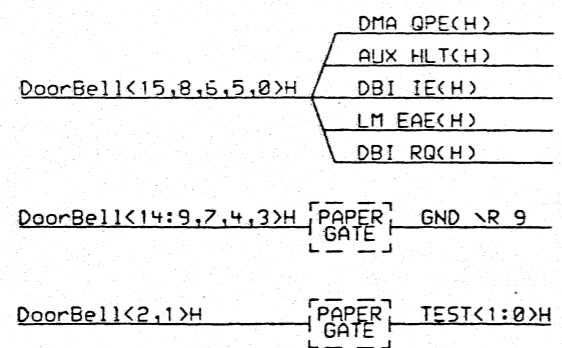
DATE	6-NOV-83
DATE	6-NOV-83

ENG.	R. McNamara	DATE	6-NOV-83	TITLE:	TOGGLE FLOP
SHEET	1	OF	1	SIZE	1000E
NEXT HIGHER ASSEMBLY:				NUMBER	19
				REV.	6

8 7 6 5 4 3 2



F1	F0	FUNCTION
0	0	<21:16> tri-state off
0	1	drive addresses <21:16>
1	0	drive <21:17> -> 0
1	1	drive <21:18> -> 0, <17:16> -> 1



1.4.1.4

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REVISION HISTORY		
REV	ECO NUMBER	DATE
1	1	11/01/83
2	1	10/10/84

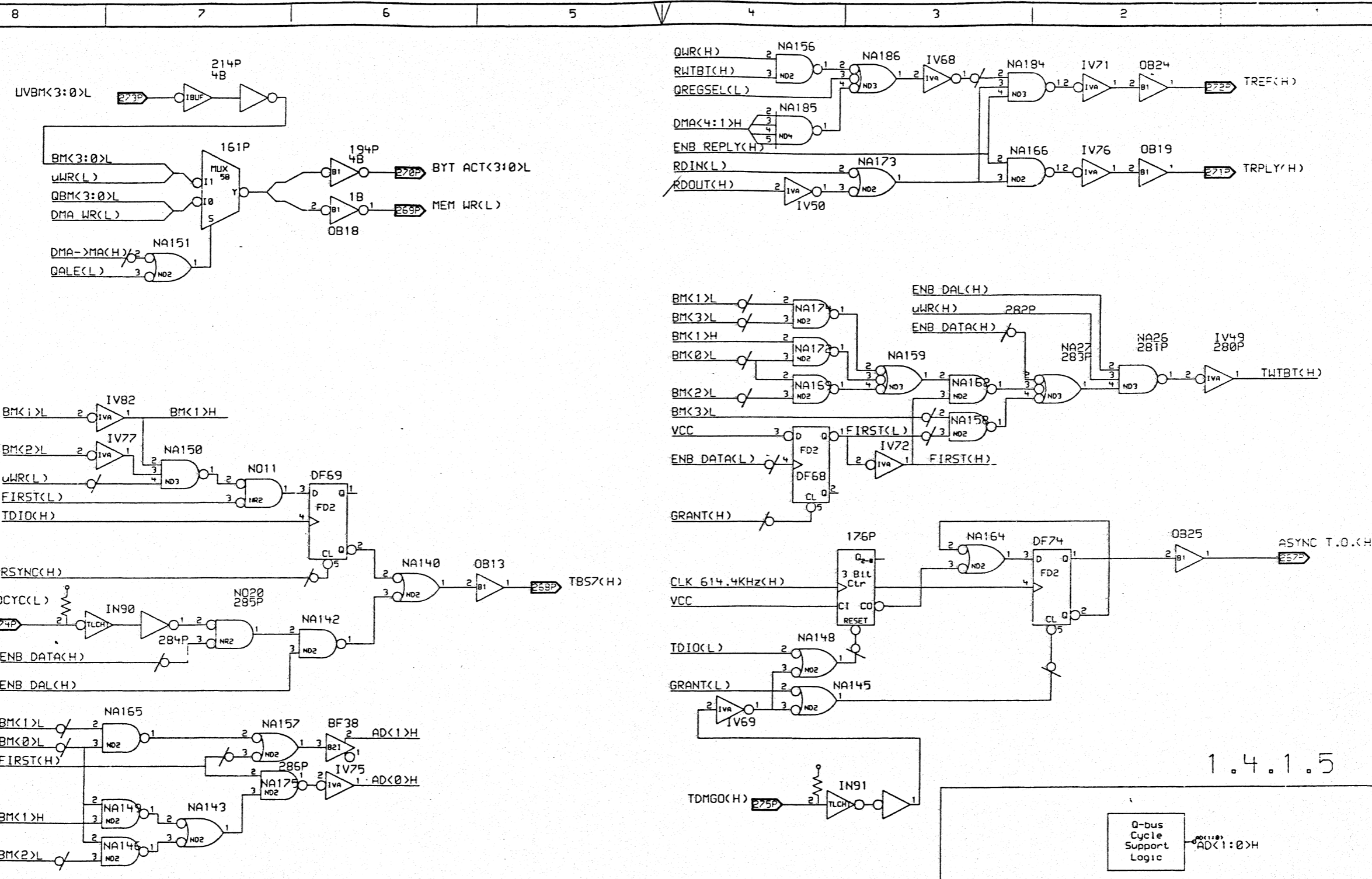
DRAWING
LAST MODIFIED=Wed Oct 10 19:36:34 1984



DRN: R. McNamara
CHK'D: R. McNamara

DATE: 1-NOV-83
DATE: 1-NOV-83

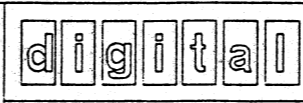
ENG: R. McNamara
SHEET 1 OF 1
TITLE: G-BUS Support Logic
STEE CODE: 1D 103
NUMBER: 7525-3-20



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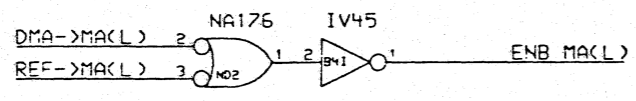
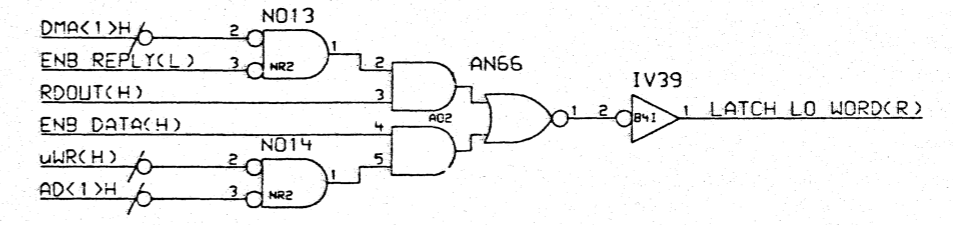
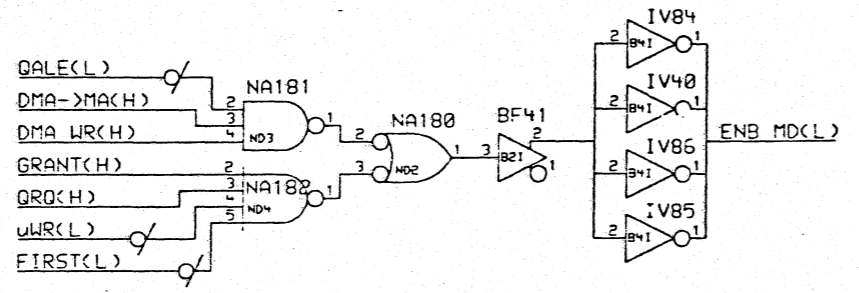
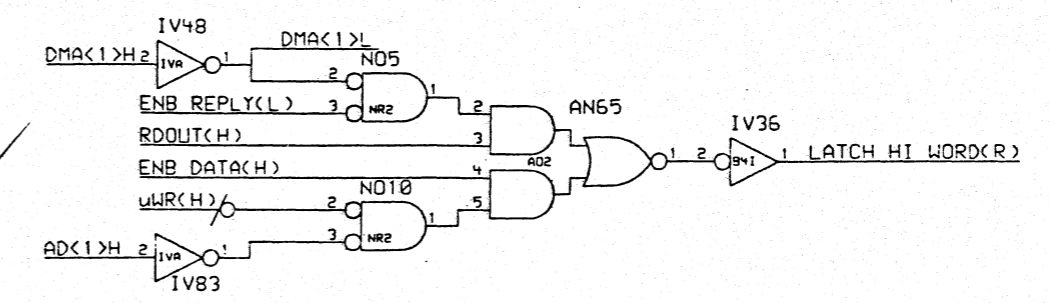
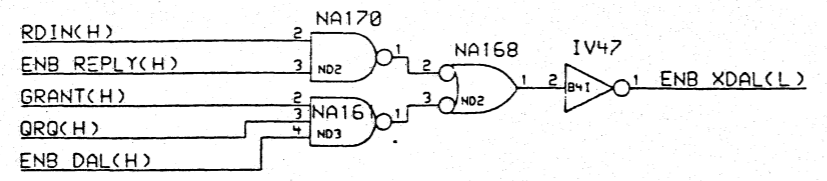
REV	TECH NUMBER	DATE	DESCRIPTION
1	175	10/21/83	INITIAL DESIGN
2	175	10/21/83	REVISED

DRAWING
 LAST MODIFIED=Wed Oct 10 19:53:46 1984

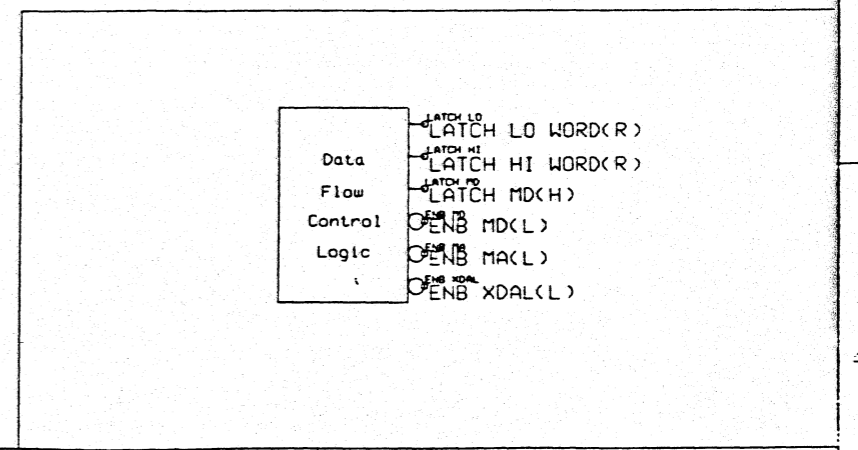


DRN: R. McNamara	DATE 21-OCT-83	ENG: R. McNamara	DATE 21-OCT-83	TITLE: Q-bus Support Logic
CHK'D: R. McNamara	DATE 21-OCT-83	SHEET 1 OF 1	NEXT HIGHER ASSEMBLY:	SIZE CODE D CS

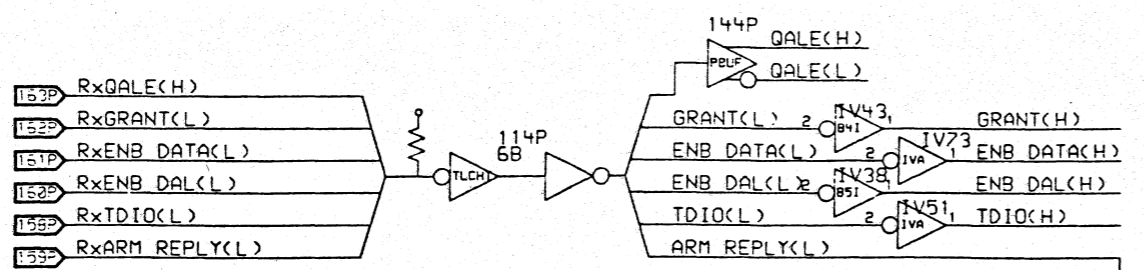
NUMBER
47525 -2 -21



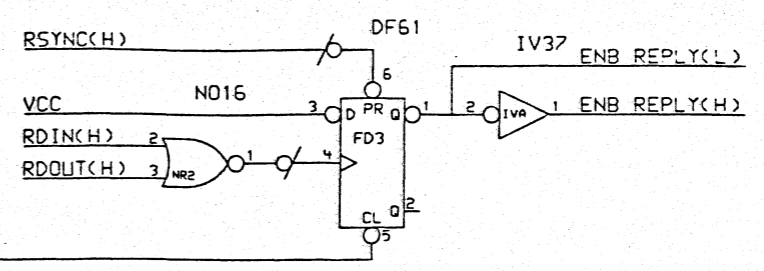
1.4.1.6



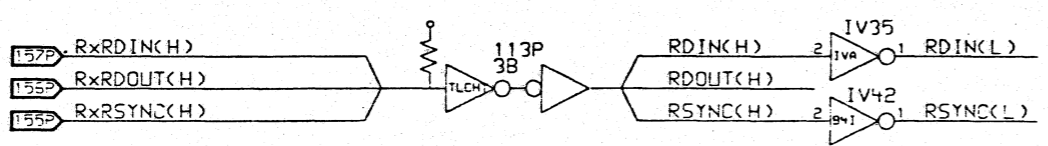
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				CHK'D: R. McNamara	DATE 09-NOV-83	SHEET 1 OF	NEXT HIGHER ASSEMBLY:	SIZE CODE D LOS	NUMBER M7505-10-22



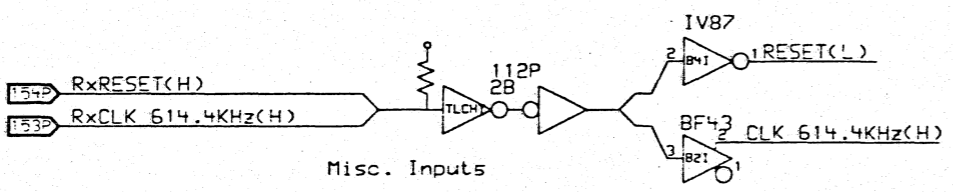
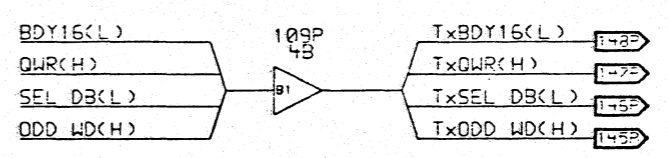
Inputs from Q-bus State Machines



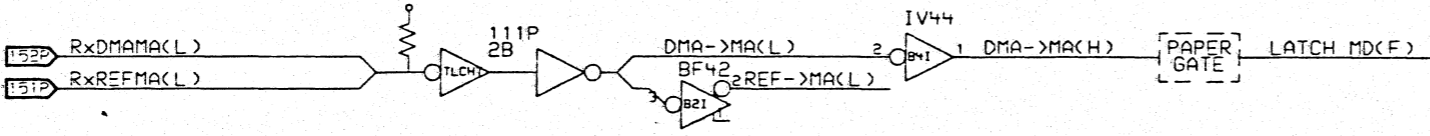
Outputs to Q-bus State Machines



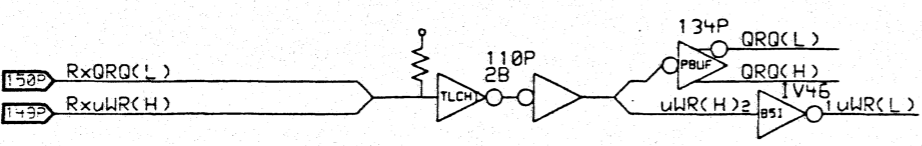
Q-bus Control Signal Inputs



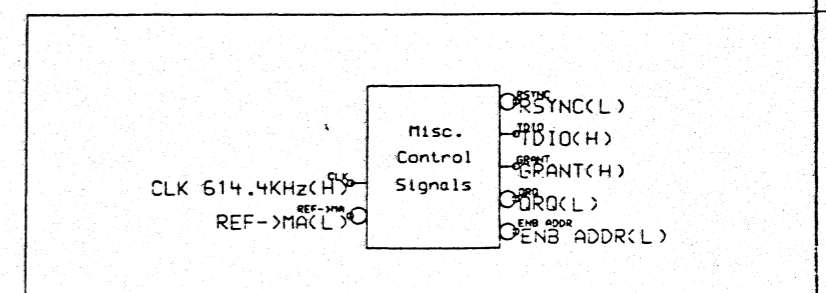
Misc. Inputs



Inputs from Main Memory Controller



Inputs from uVAX cycle machine



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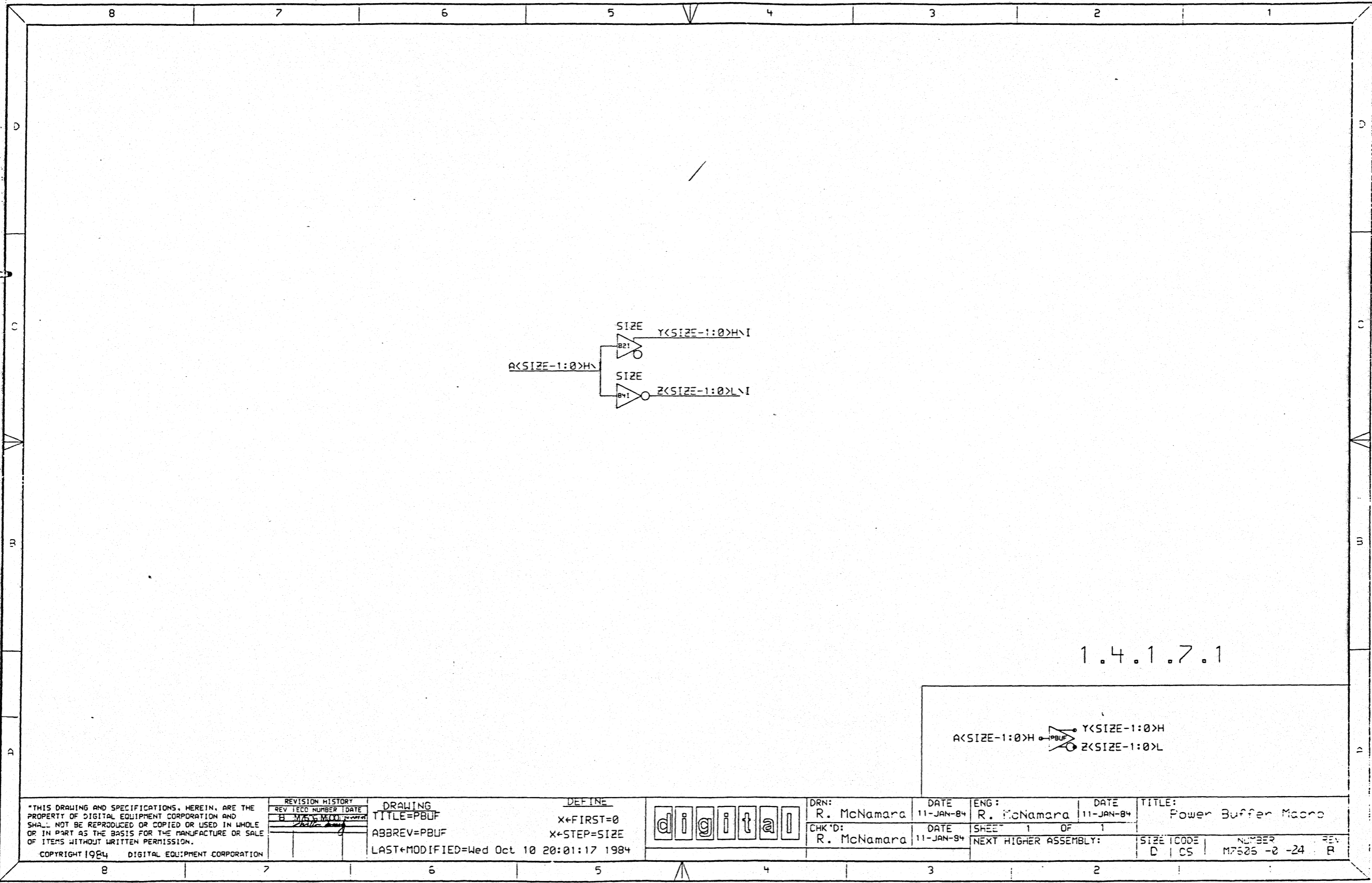
REVISION HISTORY	
REV	TECO NUMBER / DATE
1	M7525-2-23
2	11-NOV-83

DRAWING
 LAST MODIFIED=Wed Oct 10 19:49:41 1984

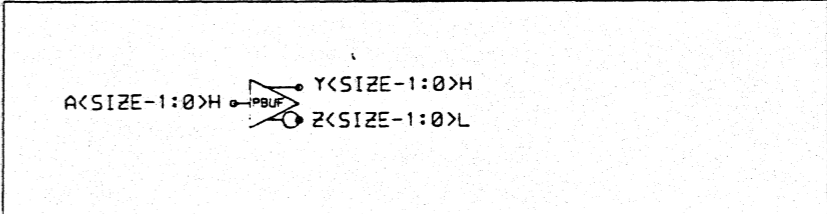
digital

DRN: R. McNamara	DATE 11-NOV-83	ENG: R. McNamara	DATE 11-NOV-83	TITLE: Q-bus Support Logic
CHK'D: R. McNamara	DATE 11-NOV-83	SHEET 1 OF 1	NEXT HIGHER ASSEMBLY:	SIZE / CODE D 05

NUMBER M7525-2-23	REV B
----------------------	----------



1.4.1.7.1



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REVISION HISTORY		
REV	ECO NUMBER	DATE
1	M7625	11-JAN-84

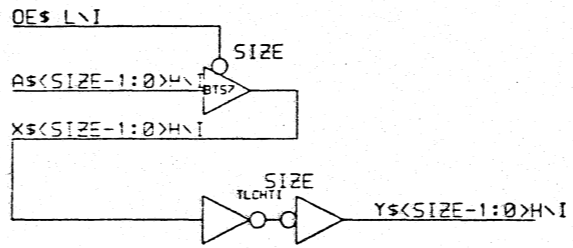
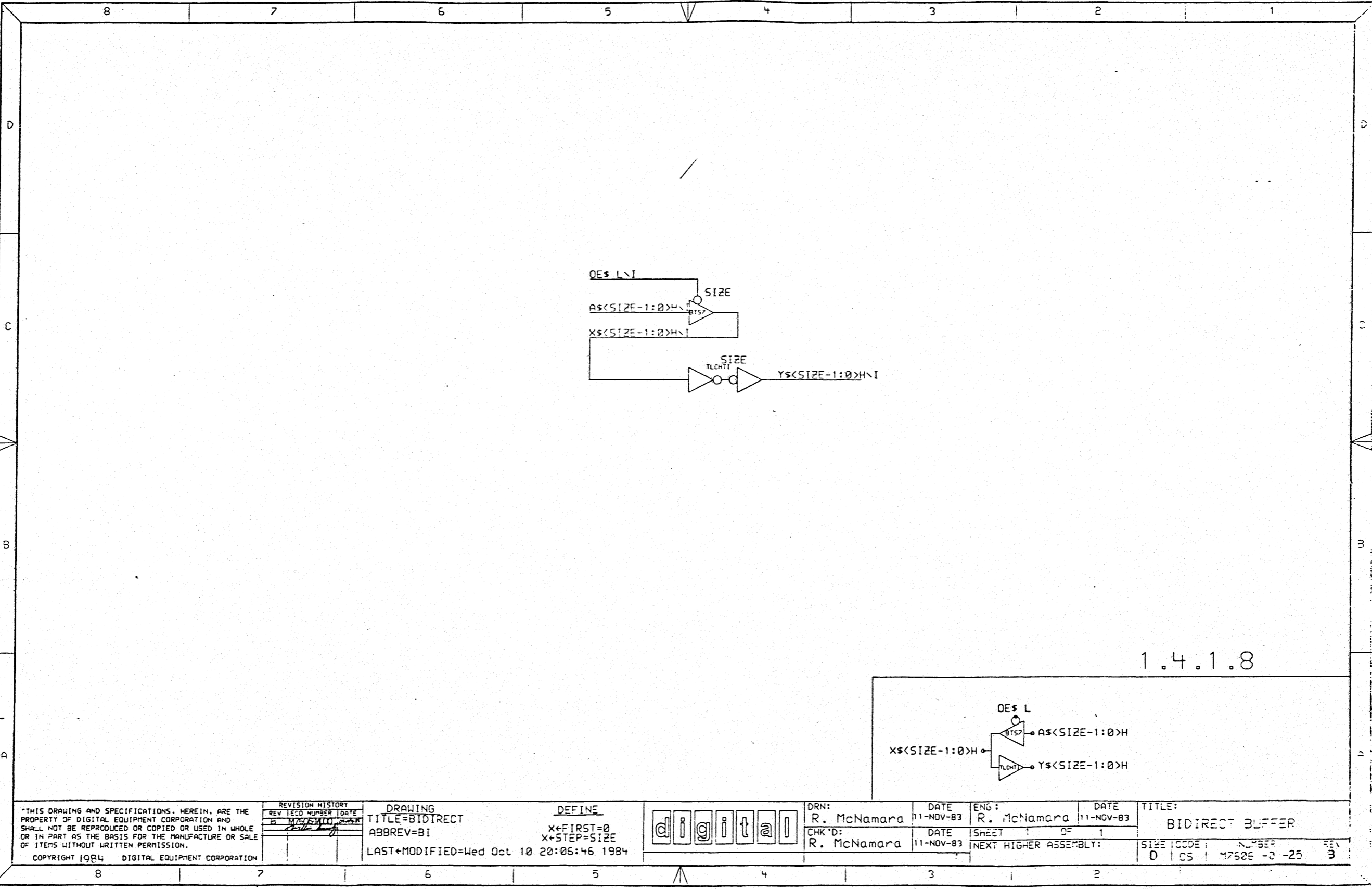
DRAWING TITLE=PBUF
 ABBREV=PBUF
 LAST MODIFIED=Wed Oct 10 20:01:17 1984

DEFINE
 X+FIRST=0
 X+STEP=SIZE
 digital

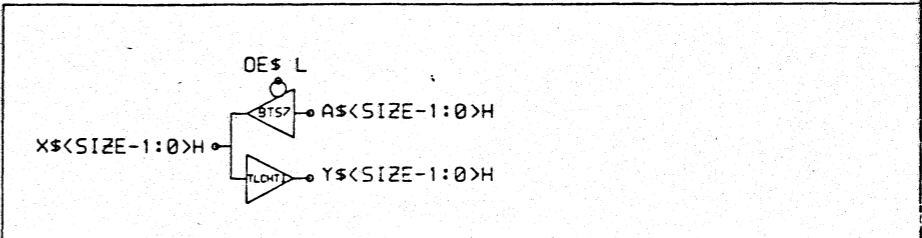
DRN: R. McNamara
 CHK'D: R. McNamara

DATE 11-JAN-84
 DATE 11-JAN-84
 SHEET 1 OF 1
 NEXT HIGHER ASSEMBLY:

ENG: R. McNamara
 DATE 11-JAN-84
 TITLE: Power Buffer Macro
 SIZE CODE D CS
 NUMBER M7625 -0 -24
 REV B



1.4.1.8



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REVISION HISTORY		
REV	TECD NUMBER	DATE
5	M75206	11-NOV-83

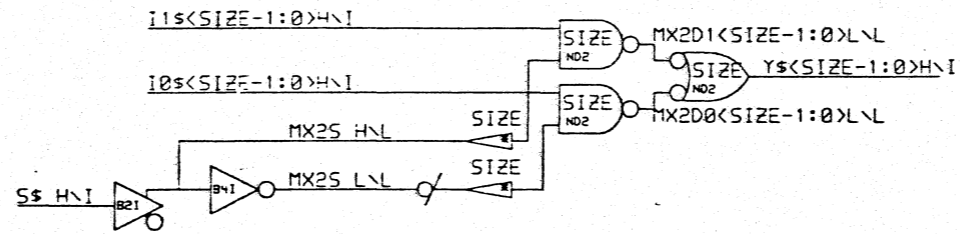
DRAWING
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ABBREV=BI
LAST*MODIFIED=Wed Oct 10 20:05:46 1984

DEFINE
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X*STEP=SIZE

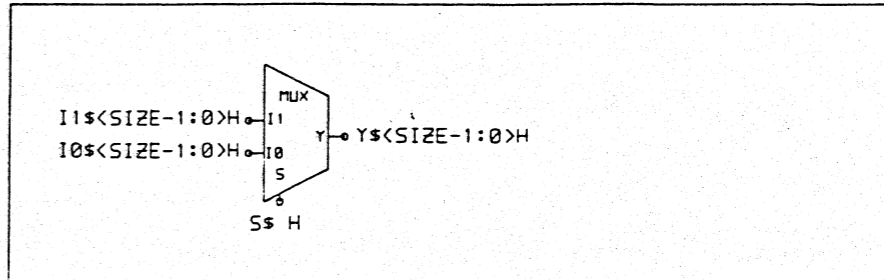
digital

DRN: R. McNamara	DATE 11-NOV-83	ENG: R. McNamara	DATE 11-NOV-83
CHK'D: R. McNamara	DATE 11-NOV-83	SHEET 1 OF 1	
NEXT HIGHER ASSEMBLY:			

TITLE: BIDIRECT BUFFER			
SIZE D	CODE CS	NUMBER M75206-0-25	REV 3



1.4.1.9



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REVISION HISTORY		
REV	ISSUED NUMBER	DATE
B	M.C.M.	10/10/84

DRAWING
TITLE=MUX16
ABBREV=MX16
LAST MODIFIED=Wed Oct 10 20:09:42 1984

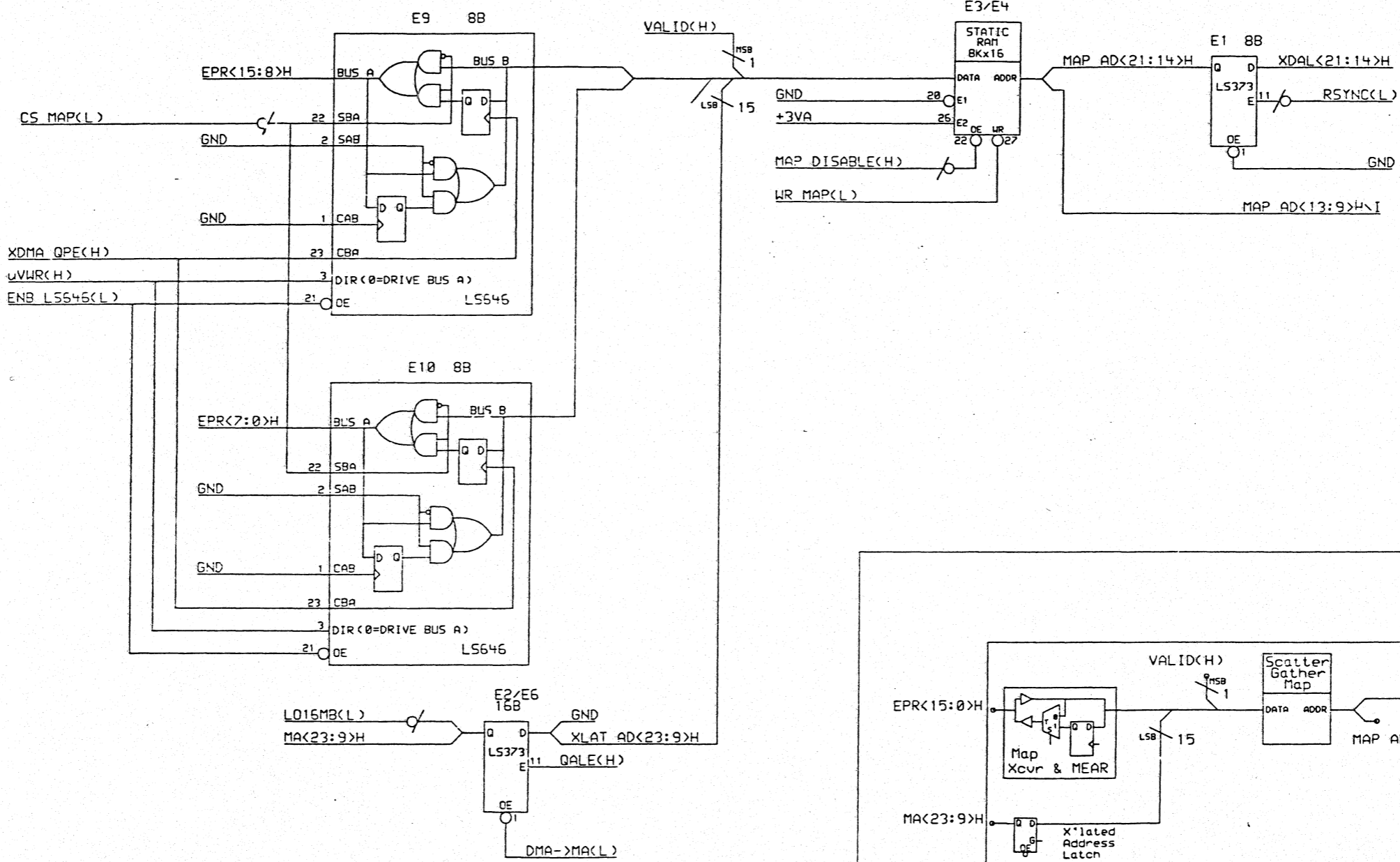
DEFINE
X*FIRST=0
X*STEP=SIZE
digital

DRN:
R. McNamara
CHK'D:
R. McNamara

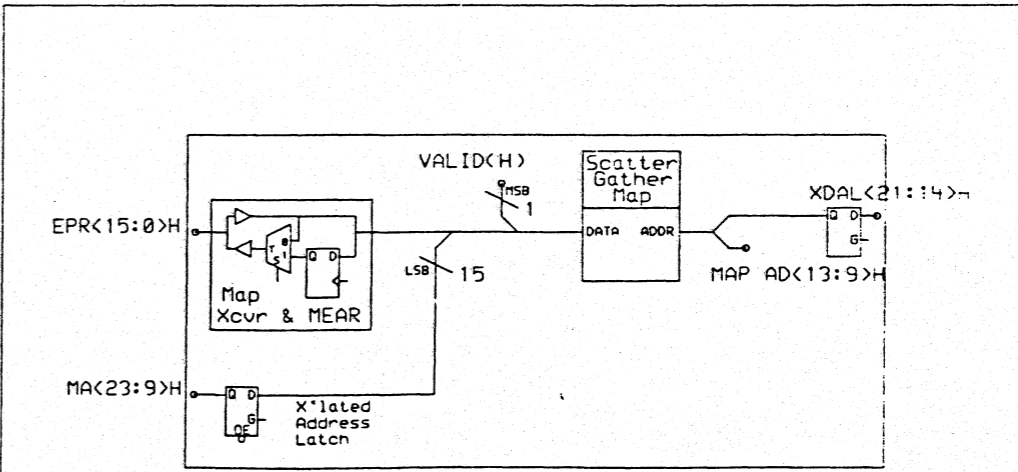
DATE
8-NOV-83
DATE
8-NOV-83
SHEET 1 OF 1
NEXT HIGHER ASSEMBLY:

ENG:
R. McNamara
DATE
8-NOV-83
TITLE:
MUX LOGIC
SIZE CODE
D 05
NUMBER
M7505 -2 -26
REV
E

8 7 6 5 4 3 2 1



1.5



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REV	ECN	NUMBER	DATE
3			

DRAWING
TITLE=MAP GROUP
ABBREV=MAP
CIRCUIT+TYPE=TRANS+MAP
LAST+MODIFIED=Sun Oct 7 18:33:49 1984

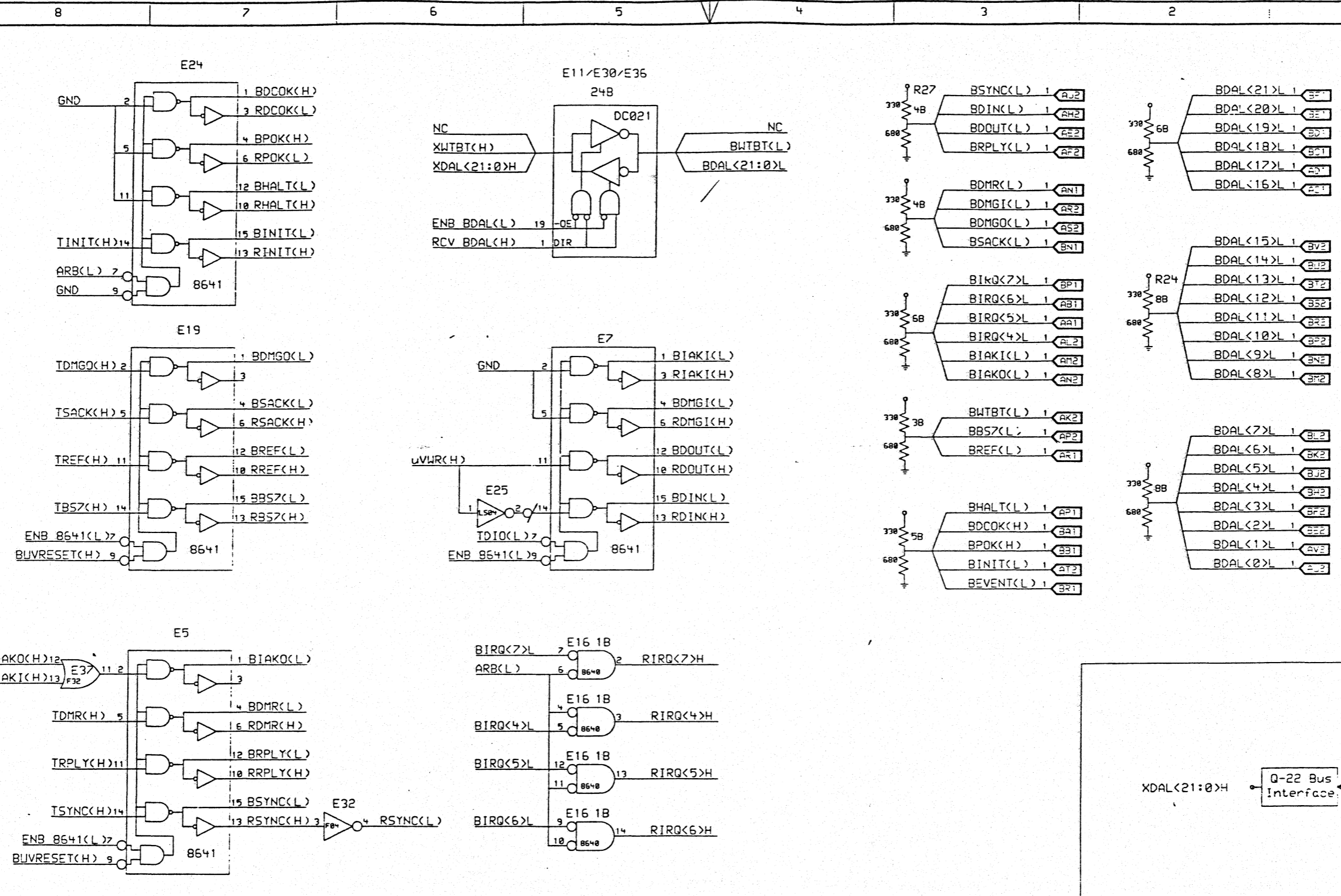
DEFINE
X*FIRST=0
X*STEP=SIZE

digital

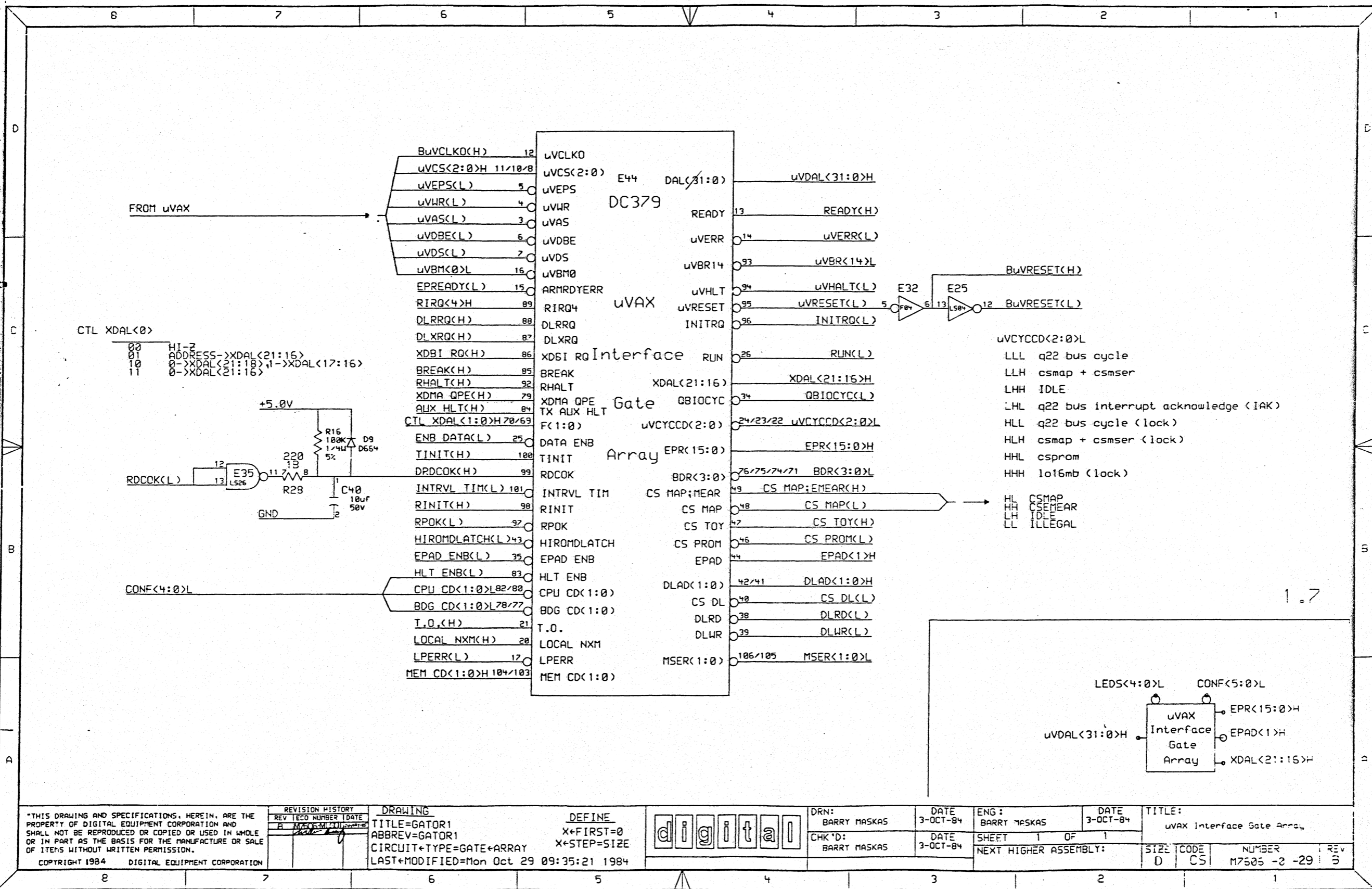
DRN: R. McNamara	DATE 3-OCT-84	ENG: R. McNamara	DATE 3-OCT-84	TITLE: Translation Map Group
CHK'D: R. McNamara	DATE 3-OCT-84	SHEET 1 OF 1	NEXT HIGHER ASSEMBLY:	

SIZ	CODE	NUMBER	REV
D	CS	M7605-2-27	3

8 7 6 5 4 3 2 1



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	CHECK'D: R. McNamara DATE 3-OCT-84	SHEET 1 OF 1 NEXT HIGHER ASSEMBLY:	SIZE CODE NUMBER REV D CS M7626 -0 -25 5				

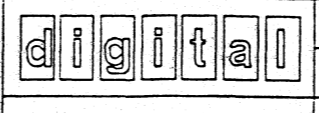


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REVISION HISTORY		
REV	TECD NUMBER	DATE
1	M7505-2	3-10-84

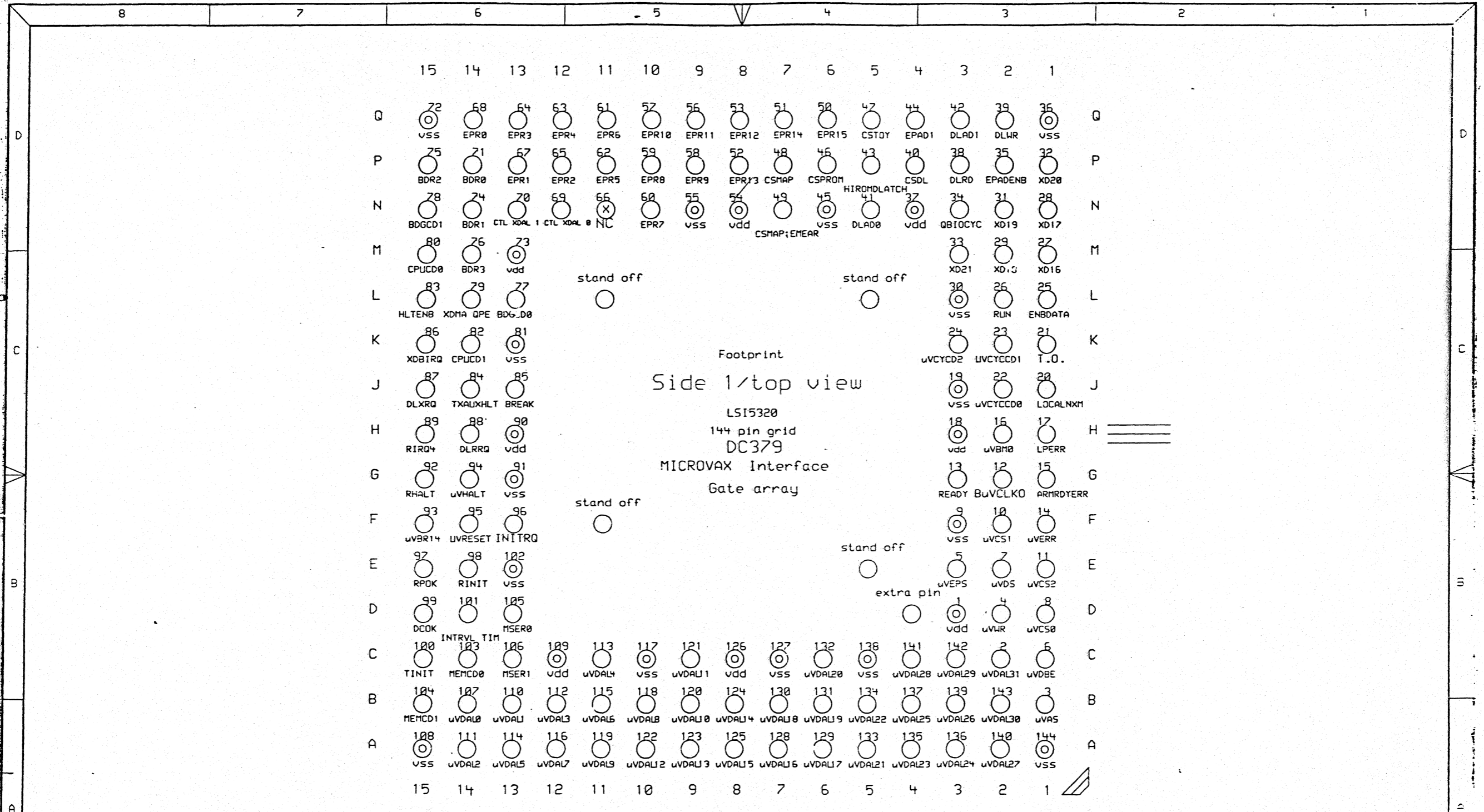
DRAWING
 TITLE=GATOR1
 ABBREV=GATOR1
 CIRCUIT+TYPE=GATE+ARRAY
 LAST+MODIFIED=Mon Oct 29 09:35:21 1984

DEFINE
 X+FIRST=0
 X+STEP=SIZE



DRN: BARRY MASKAS
 DATE: 3-OCT-84
 ENG: BARRY MASKAS
 DATE: 3-OCT-84
 SHEET: 1 OF 1
 NEXT HIGHER ASSEMBLY:

TITLE: uVAX interface Gate Array
 SIZE: D
 CODE: CS
 NUMBER: M7505-2-29
 REV: 3

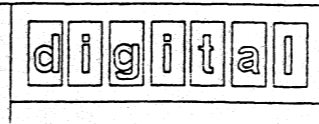


Footprint
 Side 1/top view
 LSI5320
 144 pin grid
 DC379
 MICROVAX Interface
 Gate array

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REVISION HISTORY		
REV	TECD NUMBER	DATE
1	11/23/83	11/23/83

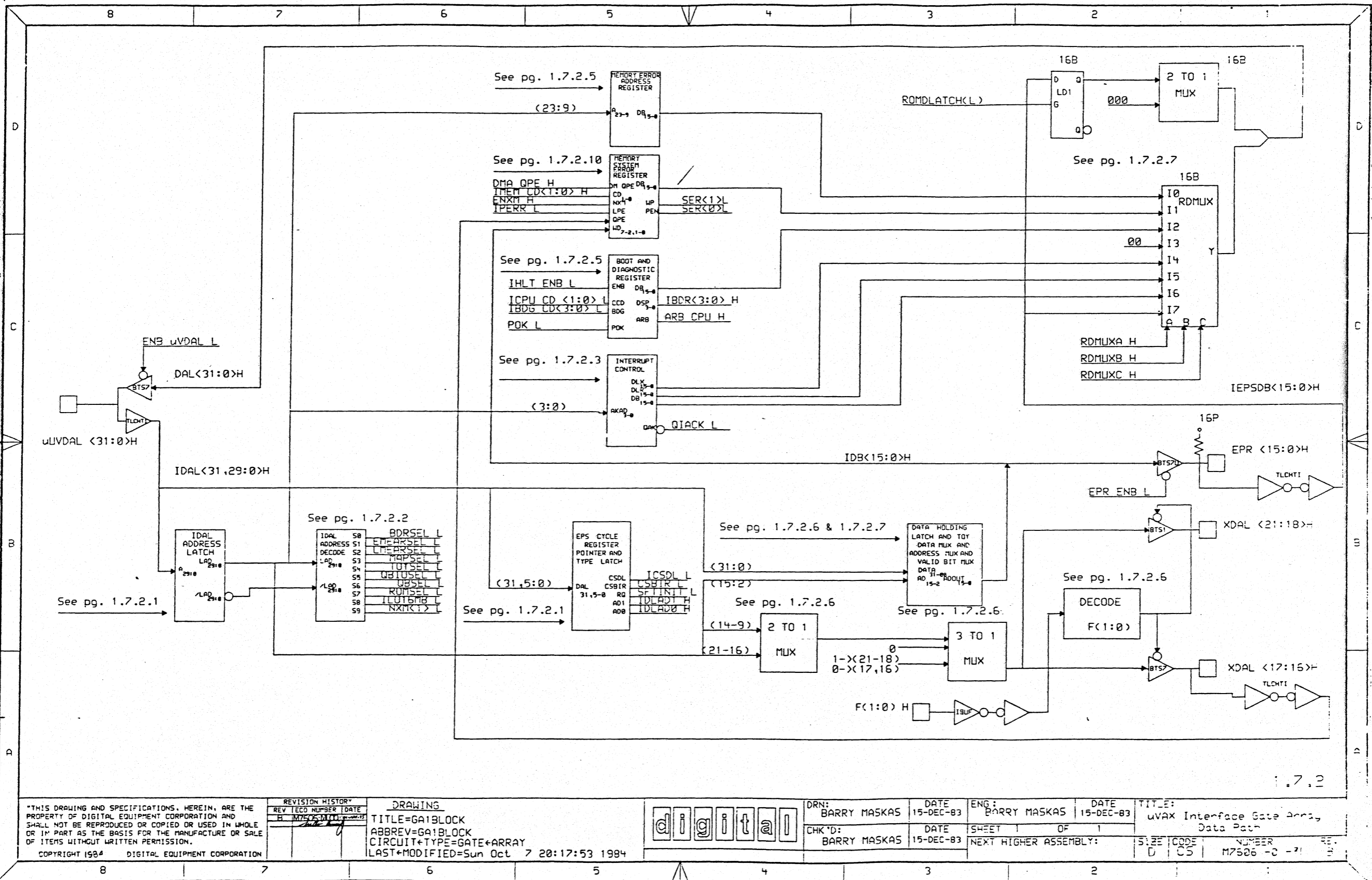
DRAWING
 TITLE=galpads
 DEFINE
 X*FIRST=0
 X*STEP=SIZE
 11:47:47 1984
 LAST*MODIFIED=Mon Oct 29



DRN:
 BARRY MASKAS
 DATE
 CHK'D:
 BARRY MASKAS
 DATE

ENG:
 BARRY MASKAS
 DATE
 SHEET 1 OF 1
 NEXT HIGHER ASSEMBLY:

TITLE:
 DC379 PAD ASSIGNMENT TOP VIEW
 LL5320 IN 144 PIN GRID ARRAY
 SIZE CODE NUMBER
 D CS M7606 -0 -30 B



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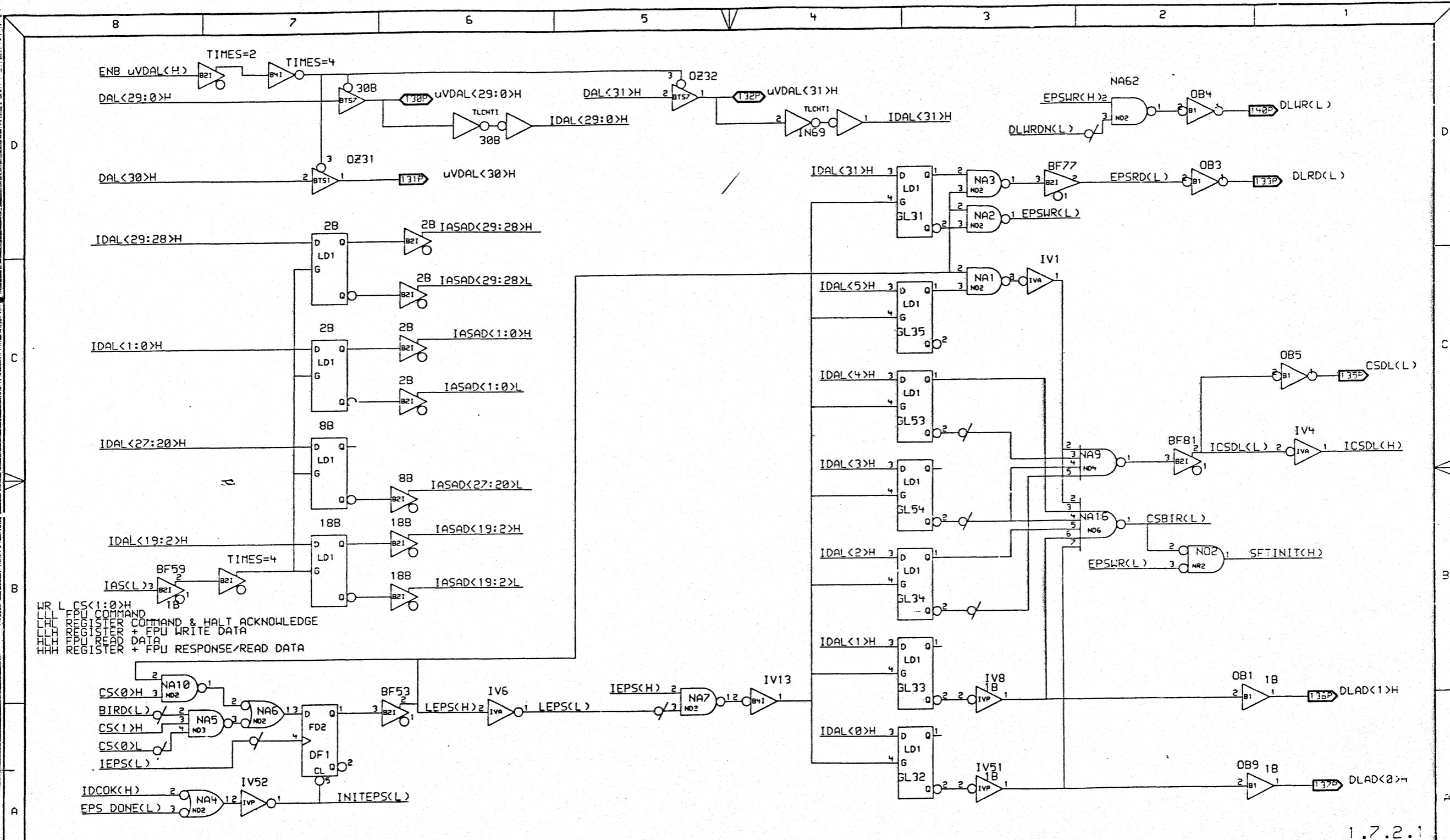
REVISION HISTORY	
REV	TECO NUMBER / DATE
1	15-DEC-83

DRAWING
 TITLE=GA1BLOCK
 ABBREV=GA1BLOCK
 CIRCUIT+TYPE=GATE+ARRAY
 LAST+MODIFIED=Sun Oct 7 20:17:53 1984



DRN: BARRY MASKAS
 DATE: 15-DEC-83
 ENG: BARRY MASKAS
 DATE: 15-DEC-83
 SHEET 1 OF 1
 NEXT HIGHER ASSEMBLY:

TITLE: uVAX Interface Gate Array Data Path
 SIZE: D
 CODE: C5
 NUMBER: M7506-2-71



WR L CS<1:0>H
 LLL FPU COMMAND
 LLH REGISTER COMMAND & HALT ACKNOWLEDGE
 LLH REGISTER + FPU WRITE DATA
 HLH FPU READ DATA
 HHH REGISTER + FPU RESPONSE/READ DATA

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REVISION HISTORY		
REV	TECO NUMBER	DATE
1	NA5	10/27/84

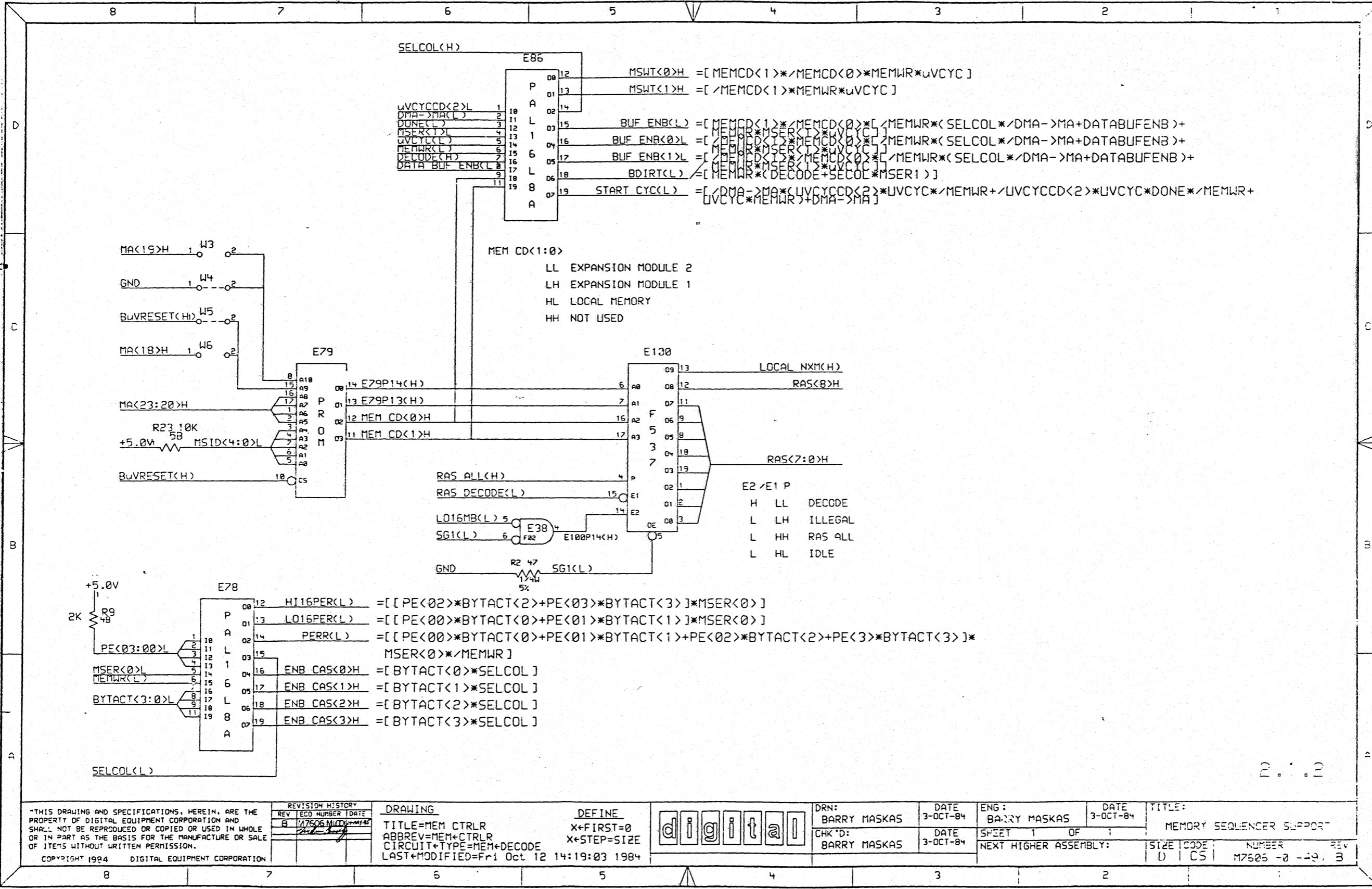
DRAWING
 TITLE=GA1
 ABBREV=GA1
 CIRCUIT+TYPE=GATE+ARRAY
 LAST+MODIFIED=Sun Oct 7 20:20:28 1984

DEFINE
 X+FIRST=0
 X+STEP=SIZE



DRN:	DATE	ENG:	DATE	TITLE:
BARRY MASKAS	19-DEC-83	BARRY MASKAS	19-DEC-83	UVDAL I/O BUFFERS, ADDR LATCHES
CHK'D:	DATE		SHEET 1 OF 1	
BARRY MASKAS	19-DEC-83		NEXT HIGHER ASSEMBLY:	

SIZE	CODE	NUMBER	REV
D	CS	M7526 -0 -02	H



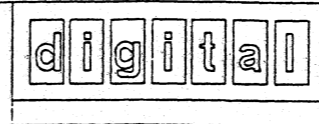
2.1.2

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REVISION HISTORY		
REV	ECO NUMBER	DATE
6	117506 MLD	11/11/84

DRAWING
TITLE=MEM CTRLR
ABBREV=MEM+CTRLR
CIRCUIT+TYPE=MEM+DECODE
LAST+MODIFIED=Fri Oct 12 14:19:03 1984

DEFINE
X+FIRST=0
X+STEP=SIZE

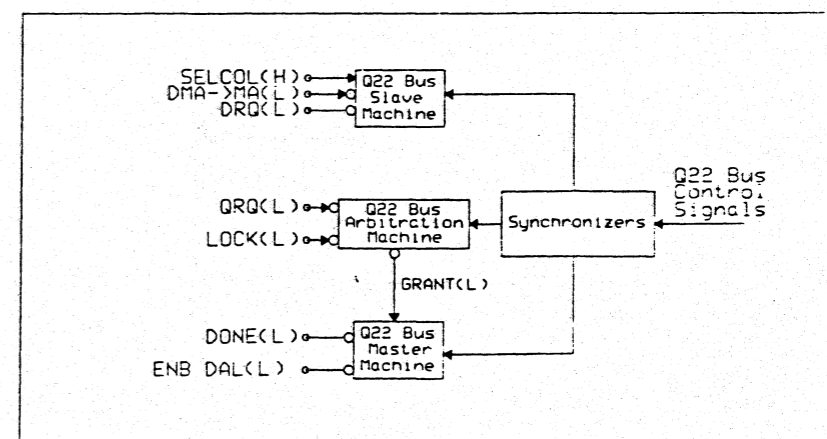
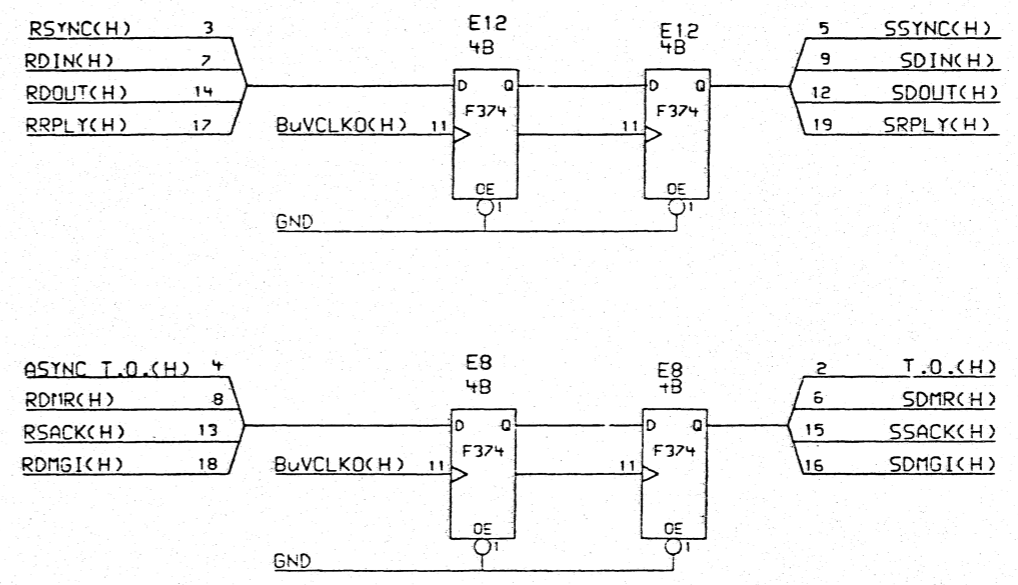
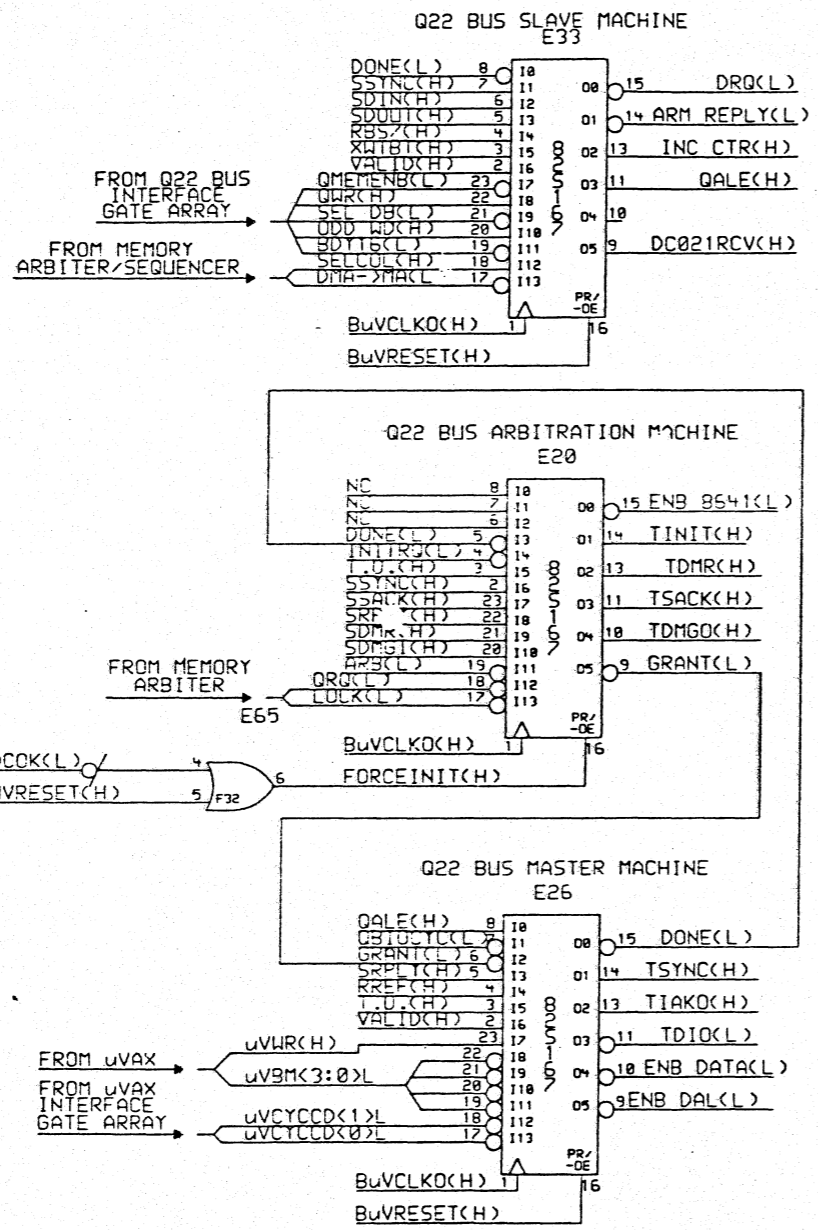


DRN: BARRY MASKAS
CHK'D: BARRY MASKAS

DATE: 3-OCT-84
DATE: 3-OCT-84

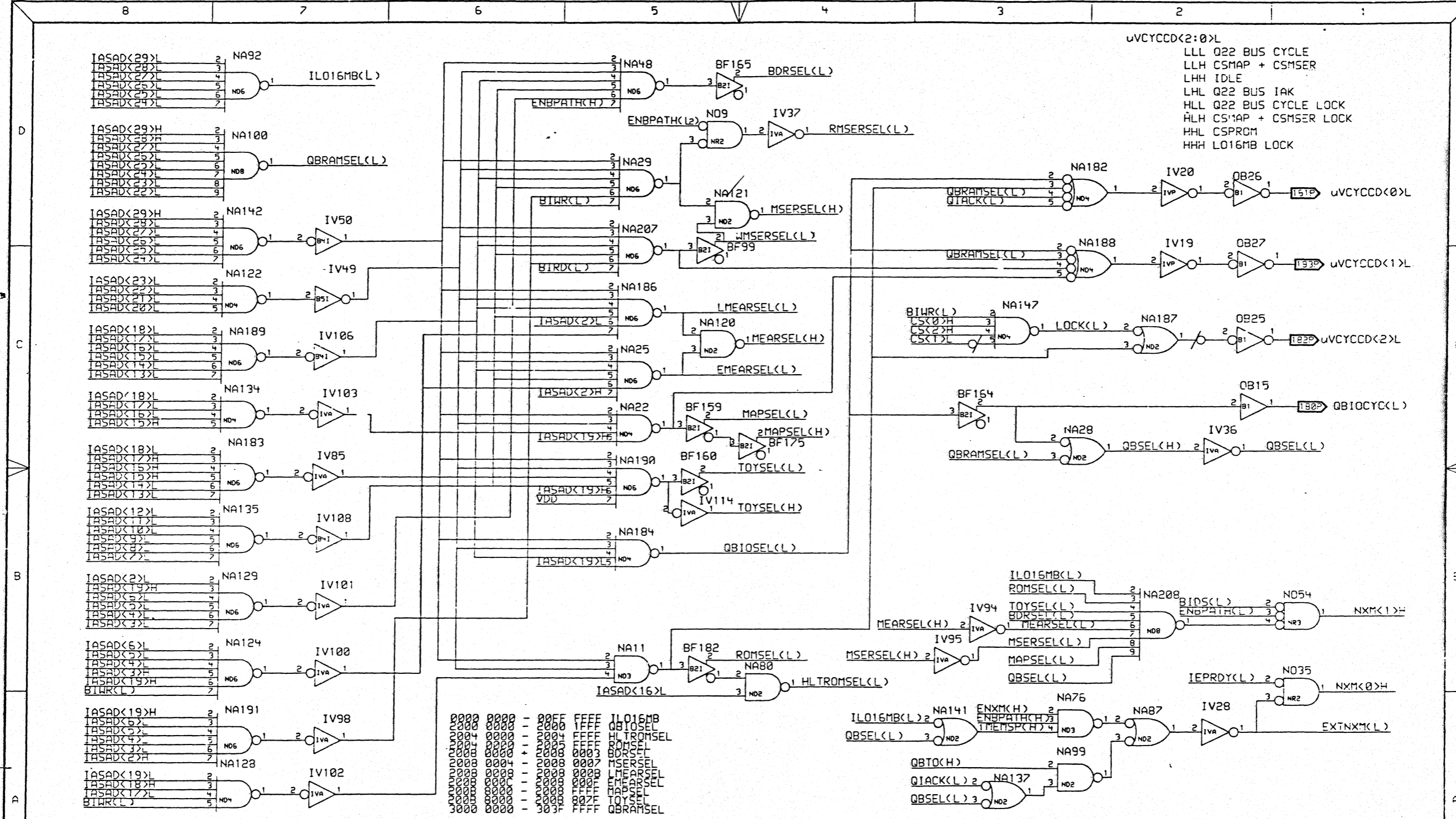
ENG: BARRY MASKAS
SHEET 1 OF 1
NEXT HIGHER ASSEMBLY:
TITLE: MEMORY SEQUENCER SUPPORT

SIZE	CODE	NUMBER	REV
D	CS	M7505-0	-19, 3



2.2

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---	--	--	--	--	----------------	--	--------------------------------	----------------------------------	--	-------------------------------	---



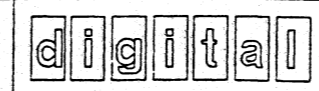
uVCYCCD<2:0>L
 LLL Q22 BUS CYCLE
 LLH CSMAP + CSMER
 LHH IDLE
 LHL Q22 BUS IAK
 HLL Q22 BUS CYCLE LOCK
 HLH CSMAP + CSMER LOCK
 HHL CSPROM
 HHH LO16MB LOCK

1.7.2.2

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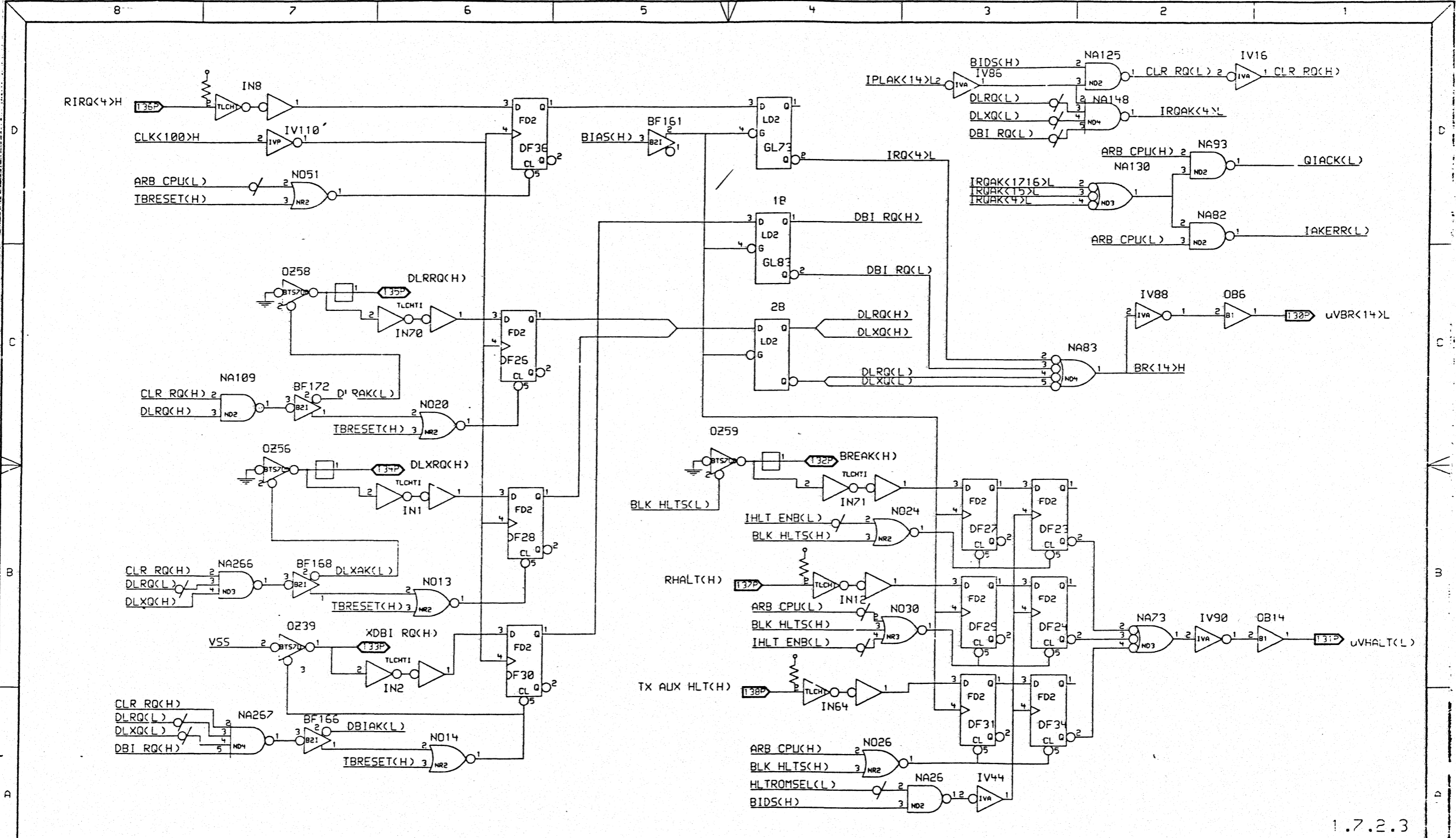
REVISION HISTORY		
REV	NO	DATE
1	1	19-DEC-83

DRAWING
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 ABBREV=GA1
 CIRCUIT+TYPE=GATE+ARRAY
 LAST+MODIFIED=Sun Oct 7 16:34:28 1984



DRN:	BARRY MASKAS	DATE:	19-DEC-83	ENG:	BARRY MASKAS	DATE:	19-DEC-83	TITLE:	ADDRESS DECODER
CHK'D:	BARRY MASKAS	DATE:	19-DEC-83	SHEET:	1	OF:	1	NEXT HIGHER ASSEMBLY:	

SIZE:	CODE:	NUMBER:	REV:
D	CS	M7605-00-33	1

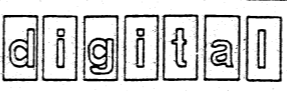


1.7.2.3

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REVISION HISTORY		
REV	ECO NUMBER	DATE
1		10-27-83

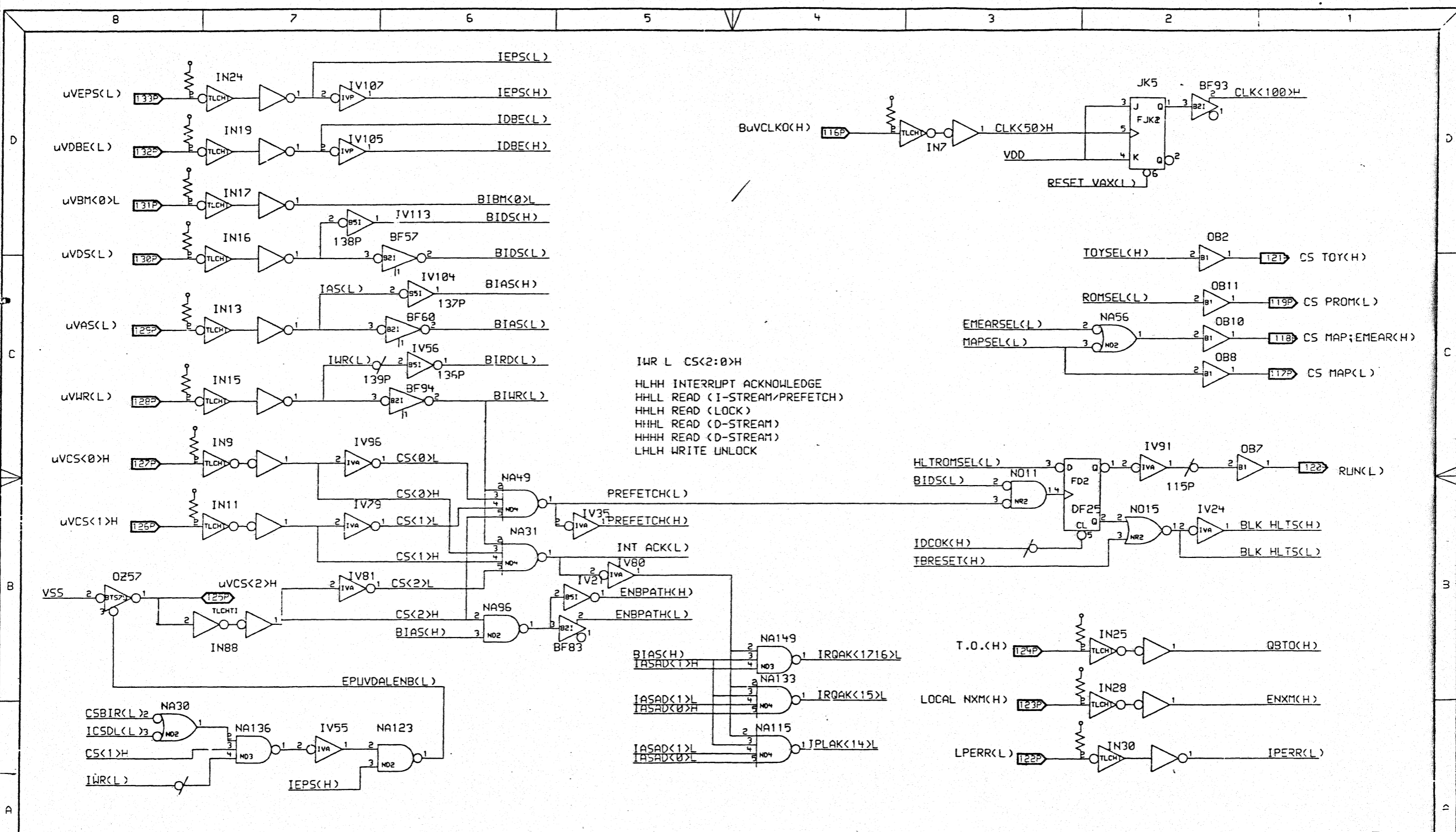
DRAWING
 TITLE=GA1
 ABBREV=GA1
 CIRCUIT+TYPE=GATE+ARRAY
 LAST+MODIFIED=Sun Oct 7 16:40:03 1984



DRN: BARRY MASKAS
 CHK'D: BARRY MASKAS

DATE	ENG	DATE	TITLE
18-DEC-83	BARRY MASKAS	18-DEC-83	EXCEPTIONS AND INTERRUPTS
DATE	SHEET	OF	
18-DEC-83	1	1	
NEXT HIGHER ASSEMBLY:			

SIZE	CODE	NUMBER	REV
D	CS	M7506 -0 -34	1



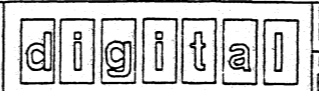
IWR L CS<2>0>H
 HLHH INTERRUPT ACKNOWLEDGE
 HLLL READ (I-STREAM/PREFETCH)
 HHLH READ (LOCK)
 HHHH READ (D-STREAM)
 LHLH WRITE UNLOCK

1.7.2.4

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REV	ECO NUMBER	DATE
1		11/20/83
2		10/20/84

DRAWING
 TITLE=GA1
 ABBREV=GA1
 CIRCUIT+TYPE=GATE+ARRAY
 LAST+MODIFIED=Sat Oct 20 18:44:09 1984

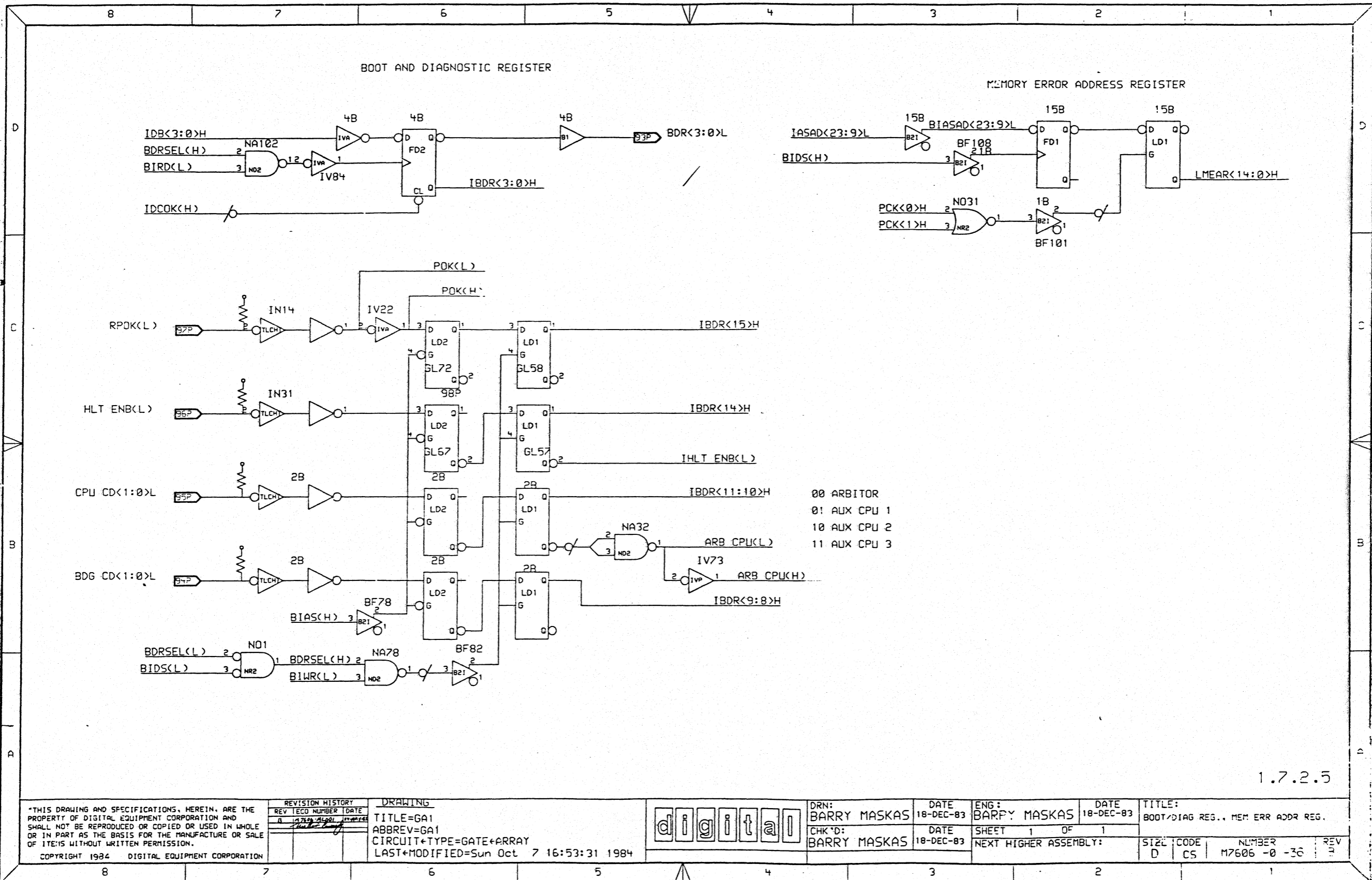


DRN: BARRY MASKAS
 CHK'D: BARRY MASKAS

DATE 19-DEC-83
 DATE 19-DEC-83

ENG: BARRY MASKAS
 SHEET 1 OF 1
 TITLE: UVAX INPUTS AND I/O PINS

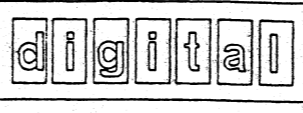
SIZE	CODE	NUMBER	REV
D	CS	M7605 -0 -35	3



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REVISION HISTORY		
REV	IECO NUMBER	DATE
1	14789-AL01	11/14/84
2		

DRAWING
 TITLE=GA1
 ABBREV=GA1
 CIRCUIT+TYPE=GATE+ARRAY
 LAST+MODIFIED=Sun Oct 7 16:53:31 1984



DRN:
 BARRY MASKAS
 CHK'D:
 BARRY MASKAS

DATE
 18-DEC-83

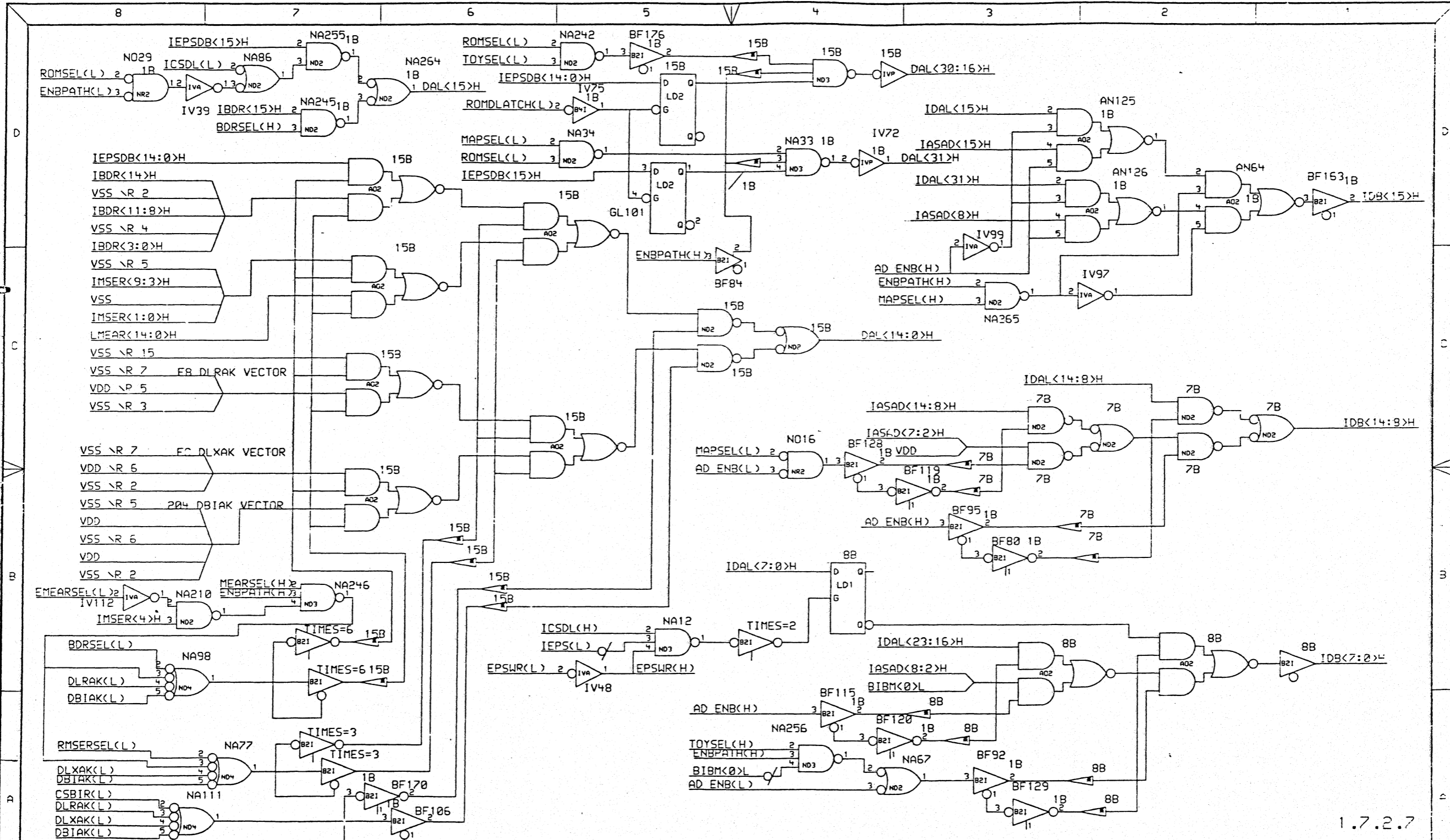
ENG:
 BARRY MASKAS

DATE
 18-DEC-83

TITLE:
 BOOT/DIAG RES., MEM ERR ADDR REG.

SHEET 1 OF 1
 NEXT HIGHER ASSEMBLY:

SIZE	CODE	NUMBER	REV
D	CS	M7606-0-36	3



1.7.2.7

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REV	TECO NUMBER	DATE
1	1760-00	10/7/84

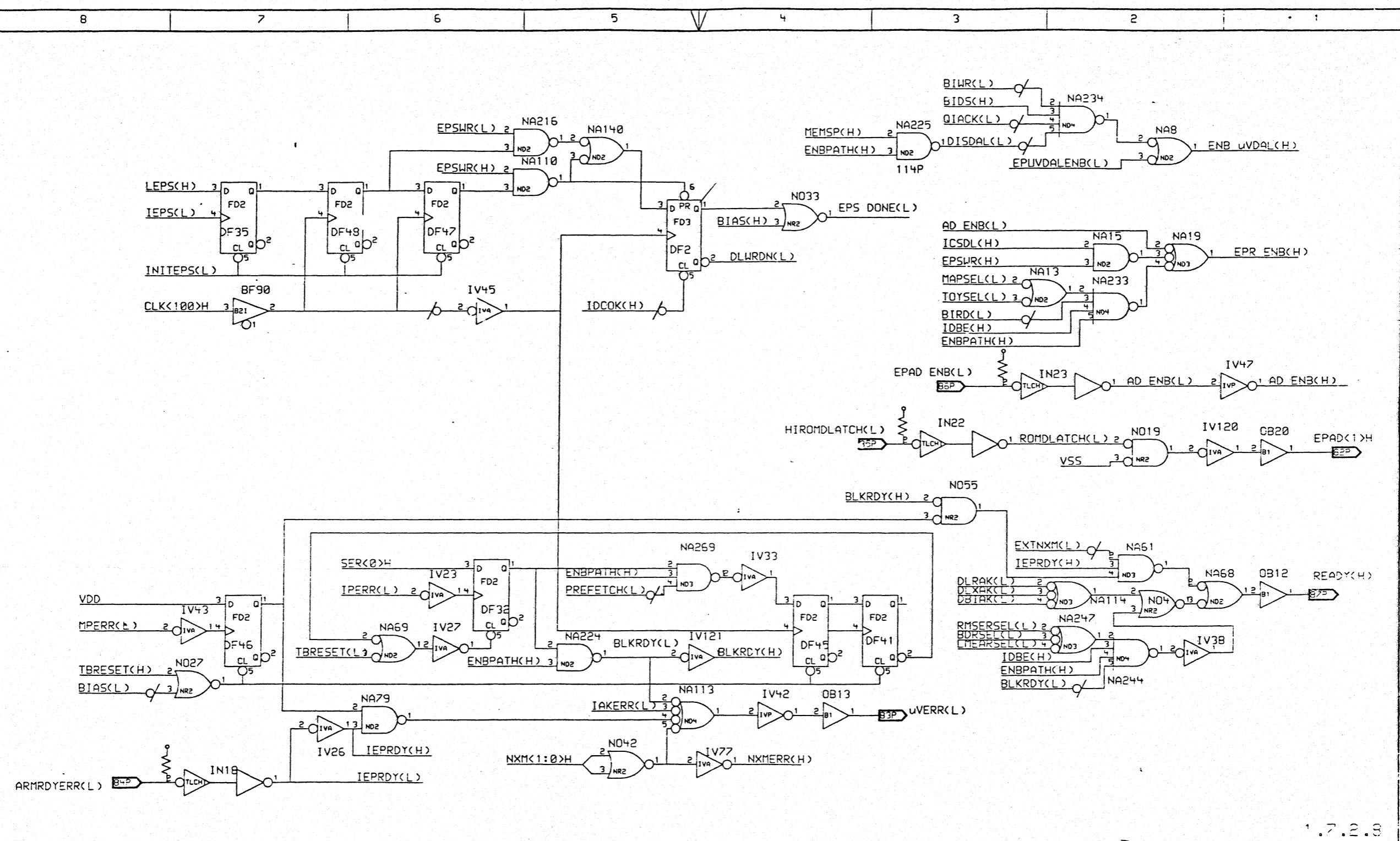
DRAWING
 TITLE=GA1
 ABBREV=GA1
 CIRCUIT+TYPE=GATE+ARRAY
 LAST+MODIFIED=Sun Oct 7 17:11:37 1984

digital

DRN: BARRY MASKAS
 DATE: 19-DEC-83
 CHK'D: BARRY MASKAS
 DATE: 19-DEC-83

ENG: BARR, MASKAS
 DATE: 19-DEC-83
 SHEET 1 OF 1
 NEXT HIGHER ASSEMBLY:

TITLE: INTERNAL DATA BUSES
 SIZE: D
 CODE: CS
 NUMBER: M7605-0-38
 REV: B



1.7.2.8

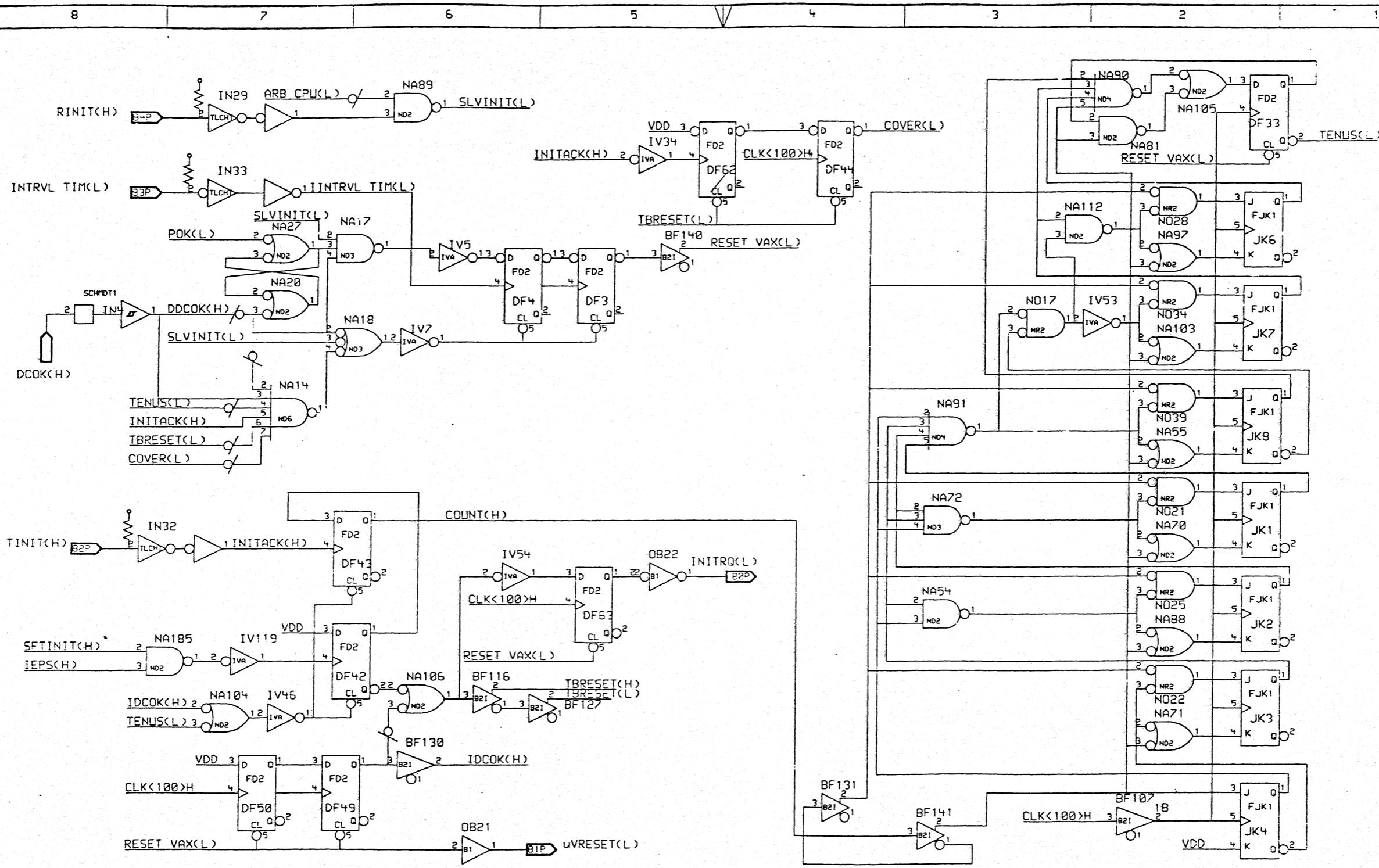
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REVISION HISTORY		DRAWING	
REV	TECO NUMBER	DATE	
0			
TITLE=GA1		ABBREV=GA1	
CIRCUIT+TYPE=GATE+ARRAY		LAST+MODIFIED=Sun Oct 7 17:15:18 1984	

digital

DRN:	BARRY MASKAS	DATE	19-DEC-83	ENG:	BARRY MASKAS	DATE	19-DEC-83	TITLE:	MISC. CONTROL STROBES
CHK'D:	BARRY MASKAS	DATE	19-DEC-83	SHEET	1	OF	1	SIZE	CODE
				NEXT HIGHER ASSEMBLY:					

NUMBER	M7525-2-89	REV	B
CODE	D	CS	



1.7.2.9

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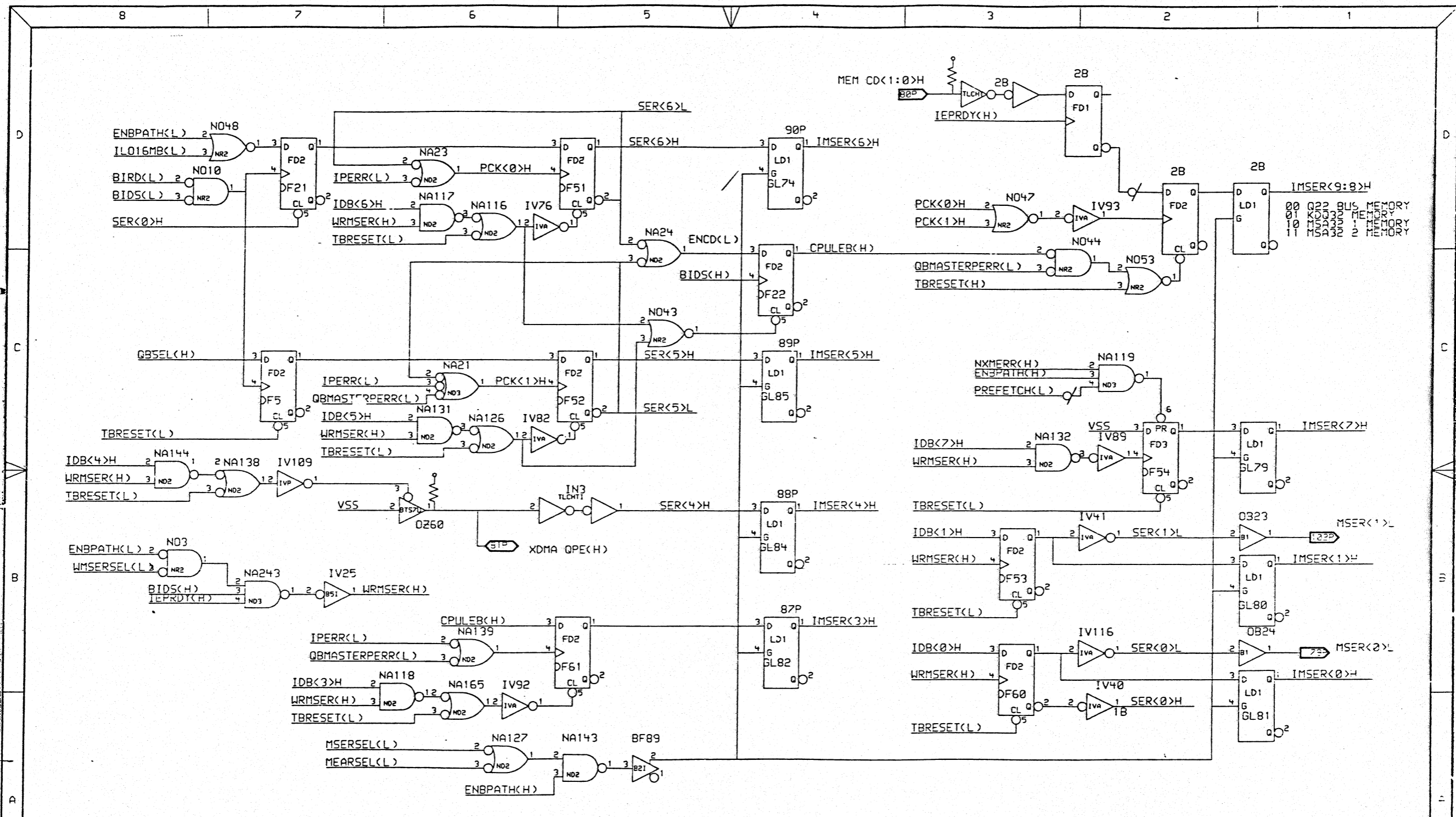
REVISION HISTORY		DRAWING	
REV	TECO NUMBER	DATE	
B	17-08-11-02	11-84	

TITLE=GA1
 ABBREV=GA1
 CIRCUIT+TYPE=GATE+ARRAY
 LAST+MODIFIED=Sun Oct 7 17:19:49 1984

digital

DRN:	BARRY MASKAS	DATE	19-DEC-83	ENG:	BARRY MASKAS	DATE	19-DEC-83	TITLE:	RESET COUNTER, POWER UP/DOWN CNTRL
CHK'D:	BARRY MASKAS	DATE	19-DEC-83	SHEET	1	OF	1	NEXT HIGHER ASSEMBLY:	

SIZE	CODE	NUMBER	REV
D	CS	M7605 -0 -10	2

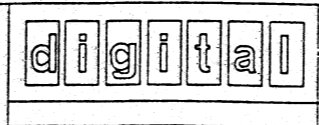


1.7.2.10

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REV	TECO NUMBER	DATE
0	14760-AL001	12/19/83

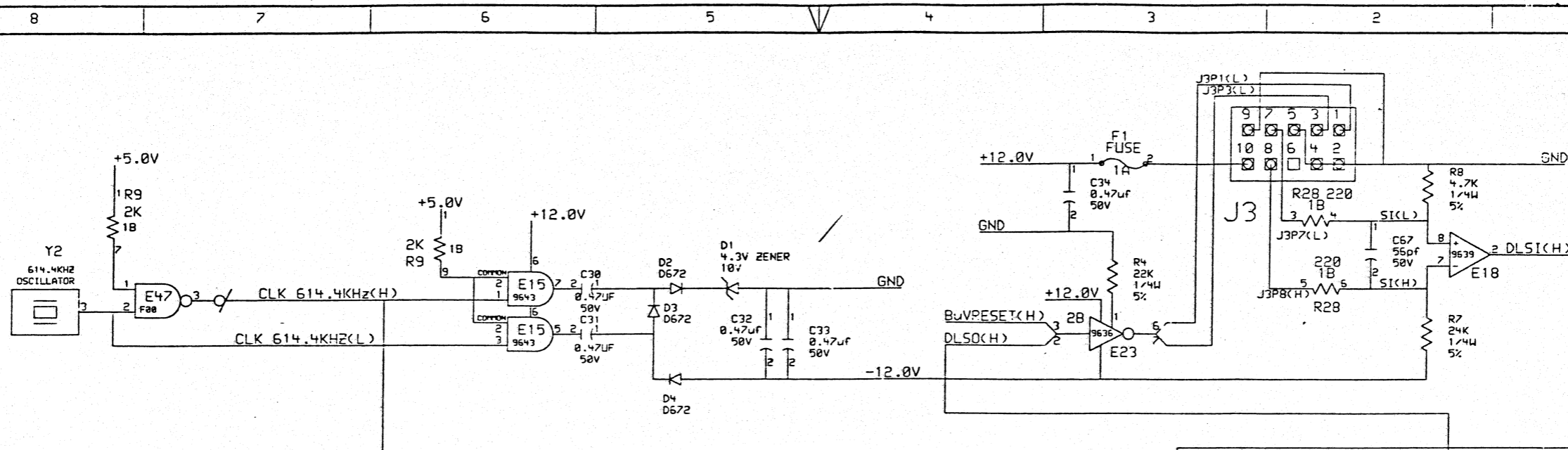
DRAWING
 TITLE=GA1
 ABBREV=GA!
 CIRCUIT+TYPE=GATE+ARRAY
 LAST+MODIFIED=Sun Oct 7 17:24:40 1984



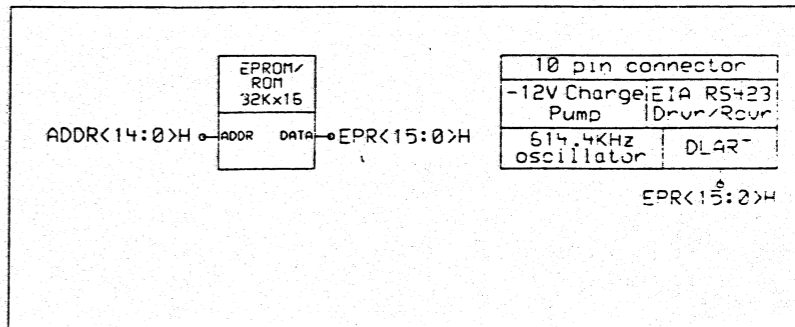
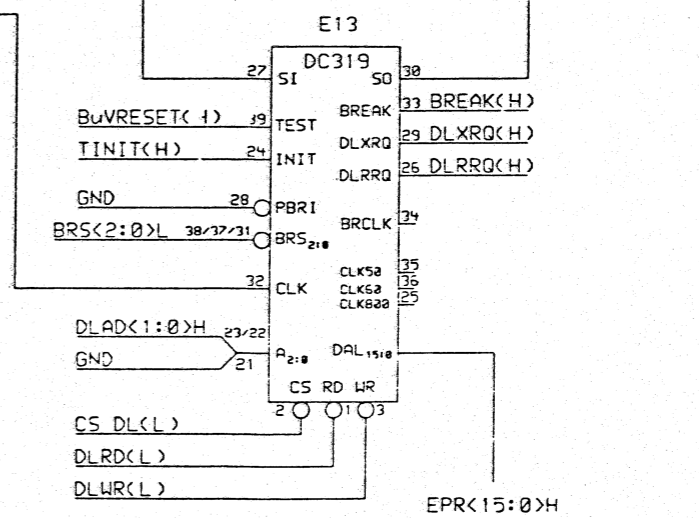
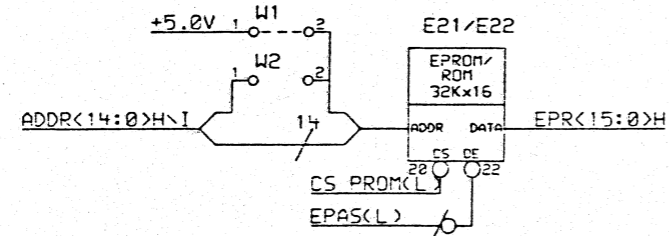
DRN: BARRY MASKAS
 CHK'D: BARRY MASKAS

DATE 19-DEC-83
 DATE 19-DEC-83
 SHEET 1 OF 1

ENG: BARRY MASKAS
 TITLE: MEMORY SYSTEM ERROR REGISTER
 NEXT HIGHER ASSEMBLY:
 SIZE CODE NUMBER REV
 D CS M7505 -2 -1 E



NOTE:
 W1 is normally installed (for 2764 & 27128 EPROM's)
 W2 is to be installed for 27256 EPROM's.



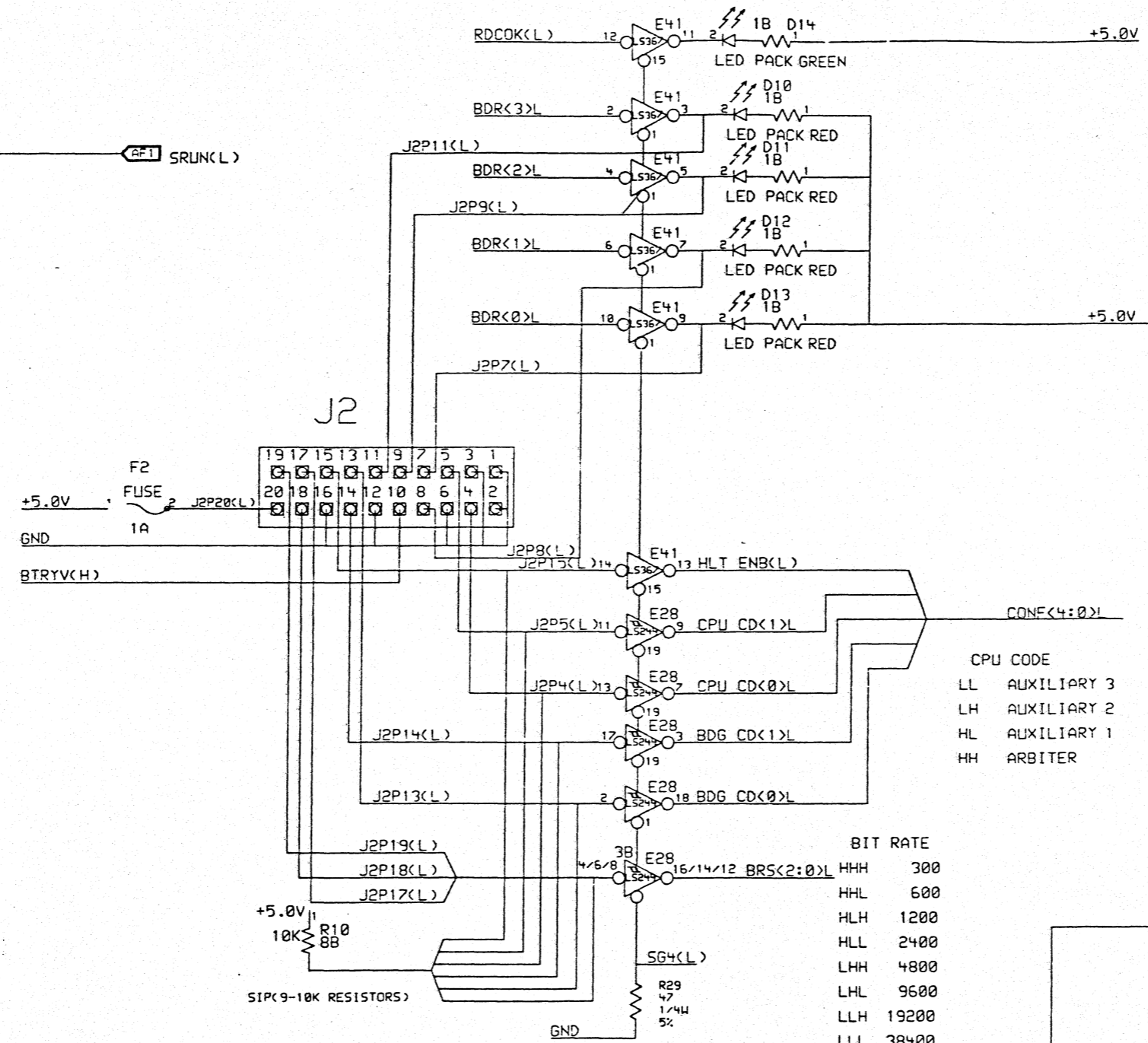
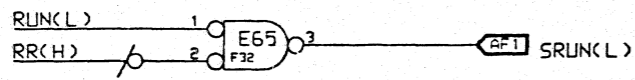
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REV	TECO NUMBER	DATE
0	11705	ALGO 12/22/83

DRAWING TITLE=COMM
 ABBREV=COMM
 CIRCUIT+TYPE=SERIAL+I/O
 LAST+MODIFIED=Fri Oct 12 14:27:55 1984

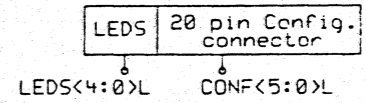
DEFINE
 X+FIRST=0
 X+STEP=SIZE

digital	DRN: BARRY MASKAS	DATE: 3-OCT-84	ENG: BARRI MASKAS	DATE: 3-OCT-84	TITLE: Console Serial Line Interface
	CHK'D: BARRY MASKAS	DATE: 3-OCT-84	SHEET: 1 OF 1	NEXT HIGHER ASSEMBLY:	SIZE: D CODE: CS NUMBER: M752E -2 -43 REV: 3



CPU CODE		BDG CODE	
LL	AUXILIARY 3	LL	MANUFACTURING
LH	AUXILIARY 2	LH	MAINTENANCE
HL	AUXILIARY 1	HL	LANGUAGE INQUIRE
HH	ARBITER	HH	NORMAL

BIT RATE	
HHH	300
HHL	600
HLH	1200
HLL	2400
LHH	4800
LHL	9600
LLH	19200
LLL	38400



1.12

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REVISION HISTORY		
REV	TECO NUMBER	DATE
B	ATVLA-1001-001442	10/29/84

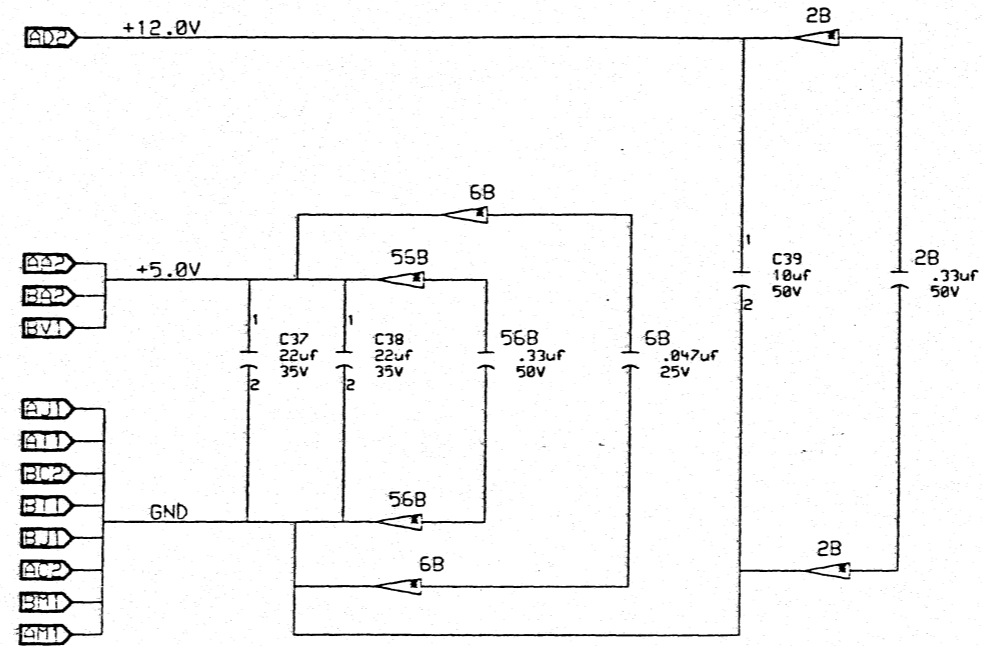
DRAWING
TITLE=LEDS
ABBREV=LEDS
CIRCUIT+TYPE=CONF+CONN
LAST+MODIFIED=Mon Oct 29 09:40:54 1984

DEFINE
X+FIRST=0
X+STEP=SIZE
digital

DRN: BARRY MASKAS
CHK'D: BARRY MASKAS
DATE: 3-OCT-84

ENG: BARRY MASKAS
SHEET OF
NEXT HIGHER ASSEMBLY:

TITLE:			
LEDS and Configuration Connector			
SIZE	CODE	NUMBER	REV
D	CS	M7605-01-44	3



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REVISION HISTORY		
REV	TECD NUMBER	DATE
1	17601-2001	10-07-84

DRAWING

TITLE=K0Q32

LAST MODIFIED=Sun Oct 7 20:49:41 1984

digital

DRN: BARRY MASKAS
 CHK'D: BARRY MASKAS

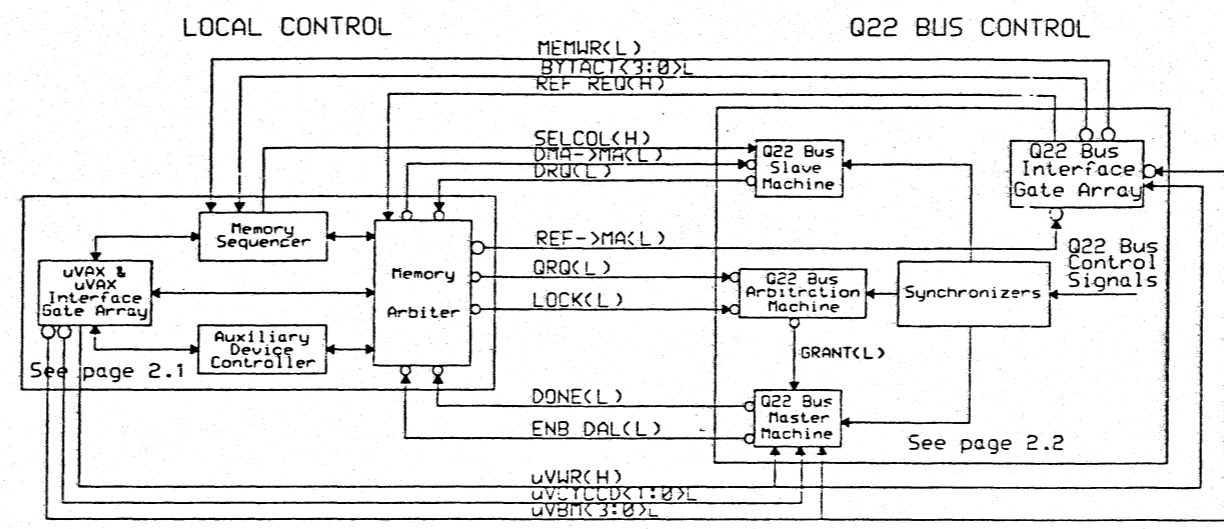
DATE 3-OCT-84
 DATE 3-OCT-84

ENG: BARRY MASKAS
 NEXT HIGHER ASSEMBLY:

DATE 3-OCT-84
 SHEET 1 OF 1

TITLE: Decoupling Capacitors

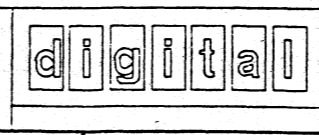
SIZE	CODE	NUMBER	REV
D	CS	M7525 -2 -5	3



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REVISION HISTORY		
REV	ECO NUMBER	DATE
0		8-DEC-83

DRAWING
 TITLE=CTLBLOCK
 ABBREV=ct1
 CIRCUIT+TYPE=CONTROL
 LAST+MODIFIED=Mon Oct 29 09:44:18 1984

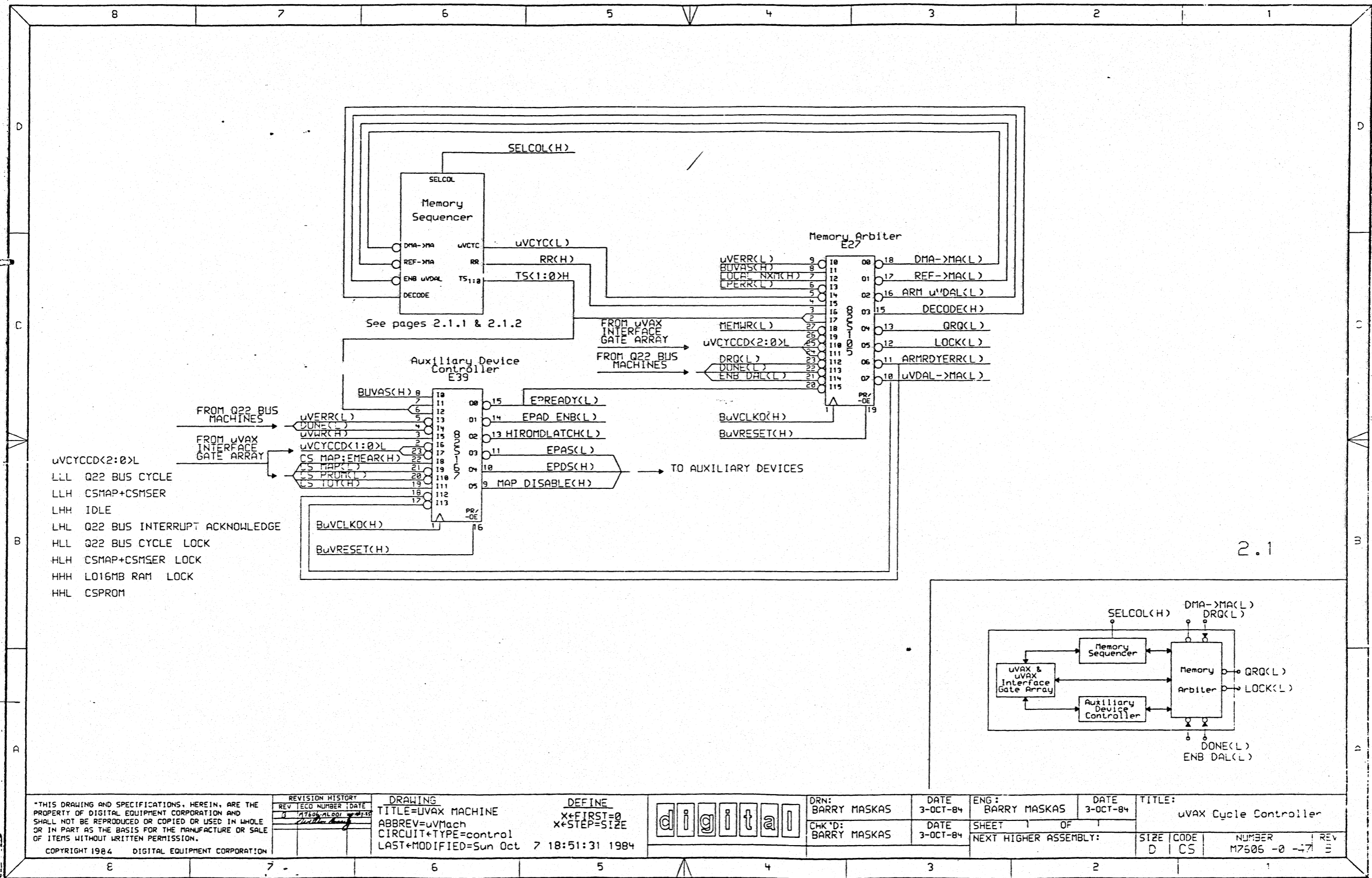


DRN: BARRY MASKAS
 DATE: 8-DEC-83
 CHK'D: R. MCNAMARA
 DATE: 8-DEC-83

ENG: BARRY MASKAS
 DATE: 8-DEC-83
 SHEET 1 OF 1
 NEXT HIGHER ASSEMBLY:

TITLE: KA530 State Machines
 SIZE: D
 CODE: CS
 NUMBER: M7535-2-46
 REV: 3

12



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REVISION HISTORY		
REV	TECD NUMBER	DATE
0	17506-1000	3-17-84

DRAWING
 TITLE=UVAX MACHINE
 ABBREV=uVMach
 CIRCUIT+TYPE=control
 LAST+MODIFIED=Sun Oct 7 18:51:31 1984

DEFINE
 X*FIRST=0
 X*STEP=SIZE

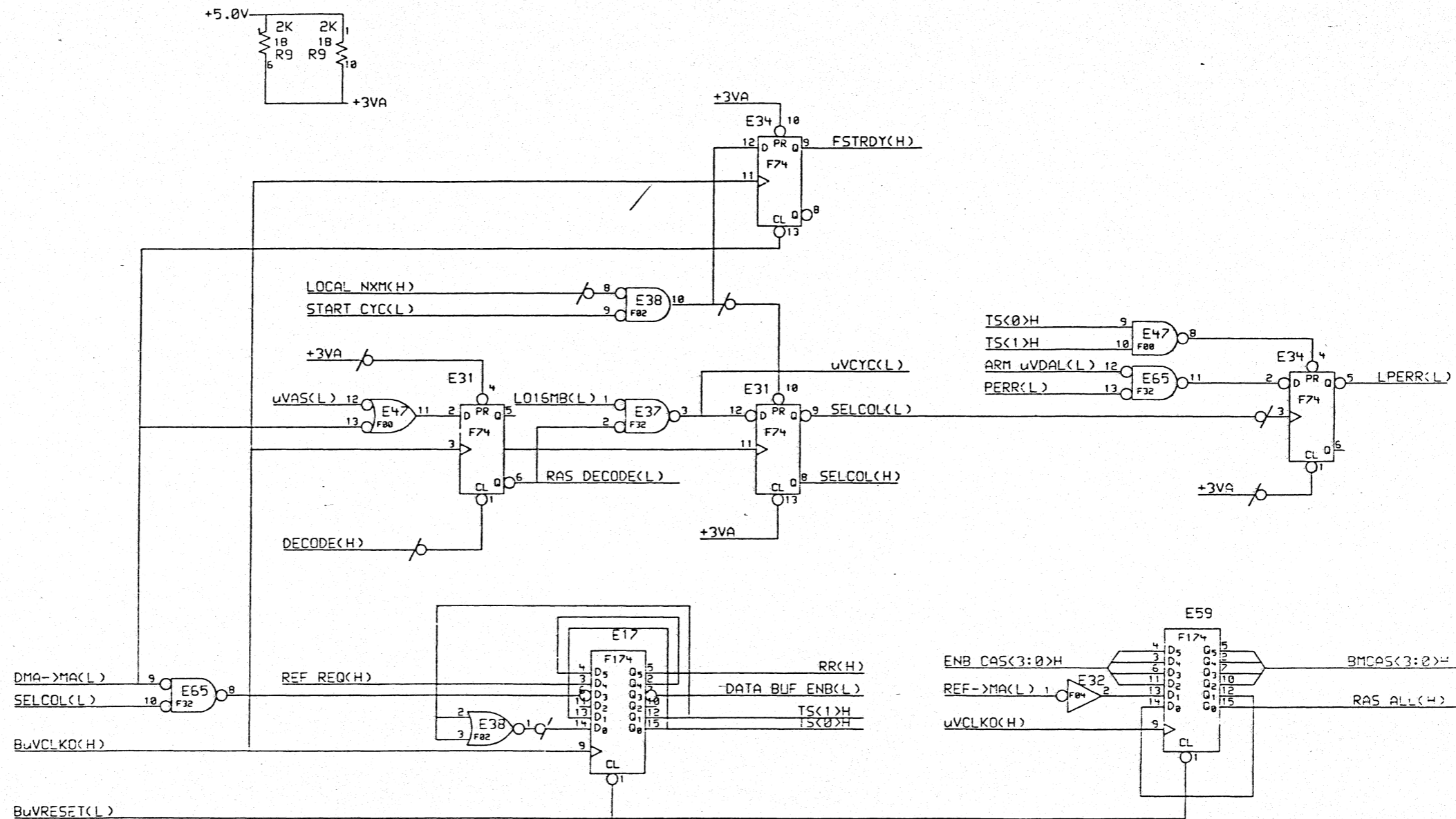
digital

DRN: BARRY MASKAS	DATE 3-OCT-84	ENG: BARRY MASKAS	DATE 3-OCT-84
CHK'D: BARRY MASKAS	DATE 3-OCT-84	SHEET 1	OF 1

TITLE:
 uVAX Cycle Controller

NEXT HIGHER ASSEMBLY:

SIZE	CODE	NUMBER	REV
D	CS	M7506-0	-47 3



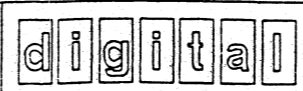
TS<1:0> STATE TABLE (uVAX Microcycle Counter)

s	ns	State
T4	00 01	first uVAX CLKO after /BuVRESET
T1	01 11	
T2	11 10	
T3	10 00	

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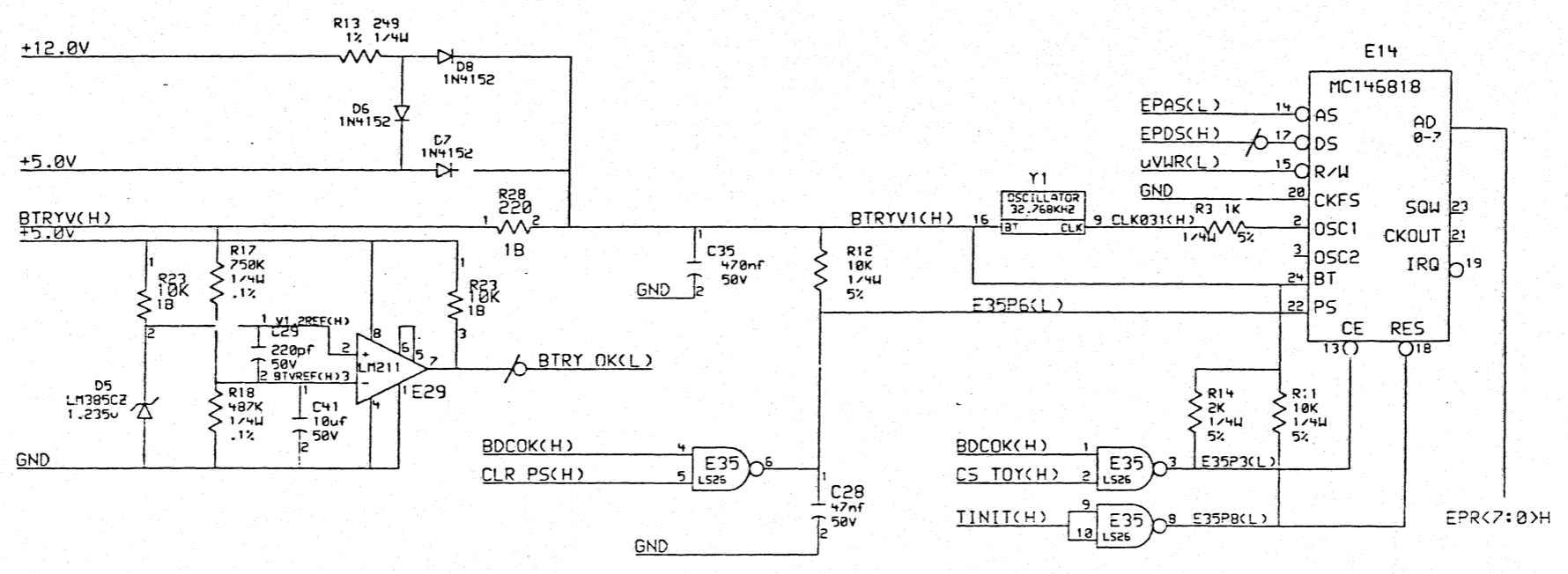
REV	TECD	NUMBER	DATE
A	M	1	10/12/84

DRAWING
 TITLE=MEM CTRLR
 ABBREV=MEMCTRL
 CIRCUIT+TYPE=MEM+CTRL
 LAST+MODIFIED=Fr1 Oct 12 14:23:21 1984



DRN: BARRY MASKAS
 DATE: 18-DEC-83
 ENG: BARRY MASKAS
 DATE: 18-DEC-83
 SHEET 1 OF 1
 NEXT HIGHER ASSEMBLY:

TITLE: MEMORY SEQUENCER
 SIZE CODE NUMBER REV
 D 05 M7605 -2 -43 B



Battery Sense/Charge
 32.768KHz TOY oscillator/Clock
 EPR<7:0>H

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REVISION HISTORY		
REV	ECO NUMBER	DATE
0	27150A	1984

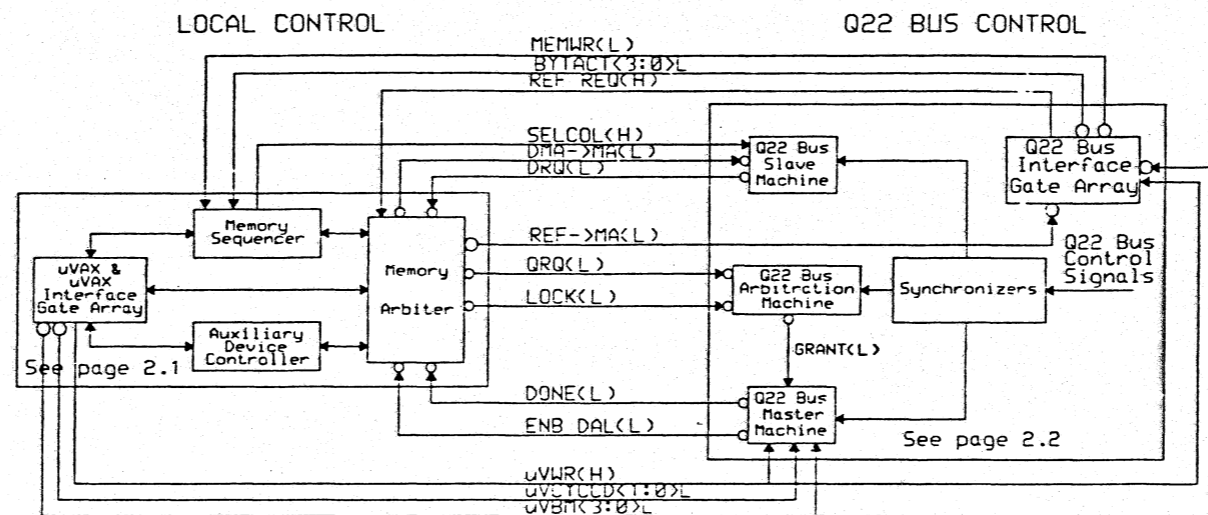
DRAWING
 TITLE=TOY
 ABBREV=TOY
 CIRCUIT+TYPE=TOY/CLOCK
 LAST+MODIFIED=Fri Oct 12 11:59:59 1984

DEFINE
 X+FIRST=0
 X+STEP=SIZE
 digital

DRN: BARRY MASKAS
 DATE: 3-OCT-84
 CHK'D: BARRY MASKAS
 DATE: 3-OCT-84

ENG: BARRY MASKAS
 DATE: 3-OCT-84
 SHEET 1 OF 1
 NEXT HIGHER ASSEMBLY:

TITLE: TIME OF YEAR (TOY) Clock
 SIZE CODE NUMBER REV
 0 CS M7625 -2 -12 6

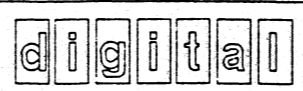


2

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REVISION HISTORY		
REV	ECO NUMBER	DATE
0		8-DEC-83

DRAWING
 TITLE=CTLBLOCK
 ABBREV=ct1
 CIRCUIT+TYPE=CONTROL
 LAST+MODIFIED=Mon Oct 29 09:44:18 1984

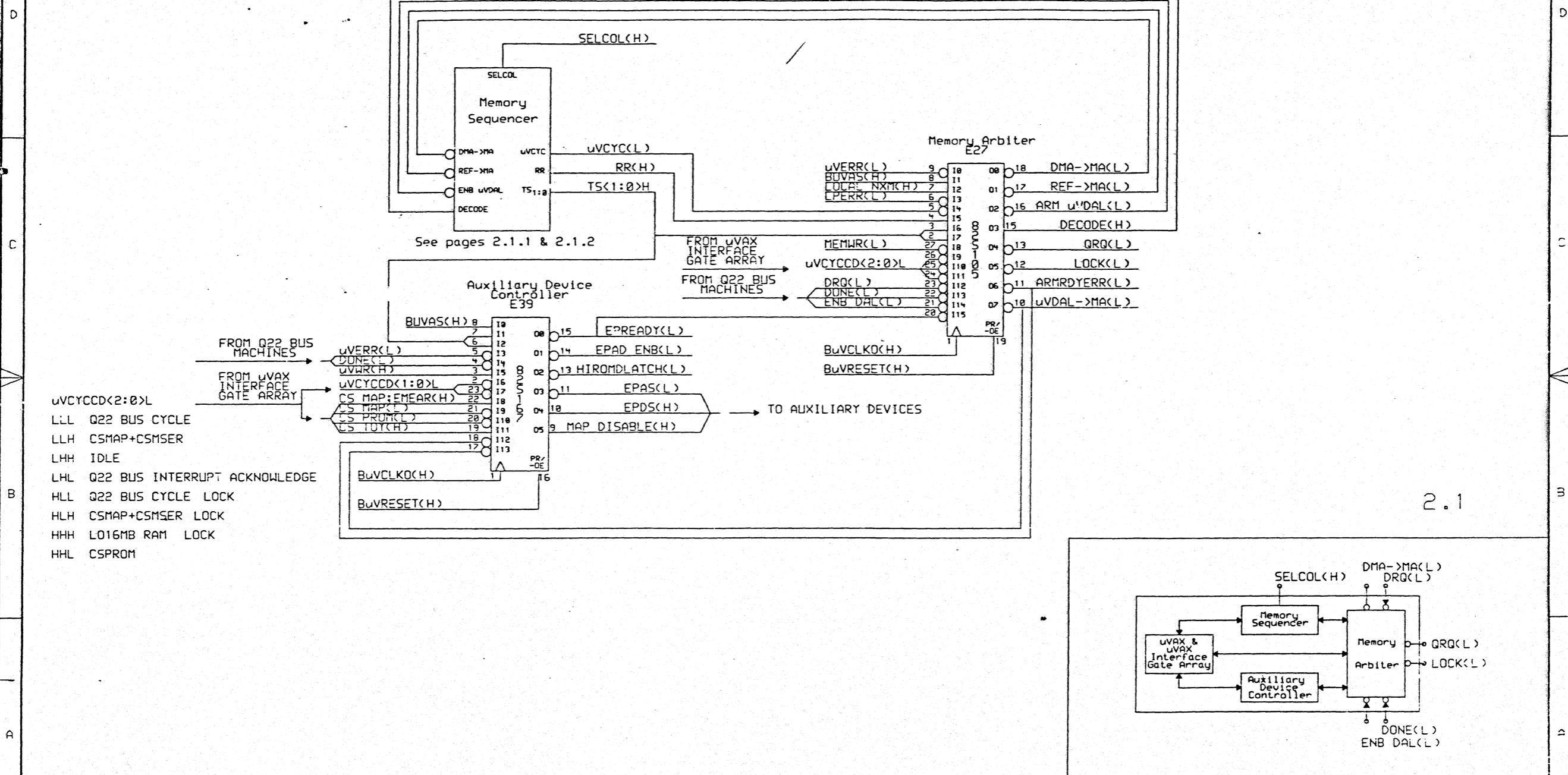


DRN: BARRY MASKAS
 DATE: 8-DEC-83
 CHK'D: R. MCNAMARA
 DATE: 8-DEC-83

ENG: BARRY MASKAS
 DATE: 8-DEC-83
 SHEET 1 OF 1
 NEXT HIGHER ASSEMBLY:

TITLE: KA530 State Machines
 SIZE: 17
 CODE: CS
 NUMBER: M7635 -2 -46
 REV: B

8 7 6 5 4 3 2 1



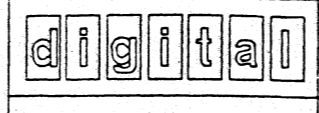
2.1

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REVISION HISTORY		
REV	TECD NUMBER	DATE
1	1760	ALGOI 10/1/83

DRAWING
 TITLE=UVAX MACHINE
 ABBREV=uvMach
 CIRCUIT+TYPE=control
 LAST+MODIFIED=Sun Oct 7 18:51:31 1984

DEFINE
 X+FIRST=0
 X+STEP=SIZE

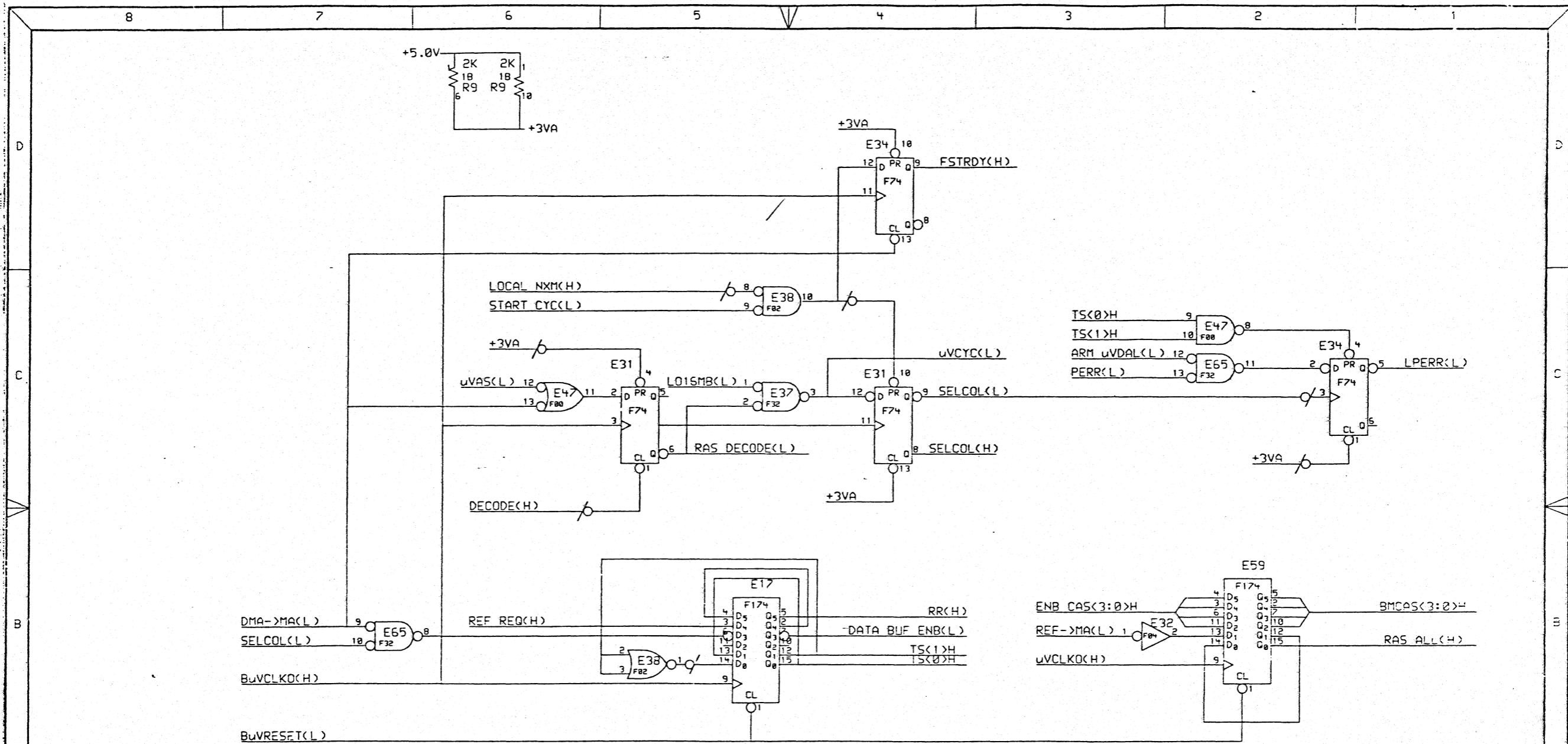


DRN: BARRY MASKAS
 DATE: 3-OCT-84
 CHK'D: BARRY MASKAS
 DATE: 3-OCT-84

ENG: BARRY MASKAS
 DATE: 3-OCT-84
 SHEET: 1 OF 1
 NEXT HIGHER ASSEMBLY:

TITLE: uVAX Cycle Controller
 SIZE: D CODE: CS NUMBER: M7505-0 REV: 1

E 7 6 5 4 3 2 1



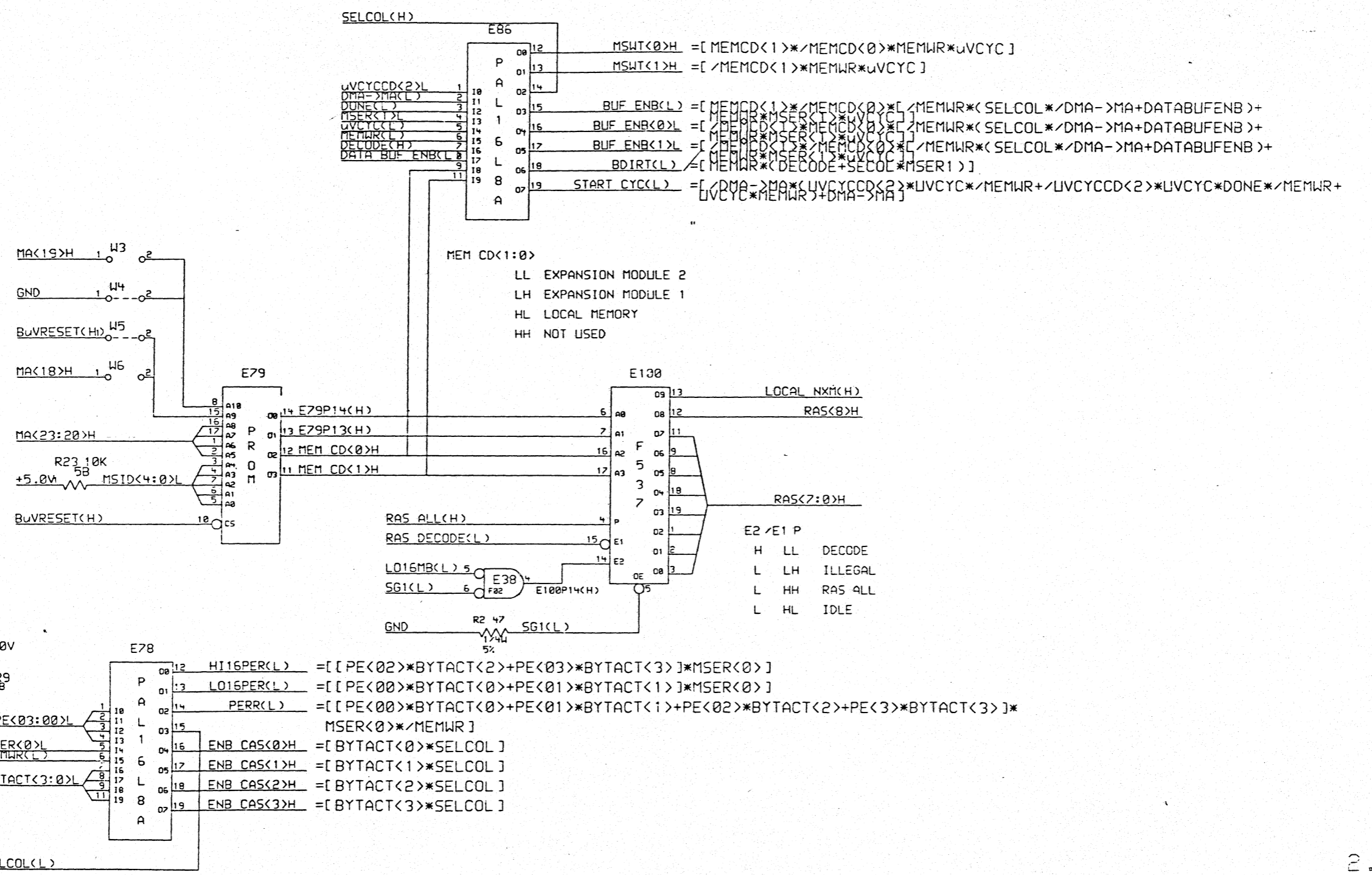
TS<1:0> STATE TABLE (uVAX Microcycle Counter)

s	ns	State
T4	00 01	first uVAX CLK0 after /BuVRESET
T1	01 11	
T2	11 10	
T3	10 00	

2.1.1

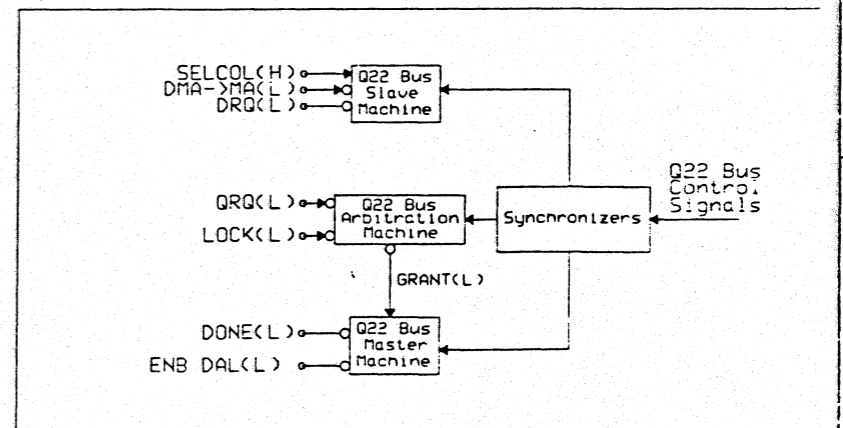
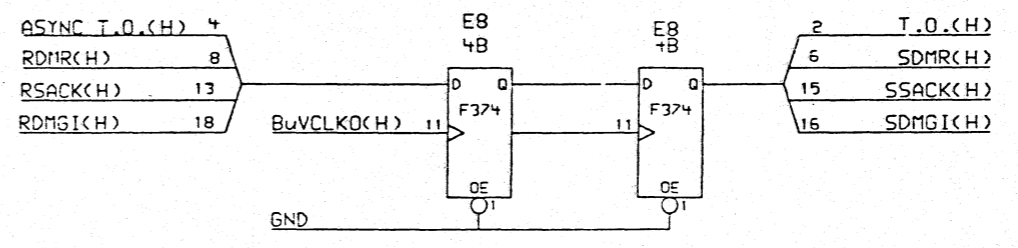
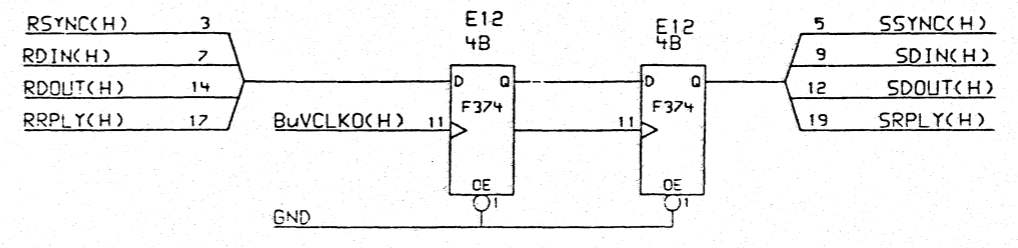
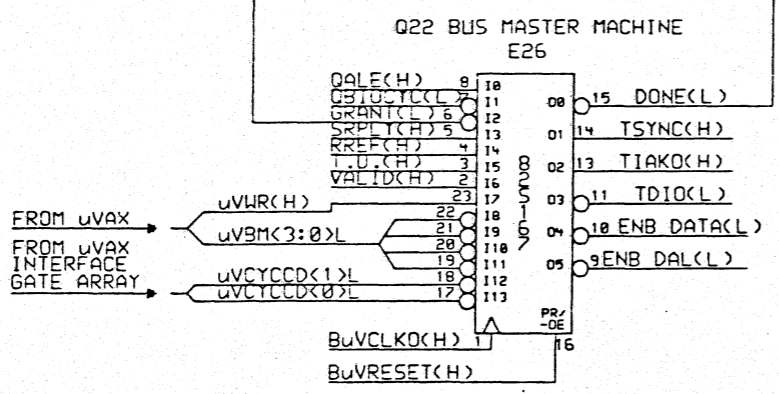
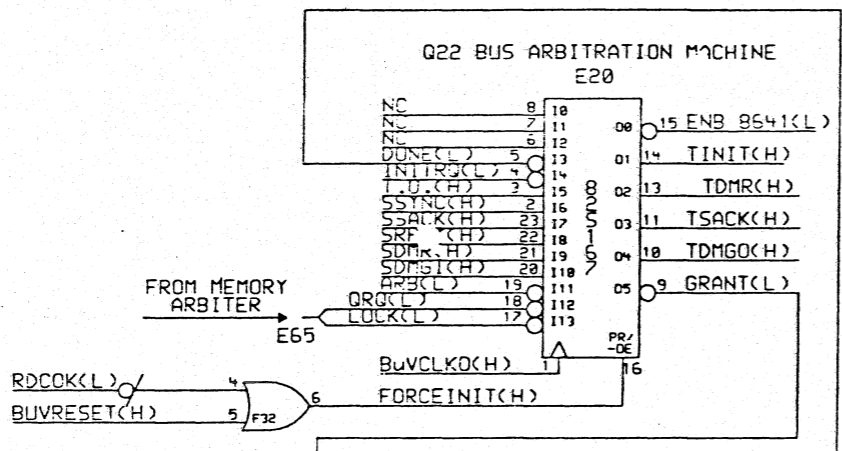
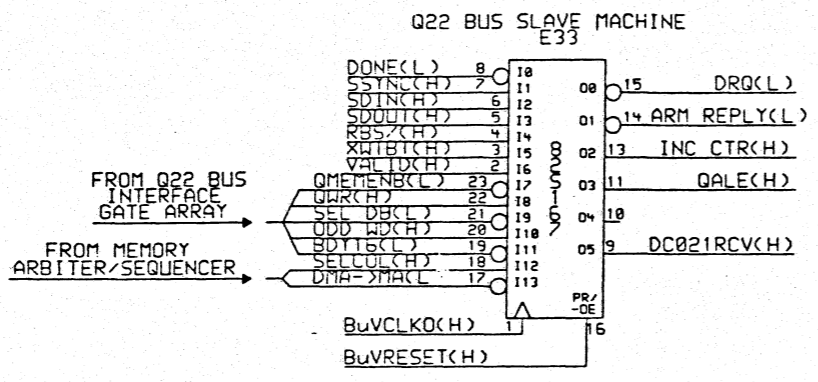
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	SIZE D	CODE CS 1	NUMBER M7605-2-13	REV B			

8 7 6 5 4 3 2 1



2.1.2

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	8 7 6 5 4 3 2 1										
	8 7 6 5 4 3 2 1										



2.2

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REV	TECO NUMBER	DATE
1		3-10-84

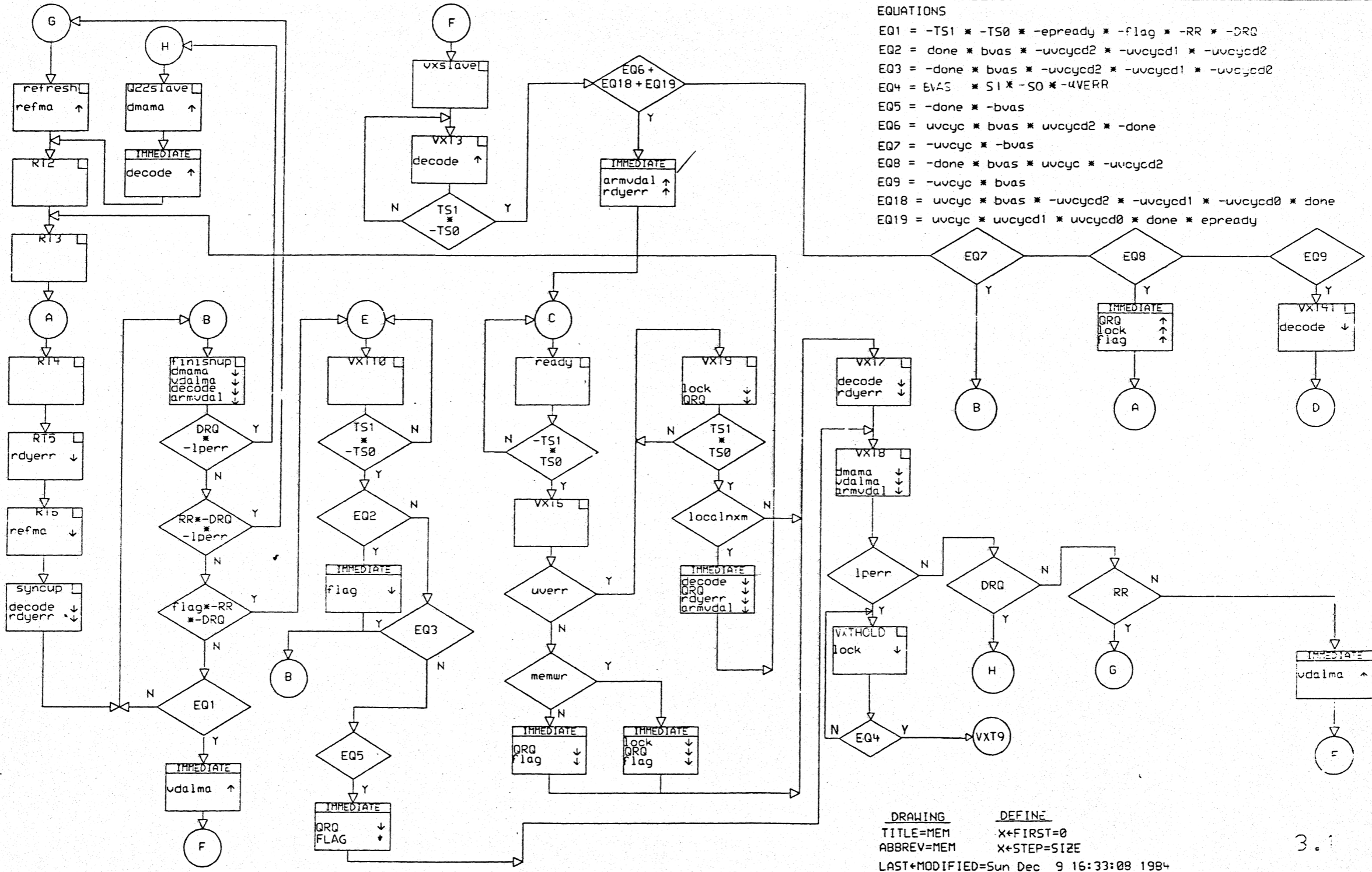
DRAWING
TITLE=QBUS MACHINE
ABBREV=QCTRL
CIRCUIT+TYPE=QBUS+CNTRL
LAST+MODIFIED=Fri Oct 12 12:21:22 1984

DEFINE
X*LIST=0
X*STEP=SIZE
digital

DRN: R. McNamara
DATE: 3-OCT-84
CHK'D: R. McNamara
DATE: 3-OCT-84

ENG: R. McNamara
DATE: 3-OCT-84
SHEET 1 OF 1
NEXT HIGHER ASSEMBLY:

TITLE: Q22 BUS STATE MACHINES
SIZE CODE: D CS
NUMBER: M7505 -0 -50
REV: B



EQUATIONS
 EQ1 = $\neg TS1 \cdot \neg TS0 \cdot \neg epready \cdot \neg flag \cdot \neg RR \cdot \neg DRQ$
 EQ2 = $done \cdot bvas \cdot \neg uvcycd2 \cdot \neg uvcycd1 \cdot \neg uvcycd0$
 EQ3 = $\neg done \cdot bvas \cdot \neg uvcycd2 \cdot \neg uvcycd1 \cdot \neg uvcycd0$
 EQ4 = $EVS \cdot S1 \cdot \neg S0 \cdot \neg UVERR$
 EQ5 = $\neg done \cdot \neg bvas$
 EQ6 = $uvcyc \cdot bvas \cdot uvcycd2 \cdot \neg done$
 EQ7 = $\neg uvcyc \cdot \neg bvas$
 EQ8 = $\neg done \cdot bvas \cdot uvcyc \cdot \neg uvcycd2$
 EQ9 = $\neg uvcyc \cdot bvas$
 EQ18 = $uvcyc \cdot bvas \cdot \neg uvcycd2 \cdot \neg uvcycd1 \cdot \neg uvcycd0 \cdot done$
 EQ19 = $uvcyc \cdot uvcycd1 \cdot uvcycd0 \cdot done \cdot epready$

DRAWING DEFINE
 TITLE=MEM X*FIRST=0
 ABBREV=MEM X*STEP=SIZE
 LAST*MODIFIED=Sun Dec 9 16:33:08 1984

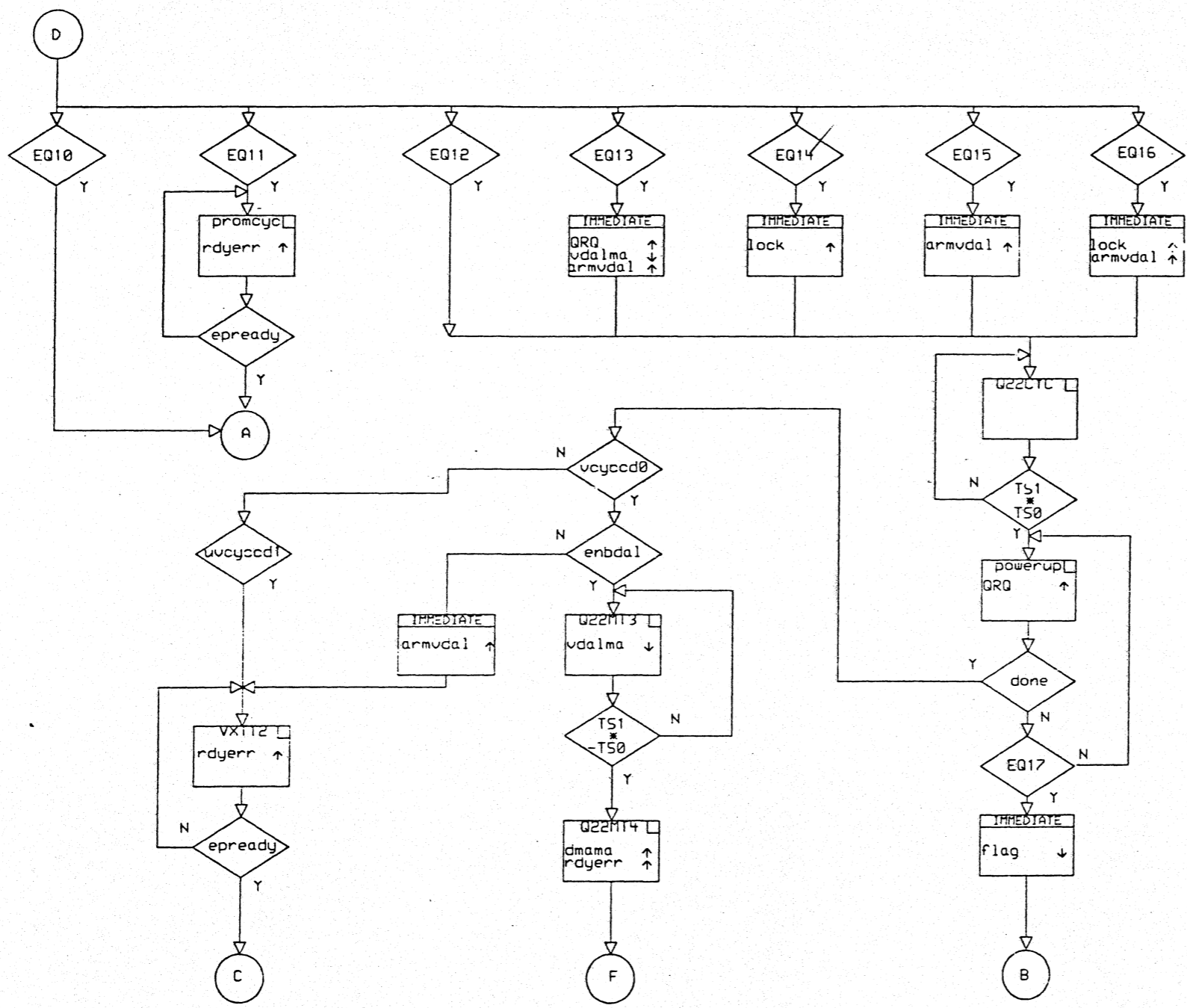
3.1

REVISION	DATE	BY
1		

DATE	BY	DATE	BY
DATE	BY	DATE	BY

TITLE	NUMBER	REV.
KAS30 MEMORY SYSTEM CONTROLLER STATE FLOW DIAGRAMS	M7606-0-02	

DIGITAL M7606 0 1 H



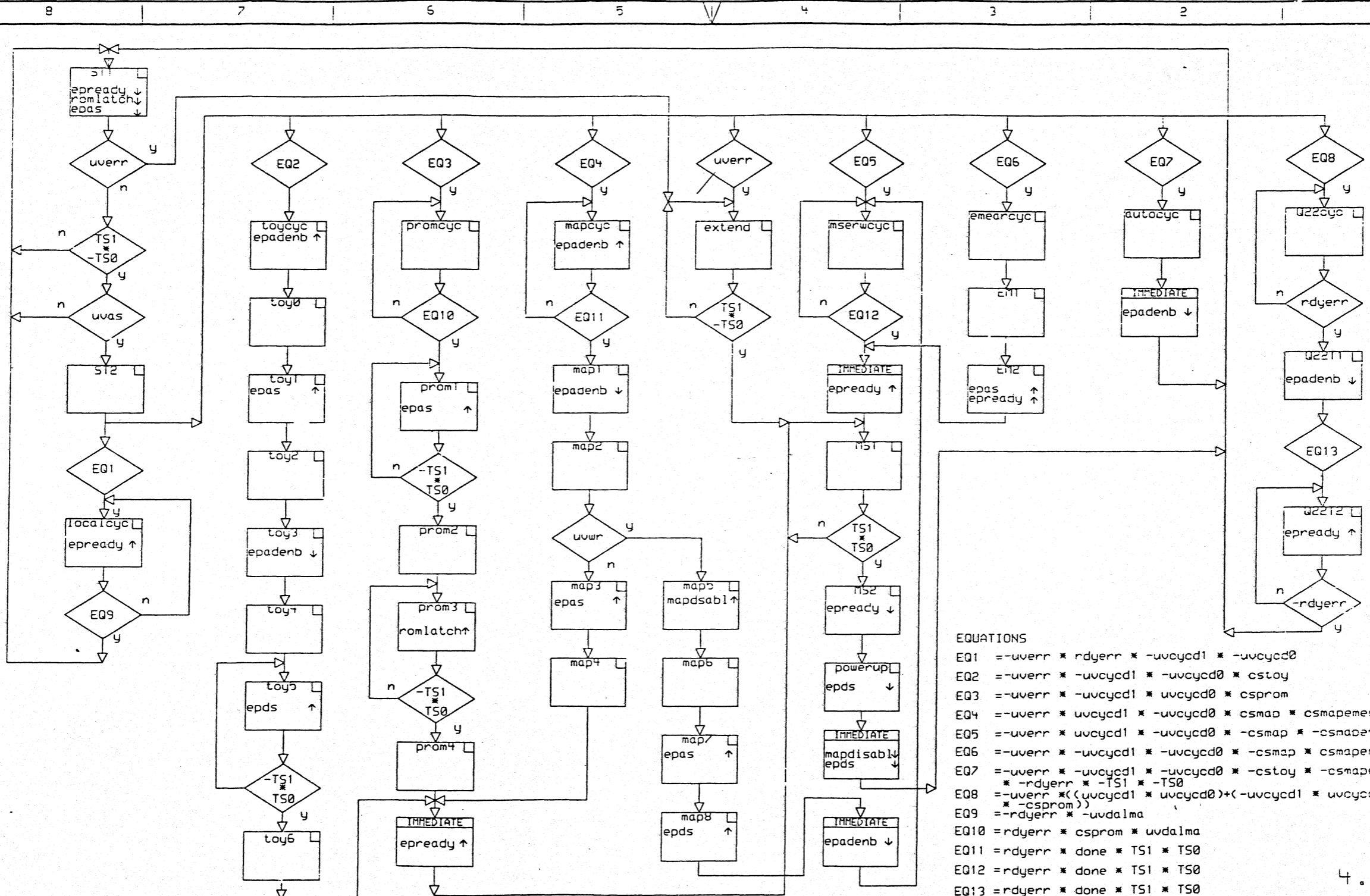
- EQUATIONS
- EQ10 = -uvccyc * -uvccyd1 * -uvccyd0
 - EQ11 = -uvccyc * -uvccyd2 * -uvccyd1 * uvccyd0
 - EQ12 = -uvccyc * uvccyd2 * uvccyd1 * -uvccyd0
 - EQ13 = -uvccyc * uvccyd2 * -uvccyd1 * uvccyd0
 - EQ14 = -uvccyc * -uvccyd2 * uvccyd1 * -uvccyd0
 - EQ15 = -uvccyc * uvccyd2 * uvccyd1 * uvccyd0
 - EQ16 = -uvccyc * -uvccyd2 * uvccyd1 * uvccyd0
 - EQ17 = DRQ + TS1 * -TS0 * RR

DRAWING
 NAME=MEM
 ABBREV=MEM
 LAST MODIFIED=Sun Dec 9 16:40:59 1984

3.2

REVISION	CHK	CHANGE NO	REV
1			

digital	DRN BARRY MASKAS	DATE 88-02-10	REV 1	DATE 88-02-10	TITLE: K4630 MEMORY SYSTEM ARBITRATOR STATE FLOW DIAGRAMS
USRA:	CHK'D BARRY MASKAS	DATE 88-02-10	SHEET 2	TOP DOCUMENT NUMBER:	SIZE CODE 0 CS
FIRST USED ON OPTION/MODEL:					NUMBER M7500-2-33
					REV 3



EQUATIONS

EQ1 = -uverr * rdycrr * -uvcycd1 * -uvcycd0

EQ2 = -uverr * -uvcycd1 * -uvcycd0 * cstoy

EQ3 = -uverr * -uvcycd1 * uvcycd0 * csrom

EQ4 = -uverr * uvcycd1 * -uvcycd0 * csmap * csmapemear

EQ5 = -uverr * uvcycd1 * -uvcycd0 * -csmap * -csmapemear

EQ6 = -uverr * -uvcycd1 * -uvcycd0 * -csmap * csmapemear

EQ7 = -uverr * -uvcycd1 * -uvcycd0 * -cstoy * -csmapemear

EQ8 = -uverr * ((uvcycd1 * uvcycd0) + (-uvcycd1 * uvcycd0 * -csrom))

EQ9 = -rdycrr * -uvdalma

EQ10 = rdycrr * csrom * uvdalma

EQ11 = rdycrr * done * TS1 * TS0

EQ12 = rdycrr * done * TS1 * TS0

EQ13 = rdycrr * done * TS1 * TS0

4.1

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REV	TECO NUMBER	DATE
1		

DRAWING

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ABBREV=EPR

LAST*MODIFIED=Mon Oct 22 15:14:12 1984

DEFINE

X*FIRST=0
X*STEP=SIZE

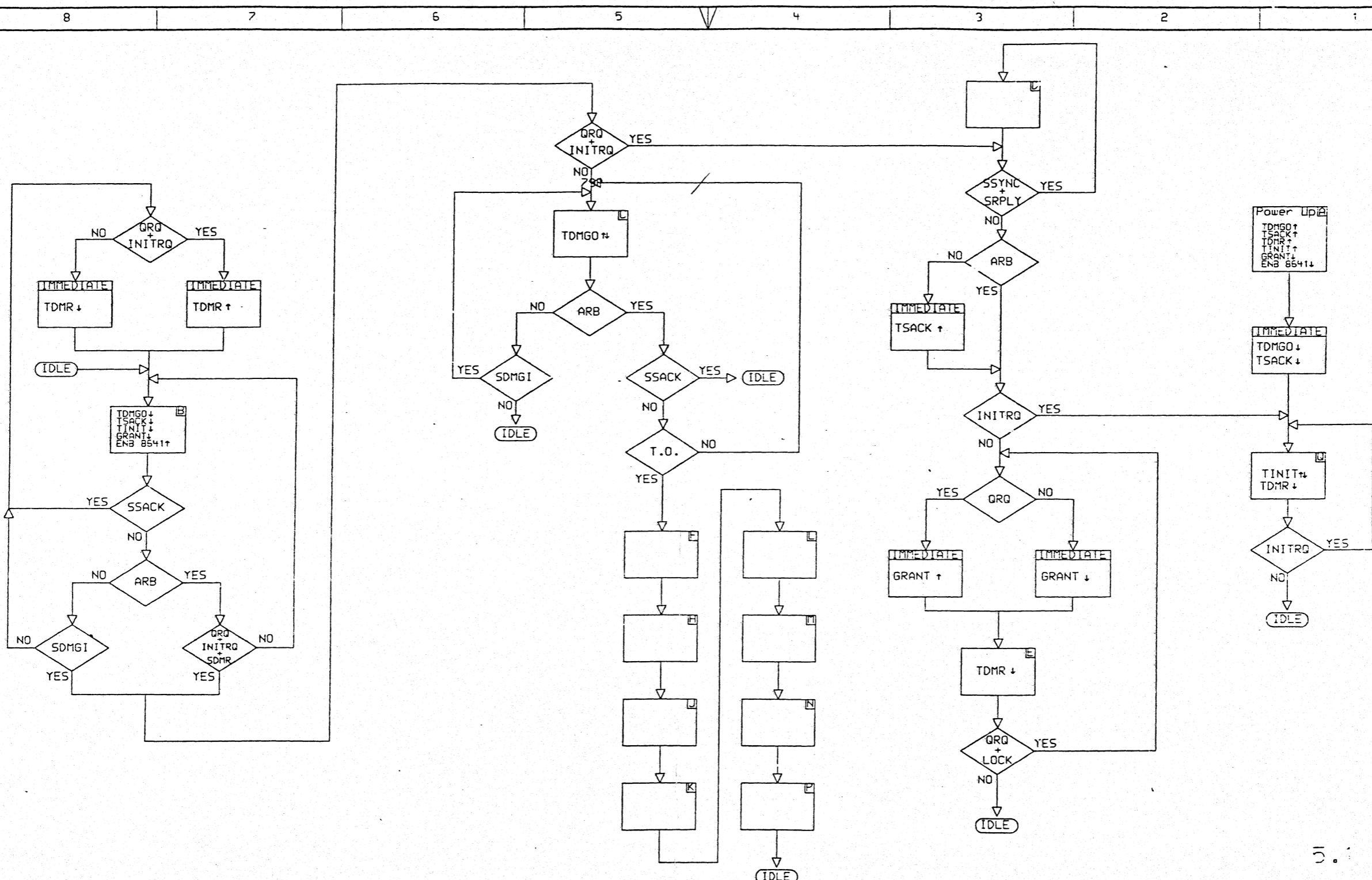
DRN: BARRY MASKAS
CHK'D: BARRY MASKAS

DATE 28-AUG-1984
DATE 28-AUG-1984

ENG: BARRY MASKAS
SHEET 1 OF 1
NEXT HIGHER ASSEMBLY:

TITLE: KA630 LOCAL I/O BUS CONTROL STATE MACHINE

SIZE	CODE	NUMBER	REV
L	CS	M7606 -0 -55	F

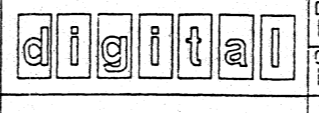


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REVISION HISTORY		
REV	ECO NUMBER	DATE
1		6-Jul-84
2		6-Jul-84

DRAWING
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 ABBREV=arb
 LAST+MODIFIED=Mon Oct 22 15:04:38 1984

DEFINE
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 X+STEP=SIZE



DRN:
 R. McNamara
 CHK'D:
 R. McNamara

DATE
 6-Jul-84

ENC:
 R. McNamara

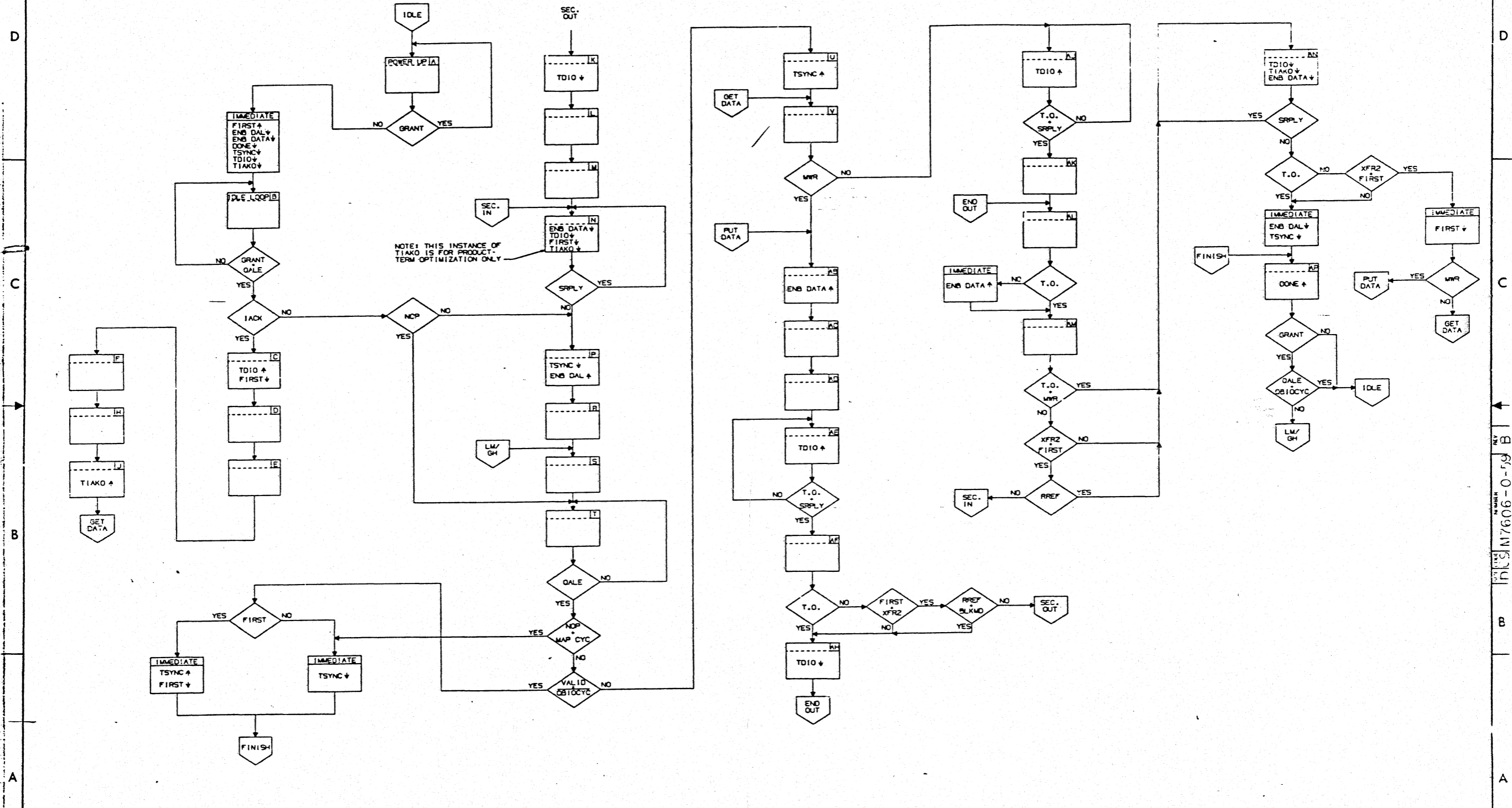
DATE
 6-Jul-84

TITLE:
 QBUS ARBITRATION CONTROLLER
 RETAILED CONTROL FLOW DIAGRAM

SHEET 1 OF 1
 NEXT HIGHER ASSEMBLY:

SIZE CODE NUMBER
 D | CS | M7535 -2 -57

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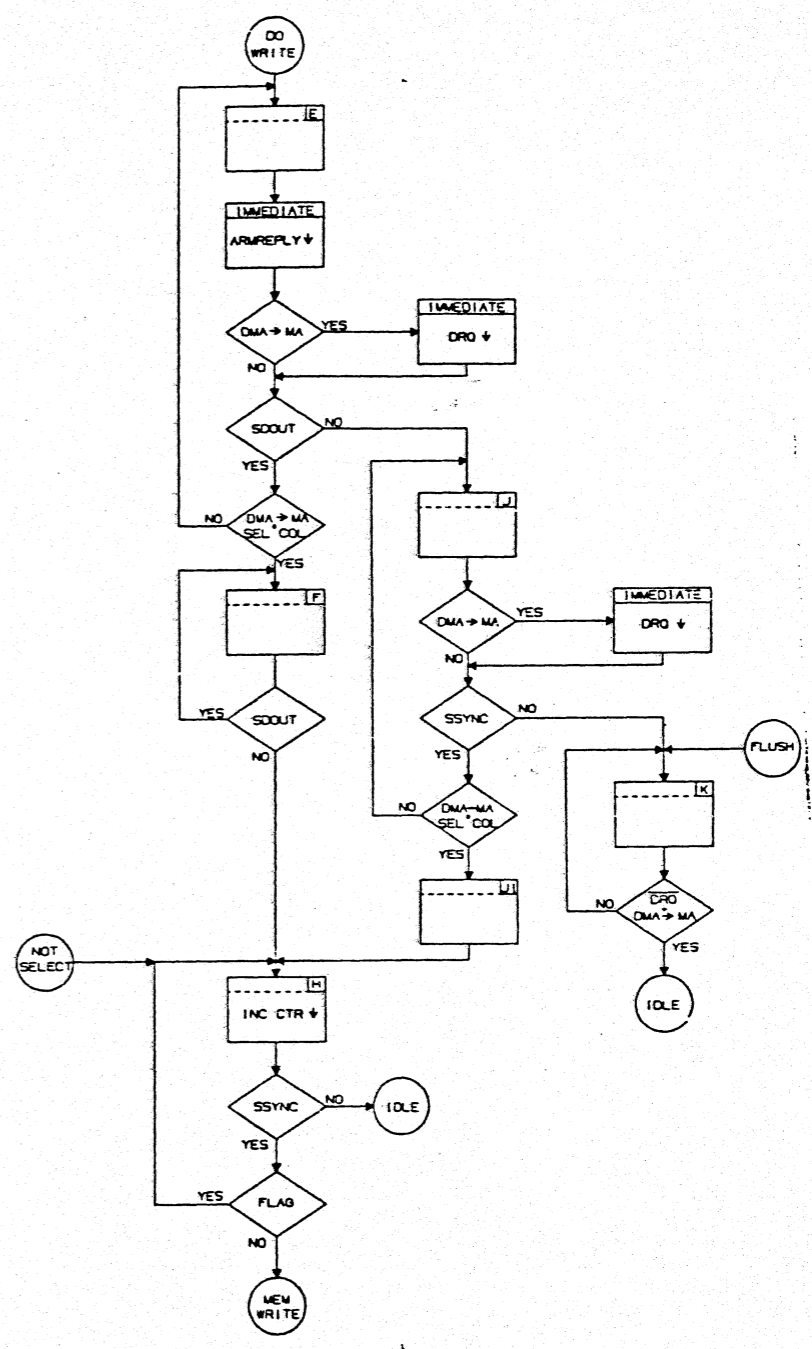
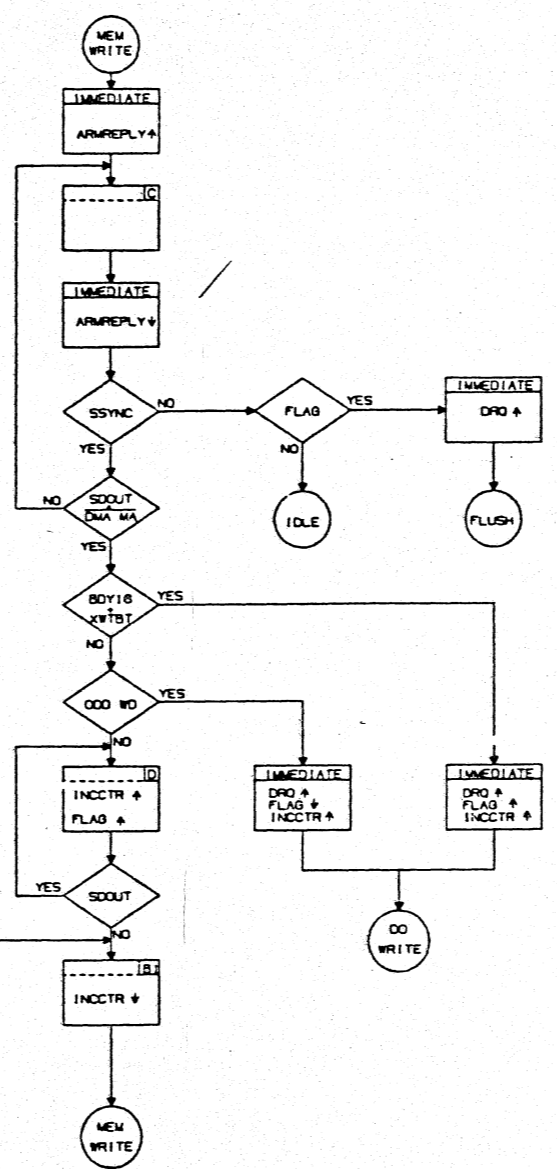
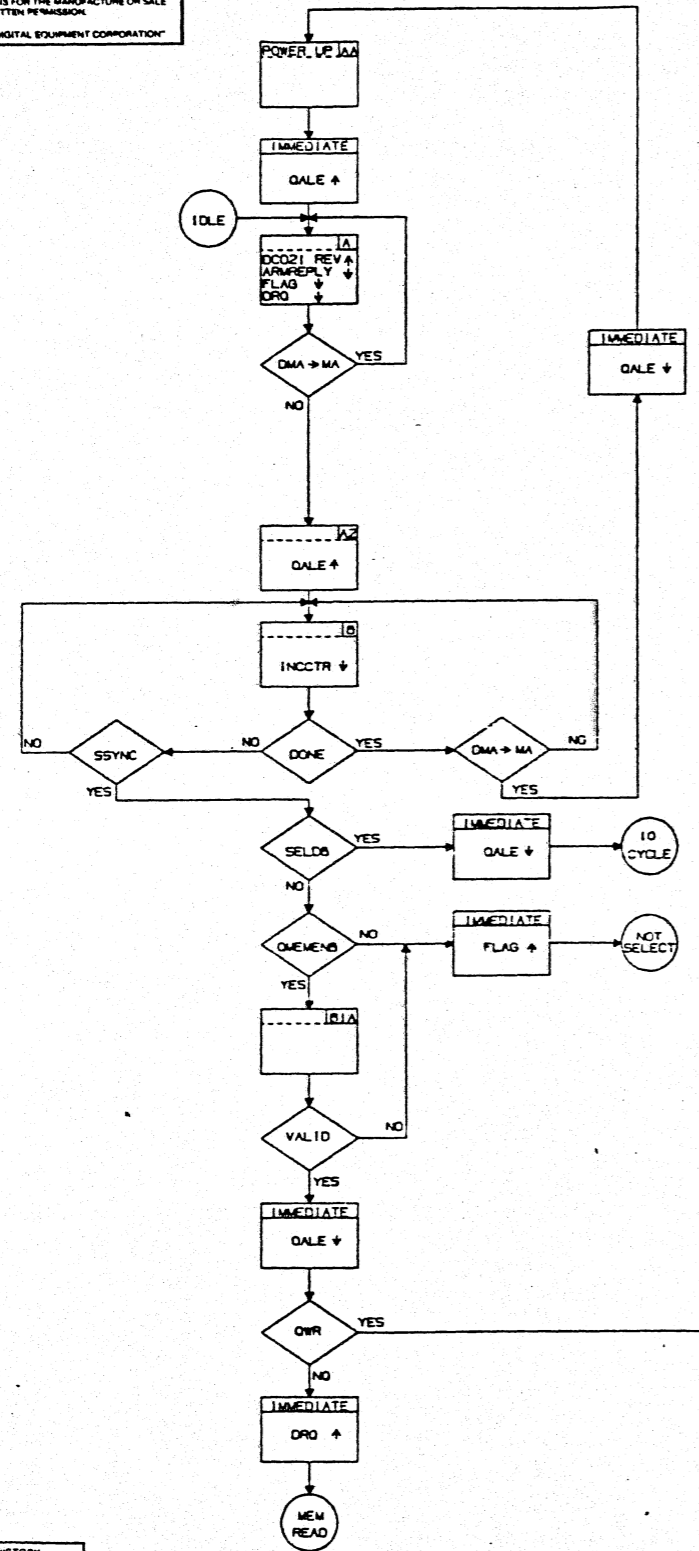


REVISION HISTORY		
DATE	ECO NUMBER	REV

TITLE
Q22 BUS MASTER CONTROL
MACHINE FLOW DIAGRAM

DOCUMENT NUMBER		
SIZE CODE	NUMBER	REV
DCS	M7606-0-59	3
SCALE	SHEET 1 OF	

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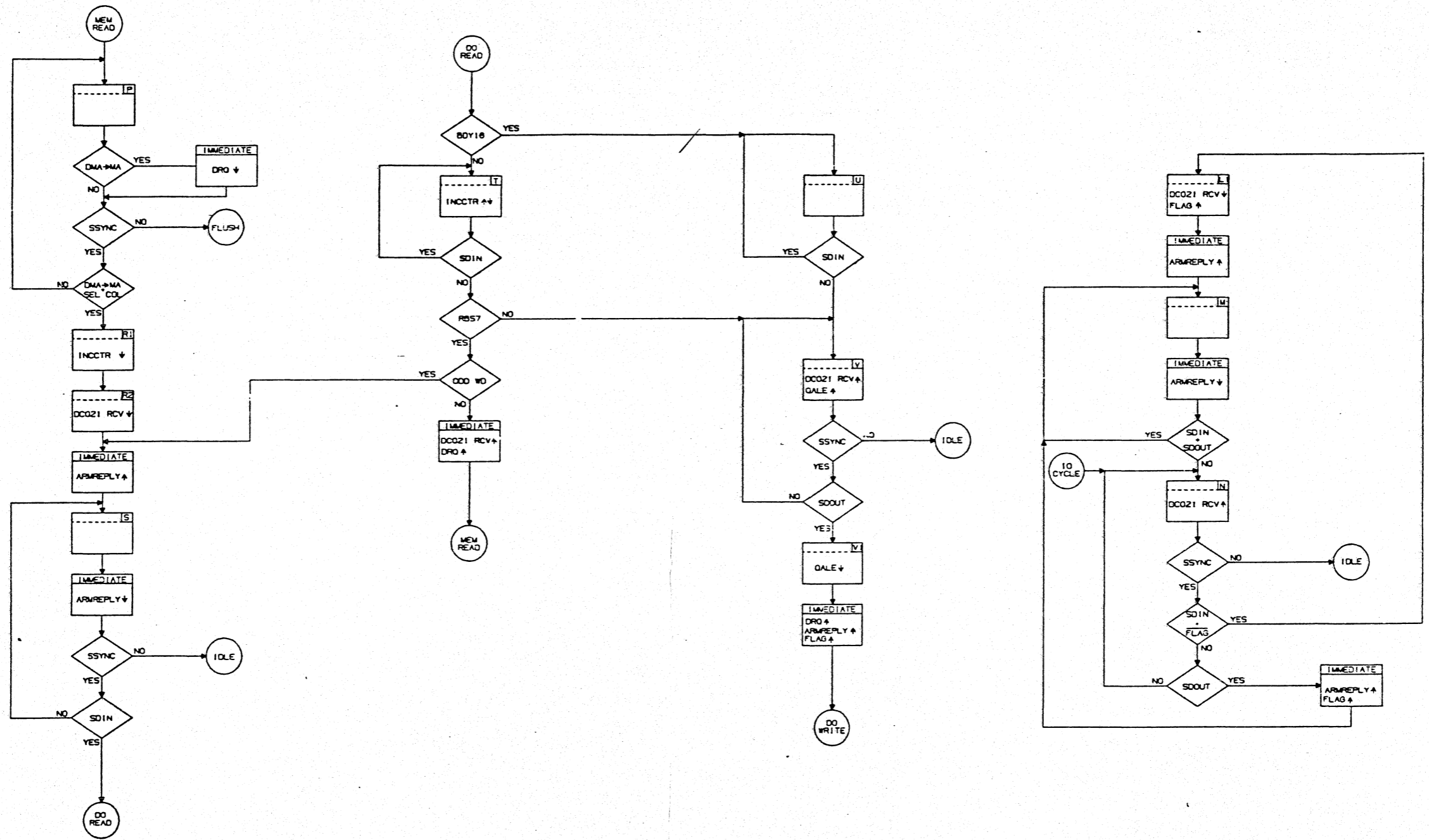


DATE	ECO NUMBER	REV
11/26/84	15501	1
12/10/84	15501	2

TITLE Q22 BUS SLAVE CONTROL MACHINE FLOW DIAGRAM

SIZE	CODE	NUMBER	REV
DCSM	7606	0-01	F

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REVISION HISTORY		
DATE	ECO NUMBER	REV

TITLE
Q22 BUS SLAVE CONTROL
MACHINE FLOW DIAGRAM

DOCUMENT NUMBER		
SIZE	CODE	NUMBER
D00	M7606-0-02	E
SCALE	SHEET / OF /	