Lectures on Analog Electronics

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C O N N E X I O N S

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Chapter 1

The New Syllabus of EC1X05_Lectures on AnalogElectronics[1]

1.1 EC 1x05Analog Electronics

L-T-P: 3-0-3 Credit: 5

Semiconductor diodes, Bipolar Junction Transistors and MOSFETs.

Biasing circuits of BJT, FET and MOSFET, RC and DC coupled amplifiers, wide-band and tuned amplifiers. Active impedance transformers(Gyrators), power amplifiers, impedance matching.

Feedback Amplifiers. RC and LC Oscillators, Blocking Oscillators.

Characteristics, limitations and applications of OP-AMPS. Internal structure of OP-AMPs.

Special purpose amplifiers (Instrumentation Amplifiers, Logarithmic Amplifiers, Current Conveyors-Current Sources[Current Mirror, Symmetrical Widlar, Widlar, Wilson, Improved Wilson]).

Special purpose ICs: Analog multipliers. Voltage regulators, Timers, VCO, PLL and function generators. Analog switches and multiplexers.

Practical:

As per above syllabus

Text Book:

Microelectronic Circuit Design by Richar C. Jaeger, 1997;

Reference Books:

Microelectronic Circuits, by Millman & Grabel, McGraw Hills, 1988;

Microelectronic Circuit Design by Sedra Smith, McGraw Hills, 2009;

Microelectronic Circuit Design by Rashid, CENGAGE Learning, 2009;

[1] This content is available online at <http://cnx.org/content/m34862/1.1/>.

Chapter 2

Solid State Physics & Devices _The harbinger of third wave of civilization_PREFACE_Unfolding of Third Information Revolution.[1]

ROAD MAP OF COMPUTER DEVELOPMENT

[Computer age- Communication fuelled Universal Empowerment]

Key words: Telegraphy, Vacuum Tube, Transistors, integrated Circuit Technology, Computer;

Summary: In the first part the lecture gives the background of Third Information Revolution. Then it describes the unfolding of Third Information Revolution. It traces the development in Electronics in general and in Computer Engineering in particular from 1833AD to date. It gives the development of SuperComputers till date. It gives the source of digital data and total data generated per annum. It gives a Table on World Wide Internet Users. Table 1 gives the evolution of μP chips, Table 2 gives the evolution of different generations of computers, Table 3 gives the evolution of Local Area Network, Table 4 gives the data on Submarine and land cables laid till now. It also gives a special note on Hard 350 Disc Drive introduced in IBM 305 Ramac Computers supplanting the magnetic tapes.

[**Science &technology year by year** –Marshall Publication,London,2001]

Gutenburg Revolution, the Second Information Revolution , gave rise to the rotating type Printing Press. "Printing Liberated people's mind by enabling the widespread dissemination of knowledge and opinion. But it remained subject to censorship and worse. Television shrank the planets into Marshall Mclean's "global village" but the representation it diffused were tightly controlled by editors, corporations, advertisers and governments."

The net in contrast provides the first totally unrestricted , totally uncensored communication system-ever. It is a living embodiment of an open market in ideas. Its patron saint (if that is not a blasphemous though for such a secular hero) is Thomas Paine, the great 18 th century libertarian who advanced the remarkable idea (remarkable for the time, anyway)that everyone had a right to speak his mind and the even more notion that they had a right to be heard."

Precisely because of this "Net is potentially more powerful than both printing and TV because Net harnesses the intellectual leverage which printing gave to the man-kind without being hobbled by the one to many broadcast television."

BC700- *The First Information Revolution* - Invention of the Phoenicians Alphabets, the mother of all European languages.

BC 400 –Invention of Brahmilipi , the mother of all Indian language except Urdu.

[1] This content is available online at <http://cnx.org/content/m29929/1.4/>.

100 AD –Invention of Kharosti language and alphabets, the mother of all Arabic languages including Urdu

1450AD –*The Second Information revolution* – Invention of rotating press by a German Mechanic named Gutenburg.

1833AD – Michael Faraday made the earliest study of semiconductors.

1834AD –Charles Babbage plans a machine to calculate and print results.

1842AD –Ada Lovelace writes a step by step Programme for Babbage's Machine.

1850AD –George Boole invented **Boolean Algebra.** Boolean Algebra is the basis of the present set of Computer Systems which use **ALGORITHMIC PROGRAMMING** as opposed to **HEURISTIC PROGAMMING** of Artificial Intillegence Computers. Heuristics programming uses **Predicate Logic.** Heuristics means working by rule of thumbs and it is self learning programme. In contrast Algorithm means a set of sequential steps which are repeated or iterated. Here there is no self learning involved.

1851AD-First successful commercial telegraph cable laid from England to France. The cable had a central core of copper wire, gutta-percha, tarred yarn, tarred hemp, and iron wires.

1858AD-First transatlantic telegraph cable.

1876AD – Alexander Graham Bell invented Telephone.

1895AD –J.J Thomson discovers electron as the basic building block of Atom through the study of Cathode Ray;

1902-1906AD- Telegraph cable crosses the Pacific ocean.

1904AD-John Ambrose Fleming invents Vacuum Tube Diode(two electrodes device).

1906AD-Lee De Forest invented Vacuum Triode (three electrodes device) and used it to achieve RC coupled Amplifier. Subsequently four electrodes device tetrode and five electrodes device pentode.

1911AD-Using Heaviside "Distortion-less Transmission Condition" i.e. loading the Telephone cables with large inductors, first long distance telephone call was made from New York to Denver, Colorado, over a distance of 2000 miles.

1913AD-Vacuum Tube Repeater introduced in Public Service Telephone Network (PSTN).

1915AD-Using inductor loading & R.C Coupled Amplifier, first transcontinental telephone call is made from New York to San Francisco across a distance of 4000miles. Telephone becomes a Public Utility Service.

1918AD-Two Frenchmen, Block & Abraham, build the first simple Calculator-a calculator with programme storage and data storage facility is a computer.

1937AD-Alan Turing invents "The Turing Machine "- it can perform all logical tasks.

1943AD- To decipher encrypted messages, British Scientist build "Colossus"- forerunners of Electronic Computers.

1945AD-IBM builds first full scale calculator, MARK-I.

1945AD-ENIAC (Electronic Numerical Integrator & Calculator) build by Moore School of Electrical Engineering at the University of Pennsylvania. ENIAC is 27Metric Tonnes , consumes 200kW and occupies a large room. The valves failed at a rate of one every 10 minutes and ENIAC had 18,000 valves. So development of user friendly home Computers was a pipe dream at that time. Development could not take place using Thermoionic Valves.

1945AD- Microwave Telephone link established.

1945AD-First Transoceanic Telephone Links established using voice quality coaxial cables. Telegraphic Cables are not suitable for Telephone Conservation. Voice quality cables were developed during World War II and introduced right after the War .Before the World War II , no TransAtlantic or TransPacific Telephonic Links were there. Across the oceans only Radio-Telephone call could be made.

1947AD-At Bell Laboratories, John Bardeen, Walter Brattain & William Shockley

invented BJT (Bipolar Junction Transistor). They were awarded Nobel Prize in 1956 in Physics for this invention.

1948AD-Magnetic Drum Memory invented at Georgia Institute of Technology for Computers.

1952AD-UNIVAC I (Universal Automatic Computer)- First computer designed for business use. The inventors were John Mauchy & John Eckart.

7.26 Metric Tonnes, 5000 Vacuum tubes & 1000 calculations per second. These are termed **FIRST GENERATION COMPUTERS**.

1955AD-Semi Automatic Ground Environment (SAGE) installed. This takes in data received by the RADAR network and computes interception trajectories and steers the defenders within 1000yards of the attacker.

1956AD-UNIVAC II using transistors come in the market. Manufactures are Sperry Rand, USA. These are termed as **SECOND GENRATION COMPUTERS**.

1956AD-TAT-1, the first transatlantic voice grade telephony coaxial cable laid across the Atlantic Ocean.Until then transatlantic telephone calls were made by Radio-Telephony.(Coaxial Cable, polythene insulation, vacuum tube repeaters).

1956AD- September 13, 1956, IBM 305 Ramac Computer with DISK DRIVE was introduced. Till then the OS and data were stored on Magnetic Drums or Magnetic Tapes as a result the booting process of the computer or access of data was very slow. This newly introduced computer had 350 Disk File. This consisted of a rack of 24" magnetically coated platters 50 in number mounted on a single vertical spindle and could store 4.4MB of data as compared to today's hard disc which store 70GB of data.[Please see the foot note].

1959AD-Integrated Circuit (IC) chip invented by Jack Kilby (Texas Instrument) and Robert Noyce (FairChild). Discrete active and passive devices are integrated together on one wafer thin silicon chip in the area of 1cm by 1cm square, mounted on a header and then properly encapsulated and sealed. At the time it started, it had only 30 components in the 1 square cm area. This heralded the Information Age and **THIRD Information Revolution**. It also produced an

Explosion in electronic consumer and communication applications such as Personal Computers to cell Phones. Jack Kilby was awarded the Nobel Prize in physics in the year 2000. Jack Kilby passed away on 1st August 2005. Robert Noyce went on to establish " INTEL" (Integrated Electronics) along with Gordon Moore and Andy Grove . He passed away earlier than Jack Kilby so he could not be awarded. Noble Prizes are not awarded posthumously.

5th October,1959-IBM1401 mainframe computer makes its debut. This becomes the best selling computer in the world in mid-1960s.This was in the category of stored program computers. These stored program computers were vastly superior to IBM 604 Electronic Calculating Punch Machine which was vacuum tube, plugboard-controlled, serial-decimal machine with 50 digits of storage.Stored Program Computers were more flexible and adaptable than plugboard-based accounting machines. But these large-scale stored program computers were too expensive for common use.By the use of alloyed junction discrete transistor logic and Automatic Logic Design software, the volume and power consumption was reduced by 50% and 95% respectively.Standard Modular System(SMS) called Cube/Rolygon for electronic packaging was used. Saturating Complementary Transistor Diode Logic(CTDL)Family was used. This could clock at a maximum rate of 250kHz.CTDL was robust and handled large fan-ins and fan-outs.Memory to Memory architecture was used.This reduced the number of instructions needed for accounting and business programming.These changes achieved a entry-level rental price target of US$2500 per month.Previously it was as high as US$40,000 per month. It had outstanding print quality, powerful magnetic tape subsystem and a stored program computer for the mass market place.By 1965, half of the approximately 26000 computers in the World were 1400-family machines.Tape-oriented 1401 system became the computer of choice. Time-life transferred 40 million punched card subscriber records to just several hundred magnetic tapes.Full size system had 500,000 discrete components, weighed up to 4 tonnes, and consumed up to 13000W.It used 10,600 Ge alloy-junction transistors and 13,200 Ge point-contact diodes on 2300SMS cards interconnected with 5.5mi of wire. Memory varied from 1400 bytes to 16000 bytes memory space.It had a clock rate of

87000cycles/sec corresponding to one clock cycle of 11.7microsecond. In 50 machine cycles corresponding to 0.5ms two positive 20-digit numbers could be added. Today a Pentium IV processor operating at 4GHz can add two 64-bit numbers in 0.5nano second.Magnetic Core Memories were priced at 60 cents per bit(or US$24 per byte in today's currency. This is 300 million times more costly than today's DRAM.Its high speed and enduring print quality made it an Industry Workhorse. By 1961, optical character recognition (OCR) devices were introduced as a peripheral to 1401. The 1401 contributed to the growth of programming as a profession and software as an industry.It had no operating system. IBM had a compatibility problem amongst its various versions and amongst its various peripherals. By April 1964 it introduced System/360. It consolidated software, peripherals and support in one compatible and scalable computer family. 1401 wound down with the announcement of S/360.[This part has been excerpted from"The Legendary IBM 1401 Data Processing System" by Robert Garner Fredrick(Rick) Dill, IEEE Solid-State Circuits Magazine, pp.28-39]

1960AD-PDP I (Programmed Data Processor).This was introduced by Digital Equipment (DEC).DEC was founded by Kenneth Olsen & Harlen Anderson .These were also made of transistor. These were used as Office Computers. They were of cabinet size. Control Panel and the Key Board sat on the desk. It cost $ 120,000.00. This was way too expensive for most customers and for most application. This started the era of Mini-Computer.

1960AD-Man-Computer Symbiosis was published by J.C. Licklider, an experimental psychologist. This article stated that rote algorithm for computers & creative heuristics for Humans put together could be far more powerful than either could be separately.

1960AD-Sir Arthur's Clark's dream of Global Satellite Communication is realized.

1961AD-FIRST RLT (Resistance Transistor logic) IC Chip is commercially marketed by T I (Texas Instrument) and FairChild.

1964AD-Semi-Automatic Business- Related Environment (SIBRE) is created by the introduction of Nation-Wide Ticketing System like our Nation-Wide Computerized Reservation System today in 2005 in Indian Railways.

1964AD-FIRST Analog IC Amp. Chip MC 1530 marketed by Motorola. Op. Amp. Stands for Operational Amplifier which were in yesteryears used in Analog Computers for different Mathematical Operations and hence the name Op. Amp.

1964AD-PDP 8, table top computer introduced in the market .It was a 8-bit computer meaning by the address size is 8 bit. Larger is the address word, larger is the address capability. 4-bit means 16 locations can be addressed and 8-bit means 256 locations can be addressed. This used IC Chips hence it was compact and less power consuming. This was **THE THIRD GENERATION COMPUTER.**

Price $18,000.00, 125 kg, and 4kBytes memory.

1965AD- Project MAC, started by Licklider at MIT, evolved into first On-Line Community, complete with bulletin boards, e-mails , virtual friendship and a "free ware" exchange.

1968AD- MODEMS are used for Wide Area Network (WAN).

1968AD- December1968, demonstration at Fall Joint Computer Conference in San Francisco established Graphical User Interface(GUI) with mouse, on screen windows, full screen word processing and a host of other innovations.

1968AD-18th July, INTEL (Integrated Electronics) was established by Robert Noyce and Gordon Moore . Later this team was joined by Andy Grove.

1970AD-Advance Research Program Agency (ARPA) established ARPANET, the first WAN, connecting Stanford Research Institute, University of Utah, University of California Los Angels and University of California Santa Barbara mainly for Defence research purposes. In three years it grew to cover whole USA.

1970AD- PDP-11 introduced with 16 address word

1970AD-Magnetic Disks replace Magnetic Drum as back up memory. These are called Floppies (8" or 20cm) or Diskettes(3.5"or 9cm).Memory capacity is 1.44MB.

1971AD- FIRST INTEL MICROPRPCESSOR CHIP (μP 4004) introduced in the market . It can handle 4-bit data word and 8-bit address word meaning by it can address 256 locations. This 1 chip combined the function of 12 subsystems of a CPU(Central Processor Unit). This one silicon chip (1cm×1cm)had 2300 transistor , system clock rate 108kHz, Cost $299.00 . In India it was available for Rs.7500.00.

[A development contract from a Japanese Company , for a set of chips needed to power an electronic calculator , triggered off what became the world's **first computer-on-a-chip: the Microprocessor.** 35 years ago, INTEL, a small Santa Clara (US) based manufacturer of memory and switching devices, unveiled a thumbnail-sized slab of silicon encased in a ceramic casing with 16 pins: this ushered in the era of Personal Computers, the era of Desk Top Computing and the era of **FOURTH GENERATION COMPUTERS.**

The contract with Busicom required INTEL to deliver the electronics for calculating machine, as a set of 12 custom built chips. The electrical engineer assigned to handle the task-Dr. Marcian "TED" Hoff , a PhD from the Stanford university-had an inspired thought. Why make a set of chips just for one application? Why not generalize the design so that other computing tools could be built with the same generalized design?

In the process ,Dr. Hoff also suggested that the composite elements of a computer , as it was then understood- a unit to do the arithmetic (ALU-Arithmetic-Logic-Unit), a small memory and input and output interface –could be combined in a single slap of silicon..

When Busicom had cash flow problems, INTEL bought back the design it had created and slipped the product into its own catalogue.

Intel μP 4004 was sold to Defence Establishment in India at a cost of Rs 7,000.00. Intel's Indian Agent was Hyderabad based Electronics International which was later named as Microelectronics International]

1971AD-Texas Instruments marketed first pocket calculator 1kg in weight and price $150.00. It was too bulky.

1971-Electronic Mail or e-mail is invented by Ray Tomilinson.

- @ is introduced by Tomilinson to separate the User Name from domain name.
- Tomilison combined the existing mail program 'SENDMSG' that worked only within an organization with a file transfer program called 'CPYNET' to create an e-mail public utility between 15 computers within the organization and use the same on the existing ARPANET.
- The first e-mail; was "QWERTYUIOP", the second row of the typewriter keyboard, sent by Tomilison.
- The first telegraphic message was sent by Samuel Morse in 1844. It was "What hath God wrought".
- The first conversation carried out between Alexander Graham Bell and his assistant Watson in 1876 was, "Mr. Watson comes here. I want you.".
- Founder of Hotmail got the idea of accessing email via the web from a computer anywhere in the world. When Sabeer Bahtia came up with the business plan for the mail service , he tried all kinds of names ending in 'mail' and finally settled for Hotmail as it included the letters "html'(hyper text mark up language), the programming language used to write web pages .It was finally referred to as HoTMaiL with selective upper casings.

1972AD-first 8 bit μP 8008 introduced by intel.

1973AD-May 22, ETHERNET IEEE 802.3standards for LOCAL AREA NETWORK were born. The inventor of Ethernet was a young Xerox Palo Alto Research Scientist named Robert M. Metcalfe.

1974AD-8080μP chip introduced.

1974AD- First paper on TCP (Transmission Control Protocol)and the architecture of the Internet by Vinton Cerf and Kahn.

1975AD-Altair 8800(mini-computer architecture) based on Intel μP Chip 8080 (8 bit data & 16 bit address word) introduced in the market. $397.00 worth kit

available.

1976AD-APPLE CO. founded by Steve Wozniak & Steve Tabs members of Home-Brew Computer Club (California) in a Garage. Apple I was introduced.

1976AD-Cray 1 designed by Seymour Grey. This was a class apart called Super Computer. It cost $8.8million. It could achieve 240MFLOPS (Floating Point Operations per second)

1977AD-Taito (Japanese Software Company) introduced a video game "SPACE INVADERS" which takes the world by storm. The first video game was introduced in 1970's by ATARI. It was a ping-pong game.

1977AD-First Personal Computer was introduced, named APPLE II , at a price of $1300.00 .It had 4kB RAM. It had a software VisiCalc the best spread sheet package of its day. This was formally the **FOURTH GENERATION COMPUTER.**

1977AD-Bill Gates, Harvard Under-Graduate dropout, and Paul Allen developed the programming language BASIC for Altair 8800 and in the process founded MICROSOFT Company at Albuquerque near MIT. The name was coined by Bill Gates to represent the company that was devoted to MICROcomputer SOFTware. MS provided DOS (disc operating system) to IBM and other PC makers.

1978AD-Intel introduces 8086 μP Chip which had 16bit data word and 16bit address word.

1978AD-HCL delivered 8CR μP based Desk Top computer.
Indigenous OS;
Indigenous BASIC Interpreter Languages.

1979AD___On July 1, 1979, Sony launched Walkman which played a magnetic tape popularly known as cassette but there was no provision for recording. While walking or moving, you could play a cassette and listen to it. It became so popular that within next two months , thirty thousand pieces were sold. To this date on 27.10.2010 altogether 385 million pieces have been sold. The production by Sony has been stopped as Apple-iPod has out sold Walkman. Apple-iPod has solid state memories and digital signal processing. Only the final stage where the music has to be played is an analog voltage amplifier. All these combined makes Apple-iPod much more handy, economical and much more diverse interms of variety of music which can be played. Hence Apple-iPod has caught the fancy of young people.

1980AD-Voice to text system was developed by IBM.

1981AD-IBM introduced its own brand of Personal Computer PC5150 based on 8088μP Intel Chip. Clock Rate was the same as that of APPLE II but memory was much bigger at 40kB. GREEN SCREEN, 2x5" Floppy Drives for loading OS. IBM PC design accounts for 90% PCs. APPLE PC design accounts for 10% PCs.

1982AD-France Telecom launches MINITEL system, a wide area network in which you can login to a central data base from any where in the country and pertinent information can be availed. This is first Public Utility On-Line Service.

1982AD-Intel introduces 80826μp Chip (16 bit data bus and 24 bit address bus and 68 pin package).

1983AD-MOUSE introduced in LISA, an Apple machine. It had a user friendly graphical user interface (GUI). Its patent was bought from Xerox research center where it was used in Xerox Star. Screen icons were introduced which could be selected by the use of cursor using a mouse.

1983AD-CD_ROM (COMPACT DISC_READ ONLY MEMORY) introduced. It has 700MB as opposed as 1.44MB in floppies. This can accommodate one hour of music .

1983AD: TCP/IP, standardized in 1978, rolls out formally 1 January 1983 and all ARPA-sponsored packet networks (ARPANET, Packet Radio Net, Packet Satellite Net) and, subsequently ethernets that are becoming commercially available, incorporate the standardized version of TCP/IP.

1984AD-APPLE MACINTOSH is introduced. It is a complete stand alone system with the latest GUI, namely mouse and screen icons. Its cost was $2500.00.

1984AD-Musical instruments digital interface (MIDI) introduced.

1985AD-Desktop publishing introduced by ALDUS PAGE MAKER along with LASER JET PRINTER in Apple Macintosh.

1986AD-80386(Intel) and 68030(Motorola) introduces 24 bit address bus.

1988AD-VIRTUAL REALITY (VR) is introduced. When VR headset is put on , you see a world of your choice with the help of computer. You can place yourself in the cockpit of a jet plane and experience the sensation of actual flight.

1988AD-Pattern Recognition Software introduced to read hand written documents by computer .

1988AD-MPEG (Moving Picture Expert Group) is devised for compressing digital videos Band Width.

1988AD-First Trans Atlantic Optical Fiber Cable, TAT8, used in place of coaxial cable.

Coaxial Cable can carry 3,000 simultaneous phone calls. In contrast Optical Fiber cable can carry 37,500 simultaneous telephone calls with the present state of art of electronics. As the switching speed increases, the number of simultaneous calls increases exponentially. Total BW: 5.12terabits/sec.

1988AD-Touch Screen Computers are developed.

1989AD-Disk Operating System (DOS) are replaced by MS WINDOW OS., MS EXCEL and MS WORD introduced. WINDOW 3.0 VERSION released.

1989AD- March 1989, computer software child prodigy, now an adult, Mr. Tim Berners-Lee of CERN, Geneva, handed a proposal 'Information Management: a proposal'. They came up with global hypertext language, the basis of "http" in website address. By October 1990, they developed the first web browser. The World Wide Web Technology was made available for wider use on INTERNET from 1991 onward without any royalties. "Internet is a vast network of networks, interconnected in many different ways yet they all speak the same language. Web is one-albeit the most influential and well known-of many different applications which run over the Internet". Today in 2009 March, as we celebrate 20^{th} Anniversary of Web Technology, Tim Berners-Lee is a researcher at MIT,US, and a Professor at Computer Science Department at South Hampton University, Britain, and still heads the World Wide Web Consortium that coordinates development of the Web.

1991AD-ARPANET was confined to exclusive clientele (DOD sponsored research). To make the NET available to University Community at large, NSF(National Science Foundation) connected his own NSFNET to ARPANET . This led to exponential growth in the use of NET. In mid-90's the collection of networks was looked at as INTERNET.

1991AD-Until 1991, internet was largely populated by academic, government and industrial researchers. Tim Bernes Lee developed Hyper Text Mark Up Language (HTML) for easy file transfer and from here he was able to build up World Wide Web (WWW). HTML is the lingua franca of WEB pages. This made Internet useful for the whole populations – academic and non academic both.

1992AD-Mobile Phones enter Digital Age. These are second generation (2G) mobiles.

1993 AD-PENTIUM I introduced . it had 3.1×10^6 CMOS(Complementary Metal Oxide Semiconductor Field Effect Transistor) placed on one chip .

- it could perform 90MFLOPS, 5 IMES THE SPEED OF 80486.
- data bus 32 bits and address bus 32 bits
- clock rate 1500 times that of 4004 .

1995AD-WINDOW 95 was introduced .**1996AD**-Multi-media Extension Pentium Chips (MMX) Chips launched. It had $5.5x10^6$
transistors (CMOS). It can perform 300MFLOPS and speed up multi media processes.

1998AD-APPLE launches iMAC fully internet compatible.

1998AD-Global Positioning System (GPS) introduced by US Defence.

1999AD-IBM's DEEP BLUE defeats Garry Kasporov (chess grand master). 200 million different chess positions are examined per second.

1999AD-DVD(Digital Versatile Device)introduced with a memory space of 8 GB as compared to 700MB in CD. DVD became a reality only after the invention of Blue Laser Diode .

1999AD-HDTV(High Definition TV) introduced.

1999AD-WEB CAM (WEB camera). Digital Camera connected to your computer. It has a special drive which allows a picture to be taken every 10 seconds, turns this into a standard file format and uploads to the server where your website is stored . People can keep visiting the site and have a look at the photographs of the location as desired.

- Handheld Internet Access introduced;
- Hand held Personal Organizer introduced;
- MP3 standard is introduced for Digital Audio Compression.

2000AD- Blue Tooth Technology introduced . This Wireless Technology allows computers, phone hand sets and CD players to communicate and share data over a distance of 10m and less. Operating frequency 2.45GHz. Switches the operating frequency 1600 times per second . This is called Frequency Hopping Spread Spectrum method. When Blue Tooth capable devices come within range of one another they have electronic conversations.

2001AD-Pentium IV chip introduced;

- Nano-electronics chip;
- It has 42 million transistors packed in an area of 1 cm by 1 cm;
- System Clock Rate is 2GHz;
- 20,000 more powerful than 4004 μP Chip;
- Cost Rs 15,000.00

2001AD- 23rd October 2001, Apple iPod, the iconic device that defines our era as distinctively as the Sony Walkman defined 1980s. An entire ecosystem of goods and services have evolved around Apple iPod. Minispeakers can be plugged into it; microphones attachment can convert it into digital audio recorder; it can be turned into small radio transmitters that beam songs to the nearest FM radio; attachments can turn it into breadth analyzer. iPod plus iTunes turned out to be a grand success where other musical gadgets and soft-wares failed.

2003AD-APPLE introduces Power Mac G5 PC.

- 64 bit data word and 64 bit address word;
- 18 PETA Memory locations can be addressed;
- System Bus operates at 800 MHz;
- System Clock operates at 2GHz, dual processors;
- 80 to 160GB hard disc;
- 256MB to 512MB high speed RAM;

2004AD-Internet Protocol Version 6 (IPv6) introduced. Till now we have been using IPv4;

- Address field is only 32 bit long in IPv4 but 128bits long in IPv6. This will

allow much larger number of users than what it can support till now;

- New version allows a larger through-put;
- New version offers a better support for options;
- New version provides better methods of authentication and privacy. This will

provide a much better protections against Hackers;

2004AD- " Project Columbia" a $50 million super-computer built by SILICON GRAPHICS is introduced;

- it is powered by 10,240 processors in 20 units;
- it is Intel Itanium chips;
- it performs 43 Tera FLOPS as compared to the world record of 36TFLOPS

performed by IBM's BlueGene/L super computer;

- This is a ten fold increase in NASA's supercomputing capacity;
- Applications in hurricane tracking, weather modeling and earth's interior

imaging;

2004AD-Norton Internet Security 2005 is introduced for Rs 3,618.00. It offers Norton Anti-Virus, Norton Anti-Spam and Norton Personal Firewall. Firewall protects the system from Trojan Horses and other attackers. It also includes parental and privacy controls;

2004AD- Radio frequency Identification (RFID). It is a stamp size chip which gives a Radio Signal as the tag mark of the product it is attached to;

2005AD- GeForce 7800 GTX (latest Graphics Processing Unit or GPU) introduced by US-based nVIDIA Corporation for Video Games;

- 302 million CMOS on one 1cmx1cm chip;
- Performs 202 GFLOPS;
- 10% less power consumption ;
- 50% quieter
- twice as powerful as its processors 6800 but it costs the same as before that is

Rs. 32,000.00 ;

- Market for video games is one of the fastest growing sectors in Computer

Industry;

2005AD-Dual cores Microprocessor chip are introduced;
Intel introduces Pentium "Extreme Edition" 840 with Clock Rate=3.2GHz and with billon transistors . This is dual core as well as it has a software called 'hyperthreading'(HT). This is a software which enables one to work with double virtual processors. Thus a dual core with HT will allow application developers to write software that can carve up the task between four processors;

- Intel introduces Xeon for servers and Pentium M for laptops;
- AMD introduces Opteron 800 series for servers and workstations;
- AMD introduces Athlon 64 X2 for consumers and business PC's;

2008 October. GeForce 9400M is a single chip solution for graphical processing platform for portable applications. It has computing rate of 55GFlops (Floating Point Operations), the most powerful integrated graphics processor in the market in 2008. It has 6 cores operating in parallel. But much less power hungry. New MacBook family will be fuelled by these chips.

2008 November. Intel and AMD have launched a native quad processor unlike the earlier version where 2 dual core chips had been combined in the same package. Intel has launched 'Nehalem',the i7 processor using 45nm technology. AMD has launched 45nmOpteron. Both achieve the 4 cores on the same silicon slab. This has Memory Bandwidth. These conserve energy by cutting down power when the device is idle.

2009 May- Interplanetary Internet Protocols are tested by using computers on the International Space Station. Eventually there will be an internet connectivity among Earth, multiple probes, rovers, orbiters and space crafts exploring the solar system. This will be the basis of Interplanetary Internet. The network's key technologies are called Delay Tolerant Networking(DTN) protocols. The problem in deep space internet is the huge delay and occultation of the nodes. To overcome this problem "store and forward" technique will be used. The node will save the data and then passes on when the link is again established. A third test is yet to be carried. In this a security protocol and a new file-transfer protocol will be used.

2010AD-Pacific Unity will lay multiple fibers. Total capacity; 7.68 terabits per second.

ROAD MAP OF SUPERCOMPUTER.['The Data', IEEE SPECTRUM, APRIL 2009]

1976 Illiac IV, 64 processors, teraflops capability, cost was 4.8×10^{-7}TeraFlops per million dollars or 4.8×10^{5}Floating Point Operations per Second which is 480×10^{3}FLOPS or 480kFLOPS per million dollars.

1976 CRAY-1, 1 processor with teraflops capability, cost was 1.778×10^{-5}TeraFlops per million dollars or 17.78MFLOPS per million dollars.

1988 CRAY Y-MP, 8-vector processors with teraflops capability, cost was 1.115×10^{-4} TeraFlops per million dollars that is 111.5MFLOPS per million dollars.

1997 ASCI RED, 4510 processors with teraflops capaability, cost was 1.818182×10^{-2} TeraFlops per million dollars which comes to 18.18182GFLOPS per million dollars.

2002 EARTHSIMULATOR , 5120 processors, cost was 17.5GFLOPS per million dollars.

2004 BLUEGENE/L, 65536 processors with 10TFLOPS capability, cost was 2.8TFLOPS per million dollars.

2007 PLAYSTATION3 CLUSTER, 8playstation 3s, 375TFLOPS per million dollars†.

2008 NVIDIA TESLA, 960 cores, 439.1 TFLOPS per million dollars*.

2008 ROADRUNNER, 19440 processors with several tens of TFLOPS capability, cost was 8.3TFLOPS per million dollars‡.

*Based on the cost of building your own Tesla supercomputer out of four Tesla C1060 units. Complete instructions are available at nvidia.com

† Seven processors per node at 150GFLPS per Unit for a single processor(11 processors per node for a dual processor). $400-plus per node.

‡ 6480 Opteron CPUs and 12960 Cell processors.

Supercomputers are massively parallel chips can be used to calculate protein folding, predict climate change and crack the encryption of hitherto-secure Web sites.

Nvidia advertises its new workstation, the Tesla, as a "personal supercomputer". It clusters 4 Nvidia C1060 processing boards, each of which unites 240 graphic cores to process instructions at nearly teraflop speed.

Tesla does single-precision floating-point calculations using 8-bit bytes.

Roadrunner uses 64-bit floating integers.

Digital Data Generation.

Sources of digital data:

a. social networking sites,
b. internet-enabled mobile phones and
c. government surveillance.
d. 70% of the digital content is created by by individuals through phne cals, emails, photos, online banking transactions or postings on social networking sites.

Digital Universe Report in 2007 gave total digital content as 161 bn gigabytes.

Digital Universe Report in 2009 gave total digital content as 487 bn gigabytes.

IDC/EMC estimate:

The cost of the computers, networks and storage facilities that drive the digital universe is $6 tn.

Medical equipment, entertainment and content creation equipments cost another $6 tn.

Total World GDP is $50tn.

80% of PC's are powered by Intel Chips and remaining 20% powered by Motorola, Digital Co., AMD and Transmeta.

2006AD-We have reached 1 billion mark in personal Computers. 39% is accounted by USA, 25% is accounted by Europe and 12% by Asia.

PC user per hundred of the population- (USA 70%), (France 35%), (Brazil 7%), (China 3%), (India 15 per 1000);

2006AD-2 billion Cellular Phones- worldwide;

China- 450m cell phones; India-95m. cell phones

World Wide Internet Usage [www.internetworld-stats.com] Total User 1.3 billion

Countries	Total Number till March 2006	% penetration in the total population
India	30m	5.4
China	123m	9.3
Japan	86m	67.2
USA	207m	69.3

Table 2.1

To bridge the Digital Divide, Government of India is planning to set up Common Service Centers (CSC)- broad band enabled computer kiosks that will offer a range of government-to-citizen and business-to-customer services, besides providing sheer access to the Internet. About 100,000 plus CSC's will be introduced in 600,000 villages by March 2008.

Companies in PC manufacturing – WIPRO, PSI, ZENITH, DCM,HCL

-27% growth rate -5m. unit/yr

Table 1.Evolution of Microprocessor Chip

Name	Date & Address Size	Packing Density	Number of Pins	Clock Rate	Instructions Per Second	Year & Price.
Intel 4004	4-bit	2300PMOS	16	108kHz	?	1971 Rs 7,500.00
Intel 8080	8-bit	6000NMOS	40	2MHz	0.64MIPS	1977
Intel 8086	16-bit	29,000 HMOS	40	5 MHz	0.33MIPS	1978

continued on next page

Intel 80286	Data 16b Address 24b	134,000 HMOS	68	6-12.5 MHz	1 MIPS	1982
Intel 80386	32-bit	275,000 CMOS	132	16 MHZ	5 MIPS	1985
Intel 80486	32-bit	1.2million CMOS	168	25 MHZ	20 MIPS	1989
Pentium	Data 64b Address32bMemory Size 2^{32}=4GB	3.1 million CMOS	?	60 MHZ	100 MIPS	1993
Pentium II	Same	7.5 million CMOS	370	233 MHZ	400 MIPS	1997
Pentium III	same	9.5 CMOS	370	450 MHZ	1000 MIPS	1999
Pentium IV	Data 64b Address 64b	42 million CMOS(Nano electronics)	478	2.2 GHz	?	2001

Table 2.2

MOORE's LAW: The packing density of CMOS on μP Chip would double every two years leading to an exponential growth in the complexity and speed of μP Chip.

Table 2. Evolution of Computers.

Generation	Components	Architecture	Logic	Programming	Language
1st (1947-ENIAC 1952-Univac I, Main-Frame)	Vacuum Tubes	Von-neumann, sequential	Boolean	Algorithm	Fortran,Basic,Algol
2nd(1956-UNIVAC II, Main Frame	Discrete BJT				
3 rd(1964-PDP8,Mini-comp.,Table Top)	IC's chips				
4 th(1977-APPLE II, Micro-comp., Desk Top, Personal Comp.	μP chips				

continued on next page

5 thRobotics, Data Based Medical Diagnostic Tools	Artificial Intelligence Machines	Data-flow, Systolic, Pipeline	Predicate	Heuristic	Prolog, Lisp

Table 2.3

Table 3. Evolution of Local Area Network

Year	Standard	Name	Data transfer rate
1973	802.1	OSI (Open System Interconnection)	10Mbps
	802.2	Logical Link Control	10Mbps
1983	802.3	CSMA/CD (Carrier Sense Multiple Access/Collision Detect)	10Mbps
	802.4	Token Bus	100Mbps
	802.5	Token Ring	100Mbps
1999	802.11	WLL (Wire Local Loop)	1 Gbps
2001	802.13	Wi-Fi (Wireless internet Access	

Table 2.4

Table 4. Development in submarine cable.(Sources: Telegraphy Research: *"History of the Atlantic Cable and Undersea Communications"* **by Bill Glover,Wikipedia.**

Region	Submarine Cable %BW utilization	LIT Submarine Cable Capacity
Asia	69%	
Middle East	73%	
Oceania	56%	
Europe	52%	
US & Europe	51%	
Latin America & Caribbean	77%	
Africa	69%	
Transatlantic Cable		15%
US-Latin America		37%
Transpacific		21%
Europe-Asia		91%
Intra-Asia		31%

Table 2.5

Submarine Cable Boom: In 2001 US $13.5 billion was spent. Due to Dot.com bust, only $2billion was spent during four lean years from 2004 to 2007. Even the during the lean periods, global demand never slaked growing at an average compound annual rate of 54% from 2002 to 2008. In Latin America and the Caribbean, traffic grew the most at more than 75%.

METALFE LAW: The value of a NETWORK grows as the square of the number of users.

Foot Note: 350 Disk Drive, introduced in IBM 305 Ramac Computer, consisted of 50 Number of 24-inch magnetically coated platters mounted on a single vertical spindle and rotating at high speed. In between the platters and looking rather like a giant animated hair-comb, was an assembly of read-write heads that clacked in and out, reading and writing data from and to the disks and passing the information to and from the machine's processor.

The drive was the size of two large refrigerators and was leased to customers at an annual rental of $35,000/-, which according to my calculations would be $250,000 in today's currency.

But corporate customers thought it a bargain because it meant that their Main Frame Computers could become much more versatile and faster. A digital computer works by taking data from a permanent storage medium, carrying out operations on that data, and then writing back into storage.

Slowest part of this process was getting data transferred to and fro from the processor to the storage. Hard Disks offered a way of easing the bottleneck. The result was faster computation and faster data processing.

IBM's colossal spinning plate rack held a total of 4.4MB of Data.

Today the hard disk in the iPod is just 1.8" in diameter and yet it can store 60GB of Data, which is almost 14,000 times the capacity of the 350 Disk File. The drive in laptop is 2.5" in diameter and has a capacity of 120GB.

This cheap and boundless mass storage has enabled the existence of companies such as Google, Amazon and eBay and services such as Apples iTunes, Wikipedia and Internet Archive.

The story of computing has been told almost entirely in terms of advances in processors and networks. Whereas in fact the success and proliferation of computer usage is as much due to the vast, fast, cheap mass storage provided by Hard Disks.

Development in Memory Technology: The convergence of consumer,computer and communication electronic system is leading to exponential growth in need of memories. Memories are required for code storage, computing input-output storage and data storage. In the past, we could associate a memory technology to a specific market segment : RAM to computer; NOR Flash memory to mobile communication; NAND Flash memory to consumer DSC; Today such distinctions are being blurred.A common format is emerging. The new electronic systems stack different non-volatile memory and xRAM and use microprocessor for facilitating interfacing and managing the overall memory.

Evolution of Telephone Exchanges.

Manual	operator directs the call
Automatic Dialling: *Strowger-rotary switches(UAXs,SAXs,TXS) *Electromechanical crossbar(TXKs) *Electronic-control reed-relay switches(TXE2) *SPC non-digital(TXE4) *Digital(Systems X and Y- AXE10: may be further categorised as to whether they are ISDN -capable, I suppose;5ESS; DMS100;UXD5)	2 letter exchange-2 to 5 digit number; 3-3-4 system adopted(area code-exchange prefix-line number); The number system 3-3-4 first used in Wichita, Falls, Texas.

continued on next page

Global Telephone System	Service switching points, mobile switching points
SS7(Signaling System 7) links telephone networks all over the globe. Every Telecom carrier and manufacturer has to work and develop around SS7	Smart coordinator that helps callers find one another
VoIP(voice on internet protocol)	It is a telephone service on Data Network(no taxes hence cheap)
Futuristic Systems (21CN-21st Century Network)	System will know how and where to locate the destination; Convergence-lots of systems but few devices; preferred formats - Voice or Video, Real Time or dekayed, reading the voice mails and hearing the emails

Table 2.6

Chapter 3

The Journey of I.C.Technology from micro (1959) to nano (2009) era_ABSTRACT.[1]

The Journey of I.C.Technology from micro (1959) to nano (2009) era_ ABSTRACT.

Keyword: Monolithic Planar Technology, Wafer, epitaxial layer, fabrication, photolithography;

Summary: This is the abstract of the main article named as above.

ABSTRACT:

The discovery of ELECTRON by J.J. Thomson started a series of inventions which was to culminate into Solid State Bipolar Junction Transistor (invented by Shockley, Bardeen and Brattain) in the year 1948. This marked the advent of the era of *Solid State Technology*. Solid State Technology laid the foundation of *Silicon Monolithic Planar Integrated Circuit Technology* in 1959. In 1960 first high temperature epitaxial based BJT IC came into market. This kick started a process of *Information Revolution* leading to the third wave of civilization or post industrial civilization. By 1970 four- bit Microprocessor Chip uP4004 was introduced. The advancement of IC Technology led to exponential increase in packing density as well as in electrical performance. From 1971 to 2001, *Small Scale Integrated* Chips evolved to *Medium Scale Integrated* Chips to *Large Scale Integrated* Chips to *Very Large Scale Integrated* Chips to the present Pentium IV which is *Ultra Large Scale Integrated* Chips packing 42 million CMOS Chips. This increase in packing density was enabled by the advancement the lithography technique. In 1966 emulsion mask patterns were contact printed on 200mm wafer with the smallest feature size of 25μm. In 2007 using Deep Ultra Violet(DUV)193nm immersion Lithography, 30nm $\pm$6nm feature size are imprinted on 300mm wafer. We moved from Wet Processing to *Dry Processing*(reactive ion etching) or *Ion beam Processing* , Diffusion was replaced by *Ion Implantation*, Mask Making Techniques were improved and automated, preparation of master art work was automated using computer, step and repeat cameras were replaced by contact cameras, photolithography used ultra violet light for exposing the Kodak Photo Resist, UV light lithography was replaced by *Deep UV lithography* and now it is in process of being replaced by *Extreme UV laser beam lithography* as the feature size became smaller, Liquid Phase Epitaxy and Chemical Vapour Phase Epitaxy developed into *Metal Organic Vapour Phase Epitaxy*, new materials were introduced for interconnections (such as *silicides* and *copper*) and *Poly- Silicon* for gate contacts, the dielectric material used in gate silicon dioxide is being replaced by *hafnium oxide* which has a higher dielectric strength and higher k , planar technology is being replaced by *trigate* technology where gate contact is on the top as well as on the side walls of the oxide layer thereby increasing the contact area, parasitic were reduced by shallower junctions, smaller feature size and oxide side walls and by using insulator as the substrate for instance silicon on

[1] This content is available online at <http://cnx.org/content/m29930/1.1/>.

sapphire. One more innovation was *Lightly Doped Drain* for improving the reliability of the MOS devices. FET depends on leading edge lithographic dimensions(45nm) but BJT depends on vertical base widths which has reached 10nm. BJT has structural flexibilities in minimizing the parasitic. It has higher transconductance, high self gain, low 1/f flicker noise and better V_{BE} matching. All these factors make BJT the device of choice for demanding applications.While microlevel BJT scaled down to nano level structure, new problems arose due to shallow EB junction, band gap narrowing in emitter due to doping concentration exceeding above 10^{18} /cc and high sheet resistance of the base layer. These problems were tackled by using *heavily implanted PolySi layer used as emitter contact. SiGe Hetro Bipolar Transistors(HBT)* hold the key to realizing high speed wire-line and wireless communication circuits and systems. Marriage of Si Technology and Bandgap Engineering Methods of III-V Compund Semiconductor which is broadly called SiGe based bandgap engineering is Si Heterostructure Bipolar Technology (SiGe HBT). This was made possible by Low Temperature Epitaxy(LTE). Scaling strategy was used here also for exponential growth in the packing density and electrical performance of devices. To reduce the time delays, base width and collector widths have to be reduced and I_C must be increased which requires Kirk Effect should be pushed to higher Current Densities. This is achieved by increasing Collector Dopent Concentration. Hence *Selectively Implanted Collector* (SIC) is introduced. Decreasing the distance between SIC and extrinsic base implant will increase the overlap i.e. C_{CB}OL. This has to be minimized. This is achieved by *Raised Extrinsic Base* structure. An optimization in Ge profile in SiGe base layer has to be done inorder to get the full advantage of increased base doping in HBT. Today SiGe HBT are surpassing GaAs HBT. The integration of SiGe HBT with CMOS is BiCMOS. BiCMOS reduces the cost of mobile consumer products, advance high BW wireless communication and collision-avoidance automobile radar. BiCMOS lead to VLSI, ASIC & Si based RF SOC(System on Chip) solution. Hence SiGe/SiGeC and BiCMOS is becoming the technology of future. The strategy of *Sidewall oxidation* and *Silicon-on-Insulator*(SOI) is adopted for reducing the parasitic capacitances and improving the frequency response. P^+ isolation diffusion is replaced by trench isolation. *Shallow Trench Isolation*(STI) is achieved by Reactive Ion Etching(RIE). This considerably helps reduce the parasitic and helps improve the speed. Since 90-nm Technology generation was introduced, off-state leakage current and power density in CMOS have made scaling a difficult and challenging job. New scaling vectors were adopted to meet this challenge. The new scaling vector was *Mobility enhancement through strained Si* and novel structure like FINFET . At 45-nm Technology and beyond, new flow process adopted was *High k + Metal Gate using Gate-Last strategy*. In the future we hope to go from 45nm technology to 32nm technology to 22nm technology to 16nm technology. Today in Bipolar Technology we have achieved 200GHz transit frequency and in CMOS Technology quad core microprocessor has come in the market. Intel and AMD have launched a native quad processor using 45nm technology. Both achieve the 4 cores on the same silicon slab. This has Memory Bandwidth. These conserve energy by cutting down power when the device is idle. These four cores are built up of 40billion transistors.

Chapter 4

Analog Electronics_Lecture 1_Independent and Controlled Sources[1]

AnalogElectronics_LECTURE NO.1_Independent and Controlled sources.

Q.1) Define Independent and Controlled/Dependent sources.

Ans:-Those sources which do not depend upon the values of the current or the voltages in any other part of that circuit are called independent sources. Independent sources are two-terminal devices.

The source between two terminals which depends upon the value of either voltage or current at a third terminal of the given circuit or device are called dependent (or) controlled sources. These are 3-terminal devices such as Vacuum Tube Triode and Pentode, Bipolar Junction Transistor (BJT) and Field Effect Transistor (FET).

In triode , the voltage at GRID controls the dependent voltage source between Anode and Cathode.

In pentode , the voltage at GRID controls the dependent current source between Anode and Cathode.

In Common Emitter BJT, the base current in the BASE controls the dependent current source between Collector and Emitter in forward active region.

In Common Source FET, the voltage at the GATE controls the current source between Drain and Source in Pentode Region of the output characteristics or the output family of curves.

Q.2) Define independent voltage source and independent current source.

Any Power Source supplies voltage as well as current. Source resistance compared to the load resistance decides if the power source will be represented as voltage source or as current source.

Ans:-When source resistance is much less than the load resistance (that is less than 1/10 of the minimum load resistance likely to be connected) then we take the Thevenin Equivalent of the power source. This Thevenin equivalent is an Independent Voltage Source representation of the power source. The open circuit voltage V_{OC} at the output terminals is the Thevenin Equivalent Voltage, V_{Th} , and the equivalent resistance measured at the output terminals with power supply inactivated is Thevenin resistance R_{Th} . Here power supply inactivated means that if we have a voltage source we consider it to be short circuited and if we have a current source we consider it to be open.

[1]This content is available online at <http://cnx.org/content/m33375/1.1/>.

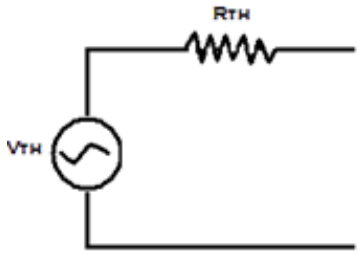


Figure 4.1

When source resistance is much greater than the load resistance (that is greater than 10 times of the maximum load resistance likely to be connected) then we take the Norton Equivalent of the power source. This Norton equivalent is an Independent Current Source representation of the power source. The short circuit current I_{SC} at the output terminals is the Norton equivalent current, I_N , and the equivalent resistance measured at the output terminals with power supply inactivated is Norton resistance R_N . Here power supply inactivated means that if we have a voltage source we consider it to be short circuited and if we have a current source we consider it to be open circuited. In actual practice it is dangerous to short the output terminals of a power source. It will lead to fuse blow up. Hence short circuit current can be determined only if we are sure that the internal impedance or the source impedance is very high.

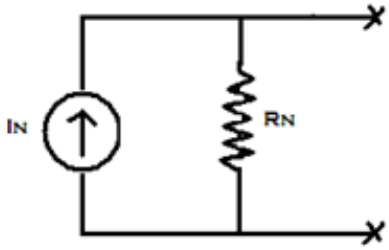


Figure 4.2

Q.3) Define Ideal Voltage and Ideal current sources.
Ans:- An ideal voltage source is constant voltage source which :

a) Has Zero internal impedance.
b) 0% Regulation i.e. it gives a constant terminal voltage irrespective of the load current.

An ideal current source is constant current source which:

a) Has Infinite internal impedance.
b) Gives constant terminal current irrespective of the load voltage.

Q.4) Give the I-V characteristics of Open Circuit and Short Circuit.

As shown in Figure 1, Open Circuit has Horizontal Line along X-axis as its I-V characteristics and Short Circuit has a Vertical Line along Y-axis as its I-V characteristics.

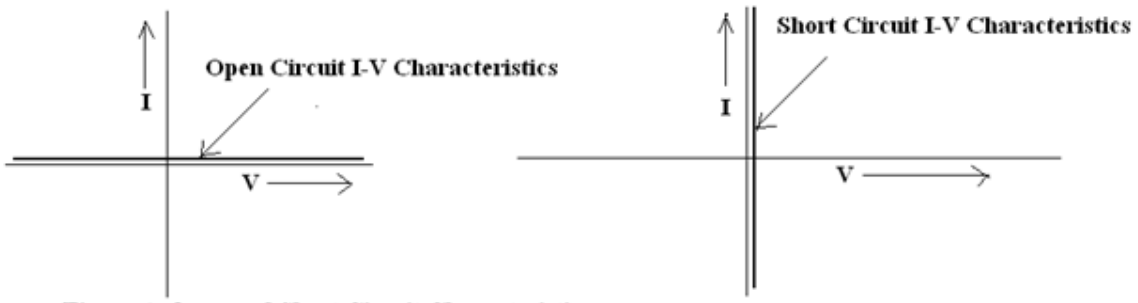


Figure 1. Open and Short Circuit Characteristics.

Figure 4.3

Q.5) Give the I-V characteristics of an Ideal Voltage Source and Ideal Current Source.

Figure 2 Ideal Voltage Source and Ideal Current Source I-V characteristics.

Figure 4.4

An ideal voltage source gives a constant terminal voltage V_{ideal} irrespective of the load current drawn out of it. I-V characteristics is vertical but shifted with respect to Y-axis . It is vertical because the source resistance is zero and hence slope is infinite.

An ideal current source supplies a constant source current I_{ideal} irrespective of the terminal voltage. I-V characteristics is horizontal but shifted with respect to X-axis. It is horizontal because the source resistance is infinite hence slope is zero.

Q.6) Give I-V characteristics of a Real Voltage Source and a Real Current Source.

Figure 3 Real Voltage Source and Real Current Source I-V characteristics.

Figure 4.5

In real life we can never have a vertical line for a voltage source. It will always have a slope = $1/R_{Th}$. Since sources with low R_{Th} are going to be represented as Voltage Source hence Voltage Sources will always be slightly positively inclined vertical line.

In real life we can never have a hoizontal line for a current source. It will always have a slope = $1/R_N$. Since sources with high R_N are going to be represented as Current Source hence Current Sources will always be slightly positively inclined horizontal line.

Q.7) Give the I-V characteristics of the active devices used in Electronics namely Diode, Triode, Pentode, BJT and FET.

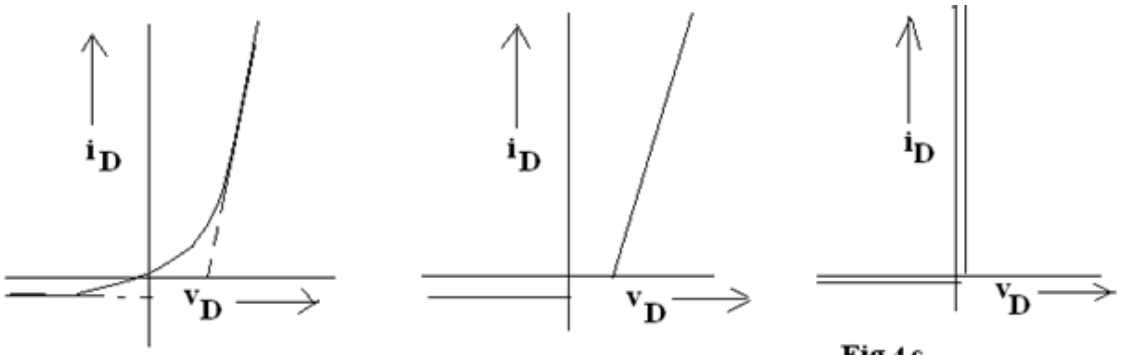


Fig.4a. Real I-V curve of a diode. **Fig.4b.** **Fig 4 c.**

Fig.4b. First level idealization of a diode.
Fig.4c. Second level idealization of a diode.

Figure 4.6

Figure 4 gives the I-V curve of a diode. Examining Figure 4c we clearly conclude that an ideal diode is a voltage controlled switch which is a short circuit under forward bias and an open circuit under reverse bias.

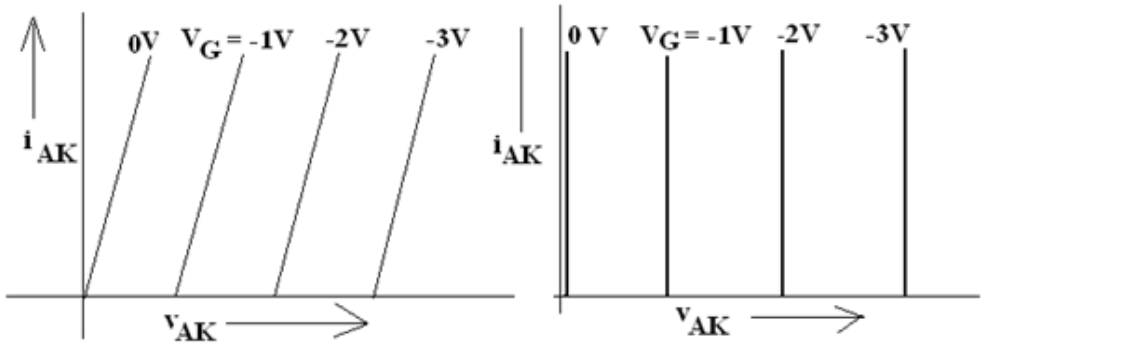


Figure 5a. I-V family of curves of TRIODE. **Figure 5b. Idealized family of curves of Triode**

Figure 4.7

Figure 5 gives the I-V family of curves for a real Triode and ideal Triode. Examining Figure 5b it is clear that Triode's family of curves is a family of constant voltage sources. Triode at a given time will behave as one of the constant voltage sources . The grid voltage V_G will decide which constant voltage source it corresponds. In order that real Triode behaves like a linear circuit element, the family of curves must be equally spaced and equally inclined. A linear Triode when used in an amplifier will give a sinusoidal output for a sinusoidal input. But a real Triode is far from linear. Hence a sine wave input will generate fundamental and harmonics. As the amplitude of input sine wave increases so will the percentage content of the harmonic waves in the output will also increase. Hence this Harmonic Distortion is called Amplitude Distortion. If the input is kept very small then there will be little or no harmonic distortion. How small is very small? In BJT this is less than 5mV and in FET it is less than 400mV. This permissible input voltage range for low level harmonic distortion is referred to as Dynamic Range.

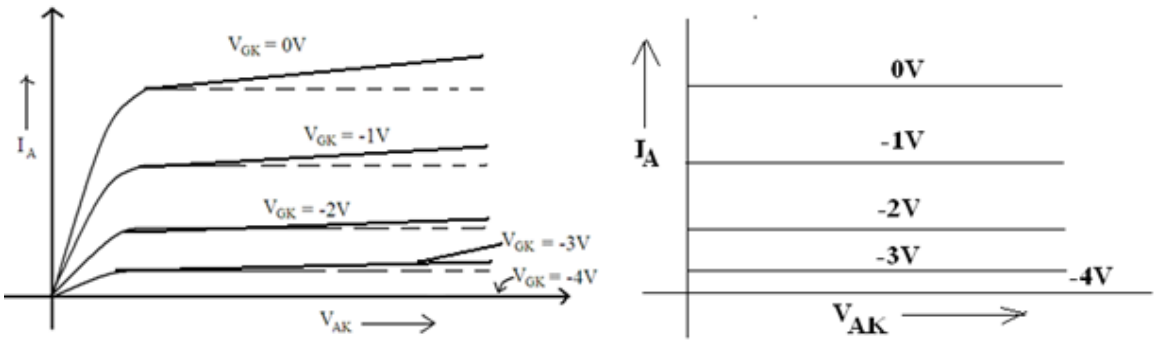


Figure 6a. I-V family of curves of a Pentode **Fig.6b.Idealized family of curves.**

Figure 4.8

Figure 6 gives the family of curves of a Pentode. By examining the idealized family of curves it is evident that Pentode output is a family of Constant Current Sources controlled by Grid Voltage. In order that Pentode behaves like a linear circuit element the family of curves must be equally spaced and equally inclined but this is not the case. Only under very small signal condition or under incremental condition it will behave like a linear element.

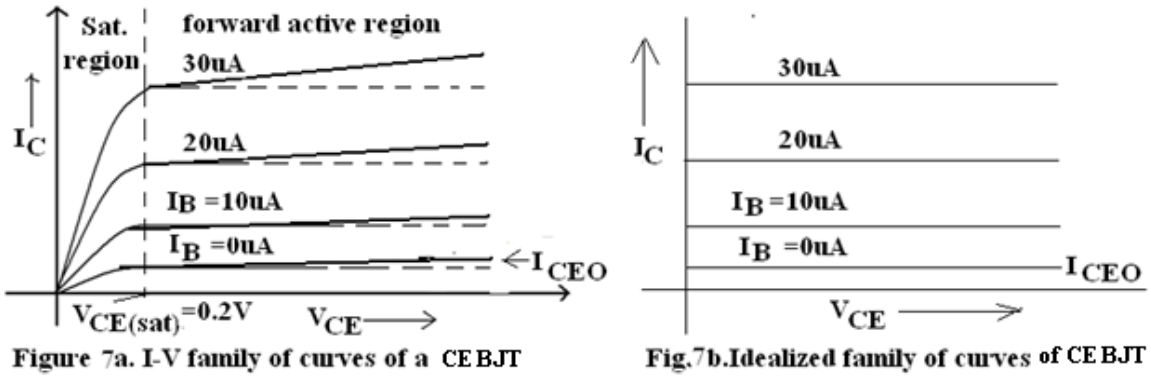


Figure 7a. I-V family of curves of a CE BJT

Fig.7b.Idealized family of curves of CE BJT

Figure 4.9

Figure 7 gives the family of curves of a Common Emitter Bipolar Junction Transistor (CE BJT). By examining the idealized family of curves it is evident that CE BJT output is a family of Constant Current Sources controlled by Base Current. In order that CE BJT behaves like a linear circuit element the family of curves must be equally spaced and equally inclined but this is not the case. Only under very small signal condition or under incremental condition it will behave like a linear element.

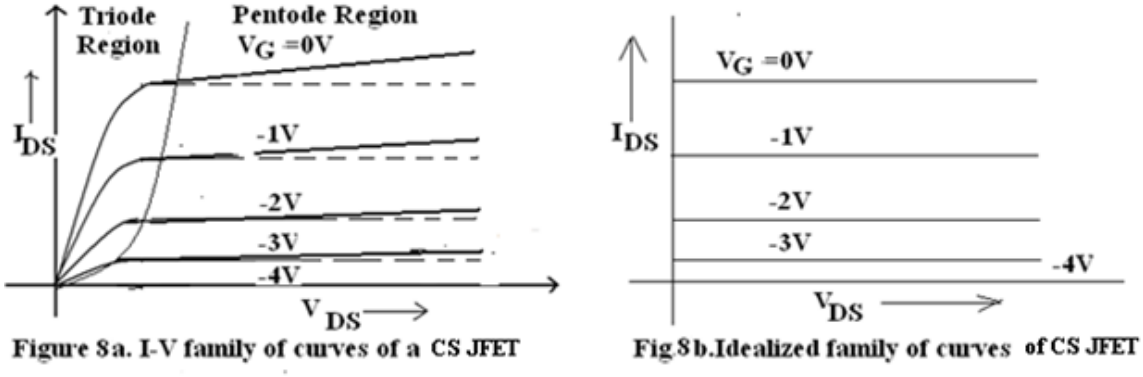


Figure 8a. I-V family of curves of a CS JFET

Fig 8 b.Idealized family of curves of CS JFET

Figure 4.10

Figure 8 gives the family of curves of a Common Source Junction Field Effect Transistor (CS_ JFET). By examining the idealized family of curves it is evident that CS_JFET output is a family of Constant Current Sources controlled by Gate Voltage. In order that CS_JFET behaves like a linear circuit element the family of curves must be equally spaced and equally inclined but this is not the case. Only under very small signal condition or under incremental condition it will behave like a linear element.

Q.8) what are the different types of controlled sources?

Ans:- The types of CONTROLLED sources are:-

a) Voltage Controlled Voltage Source
b) Voltage Controlled Current Source
c) Current Controlled Voltage Source
d) Current Controlled Current Source

The controlled sources shown in the figure 9 are ideal. In practice we do not have ideal controlled sources hence R_{out} of the controlled sources must be shown. Also at the input R_{in} will have to be shown.

In each of the controlled sources R_{in} and R_{out} should be shown as indicated in the Table below.

Table 1. Set of R_{in} and R_{out} and their placements in the four controlled sources.

Type of controlled source	Input impedance (R_{in})	Output Impedance(R_{out})
VCVS	High impedance at I/P node pair	Low impedance in series with controlled voltage source
VCCS	High impedance at I/P node pair	High impedance in parallel with controlled current source
CCVS	Low impedance at I/P node pair	Low impedance in series with controlled voltage source
CCCS	Low impedance at I/P node pair	High impedance in parallel with controlled current source

Table 4.1

Type Of Controlled Source	Rin	Rout	Controlled Source	Controlling Parameter	Type Of Ideal Amplifier	Parameter	Example Of Such A Device
Voltage Controlled Voltage Source	∞	0	Voltage	Input Voltage	Voltage Amplifier	Av	Triode,Op-Amp

continued on next page

Voltage Controlled Current Source	∞	∞	Current	Input Voltage	Transconductance Amplifier	G_m	Pentode,Field Effect Transistor(FET)
Current Controlled Voltage Source	0	0	Voltage	Input Current	Transresistance Amplifier	R_m	_ _
Current Controlled Current Source	0	∞	Current	Input Current	Current Amplifier	A_I	Bipolar Junction Transistor(BJT)

Table 4.2

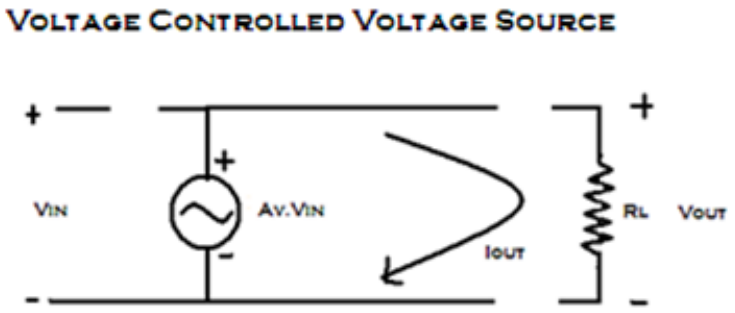


Figure 4.11

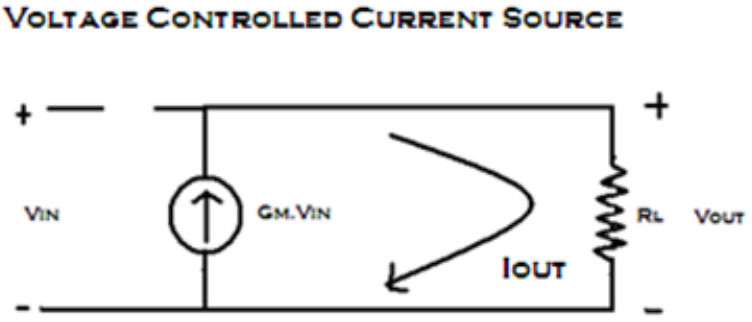


Figure 4.12

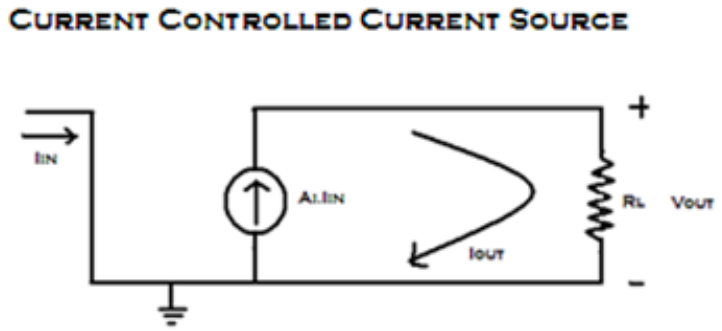


Figure 4.13

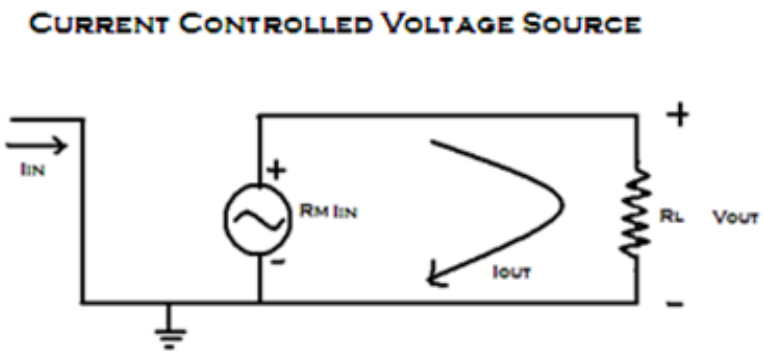


Figure 4.14

Figure 9. The incremental model of four controlled sources: VCVS,VCCS,CCCS and CCVS
The above controlled sources can be implemented using the four feedback topologies.
Voltage Sampling Voltage Comparison (Voltage-Series) feedback topology implements VCVS.
Voltage Sampling Current Comparison (Voltage-Shunt) feedback topology implements CCVS.
Current Sampling Voltage Comparison (Current-Series) feedback topology implements VCCS.
Current Sampling Current Comparison (Current-Shunt) feedback topology implements CCCS.
Q 9) What is the difference between passive device/component and active device/component?

Passive Device	Active Device
	continued on next page

R, L and C are passive devices	Diode, Vacuum Tubes, BJT, FET are active devices
A passive network comprising of passive components can neveramplify.	An active network comprised of active and passive-components, if suitably biased with a dc power supply,can amplify.
A passive network is unconditionally stable. It always has its poles lying in left half plane(LHP) or on jω axis of the complex plane.	An active network is potentially unstable. Its poles can lie in right half plane(RHP).

Table 4.3

Q.10) Are the controlled sources active network or passive network?

Since controlled sources have an amplifying property hence they are always Active Network. In a Controlled Source the controlling parameter may get amplified. This controlling parameter may be voltage or may be current. A VCVS is a Voltage Amplifier. CCCS is a current Amplifier.

Q.11) What is meant by Poles of a given network ?

This comes from network analysis of a given network in S-plane where S-plane is complex frequency plane. Laplace Transformation uses the complex frequency concept . The solution of S-plane analysisleads to complete response of the circuit. The complete response is the sum of transient plus steady state response. This is also known as natural response plus forced response. By Fourier Transform or by treating inductor as jωL and by treating capacitance as $1/(j\omega C)$ we arrive at steady state sinusoidal response of the network. The total response can be determined by Theory of Operator method also. In this approach the differential equation is set up and its solution determined. When the forcing function is made zero then the differential equation obtained is known as the characteristic equations or homogeneous equation. The roots of this characteristic equation are the poles of the system also known as natural frequencies of the system.These poles can be real or complex hence we say that the poles lie in complex plane. The nature of these poles determine the nature of transient response which is the solution of the characteristic equation or the homogeneous equation known as Complementary Function. This Complementary Function corresponds to the natural response or the transient response in Laplace Transform jargon.In Figure 10 we give the location of poles and its corresponding time-domain transient response.As seen from the Figure, poles in LHP correspond to exponentially decaying type transients which is an indication of stability. On the other hand the poles in RHP correspond to exponentially growing type transients which is an indication of instability which ultimately will lead to catastrophic collapse of the system.

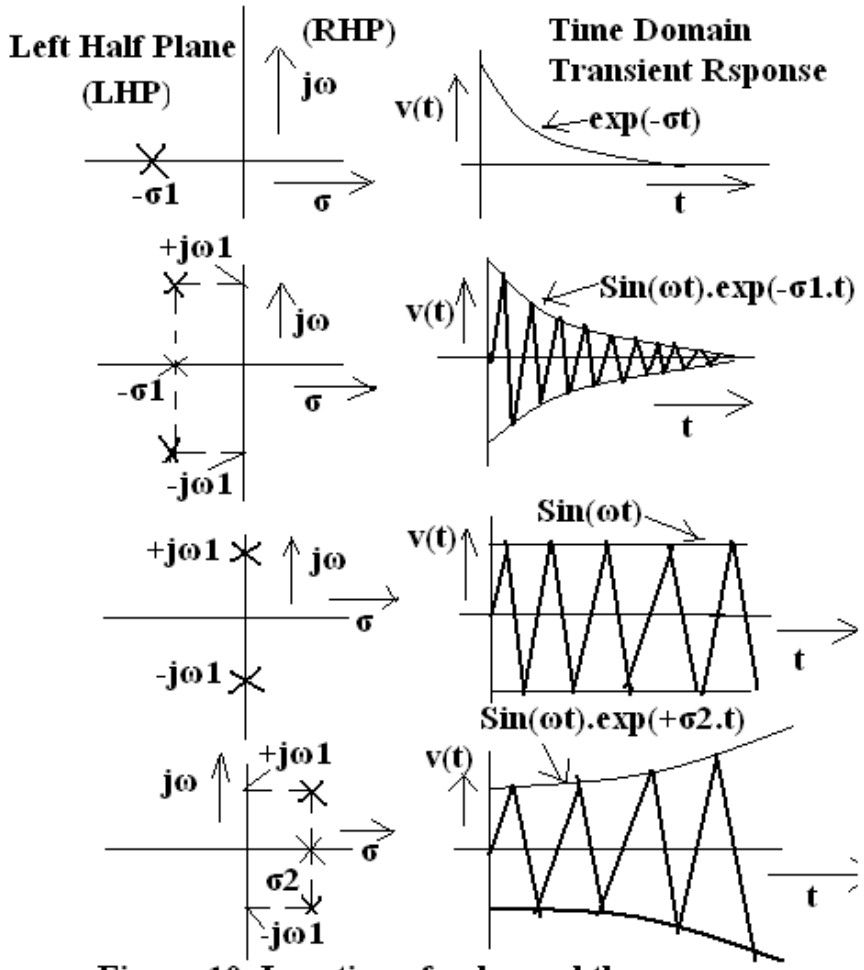


Figure 10. Location of poles and the corresponding Time-Domain Transient Response of the Network.

Figure 4.15

Chapter 5

Analog Electronics_Lecture 1_Supplement_Incremental Model of Controlled Sources[1]

AE_Lecture1_Supplementary_Incremental Model of Controlled Sources.

In last Chapter in Figure 9, we have given the incremental model of the controlled sources. Here we will describe the methodology of deriving the incremental model say of CE BJT.

A DC model of CE BJT will relate the output dc current, I_C , and output dc voltage, V_{CE} , to input dc current, I_B , and input dc voltage, V_{BE} , as shown in Figure 11.

[1] This content is available online at <http://cnx.org/content/m33376/1.1/>.

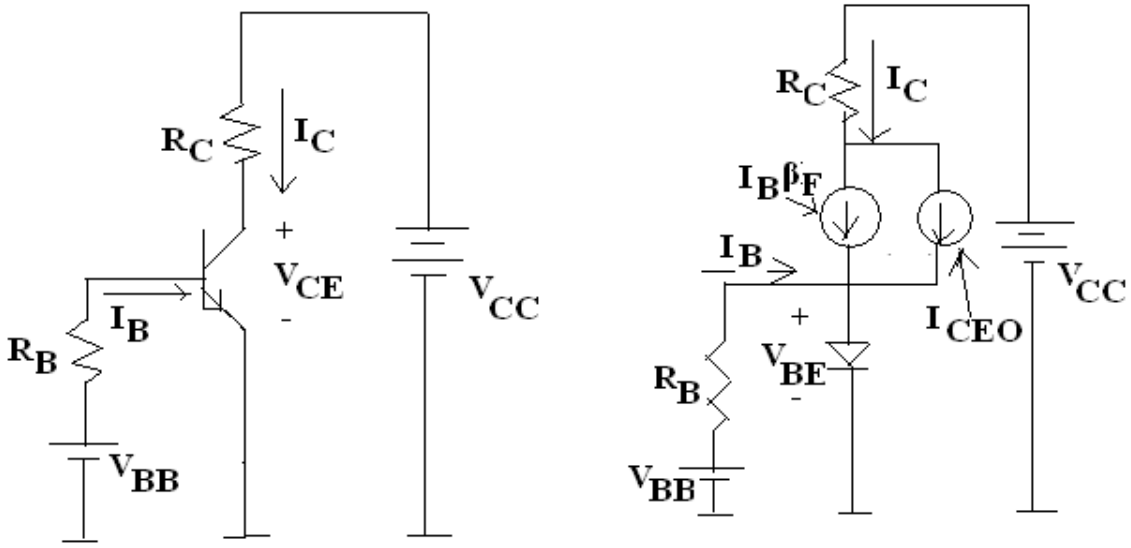


Figure 11. D.C. Model of CE BJT.

Figure 5.1

In Figure 11, the dc model of CE BJT is given. Since BJT is CCCS hence input current I_B controls the output current through current amplification factor β_F which is the short circuit current gain of CE BJT. The output current is:

$I_C = \beta_F.I_B + I_{CEO}$ 1

The second part of the output current, I_{CEO},is reverse leakage current of CB junction and is not controlled by input current I_B hence is non-useful current and is responsible for thermal –runaway as it is temperature sensitive. It doubles for every 10 °C rise in temperature.

The forward bias V_{BE} of BE junction decides the input current I_B and I_B in turn decides the output current I_C.

$$I_B = \frac{I_{EO}\, e^{\frac{V_{BE}}{V_T}}}{(1+\beta_F)}$$

Figure 5.2

2

Thus DC Model inter-relates output DC voltage and current to input DC voltage and current.

In a similar manner Incremental Model linearly inter-relates the incremental output voltage and current to the incremental input voltage and current. It is because of this linear inter-relationship between output

and input that we are forced to maintain the small signal condition or incremental signal condition. The moment the small signal condition is violated, the faithful amplification stops . The high fidelity of the system is lost.

To derive the incremental model we must introduce incremental voltage at the input as we have done in Figure 12.

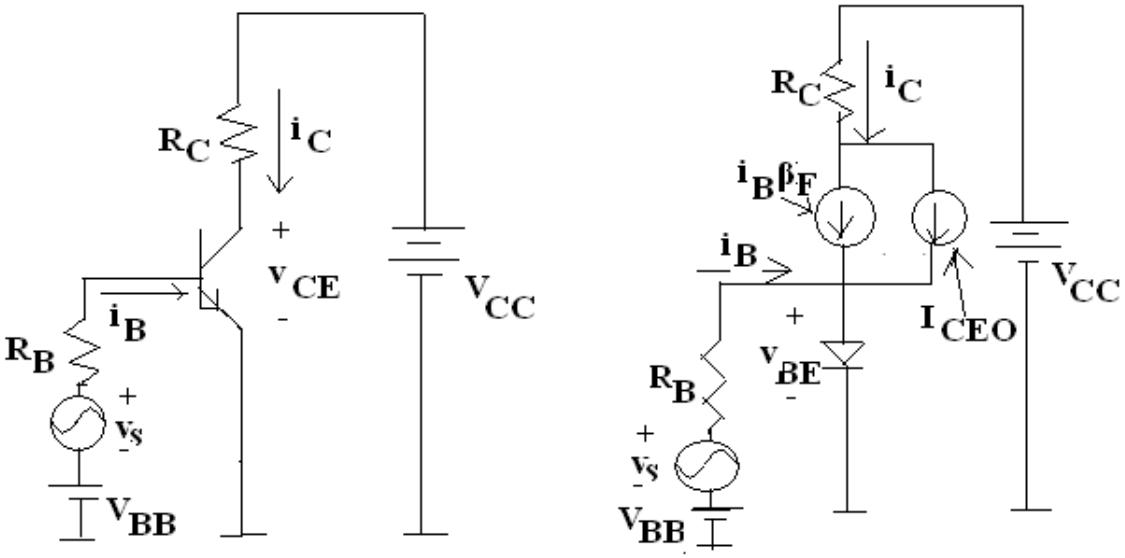


Figure 12. Instantaneous Model of CE BJT.

Figure 5.3

In Figure 12, we have instantaneous voltages and currents namely:
$i_B = I_B + i_b$,
$i_C = I_C + i_c$,
$v_{CE} = V_{CE} + v_{ce}$,
$v_{BE} = V_{BE} + v_{be}$.
Here we have DC voltage + incremental voltage and DC current + incremental current.

We are interested in finding an incremental model which only inter-relates the incremental part of the output -input voltage and output-input current.

There are two ways of doing it:

First way is that from the physics of the device we derive the incremental model. This is what we are going to do in subsequent chapters with respect to diodes, BJT and FET. This is called the physical incremental model and in respect to CE BJT it is called Hybrid-π Model and in respect to CB BJT it is called T-Model.

Second way is to develop a mathematical model. Here we short circuit the DC voltage sources and open circuit DC current sources, and retain only the incremental portions of the voltages and current and the incremental equivalent of diode and controlled sources. Once we apply this rule we get the incremental model as shown in Figure 13.

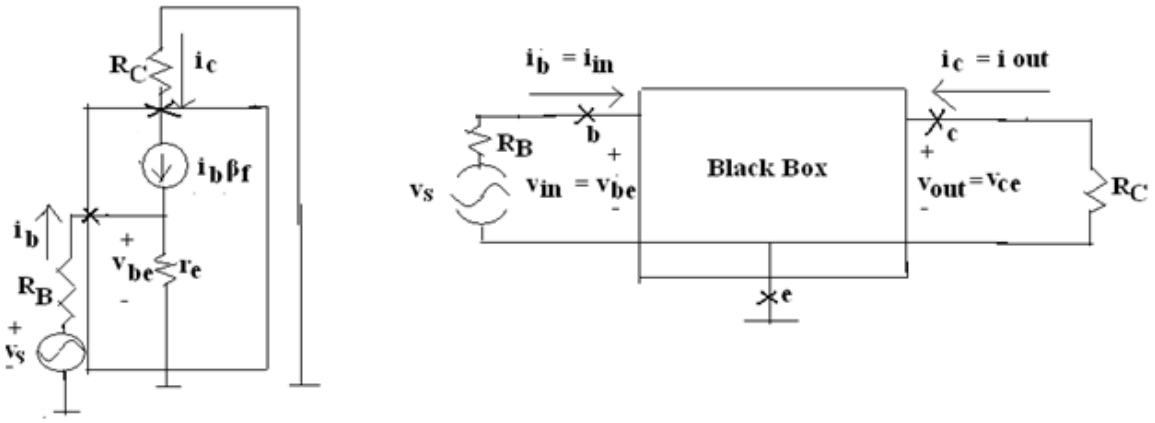


Figure 13. Incremental Model of CE BJT.

Figure 5.4

We have enclosed the active device in a black box and by measurements taken at the two ports, input and output ports, we determine the incremental parameters of the incremental model of the active device which is being treated as a black box.

If we relate (v_{in} , i_{out}) to (i_{in}, v_{out}) we have hybrid model.

If we relate (i_{in} , i_{out}) to (v_{in}, v_{out}) we have admittance model.

If we relate (v_{in} , v_{out}) to (i_{in}, i_{out}) we have impedance model.

In our syllabus we have hybrid model so we will deal with hybrid model.

In hybrid model of CE BJT:

(v_{in}) =F1 (i_{in}, v_{out}) = $h_{ie}.i_{in} + h_{re}.v_{out}$;

(i_{out}) =F2(i_{in}, v_{out}) = $h_{fe}.i_{in} + h_{oe}.v_{out}$;

From partial derivative theorem we know that :

(v_{in}) = total increment in instantaneous value of input voltage =

$$\Delta v_{IN} = v_{in} = \frac{\partial F1}{\partial i_{IN}}|_{V_{OUT}} \times \Delta i_{IN} + \frac{\partial F1}{\partial v_{OUT}}|_{I_{IN}} \times \Delta v_{OUT}$$

Figure 5.5

3

Physically this is interpretive as follows:

Input Voltage is a function of Input Current and Output Voltage hence

Total Increment in Instantaneous Input Voltage = incremental Input Voltage =

Partial derivative of F1 w.r.t.(with respect to) instantaneous Input Current with Output Voltage held constant ×increment in Instantaneous Input Current

PLUS

Partial derivative of F1 w.r.t.(with respect to) instantaneous Output Voltage with Input Current held constant ×increment in Instantaneous Output Voltage.

$$\frac{\partial F1}{\partial i_{IN}}|_{V_{OUT}}$$

Figure 5.6

= h_{ie} = input impedance with output shorted hence this is a short circuit parameter
=

$$\frac{v_{in}}{i_{in}}|_{v_{out}=0}$$

Figure 5.7

;

$$\frac{\partial F1}{\partial v_{OUT}}|_{I_{IN}} =$$

Figure 5.8

h_{re} = reverse transmission factor with input open hence this open circuit parameter
=

$$\frac{v_{in}}{v_{out}}|_{i_{in}=0}$$

Figure 5.9

;
Similarly

$$\Delta i_{OUT} = i_{out} = \frac{\partial F2}{\partial i_{IN}}|_{V_{OUT}} \times \Delta i_{IN} + \frac{\partial F2}{\partial v_{OUT}}|_{I_{IN}} \times \Delta v_{OUT}$$

Figure 5.10

$$\frac{\partial F2}{\partial i_{IN}}|_{V_{OUT}} =$$

Figure 5.11

h_{fe} = short circuit current gain =

$$\frac{i_{out}}{i_{in}}|_{v_{out}=0}$$

Figure 5.12

;

$$\frac{\partial F2}{\partial v_{OUT}}|_{I_{IN}}$$

Figure 5.13

= h_{oe} = open circuit output conductance if resistive
and open circuit output admittance if complex =

$$\frac{i_{out}}{v_{out}}|_{i_{in}=0}$$

Figure 5.14

.

At low and mid-frequencies h_{oe} is open circuit output conductance and high frequencies it is open circuit output admittance.

In Figure 14 , the Hybrid Model of CE BJT. It should be noted that there are two control sources:

First is $h_{fe}.i_b \rightarrow$ this causes a signal current gain in forward direction and

second is $h_{re}.v_{ce} \rightarrow$this causes a reverse transmission of signal voltage from output to input.

The second control source is not a desirable feature and it makes CE BJT a non-Unilateral Device which makes active networks made of CE BJT vulnerable to instability and parasitic oscillation at RadioFrequencies (RF) and above.

In subsequent chapters we will not take this mathematical route to arrive at the incremental model of the Active Devices. Rather from the first principle of Device Physics we will arrive at the incremental model of Active Devices.

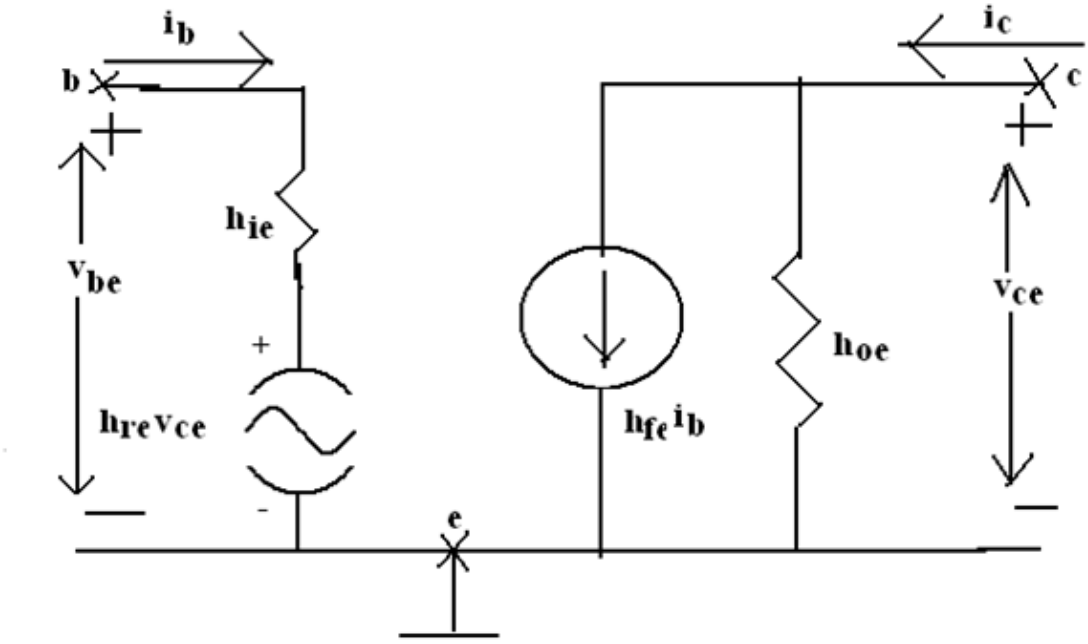


Figure 14. Hybrid Model of CE BJT

Figure 5.15

Chapter 6

Analog Electronics Lecture 2_PartA_I-V characteristics of Vacuum Tubes[1]

LECTURE NO.2_PartA

Analog Electronics Lecture 2_PartA_I-V characteristics of Vacuum Tubes

Key words; Triode, Pentode;

Summary: The family of Output Curves and the incremental model of Triode, Pentode ;

All the amplifying devices are Active Devices. Vacuum Tubes, Bipolar Junction Transistor(BJT) and Field Effect Transistors(FET) belong to this group. Whereas Resistors, Inductors and Capacitors are passive devices.

OUTPUT FAMILY OF CURVES OF ACTIVE DEVICES

TRIODE OUTPUT CHARACTERISTICS

The general output characteristics of a triode is as follows:

[1] This content is available online at <http://cnx.org/content/m29634/1.1/>.

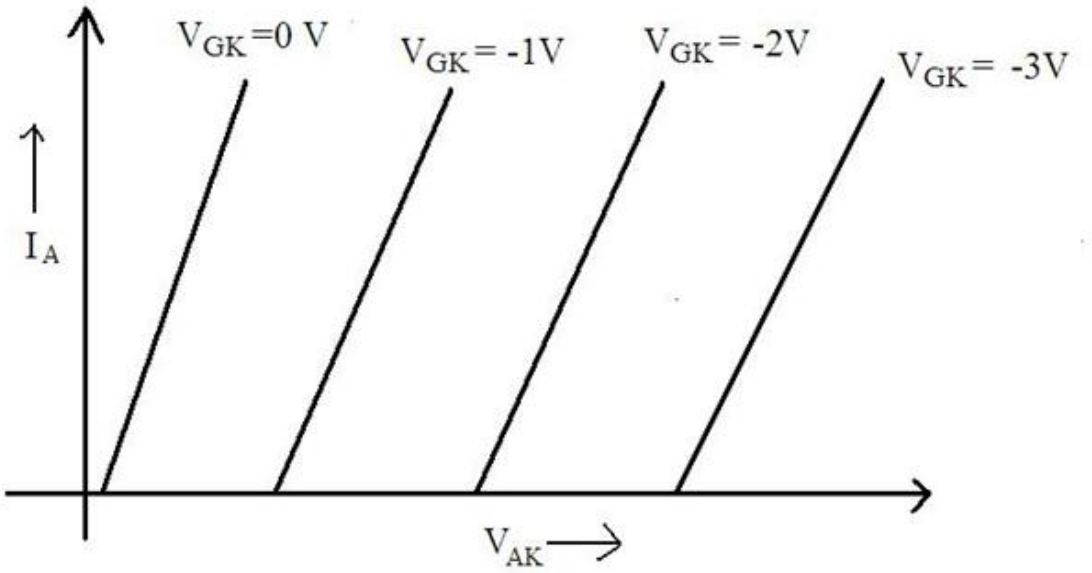


Figure 6.1

But the idealized output characteristics would look like:

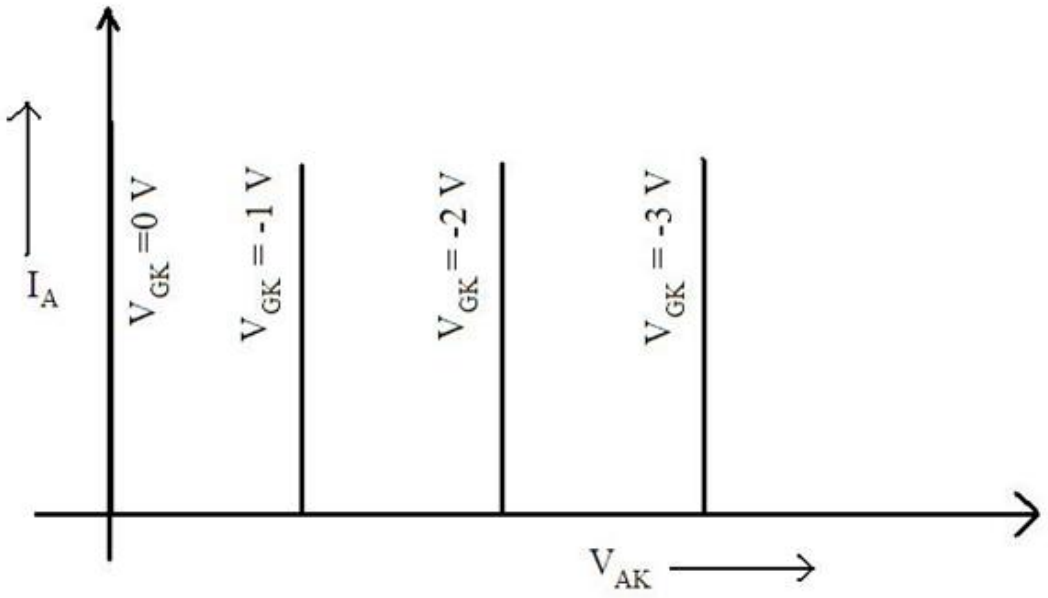


Figure 6.2

Thus triode is a voltage controlled voltage source.
The incremental model of a triode is:

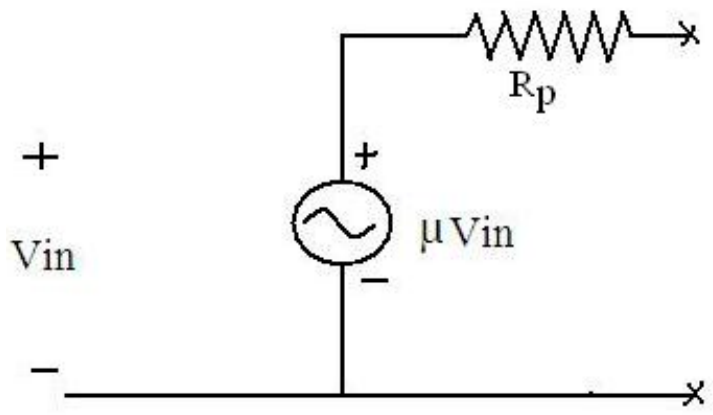


Figure 6.3

Where r_p =plate resistance

μ = Amplification factor

PENTODE OUTPUT CHARACTERISTICS

A pentode has 5 plates. They are cathode, grid, screen, suppressor and anode.

The general output characteristics of a pentode is as follows:

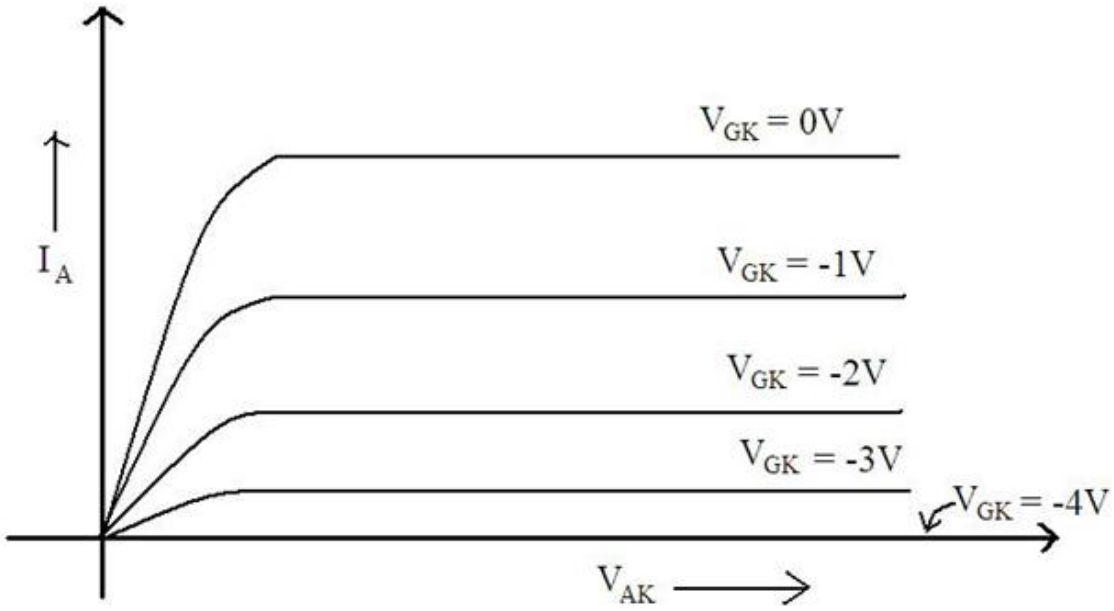


Figure 6.4

But the idealized output characteristics would look like:

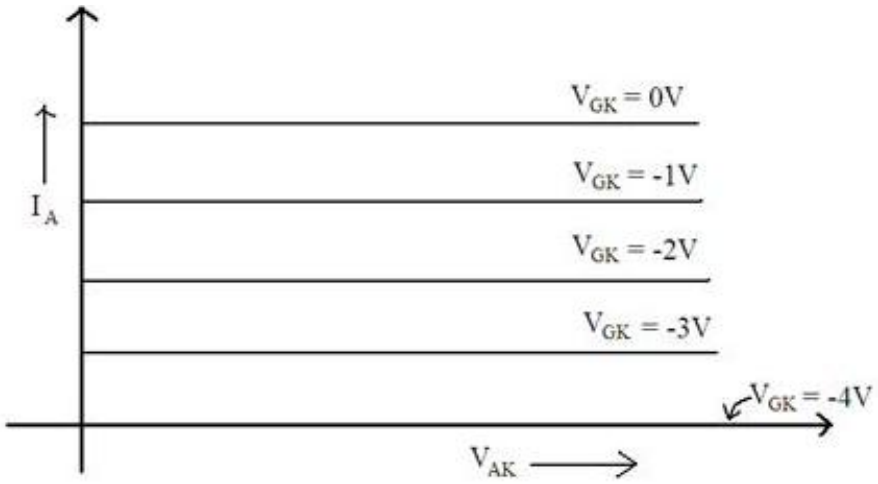


Figure 6.5

Thus pentode is a voltage controlled current source.
The incremental model of a pentode is:

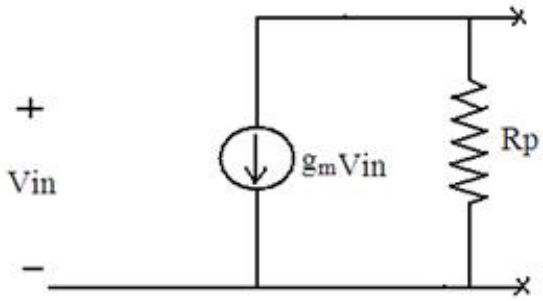


Figure 6.6

Rp is plate resistance and gm is transconductance and product of the two are amplication factor mu. Amplification factor is the maximum voltage gain that can be obtained from a Common Cathode Pentode Amplifier.

Chapter 7

Analog Electronics Lecture 2_PartB_BJT configurations & modes[1]

Analog Electronics Lecture 2_PartB_BJT configurations & modes

Key words;CE,CC & CB BJT;

Abstract: This describes three circuit configurations, four modes of operation and five schemes of biasing;

BIPOLAR JUNCTION TRANSISTOR

FOUR MODES OF OPERATION

Type Of Biasing	Emitter-Base Junction	Base-Collector Junction
Forward Active Mode	Forward Biased	Reverse Biased
Inverse Active Mode	Reverse Biased	Forward Biased
Saturation Mode	Forward Biased	Forward Biased
Cut-Off Mode	Reverse Biased	Reverse Biased

Table 7.1

THREE CIRCUIT CONFIGURATIONS

(1) COMMON BASE CONFIGURATION

[1]This content is available online at <http://cnx.org/content/m29635/1.1/>.

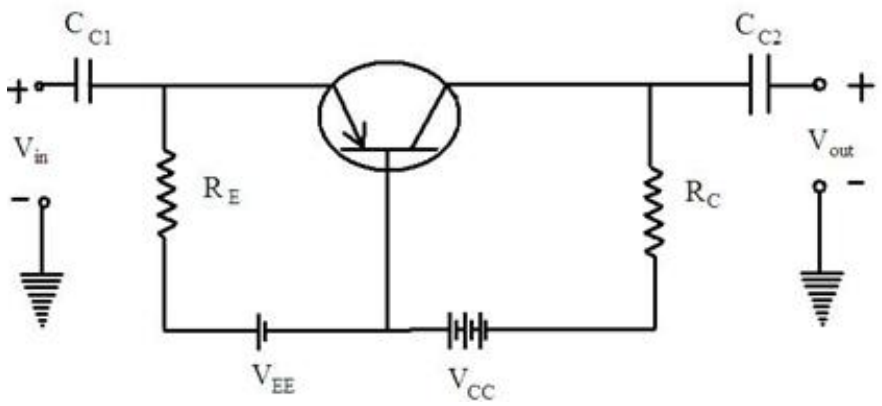


Figure 7.1

(1) COMMON EMITTER CONFIGURATION

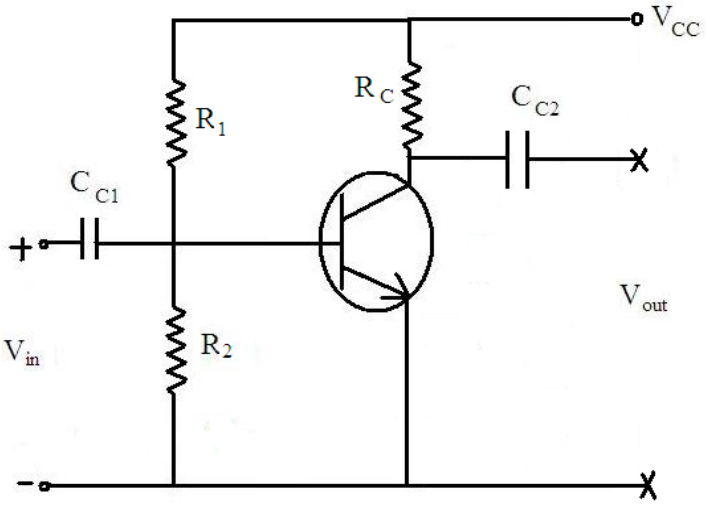


Figure 7.2

(1) COMMON COLLECTOR CONFIGURATION

TYPES OF BIASING SYSTEM USED

(1)Two battery biasing:
The 3 circuit configurations shown in the previous page are the examples of this biasing.
(2)Fixed Bias:
This type of biasing system offers poor stability because it has negative feedback..

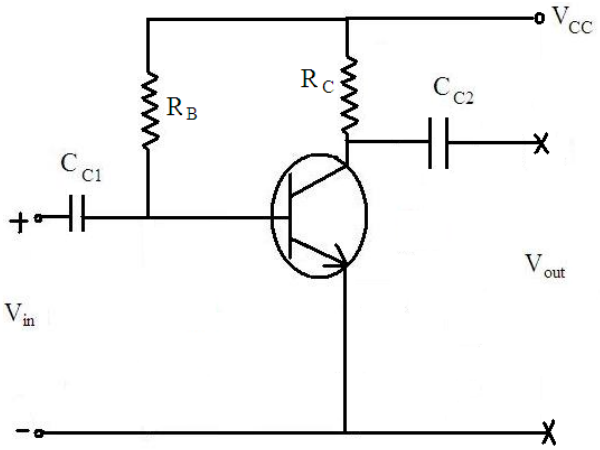


Figure 7.3

(3)Potential Divider Bias:
This type of biasing also offers poor stability because this also has no negative feedback.

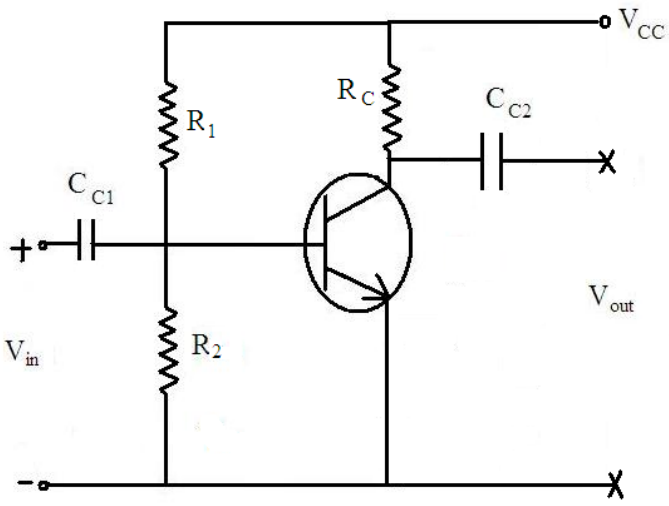


Figure 7.4

(4)Self Biasing:
This type of biasing system offers high stability because of current series feed-back.

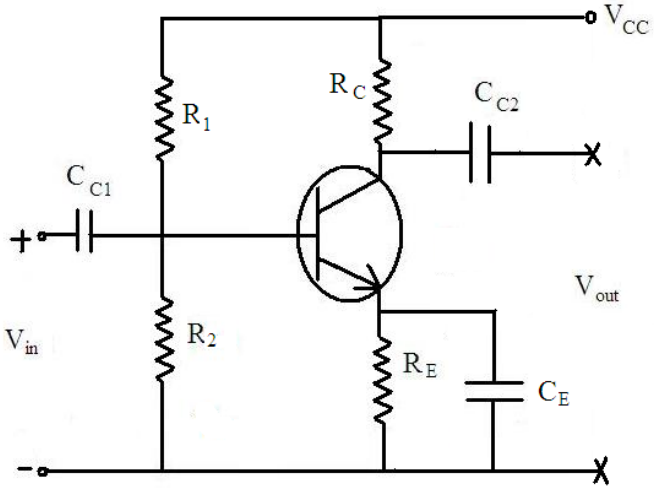


Figure 7.5

(5)Widlar Biasing:
The above types of biasing systems are used normally for discrete circuits. But this type of biasing is used for IC technologies. It offers high stability because of voltage shunt feed-back.This is also known as

collector to base feed-back.

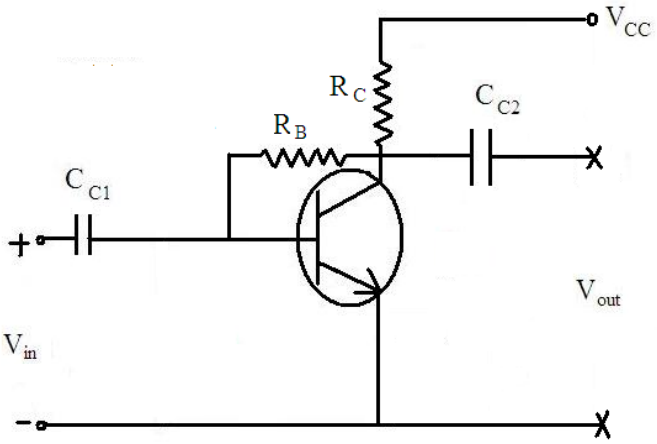


Figure 7.6

Chapter 8

Analog Electronics Lecture 2_PartC_I-V output characteristics of BJT[1]

Analog Electronics Lecture 2_PartC_I-V output characteristics of BJT

Key words;BJT;

Abstract: This describes the D.C. parameters of BJT.

BJT Common Base Configuration:

For CB Configuration :

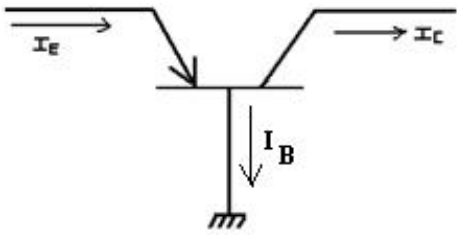


Figure 8.1

$I_C = \alpha_F M I_E + I_{CBO}$

Where α_F = D.C. Forward current transfer Ratio of CB BJT = I_C/I_E ;

M = Avalanche Multiplication Factor at Base-Collector Junction given by = 1/[1-(Vcb/BVcbo)^n]

[1] This content is available online at <http://cnx.org/content/m29636/1.2/>.

$$BV_{CBO}$$

Figure 8.2

Where n= Miller Indices =2∼6
I_{CBO} = Reverse leakage current at CB Jn with emitter open.

$$BV_{CBO}$$

Figure 8.3

= Avalanche breakdown voltage at CB Jn with emitter open
OUTPUT CHARACTERISTICS OF Common Base Bipolar Junction transistor

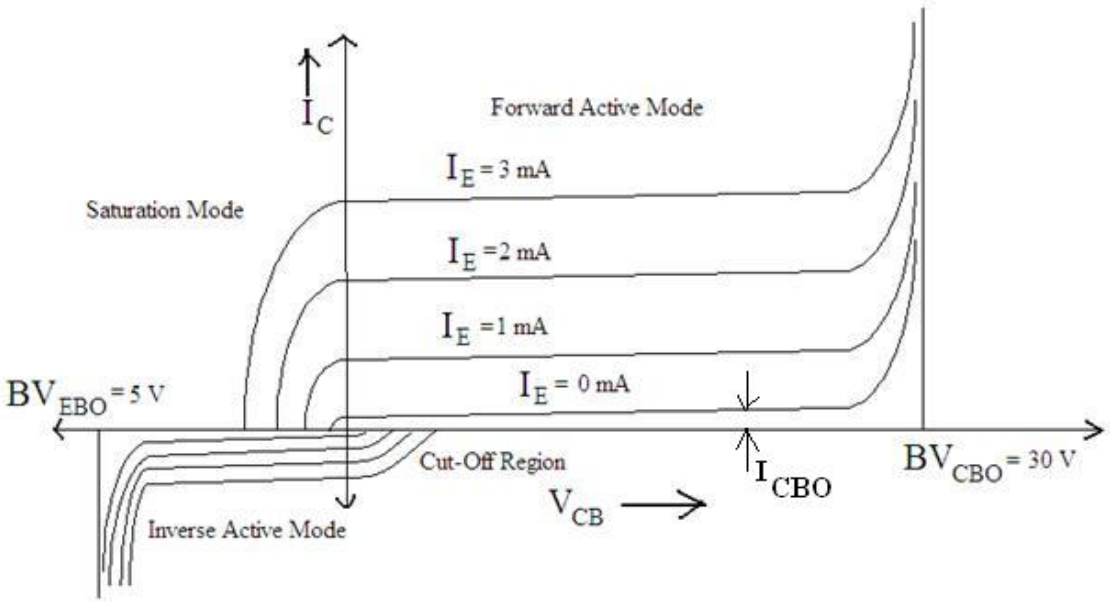


Figure 8.4

$I_C = I_{CBO}$ when $I_E = 0$ mA. This is the reverse leakage current at CB Junction with Emitter open and is of nA range.

BJT Common Emitter(CE) Configuration:

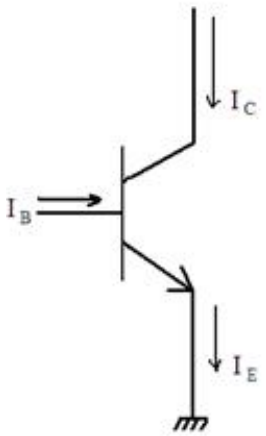


Figure 8.5

For CE Configuration :

$I_C = \alpha_F M I_E + I_{CBO}$

$=> I_C = \alpha_F M(I_B + I_C) + I_{CBO}$

$=> I_C(1-\alpha_F M) = \alpha_F M I_B + I_{CBO}$

$$=> I_C = \frac{\alpha_F M\, I_B}{(1-\alpha_F M)} + \frac{I_{CBO}}{(1-\alpha_F M)} \qquad \textbf{Eq.2}$$

Figure 8.6

$$=>I_C= \frac{\alpha_F M\, I_B}{(1-\alpha_F M)} + I_{CEO} \qquad \textbf{Eq.3.}$$

Figure 8.7

$$\text{Where } I_{CEO} = \frac{I_{CBO}}{(1-\alpha_F M)}$$

Figure 8.8

If M=1,

$$\frac{\alpha_F M}{(1-\alpha_F M)} = \frac{\alpha_F}{1-\alpha_F} = 100$$

Figure 8.9

Where α_F =0.99.
At low voltages we have M=1.

$$=>I_C= \frac{\alpha_F}{(1-\alpha_F)}\, I_B + \frac{I_{CBO}}{(1-\alpha_F)} \qquad \textbf{Eq.4.}$$

Figure 8.10

If we define $\frac{\alpha_F}{(1-\alpha_F)} = \beta_F$ =D.C. Short Circuit Current gain of CE BJT

$$= \frac{I_C}{I_B}$$

Figure 8.11

Then we get:

$$=>I_C = \beta_F I_B + (1 + \beta_F) I_{CBO} \qquad \textbf{Eq.5}$$

Figure 8.12

That is:

$$=>I_C = \beta_F I_B + I_{CEO} \qquad \textbf{Eq.6}$$

Figure 8.13

$$\text{Where } I_{CEO} = (1 + \beta_F) I_{CBO}$$

Figure 8.14

OUTPUT CHARACTERISTICS OF Common Emitter Bipolar Junction transistor

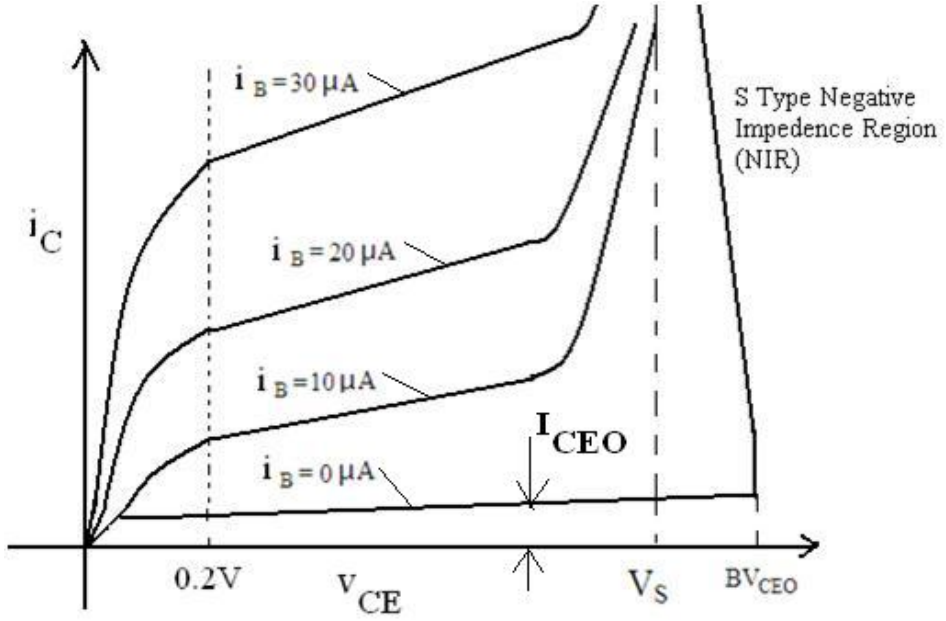


Figure 8.15

NOTE:-The slope in the figure is due to base width modulation which is also known as Early Effect.

$I_C = I_{CEO}$ when $I_B = 0$ mA. This is the collector junction leakage current at CB Junction with Base open and is of μA range.

Let us consider :

$$I_C = \frac{\alpha_F M\, I_B}{(1-\alpha_F M)} + \frac{I_{CBO}}{(1-\alpha_F M)} \qquad \textbf{Eq.7}$$

Figure 8.16

If $\alpha_F M = 1$, then

$$\frac{I_{CBO}}{(1-\alpha_F M)} = \infty$$

Figure 8.17

At this point , break over occurs. And we have BV_{CEO}=Break-over Voltage with Base Circuit open.
When $\alpha_F M$ =1
That is

$$\alpha_F \left[\frac{1}{1 - \left(\frac{V_{CB}^*}{BV_{CBO}} \right)^n} \right] = 1 \qquad \textbf{Eq.8}$$

Figure 8.18

$$\alpha_F = 1 - \left(\frac{V_{CB}^*}{BV_{CBO}} \right)^n$$

Figure 8.19

$$\left(\frac{V_{CB}^*}{BV_{CBO}} \right)^n = 1 - \alpha_F$$

Figure 8.20

But :

$$1-\alpha_F = \frac{1}{1+\beta_F} \qquad \textbf{Eq.9.}$$

Figure 8.21

Thus :

$$\left(\frac{V_{CB}^*}{BV_{CBO}}\right) = \frac{1}{\sqrt[n]{1+\beta_F}} \qquad \textbf{Eq.10}$$

Figure 8.22

Thus:

$$V_{CB}^* = \frac{BV_{CBO}}{\sqrt[n]{1+\beta_F}} \qquad \textbf{Eq.11}$$

Figure 8.23

Putting the required Values i.e. BV_{CBO}=30V, β_F = 100 , we get $V_{CB}{}^*$=18 V = BVceo ;
Now we have to know more about BV_{CES} (Breakover Voltage when the base circuit is shorted)
$BV_{CBO} > BV_{CEX} > BV_{CES} > BV_{CEO}$
Where BV_{CBO}= Breakover Voltage of the collector base junction when the emitter circuit is open.
BV_{CEX}= Breakover Voltage of CE BJT for a given termination R_X at the base
BV_{CEO}= Breakover Voltage of CE BJT when the base circuit is open.
BV_{CES}= Breakover Voltage of CE BJT when the base circuit is shorted to ground.
BV_{CEX}= Breakover Voltage when the base circuit is connected to ground through a source Resistance (R_S) .
By proper base termination, the permissible region of operation can be extended upto BV_{CBO}.

Thus we have seen that breakover occurs at $\alpha_F M = 1$. At low current α_F is very small, almost about 0.1.Therefore voltage has to be taken to a large value to satisfy $\alpha_F M = 1$. But as soon as breakover occurs large current starts flowing. With large current α_F improves from 0.1 to 0.99. Hence $\alpha_F M = 1$ is satisfied at lower voltage Vs. Therefore breakover curves settles down at Vs. This voltage V_S is known as sustaining voltage. Because of the fact that :

$V_S < BV_{CEO}$

We get a S Type Negative Impedance Region(NIR). In SCR and UJT also we get S Type NIR but in Tunnel Diode as shown in the Figure below we get N Type NIR.

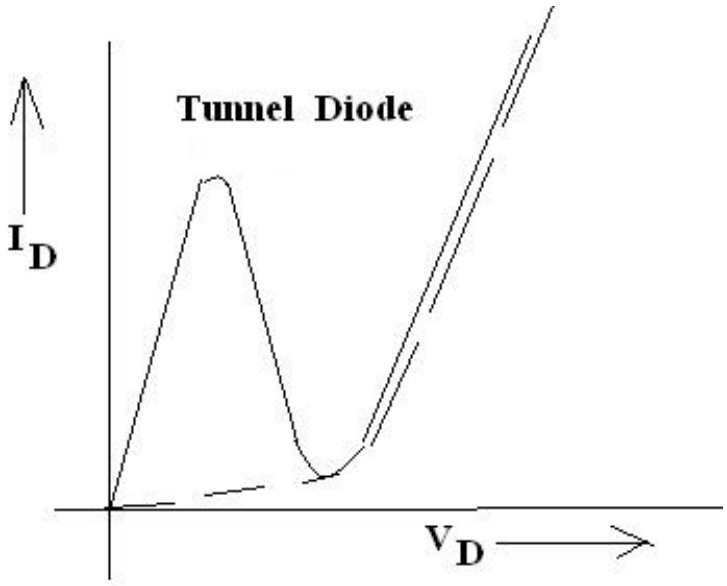


Figure 8.24

COMPARISON BETWEEN COMMON BASE AND COMMON EMITTER CONFIGURATIONS

S.No.	COMMON BASE	COMMON EMITTER
1	h_{rb}(reverse transmission factor)$\sim 10^{-5}$Thus it behaves as a near unilateral device.	$h_{re} \sim 10^{-4}$Thus it behaves as a non-unilateral device.

continued on next page

2	In RF applications the circuit has a high probability of parasitic oscillations but in CB because of near unilaterality , probability of parasitic oscillation goes down. Hence for RF applications CB is the preferred circuit configuration.	At low frequencies there is no danger of parasitic oscillations hence CE can be used even with poor reverse transmission factor.
3	h_{ob} = 1/(2M)Thus it behaves as a near ideal current source. Thus it is very suitable for charging a capacitance with a constant current to generate a saw-tooth waveform.	h_{oe}=1/(40K)Thus it behaves as a non-ideal current source.

Table 8.1

Both CB and CE are Current Controlled Current Source. CB is a near ideal CCCS whereas CE is a non-ideal CCCS.

Chapter 9

AnalogElectronics_Lecture2_Supplementary.[1]

AnalogElectronics_Lecture2_Supplementary.

Keywords: JFET, NMOS(enhancement) Normally-Off NMOS, NMOS(depletion)-Normally On NMOS,CMOS;

Abstract: This second part of Lecture 2 gives the Symbol, Output Characteristics and Transfer characteristics of nJFET, NMOS(enhancement) Normally-Off NMOS, NMOS(depletion)Normally-On NMOS.It gives the symbol of CMOS. It also gives a comparative study of BJT and FET.

FIELD EFFECT TRANSISTOR

A Field Effect Transistor is like a pentode. It is an analogue of pentode. Both are Voltage controlled Current Sources.

FET

JFET MOSFET

PJFET NJFET NMOS PMOS CMOS

Following are the symbols of JFET and MOSFET.

Just as we have NPN and PNP BJT, in exactly the same way we have P type FET and N type FET .

BJT are Bipolar devices. Here both majority and minority carriers partake in Transistor Action.

FET are Unipolar devices. Here only majority carriers take part in Transistor Action.

In NPN_BJT, electrons are emitted from Emitter and injected into Base and collected by Collector. Electrons play the dominant role.

In PNP_BJT, holes are injected into Base and eventually collected by the Collector.

In N type FET, electrons are sourced at SOURCE end into the channel and electrons are drained out of the DRAIN.

Vica Versa in P type FET, holes are sourced at SOURCE end into the channel and holes are drained out of the DRAIN.

JFET are DEPLETION Type also known as Normally-ON device. Here channel is present under zero gat voltage. By application of appropriate voltage the channel is gradually pinched off until complete pinch off occurs.

MOSFET can be both types: Normally On and Normally Off.

MOSFET(D) are depletion or Normally ON devices. Here under GATE Zero Voltage , channel is present.Therefore channel is represented by a continuous line. It can be depleted or enhanced.

MOSFET(E) are enhancement or Normally OFF devices. Here there is no channel therefore channel is represented by a broken line. When Gate Voltage crosses a threshold voltage then only channel is induced. Once the channel is induced the transistor is ON otherwise it is OFF.

[1] This content is available online at <http://cnx.org/content/m29589/1.1/>.

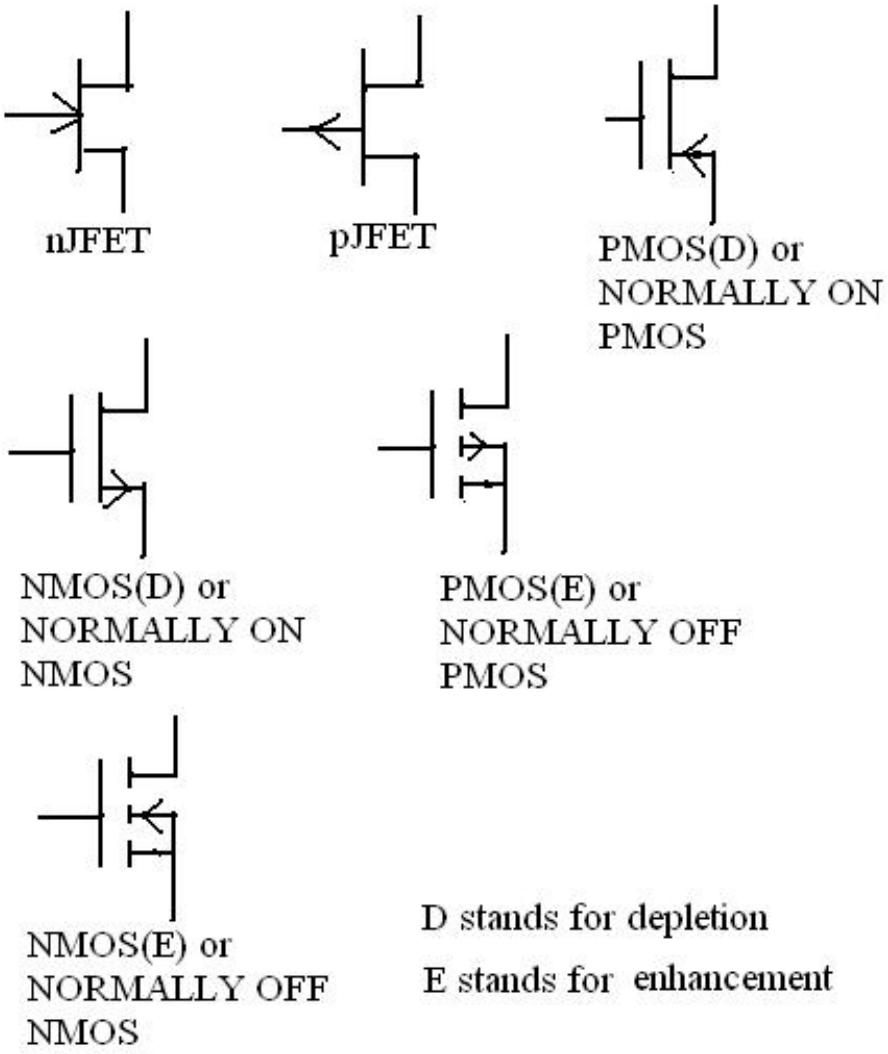

nJFET
pJFET
PMOS(D) or
NORMALLY ON
PMOS
NMOS(D) or
NORMALLY ON
NMOS
PMOS(E) or
NORMALLY OFF
PMOS
NMOS(E) or
NORMALLY OFF
NMOS
D stands for depletion
E stands for enhancement

Figure 9.1

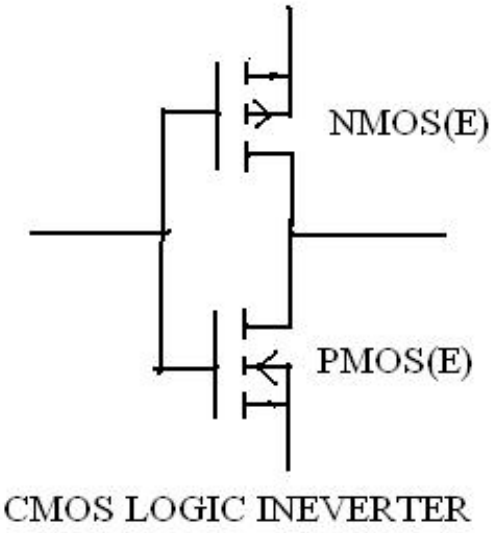


Figure 9.2

The following is the circuit diagram of a Common Source Amplifier using N-channel JFET:

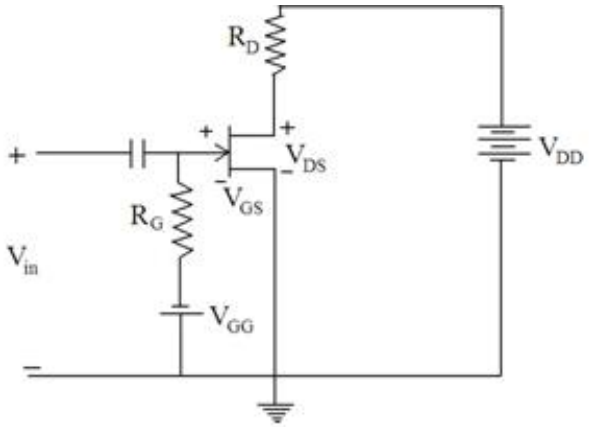


Figure 9.3

Characteristics of N-channel JFET

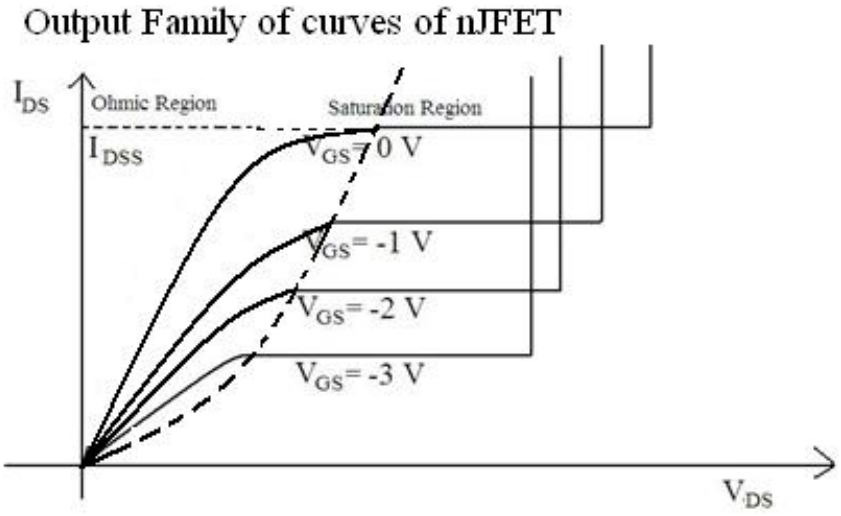


Figure 9.4

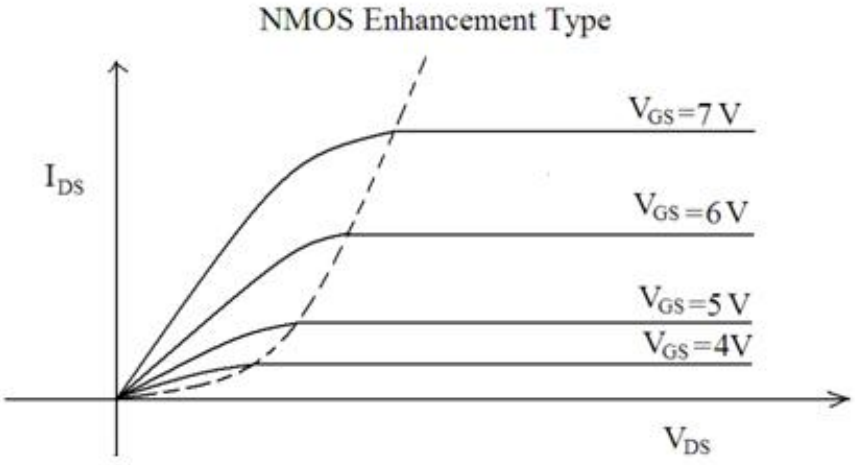


Figure 9.5

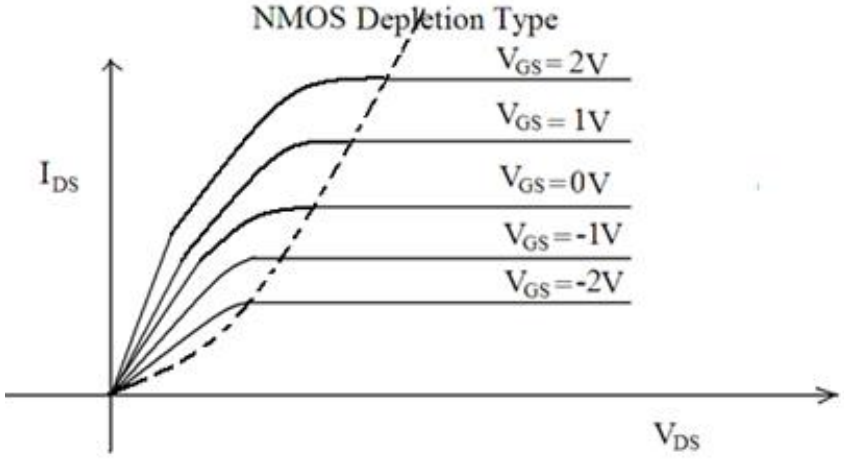


Figure 9.6

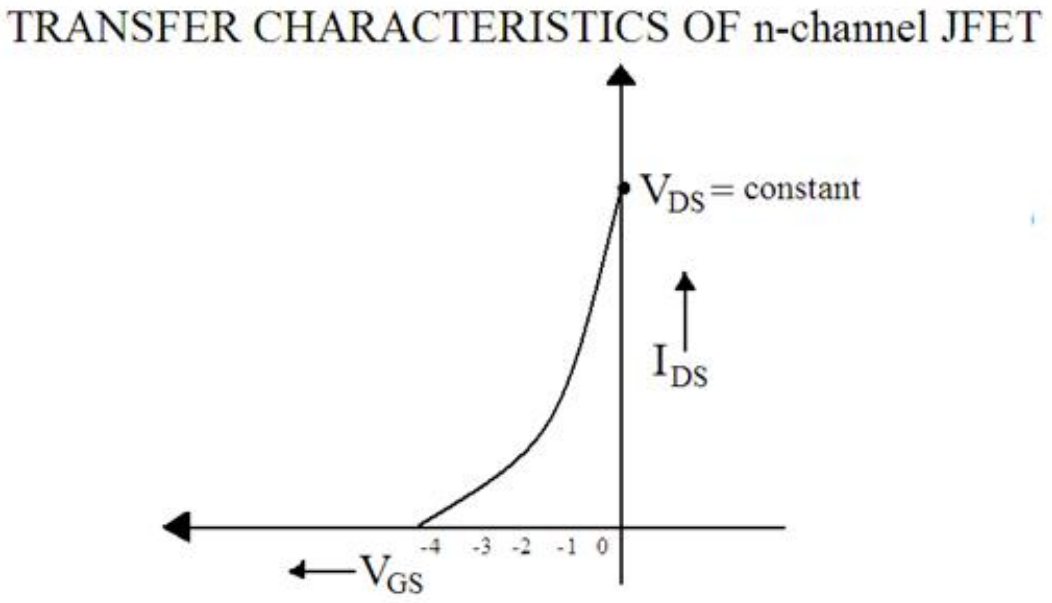


Figure 9.7

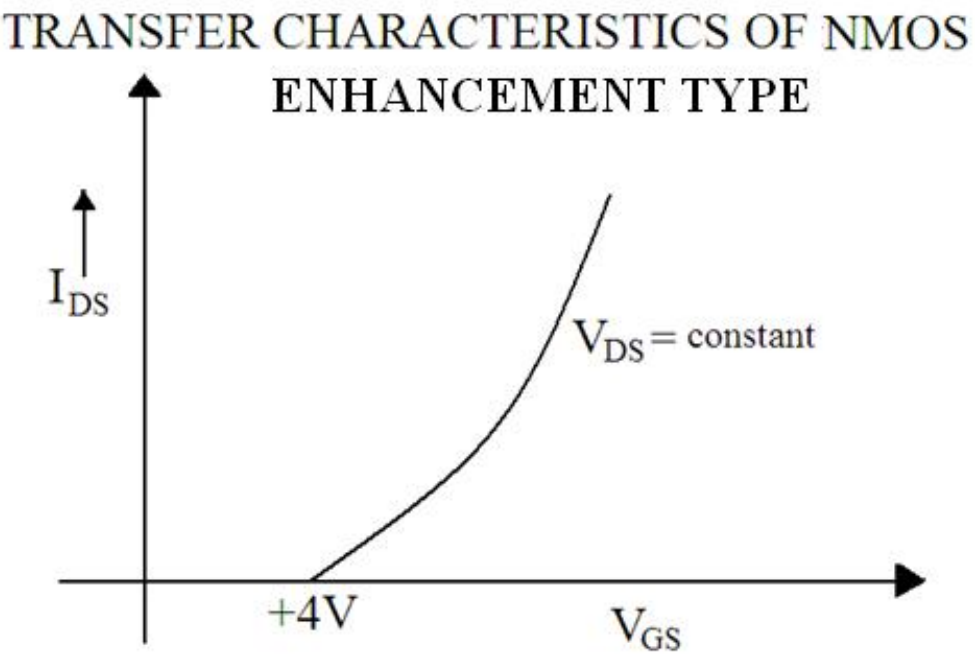

TRANSFER CHARACTERISTICS OF NMOS
ENHANCEMENT TYPE
I_{DS}
V_{DS} = constant
+4V
V_{GS}

Figure 9.8

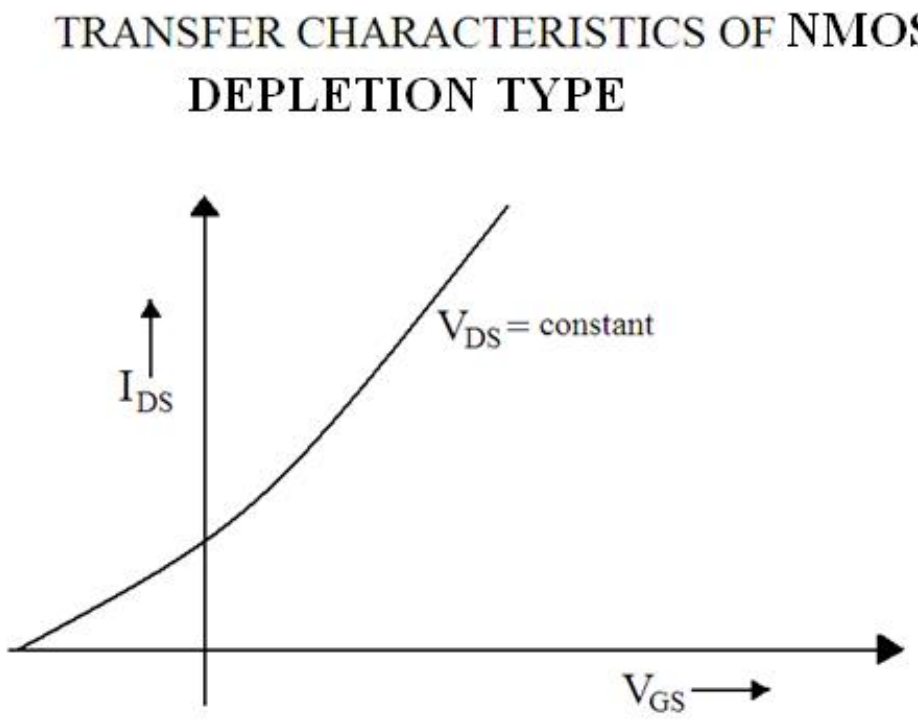


Figure 9.9

JFET has not proved amenable to integration. MOSFET are much more suitable for integration. It has a much better packing density. Historically MOSFET has a been two orders of magnitude slower. Today Pentium IV is toggling at 3GHz whereas best BJT is clocking at 300GHz. The following Table gives the comparative study of BJT and MOSFET:

	Bipolar Junction Transistor	Metal Oxide Semiconductor Field Effect Transistor
Carriers in action	Here both minority and majority take part in transistor action therefore BIPOLAR.	Here only majority carriers take part in transistor action therefore UNIPOLAR.

continued on next page

Speed	2 orders of magnitude faster	
Packing Density	Because of ISOLATION DIFFUSION packing density is one order of magnitude less	This a much higher packing density.MOS circuits are reaching 1 billion mark
Dynamic range	This exponential device hence harmonic distortion occurs beyond 5mV at the I/P	This is a quadratic device hence same order od harmonic distortion is beyond 400mV.
Noise Figure	This has THERMAL noise, SHOT noise, PARTITION noise but little FLICKER noiseHence Noise Figure is large	This has only THERMAL and FLICKER hence much quieter device. In fact for deep space communication cryogenically cooled MESFET is preferred for Low Noise Amplifier (LNA) at the front end.

Table 9.1

CMOS has the advantage of low stand by power dissipation over NMOS circuits hence CMOS is the technology of choice for PC revolution. CMOS is known as nano-watt logic.

JFET is not in common use but its variant Metal Semiconductor Field Effect Transistor(MESFET) is the technology of choice for LNA(Low Noise Amplifier).

Chapter 10

AnalogElectronics_Lecture3_Incremental Model of Diode.[1]

LECTURE NO. 3

INCREMENTAL MODEL OF A PN JUNCTION DIODE

Fig.1. A dc diode circuit.

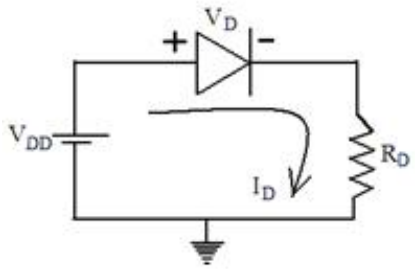


Figure 10.1

$V_{DD} = V_D + I_D . R_D$_____(1) This describes DC load line.

$I_D = I_{D0} \exp(V_D/V_T)$_____(2) This is the device characteristics.

Q-point or the quiescent point is the DC operating point and is obtained as the intersection of DC load line and the device characteristics.

[1] This content is available online at <http://cnx.org/content/m30500/1.1/>.

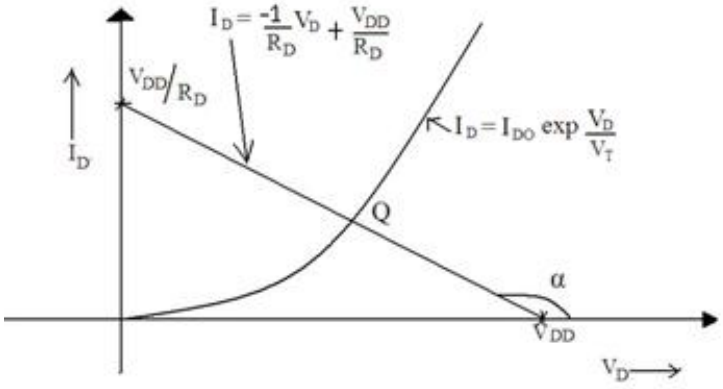


Figure 10.2

Figure 2. The dc load line , the device characteristics and the Q point.
Tan(α)= slope of the load line= (-1/R_D)
Under signal conditions:

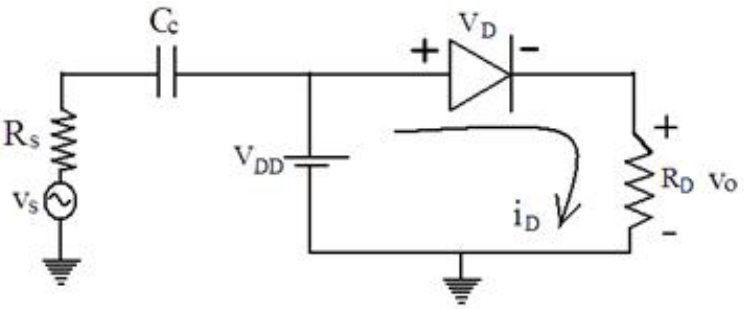


Figure 10.3

Figure 3. Signal is being coupled with the diode circuit.
$i_D = I_D + i_d$ where i_D is the instantaneous diode current.
I_D is the DC diode current.
i_d is the incremental diode current.
And v_D (instantaneous diode voltage) = V_D (DC Diode Voltage) + v_d_(incremental diode voltage)
Now the loop or the mesh equation is:-
$(V_{DD} + v_s) = v_D + i_D R_D$_____(3)
Rewriting the above equation we get:-
$(V_{DD} + v_s) = (V_D + v_d) + (I_D + i_d) R_D$_____(4)

Now we have (Instantaneous – DC) = Incremental part,
that is Eq.(4)-Eq.(1) :
$v_s = v_d + i_d R_D = v_d + v_o$;
Incremental circuit will be:-

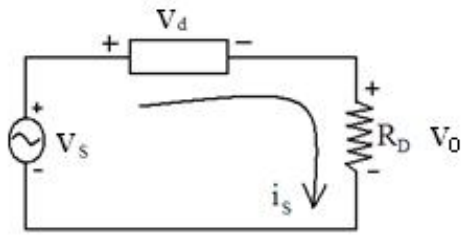


Figure 10.4

Figure 4. The incremental circuit of the Diode Circuit with signal.
A diode under instantaneous conditions has two parts :-

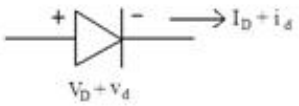


Figure 10.5

$$(I_D + i_d) = I_{DO} \exp\left(\frac{V_D + v_d}{V_T}\right)$$

Figure 10.6

The above is a relation between the diode current and the diode voltage.
We know that
$e^{[U+019F]} = 1 + [U+019F] + ([U+019F]^2/2!) + ([U+019F]^3/3!) + \ldots\ldots\ldots\ldots$
If $[U+019F] \ll 1$; $e^{[U+019F]} = 1 + [U+019F]$ This now becomes a linear equation.

If incremental voltage across the diode is less than 5 mV then [U+019F]≪1.
To maintain linearity, we maintain all the signals small.
So under small signal approximations,
$e^{[U+019F]} = 1+$[U+019F] will hold good.

$$(I_D+i_d) = I_{DO}\left[\exp\left(\frac{V_D}{V_T}\right)\right]\left[\exp\left(\frac{v_d}{V_T}\right)\right]$$

Figure 10.7

Now we note that V_T=26mV and the room temperature=300K and if $V_d < 5$ mV then we satisfy the small signal condition and we obtain:

$$(I_D+i_d) = I_D\left[1+\frac{v_d}{V_T}\right]$$

Figure 10.8

Then we have;

$$\cancel{I_D}+i_d = \cancel{I_D} + I_D\frac{v_d}{V_T}$$

Figure 10.9

Thus;

$$i_d \frac{V_T}{I_D} = v_d$$

Figure 10.10

Let:

$$\frac{V_T}{I_D} = r_d$$

Figure 10.11

Putting V_T=26mV and I_D=1mA we get r_d=26Ω.
Thus the incremental part of the diode circuit was determined as follows:

- We short circuit the DC voltage source(DC current source would have been open circuited).
- Any forward biased junction would be replaced by incremental resistance.

Incremental resistance r_d = (Thermal Resistance V_T/ Quiescent Current through the diode)

$$r_d = \frac{V_T}{I_D}$$

Figure 10.12

$$r_d = \frac{1}{\text{Slope of the tangent drawn at the Q-point}}$$

Figure 10.13

- All backward bias junction will act as open circuit.
- Ohmic resistance will offer resistance in both DC and incremental part.

This is small signal approximation. Thus Diode equivalent circuit is composed of linear elements only under small signal condition. Hence the circuit in Figure 4 is incremental circuit or small signal equivalent circuit. The incremental resistance r_d offered by the diode under small signal condition is a linear resistance and is included in the circuit only under incremental condition.

Table 1. Values of incremental resistance at 300K offered by a diode under various DC diode currents.

I_D (mA)	r_d (ohms)=V_T/I_D at Room Temerature(300K
1μA	26 kohms
10μA	2.6 kohms
100μA	260 ohms
1 mA	26 ohms
10mA	2.6ohms
100mA	0.26 ohms.

Table 10.1

Amplitude or Harmonic Distortion.

As can be seen from Figure 3, input sinusoidal voltage v_S appears as addition and subtraction to V_{DD}. Hence under signal condition, the load line is being shifted as shown in Figure 5. In doing so Q pint also shifts generating sinusoidal current swing. As can be seen in the figure, a small segment of I-V curve of the diode(which is the case under small signal condition) is essentially a straight line. Hence Q moves along a straight segment and in the process generates a sinusoidal swing in the current.

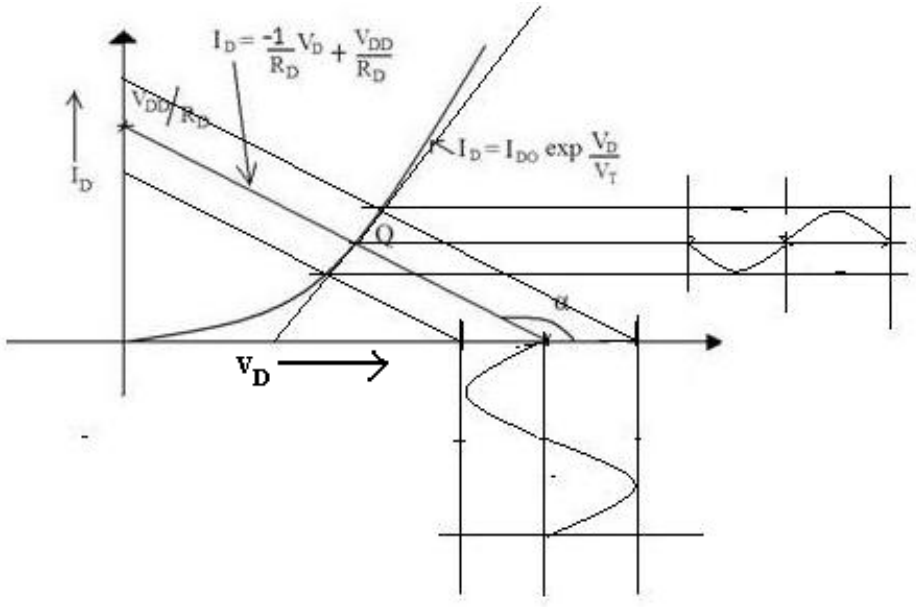


Figure 10.14

Figure 5. Diode Current Sinusoidal Swing under Sinusoidal Input Voltage under small signal condition.

But as seen in Figure 6, if input voltage is a large signal then Q traces a non-linear segment of I-V curve. This results in non-sinusoidal current swing in the diode. This means a sinusoidal voltage is not giving rise to a sinusoidal current in the output load resistance R_L. Hence the output voltage will be non-sinusoidal and its Fourier Series Expansion will contain Fundamental and Harmonics. This is known as Amplitude or Harmonic Distortion.

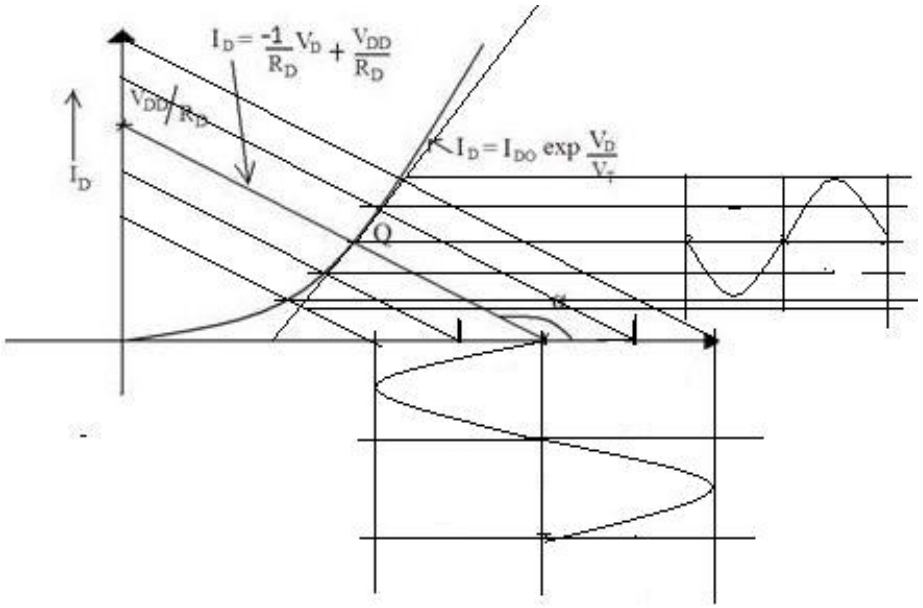


Figure 10.15

Figure 6. Non-sinusoidal diode current swing when input voltage is a large voltage.

Chapter 11

AnalogElectronics_Lecture3supp._High Frequency Model of PN Junction Diode.[1]

AnalogElectronics_Lecture3supp._High Frequency Model of PN Junction Diode.

At high frequency, the Depletion Layer Junction Capacitance(C_{JD}) under reverse biased and {C_{JD} plus C_D(Diffusion Capacitance)} comes in parallel with the incremental resistance r_d . At very high frequencies even the leads will offer an inductive reactance but we are going to neglect it for the present syllabus. The incremental Model of PN Junction Diode at high frequencies is given in Figure 1.

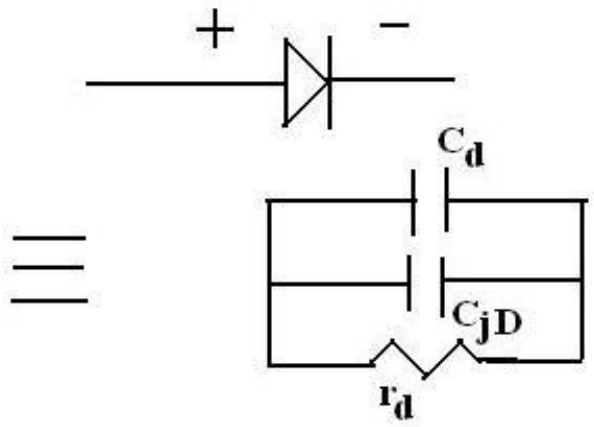


Figure 11.1

Figure 1. Incremental Model of Diode at high frequencies.

Junction Capacitance (C_{jD}) is present in both reverse and forward biased diodes because it is due to depletion layer/space charge layer/dipole layer present at the metallurgical junction of the diode.

Diffusion Capacitance(C_d) is present only in forward bias because it is due to excess minority carrier stored under forward biased condition. In reverse bias condition there is no excess minority carrier stored in the bulk region.

[1]This content is available online at <http://cnx.org/content/m30790/1.1/>.

In Figure 2 we see the deleterious effect of $C_d + C_{jD}$ on the switching performance of the diode. Ideally a diode should stop conducting and it should switch off but this switch off is not instantaneous. If a forward biased diode is reverse biased it continues to conduct in the reverse direction for time ($t_{storage} + t_{discharge}$) before it switches off. The switching transient of a diode is shown in Figure 2.

The delay in switching is due to the time delay in removing the excess minority carriers and time taken in discharging the junction capacitance.

Time delay in removing the minority carriers is storage delay = $t_{storage}$;

Time taken in discharging the junction capacitance shows up as a fall time = $t_{discharge}$;

The Physics of removal of minority carriers and discharging of C_{JD} are shown in Figure 3.

A diode circuit which is initially forward biased. At time t1, by a Single Pole Double Throw Switch(SPDT), it is abruptly reverse biased. Note that diode does not abruptly switch off.

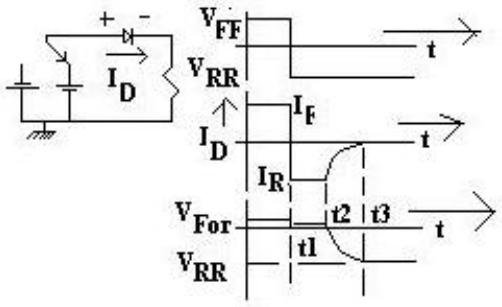
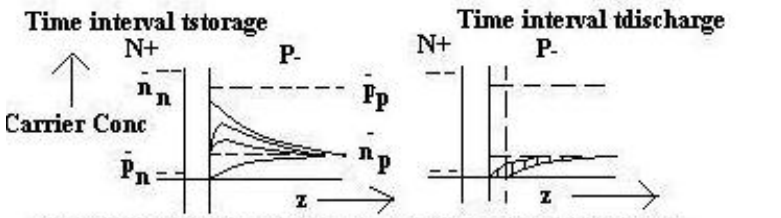


Figure 11.2

Figure 2.Switching Transient of a Diode.



Since we are considering one-sided step junction we need to consider the minority carriers in lightly doped region in this case P- region.

As can be seen, excess minority carriers are gradually removed. In this time interval reverse diode current flows with as much ease as forward diode current flows

Figure 11.3

Figure 3. The process of minority carrier removal during (t storage + t discharge)

Diode Junction Capacitance (CjD) = $(\varepsilon_0 \varepsilon_r A/d)$ where A= cross sectional area of the diode and d=depletion width;

Physics of Diode Junction Capacitance:

The doping profile of N+ and P- decide the voltage dependence of Junction Capacitance.

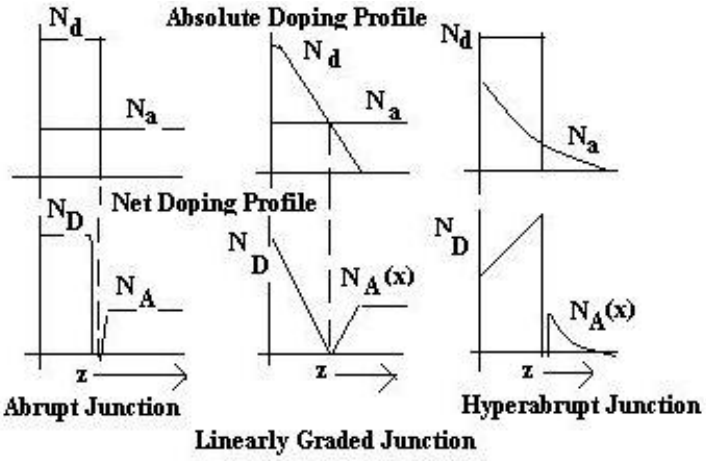


Figure 11.4

Figure 4. Doping profile of abrupt junction, linearly graded junction and hyper-abrupt junction.

$$N_A(z) = B(\frac{z}{z_0})^m$$

Figure 11.5

z_0 = position of metallurgical junction along the longitudinal axis.
Depletion Width in a hyper-abrupt junction:
$d \sim d_p = K(V_R)^{1/(m+2)}$

$$C_{jD} = \frac{\varepsilon A}{d} = \frac{\varepsilon A}{K(V_R)^{\frac{1}{m+2}}}$$

Figure 11.6

In an abrupt junction or one sided step junction, m = 0 :

$$C_{jD} = \frac{\varepsilon A}{K(V_R)^{\frac{1}{2}}} =$$

Figure 11.7

varies as $1/(\text{Reverse Bias Voltage} = V_R)^{1/2}$;
In linearly graded junction, m = 1:

$$C_D = \frac{\varepsilon A}{K(V_R)^{\frac{1}{1+2}}} = \frac{\varepsilon A}{K(V_R)^{\frac{1}{3}}} :$$

Figure 11.8

varies as 1/(Reverse Bias Voltage= V_{RR})$^{1/3}$;
In hyper - abrupt junction, m = -

$$\frac{3}{2}$$

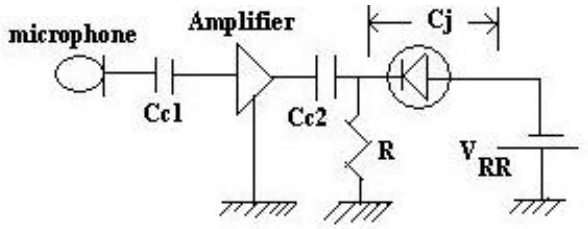
Figure 11.9

:

$$C_D = \frac{\varepsilon A}{\frac{1}{K(V_R)^{-(\frac{3}{2})+2}}} = \frac{\varepsilon A}{K(V_R)^2} =$$

Figure 11.10

varies as (Reverse Bias Voltage= V_{RR})^2;
Hyper - abrupt Junction Diode is known as VARACTOR DIODE. It is used for Frequency Modulated Waves generation.

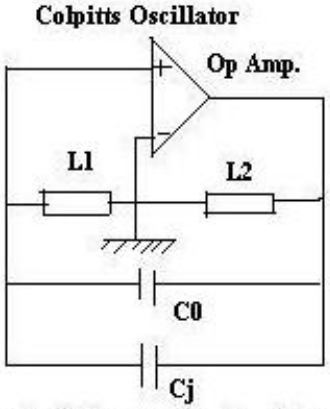


Arrangement for modulating a varactor diode capacitance Cj in accordance with a audio signal generated by a microphone.

This Cj can be used in RF oscillator to generate a FM carrier. The carrier frequency will be directly proportional to the reverse voltage Vj applied across Cj.

Figure 11.11

Figure 5. Arrangement for modulating Varactor diode junction capacitance by audio signal.



Varactor Diode represents element Cj.

As Cj is modulated so is the carrier frequency modulated.
This modulated carrier is FM carrier

Figure 11.12

Figure 6. A Colpitts Oscillator with a varactor diode in its tank circuit.
The frequency of oscillation of Colpitts Oscillator is the Frequency of Resonance of the Tank Circuit.
Radial Frequency of Oscillation=ω_0 =

$$\frac{1}{\sqrt{(L_1+L_2)(C_0+C_j)}};$$

Figure 11.13

Let $C_j/C_0 \gg 1$ then ω_0 =

$$\frac{1}{\sqrt{(L_1+L_2)(C_0+C_j)}} = \frac{1}{\sqrt{(L_1+L_2)\left(C_0\right)(1+\frac{C_j}{C_0})}} = \frac{1}{\sqrt{(L_1+L_2)(C_0)}}\sqrt{\frac{C_0}{C_j}};$$

Figure 11.14

Therefore ω_0 =

$$\frac{1}{\sqrt{(L_1+L_2)(C_0)}}\sqrt{\frac{C_0}{\frac{\varepsilon A}{K(V_R)^2}}} = \frac{1}{\sqrt{(L_1+L_2)(C_0)}}\sqrt{\frac{C_0}{\frac{\varepsilon A}{K}}} \times V_R$$

Figure 11.15

Thus we obtain frequency proportional to frequency. This generates FM carrier.
Physics of Diffusion Capacitance:
It can be shown that diffusion capacitance C_d can be obtained by the following relation:
For one sided step junction N+P,
$r_dC_d = \tau_n$ where τ_n life-time of minority carriers in lightly doped side.
In equally doped diode,
$1/\ r_dC_d = 1/\tau_n + 1/\tau_p$ where τ_n life-time of minority carriers on P-type doped side.
τ_p life-time of minority carriers in N-type doped side.
In BJT in forward active mode:
$r_eC_d = \tau_t$
where r_e = incremental resistance of EB diode;
τ_t = transit time across the base.

Chapter 12

AnalogElectronics_Lecture4_PartA_dc,low&h frequency model of CB BJT.[1]

AnalogElectronics_Lecture4_PartA_dc,low&high frequency model of CB BJT.

The DC model of BJT.

PNP is a face to face diode.

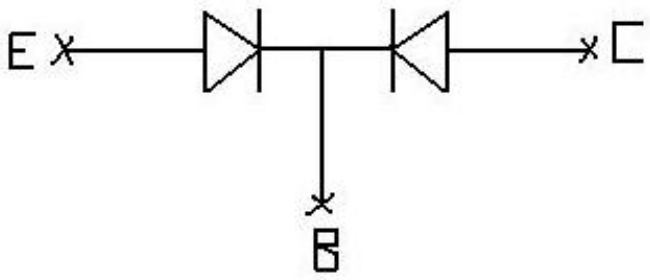


Figure 1. PNP is a face to face diode configuration.

Figure 12.1

NPN is a back to back diode.

[1] This content is available online at <http://cnx.org/content/m30983/1.1/>.

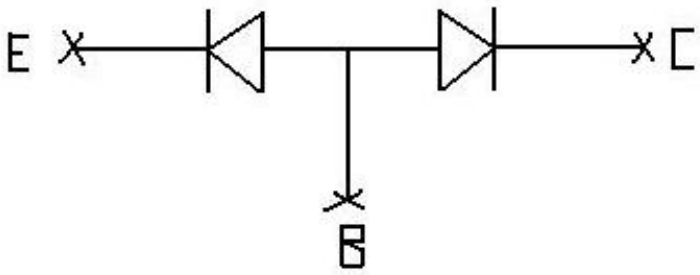


Figure 2. NPN is a back to back diode

Figure 12.2

DC Biasing of CB BJT (Common Base BJT) In the figure base is grounded.

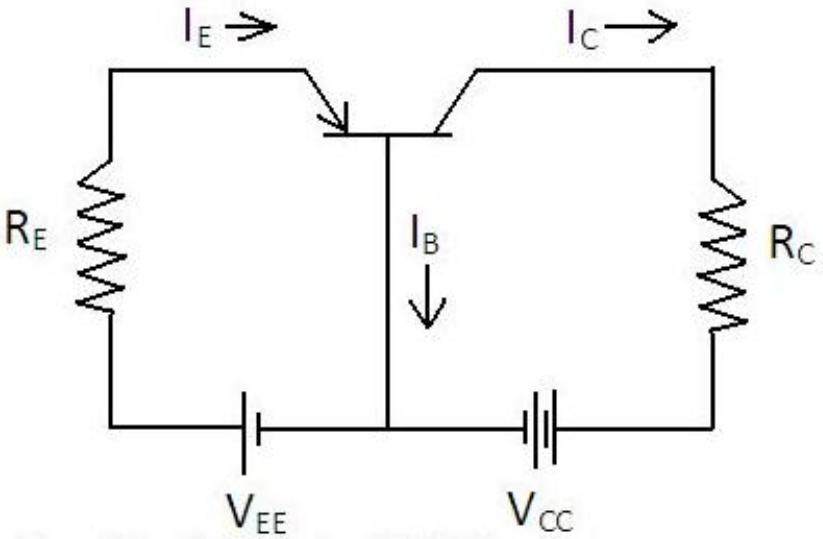


Figure 3. Two Battery biasing of CB BJT.

Figure 12.3

The DC model of CB BJT is called Eber Moll Model. It is a large signal model.

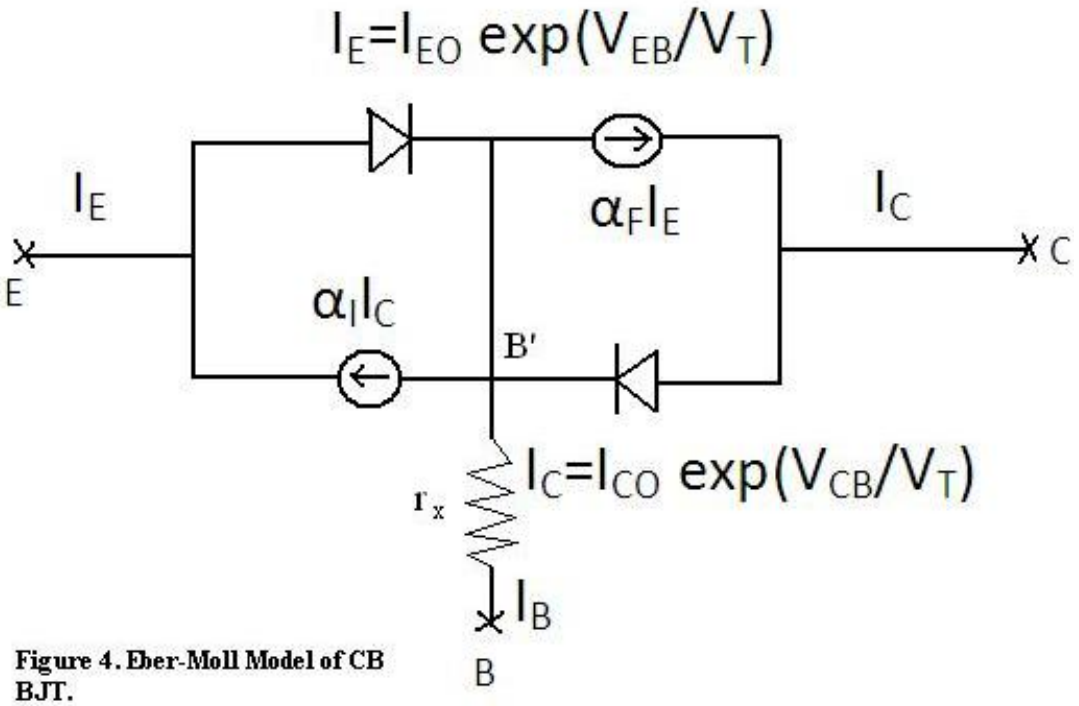


Figure 12.4

Figure 4. Eber Moll Model of PNP Transistor under no bias.

As can be seen from the Eber Moll Model:

$\alpha_F I_E$ is the controlled current source controlled by the current injected from E to B where α_F is short circuit forward current transfer ratio.

$\alpha_I I_C$ is the controlled current source controlled by the current injected from C to B where α_I is short circuit inverse current transfer ratio.

Because of asymmetrical doping density, [Heavy Emitter doping(10^{19}/cc), Intermediate Base doping(10^{17}/cc) and light Collector doping(10^{16}/cc)]

emitter to base injection efficiency is 99%

whereas collector to base injection efficiency is less than 10% therefore ($\alpha_I = 0.1$)$\ll$ (α_F=0.99).

Under Forward Active Mode:

EB diode is forward biased and CB diode is reversed biased. Hence current is being injected from emitter to base but no current is being injected from collector to base. Therefore EB diode is shown and CB diode has been omitted but there is reverse saturation current/reverse leakage current I_{CBO} flowing through reverse biased CB junction. In fact there are two currents flowing across the CB junction. One is the leakage current I_{CBO} and the other is the useful transistor current $\alpha_F I_E$ due to transistor action at EB junction.

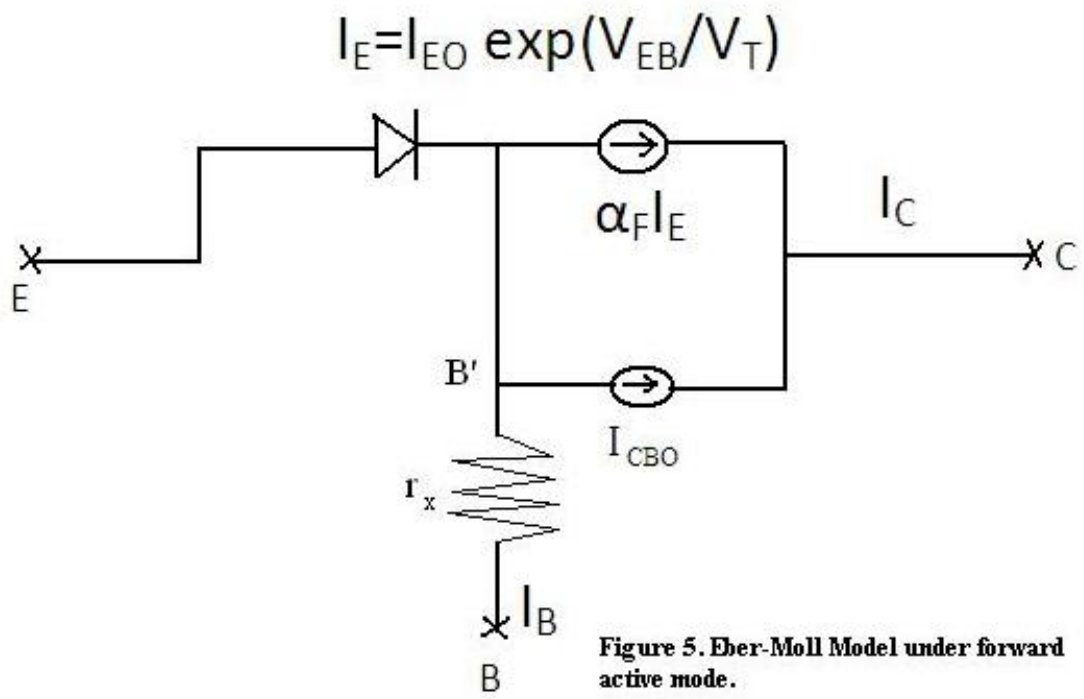


Figure 12.5

Figure 5. Eber Moll Model under Forward Active Mode.

LOW FREQUENCY MODEL OF CB BJT.

A capacitively coupled CB Amplifier is shown in Figure 6. It amplifies sinusoidal signal but blocks dc signal.

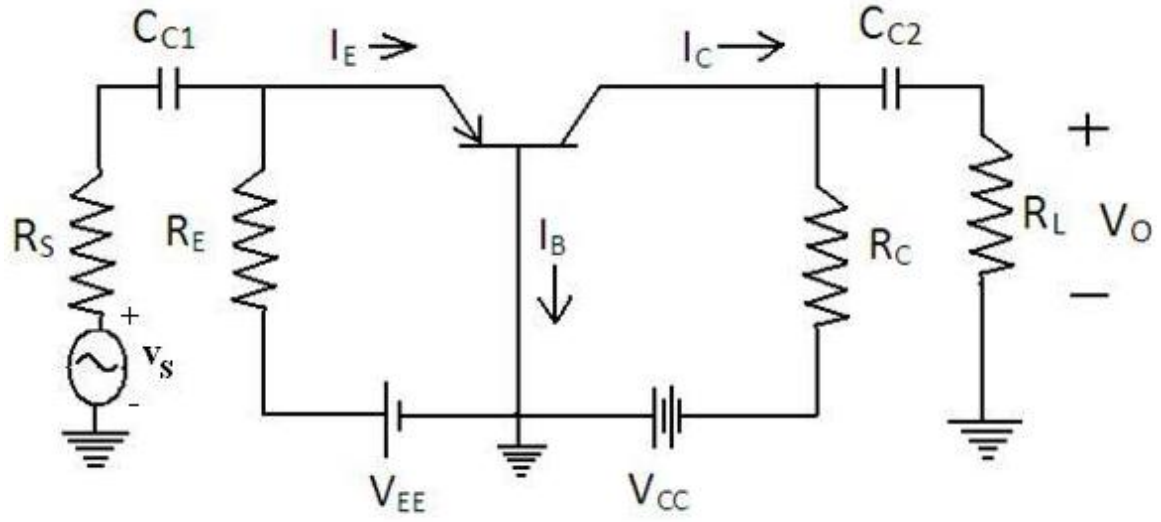


Figure 6. RC-coupled CB BJT Amplifier with two battery biasing.

Figure 12.6

In Figure 6 we have capacitively coupled source and capacitively coupled load in CB BJT.

In Figure 6 we show a CB BJT Amplifier. Because of near unilaterality of CB BJT (h_{rb} negligible), it is very suitable for RF tuned amplifiers. RF tuned amplifiers have a serious problem of parasitic oscillation because of output - input interaction and this interaction is due to h_r(reverse transmission factor).

CE BJT has $h_{re} = 10^{-4}$ hence CE BJT Amplifier is very prone to parasitic oscillations. But CB BJT has $h_{rb} = 10^{-5}$ hence CB BJT is the configuration of choice for implementing RF tuned amplifiers.

Also capacitive coupling is used because once a Quiescent Point or DC operating point is set up we do not want it to be disturbed by load or source. That is load and source must be a.c. coupled but d.c. decoupled. Capacitive coupling serves this end.

Capacitively coupled Amplifiers (CE, CB & CC) are always ac amplifiers. But inverting amplifiers made of Op Amp with dual power supply is a direct coupled amplifier. There are no coupling capacitors. Hence they are dc amplifiers. DC amplifiers can amplify from dc to high frequencies.

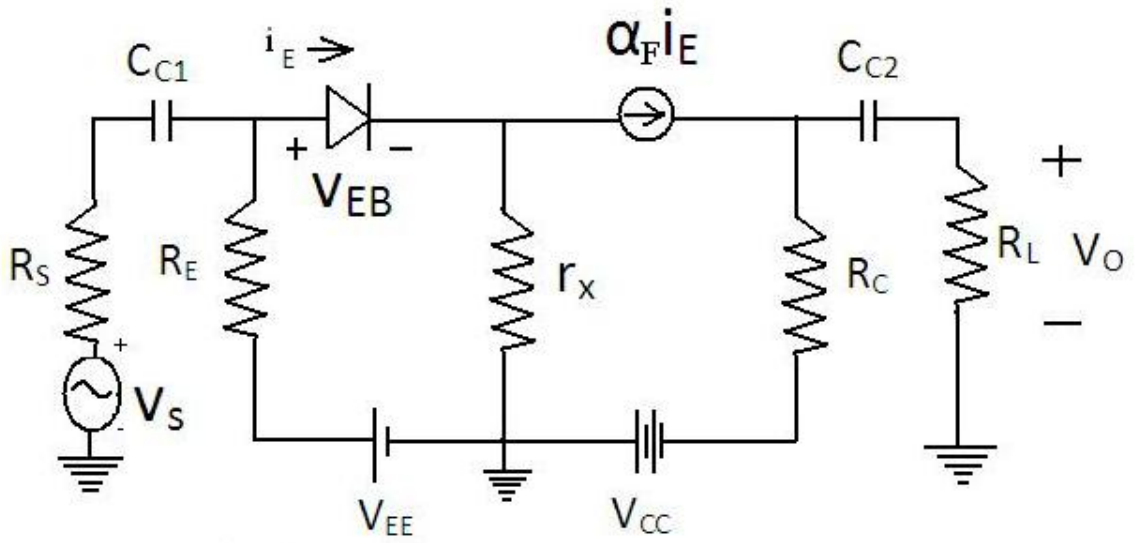


Figure 7. DC Model of CB BJT.

Figure 12.7

In Figure 7 we have the instantaneous model of CB Amplifier with signal coupled to it.

Therefore i_E (instantaneous emitter current) = I_E(emitter quiescent current) + i_e(emitter incremental current);

Similarly we have $i_C = I_C + i_c$ and $i_B = I_B + i_b$;

Also $I_C = \beta_F \times I_B$ and $i_c = \beta_f \times i_b$;

Here β_F = dc short circuit current gain and β_f = incremental short circuit current gain.

In BJT : $\beta_F = \beta_f$;

The instantaneous model also contains $r_x = r_{bb'}$ = base spreading resistance.

This is an ohmic resistance offered by the thin layer of P type silicon sand-witched between Emitter layer and Collector layer as shown in the cross sectional view of IC vertical npn BJT (Figure 8)

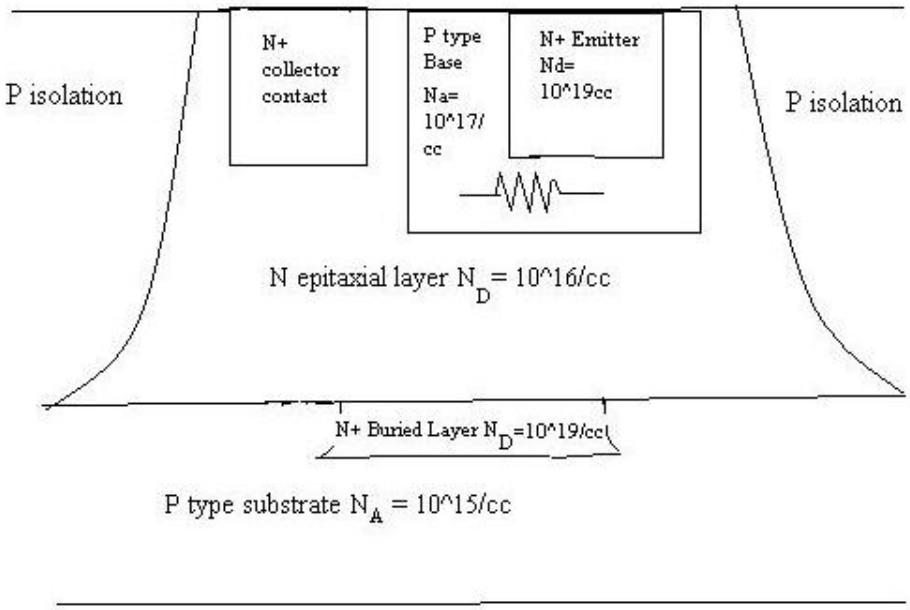


Figure 8 Cross-sectional view of Vertical NPN IC BJT.

Figure 12.8

Figure 8. Cross sectional View of Integrated Circuit Vertical NPN BJT.

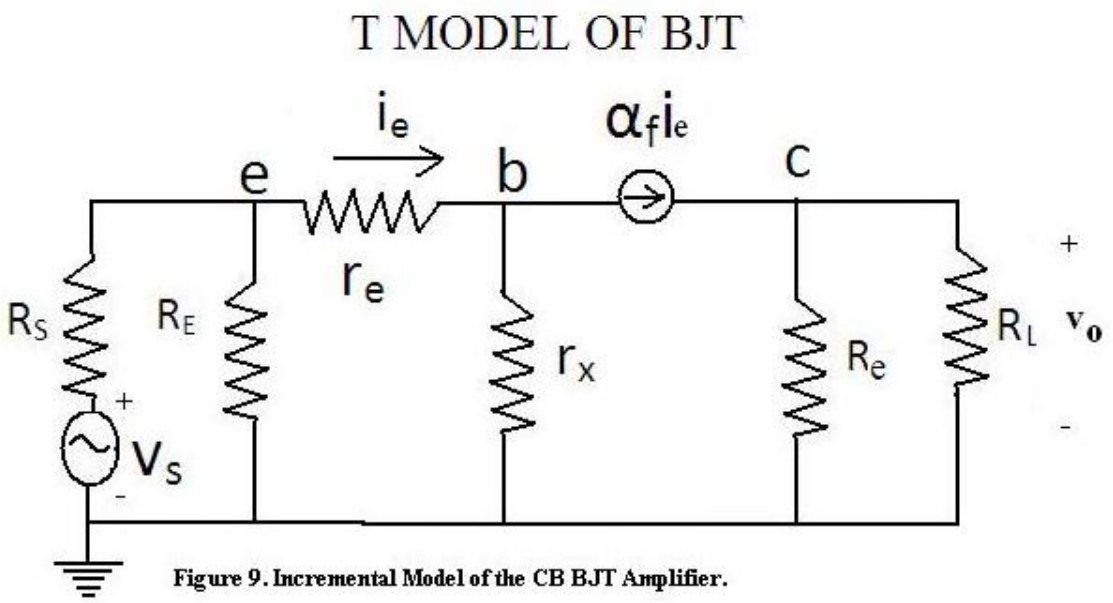


Figure 9. Incremental Model of the CB BJT Amplifier.

Figure 12.9

Figure 9. Incremental Model of CB BJT Amplifier.(the controlled current source is $\alpha_f i_e$).

This incremental model is known as the T-model of CB BJT.

As in incremental diode circuit, here also we short the DC Voltage Sources(V_{CC} and V_{EE}), we open circuit DC Current sources such as ($I_{CBO} + \alpha_F I_E$) but we retain the incremental current source $\alpha_f i_e$.

The coupling capacitances are shorted.

EB Diode is replaced by incremental resistance $r_e = (V_T/I_{EQ})$.

The ohmic resistances are retained as they offer resistance to DC as well as incremental component of the current.

HIGH FREQUENCY MODEL OF COMMON BASE BJT

Under high frequency condition the Junction Capacitances associated with the depletion layers EB and BC and Diffusion Capacitance associated with minority carriers stored in base region start effecting the performance of the BJT. These parasitic capacitances effect the Frequency Response as well as the short circuit current gain.

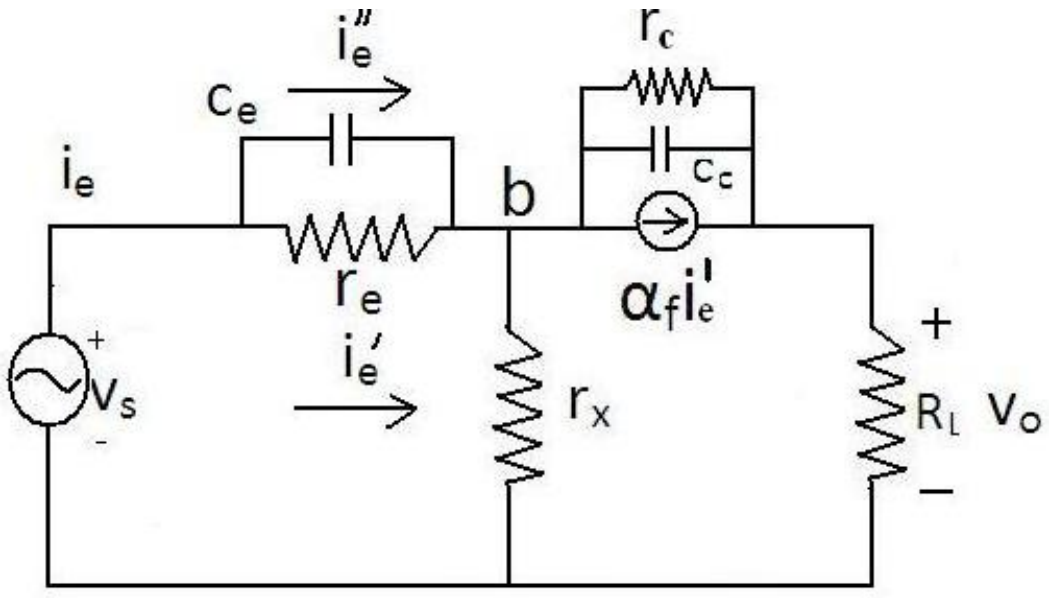


Figure 10. High Frequency T-model of CB BJT.

Figure 12.10

Figure 10. Incremental T-Model of the CB Amplifier Circuit at high frequency. (the controlled current source is $\alpha_f i_e$)

At high frequency diffusion and junction capacitances come into play.

$$C_e = C_{jEB} + C_D$$

Figure 12.11

$$C_c = C_{jBC} = C_{BO}$$

Figure 12.12

$= C_{BO}$ This is generally 5pF.

$$(C_D)(r_e) = \tau_t$$

Figure 12.13

C_D = more than 70pF.
Where

$$\tau_t$$

Figure 12.14

is the transit time across the base.

$$C_{jEB} = \frac{\epsilon_o \epsilon_r A_1}{d_{EB}}$$

Figure 12.15

$$C_{jBC} = \frac{\epsilon_o \epsilon_r A_2}{d_{BC}}$$

Figure 12.16

$$d_{EB}$$

Figure 12.17

= Depletion layer width at EB Junction

$$d_{BC}$$

Figure 12.18

=Depletion layer width at BC Junction

$$A_1$$

Figure 12.19

=Cross sectional area of EB junction

$$A_2$$

Figure 12.20

=Cross sectional area of BC junction

$$i_e = i_e' + i_e''$$

Figure 12.21

Here

i_e'

Figure 12.22

is the useful transistor current which controls the output current sources ($\alpha_{fo} i_e'$)and

i_e''

Figure 12.23

is the parasitic current.

i_e''

Figure 12.24

has no role to play in the transistor action

---

i_e'' *does not contribute to transistor action .*

Figure 12.25

α_{fo}=short circuit incremental forward current transfer ratioat low frequency.

$$v_o = \left(\alpha_{fo} i_e' R_L\right)$$

Figure 12.26

This is true only when we consider r_c = infinity and C_C to be open.
This means this model is valid only till

ω_T

Figure 12.27

/3. Because only till

ω_T

Figure 12.28

/3 the above assumption is valid. Above

ω_T

Figure 12.29

/3 this model gives incorrect result.

$$i'_e = \frac{i_e}{\left(r_e + \frac{1}{j\omega C_e}\right)} \times \frac{1}{j\omega C_e}$$

Figure 12.30

$$i'_e = \frac{i_e}{(1 + j\omega r_e C_e)}$$

Figure 12.31

$$v_o = \frac{\alpha_{fo} i_e}{(1 + j\omega r_e C_e)} R_L$$

Figure 12.32

$$i_c = \frac{\alpha_{fo} i_e}{1 + j\left(\frac{\omega}{\omega_\alpha}\right)}$$

Figure 12.33

$$\alpha_f = \frac{\alpha_{fo}}{1 + j\left(\frac{\omega}{\omega_\alpha}\right)}$$

Figure 12.34

Here α_f = short circuit current transfer ratio at all frequencies for CB BJT.

$$Here\ \omega_\alpha =$$

Figure 12.35

alpha cut-off frequency

$$\omega_\alpha = \frac{1}{C_e r_e}$$

Figure 12.36

$$\omega_\alpha \sim \frac{1}{\tau_t} = \omega_T$$

Figure 12.37

Here

$$\omega_T$$

Figure 12.38

Figure 12.39

is the transit frequency and

τ_t

Figure 12.40

Figure 12.41

is the transit time.
The Bode Plot of the above expression of

α_f

Figure 12.42

is given in Figure 12.

Chapter 13

AnalogElectronics_Lecture4_PartB_low and high frequency model of CE BJT.[1]

AnalogElectronics_Lecture4_PartB_low and high frequency model of CE BJT.
INCREMENTAL MODEL OF CE BJT FROM T MODEL OF CB BJT

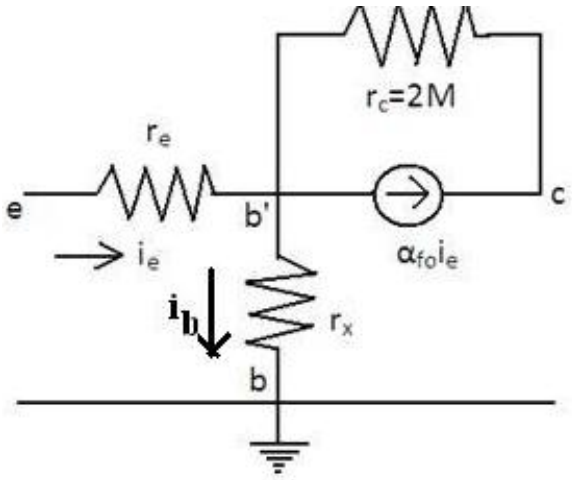


Figure 11a. The T-model of CB BJT.

Figure 13.1

Figure 11a. Low Frequency Incremental T Model of CB BJT.
Let us re-orient this as CE configuration.

[1] This content is available online at <http://cnx.org/content/m31035/1.1/>.

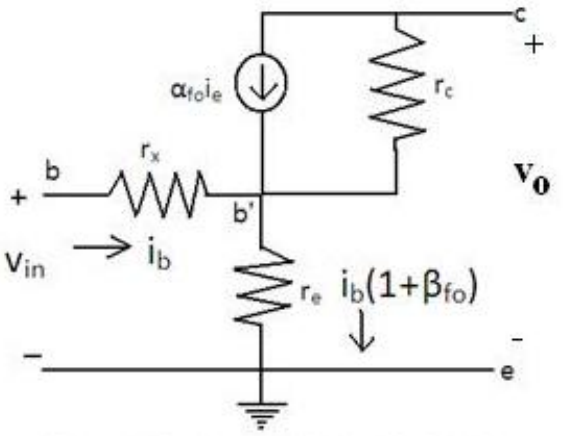


Figure 11b. Reoriented T-model of CB BJT.

Figure 13.2

Figure 11b. The reoriented T Model to represent CE BJT.

It should be noticed that in T-Model under normal orientation has controlled current($\alpha_f i_e$) coming out of collector node since base current is coming out of base node. But in reoriented T Model controlled current($\alpha_f i_e$) coming into collector node since base current is coming into base node.

Input Mesh Equation:

$$v_{in} = i_b \times r_x + (i_b(1+\beta_{fo})r_e)$$

Figure 13.3

$$v_{in} = i_b[r_x + (1+\beta_{fo})r_e]$$

Figure 13.4

$$(1+\beta_{fo})r_e = r_\pi = \frac{\beta_o}{g_m}$$

Figure 13.5

Where g_m = trans conductance = I_C/V_T whereas $r_e = V_T/ I_E$ and $I_C = \alpha_F I_E$

$$v_{in} = i_b[r_x + r_\pi]$$

Figure 13.6

The output current is =

$$i_C = \alpha_{fo} i_e = \beta_{fo} i_b$$

Figure 13.7

Here

$$\beta_{fo} = \frac{\alpha_{fo}}{1-\alpha_{fo}} \text{ or } \alpha_{fo} = \frac{\beta_{fo}}{1+\beta_{fo}}$$

Figure 13.8

.

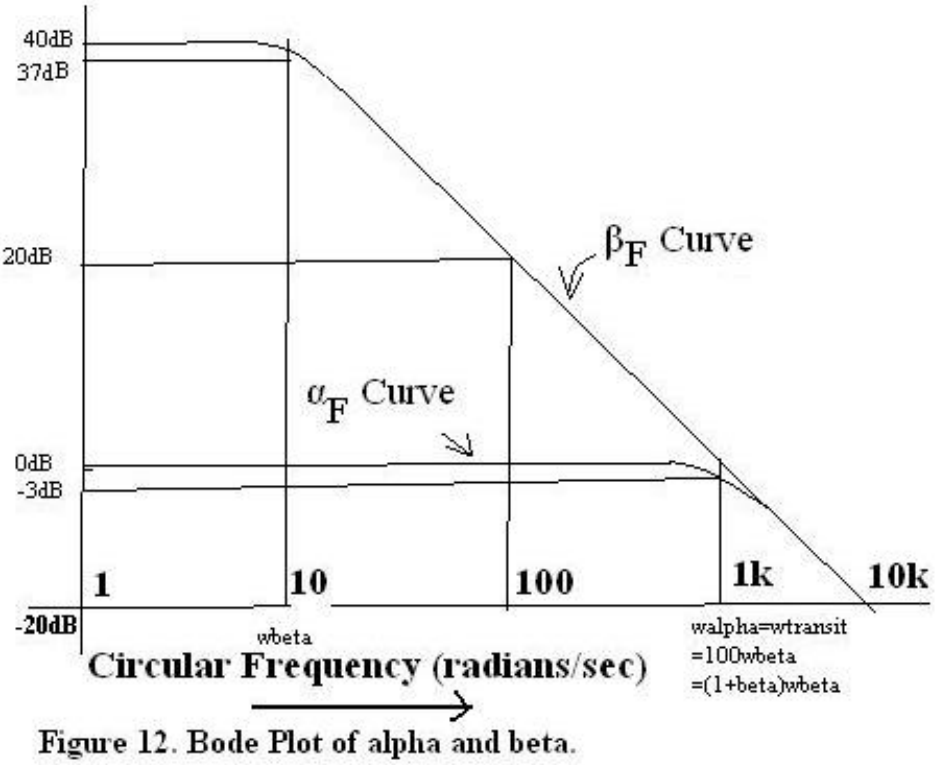


Figure 13.9

Figure 12. Bode Plot of beta and alpha and location of ω_β and ω_α.
Beta cutoff frequency = ω_β and alpha cutoff frequency = ω_α .
Cut-off frequency = -3dB frequency
= this is the frequency where parameter falls to 0.707 of its flat band value or midband value
= corner frequency
= half power frequency

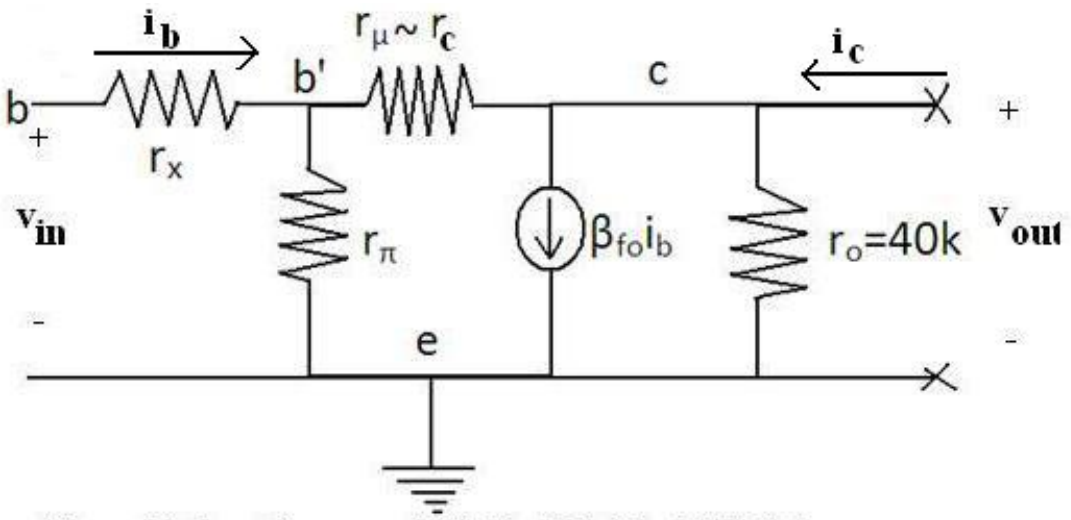


Figure 13. Low Frequency Hybrid-pi Model of CE BJT.

Figure 13.10

Figure 13. Low Frequency Hybrid-π Model of CE BJT.

$$r_o = \left(\frac{r_c}{1+\beta_o}\right)$$

Figure 13.11

This is due to EARLY EFFECT or due to Base Width Modulation. A parameter Early Voltage V_A is used for determining the output impedance of the hybrid $-\pi$ Model. This output impedance is $1/h_{oe}$. The definition of Early Voltage V_A is given in Figure 14.

$$r_0 = \frac{1}{slope} = \frac{1}{\frac{I_{CQ}}{V_A + V_{CEQ}}}$$

$$r_o = \frac{V_A + V_{CEQ}}{I_{CQ}}$$

Figure 13.12

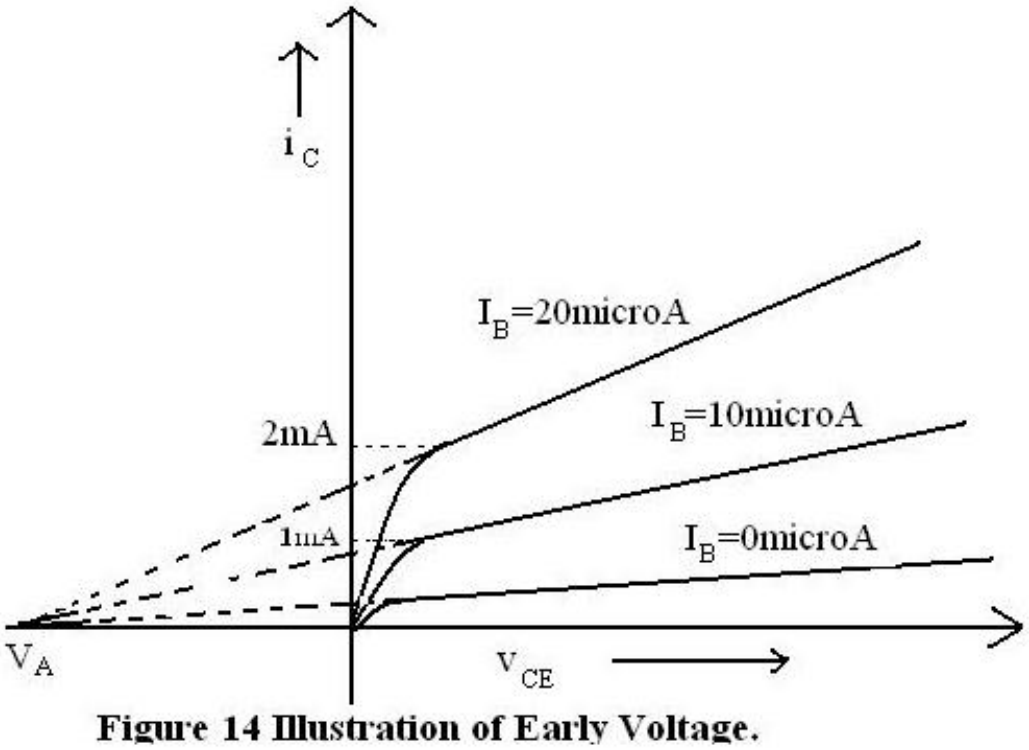


Figure 13.13

Figure 14. The definition of Early Voltage for a CE BJT.

COMPARISON BETWEEN HYBRID-pi MODEL OF CE BJT AND T MODEL OF CB BJT

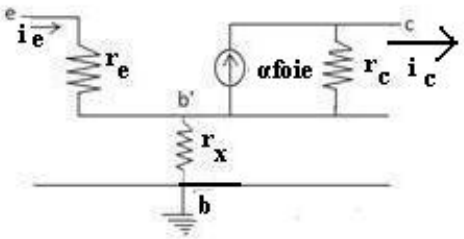


Fig15a. T-Model of CB BJT.

Figure 13.14

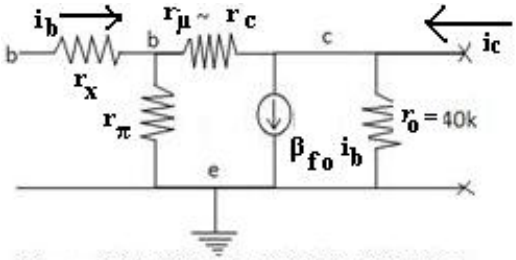


Figure 15b. Hybrid-pi Model of CE BJT.

Figure 13.15

T-model of CB BJT	Hybrid-pi Model of CE BJT
Unilateral model	Non Unilateral model
$h_{rb}=\frac{r_x}{r_c}=\frac{100}{10M}=10^{-5}$	$h_{re}=\frac{r_\pi}{r_\mu}=\frac{10^3}{10^7}=10^{-4}$

Table 13.1

In CB BJT,if we consider base spreading resistance to be zero then

$$h_{ib} = r_e \quad h_{rb} = 0 \quad h_{fb} = -\alpha_{fo} \quad h_{ob} = \frac{1}{r_c}$$

$$\frac{v_o}{v_{in}} = \frac{\alpha_{fo} i_e R_L}{i_e r_e} = \alpha_{fo} \frac{R_L}{r_e} = A_{Vo}$$

$$R_{in} = r_e$$

Figure 13.16

$$R_{out} = r_c = \frac{1}{h_{ob}} = 10M$$

Figure 13.17

For CE BJT if we consider r_μ to be infinity then:

$$h_{ie} = r_x + r_\pi, h_{re} = 0, h_{fe} = +\beta_{fo},$$

Figure 13.18

$$h_{oe} = \frac{1}{r_o}$$

$$r_o = \frac{V_A + V_{CEQ}}{I_{CQ}}$$

$$v_o = -\left(\beta_{fo} i_b\right)(R_c \,||\, r_o)$$

Figure 13.19

$$\frac{v_o}{v_{in}} = \frac{(-\beta_{fo})(R_c \,||\, r_o)}{r_x + r_\pi}$$

$$A_{vo} = -g_m(R_c \,||\, r_o)$$

$$R_{in} = r_x + r_\pi$$

$$R_{out} = r_o$$

Figure 13.20

Incremental model at high frequency

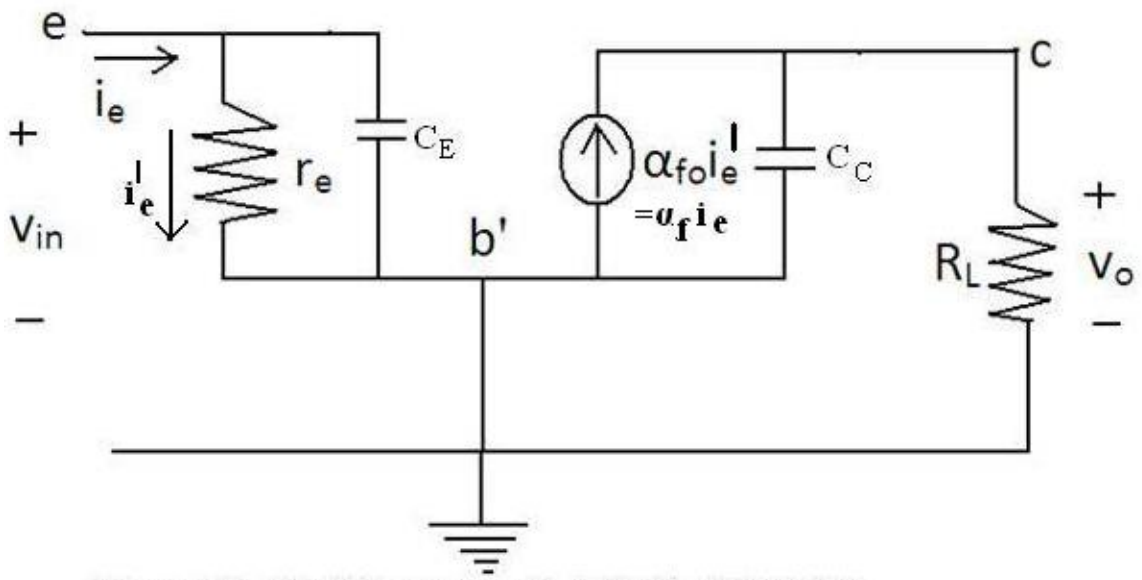


Figure 16. High Frequency T - Model of CB BJT.

Figure 13.21

Figure 16. High frequency T-Model of CB BJT.

$$\alpha_f = \frac{\alpha_{fo}}{1 + i\left(\frac{\omega}{\omega_\alpha}\right)}$$

$$\omega_\alpha \; is \; the \; \alpha \; cutoff \; frequency$$

$$\omega_\alpha \sim \omega_T = \frac{1}{\tau_t}$$

Figure 13.22

$$C_e = C_{jE} + C_D$$

$$\omega_\alpha = \frac{1}{r_e\left(C_{JE} + C_D\right)}$$

$$C_{jE} \ll C_D$$

$$\therefore \omega_\alpha = \frac{1}{r_e C_D}$$

Figure 13.23

$$\omega_\alpha = \frac{1}{\tau_t} = \omega_T \text{ (Transit Frequency)}$$

Where τ_t is the transit time.

Figure 13.24

Here τ_t is the transit time taken by the minority carriers to cross the base width. The mechanism of transit is both diffusion and drift.

Now let us consider CE BJT at high frequency:

Here β_f (short circuit current gain in CE BJT) is arrived at in exactly the same manner as α_f was arrived at in CB BJT.

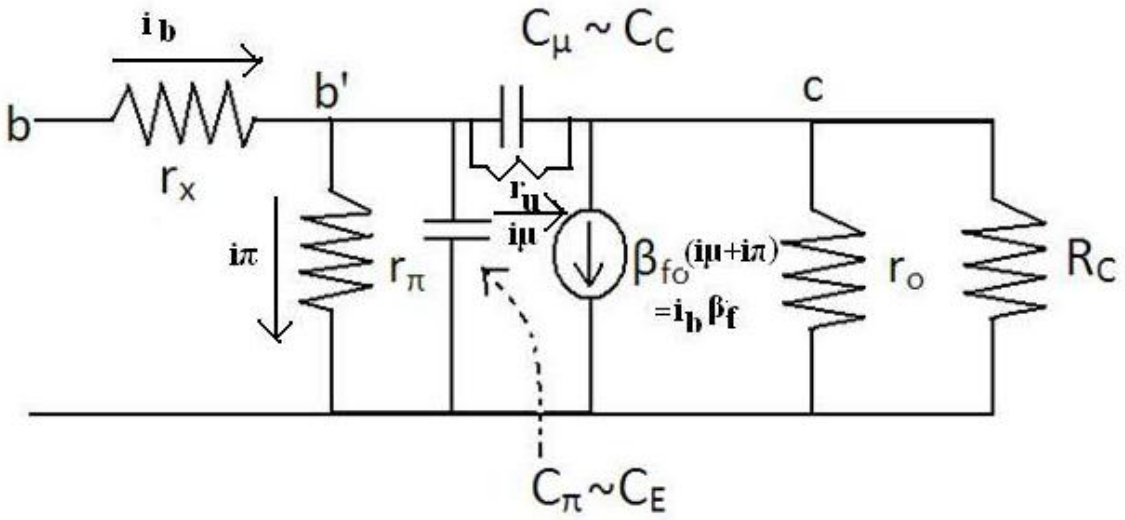


Figure 17. High Frequency Hybrid-pi Model

Figure 13.25

Figure 17. High Frequency Hybrid-π Model of CE BJT.

$$\beta_f = Short\ circuit\ current\ gain$$

$$\beta_f = \frac{\beta_{fo}}{1 + i\frac{\omega}{\omega_\beta}}$$

Where ω_β=β cutoff frequency=$\frac{1}{r_\pi(C_\pi+C_\mu)}$

Figure 13.26

$$= \frac{1}{\frac{\beta_o}{g_m}C_\pi} = \omega_\alpha/(1+\beta_0)$$

Here we neglect C_μ assuming $C_\pi \gg C_\mu$.

Figure 13.27

Chapter 14

AE_Lecture4_PartD1_Time_Domain_Respor

Analog Electronics_Lecture4_PartD
Experimental Methods of measuring
the Frequency Band-Width of an Amplifier.
There are two methods of determining the frequency Band Width (BW) of any amplifier:

a. Frequency Domain Response method and
b. Time Domain Response Method.

Frequency Domain Response

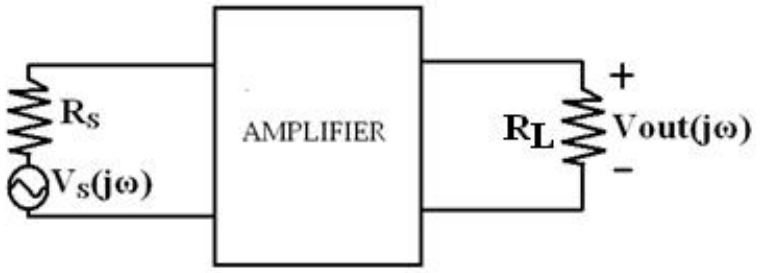


Figure 1. Set up for measuring the steady state sinusoidal frequency response of an amplifier.

Figure 14.1

Figure 1. Block Diagram of an Electronic System(Amplifier) connected to the source at the Input and to the Load at the Output.

[1]This content is available online at <http://cnx.org/content/m31472/1.1/>.

$$A_V(j\omega) = \frac{V_{out}(j\omega)}{V_{in}(j\omega)}$$

Figure 14.2

Plot of

$$|A_V(j\omega)|$$

Figure 14.3

vs Frequency - magnitude frequency response ;
Plot of

$$\angle A_V(j\omega)$$

Figure 14.4

vs frequency - phase angle frequency response.
Both together constitute the Frequency domain response.

Time Domain Response

When we apply square wave and measure the rise time(t_r) at high frequency and measure the sag (10% sag frequency) at low frequency then we say that we are looking at time domain response.

1. Rise Time Method of determining the upper -3dB frequency.

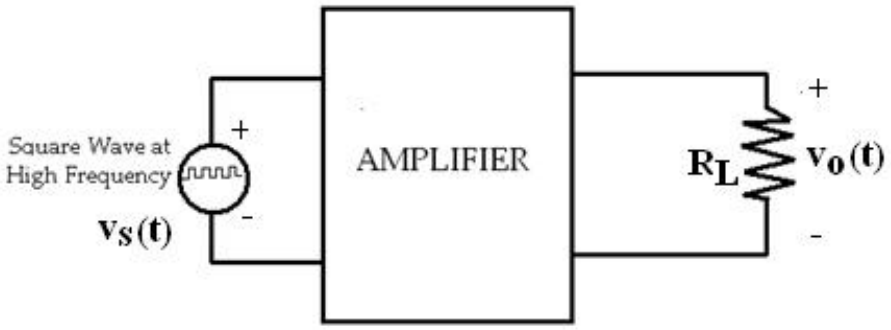


Figure 2. Set up for studying the Time Domain Respose of an Amplifier.

Figure 14.5

Figure 2. Square Wave Input into an amplifier gives a response from which Time Domain studies can be done.

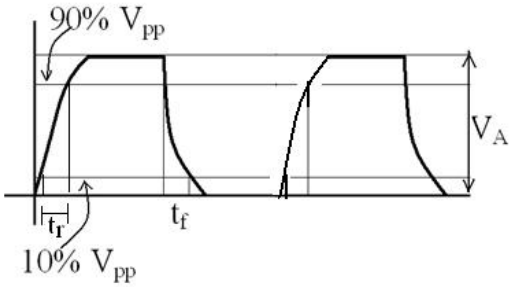


Figure 3. A square wave passing through a Low Pass Filter experiences the rounding off of the leading and lagging edges because LPF suppresses high frequency components and high frequency components constitute the edges and low frequency components constiotute the top and bottom of the square wave.

Figure 14.6

Figure 3. Square Wave Response of an Amplifier at high frequencies. Because of upper -3dB frequency the leading and lagging edges get rounded off. At the leading edge rise time and at lagging edge fall time is introduced.

$$t_{r_o} = \frac{t_r + t_f}{2}$$

$$f_h t_{r_o} = 0.34$$

$$f_h = \frac{0.34}{t_{r_o}} = The\ upper\ (-3\ dB)\ frequency$$

Figure 14.7

NOTE: At the leading edge we measure the rise time and at the lagging edge we measure the fall time.

1. **DETERMINATION OF LOWER -3dB FREQUENCY(f L) BY TIME DOMAIN METHOD**

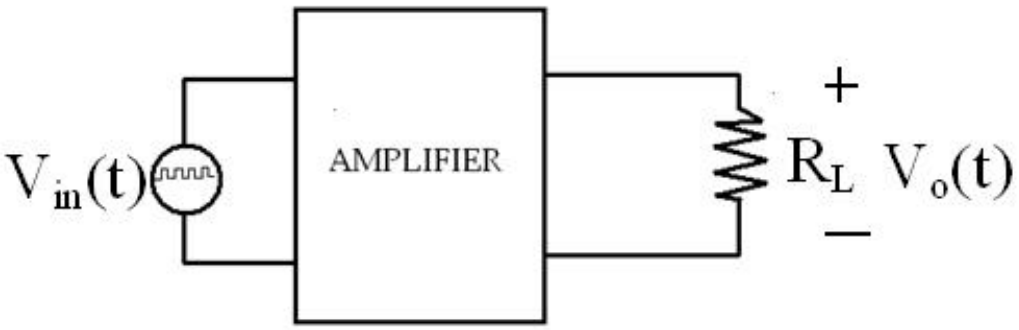


Figure 4. Set up for measuring the Time Domain Response at low pulse repetition frequency. If the amplifier has a High Pass Filter characteristics then sag will appear at the top and bottom of the square wave response.

Figure 14.8

Figure 4. Square Wave Response of the Amplifier at low frequencies gives a sag at the top and bottom as shown below.

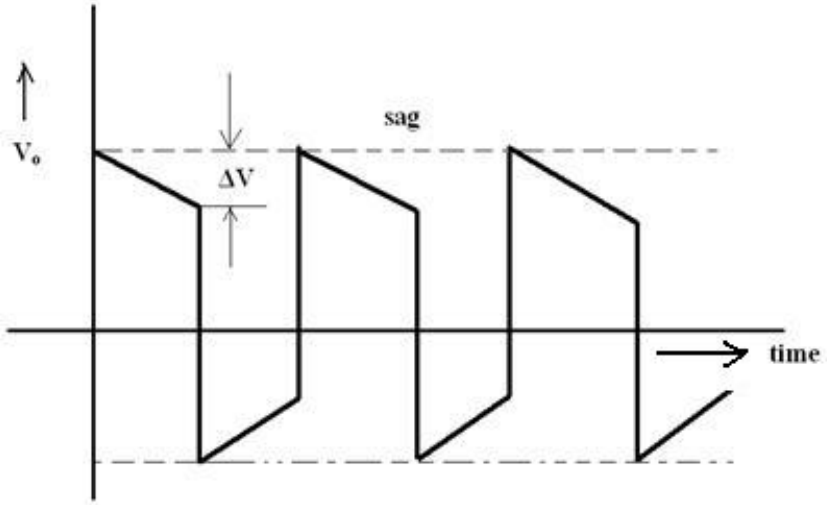


Figure 5. A square wave passing through HPF will lose its DC component and will experience a sag at the top and bottom of the square wave. But this sag will be evident only at low square wave frequencies.

Figure 14.9

Figure 5. Square Wave Response of the Amplifier at low frequencies. % Sag = (ΔV/V 0)$\times$100 where V 0 is peak to peak amplitude and ΔV is the tilt at the top or at the bottom.
(ΔV/V 0)$\times$100 = % sag.
The p.r.f is adjusted to f* to obtain 10% ag then f L = (0.1f*/π).
Where f L = lower -3dB frequency.

High frequency suppression leads to the rounding off the leading and the lagging edges of the square wave.

Low frequency suppression leads to the sag of the top and bottom of the square wave.

Chapter 15

AE_Lecture4_PartD2_Line Spectrum of a Pulse Train.[1]

Analog Electronics_Lecture4_PartD
Experimental Methods of measuring
the Frequency Band-Width of an Amplifier.

1. FREQUENCY SPECTRUM OF A PULSE TRAIN.

Let us look at the spectrum of a pulse train

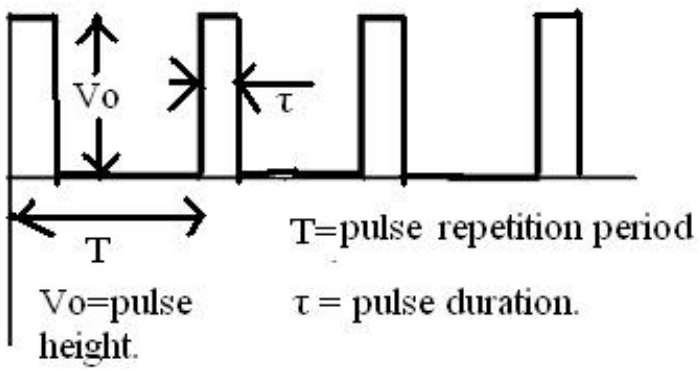


Figure 6. A pulse train with an offset of (Vo.τ)/T , pulse duration τ, pulse repetition period T , pulse repetition frequency (1/T) and duty ratio or duty cycle equal to τ/T. In a square wave duty ratio is 50%.

Figure 15.1

[1] This content is available online at <http://cnx.org/content/m31495/1.1/>.

Figure 6. A pulse train, offseted with respect to the time axis.

In the above Figure we represent a pulse train of Pulse Repetition Frequency = 1/T
and duty cycle of $(\tau/\mathrm{T})\times 100$ percent and pulse duration of τ secs and pulse height of Vo.
Let us find out the FOURIER SERIES EXPANSION of the pulse train shown in the above figures.
FOURIER SERIES METHOD states that :
Any time periodic function contains a D.C. component , contains a fundamental frequency $f_o = (1/T)$ and its harmonics.

$$\tilde{V}(e^{j\omega}) = Series\ Summation$$

$$= a_o + \sum_{n=1}^{N} a_n \cos n\omega_o t + \sum_{m=1}^{M} b_m \sin m\omega_o t$$

$$a_o = d.c.component$$

$$a_n = Amplitude\ of\ the\ nth\ cosine\ harmonic$$

$$b_m = Amplitude\ of\ the\ mth\ \ sine\ harmonic$$

This is the single sided frequency spectrum of the periodic function=$\tilde{V}(t)$

Engineers and Scientists all over the world use the double-sided spectrum.

$$\cos\theta = \frac{e^{j\theta} + e^{-j\theta}}{2}$$

Figure 15.2

In terms of phasors(a rotating vector)

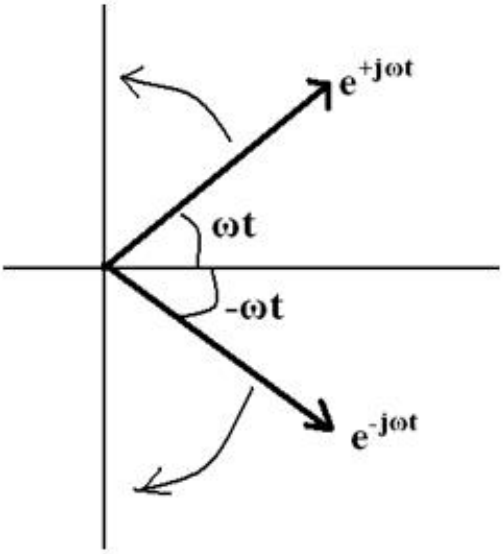


Figure 7. Here we show two rotating vectors also known as phasors. Anti-clockwise phasor is making positive phase angle with respect to the x axis and Clockwise phasor is making negative angle. All phasors start from X-axis. By phasor diagram it becomes simple to analyze R,L,C circuit with steady state sinusoidal input.

Figure 15.3

Figure 7. Two oppositely rotating vectors are shown. These rotating vectors are known as Phasors.

$e^{j\omega t}$ is a positively rotating phasor and $e^{-j\omega t}$ is a negatively rotating phasor

Periodic function has a very simple series expansion in terms of phasors.

$$\tilde{v}(t) = \sum_{n=-\infty}^{\infty} a_n e^{jn\omega_o t}$$

Figure 15.4

Here $a_n = a_{-n}$ are magnitudes of the nth Harmonic oppositely rotating phasors.
This gives the double sided spectrum.

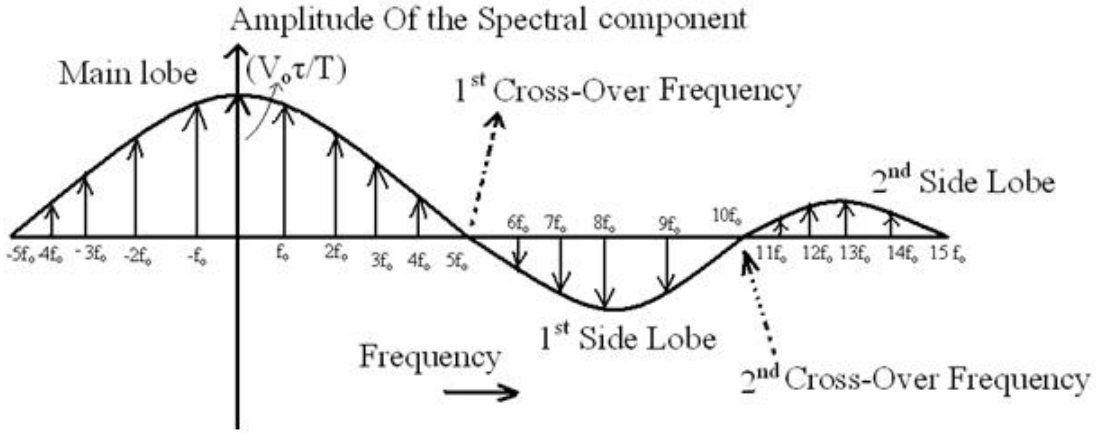


Figure 8. Double-sided frequency spectrum of a pulse train of duration τ and T/τ=5; 1/T=fo; 1/τ=5/T=5fo. Note that cross over occurs at the reciprocal of duration and multiples of reciprocal of duration i.e. at 1/τ , 2/τ . 3/τ . Also note that if pulse train becomes an implse train then τ = 0 and cross over will occur at infinity and Sinc Function envelope will become a flat envelope. Hence the frequency spectrum of impulse train is an uniform spectrum with equal height spectral components.

Figure 15.5

Figure 8. Frequency Spectrum of a pulse train.

Here we assume that $\frac{T}{\tau} = 5$; $\frac{1}{T} = f_o$; $\frac{1}{\tau} = \frac{5}{T} = 5f_o$

Envelope of the tip of the spectral component $= \frac{\sin\theta}{\theta} = sinc\,\theta$

$$\theta = \left(2\pi\left(\frac{\tau}{T}\right)n\right)$$

Figure 15.6

A signal has a frequency spectrum. For a periodic signal we use FOURIER SERIES techniques. For a non-periodic signal we use FOURIER-TRANSFORM techniques.

If a signal passes through an infinite Band Width system we are able to maintain 100% FIDELITY in reproducing the signal on the output of the system. This is why a wide-band musical system is called a Hi-Fi System. Here Hi-Fi is HIGH FIDELITY. But if we pass a complex signal through a finite B.W. System inevitably there will be suppression of frequency on the high frequency end of the spectrum as well as on the low frequency end of the spectrum .This leads to FREQUENCY DISTORTION as well as PHASE DISTORTION.

Chapter 16

AE_Lecture4_PartD3_Time Domain Response of Low Pass Filter.[1]

Analog Electronics_Lecture4_PartD2
Experimental Methods of measuring
the Frequency Band-Width of an Amplifier.

1. Study of R-C Low Pass Filter.

[1] This content is available online at <http://cnx.org/content/m31504/1.1/>.

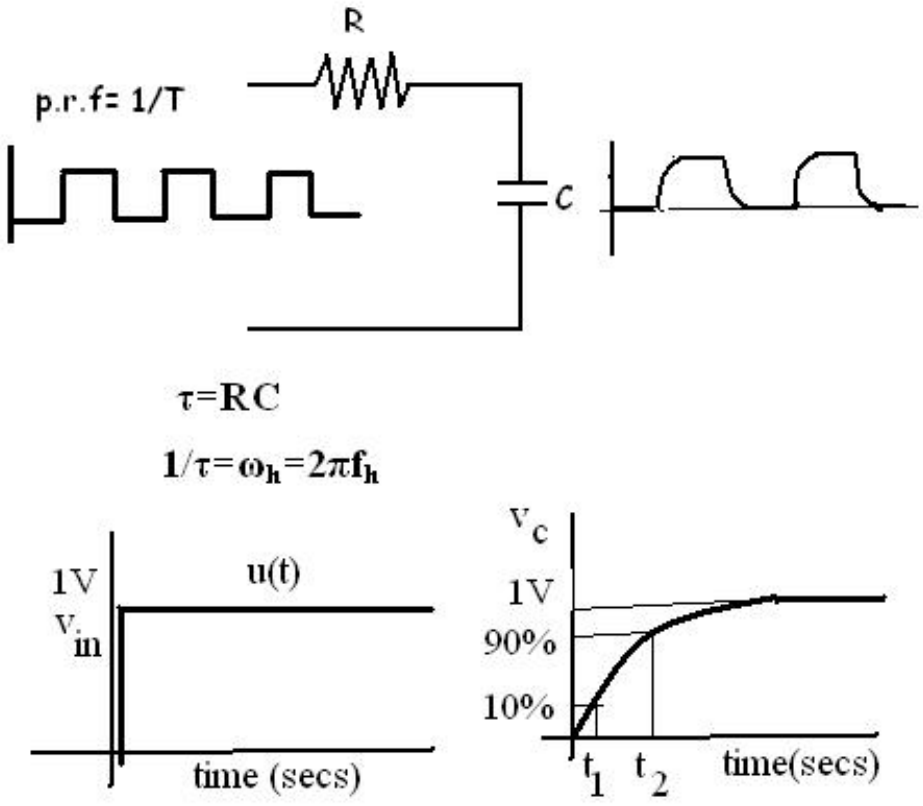


Figure 9. Square wave response and step response of RC-Low Pass Filter.

Figure 16.1

Figure 9. The circuit diagram of a R-C Low Pass Filter.

In Figure 9, the square wave response as well as the step response of R-C Low Pass Filter is shown.
The Step Response of LPF = $v_c(t)$ = charging of the capacitor = [1- Exp(-t/τ)];
The final voltage across the capacitor is 1V since unit step voltage u(t) is the input.
10% of 1V = 0.1= [1- Exp(-t_1/τ)]; A
90% of 1V = 0.9 = [1- Exp(-t_2/τ)]; B
From Eq(A) and (B) we get:
t_2 - t_1 = t_r = 2.2τ = 2.2/ω_h
Therefore **tr×fh = 0.35**

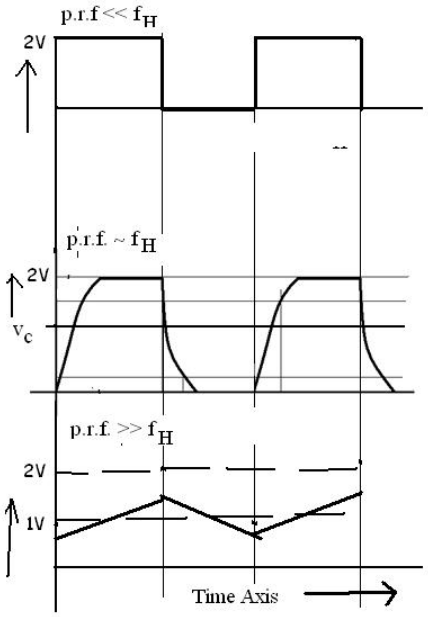


Figure 10. Square wave response of LPF at different prf. Note that at very high prf, LPF behaves like an integrator. Square wave is lost. Only the DC component is retained.

Figure 16.2

Figure 10. Square Wave Response(also known as Time Domain Response) of R-C LPF.

By inspection we find that

when prf $\ll f_H$ then we have faithful reproduction of the square wave;

when prf $\sim f_H$ then we have rise time and fall time effect at the leading and lagging edges respectively;

when prf $\gg f_H$ then we get the average value of the square wave. In this case we get about 1V.

Hence at frequencies much higher than the cutoff frequency of LPF, the filter behaves like an integrator. The positive flat top becomes a positive sloped ramp and negative flat top becomes a negative sloped ramp.

Above 30 Hz our RETINA acts as an integrator.

4.1 The Frequency Response of a Low Pass R-C Filter

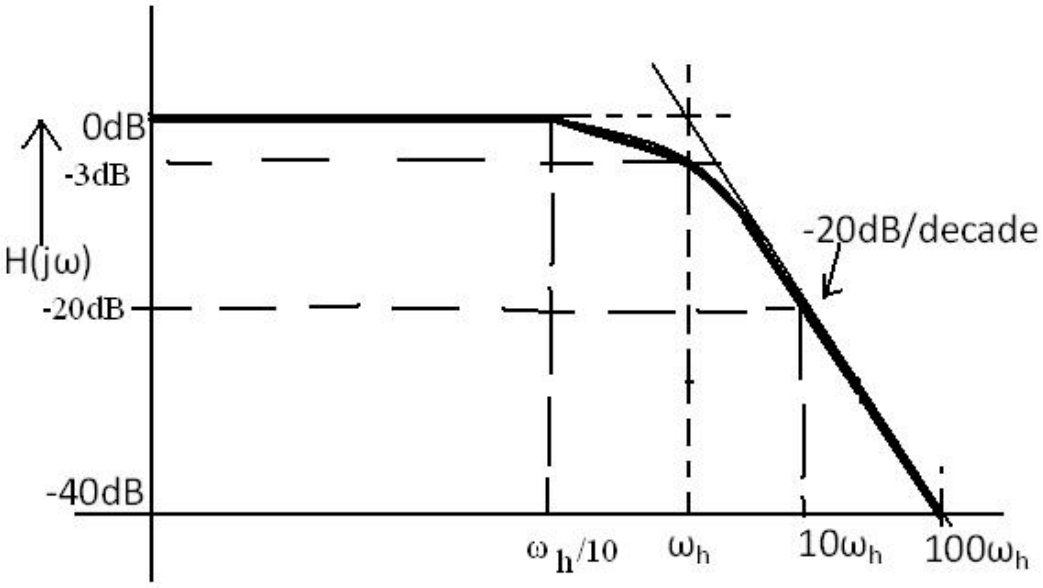


Figure 11. Bode plot of the steady state sinusoidal frequency response magnitude. Note that skirt is -20dB/decade. Since it has one cut-off or one corner frequency it is called First-order system. First order system will have a skirt of -20dB per decade. Nth order system will have N corner frequencies and -20NdB/decade skirt.

Figure 16.3

Figure 11. Magnitude of the transfer function-Frequency Response of a LPF.

$$V_{in}(j\omega) = I(j\omega)\left(R + \frac{1}{j\omega C}\right)$$

Figure 16.4

$$V_{out}(j\omega) = I(j\omega)\left(\frac{1}{j\omega C}\right)$$

Figure 16.5

$$\frac{V_{out}(j\omega)}{V_{in}(j\omega)} = H(j\omega) = \frac{1}{\left(1 + j\frac{\omega}{\omega_h}\right)}$$

Figure 16.6

(1)

$$\omega_h = \frac{1}{RC}$$

Figure 16.7

Equation (1) has a zero at infinity and a pole at

$$\omega_h$$

Figure 16.8

. Hence it has -20dB asymptote at

$$\omega_h$$

Figure 16.9

. This gives 100% transmission below

ω_h

Figure 16.10

and suppression of frequencies higher than

ω_h

Figure 16.11

at the rate of 20dB per decade as we move up the frequency scale .

The Time-Domain Response at high frequencies and Frequency Response of a LPF are related to each other through the relation:

$$t_r f_h = 0.35$$

Figure 16.12

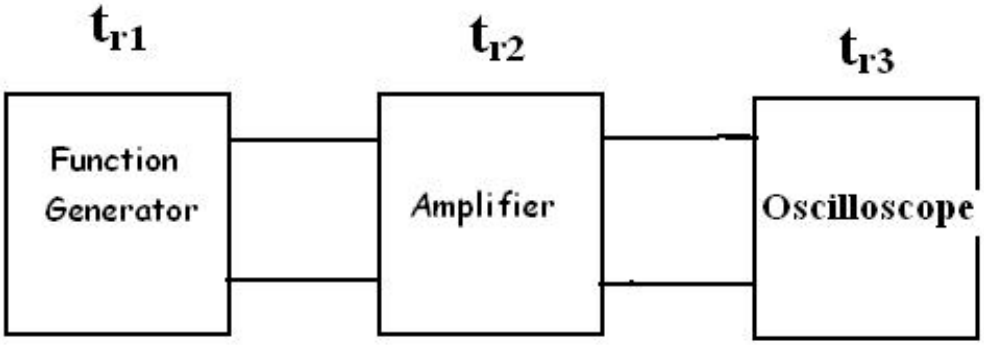


Figure 12. In a typical measurement set up the final rise time measured is the sun total effect of the rise times inherently present in different subsystems such as signal source and Oscilloscope. While trying to measure the rise time of an Amplifier, the rise times effect of the signal source and oscilloscope will have to be isolated to obtain the true rise time of the amplifier.

Figure 16.13

Figure 12. The estimation of the overall rise time as observed in the Oscilloscope. The overall rise time will be influenced by the rise time of the oscilloscope as well as that of the source.

$$(t_r)_{overall} = \sqrt{(t_{r_1})^2 + (t_{r_2})^2 + (t_{r_3})^2}$$

$$f_{h_2} t_{r_2} = 0.35$$

Figure 16.14

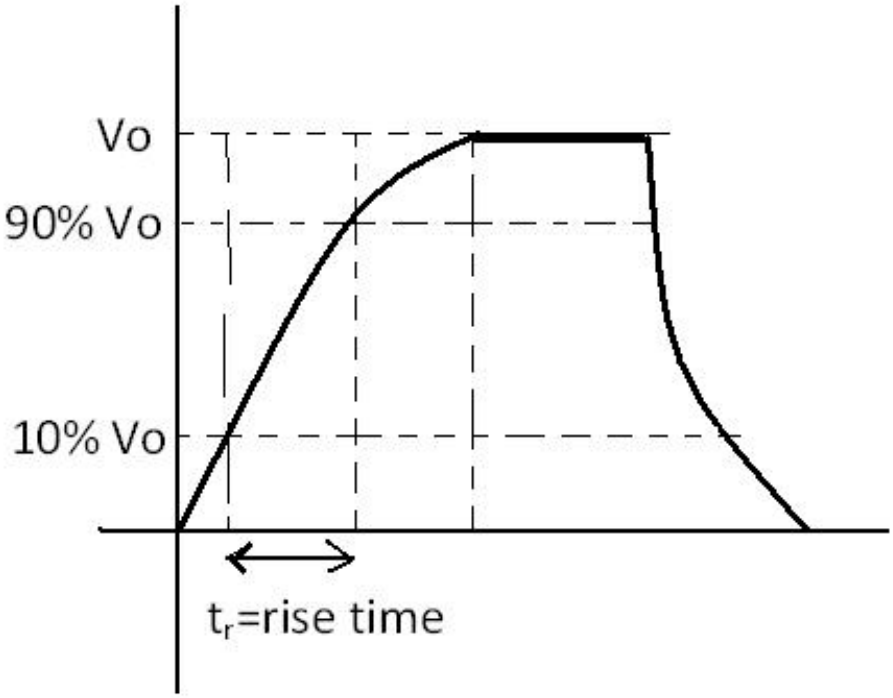


Figure 13. We define rise time as time taken by the leading edge to rise from 10% of Vo to 90% of Vo. Similarly fall time is defined.

Figure 16.15

Figure 13. Definition of the rise time.

Chapter 17

AE_Lecture4_PartD4_Time Domain Response of High Pass Filter.[1]

1. The study of a C-R High Pass Filter.

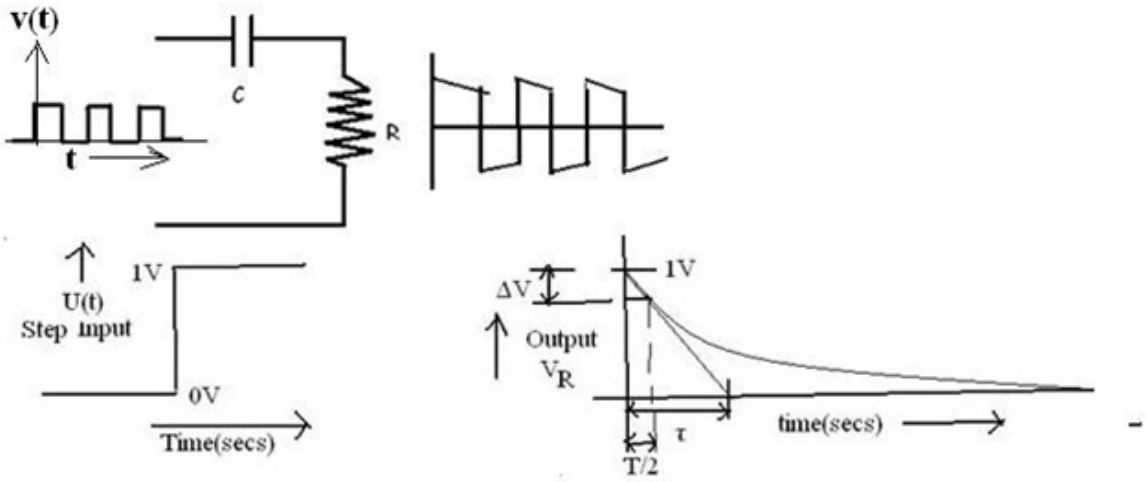


Figure 14. Square wave response and step response of a high pass filter. Note at the output d.c. component is completely blocked.

Figure 17.1

Figure 14. The circuit diagram of C-R high Pass Filter and square wave response.

[1] This content is available online at <http://cnx.org/content/m31505/1.1/>.

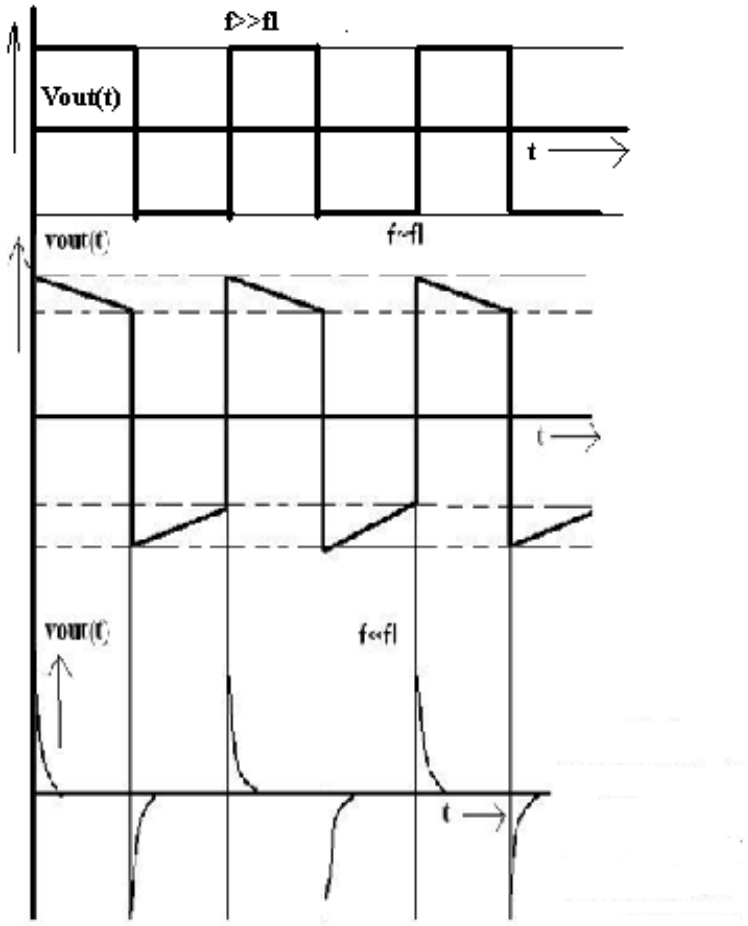


Figure 17.2

Figure 15. The Square Wave Response or Time Domain Response of HPF.

In Figure 14, the square wave response as well as the step response of C-R High Pass Filter is shown.

The slope of the tangent drawn to the exponentially decaying curve at t=o is:

$d(v_R)/dt|_{t=0}$ = (1V/τ sec) ;

Two triangles shown are similar hence:

$\Delta V/(T/2)$ = (1V/τ sec) ;

Or $\Delta V/1V$ = fractional sag = $T/(2\tau)$;

We have to adjust the frequency of the periodic square wave to achieve 10% sag;

Say the frequency of 10% sag is f*= 1/T where T is the period of repetition.

Therefore $T=(2\tau) = 0.1= (2\pi f_L)/(2f^*)$; since $1/\tau = \omega_L = 2\pi f_L$.

Therefore $\mathbf{fL = (0.1f^*)}/\pi$

In figure 15, the square wave response is shown.

By inspection we find that

when prf $\gg f_L$ then we have faithful reproduction of the square wave except that the dc component is blocked by the series capacitance;

when prf $\sim f_L$ then we have sag effect at the top and bottom of the square wave;

when prf $\ll f_L$ then we get the differentiation of the leading and lagging edge. Since the leading edge and lagging edge are positive step and negative step, we get positive impulse and negative impulse at the instants where step voltages had occurred.

Hence at frequencies much lower than the cutoff frequency of HPF, the filter behaves like a differentiator.

5.1 Frequency Response of High Pass Filter.

$$V_{in}(j\omega) = I(j\omega)\left(R + \frac{1}{j\omega C}\right)$$

$$V_{out}(j\omega) = I(j\omega)R$$

$$\frac{V_{out}(j\omega)}{V_{in}(j\omega)} = H(j\omega) = \frac{R}{\left(R + \frac{1}{j\omega C}\right)}$$

$$\text{Let } \omega_L = \frac{1}{RC}$$

$$H(j\omega) = \frac{j\frac{\omega}{\omega_L}}{\left(1 + j\frac{\omega}{\omega_L}\right)}$$

Figure 17.3

(2)

Equation (2) has zero at zero frequency and a pole at

$$\omega_L$$

Figure 17.4

. The zero introduces an +20dB asymptote at zero frequency and an -20dB asymptote at

$$\omega_L$$

Figure 17.5

. The net result is a High Pass Filter where frequencies higher than

$$\omega_L$$

Figure 17.6

have 100% transmission and frequencies lower than

$$\omega_L$$

Figure 17.7

are progressively suppressed at 20dB per decade as we move down the frequency scale as shown in the frequency response curve..

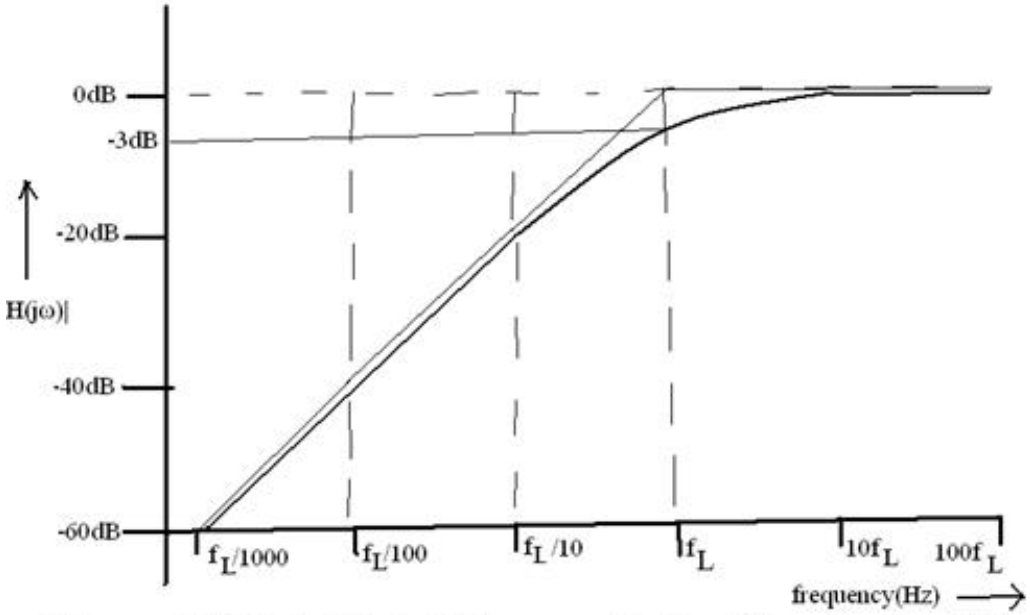


Figure 16. Bode Plot of the magnitude of the steady state sinusoidal frequency response of a high pass filter.

Figure 17.8

Figure 16. Magnitude of Transfer Function vs Frequency response of HPF.

Chapter 18

AnalogElectronics_Lecture4_Supplement_BOI

AnalogElectronics_Lecture4_Supplement_BODE_PLOT

Bode Plot of short circuit forward current transfer ratio of CB BJT(α_f) .

As we have already seen in the T Model of CB BJT, the short circuit forward current transfer ratio is given by the expression:

$$\alpha_f = \frac{\alpha_{fo}}{1 + j\left(\frac{\omega}{\omega_\alpha}\right)}$$

Figure 18.1

Magnitude-Frequency response of this parameter is :-

[1] This content is available online at <http://cnx.org/content/m31062/1.1/>.

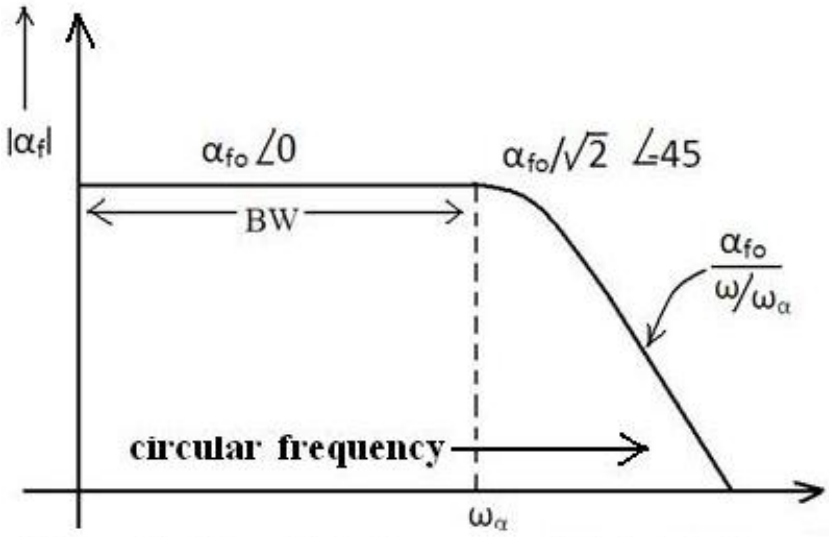


Figure 1. Magnitude-frequency Plot alphaf.

Figure 18.2

Absolute value of

$$\alpha_f \text{ is } \frac{|\alpha_{fo}|}{|1+j\left(\frac{\omega}{\omega_\alpha}\right)|}$$

Figure 18.3

$$|\alpha_f| = \frac{|\alpha_{fo}|}{\sqrt{1+\left(\frac{\omega}{\omega_\alpha}\right)^2}}$$

Figure 18.4

Other way is to plot the log value(decibel value)
dB value of

$$\alpha_f = 20 \log\left(\frac{\alpha_f}{\alpha_{fo}}\right)$$

Figure 18.5

If

$$\alpha_f = \alpha_{fo}$$

Figure 18.6

then dB =0 dB,
In direct calculation:

$$\omega << \omega_\alpha ; \alpha_f = \alpha_{fo}$$

Figure 18.7

$$\omega \sim \omega_\alpha ; \ |\alpha_f| = \frac{|\alpha_{fo}|}{\sqrt{1+\left(\frac{\omega}{\omega_\alpha}\right)^2}}$$

Figure 18.8

$$\text{At } \omega = \omega_\alpha; \ |\alpha_f| = \frac{\alpha_{fo}}{2} \ ; \qquad \angle\alpha_f = \angle -45^o$$

Figure 18.9

$$\omega_\alpha = Alpha\ cutoff\ frequency$$

Figure 18.10

= -3dB frequency =

$$0.707\ frequency$$

Figure 18.11

=corner frequency

$$\text{Bode Plot OF } \alpha_f$$

$$\text{At } \omega << \omega_\alpha, \alpha_f(in\ dB) = 0\ dB$$

$$\text{At } \omega = \omega_\alpha, \alpha_f(in\ dB) = -3\ dB$$

Figure 18.12

Let f_α = 1GHz then the circular frequency is:

$$\omega_\alpha = 2\pi(1 \times 10^9)Hz$$

$$\omega_\alpha = 2\pi \times 10^9 \frac{rad}{sec}$$

$$\alpha_f = \frac{\alpha_{fo}}{1 + j\left(\frac{\omega}{\omega_\alpha}\right)}$$

Figure 18.13

$$\angle\alpha_f = \frac{0^\circ}{\tan^{-1}\left(\frac{\omega}{\omega_\alpha}\right)}$$

Figure 18.14

At $\omega \ll \omega_\alpha$, phase angle is 0°
At $\omega = \omega_\alpha$, phase angle is -45 $^\circ$
At $\omega \gg \omega_\alpha$, phase angle is -90 $^\circ$
PHASE RESPONSE

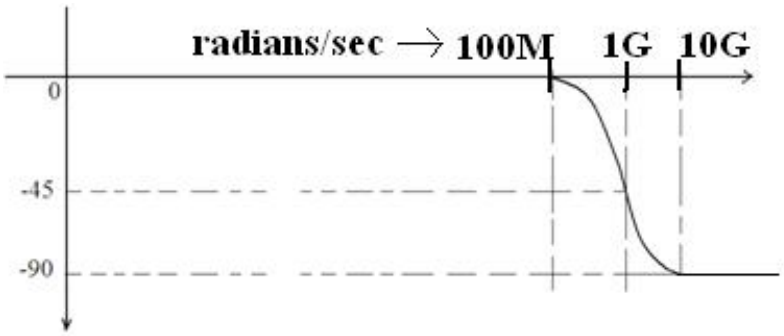


Figure 2. Phase Response of forward current transfer ratio.

Figure 18.15

In Bode Plot, total frequency can be plotted without breaking the scale. So this plot is preferred.

$$\frac{\alpha_f}{\alpha_{fo}} = \frac{1}{1 + j\left(\frac{\omega}{\omega_\alpha}\right)}$$

Figure 18.16

Consider the plot at frequencies $\omega \gg \omega_\alpha$:

$$A_1 = 20\ \log_{10}\left(\frac{\alpha_f}{\alpha_{fo}}\right)$$

$$= 20\ \log_{10}\left(\frac{\omega_\alpha}{\omega}\right)$$

$$A_2 = 20\ \log_{10}\left(\frac{\omega_\alpha}{10\omega_1}\right)$$

$$A_1 = 20\ \log_{10}\left(\frac{\omega_\alpha}{\omega_1}\right)$$

$$A_2 = 20\log\omega_\alpha - 20\log 10\omega_1$$

$$A_1 = 20\log\omega_\alpha - 20\log\omega_1$$

Figure 18.17

A_1-A_2 = 20dB

SO if frequency is increased by 10 times, difference is 20dB. This gives a skirt of -20dB per decade. That is for every 10 times increase in frequency, magnitude of response falls by 20dB as shown in Figure 3.

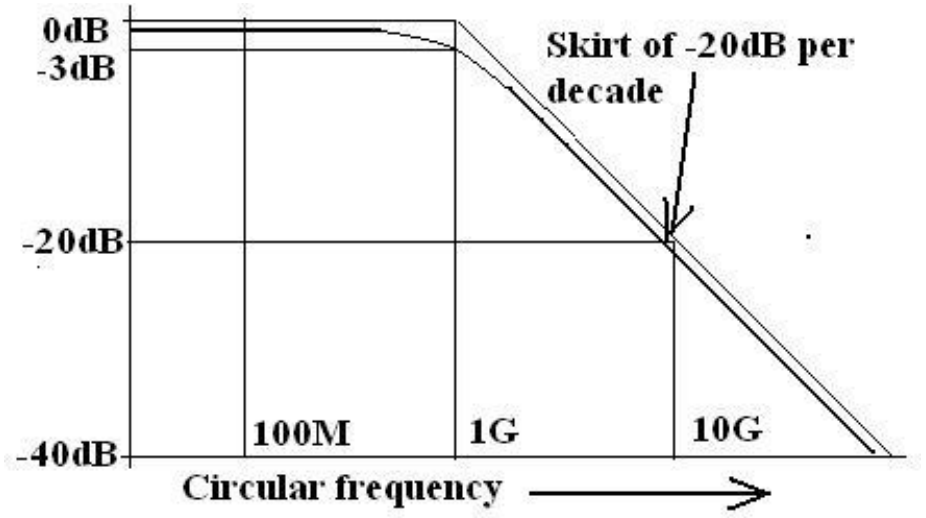


Figure 18.18

In the above plot, light continuous line is ASYMPTOTIC PLOT and dark continuous line is Actual Response Plot.

Chapter 19

AE_Lecture5_PartA_Low FrequencyAnalysisofCE_Amplifier[1]

AnalogElectronics_Lecture5_PartA_Low Frequency Analysis of CE Amplifier(Final)

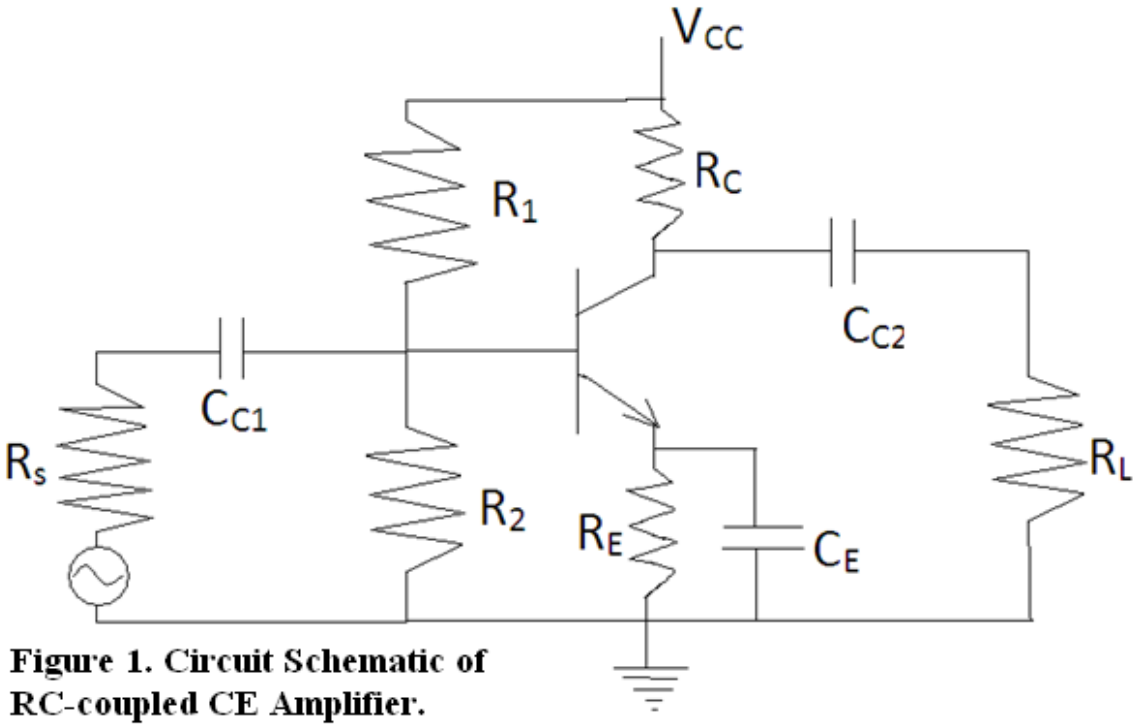


Figure 1. Circuit Schematic of RC-coupled CE Amplifier.

Figure 19.1

[1]This content is available online at <http://cnx.org/content/m31527/1.1/>.

Figure 1. RC-coupled CE Amplifier.

Lower -3dB frequency of CE Amplifier is determined by Short Circuit Time Constant Method.

Coupling Capacitors and Emitter By-pass capacitor are responsible for lower -3dB frequency(f_L).

We consider the time constant associated with each capacitor with the remaining capacitors shorted. Suppose the time constants associated with C_{C1}, C_{C2} and C_E are τ_{1S} , τ_{2S} and τ_{3S} . Then the overall time constant associated with the amplifier due to combined effect of C_{C1}, C_{C2} and C_E is τ_L where:

$$\frac{1}{\tau L} \triangleq \frac{1}{\tau 1s} + \frac{1}{\tau 2s} + \frac{1}{\tau 3s} = 2\pi f_L = \omega_L$$

Figure 19.2

Here Time Constant associated with each capacitor is τ = RC where R is the equivalent resistance seen by each Capacitor.

$$R_s = 5k\Omega, R_B = R_1||R_2 = 10k\Omega, R_C = 2k\Omega$$

$$r_x = 100\Omega, r_\pi = 0.4k\Omega, g_m = \frac{I_C}{V_T} = 100mmho$$

Figure 19.3

$$I_C = 2.5mA, R_E = 0.4k\Omega, \beta_{fo} = 40$$

Figure 19.4

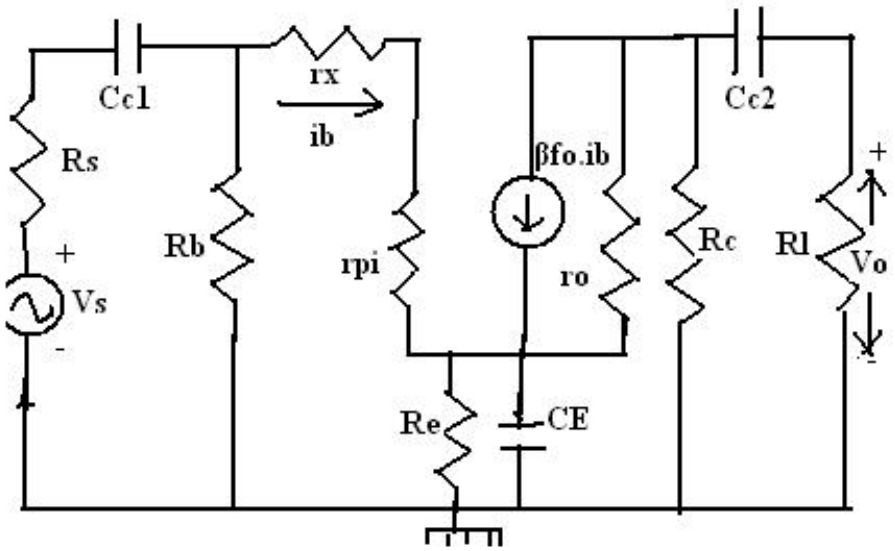


Figure 2. The incremental model of RC-coupled CE Amplifier. Battery Vcc has been shorted and BJT has been replaced by Hybrid-pi Model.

Figure 19.5

Figure 2. Low Frequency Incremental model

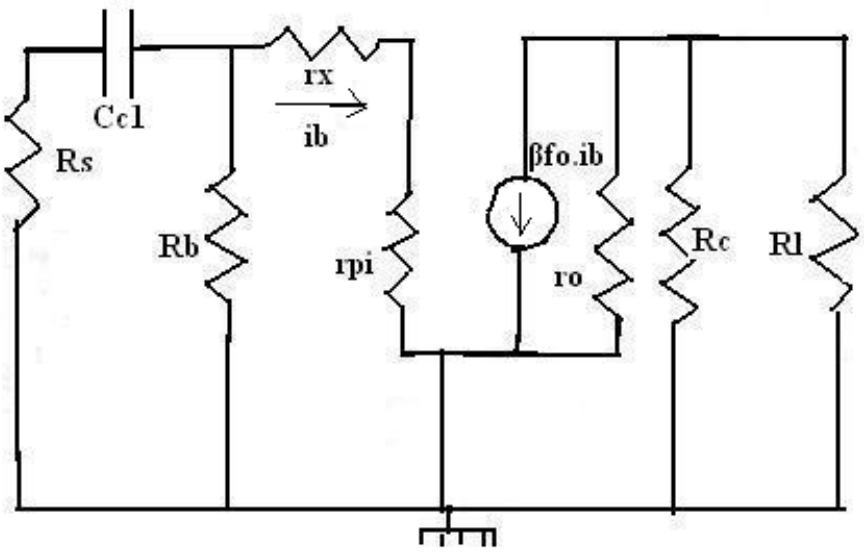


Figure 3. Calculation of Short Circuit Resistance as seen by Cc1.

Figure 19.6

Figure 3. Low frequency Incremental Model with C_E and Cc2 shorted. Equivalent resistance seen by Cc1 is $R_S + (R_B||(r_x+r_\pi))$

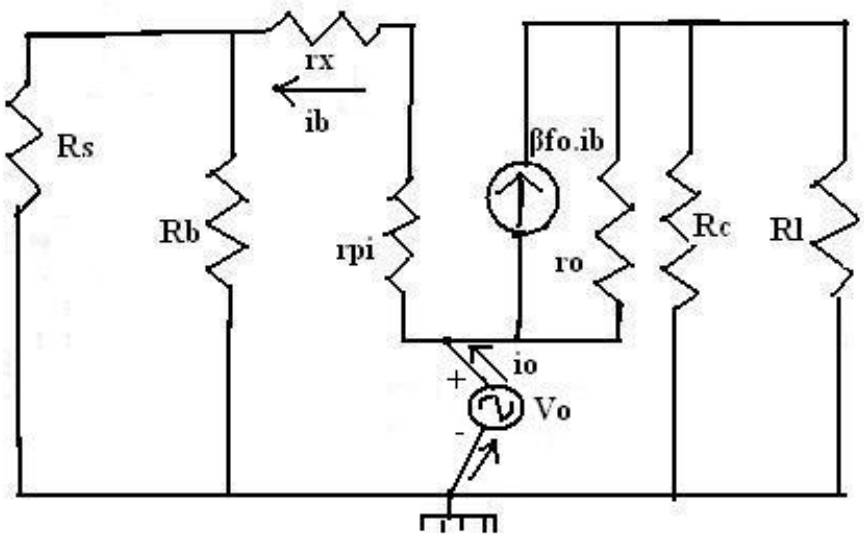


Figure 4. Equivalent circuit for measuring the short circuit resistance as seen by Ce

Figure 19.7

Figure 4. Incremental Model with Cc1 and Cc2 shorted. Ce sees the equivalent Resistance $R_{2s}= v_o/i_o$
In Figure 4 , a voltage source v_o is connected in place of C_E .
Current drawn from the source is : $i_o= i_b + \beta_{fo}.\ i_b$
where $i_b = v_o/(r_\pi + r_x + R_B||R_S)$ therefore $i_o = i_b(1 + \beta_{fo})= (1 + \beta_{fo}).v_o/(r_\pi + r_x + R_B||R_S)$;
Therefore $v_o/\ i_o = (r_\pi + r_x + R_B||R_S)/\ (1 + \beta_{fo})= R_{2s}$;

$$R_{1s} = R_s + R_B||(r_x + r_\pi) = 5.48k\Omega$$

$$R_{2s} = R_E||\left[\frac{r_x + r_\pi + R_S||R_B}{\beta_{fo} + 1}\right] = 0.0758k\Omega$$

$$C_{C1} and C_E \text{ are both present. } C_{C2} = \infty$$

Overall -3dB frequency will be:

$$\omega_l = \frac{1}{\tau_L} = \frac{1}{\tau_{1s}} + \frac{1}{\tau_{2s}}$$

For equal poles:-

$$1.15\omega_l = \frac{1}{\tau_{1s}} + \frac{1}{\tau_{2s}}$$

Figure 19.8

If $f_l = 30Hz; \omega_l = 188.5\frac{rad}{sec} = 0.1885(msec)^{-1}$

$$\therefore 0.217(msec)^{-1} = \frac{1}{5.48C_C} + \frac{1}{0.0758C_E}$$

$$C_C = 1.68\mu F, C_E = 122\mu F$$

From first principles:

(i.e. detailed circuit analysis)

$$A_V(j\omega) = \frac{-A_{vo}(j\omega)(j\omega + \omega_z)}{(j\omega + \omega_{p1})(j\omega + \omega_{p2})}$$

At $\omega \gg \omega_{p1}, \omega_{p2}, \omega_z,$

Figure 19.9

$$A_V(j\omega) = \frac{-A_{vo}(j\omega)(j\omega)}{(j\omega)(j\omega)} = -A_{vo}$$

Figure 19.10

By detailed analysis,

$$\frac{1}{\tau L} \triangleq \frac{1}{\tau 1s} + \frac{1}{\tau 2s} + \frac{1}{\tau 3s} = 2\pi f_L = \omega_L$$

Figure 19.11

Here there are two poles corresponding to two capacitors C_{C1} and C_E . The second coupling capacitor is considered to be infinity. The highest pole decides lower -3dB frequency. So 0.188Krads/sec decides the lower -3dB frequency which comes out to be 30Hz.

Chapter 20

AE_Lecture5_PartA_The Low frequency Voltage Gain Expression by detailed circuit analysis.[1]

By detailed analysis,

$$A_V(j\omega) = \frac{-(13.9)(j\omega)(j\omega + 0.025)}{(j\omega + 0.188)(j\omega + 0.029)}$$

Figure 20.1

Here there are two poles corresponding to two capacitors C_{C1} and C_E . The second coupling capacitor is considered to be infinity. The highest pole decides lower -3dB frequency. So 0.188Krads/sec decides the lower -3dB frequency which comes out to be 30Hz.

[1] This content is available online at <http://cnx.org/content/m31582/1.1/>.

Chapter 21

AE_Lecture5_PartB_High Frequency Analysis of CE Amplifier[1]

MID FREQUENCY ANALYSIS OF CE AMPLIFIER

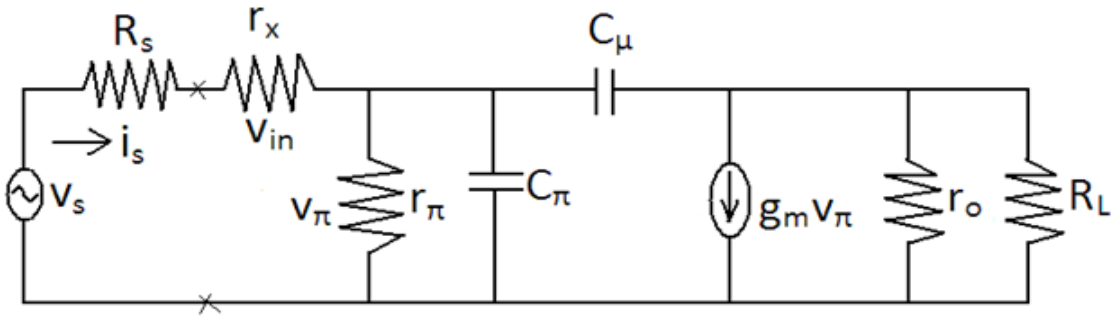


Figure 2. High Frequency Incremental Model of CE BJT Amplifier

Figure 21.1

$$v_o = -(\beta_{fo} i_b) R_c$$

Figure 21.2

_____(1)

[1]This content is available online at <http://cnx.org/content/m31564/1.1/>.

$$v_{in} = i_b(r_x + r_\pi)$$

Figure 21.3

_ _ _ _ _ _ _ (2)

$$\therefore \frac{v_o}{v_{in}} = A_{vo} = Internal\ Voltage\ Gain = \frac{-(\beta_{fo})(R_c)}{(r_x + r_\pi)}$$

Figure 21.4

$$v_s = i_s[R_s + R_B \,||\, (r_x + r_\pi)]$$

Figure 21.5

_ _ _ _ _ (3)

$$i_b = \frac{i_s R_B}{(R_B + (r_x + r_\pi))}$$

Figure 21.6

$$\therefore \frac{i_b}{i_s} = \frac{R_B}{(R_B + (r_x + r_\pi))}$$

Figure 21.7

Dividing Eq(1) by Eq(3) we get:

$$\frac{v_o}{v_s} = A_{vso} = Voltage\ Gain\ w.r.t.\ source$$

Figure 21.8

$$A_{vso} = \frac{-(\beta_o)(R_C)}{[R_S + R_B \,||\, (r_x + r_\pi)]} \times \frac{i_b}{i_s}$$

Figure 21.9

But

$$\frac{i_b}{i_s} = \frac{R_B}{(R_B + (r_x + r_\pi))}$$

Figure 21.10

$$A_{vso} = \frac{-(\beta_o)(R_C)}{[R_S + R_B \,||\, (r_x + r_\pi)]} \times \frac{R_B}{(R_B + (r_x + r_\pi))}$$

Figure 21.11

Normally $R_B \gg (r_x + r_\pi)$ therefore

$$A_{vso} = \frac{-(\beta_o)(R_C)}{[R_S + (r_x + r_\pi)]} \times \frac{R_B}{(R_B)}$$

Figure 21.12

$$A_{vso} = \frac{-(\beta_o)(R_C)}{[R_S + (r_x + r_\pi)]}$$

Figure 21.13

In the actual gain with respect to the source , source resistance plays a very important role. Smaller is R_S larger is the voltage gain.

HIGH FREQUENCY RESPONSE OF CE AMPLIFIER.

Upper -3dB frequency (f_H) is determined by Open Circuit Time Constant Method.

The parasitic capacitances C_π and C_μ are responsible for the fall in the Voltage Gain Response at high frequencies. The time constant associated with C_π is the Open Circuit Time Constant τ_{10} and the time constant associated with C_μ is the Open Circuit Time Constant τ_{20} .

The overall time constant associated with the amplifier is $\tau_H = \tau_{10} + \tau_{20} =$

$$\frac{1}{\omega H}$$

Figure 21.14

Therefore $\omega_H =$

$$\frac{1}{(\tau 10 + \tau 20)}$$

Figure 21.15

;

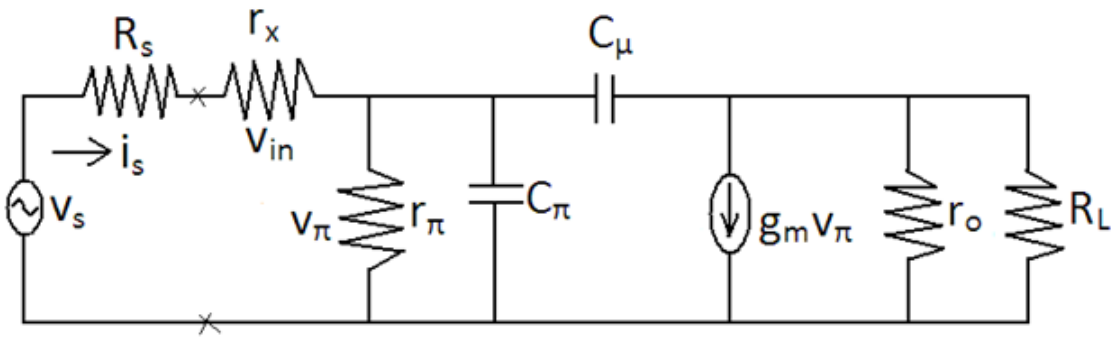


Figure 2. High Frequency Incremental Model of CE BJT Amplifier

Figure 21.16

GBP=

$$|A_V \omega_H| \leq \left(\frac{\beta_o R_L}{R_S+(r_x+r_\pi)}\right)\left(\frac{1}{r_{\pi o} C_T}\right)$$

Figure 21.17

$$r_{\pi o} = r_\pi \,||\, (R_S + r_x)$$

Figure 21.18

$$\omega_h =$$

Figure 21.19

$$\frac{1}{r_{\pi_o} C_T}$$

Figure 21.20

$$C_T = C_\pi + C_\mu(1 + g_m R_L)$$

Figure 21.21

If

$$R_s = 0, r_{\pi_o} \sim r_x; \&\quad C_T = (C_\mu g_m R_L)$$

Figure 21.22

$$\therefore GBP \leq \frac{\beta_o R_L}{r_\pi} \times \frac{1}{(r_x)(C_\mu g_m R_L)}$$

Figure 21.23

$$\leq \frac{\beta_o}{\left(\frac{\beta_o}{g_m}\right)} \frac{R_L}{(r_x)(C_\mu)(g_m)(R_L)}$$

Figure 21.24

$$GBP \leq \left(\frac{1}{r_x C_\mu}\right)$$

Figure 21.25

$$\omega_T = \frac{1}{\tau} = \frac{1}{\frac{W^2}{2D_n}} = \frac{2D_n}{W^2}$$

Figure 21.26

So we see that base spreading resistance is very important from GBP point of view which is the figure of merit of the given transistor. Also the transit frequency solely depends on the base width. Narrower the base width, faster is the response. But narrow base is detrimental to r_x which in turn is detrimental for GBP. The only way out is higher doping of Base which is going to reduce the Injection Efficiency. So the new concept of Si-SiGe-Si heterojunction Bipolar Junction Transistor solves all these contradictory requirements. Here we have very narrow base width of the order of 10nm leading to picoseconds transit time through the narrow base, high base doping thereby reducing base spreading resistance and since base is made of Si-Ge alloy which has a narrower band-gap as compared to that of Si, hence inspite of high base doping high injection efficiency is maintained from Emitter to Base thereby obtaining best short circuit forward active current gain. Thus we have achieved the best of all performance parameters. In this process we have been able to achieve Si-Ge HBT with transit frequency of 200GHz.

High Frequency Response Of CB Amplifier.

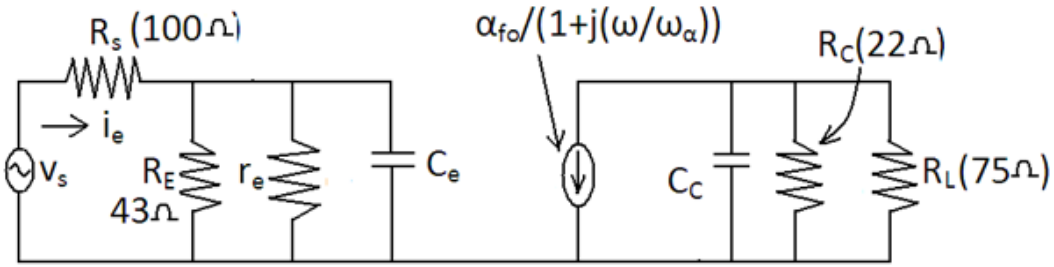


Figure 3. High Frequency Model after Miller Transformation.

Figure 21.27

$$\tau_{o1} = (C_e)(r_e \,||\, R_E \,||\, R_s)$$

Figure 21.28

$$\tau_{o2} = (C_C)(R_C \,||\, R_L)$$

Figure 21.29

$$\tau_o = \tau_{o1} + \tau_{o2}$$

Figure 21.30

$$\sim\tau_{o2}$$

Figure 21.31

$$\omega_h = \frac{1}{\tau_{o2}} = \frac{1}{(C_C)(R_C \,||\, R_L)}$$

Figure 21.32

Chapter 22

AE_Lecture5_PartC_Figure4 of High Frequency Analysis of CB & CC Amplifier[1]

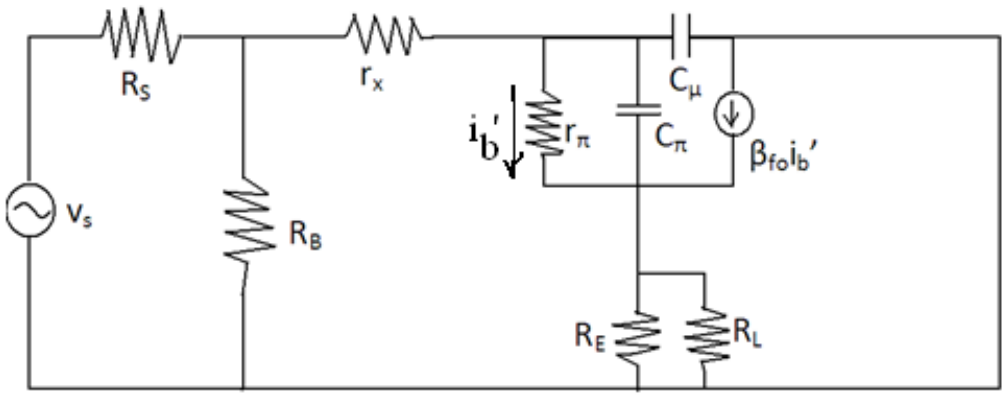


Figure 4. High Frequency Model of CC Amplifier. BJT has been replaced by Hybrid-pi Model.

Figure 22.1

[1] This content is available online at <http://cnx.org/content/m31580/1.2/>.

Chapter 23

AE_Lecture5_PartC_High Frequency Analysis of CB & CC Amplifier[1]

High Frequency Response Of CB Amplifier.

CB Amplifier is almost an uni-lateral circuit. It has negligible reverse transmission. Hence it is ideal for RF applications where there is always a danger of parasitic oscillations.

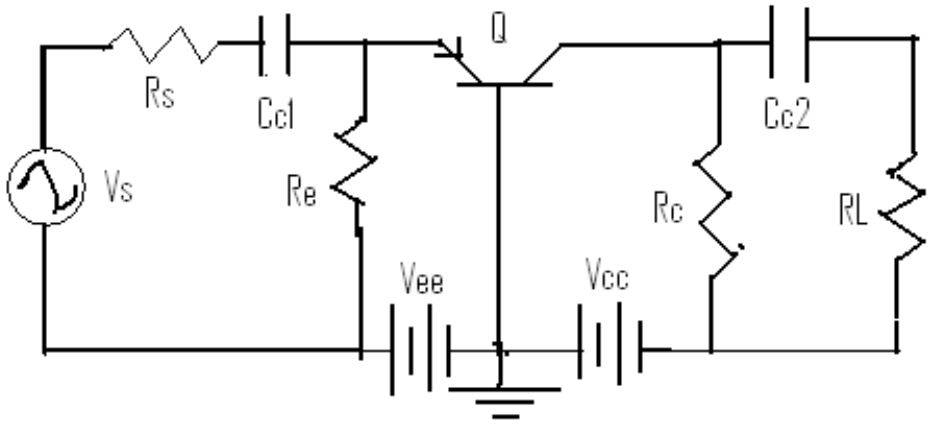


Figure 1. CB BJT Amplifier using two battery biasing.

Figure 23.1

In Figure 1, we have a CB BJT Amplifier with two battery biasing. This circuit has to be analyzed for its upper cut off frequency.

[1]This content is available online at <http://cnx.org/content/m31574/1.1/>.

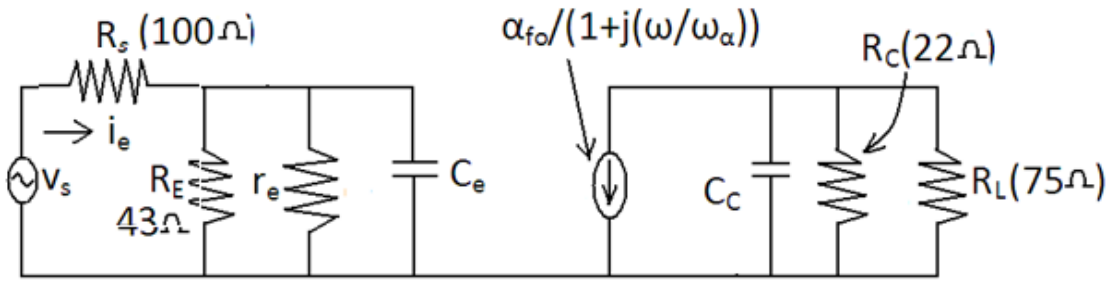


Figure 2. High Frequency Incremental Model of CB BJT Amplifier

Figure 23.2

In Figure 2, we have given the high frequency model of CB BJT using the T-Model of BJT.

Following is the open circuit time constant method for arriving at the upper cut-off frequency of the amplifier.

$$\tau_{o1} = (C_e)(r_e \,||\, R_E \,||\, R_s)$$

Figure 23.3

$$\tau_{o2} = (C_C)(R_C \,||\, R_L)$$

Figure 23.4

$$\tau_o = \tau_{o1} + \tau_{o2}$$

Figure 23.5

$$\sim \tau_{o2}$$

Figure 23.6

$$\omega_h = \frac{1}{\tau_{o2}} = \frac{1}{(C_C)(R_C \,||\, R_L)}$$

Figure 23.7

HIGH FREQUENCY MODEL OF CC AMPLIFIER

CC Amplifier is also known as Emitter Follower. It is also known as Buffer. Buffer isolates the output system from input system.

It is used for driving transmission lines. It is a voltage controlled voltage source. Its output is a constant current source hence it is suitable for driving variable load.

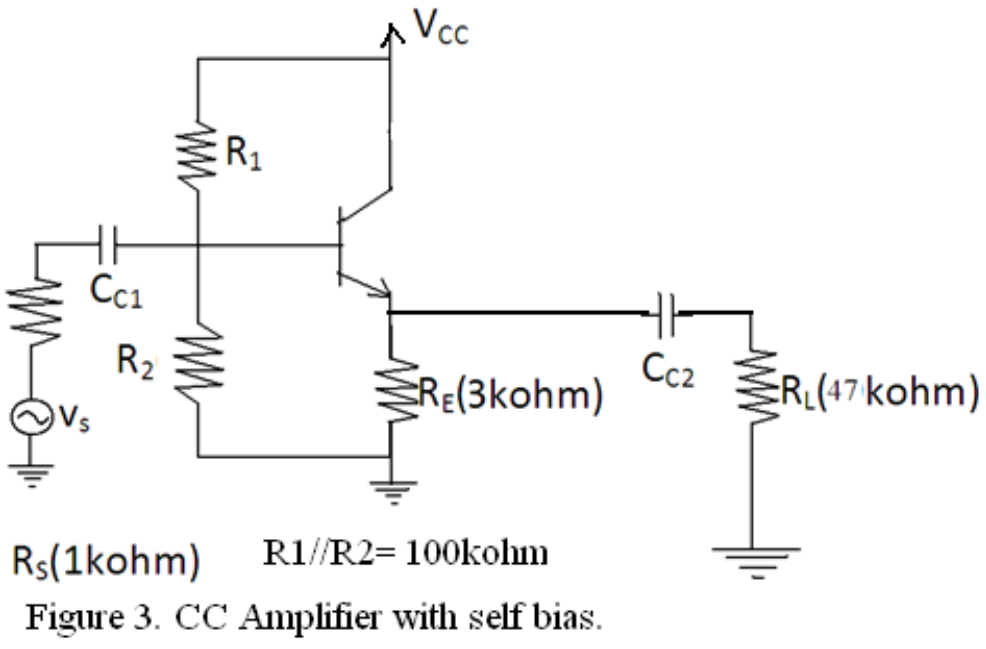


Figure 3. CC Amplifier with self bias.

Figure 23.8

In Figure 3, we have CC Amplifier with self bias. We will analyze the upper cut-off frequency of the amplifier.

The Trnsistor is operating at Q point (1.5mA,5V). Following Hybrid-π are given:

$$\beta_{fo} = 100, r_x = 150\Omega$$

Figure 23.9

$$C_\mu = 0.5pF, f_T = 500MHz$$

Figure 23.10

$$g_m = \frac{I_C}{V_T} = \left(\frac{1.5}{25}\right); r_\pi = \frac{\beta_o}{g_m}$$

Figure 23.11

$$R_1 \| R_2 = R_B = 100k\Omega \ ; \ R_E \| R_L = 2.82k\Omega = R_E'$$

Figure 23.12

$$r_\pi = \frac{100 \times 25}{1.5} = \frac{2500}{1.5} = 1666.6\Omega = 1.67k\Omega$$

Figure 23.13

High Frequency INCREMENTAL CIRCUIT of the CC Amplifier is:
Figure 4 is given as supplementary of AE_lecture5_PartC
i_b' is the useful transistor current which takes part in transistor action and is the component of i_b , the base current , which flows through r_π .
The

Figure 23.14

Thevenin Equivalent Voltage at the input of the amplifier is:
$R_{Th} = R_S \,||R_B$

$$v_{Th} = \frac{v_s}{R_s + R_B} \times R_B$$

Figure 23.15

$$\therefore \frac{v_{Th}}{v_s} = \left(\frac{100}{101}\right) = 0.99$$

Figure 23.16

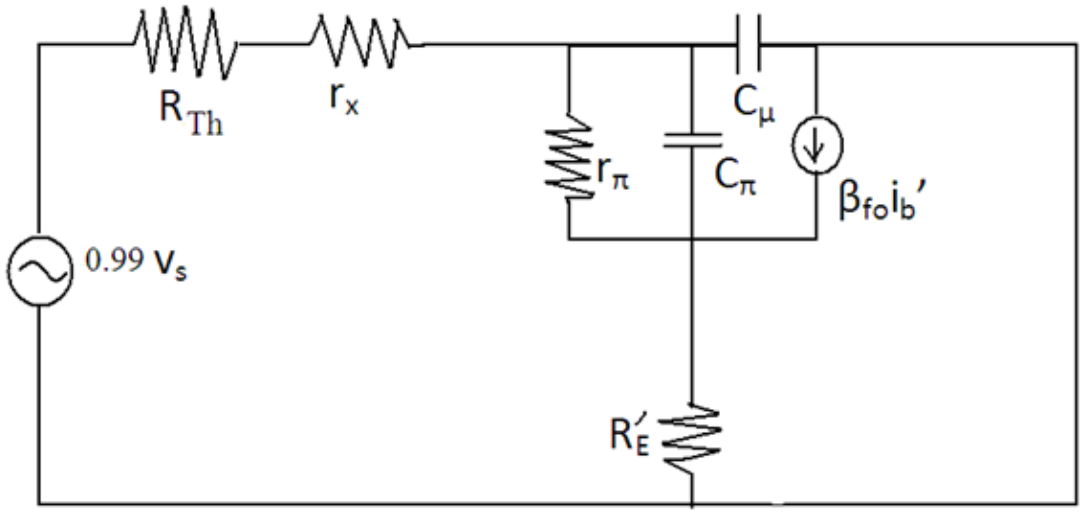


Figure 5. The simplification of the circuit in Figure 4.

Figure 23.17

v

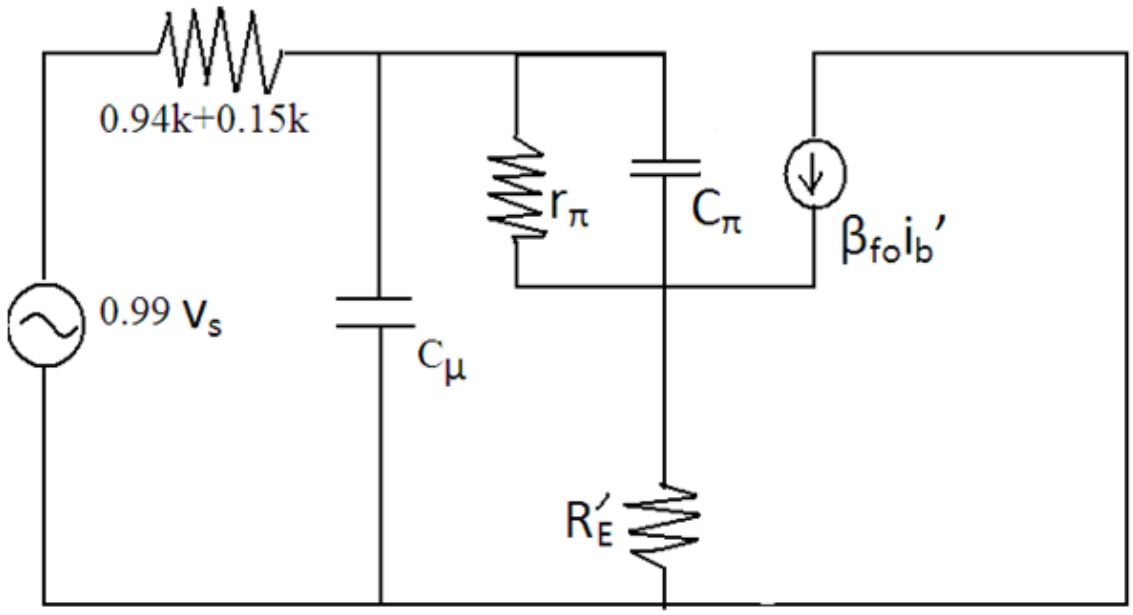


Figure 6. Numerical values of Vth and Rth inserted in the circuit.

Figure 23.18

$$R_S \,||\, R_B = R_{Th} = \frac{(1)(17)}{18} = 0.94k\Omega$$

Figure 23.19

What is $\tau_{\mu o}$ (open-circuit time constant associated with C_μ) and $\tau_{\pi o}$ (open-circuit time constant associated with C_π)?

$\tau_{\mu o}=(C_\mu)(R_{10})$

$\tau_{\pi o}=(C_\pi)(R_{20})$

Circuit for finding R_{1o}

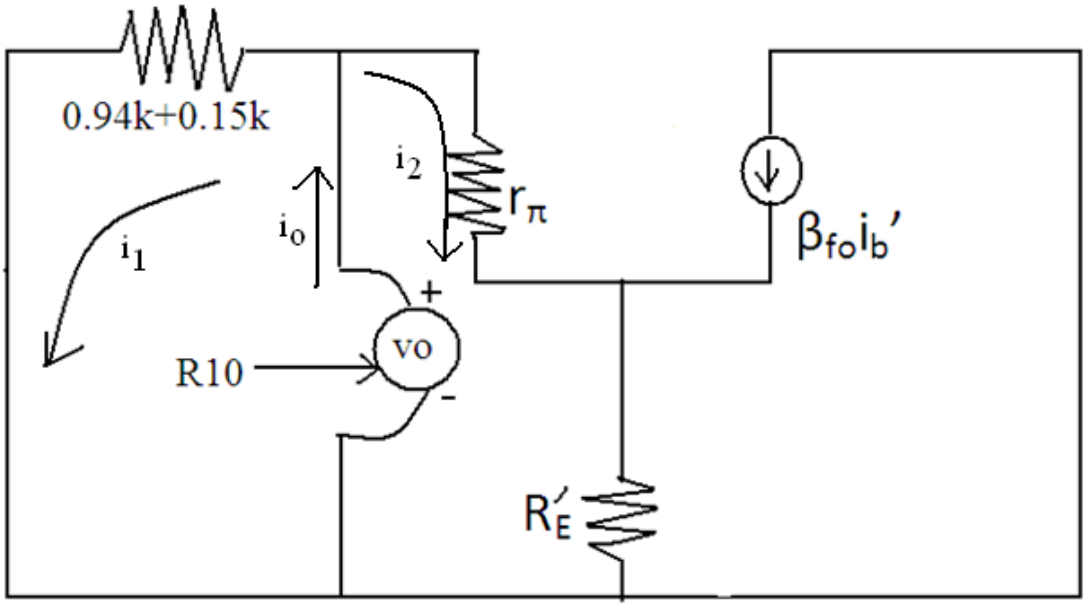


Figure 7. Circuit for determining the equivalent resistance associated with Cu. Note that Cu is connected between base and collector and collector is grounded. Therefore Cu is connected between base and ground. By applying a voltage source between base and grond we can determine the equivalent resistance seen by Cu.

Figure 23.20

To find the equivalent resistance seen by Cμ, we apply a voltage source at base and ground.
Total current drawn from vo is i1+i2.
Therefore vo/(i1+i2)= R1o

$$R_{1o} = (R_{Th} + r_x) \,||\, \left(r_\pi + \left(1 + \beta_{fo}\right)R'_E\right)$$

Figure 23.21

$$R_{1o} = (1.09k) \,||\, \big(1.67k + (101)(2.82k\Omega)\big)$$

Figure 23.22

$$= (1.09k) \,||\, (285.6k\Omega) = 1.1k$$

Figure 23.23

$\tau_{\mu o}$=(0.5pF x 1.1kΩ)=0.54nsec
Circuit for finding R_{2o}

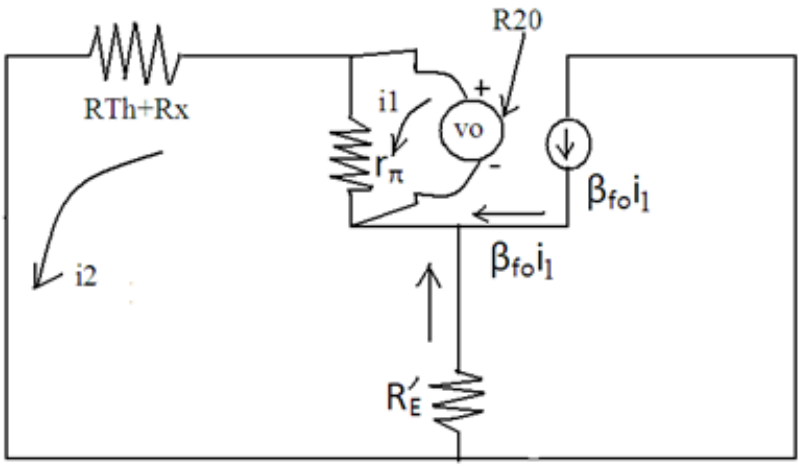


Figure 8. The circuit for determining the equivalent resistance seen by Cpi. Exactly the same procedure is adopted as in case of Cu.

Figure 23.24

A voltage source is applied at the node pair where Cπ was connected.
Total current drawn is $i_0 = i_1 + i_2$;

$$i_1 = \frac{v_o}{r_\pi}$$

Figure 23.25

$$i_2 = \left(\frac{v_o}{R_{Th} + r_x + R_E'}\right)$$

Figure 23.26

$$\therefore i_o = i_1 + i_2 + \beta_{fo} i_1$$

Figure 23.27

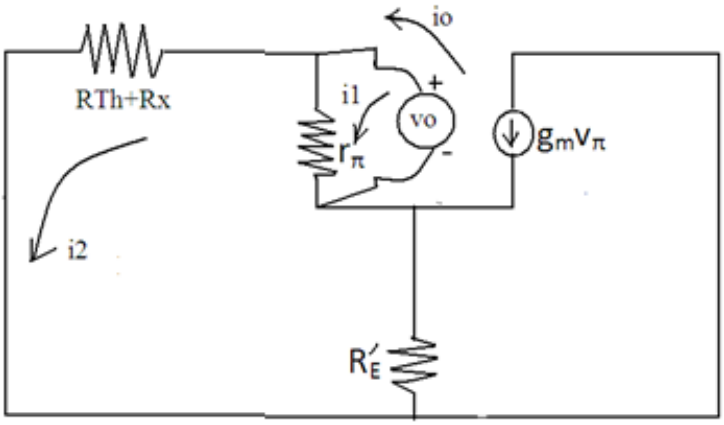


Figure 9.The current source βf0i1 is replaced by gmvπ. This simplifies the calculation of Req.

Figure 23.28

$$R_{\pi_o} = R_{2_o} = r_\pi \,||\, R_{eq} = r_\pi \,||\, \left(\frac{R_{Th} + r_x + R'_E}{1 + g_m R'_E}\right)$$

Figure 23.29

And $\beta_{f0} i_1$ $g_m v_\pi$

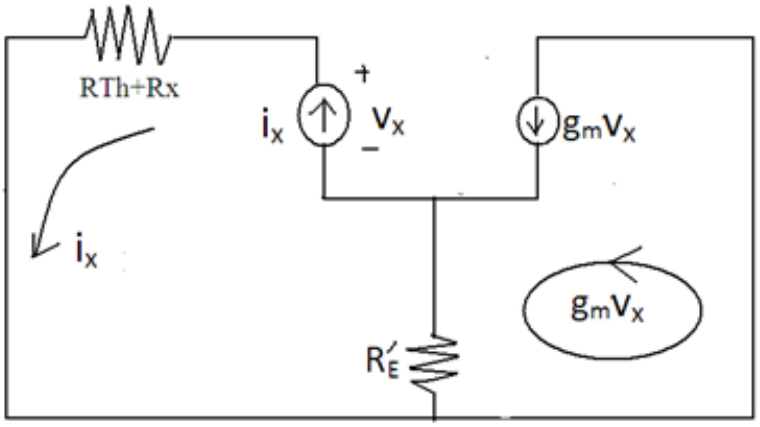


Figure 10. By this circuit we determine the analytic relation of Req.

Figure 23.30

R_{eq} =

$$\left(\frac{R_{Th}+r_x+R_E'}{1+g_m R_E'}\right)$$

Figure 23.31

This expression is derived as follows(Refer to Figure 10):

$$\therefore v_x = i_x(R_{Th}+r_x)+(i_x-g_m v_x)R_E'$$

Figure 23.32

$$(v_x + g_m R_E' v_x) = i_x (R_{Th} + r_x + R_E')$$

Figure 23.33

$$\therefore R_{eq} = \frac{v_x}{i_x} = \left(\frac{R_{Th} + r_x + R_E'}{1 + g_m R_E'} \right)$$

Figure 23.34

$$R_{\pi_o} = 1.67k\Omega \,||\, \left(\frac{1.09k + 2.82k}{1 + \frac{1.5}{25} \times 2820} \right)$$

Figure 23.35

$$R_{\pi_o} = 1.67k\Omega \,||\, \left(\frac{3.9k}{170} \right)$$

Figure 23.36

$$R_{\pi_o} = 1670 \,||\, \left(\frac{3900}{170}\right)$$

Figure 23.37

$$= 1670 \,||\, 23 = 22.7\Omega$$

Figure 23.38

$$\therefore \tau_{\pi o} = (R_{2o})(C_{\pi})$$

Figure 23.39

$$= (22.7)(19.9pF)$$

Figure 23.40

$$\therefore \tau_{\pi o} = 0.45nsec$$

Figure 23.41

$$\therefore \tau_o = 0.54 + 0.45 = 1nsec$$

Figure 23.42

$$\therefore \omega_h = \frac{1}{\tau_0} = 1G\,\frac{rad}{sec}$$

Figure 23.43

$$f_h = \frac{1000}{2\pi} MHz = 159MHz$$

Figure 23.44

CC has unity gain hence largest 159 MHz largest B.W.

Configuration	B.W.
CE	1.56MHz
CE Degenerate	10.7MHz
CB	15.9MHz
CC	159MHz

Table 23.1

Chapter 24

AE_Lecture 5_Part C_continued_High frequency analysis of CB.[1]

AE_Lecture 5_Part c_continued_High frequency analysis of CB.

In this continuation of high frequency application, we use the same self-biasing configuration to achieve CB, CE and CC amplifier. These three Circuit Configuration have the same Q point (I_{CQ} = 1mA , V_{CEQ} = 5V). Hence they have the same Hybrid-π parameters namely:

β fo = incremental short circuit gain at low frequencies = 100;

Transit frequency given = f T = 200MHz;

At the Q point, C ob = C μ = C jBC =

$$C_c$$

Figure 24.1

= 5pF ;

Circular Transit Frequency = ω T =

$$\frac{1}{\tau_t} =$$

Figure 24.2

1.2566×10 9 radians/second;

Here it may be noted that reciprocal of frequency gives Time Period of repetition T but reciprocal of circular frequency always gives the Time –Constant. In filters the reciprocal of circular cut-off frequencies gives the RC time constant of the associated RC configuration. Here the reciprocal of the circular transit frequency gives the transit time across the narrow base of the BJT .

[1] This content is available online at <http://cnx.org/content/m34116/1.1/>.

Transit Time =

$$\tau_t = \frac{1}{1.2566 \times 10^9} =$$

Figure 24.3

0.8nsec;
Trans-conductance = g m =

$$\frac{I_C}{V_T} =$$

Figure 24.4

40mSiemens(or mS) =

$$\frac{1}{r_m}$$

Figure 24.5

= 1/25Ω;
Whereas

$$r_e = \frac{V_T}{I_E} = \frac{25mV}{\frac{1mA}{\alpha_F}} \approx 25\Omega$$

Figure 24.6

;

$$\frac{C_{\mu} + C_{\pi}}{g_m} = 0.8nsec$$

Figure 24.7

Therefore

$$C_{\pi} \times 25 = 0.8 \times 10^{-9} - 5 \times 10^{-12} \times 25 = 0.725nsec$$

Figure 24.8

Therefore

$$C_{\pi} = C_e = 29pF$$

Figure 24.9

Base spreading resistance is given as r x =100Ω ;

$$r_{\pi} = \frac{\beta_{fo}}{g_m} = 2.5k\Omega$$

Figure 24.10

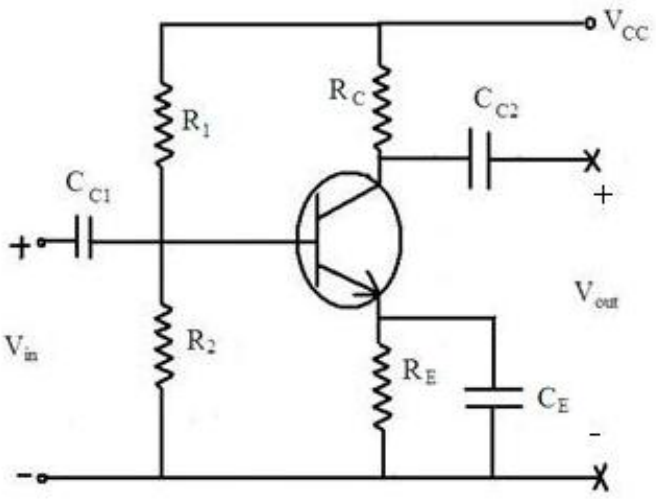


Figure 1 . RC-coupled CE BJT Amplifier

Figure 24.11

Self –biasing configuration is connected as CE BJT Amplifier by the use of Emitter bypass capacitance C_E.

The circuit elements are given as :

$R_C = 5k$, $R_E = 2k$, $R_1 = 200k$, $R_2 = 60k$, $R_L = 100k$, $R_S = 50\Omega$,

$R_B = R_1 \,||\, R_2 = 46k$, $R_L' = 5k||100k - 4.76k$;

The same configuration can be connected as CB Amplifier by the use of Base bypass capacitance C_B as shown in the Figure 3. The same configuration can be connected as CC Amplifier by the use of Collector bypass capacitance C_C as shown in the Figure 4.

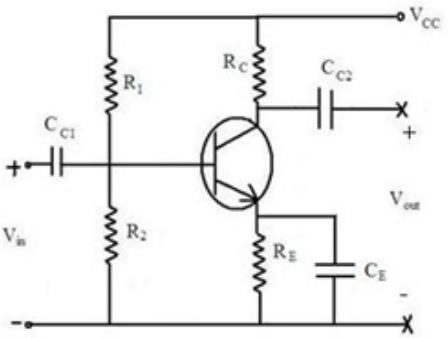


Figure 2 . RC-coupled CE BJT Amplifier

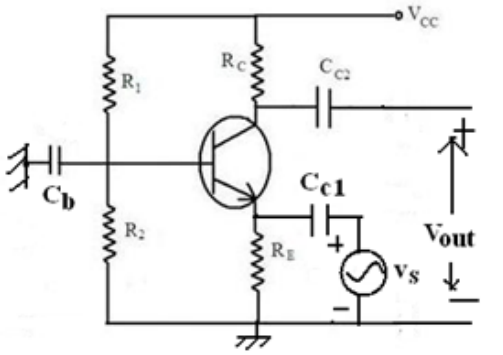


Figure 3 . RC-coupled CB BJT Amplifier

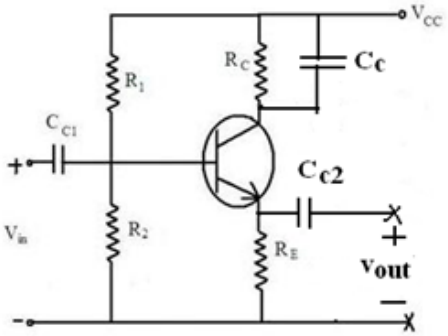


Figure 4 . RC-coupled CC BJT Amplifier

Figure 24.12

High Frequency Analysis of CB Amplifier:

Under incremental condition (refer to Figure 3),

C_B shorts out R_1 and R_2 . Coupling capacitors appear as short circuit. Battery V_{CC} appears as short circuit. Hence the incremental circuit of CB amplifier is the following as shown in Figure 5 :

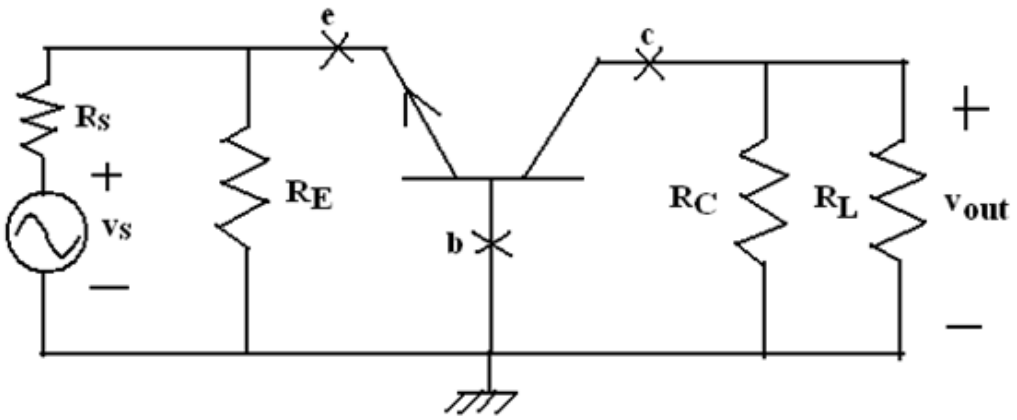


Figure 5. Incremental circuit representation of CB Amplifier.

Figure 24.13

For circuit analysis we replace CB configuration of BJT with its corresponding T-Model as shown in Figure 6.

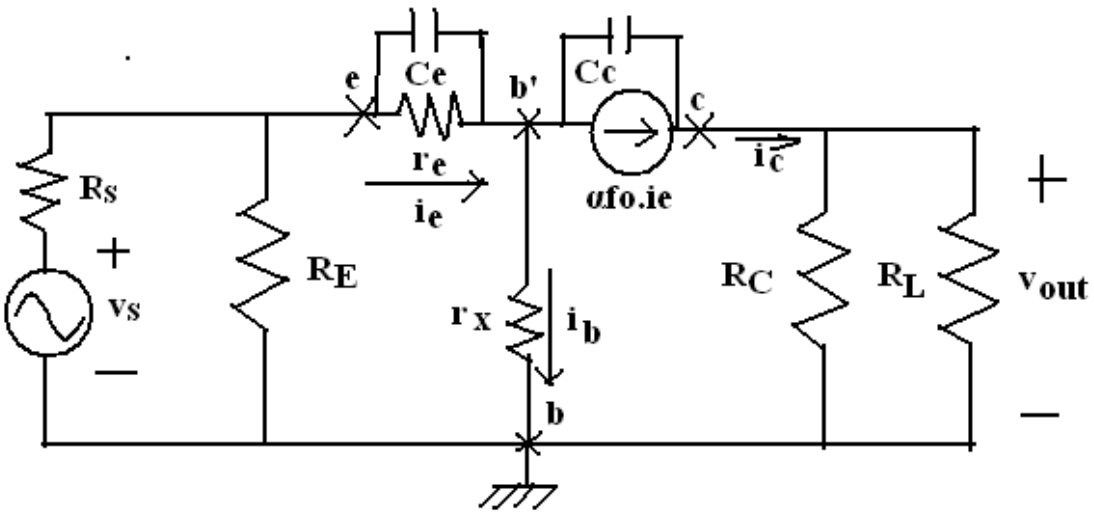


Figure 6 . Incremental circuit representation of CB Amplifier with T-Model of CB BJT.

Figure 24.14

In Figure 6, b[U+05F3] is the active base region and b is the external base terminal. The T-Model is further re-oriented as two input and output loop as shown in Figure 7.

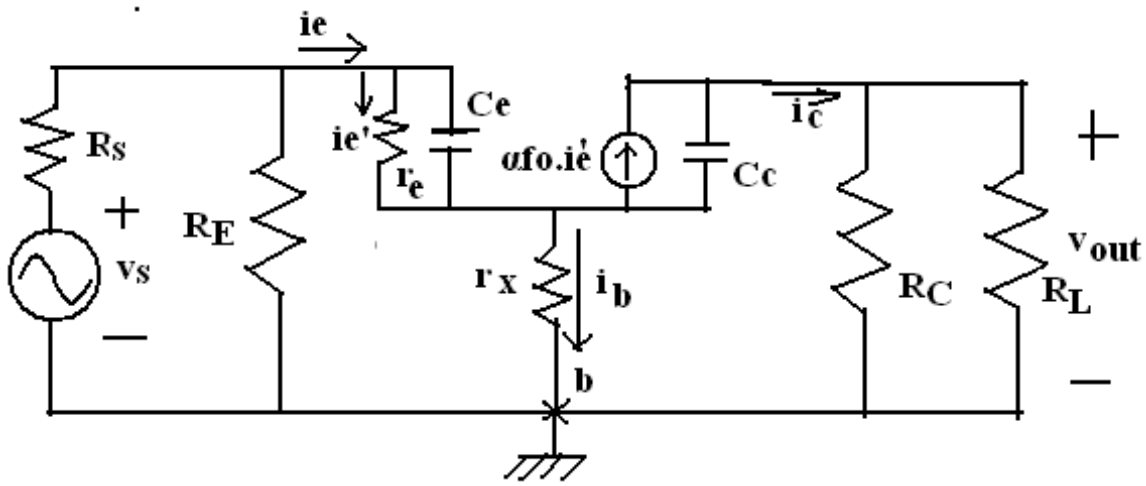


Figure 7. Incremental circuit representation of CB Amplifier with input-output loop.

Figure 24.15

The T-Model of CB BJT is further simplified into two non-interacting loops as shown in Figure 8.

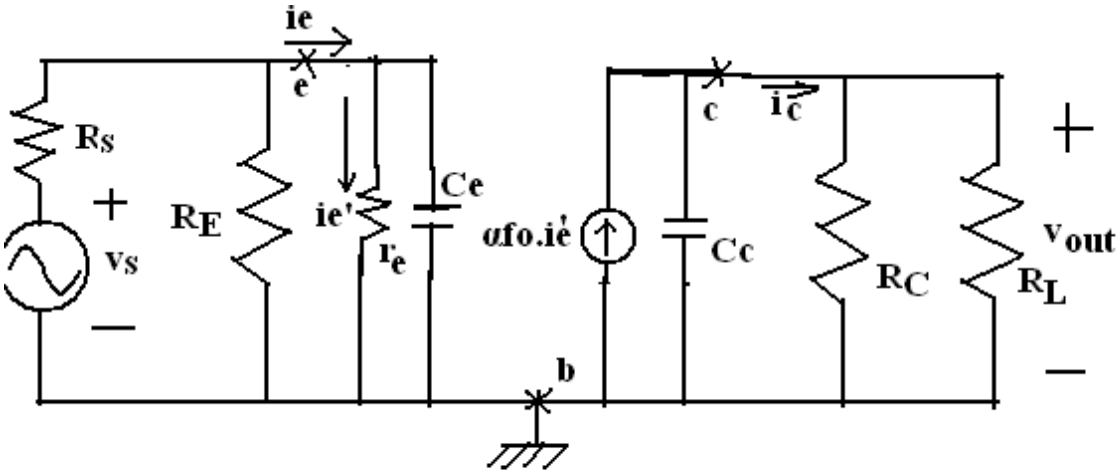


Figure 8 . Incremental circuit representation of CB Amplifier with non-interacting loop

Figure 24.16

Base spreading resistance r_x is reflected as $(1\text{-}\alpha_{fo})r_x$ in input loop and in output loop it is not reflected since it is controlled loop. Since $(1\text{-}\alpha_{fo})r_x$ is a negligible resistance hence in input loop it has been completely neglected as a result the input and output loops are completely non-interacting. This is the reason reverse transmission factor is almost non-existent in CB BJT and it is a near-Unilateral device. Hence it is very suitable for RF applications. RF Amplifier are very prone to parasitic oscillations. But if we use a Unilateral Active Device the possibility of parasitic oscillation is minimal.

Referring to Figure 8, we see there are two capacitors Ce and Cc. Both have two time-constants associated with them.

R_{10} as seen by Ce is $r_e||R_E||R_S = 25\Omega$

Therefore time constant associated with Ce $= \tau_{10} = 29\text{pF}.25\Omega = 725\text{psec}.$

R_{20} as seen by Cc is $R_C||R_L = 4.76\text{k}\Omega$

Therefore time constant associated with Cc $= \tau_{20}$

$= 5\text{pF}.4.76\text{k}\Omega = 2380\text{psec}.$

$$\omega_h = \frac{1}{\tau_{10} + \tau_{20}} = 2\pi \times 6.489MHz.$$

Figure 24.17

Therefore higher cut-off frequency = f_h = 6.489kHz.
Midband Voltage Gain w.r.t. source (shown previously)
=

$$\frac{\alpha_{fo} R_C || R_L}{(R_S + r_e)}$$

Figure 24.18

=

$$\frac{4760 \times 0.99}{50+25}$$

Figure 24.19

= 63.4
Internal Voltage Gain =

$$\frac{\alpha_{fo} R_C || R_L}{(R_S + r_e)} = 190.4$$

Figure 24.20

.
Note these are non-inverting gains.
In the lab, we will get vastly different gains by including source resistance and neglecting source resistance. So while making voltage gain measurement we have to be careful as to which gain we are measuring.

Chapter 25

AE_Lecture 5_Part C_continued_high frequency analysis of CE & CC[1]

AE_Lecture 5_Part C_continued_high frequency analysis of CE & CC

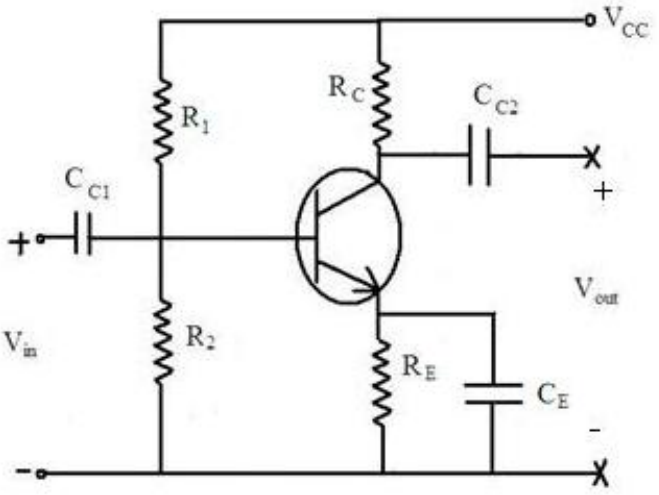


Figure 1 . RC-coupled CE BJT Amplifier

Figure 25.1

In Figure 1 we have RC-coupled CE BJT Amplifier. This has a Q point (I_{CQ} = 1mA, V_{CEQ} = 5V). The Hybrid- π parameters are same as in last chapter namely:

β **fo = incremental short circuit gain at low frequencies = 100;**

[1] This content is available online at <http://cnx.org/content/m34081/1.1/>.

Transit frequency given = f T = 200MHz;
At the Q point, C ob = C μ = C jBC =

$$C_c$$

Figure 25.2

= 5pF ;
Circular Transit Frequency = ω T =

$$\frac{1}{\tau_t} =$$

Figure 25.3

1.2566×10 9 radians/second;
Trans-conductance = g m =

$$\frac{I_C}{V_T} =$$

Figure 25.4

40mSiemens(or mS) =

$$\frac{1}{r_m}$$

Figure 25.5

= 1/25Ω;
Whereas

$$r_e = \frac{V_T}{I_E} = \frac{25mV}{\frac{1mA}{\alpha_F}} \approx 25\Omega$$

Figure 25.6

;

$$C_\pi = 29pF$$

Figure 25.7

Base spreading resistance is given as r x =100Ω ;

$$r_\pi = \frac{\beta_{fo}}{g_m} = 2.5k\Omega$$

Figure 25.8

The circuit elements are given as :
R_C = 5k, R_E = 2k, R_1 = 200k, R_2 = 60k, R_L = 100k , R_S = 50Ω,
R_B = R_1 || R_2=46k, $R_L^{'}$ = 5k||100k = 4.76k;
Under incremental condition, the circuit is represented as Figure 2. Bias Supply V_{CC} is shorted, coupling capacitances C_{C1} and C_{C2} are shorted and Emitter Bypass Capacitance C_E is is shorted.

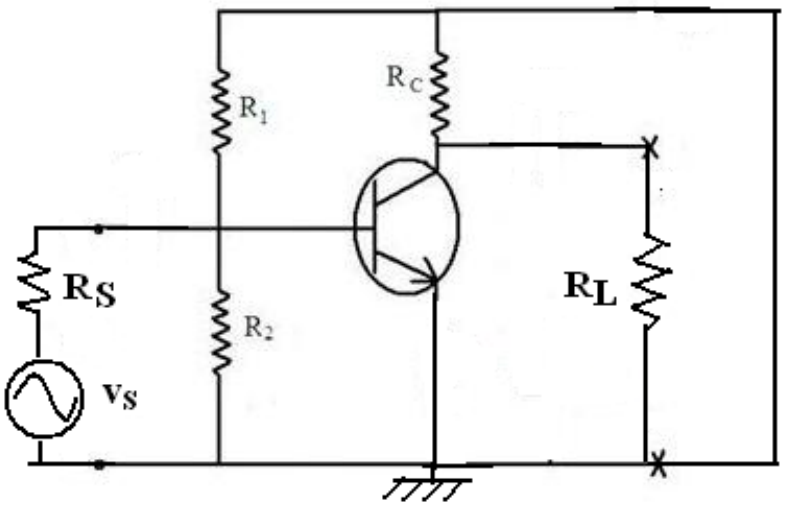


Figure 2 . Incremental Circuit representation of RC-coupled CE BJT Amplifier

Figure 25.9

For incremental analysis at high frequencies, BJT is replaced by its corresponding high frequency Hybrid-π Model as shown in Figure 3.

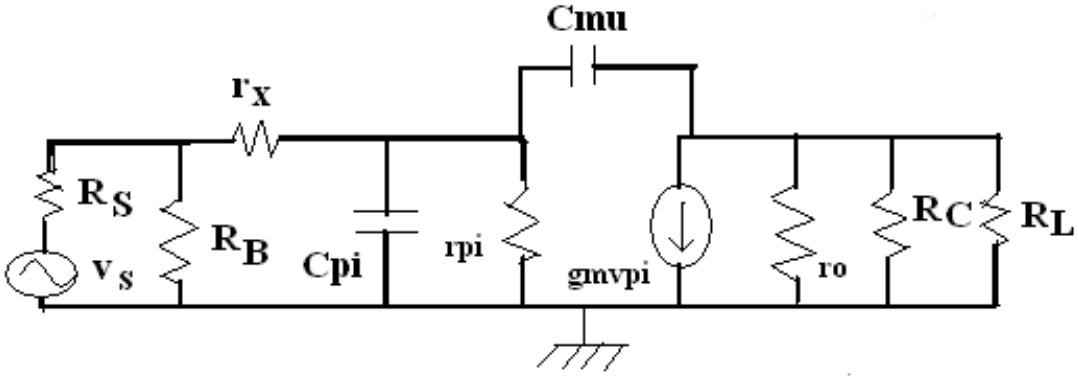


Figure 3. Incremental representation of RC-coupled CE Amplifier with BJT replaced by Hybrid-pi Model.

Figure 25.10

In the beginning of the Lecture 5 we have already discussed that the number of energy storage elements decide the order of the system and accordingly the number of poles. We have also discussed that in Low Pass Filter situation if the lowest pole is well below the higher poles then it is the dominant pole and it decides the higher -3dB frequency (f_h) and in High Pass Filter situation the highest pole decides the lower -3dB frequency (f_l).

In the present case by inspecting the incremental circuit diagram, we find two Capacitances , C_π and C_μ . Each has its open circuit time constant , τ_{10} and τ_{20} respectively.

Effective time constant $\tau_{eff} = \tau_{10} + \tau_{20}$;

Therefore ω_h =

$$\frac{1}{\tau_{10}+\tau_{20}}$$

Figure 25.11

= higher -3dB frequency ($2\pi f_h$);

Fortunately by applying Miller Transformation we can make single pole approximation of the incremental circuit.

By Miller Transformation, Cμ is transformed as:

$$C_\mu(1 - A_{V0})$$

Figure 25.12

at the input pair of nodes b[U+05F3] e and

$$\frac{C_\mu(1-A_{V0})}{A_{V0}}$$

Figure 25.13

at the output pair of nodes ce.

Here $A_{V0} = -g_m R_C||R_L$ = midband gain of the basic CE amplifier.

$$(1 - A_{V0})$$

Figure 25.14

is known as Miller Multiplicaion Factor and

$$C_\mu(1 - A_{V0})$$

Figure 25.15

is known as the Miller Capacitance.
Therefore total Capacitance appearing at the input node pair is:
$C_T = C_\pi +$

$$C_\mu(1 - A_{V0})$$

Figure 25.16

= 29pF +5pF(1+180)= 934pF;
Hence the incremental circuit is modified to the circuit shown in
Figure 4 with single pole approximation :

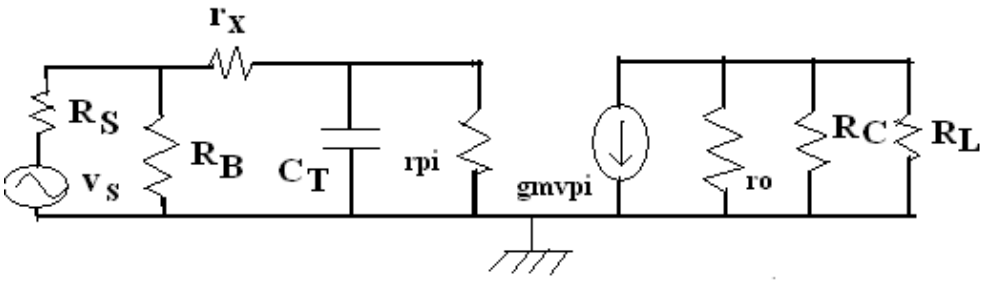


Figure 4. Incremental representation of RC-coupled CE Amplifier with single pole approximation using Miller Transformation.

Figure 25.17

The equivalent resistance seen by C_T by inspection is:

$$R_{10} = r_\pi || (r_x + R_S || R_B) = 141.4\ \Omega$$

Figure 25.18

;
Therefore ω_h =

$$\frac{1}{R_{10} C_T}$$

Figure 25.19

;
Thererfore $f_h = 1/0.8304\mu sec = 1.2MHz$;
The mid-frequency analysis gives the Midband Voltage Gain as :

$$A_{VS0} = -\frac{\beta_{f0}(R_C || R_L)}{(R_S + r_x + r_\pi)} = -\frac{100 \times 4.76k}{2650}$$

Figure 25.20

= -177.36;
A_{VO} = -183.076
High Frequency Analysis of CC Amplifier.
In Figure 5, the circuit configuration of CC Amplifier or more commonly known as Emitter Follower is given. This has a Voltage Gain of Unity hence it is always used as a Buffer with a very large input impedance and a very low output impedance. Hence emitter follower is ideal for driving variable loads and transmission lines. This also helps isolate the load from the Amplifier Circuit thereby ensuring maximum voltage gain of the Amplifier Circuit. If the load is not isolated then loading will occur and Voltage Gain will fall.

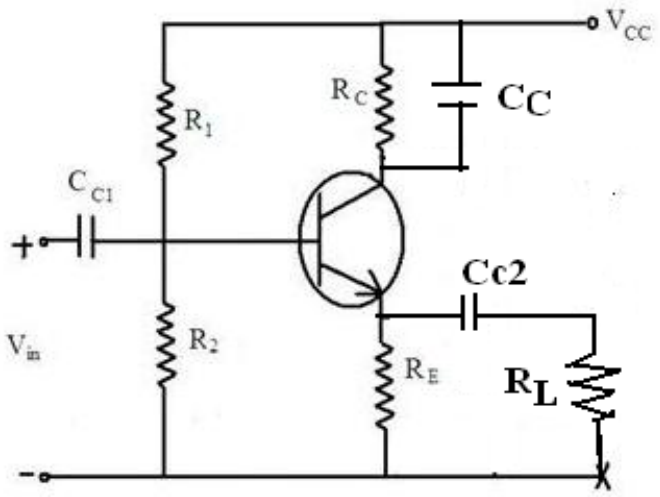


Figure 5 . RC-coupled CCBJT Amplifier

Figure 25.21

The incremental representation of CC BJT Amplifier is given
in Figure 6. In the incremental representation, biasing Battery is treated as short. C_{C1} , C_{C2} and C_C are also treated as a short circuit.

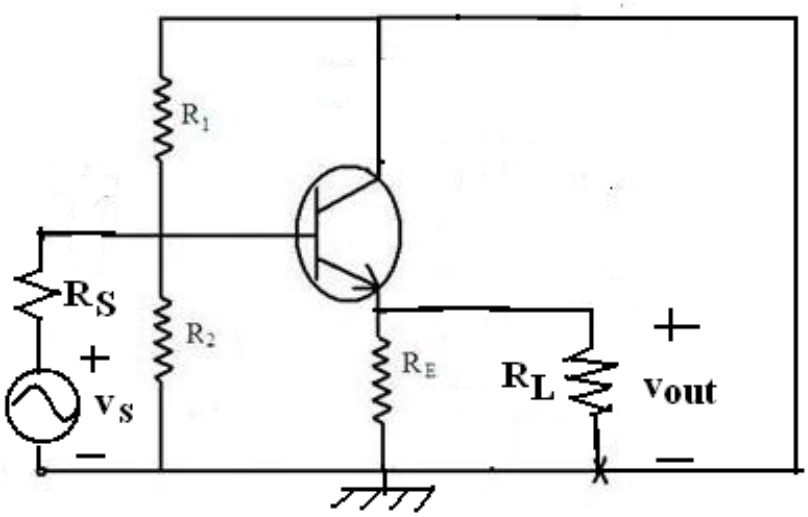


Figure 6 . RC-coupled CCBJT Amplifier

Figure 25.22

Replacing BJT by Hybrid-π model we get the incremental representation as shown in Figure 7.

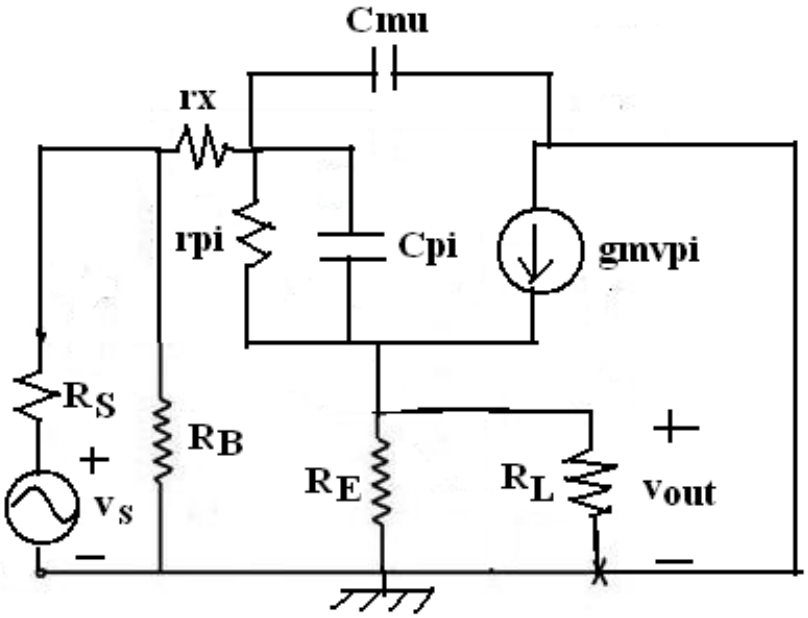


Figure 7 . Incremental Model of CC Amplifier applicable at mid and high frequencies.

Figure 25.23

By inspection we see that we have capacitances ; C_π and C_μ . They have their associated open circuit time constants τ_{10} and τ_{20} . For determining these time constants we must know the open circuit resistances seen by C_π and C_μ .

The equivalent resistance R_{10} is seen by C_π can be determined from Figure 8.

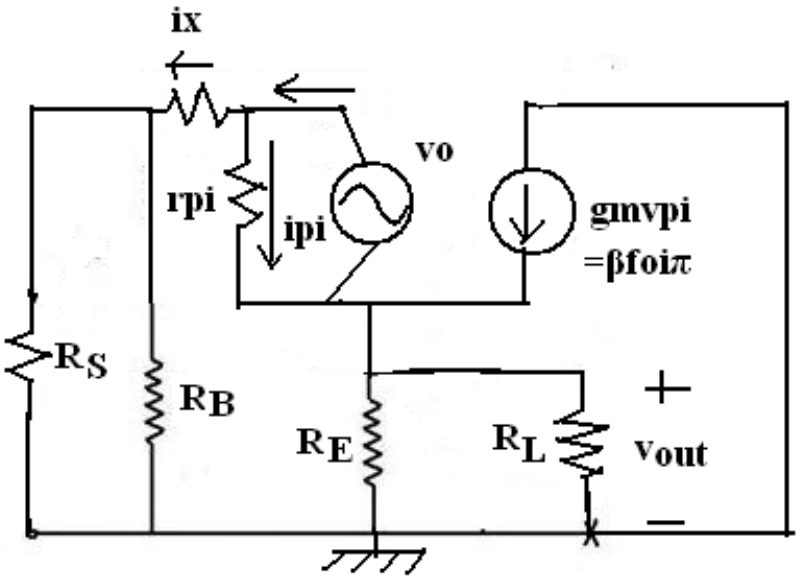


Figure 8 . The circuit topology for determining the equivalent resistance seen by Cpi.

Figure 25.24

Total current drawn from the voltage source v_o is $i_o = i_x + i_\pi$;
Where i_π =

$$\frac{v_o}{r_\pi}$$

Figure 25.25

;
And in the second path of base spreading resistance (r_x) :
We have $v_o = i_x (r_x + R_S||R_B + R_E||R_L) - \beta_{fo} i_\pi R_E$
$= i_x (r_x + R_S||R_B + R_E||R_L) - \beta_{fo} \times R_E \times$

$$\frac{v_o}{r_\pi}$$

Figure 25.26

$= i_x\ (r_x + R_S||R_B + R_E||R_L) - g_m \times R_E \times$

$$\frac{v_o}{1}$$

Figure 25.27

Rearranging the terms we get: $v_o/i_x =$

$$\frac{r_x+R_S||R_B+R_E||R_L}{1+g_mR_E}$$

Figure 25.28

Therefore R_{10}

$$= r_\pi||\left(\frac{r_x+R_S||R_B+R_E||R_L}{1+g_mR_E}\right)$$

Figure 25.29

Substituting the parameter and element values we get :
R_{10}

$$= 2.5k\left|\left|\left(\frac{100+50+2k}{1+\frac{2000}{25}}\right) = 2.5k\right|\right|\left(\frac{2150}{81}\right) = 26.54\ \Omega$$

Figure 25.30

The equivalent resistance seen by C_μ is R_{20} . This equivalent resistance can be determined by the Figure 9.

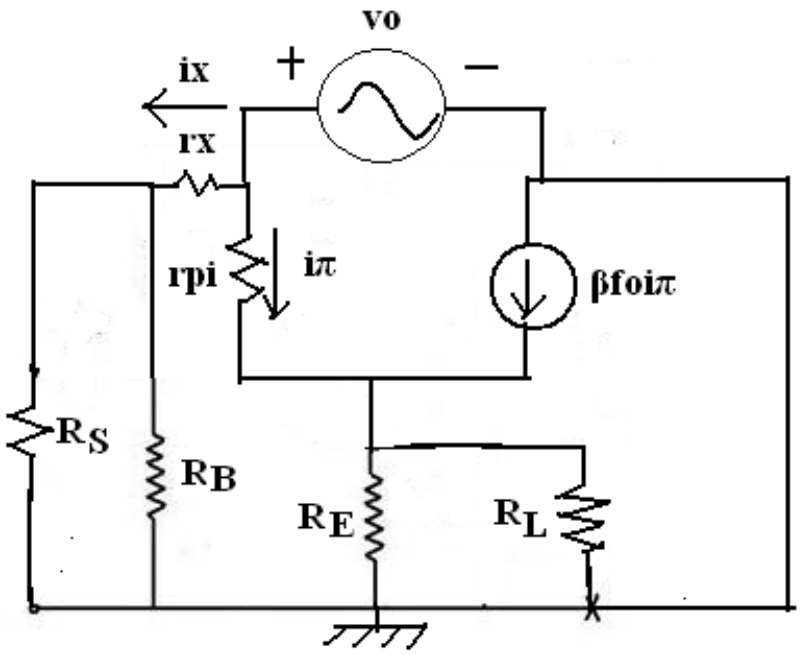


Figure 9. The equivalent circuit from which R20, the resistance seen by Cmu, is determined.

Figure 25.31

By inspection we see that there are two currents flowing out of the source v_0 . The two currents are i_x and i_π .

The current i_x sees the resistance $(r_x + R_S||R_B)$.

The current i_π sees the resistance $[r_\pi + (1+\beta_{fo})\ R_E||R_L]$.

Therefore $R_{20} = (r_x + R_S||R_B)||\ [r_\pi + (1+\beta_{fo})\ R_E||R_L]$

Substituting the parameter values and element values in the above equation we get:

$R_{20} = (100 + 50)||\ [2500 + (1+100)\ 2000] = 150\Omega$

Therefore $\tau_{10} = R_{10}\times C_\pi = 26.54\Omega\times 29pF = 769.66psec.$

And $\tau_{20} = R_{20}\times C_\mu = 150\Omega\times 5pF = 750psec.$

Therefore $f_h =$

$$\frac{1}{2\pi(\tau_{10}+\tau_{20})} = \frac{1}{2\pi(1.51966nsec)} = 104.73MHz$$

Figure 25.32

Referring to Figure 6, we can determine the midband overall gain:

$$A_{vso} = \frac{(1+\beta_{fo})(R_E||R_L)}{R_S+r_x+r_\pi+(1+\beta_{fo})(R_E||R_L)}$$

Figure 25.33

≈ 1

Here we have assumed that loading by R_B has been removed by boot-strapping technique. As can be seen from the formula above, the internal gain and overall gain including R_S is the same.

Determination of the output impedance of CC Amplifier:

Determination of the output impedance of CE and CB is quite straight forward.

R_{out} =

$$\frac{1}{h_{oe}}$$

Figure 25.34

in CE Amplifier. The default value of

$$\frac{1}{h_{oe}}$$

Figure 25.35

= 40k.

R_{out} =

$$\frac{1}{h_{ob}}$$

Figure 25.36

in CB Amplifier. The default value of

$$\frac{1}{h_{ob}}$$

Figure 25.37

= 2M.

For CC amplifier we will have to go to the incremental model with source inactivated and a source v_o applied at the output pair of nodes as shown in Figure 10:

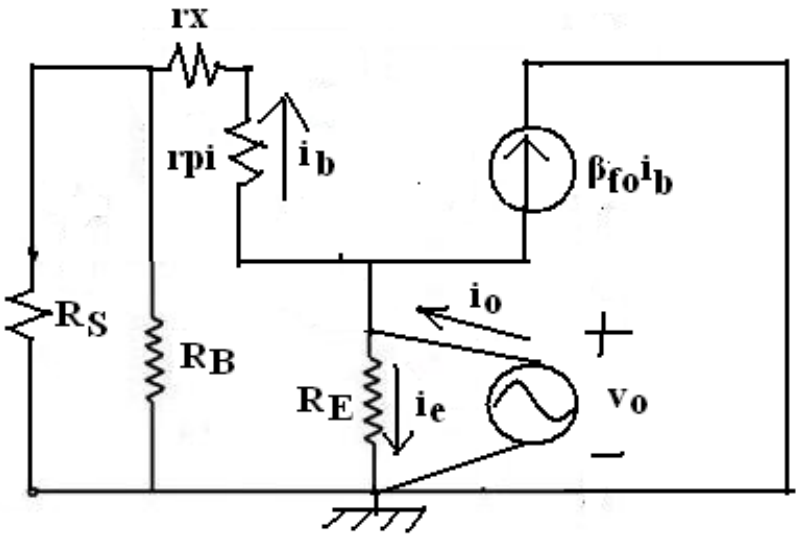


Figure 10 . The incremental circuit for determining the output impedance of CC Amplifier.

Figure 25.38

By inspection we see that output current from the applied source is flowing through three paths:

Through R_E we have i_e flowing.
Through $(r_\pi + r_x + R_S||R_B)$ we have i_b (controlling current) flowing.
Through controlled source we have $\beta_{fo} i_b$ flowing.
Hence total current $i_o = i_e + i_b + \beta_{fo} i_b$
$= v_o($

$$\frac{1}{R_E} + \frac{1}{r_\pi + r_x + R_S} + \frac{\beta_{fo}}{r_\pi + r_x + R_S}) =$$

Figure 25.39

$v_o($

$$\frac{1}{R_E} + \frac{1+\beta_{fo}}{r_\pi + r_x + R_S})$$

Figure 25.40

Therefore R_{out} as seen by v_o is

$$R_E || \frac{(r_\pi + r_x + R_S)}{(1+\beta_{fo})}$$

Figure 25.41

$\approx$

$$\frac{1}{g_m}$$

Figure 25.42

$= 25\Omega$.
Hence output impedance of CC Amplifier is 25Ω but input impedance is $200k\Omega$. Therefore CC Amplifier acts as voltage controlled voltage source with unity voltage gain hence it is ideal for BUFFER applications as well as for driving transmission lines and for driving variable loads.

In Table 1, we make a comparative study of the performance parameters of the three configurations of BJT Amplifier.

Table 1. Comparative study of the performance parameters of CE,CB and CC amplifier.

	A_{VSO} (Overall gain)	A_{VO} (Internal gain)	Band width	R_{in}	R_{out}
CE	-177.36	-183.07	1.2MHz	2.6k	40k= $1/h_{oe}$
CB	63.4	190.4	6.5MHz	25Ω	2M = $1/h_{ob}$
CC	0.987	0.987	104.73MHz	204.6k	25Ω

Table 25.1

As can be seen from the Table 1, the internal gain and overall gain are different only in CB. In the remaining two configurations the gains are approximately the same.

Also Open Circuit Time Constant method gives a conservative value of upper -3dB frequency and Short Circuit Time Constant method also gives a conservative value of lower -3dB frequency. The actual BW is 1.1 times larger than the calculated values.

Chapter 26

AE_Lecture 5_Part C_continued_Simulated Frequency Domain Study of CB,CE,Emitter Degenerate Amplifier and CC Amplifier.[1]

AE_Lecture 5_Part C_continued_Simulated Frequency Domain Study of CB,CE,Emitter Degenerate Amplifier and CC Amplifier.

In this Lecture , we carry out the frequency domain studies of Common Base, Common Emitter, Emitter Degenerate Amplifier and Common Collector Amplifier. These studies had been carried in Laboratory also. We find that the frequency response Band Width of the two studies have a remarkable correspondence. The simulation has been carried out using Multisim Simulation Software marketed by National Instruments.

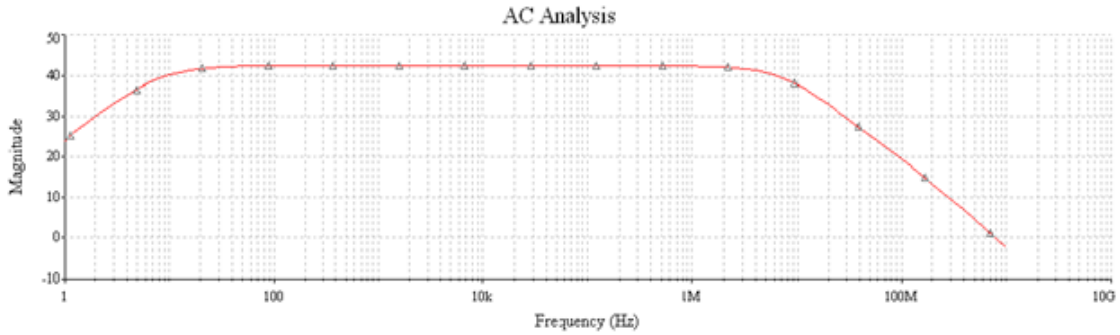


Figure 1. Gain Magnitude Frequency Response Curve of CE Amplifier.
y-axis: Gain Magnitude in dB;
x-axis: Frequency Plot in logrithmic Scale;

Figure 26.1

[1]This content is available online at <http://cnx.org/content/m34083/1.1/>.

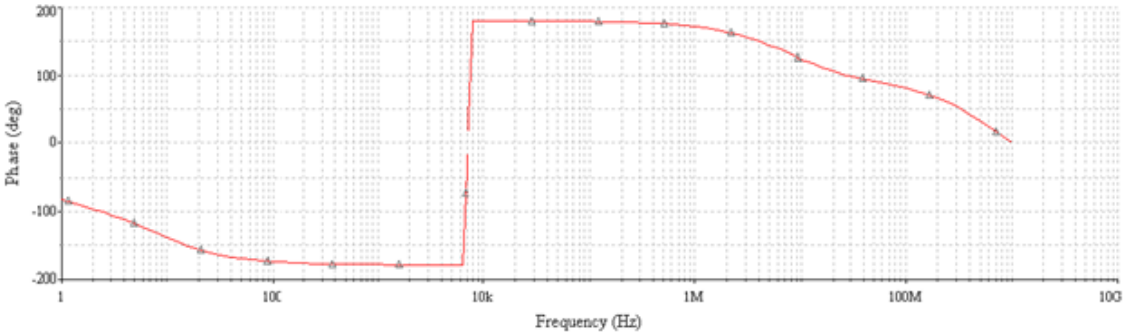


Figure 1.b. Phase of Gain vs Frequency of CE Amplifier.
y-axis: Phase of Gain in dB;
x-axis: Frequency plot on logrithmic scale.

Figure 26.2

Common Emitter Circuit Schematics is given in Figure 1c. The Gain Magnitude Plot and Gain Phase plot are given in Figure 1 and 1b.

By inspecting Figure 1 we find a Band-width of 5Mhz. The midband gain is 43dB and -3dB frequencies are i.e. 40dB frequencies are 10Hz and 5Mhz.

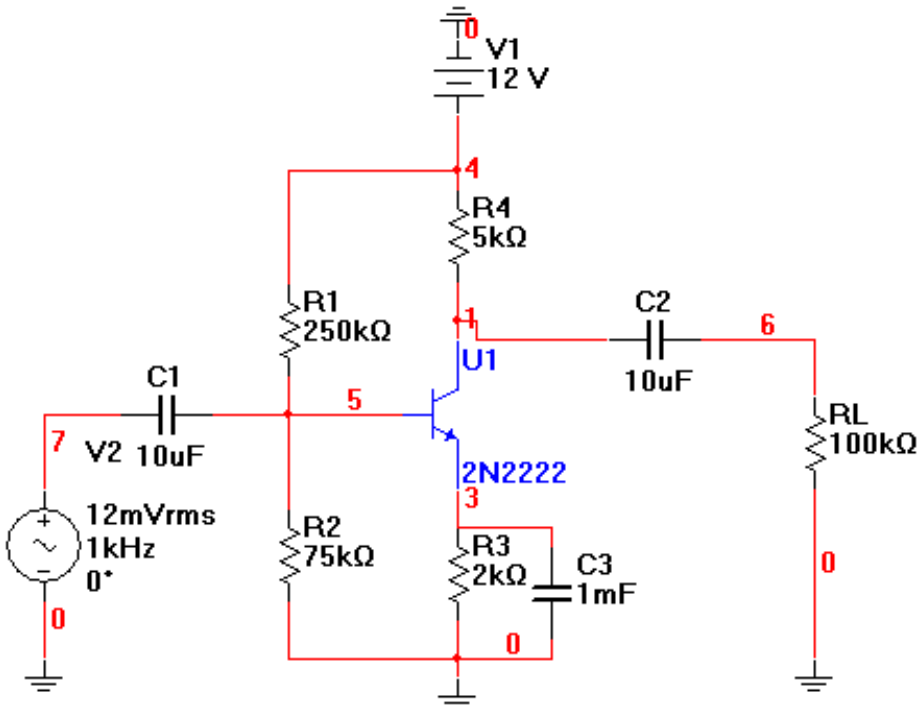


Figure 1.c. Circuit Schematics of CE Amplifier.

Figure 26.3

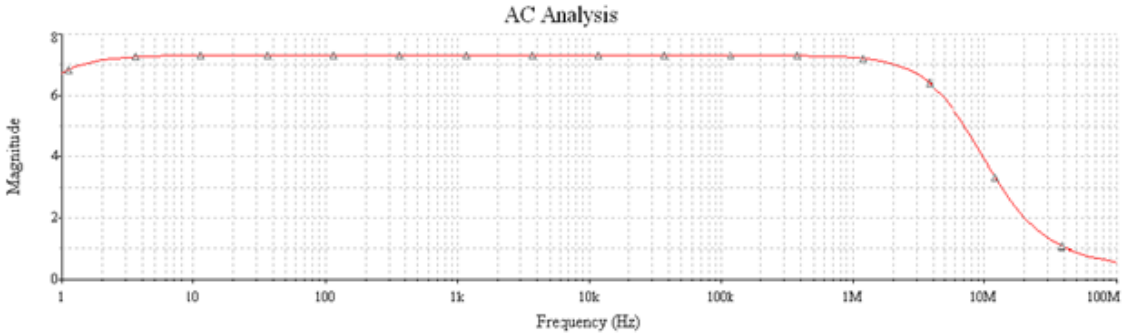


Figure 2. Gain Magnitude Frequency Response Curve of Emitter Degenerate Amplifier.
y-axis: Gain Magnitude in dB;
x-axis: logrithmic frequency plot in Hz;

Figure 26.4

Emitter Degenerate Circuit Schematics is given in Figure 2c. The Gain Magnitude Plot and Gain Phase plot are given in Figure 2 and 2b.

By inspecting Figure 2 we find a Band-width of 10Mhz. The midband gain is 7dB and -3dB frequencies are i.e. 4dB frequencies are (less than 1Hz) and 10Mhz.

Emitter Degenerate Amplifier is a negative feedback amplifier with current-series feedback. The improvement is little less than $2\times$.

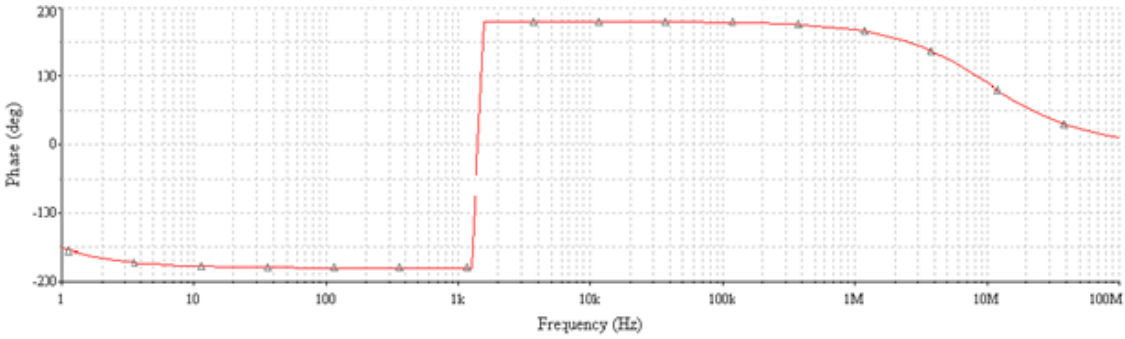


Figure 2b. Phase of the Gain of Emitter Degenerate Amplifier vs Frequency Response Curve.
y-axis:Phase of Gain in degrees;
x-axis: logrithmic plot of frequency in Hz;

Figure 26.5

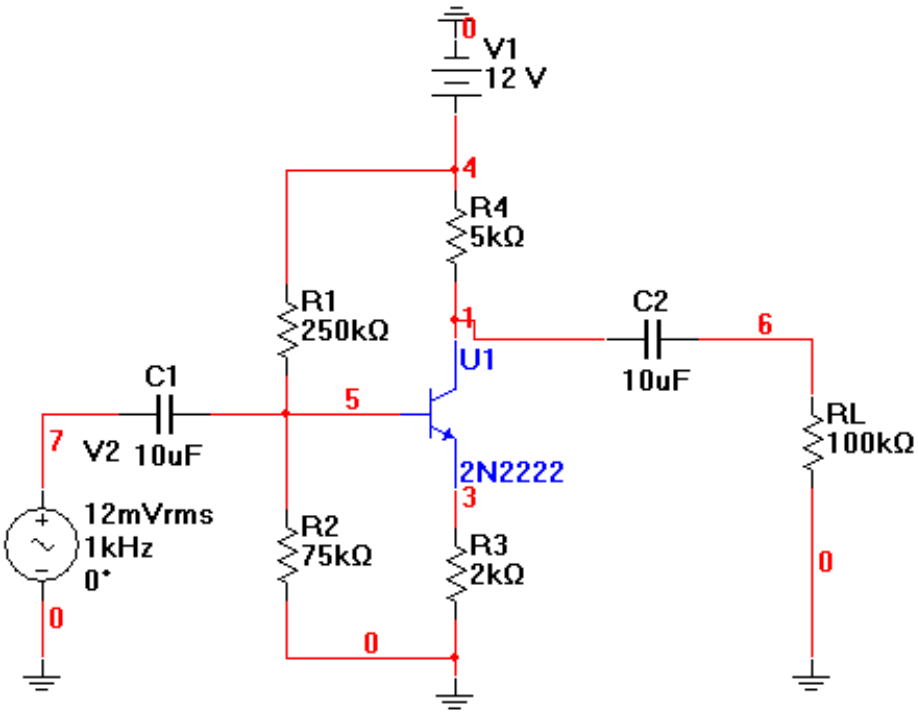


Figure 2.c.Circuit Schematics of Emitter Degenerate Ampl.

Figure 26.6

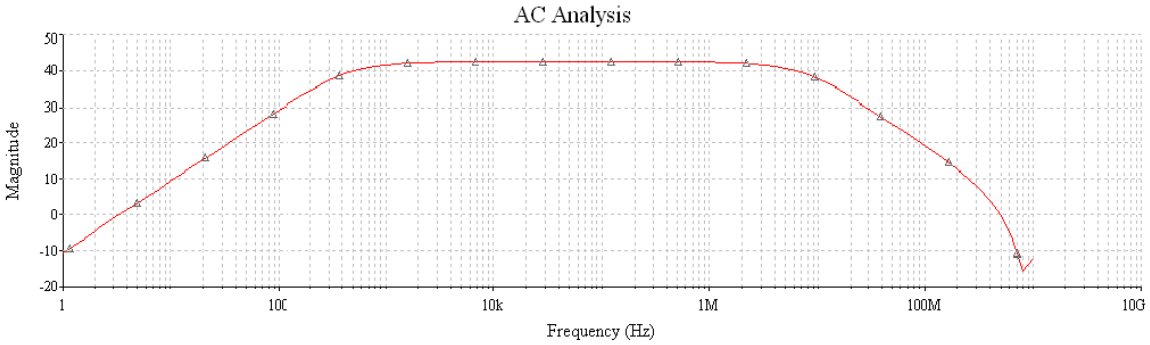


Figure 3. Gain Magnitude Frequency Response Curve of CB Amplifier
y-axise: Gain Magnitude in dB; x-axis: Frequency Plot on logrithmic scale;

Figure 26.7

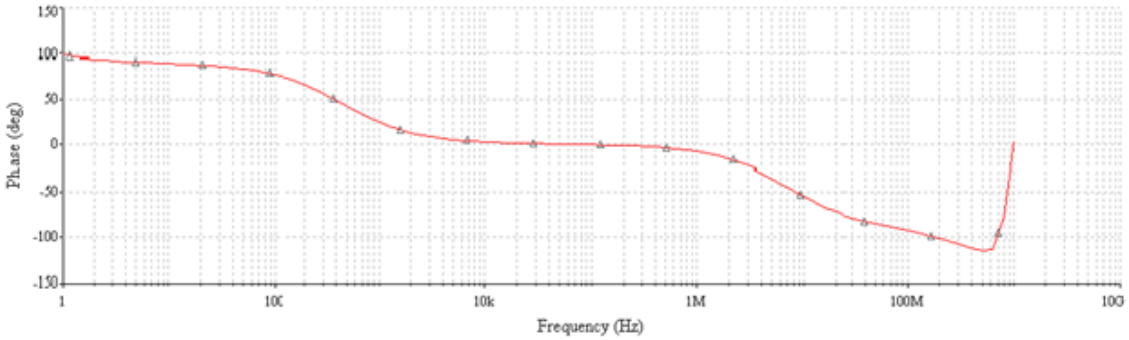


Figure 3.b. Phase of Gain vs frequency plot of CB Amplifier.
y-axis: Phase of Gain in degrees; x-axis: frequency plot on logrithmic scale.

Figure 26.8

Common Base Circuit Schematics is given in Figure 3c. The Gain Magnitude Plot and Gain Phase plot are given in Figure 3 and 3b.

By inspecting Figure 3 we find a Band-width of 5Mhz. The midband gain is 43dB and -3dB frequencies are i.e. 40dB frequencies are 500Hz and 5Mhz.

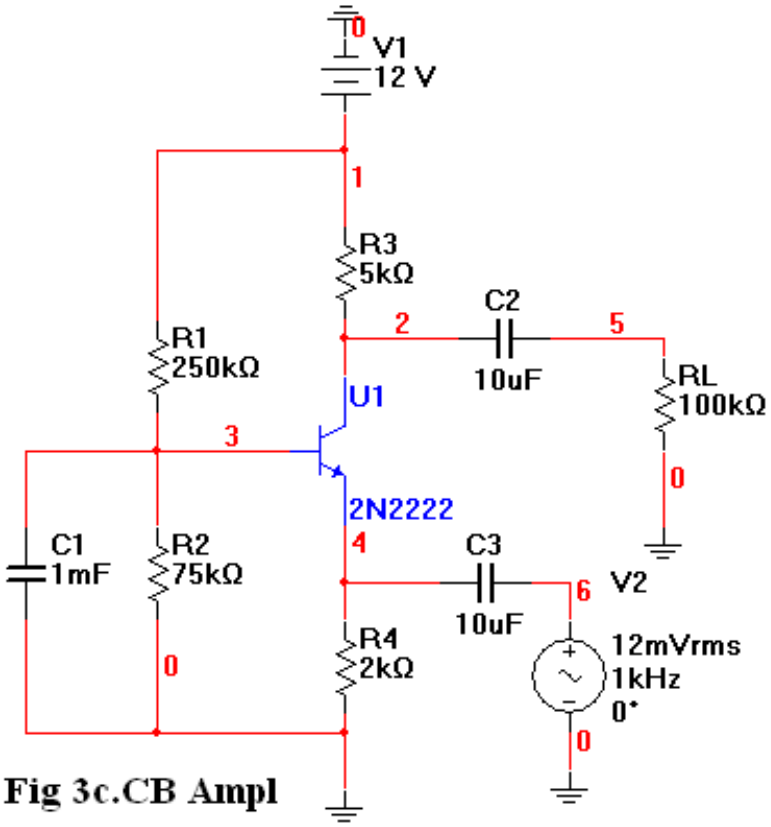

0
V1
12 V
1
R3
5kΩ
C2
2
5
10uF
R1
250kΩ
U1
RL
100kΩ
3
0
2N2222
C1
1mF
R2
75kΩ
4
C3
6
V2
10uF
R4
2kΩ
12mVrms
1kHz
0°
0
0
Fig 3c.CB Ampl

Figure 26.9

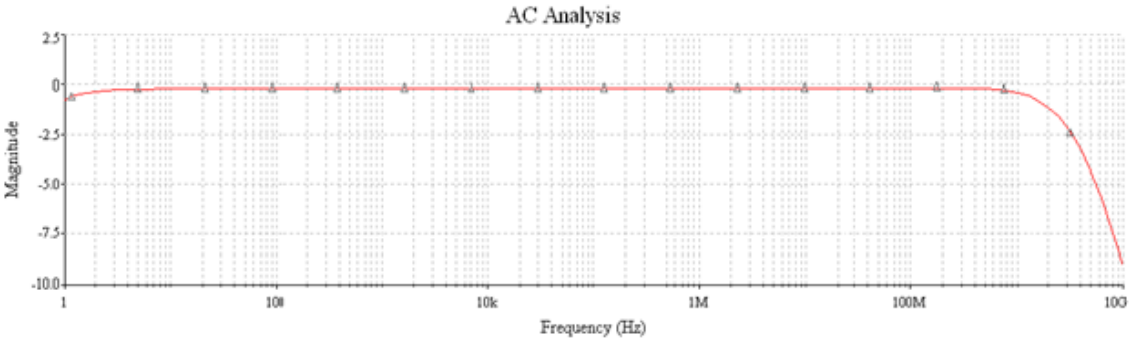


Figure 4. Gain Magnitude Plot in dB of CC Amplifier.
y-axis: Gain Magnitude in dB; x-axis: Frequency plot on logrithmic scale.

Figure 26.10

Common Collector Circuit Schematics is given in Figure 4c. The Gain Magnitude Plot and Gain Phase plot are given in Figure 4 and 4b.

By inspecting Figure 1 we find a Band-width of 4GHz. The midband gain is 0dB and -3dB frequencies are (less than 1Hz) and 4GHz.

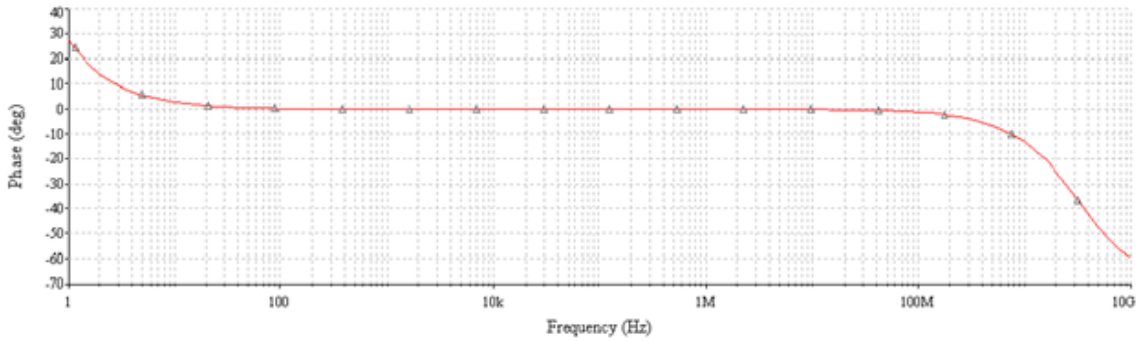


Figure 4.b. Phase of Gain of CC Amplifier vs Frequency.
y-axis: Phase of Gain in degrees; x-axis: Frequency Plot on logrithmic scale.

Figure 26.11

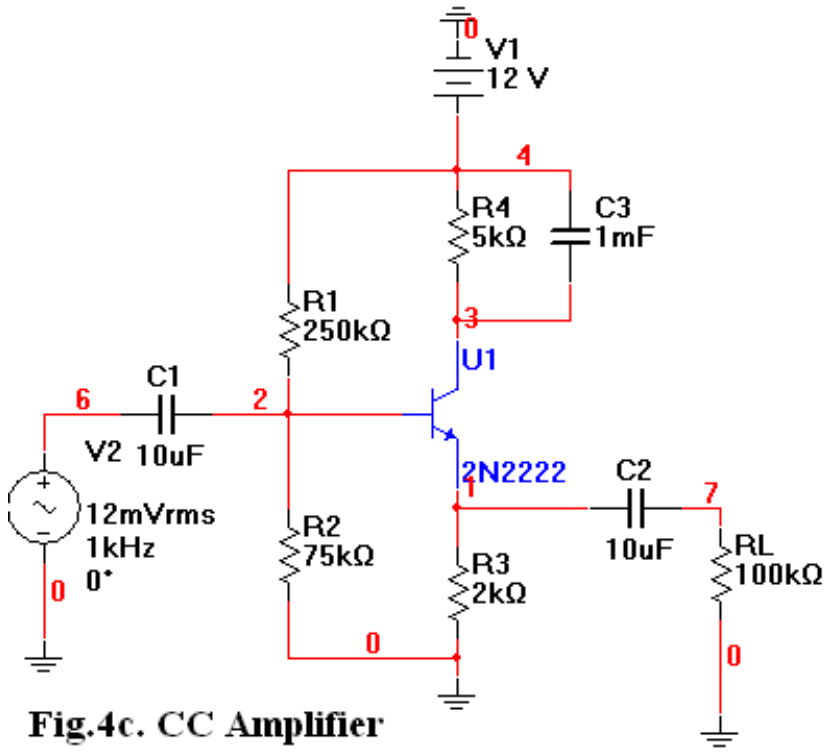

0
V1
12 V
4
R4
5kΩ
C3
1mF
R1
250kΩ
3
U1
C1
6
2
V2
10uF
2N2222
C2
1
7
12mVrms
1kHz
0°
R2
75kΩ
R3
2kΩ
10uF
RL
100kΩ
0
0
0
Fig.4c. CC Amplifier

Figure 26.12

Chapter 27

AE_Lecture 5_Part C_continued_High frequency analysis of CB.[1]

AE_Lecture 5_Part C_continued_High frequency analysis of CB.

In this continuation of high frequency application, we use the same self-biasing configuration to achieve CB, CE and CC amplifier. These three Circuit Configuration have the same Q point (I_{CQ} = 1mA , V_{CEQ} = 5V). Hence they have the same Hybrid-π parameters in all three configurations namely:

β fo = incremental short circuit gain at low frequencies = 100;

Transit frequency given = f T = 200MHz;

At the Q point, C ob = C μ = C jBC =

$$C_c$$

Figure 27.1

= 5pF ;

Circular Transit Frequency = ω T =

$$\frac{1}{\tau_t} =$$

Figure 27.2

1.2566×10 9 radians/second;

Here it may be noted that reciprocal of frequency gives Time Period of repetition T but reciprocal of circular frequency always gives the Time –Constant. In filters the reciprocal of circular cut-off frequencies gives the RC time constant of the associated RC configuration. Here the reciprocal of the circular transit frequency gives the transit time across the narrow base of the BJT .

[1] This content is available online at <http://cnx.org/content/m33873/1.2/>.

Transit Time =

$$\tau_t = \frac{1}{1.2566 \times 10^9} =$$

Figure 27.3

0.8nsec;
Trans-conductance = g m =

$$\frac{I_C}{V_T} =$$

Figure 27.4

40mSiemens(or mS) =

$$\frac{1}{r_m}$$

Figure 27.5

= 1/25Ω;
Whereas

$$r_e = \frac{V_T}{I_E} = \frac{25mV}{\frac{1mA}{\alpha_F}} \approx 25\Omega$$

Figure 27.6

;

$$\frac{C_{\mu} + C_{\pi}}{g_m} = 0.8nsec$$

Figure 27.7

Therefore

$$C_{\pi} \times 25 = 0.8 \times 10^{-9} - 5 \times 10^{-12} \times 25 = 0.725nsec$$

Figure 27.8

Therefore

$$C_{\pi} = C_e = 29pF$$

Figure 27.9

Base spreading resistance is given as r x =100Ω ;

$$r_{\pi} = \frac{\beta_{fo}}{g_m} = 2.5k\Omega$$

Figure 27.10

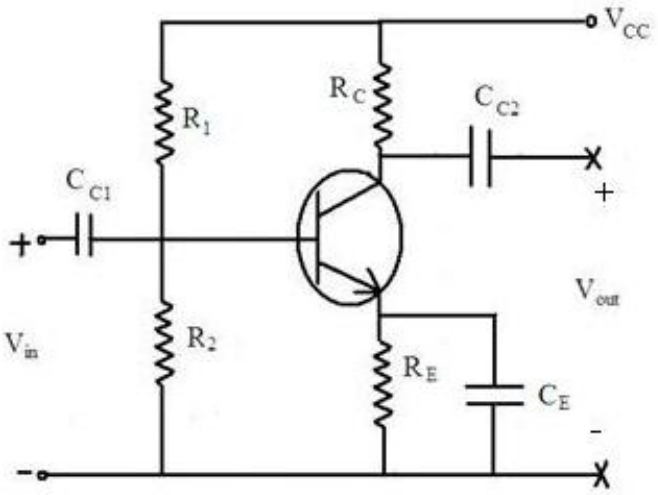


Figure 1 . RC-coupled CE BJT Amplifier

Figure 27.11

Self –biasing configuration is connected as CE BJT Amplifier by the use of Emitter bypass capacitance C_E.

The circuit elements are given as :

$R_C = 5k$, $R_E = 2k$, $R_1 = 200k$, $R_2 = 60k$, $R_L = 100k$, $R_S = 50\Omega$,

$R_B = R_1 \,||\, R_2 = 46k$, $R_L' = 5k||100k = 4.76k$;

The same configuration can be connected as CB Amplifier by the use of Base bypass capacitance C_B as shown in the Figure 3. The same configuration can be connected as CC Amplifier by the use of Collector bypass capacitance C_C as shown in the Figure 4.

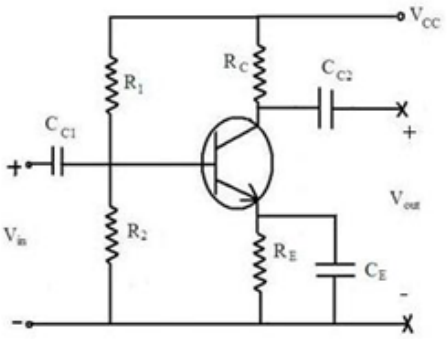


Figure 2 . RC-coupled CE BJT Amplifier

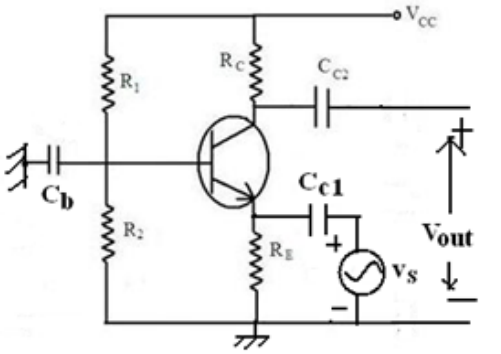


Figure 3 . RC-coupled CB BJT Amplifier

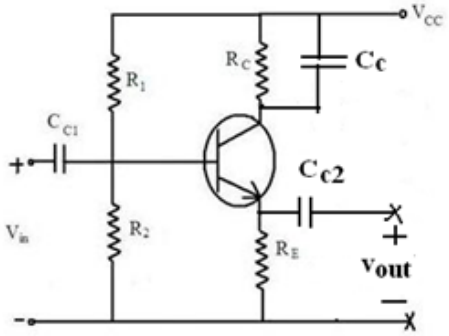


Figure 4 . RC-coupled CC BJT Amplifier

Figure 27.12

High Frequency Analysis of CB Amplifier:

Under incremental condition (refer to Figure 3),

C_B shorts out R_1 and R_2 . Coupling capacitors appear as short circuit. Battery V_{CC} appears as short circuit. Hence the incremental circuit of CB amplifier is the following as shown in Figure 5 :

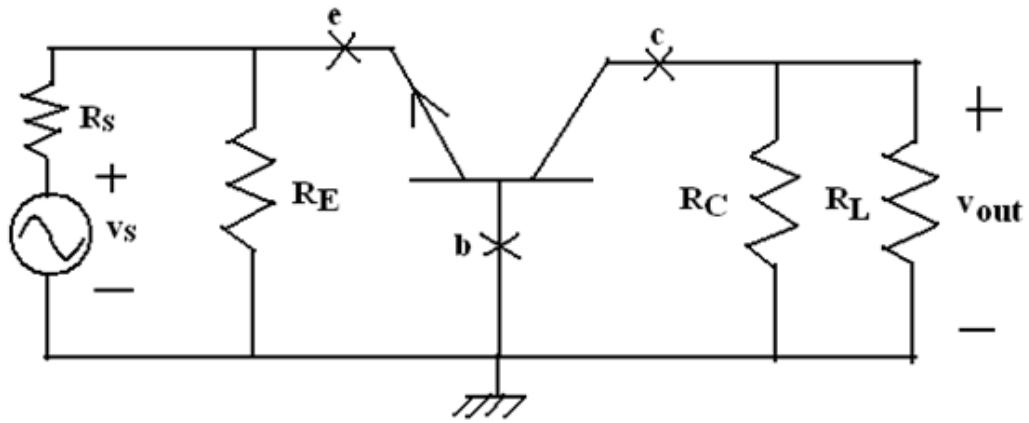


Figure 5. Incremental circuit representation of CB Amplifier.

Figure 27.13

For circuit analysis we replace CB configuration of BJT with its corresponding T-Model as shown in Figure 6.

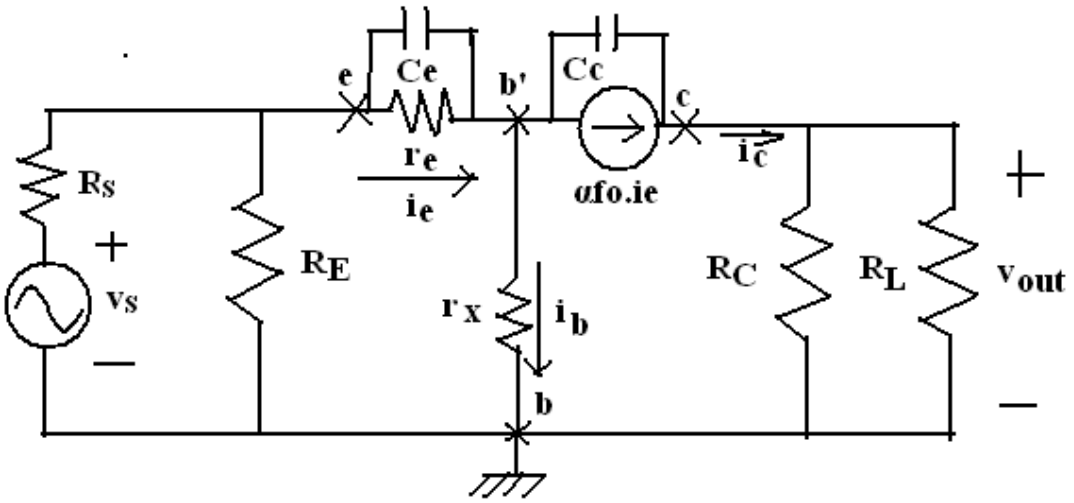


Figure 6 . Incremental circuit representation of CB Amplifier with T-Model of CB BJT.

Figure 27.14

In Figure 6, b[U+05F3] is the active base region and b is the external base terminal. The T-Model is further re-oriented as two input and output loop as shown in Figure 7.αfo

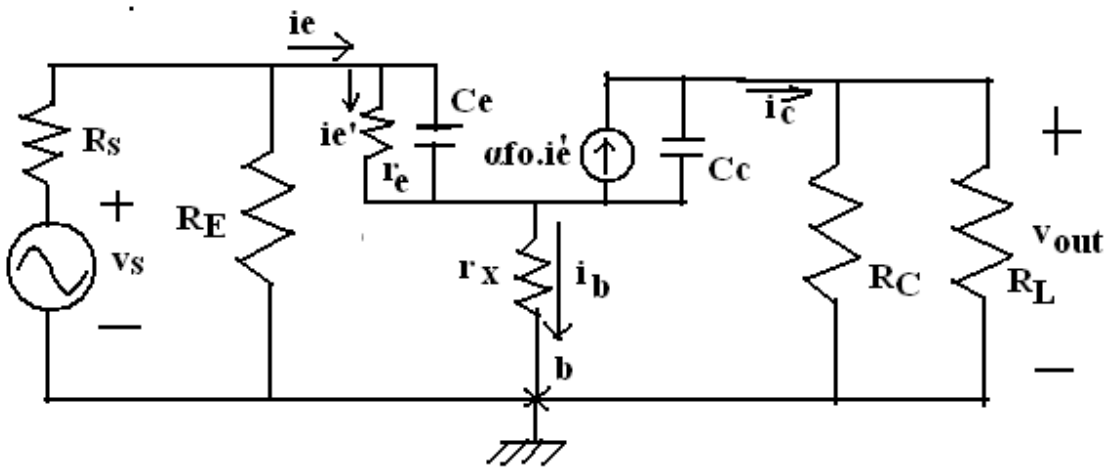


Figure 7. Incremental circuit representation of CB Amplifier with input-output loop.

Figure 27.15

The T-Model of CB BJT is further simplified into two non-interacting loops as shown in Figure 8.

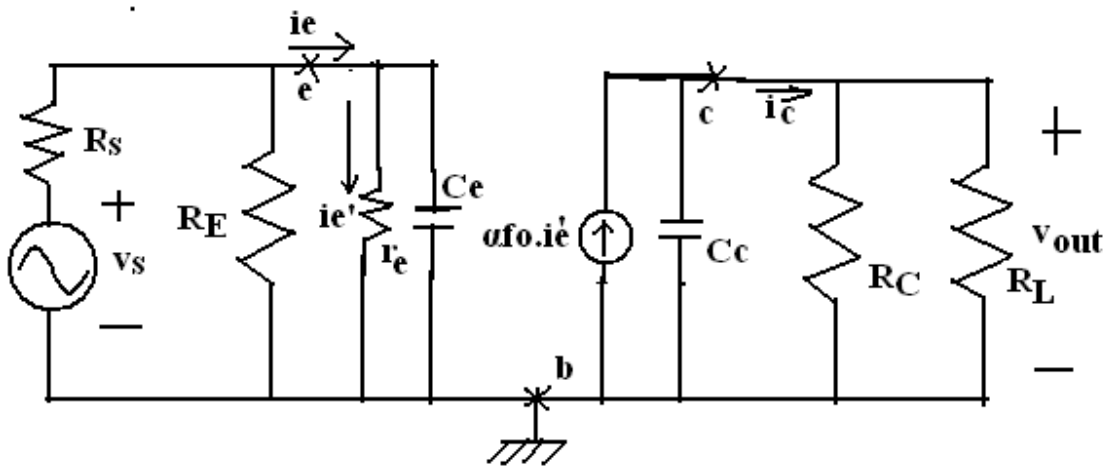


Figure 8 . Incremental circuit representation of CB Amplifier with non-interacting loop

Figure 27.16

Base spreading resistance r_x is reflected as $(1\text{-}\alpha_{fo})r_x$ in input loop and in output loop it is not reflected since it is controlled loop. Since $(1\text{-}\alpha_{fo})r_x$ is a negligible resistance hence in input loop it has been completely neglected as a result the input and output loops are completely non-interacting. This is the reason reverse transmission factor is almost non-existent in CB BJT and it is a near-Unilateral device. Hence it is very suitable for RF applications. RF Amplifier are very prone to parasitic oscillations. But if we use a Unilateral Active Device the possibility of parasitic oscillation is minimal.

Referring to Figure 8, we see there are two capacitors Ce and Cc. Both have two time-constants associated with them.

R_{10} as seen by Ce is $r_e||R_E||R_S = 25\Omega$

Therefore time constant associated with Ce = τ_{10} = 29pF.25Ω=725psec.

R_{20} as seen by Cc is $R_C||R_L = 4.76k\Omega$

Therefore time constant associated with Cc = τ_{20}

=5pF.4.76kΩ=2380psec.

$$\omega_h = \frac{1}{\tau_{10} + \tau_{20}} = 2\pi \times 6.489MHz.$$

Figure 27.17

Therefore higher cut-off frequency = f_h = 6.489kHz.

Midband Voltage Gain w.r.t. source (shown previously)
=

$$\frac{\alpha_{fo} R_C || R_L}{(R_S + r_e)}$$

Figure 27.18

=

$$\frac{4760 \times 0.99}{50+25}$$

Figure 27.19

= 63.4
Internal Voltage Gain =

$$\frac{\alpha_{fo} R_C || R_L}{(R_S + r_e)} = 190.4$$

Figure 27.20

.
Note these are non-inverting gains.
In the lab, we will get vastly different gains by including source resistance and neglecting source resistance. So while making voltage gain measurement we have to be careful as to which gain we are measuring.

Chapter 28

AE_Lecture5_PartD_Bootstrapping and Darlington Pair.[1]

AE_LECTURE9_Bootstrapping & Darlington Pair Configuration of BJT.

For instrumentation application and particularly for constructing Vacuum Tube VoltMeter(VTVM) typ meters the input stage must offer a very large input impedance of the order of tens of megohms. To achieve this goal we go for emitter follower but emitter follower uses self biasing and the potential divider network made of R1 and R2 considerable load the input impedance of emitter follower thereby making the goal of high input impedance of the order of tens of megaohms unattainable. To overcome this problem we resort to Bootstrapping.

BOOT STRAPPING TECHNIQUE for improving the input impedance of EMITTER FOLLOWER.

[1] This content is available online at <http://cnx.org/content/m31651/1.1/>.

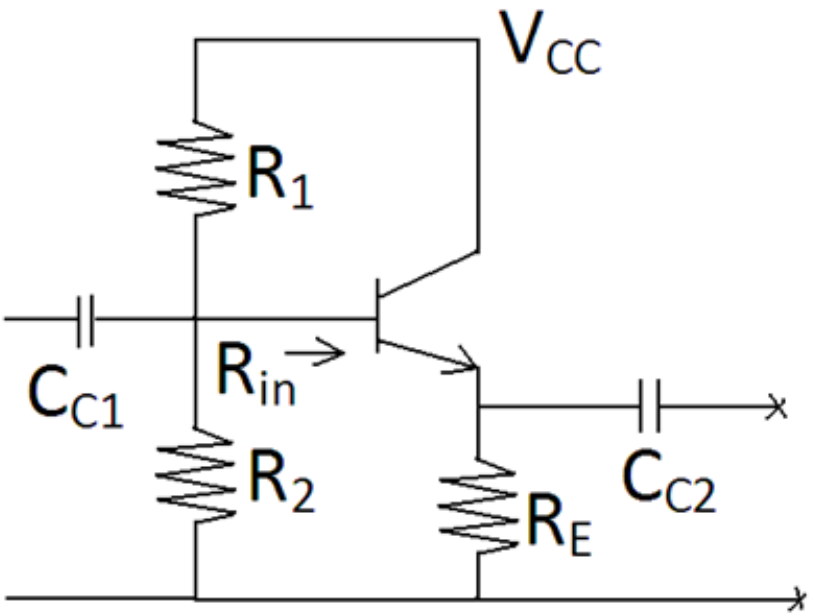


Figure 1. The conventional emitter follower circuit.

Figure 28.1

$$R_{in} = r_x + r_\pi + (1 + \beta_{fo})R_E$$

Figure 28.2

$R_1||R_2 loads\ R_{in}$ *and the advantage*

Figure 28.3

But

is lost .We use bootstrapping to maintain high

R_{in}.

Figure 28.4

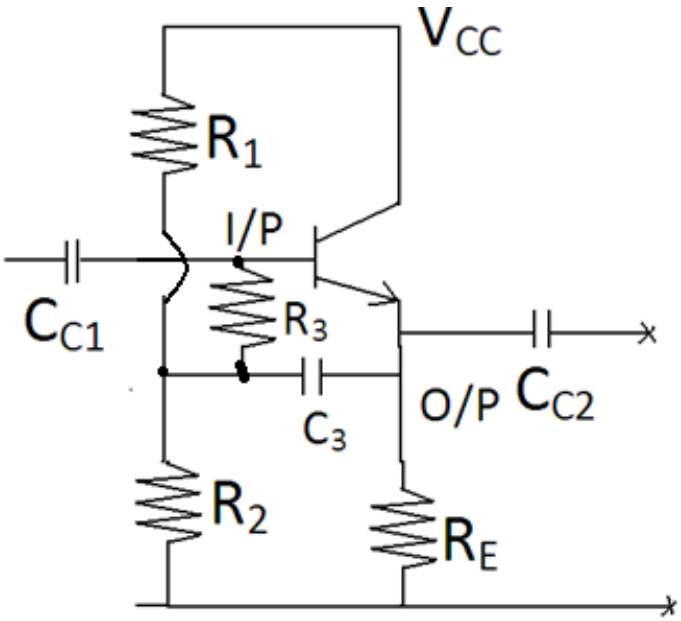


Figure 2. An emitter follower circuit with boot-strapping.

Figure 28.5

A resistance R_3 is connected between I/P and O/P of the amplifier. Here O/P connection is through a coupling capacitance hence it is only AC connection and not DC therefore Q point remains undisturbed. R_1 and R_2 provide the base biasing as before.

By Miller Transformation:-

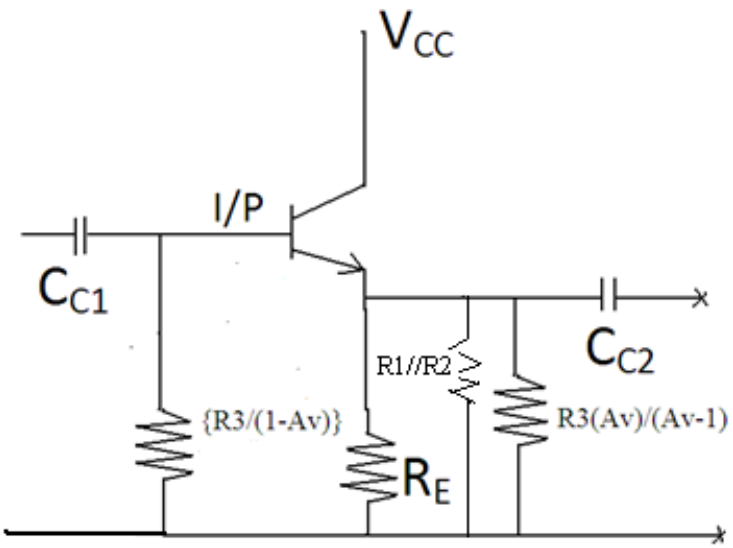


Figure 3. Miller Transformation of R3 to I/P node pair and O/P node pair.

Figure 28.6

Now

$$\left(\frac{R_s}{1-A_V}\right) \gg R_{in}$$

Figure 28.7

So high input impedence of

$$R_{in} = r_x + r_\pi + (1+\beta_{fo})R_E$$

Figure 28.8

is fully realized without being loaded by the biasing network consisting of

$$R_1$$

Figure 28.9

,

$$R_2 \; and \; R_3$$

Figure 28.10

.

Here the Miller Transformation of R_3 to the output node pair is

$$\frac{R_3 \times A_V}{(A_V - 1)}$$

Figure 28.11

This is a negative resistance but it does not have a deleterious effect on the performance of emitter follower. It is a vey large negative resistance hence it is very small negative conductance. This in parallel with R_E gives a net positive resistance only. Hence it does not make the circuit oscillatory.

By the use of Darlington Pair we can achieve super beta transistor

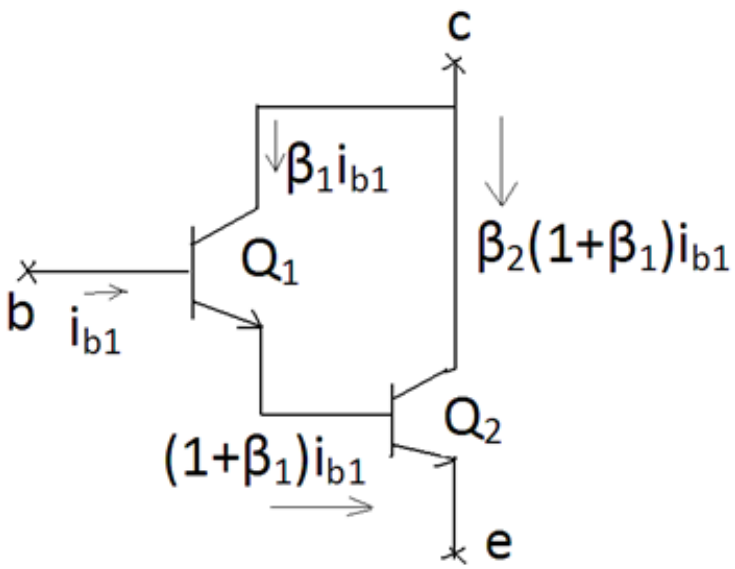


Figure 4. Two transistors connected as a Darlington Pair so as to give a overall short circuit current as te product of the individual short circuit current gains.

Figure 28.12

$$I_c^* = \beta_{F1} I_{B1} + \beta_{F2}(1 + \beta_{F1}) I_{B1}$$

Figure 28.13

$$\frac{I_c^*}{I_{B1}} = (\beta_{F1} + \beta_{F2} + \beta_{F1}\beta_{F2}) = \beta \ composite$$

Figure 28.14

Now if

$$\beta_{F2} = 100, \quad \beta_{F1} will\ be\ almost\ 10.$$

Figure 28.15

$$\therefore \beta_{composite} =$$

Figure 28.16

$Q_1 -> \beta_1 = 10 \times Q_2 -> \beta_2 = 100$

$$\equiv 1{,}000.$$

Figure 28.17

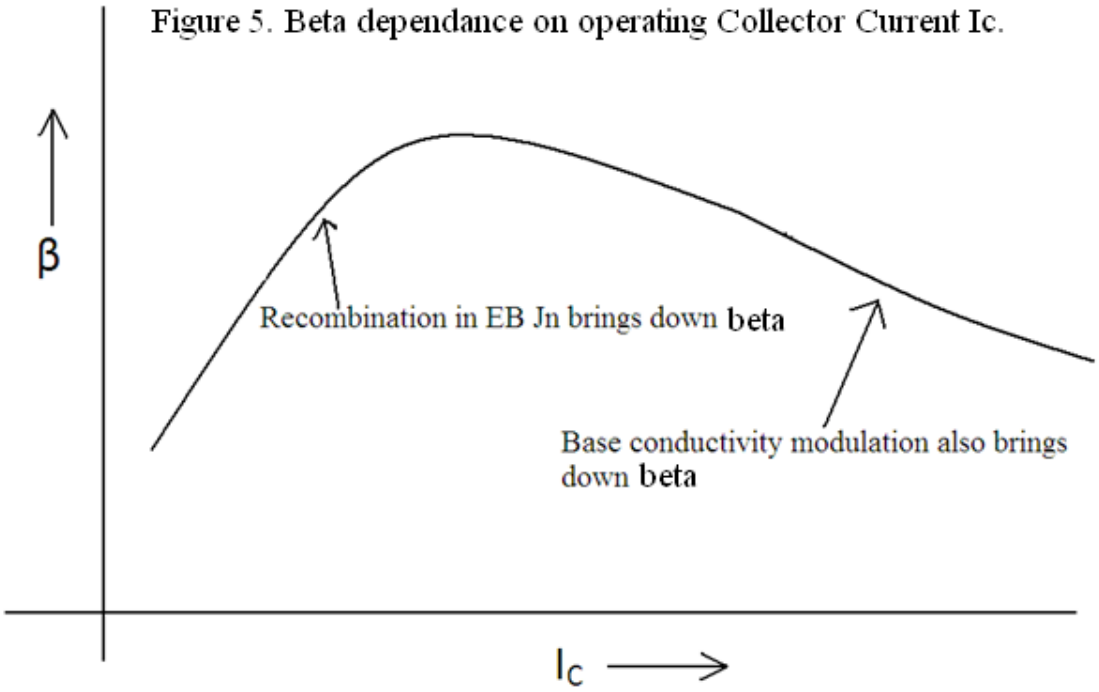


Figure 28.18

Figure 5. Beta dependence on operating current

$$I_{CQ}$$

Figure 28.19

.

As seen in the curve, Emitter Injection Efficiency (γ) deteriorates at low operating currents below 0.5mA due to recombination current within EB depletion layer.

Emitter Injection Efficiency (γ) deteriorates at high operating currents above 5mA due to base conductivity modulation.

Hence by this technique, a Darlington Pair Composite Transistor short circuit current gain can never be better than 1000.

If

Figure 28.20

=

Figure 28.21

better than 10,000 is to be realized then we will have to go for the fabrication of super beta transistor by realizing ultra thin base layer in vertical NPN transistor. By the use of Ion-Implantation as thin as 10nm base width is being realized to date.

Chapter 29

AE_Lecture6_Analysis of CASCODE AMPLIFIER.[1]

AE_LECTURE 6_Analysis of CASCODE AMPLIFIER

CASCODE AMPLIFIER- This is a form of composite transistor where CE and CB have been cascaded. By using the composite form we achieve best of both the circuit configurations namely we get a moderate input impedance and high voltage gain of CE configuration and almost near unilaterality , very large output impedance , large output voltage swing limited by BV_{CBO} and much larger Band Width of CB configuration. Because of near uni-laterality on account of near zero reverse transmission factor, this CASCODE is very suitable RF Amplifier applications. This configuration is also suitable for constant current drive as required in generating SAW TOOTH WAVEFORM.

[1] This content is available online at <http://cnx.org/content/m31596/1.1/>.

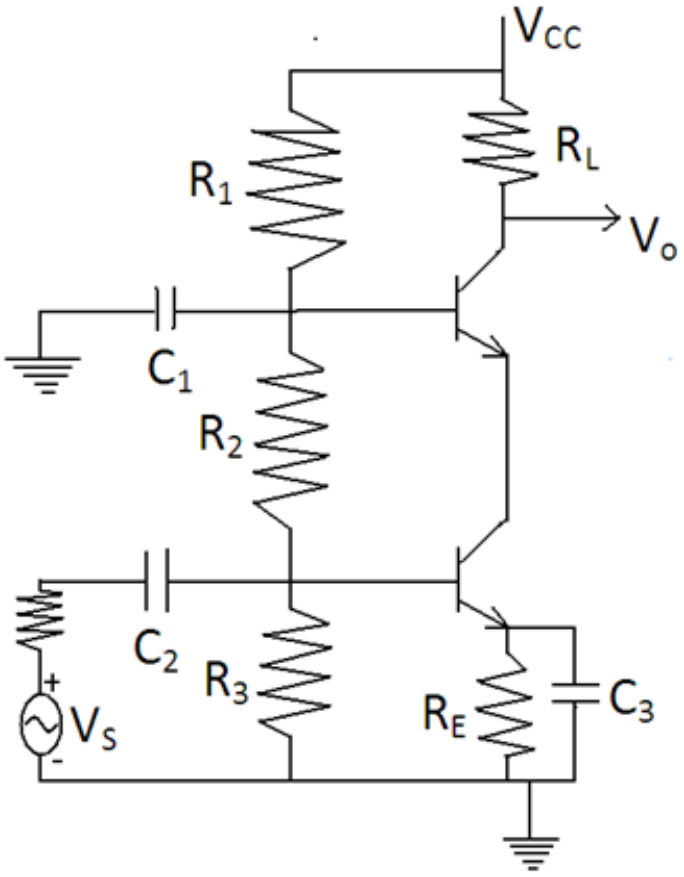


Figure 1.The Circuit Schematic of Cascode Amplifier with self-biasing.

Figure 29.1

This CASCODE configuration has a self biasing for Q point stabilization. Both Transistors are in forward active mode. Q_1 is connected in CE configuration under signal condition and Q_2 is in CB configuration under signal condition.

C_1 provides the ground to Q_2 under signal condition.

C_2 is the coupling capacitor and C_3 provides the by-pass capacitor of emitter resistance.

INCREMENTAL MODEL

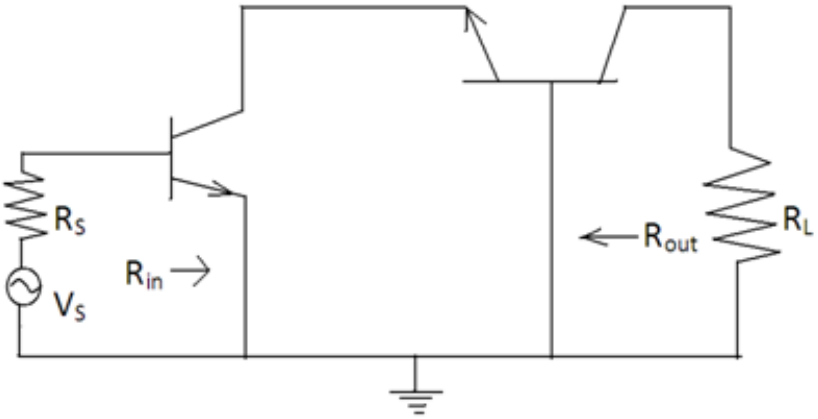


Figure 2. Midfrequency Incremental model of the Cascode Amplifier with BJT not replaced by its incremental model.

Figure 29.2

Effectively we obtain CE configuration followed by CB configuration hence we call it CE-CB cascade.
Overall Reverse transmission factor= $h_{re}.h_{rb}$
=

$$\left(\frac{r_\pi}{r_\mu}\right) \times \left(\frac{r_x}{r_c}\right)$$

Figure 29.3

$= 10^{-4} \times 10^{-5} = 10^{-9}$= this provides the near-unilaterality property to CASCODE configuration making it suitable for RF applications.

Overall $R_{out}=1/h_{ob}=2M$

Overall $R_{in}=h_{ie}=r_x+r_\pi=(100+2.6k\Omega)$

Frequency response of CB$\gg$ Frequency response of CE

CE configuration faces a load which is R_{in} of CB which is r_e . Hence Miller Muliplication factor is only 1+1 hence Miller Capacitance is much lower thereby boosting the frequency response of CASCODE configuration.

INCREMENTAL MODEL

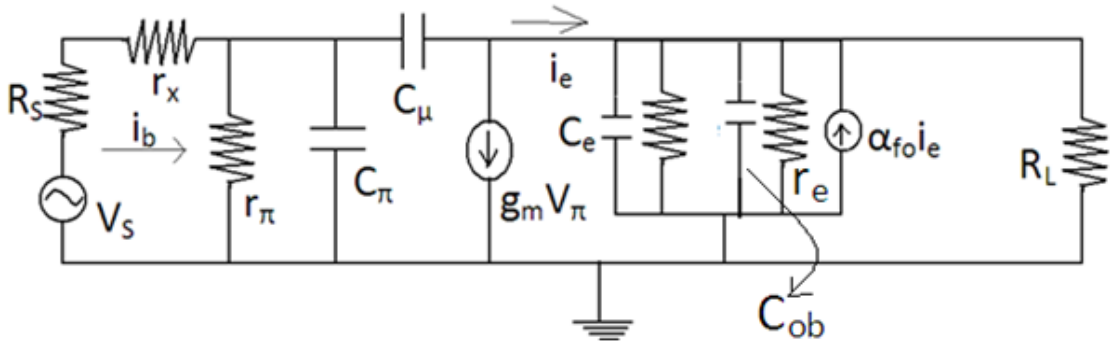


Figure 3. The incremental model of Cascode Amplifier with CE BJT being replaced by Hybrid-pi Model and CB BJT being replaced by T-Model. This is high frequency Model.

Figure 29.4

R_s=1kΩ, β_{fo}=100, r_x=0.1k, C_μ=2pF, R_L=2k, g_m=40mS, r_π=2.5k, C_π=100pF

$$g_m = \frac{I_C}{V_T} = \frac{1}{25} = 40mS; I_C = g_m V_T = 25mV \times 40mS = 1mA$$

Figure 29.5

$$r_\pi = \frac{\beta_o}{g_m} = \frac{\beta_o \times V_T}{I_C} = \frac{100 \times 25mV}{1mA} = 2.5k$$

Figure 29.6

$$r_e = \frac{V_T}{I_E} = 25\Omega; \alpha_{fo} = 0.99; \beta_{fo} = \frac{\alpha_{fo}}{1-\alpha_{fo}} = \frac{0.99}{1-0.99} = 99 \sim 100$$

Figure 29.7

$$C_\pi = 100pF = C_e; C_\mu = C_{bo} = 2pF$$

Figure 29.8

$$\omega_T = \left(\frac{g_m}{C_\pi + C_\mu}\right) = \frac{0.04}{102 \times 10^{-12}} \frac{rad}{sec} = \frac{0.04}{102} \times 10^{12} \frac{rad}{sec}$$

Figure 29.9

$$\omega_T = \frac{040000}{102} \times 10^6 \frac{rad}{sec} = 400M \frac{rad}{sec}$$

Figure 29.10

$$f_T = \frac{400}{2\pi} MHz = 63.66MHz$$

Figure 29.11

AT MID FREQUENCIES

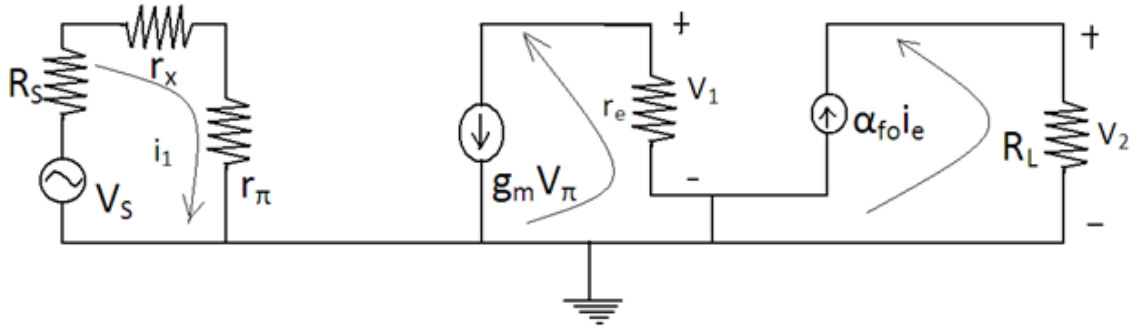


Figure 4. Midfrequency incremental model of CASCODE AMPLIFIER.

Figure 29.12

$$v_2 = -R_L(\alpha_f i_e); i_e = \frac{v_1}{r_e};$$

Figure 29.13

$$v_1 = -r_e(100 i_1)$$

Figure 29.14

$$i_1 = \frac{v_s}{R_s + r_x + r_\pi} = \frac{v_s}{1k + 0.1k + 2.5k} = \left(\frac{v_s}{3.6k}\right)$$

Figure 29.15

$$\therefore v_1 = -(100)\left(\frac{v_s}{3.6k}\right)(25\Omega)$$

Figure 29.16

$$\left(\frac{v_1}{v_s}\right) = A_{vo1} = \frac{-(100)(25)}{3600} = \frac{-2500}{3600} = -0.715$$

Figure 29.17

$$v_2 = -(\alpha_f)(R_L)\left(-\frac{v_1}{r_e}\right)$$

Figure 29.18

$$\therefore \frac{v_2}{v_1} = \frac{(\alpha_f)(R_L)}{r_e} = \frac{(0.99)(2000)}{25} = 79.2$$

Figure 29.19

$$\therefore A_{vo2} = 79.2$$

Figure 29.20

$$\therefore A_{vo} = -(0.715)(79.2) = -56.6$$

Figure 29.21

$$A_{vo} = \frac{-\beta_o R_L}{R_S + r_x + r_\pi} = \frac{-(100)R_L}{(3600)}$$

Figure 29.22

Midband gain of cascade $\sim$ a single stage CE amplifier with a load resistance of 2k.
BW calculations
The midband gain of CE stage $=-g_m r_e=-1$
Therefore Miller Capacitance$=C_\mu[1-(-1)]=2C_\mu$
Therefore total input Capacitance$=C_\pi+C_\mu\ (1-A_V)=100+8=108$pF
There is very little Miller Multiplication of C_μ.
R_{eq} of C_M (Miller Capacitance) is =

$$r_\pi \| (R_S + r_x) = (2.5k) \| (1.1k) = \frac{(2.5)(1.1)}{(2.5+1.1)} = 0.763k$$

Figure 29.23

$$\tau_{10} = C_M R_e = (108pF \times 0.763k) = 82.5ns$$

Figure 29.24

$$\therefore \omega_h = \frac{1}{82.5ns} = 0.0121 \frac{Grad}{sec}$$

Figure 29.25

$$f_h(for\ CE) = \frac{12.1}{2\pi} MHz = 1.93MHz$$

Figure 29.26

The BW of common base is much larger.

$$\omega_h(for\ CB) = \frac{1}{\tau_1 + \tau_2} = \frac{1}{C_e r_e + C_{bo} R_L}$$

Figure 29.27

$$= \frac{1}{100 \times 10^{-12} \times 25 + 4 \times 10^{-12} \times 2000}$$

Figure 29.28

$$= \frac{1}{2.5 \times 10^{-9} + 8 \times 10^{-9}}$$

Figure 29.29

$$= \frac{1}{10.5 \times 10^{-9}}$$

Figure 29.30

$$= \frac{1}{1.05 \times 10^{-8}}$$

Figure 29.31

$$= 95.2M \frac{rad}{sec}$$

Figure 29.32

$$f_h(CB) = 15MHz$$

Figure 29.33

Overall BW of Cascode=1.93Mhz

Exact analysis gives the same result.

$$A_V(s) = \frac{-k\left[s-(0.2+j0.98)\frac{Grad}{sec}\right]\left[s-(0.2-j0.98)\frac{Grad}{sec}\right]}{\left[s+0.0124\frac{Grad}{sec}\right]\left[s+0.1\frac{Grad}{sec}\right]\left[s+0.4\frac{Grad}{sec}\right]\left[s+3.26\frac{Grad}{sec}\right]}$$

Figure 29.34

Four poles because there are C_μ,C_e,C_π,C_{bo}.

There are two zeroes which are complex conjugate.

If CB stage was replaced by 2k to obtain the same gain the Miller Multiplication would have increased and BW fallen to 491 kHz.

$$\tau = (r_{\pi_1}||R_s + r_x)\left[C_\pi + C_\mu(1+g_m R_L)\right] = 324nsec$$

Figure 29.35

$$\omega_h = \frac{1}{324}\frac{Grad}{sec}$$

Figure 29.36

f_h=491kHz

(1)Large gain x BW or large GBP

(2)Output Voltage swing is limited by BV_{CBO} and not BV_{CEO}.

Applications:-

(1)Wide band video amplifier(TV & FM Radio)

(2)Wide Band Amplifier used in RF communication,

(3)Near ideal current sources and in high gain amplifiers.

(4)Current Amplification factor is increased(β_{fo} +1).

(5)Used in high performance differential amplifers which is the building block of op amps. This enables very high gain & high CMRR.

(6)We can realize near ideal current sources.

(7)Much higher B.W.

Chapter 30

AE_Lecture7_Multistage Amplifier[1]

AE_LECTURE7_ MULTISTAGE AMPLIFIERS

In real world, a variety of combination of performance specifications have to be achieved.

One such combination as required for an op-amp is:

$$R_{in} = \infty; A_{V_o} = \infty; R_{out} = 0; BW = \infty$$

Figure 30.1

This cannot be met by a single stage amplifier. By cascading several stages we achieve it .

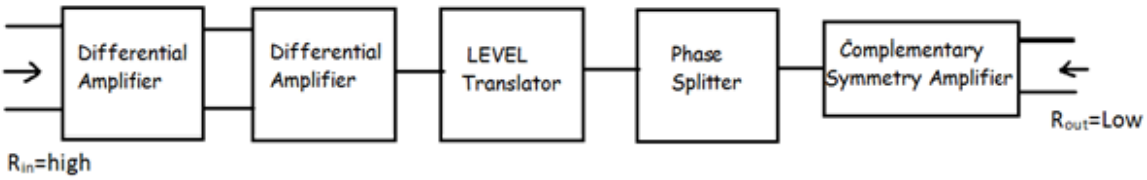


Figure 1. Block Diagram of Oprational Amplifier which is multi-stage amplifier.

Figure 30.2

Figure 1. Block Diagram of an Op Amp which is a cascaded amplifier.

While designing multi-stage amplifier, if we have capacitance coupling then it becomes easier to design since there is no DC interaction.

But in a directly coupled multistage amplifier since we have DC interaction hence it is difficult to design.

[1]This content is available online at <http://cnx.org/content/m31668/1.1/>.

A direct coupled amplifier implies DC Amplifier whereas a capacitive coupled amplifier implies AC Amplifier as RC-coupled Amplifier is.

COMMONLY USED CASCADED AMPLIFIER

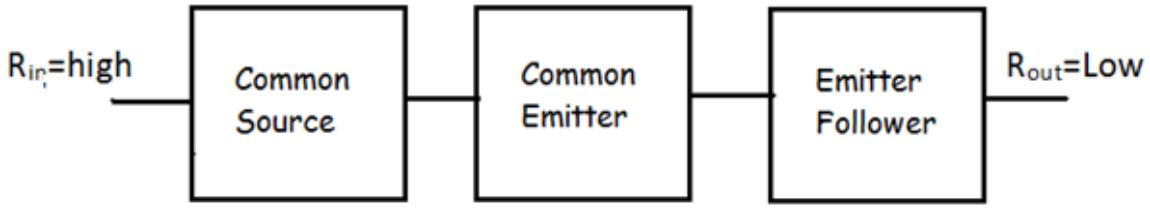


Figure 2. A multistage amplifier used in Instrumentation Application.

Figure 30.3

Figure 3. The Block Diagram of commonly used Cascaded Amplifier.

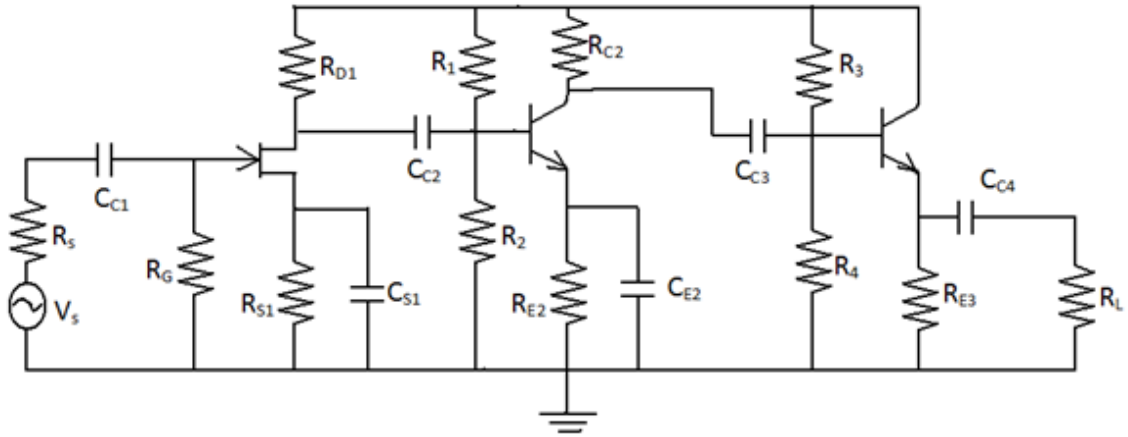


Figure 3. Circuit Diagram of Instrumentation Amplifier.

Figure 30.4

v

Figure 3. Actual implementation of Instrumentation Amplifier using a cascade of CS-CE-CC.

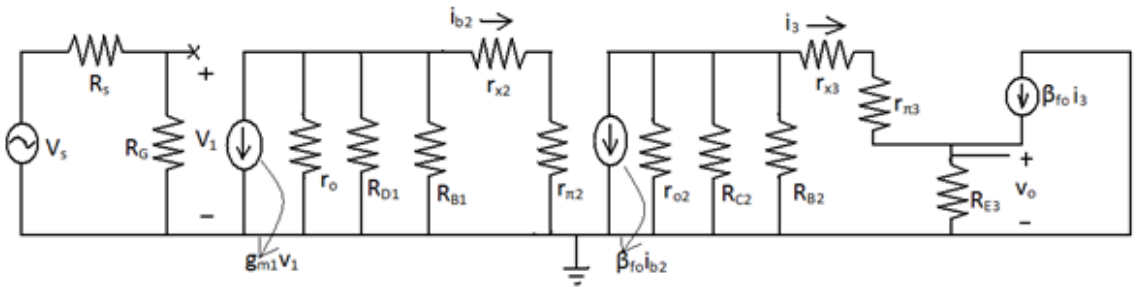


Figure 4. Mid-frequency incremental model of the cascaded amplifier shown in Figure 3.

Figure 30.5

Figure 4. EQUIVALENT CIRCUIT of the above cascade at MID FREQUENCY.

In Multi-stage amplifiers we have the problem of BAND WIDTH SHRINKAGE.

In Figure 5, the Bode Plot of single stage amplifier is shown. As can be seen the frequency response is that of Band-Pass filter with lower -3dB frequency being f_L and upper -3dB being f_H . The skirt of the response is -20dB/decade at the higher end and +20dB/decade at lower end. The mid-band gain or flat band-gain is 20dB.

If two such identical Amplifiers are cascaded in a non-interacting fashion then overall gain will be +40dB but the BW will shrink as shown in Figure 6. The skirts are steeper: 40dB/decade at lower end and -4-dB/decade at higher end. The upper cut-off frequency now is

$f_H = f_H' \times Sn$ where Sn=shrinkage factor and $f_L = f_L'/Sn$ as shown in Figure 6.

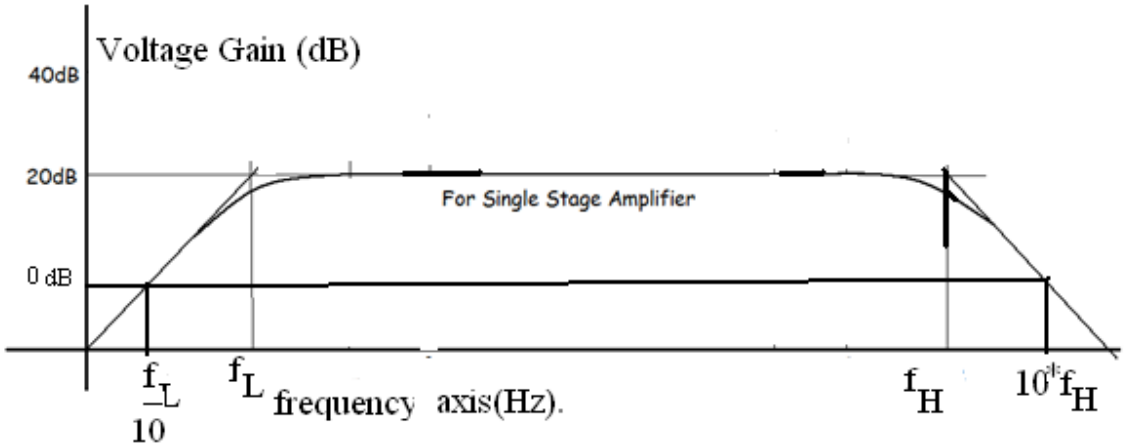


Fig. 5 . Frequency Response of a single stage amplifier with a skirt of +20dB/decade below lower -3dB freq. and -20dB/decade above upper -3dB frequency.

Figure 30.6

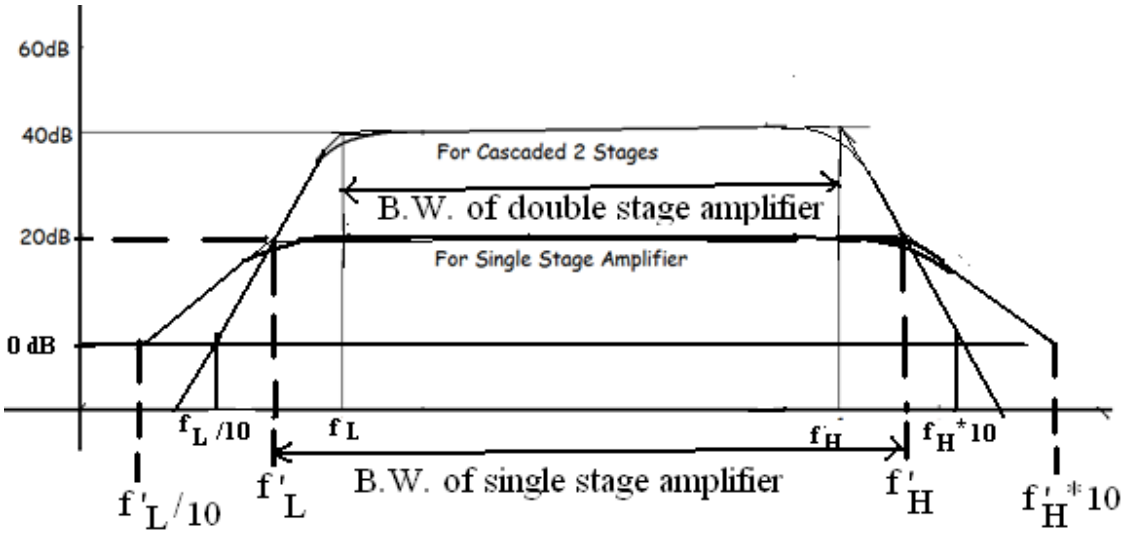


Fig. 6 . Gain Magnitude-Frequency Response of a single stage and double stage amplifier

Figure 30.7

From Figure 6 it is clear that single stage amplifier has a mid-band gain of 20dB and -3dB BW of $[f'_H - f'_L]$ whereas a double stage amplifier has a mid-band gain of 40 dB and -3dB BW is $[f_H\text{-}f_L]$ where $[f_H\text{-}f_L] = f'_H \times S_2 - f'_L / S_2$ and $S_2 = \sqrt{(2^{1/2}\text{-}1)} = 0.64$= shrinkage factor of a double stage amplifier.

$$Band\ Width\ Shrinkage\ Factor = S_n = \sqrt{2^{1/n} - 1}$$

Figure 30.8

For n stage cascade of identical amplifiers

$$(f_L)_{overall} = \frac{f_L}{\sqrt{2^{1/n} - 1}}$$

Figure 30.9

$$(f_H)_{overall} = f_H\sqrt{2^{1/n} - 1}$$

Figure 30.10

Where f_L = lower -3dB frequency of single stage and f_H = Upper -3dB frequency of single stage amplifier.

n	1	2	3	4	5
$\sqrt{2^{1/n} - 1}$	1	0.64	0.51	0.44	0.34

Table 30.1

This formula is applicable only if there are identical stages which we cascade in a non interacting manner.

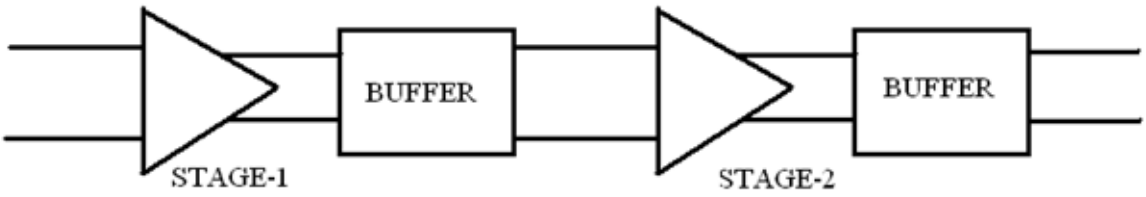


FIGURE 7 Identical Stages Cascade in an non-interacting manner. The non-interacting cascade is achieved by using buffers. In this particular case the shrinkage factor is applicable.

Figure 30.11

If these identical stages are cascaded without buffer then they will interact among themselves and even if they are identical their individual upper -3dB frequencies and lower -3dB frequencies will get dispersed and there are non-identical upper -3dB frequencies

$$\omega_{h_1}, \omega_{h_2}, \omega_{h_3}, - - - - - - - , \omega_{h_n}$$

Figure 30.12

.
Then the overall upper -3dB frequency

$$\omega_h{}^o$$

Figure 30.13

,

$$\frac{1}{\omega_h{}^o} = \sqrt{\frac{1}{(\omega_{h_1})^2} + \frac{1}{(\omega_{h_2})^2} + \frac{1}{(\omega_{h_3})^2} + - - - - - - - + \frac{1}{(\omega_{h_n})^2}}$$

Figure 30.14

This equation implies that in time domain the overall rise time

$$t_r^o = \sqrt{(t_{r1})^2 + (t_{r2})^2 + (t_{r3})^2 + - - - - - - - + (t_{rn})^2}$$

Figure 30.15

In case of lower -3dB frequencies, the individual lower -3dB frequencies are

$$\omega_{l_1}, \omega_{l_2}, \omega_{l_3}, - - - - - - - , \omega_{l_n}$$

Figure 30.16

and in that case the overall -3dB frequency is given by the following formula:

$$\omega_l{}^{o} = \sqrt{(\omega_{l_1})^2 + (\omega_{l_2})^2 + (\omega_{l_3})^2 + - - - - - - - - - +(\omega_{l_n})^2}$$

Figure 30.17

This formula implies that overall sag=

$$\sum individual\ sags.$$

Figure 30.18

Therefore for obtaining 10% sag we will have to increase the frequency

$$f^*$$

Figure 30.19

Hence

$$f_L = \frac{0.1\, f^*}{\pi}$$

Figure 30.20

will also increase.

In identical stages with non-interacting cascade shrinkage factor will decide the band-width whereas in interacting cascade the above equations will decide the band-width.

Chapter 31

AE_Lecture8_MOSFET & JFET_PartA[1]

AE_Lecture8_PartA Static characteristics of FIELD EFFECT TRANSISTORS

A Field Effect Transistor is like a pentode. It is an analogue of pentode. Both are Voltage Controlled Current Sources.

FET is of two types JFET and MOSFET.

JFET is n channel FET known as nJFET and p channel FET known as pJFET.

Similarly MOS is n channel NMOS and p channel PMOS.

MOS can be enhancement mode which is normally-off or depletion mode normally-on device.

So NMOS can be (E)NMOS and (D)NMOS.

PMOS can be (E)PMOS and (D)PMOS.

The following is the circuit diagram of an Amplifier using N-channel JFET:

[1]This content is available online at <http://cnx.org/content/m31717/1.3/>.

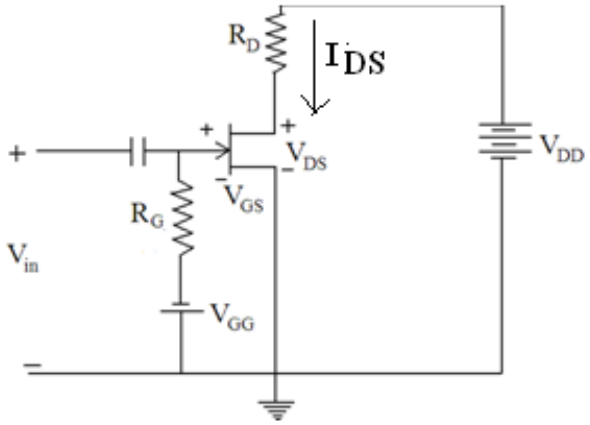


Figure 1. Circuit Set-up for measuring the Static Charactristics of nJFET.

Figure 31.1

Measurement of characteristics of N-channel JFET

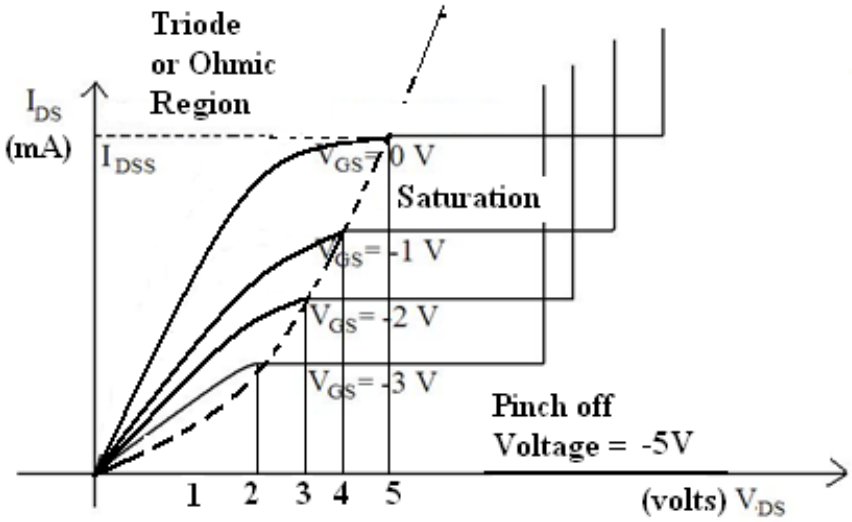


Figure 2. Static Output Characteristics of nJFET.

Figure 31.2

Figure 2 gives the dc output characteristics nJFET. Note that Gate Voltage is always kept negative so that the gate current is always zero. We indicate the Gate-Drain breakdown also. As gate voltage becomes more negative , Avalanche Breakdown of Gate to Drain Junction takes place earlier.When ($V_{DS} - V_{GS}$) exceeds V_P (Vpinchoff), the channel gets pinched off towards the Drain End and current becomes constant. This is saturation region. The dotted parabola seperates the Ohmic region or Triode Region from Saturation Region or Pentode Region. Here the pinch off voltage is -5V.

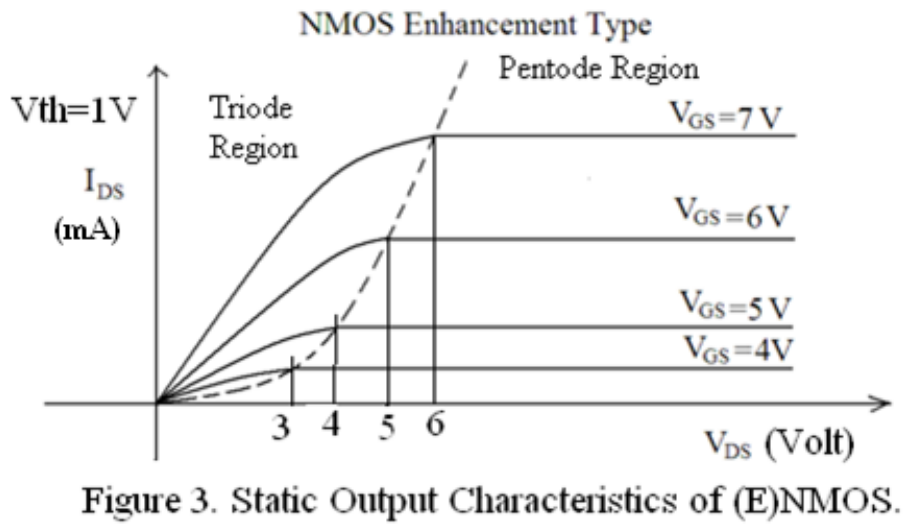


Figure 3. Static Output Characteristics of (E)NMOS.

Figure 31.3

Figure 3 gives the output characteristics of (E)NMOS with a Threshold Voltage of 1V. Therefore when V_{DS} increases and becomes equal to (V_{GS} - V_{Th}) the channel pinches off near the drain end and current saturates.. As V_{DS} assumes larger values the pinched off region becomes wider, (V_{GS} - V_{Th}) drops across the channel and excess part of V_{DS} drops across the pinched off region. Since there is a constant voltage dropping across the channel and since the channel is of constant length hence I_{DS} is constant. But in real life there is a shortening of channel length leading to a slope of the saturated current. This channel length modulation is responsible for a finite output impedance r_{ds} of the voltage controlled current source modeling (E)NMOS under incremental condition.

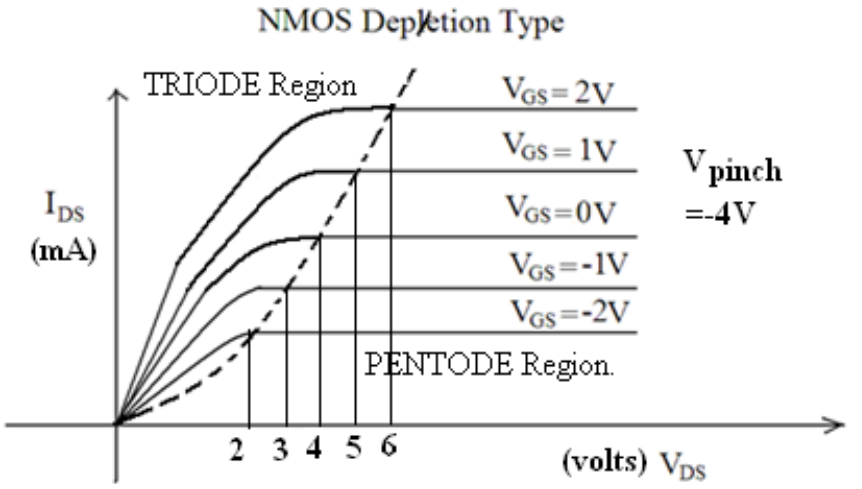


Figure 4.Static Output Characteristics of (D)NMOS.

Figure 31.4

In Figure 4 we give the output characteristics of (D)NMOS. Depletion type device is normally-on device hence it gives a characteristic for positive gate voltage, zero gate voltage and negative voltage. In (D)NMOS when gate voltage becomes equal to Pinch-off voltage then (D)NMOS turns off. Here pinch off voltage is -4V.

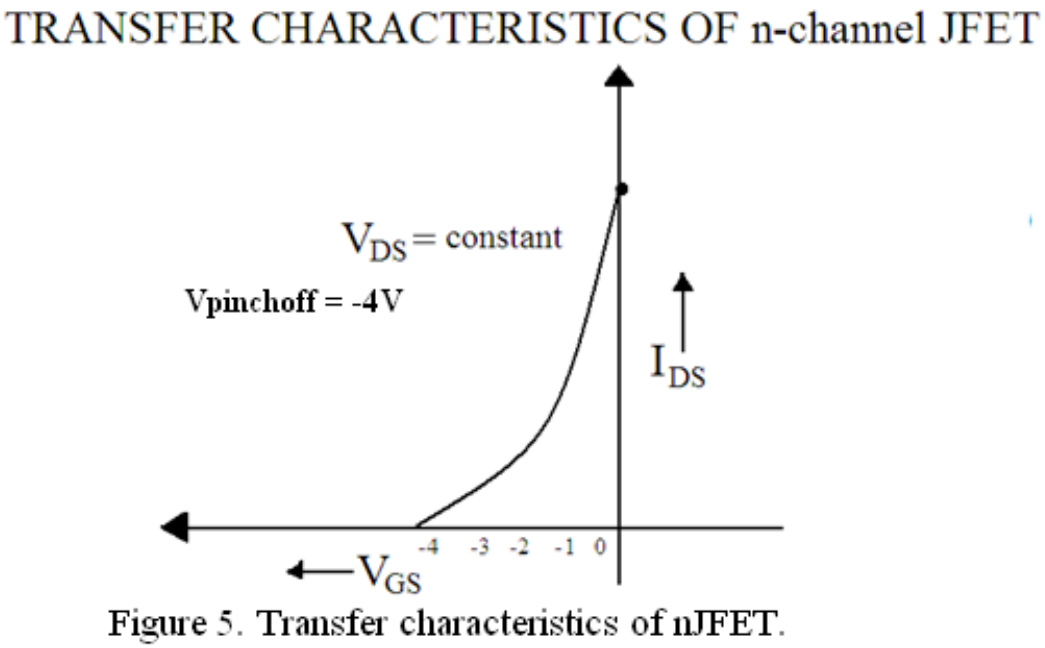

TRANSFER CHARACTERISTICS OF n-channel JFET
V_{DS} = constant
Vpinchoff = -4V
I_{DS}
-4 -3 -2 -1 0
V_{GS}
Figure 5. Transfer characteristics of nJFET.

Figure 31.5

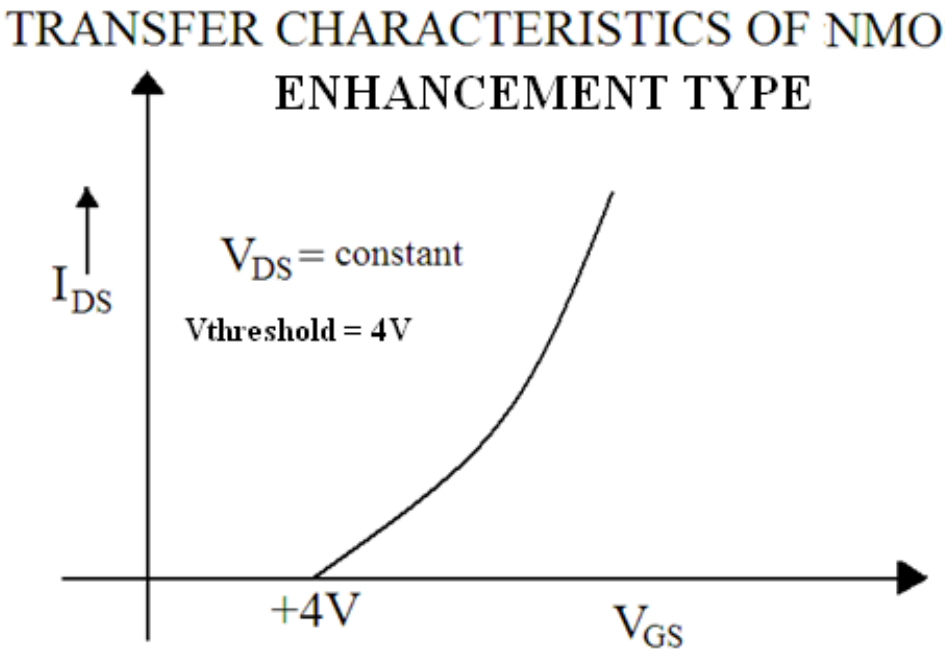


Figure 6. Transfer characteristics of (E)NMOS which is normally off device.

Figure 31.6

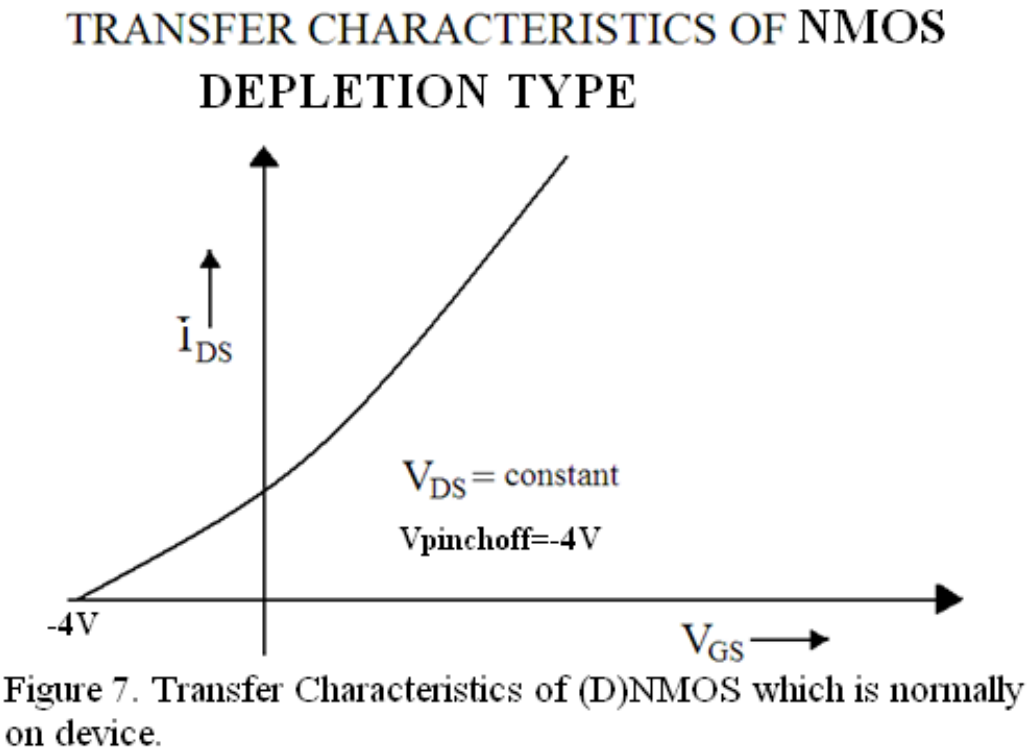


Figure 7. Transfer Characteristics of (D)NMOS which is normally on device.

Figure 31.7

Comparing the transfer characteristics of nJFET, (E)NMOS and (D)NMOS as given in Figure 5, 6 and 7 we can say that (D)NMOS is most flexible device from design point of view as it accepts both positive and negative voltages as the gate voltage.

NMOS Transistor (Pentode and Triode Region)

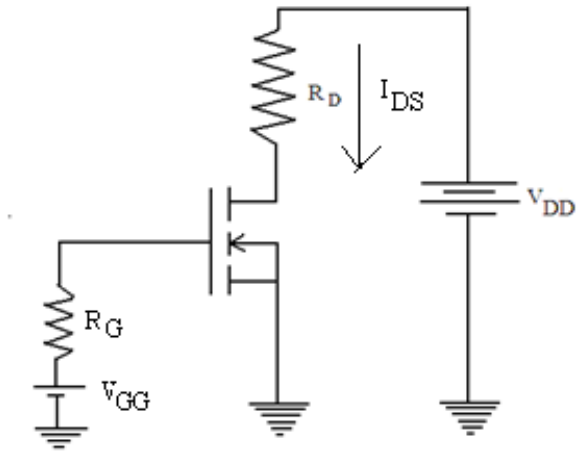


Figure 8. Circuit Set-up to study the Triode and Pentode Region of (E)NMOS.

Figure 31.8

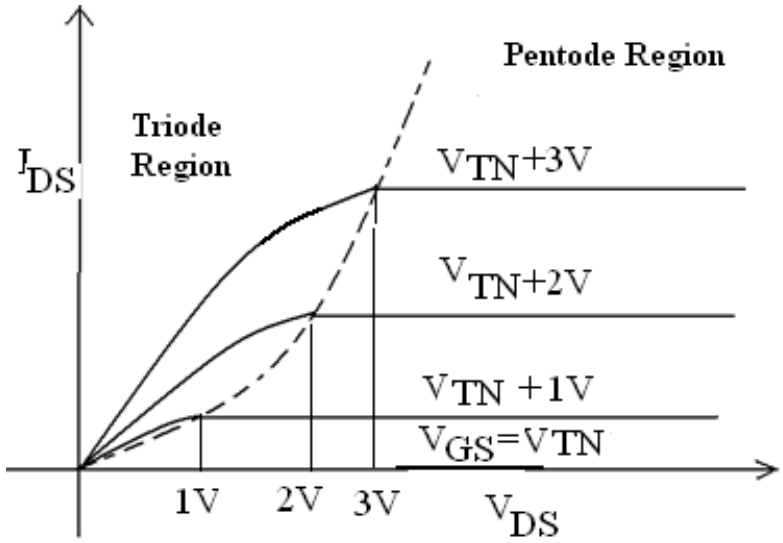


Figure 9. Output Characteristics of (E)NMOS demarcating the TRIODE and PENTODE region.

Figure 31.9

TRIODE REGION:

$$i_D = K_n\left(v_{GS} - V_{TN} - \frac{(v_{DS})}{2}\right)(v_{DS})$$

Figure 31.10

_____(1)
K_n=K_n'multiplied_by

$$\left(\frac{W}{L}\right)$$

Figure 31.11

K_n'= $\mu_n C_{ox}$" .....Kn' ia a transconductance parameter which is fixed for a given technology and cannot be changed by the circuit designer. Whereas Kn = Kn'×(W/L) = this is also a transconductance

parameter but it includes the aspect ration (W/L) of the given MOSFET. The aspect ratio gives the geometry of the device and this is under control of a circuit designer . This second transconductance parameter can be controlled when he is generating the masks for a given circuit or system during ASIC(Application Specefic IC) or SOC(System –on- Chip) design. W is the width of the gate and L is the length of the gate or the length of the channel.

$$\mathrm{Cox}'' = \frac{\epsilon_{ox}}{T_{ox}}\left(\frac{F}{cm^2}\right)$$

Figure 31.12

$$\epsilon_{ox} = oxide\ permittivity\left(\frac{F}{cm}\right) = 3.9 \times 8.854 \times 10^{-14}\frac{F}{cm}$$

Figure 31.13

$$T_{ox} = oxide\ thickness$$

Figure 31.14

Triode Region exists as long as

$$(V_{GS} - V_{DS}) \geq V_{TN}$$

Figure 31.15

.
Channel should not pinch off on the drain side.
PENTODE REGION
At

$$V_{DS}^{*} = V_{GS} - V_{TN}$$

Figure 31.16

_ _ _ _ _ _ _ _ _ _ _ (2)
channel pinches off at drain end. From here onwards current becomes constant or current saturates. Substituting (2) in (1),

---

$$I_D = K_n \left(V_{GS} - V_{TN} - \frac{(V_{GS} - V_{TN})}{2} \right) (V_{GS} - V_{TN})$$

Figure 31.17

$$I_D = K_n \frac{(V_{GS} - V_{TN})^2}{2}$$

Figure 31.18

$$I_D = K_n^{\square} \frac{W}{L} \frac{(V_{GS} - V_{TN})^2}{2}$$

Figure 31.19

$$\therefore I_D = K_n^{\square} \frac{W}{L} (V_{GS} - V_{TN})^2$$

Figure 31.20

$$I_D = \mu_n C_{ox}'' \frac{W}{L} (V_{GS} - V_{TN})^2$$

Figure 31.21

Quadratic Law

$$I_D = \left[C_{ox}'' W \frac{(V_{GS} - V_{TN})}{2} \right] \left[\mu_n \frac{(V_{GS} - V_{TN})}{L} \right]$$

Figure 31.22

Where:

$C_{ox}'' W \frac{(V_{GS} - V_{TN})}{2}$ *is the average electron charge per unit length in the inversion layer*

Figure 31.23

And $\mu_n \frac{(V_{GS} - V_{TN})}{L}$ *is the drift velocity in the channel*

Figure 31.24

Pinch Off locus is parabolic

$$\because I_D = \frac{K_n (V_{DS}^*)^2}{2}$$

Figure 31.25

For any V_{GS} , at $V^*_{DS} = V_{GS} - V_{TN}$ the saturation sets in as the channel gets pinched off at that point. Beyond that point: $V_{DS} = V^*_{DS} + \Delta V$ and V^*_{DS} drops across the channel and ΔV drops across the depleted region towards the drain end as shown in Figure 11. Since the voltage across the channel is constant at V^*_{DS} and since the channel is approximately constant (it shortens slightly as Drain to Source Voltage increases) for practical purposes we assume that the drain current is constant and hence it has saturated. But in practice due to channel length shortening, there is slight increase in drain current with drain to source voltage. Hence output characteristics does have a slope. At higher currents the slope is higher.

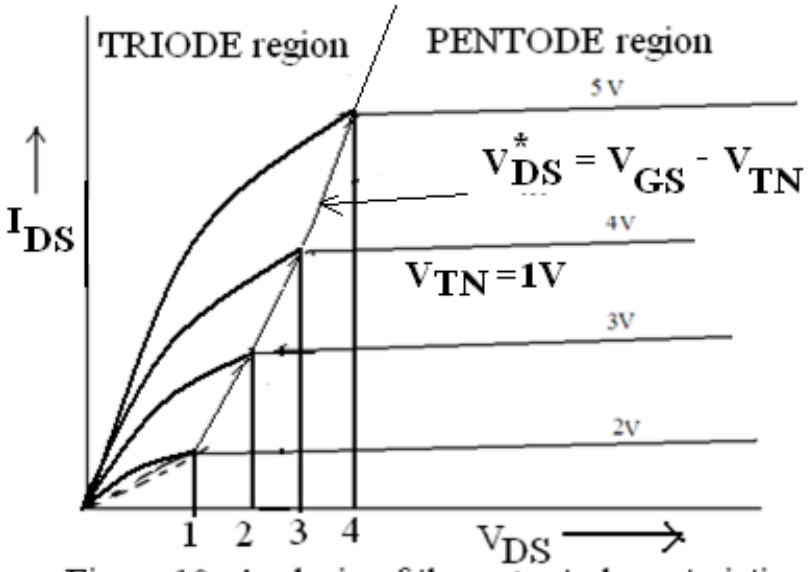


Figure 10. Analysis of the output characteristics of (E)NMOS for demarcating the TRIODE and PENTODE regions.

Figure 31.26

V_{TN}=1V
K_n=25 μA/V^2

$$i_D = K_n \frac{(V_{GS} - V_{TN})^2}{2}$$

Figure 31.27

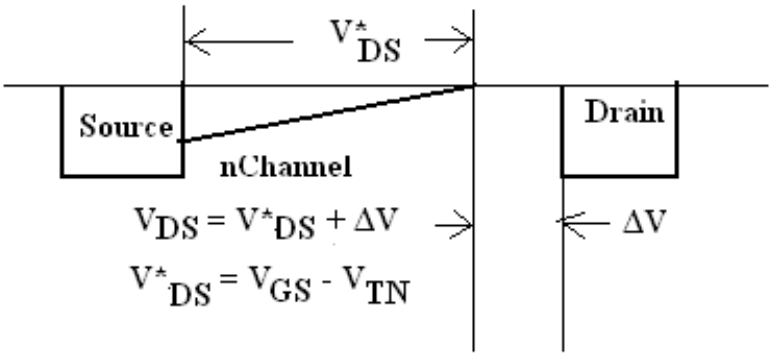


Figure 11. Physical mechanism of current saturation after the channel gets pinched off at drain end. Drain Current continues to flow evn though the channel is interrupted. At the drain end the electron manages to hop across the depletion region by Ballistic Mechanism.

Figure 31.28

N channel JET has identical formulation except threshold voltage is replaced by pinch off voltage.

Chapter 32

AE Lecture 8_Part A_MOSFET & JFET continued[1]

AE_Lecture 8_MOSFET & JFET_Part A continued.

In Part A of Lecture 8 we have seen the quantitative formulation of Enhancement and Depletion type MOSFET in Triode as well as in Pentode region. In this lecture, the continuation of Lecture 8_Part A, we will study the quantitative formulation of nJFET in ohmic and saturation region also known as triode and pentode region respectively.

Enhancement Type MOSFET was termed as Normally-Off device since with Gate-Voltage zero we have no current.

Similarly Depletion Type MOSFET is termed as Normally-On device since here even under Gate Voltage zero we do have a drain current because in NMOS(D), n-channel has been ion-implanted at fabrication stage hence it conducts at zero Gate Voltage.

In exactly the same fashion, JFET has a conducting channel at Gate Voltage zero. Hence it conducts under zero Gate Voltage therefore it is called Normally – On device. It is a depletion-mode device.

The physical structure of nJFET in a simplified manner is given in Figure 1.

[1] This content is available online at <http://cnx.org/content/m35758/1.1/>.

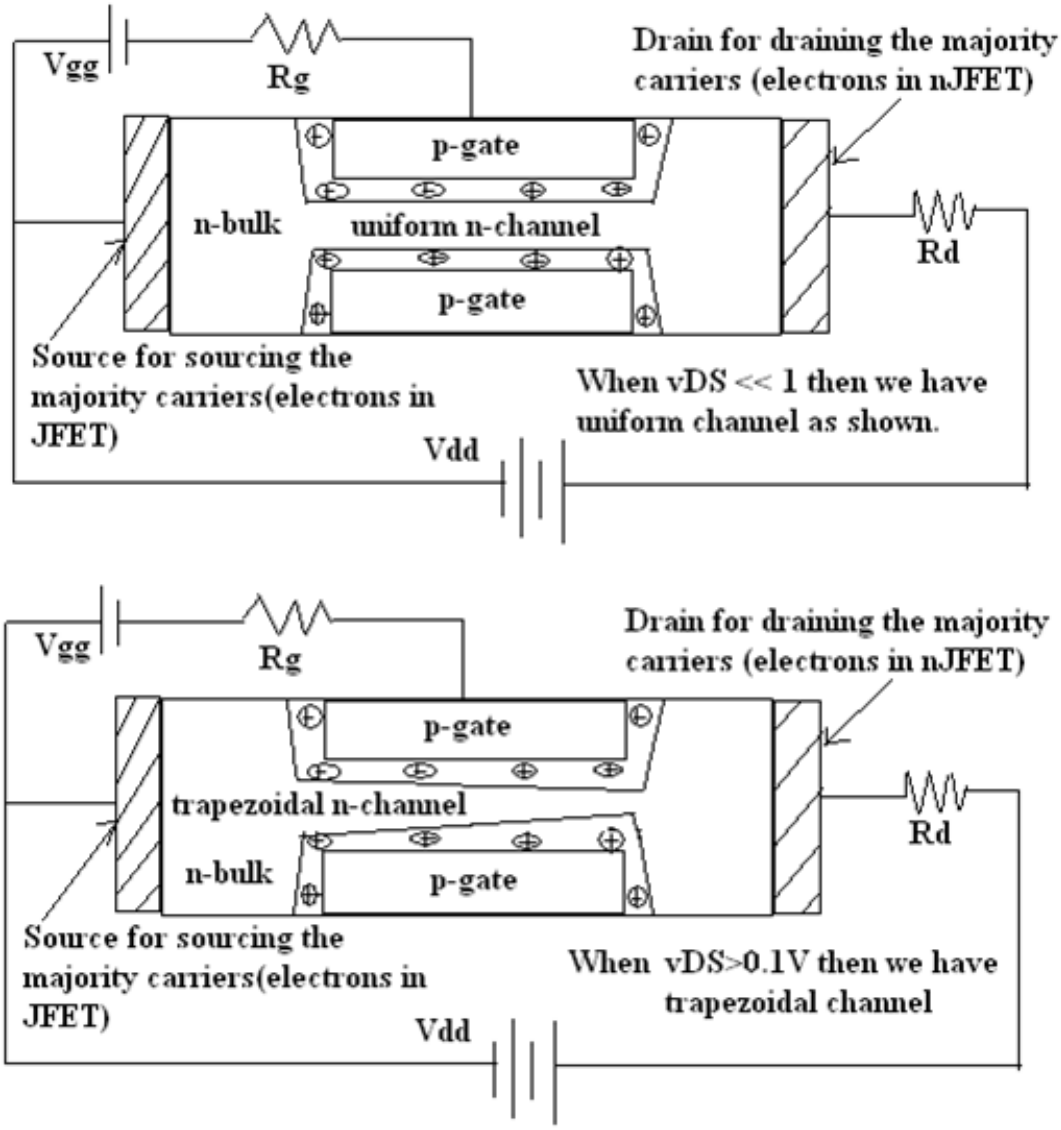


Figure 32.1

Figure 1. Physical structure of nJFET is given for negligible Drain-to-Source biasing and significant Drain-to-Source biasing respectively.

For negligible Drain-to-Source biasing, we have uniform n-channel as shown in the upper diagram. In this biasing condition, nJFET is operating in ohmic region or in Triode region.

For $V_{DS} > 0.1$ V, we have trapezoidal n-channelas shown in the lower diagram. The device is still in Triode region but its ohmic behavior is non-linear.

When $V_{DS} = (V_{GS} - V_P)$ then the n-channel gets pinched off near the Drain and current saturates at that point. Now the device has entered saturation region. For $V_{DS} > (V_{GS} - V_P)$, the current remains

constant and device is said to be in Pentode region.

In Ohmic Region:

$i_D = K_n [2(v_{GS} - V_P) v_{DS} - v_{DS}^2]$ for $0 < v_{DS} \leq ((v_{GS} - V_P)$……1

For small values of v_{DS} ,

$i_D = K_n [2(v_{GS} - V_P) v_{DS}]$……2

At $v_{DS}^* = (V_{GS} - V_P)$, device enters the saturation region since channel is pinched off near the drain.

In saturation region, irrespective of v_{DS} current becomes constant at the value decided by $v_{DS}^* = (V_{GS} - V_P)$. Substituting $v_{DS}^* = (V_{GS} - V_P)$ in Equation 1, we get:

$I_D = K_n (V_{GS} - V_P)^2$ for $v_{DS} \geq v_{DS}^*$ ……3

At $V_{GS} = 0$, we have $I_D = K_n (-V_P)^2$ = this denoted by I_{DSS} ;

Hence

$$K_n = \frac{I_{DSS}}{V_P^2}$$

Figure 32.2

……4

Typical values of Pinch-off voltage $V_P = 0$ to -25V and typical values of I_{DSS} is from 10μA to 10A.

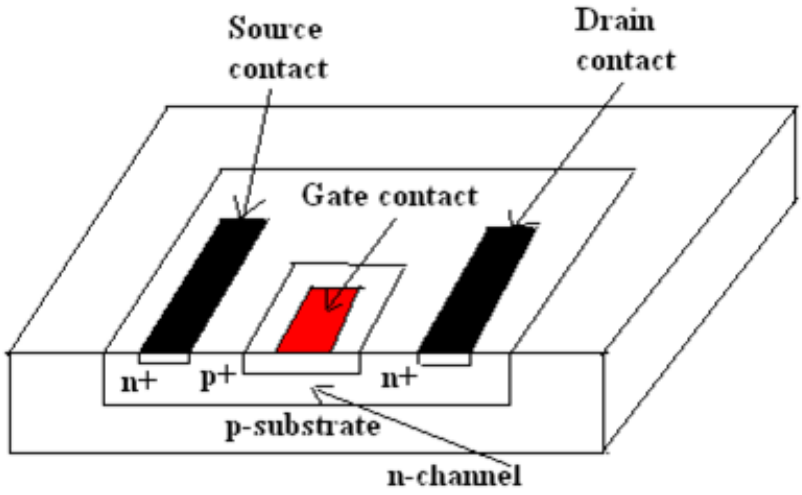
For a given value of I_D , Equation 3 gives two values of V_{GS} . Only one value is physically tenable. It must lie in the range:

……$V_P < V_{GS} < 0$

The line of demarcation or the pinch-off locus is a parabola. By substituting

$v_{DS}^* = (V_{GS} - V_P)$ in Equation 3 we get:

$I_D = K_n (V_{GS} - V_P)^2 = I_D = K_n (V_{DS}^*)^2$ which is a parabola and is defined as pinch off parabola.



Planar IC n-channel JFET structure.

Figure 32.3

Figure 2. IC version of JFET.

Chapter 33

AE_Lecture8_PartB_Incremental Model of FET[1]

AE_Lecture8_Incremental Model of FET.

FET behaves as Voltage Controlled Current Source. Hence its model is as given in Figure 1.

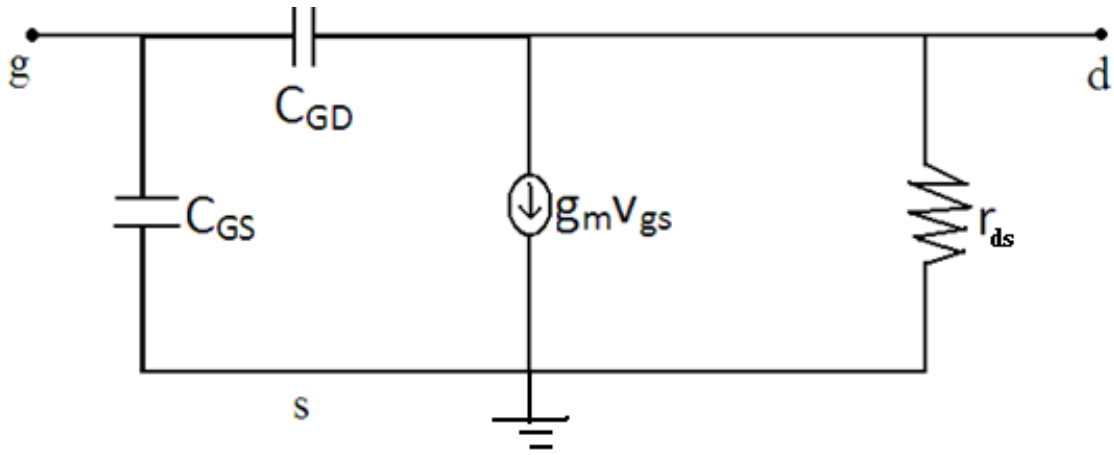


Figure 1. The incremental model of MOSFET.

Figure 33.1

At low frequencies Capacitances can be considered to be open circuit. And the Incremental Model at low Frequencies will have infinite impedance as shown in Figure 2.

[1]This content is available online at <http://cnx.org/content/m31726/1.1/>.

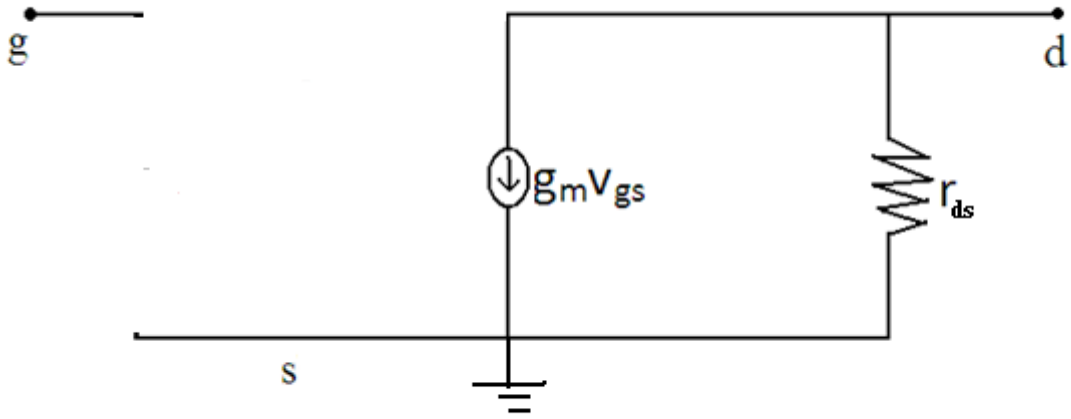


Figure 2. Low Frequency Incremental Model of MOSFET.

Figure 33.2

At low frequencies, input current is zero and short circuit current gain is INFINITY. But at high frequencies gate to source Capacitance due to overlap Capacitance (overlap between source and gate) and Gate Oxide Capacitance and gate to drain Capacitance again due to overlap Capacitance (overlap between drain and gate) and Gate Oxide Capacitance draw considerable currents. Hence Short Circuit Current Gain is finite and falls at the rate of 20dB/decade.

In the low frequency model, we have transconductance (g_m) and output impedance of the current source (r_{ds}).

Derivation of Transconductance.

$$\frac{di_D}{dV_{GS}}$$

Figure 33.3

=

$$\frac{(K_n)(2)}{2}(V_{GS} - V_{TN})$$

Figure 33.4

_ _ _ _ _(1)

$$g_m = (K_n)(V_{GS} - V_{TN})$$

Figure 33.5

$$But\ V_{GS} - V_{TN} = \left(\frac{2I_D}{K_n}\right) \times \frac{1}{(V_{GS} - V_{TN})}$$

Figure 33.6

$$\therefore g_m = \frac{(K_n)(2I_D)}{K_n(V_{GS} - V_{TN})}$$

Figure 33.7

$$g_m = \frac{(2I_D)}{(V_{GS} - V_{TN})}$$

Figure 33.8

1.

Due to channel length modulation the family of curves are not horizontal but have a finite slope.as shown in Figure 3. To account for this ,channel-length modulation parameter λ is introduced.

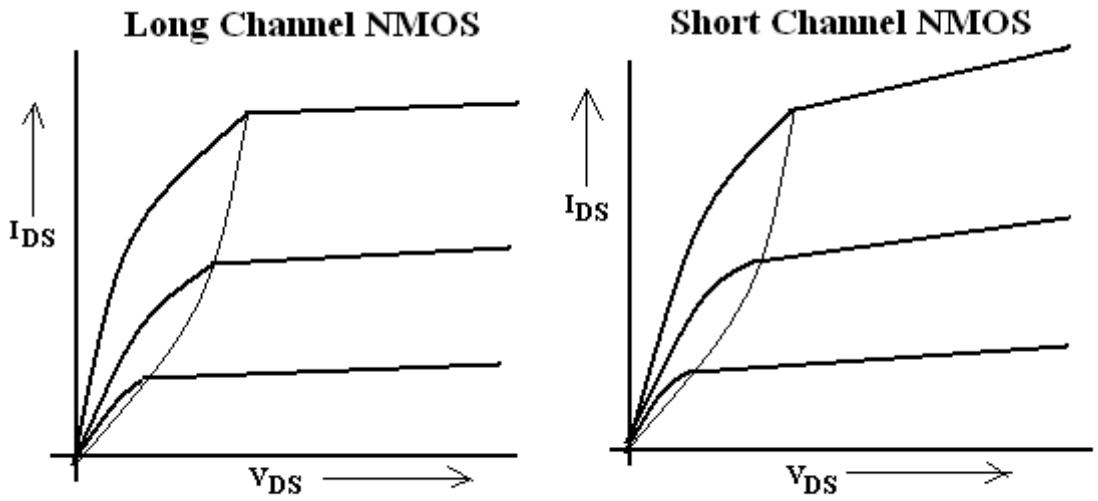


Figure 3. Effect of Channel Length Modulation on the SLOPE.

Figure 33.9

In long channel NMOS(with channel length of 10μm) of bygone MSI(Medium Scale Integration) and LSI(Large Scale Integration) era, the slope was minimal. But as packing density increased to 40 million transistors, lateral scaling reduced the channel length to 100nm. In short channel NMOS channel length modulation is very pronounced as seen in Figure 3.

$$\therefore I_D = \frac{K_n}{2}(V_{GS} - V_{TN})^2(1 + \lambda V_{DS})$$

Figure 33.10

$$0.001V^{-1} \leq \lambda \leq 0.1V^{-1}$$

Figure 33.11

$$\left[\frac{\partial i_D}{\partial v_{ds}}\right] at\ constant\ V_{GS} = \frac{K_n}{2}(V_{GS} - V_{TN})^2(0 + \lambda)$$

Figure 33.12

=

$$\lambda \frac{K_n}{2}(V_{GS} - V_{TN})^2$$

Figure 33.13

We know that

$$\frac{K_n}{2}(V_{GS} - V_{TN})^2 = \frac{I_D}{1+\lambda V_{DS}}$$

Figure 33.14

$$\therefore \frac{1}{r_{ds}} = \frac{\lambda I_D}{1+\lambda V_{DS}}$$

Figure 33.15

=

$$\frac{I_D}{\left(\frac{1}{\lambda}+V_{DS}\right)}$$

Figure 33.16

2.

Amlification Factor=μ= $g_m \times r_0$ = the maximum gain which can be achieved from a Common Source or Common Emitter Amplifier.

Combining Eq 1 and Eq 2 we get the following:
Amplification Factor of CS MOS Amplifier=[

$$\frac{\frac{1}{\lambda}+V_{DS}}{I_{DS}}$$

Figure 33.17

]
Amplification Factor of CE BJT Amplifier=[

$$\frac{V_A+V_{CE}}{V_T}]$$

Figure 33.18

V_A is the Early Voltage which was discussed in Lecture 3 in connection with the Static Output characteristics of CE BJT.

As seen above the amplification factor of CE BJT is independent of Quiescent Collector Current. From the Table we see that it is only 3400. But my research on CE BJT is showing that a much larger gain can be realized.

In the following Table we make a comparative study of BJT and FET.

FET	BJT
Geometry dependent parameters $\left(\frac{W}{L}\right)$	Geometry independent parameters
μ(amplification factor varies inversely with I_D)	μ(amplification factor is independent of I_D)
V_{DS}=10V,K_n=1 $\frac{mA}{V^2}$,λ=0.0133 V^{-1}	β_o =100,V_A=75V,V_{CE}=10V
gm=$\sqrt{2K_nI_D}$	gm=$\left(\frac{I_C}{V_T}\right)$

continued on next page

Small signal approximation holds good for values: $v_{gs} \ll 2(\mid V_{GS} \mid - \mid V_{TN} \mid)^2$ $v_{gs} \sim 0.2(V_{GS} - V_{TN})^2$ $v_{gs} \sim 400mV$	Small signal approximation holds good for values: $v_{be} \ll V_T(26mV)$ $v_{be} \sim 0.2V_T$ $v_{be} < 5mV$
Much higher packing density because no isolation diffusion required.	Here isolation diffusion is required hence historically it is one generation behind as far as packing density is concerned
This is slower. The best clocking speed is 3GHz	BJT is historically much faster . The state of art in BJT is achieving 300GHz transit frequency.
Noise Figure is much better. This has no SHOT noise , no PARTITION noise. It has flicker noise. For Low Noise Amplifier cryogenically cooled MESFET.	Noise Figure is poorer because of SHOT noise, PARTITION noise and THERMAL noise.

Table 33.1

I_D (μA)	g_m ($\times 10^{-3}$ S)	r_{ds} (MΩ)	μ	I_C (μA)	g_m ($\times 10^{-3}$ S)	r_π (kΩ)	r_0 (MΩ)	μ
1	0.0476	85.2	4060	1	0.04	2500	85	3400
10	0.151	8.52	1280	10	0.4	250	8.5	3400
100	0.476	0.852	406	100	4	25	0.85	3400
1000	1.51	0.085	128	1000	40	2.5	0.085	3400
10,000	4.76	0.0085	40	10,000	400	0.25	0.0085	3400

Table 33.2

HIGH FREQUENCY MODEL OF FET

In Figure 4, high frequency model of MOSFET is set up for calculating the short circuit current. We follow the same procedure as we followed in CE BJT.

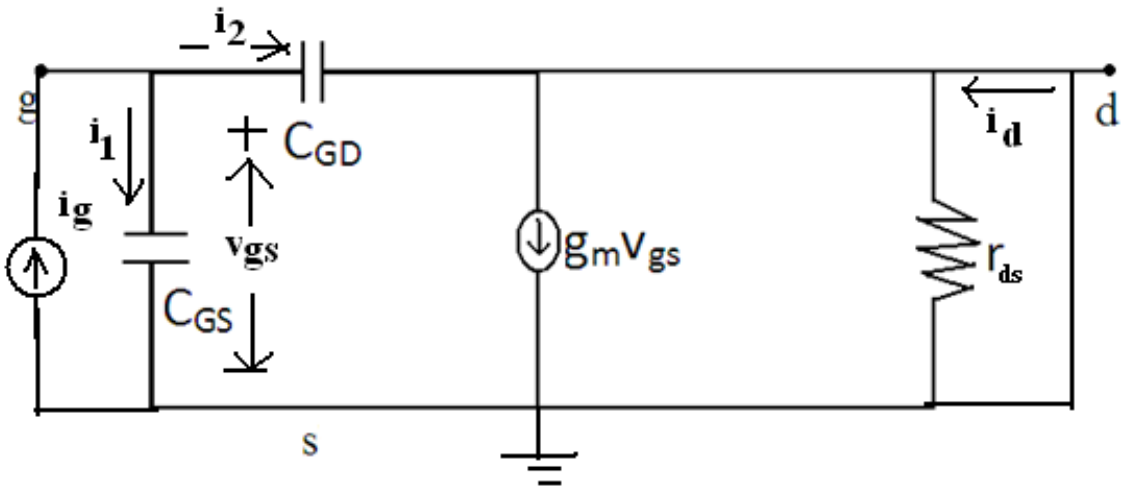


Figure4.. The incremental model of MOSFET at high frequency

Figure 33.19

There are various values for C_{gs} and C_{gd} in Triode Region, in Pentode Region and in Cut-off Region. In Analog Electronics for linear applications we are concerned only with Pentode Region. So we will consider the two capacitances in Pentode or in Saturation Region.

$C_{GS} = (2/3)\ C_{GC} + C_{GSO}.W$

$C_{GD} = C_{GDO}.W$

Where $C_{GC} = C_{OX}.WL$ and $C_{OX} = (\varepsilon_0.\ \varepsilon_{oxide})/D_{oxide}$ F/cm^2;

C_{GSO} = overlap capacitance between Gate and Source;

C_{GDO} = overlap capacitance between Gate and Drain;

Since r_{ds} is shorted therefore :

$I_2(j\omega) + I_d(j\omega) = g_m .\ V_{gs}(j\omega)$ 3

$V_{gs}(j\omega) = I_g(j\omega)/(j\omega(C_{GS} + C_{GD})$ 4

From Eq3 and Eq4:

$$\beta(j\omega) = \frac{I_d(j\omega)}{I_g(j\omega)} = \frac{g_m(1-\frac{j\omega C_{GD}}{g_m})}{j\omega(C_{GS}+C_{GD})}$$

Figure 33.20

5

Eq 5 can be rewritten as :

$$\beta(j\omega) = \frac{\omega_T}{j\omega}\left(1 - \frac{j\omega}{\omega^*}\right)$$

Figure 33.21

6
Where $\omega_T = g_m/(C_{GS} + C_{GD})$ = Unity Gain BW or Gain×BW or Gain BW Product(GBP);
And $\omega^* = g_m/C_{GD}$ and $\beta(j\omega)$ falls at 20dB per decade.
Through proper substitutions in GBP expression we get :

$$\omega_T = \frac{g_m}{(C_{GS} + C_{CD})}$$

Figure 33.22

$$f_T = \frac{3}{2}\mu_n \frac{(V_{GS} - V_{TN})}{L^2}$$

Figure 33.23

A reduction in channel length by a factor of 10 increases f_T by 100.
In BJT GBP $< 1/(r_x C_\mu)$
BODY EFFECT or SUBSTRATE SENSITIVITY

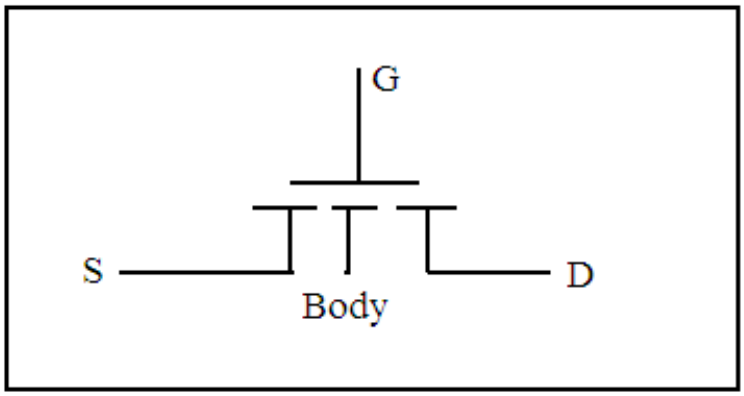


Figure 5. The symbol of (E)NMOS.

note there are 4 terminals: three for Source, Gate and Drain and fourth for the substrate or the body.

Figure 33.24

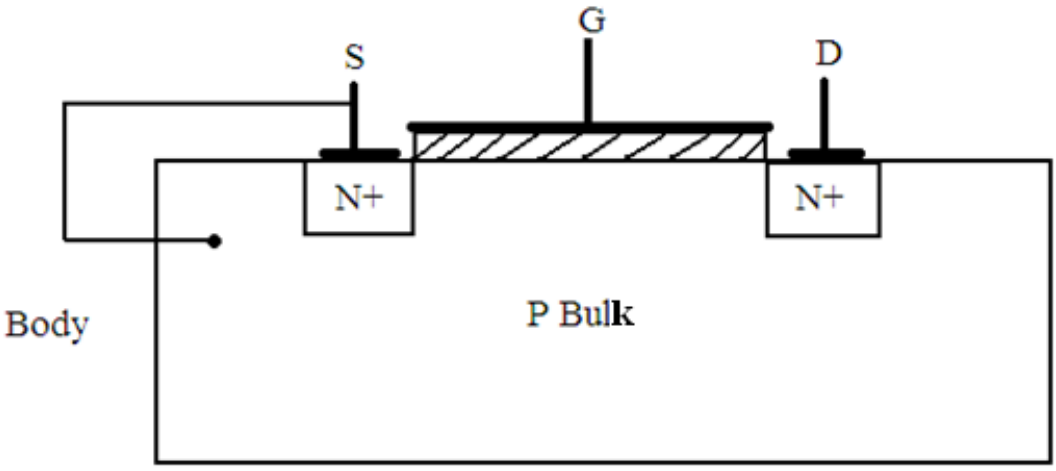


Figure 6. NMOS with source tied with body.

Figure 33.25

$$When\ V_{SB} = 0V, V_{TN} = 1V$$

Figure 33.26

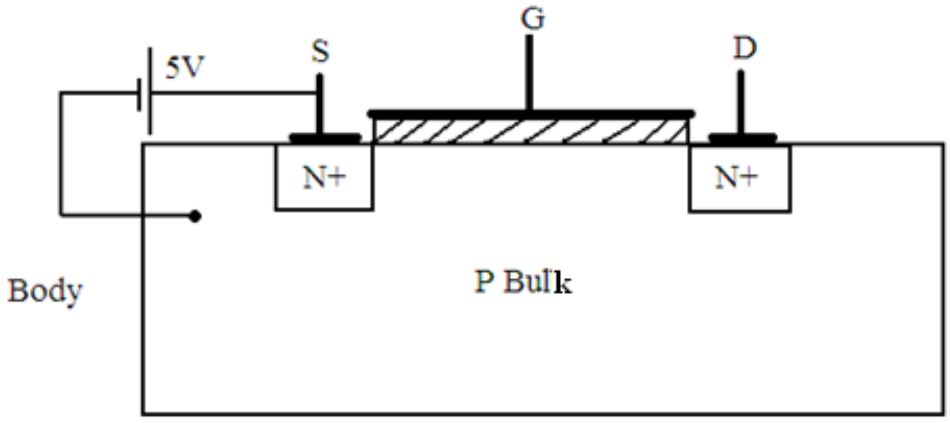


Figure 7. Here there is Source to Substrate bias of 5V.

Figure 33.27

$$When\ V_{SB} = 5V, V_{TN} = 2V$$

Figure 33.28

$$V_{TN} = V_{TO} + \gamma\left(\sqrt{V_{SB} + 2\Phi_F} - \sqrt{2\Phi_F}\right)$$

Figure 33.29

Where

$$V_{TO} = Zero\ substrate\ bias\ value\ for\ V_{TN}(V)$$

Figure 33.30

$$\gamma$$

Figure 33.31

=*Body Effect parameter*

$$\left(\sqrt{V}\right)$$

Figure 33.32

$$2\Phi_F = Surface\ Potential\ Parameter$$

Figure 33.33

(V)
Typical Values are :-

$$-5V \leq V_{TO} \leq 5V$$

Figure 33.34

$$0 \leq \gamma \leq$$

Figure 33.35

3

$$\sqrt{V}$$

Figure 33.36

$$0.3V \leq 2\Phi_F \leq 1V$$

Figure 33.37

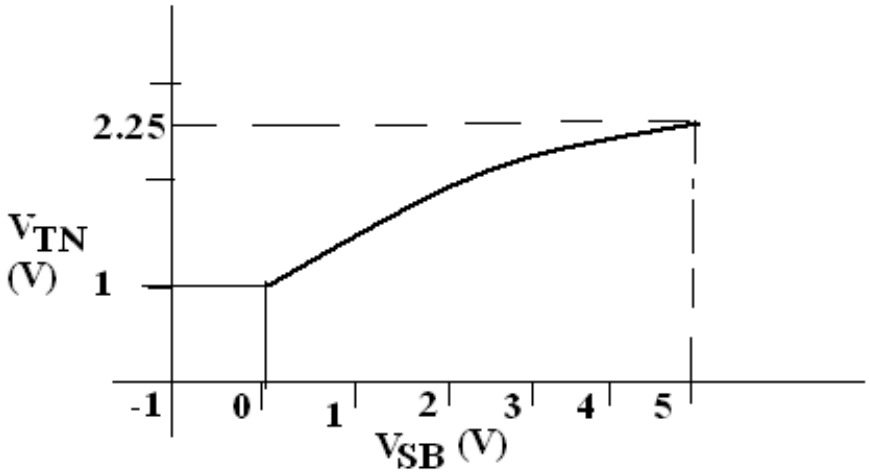


Figure 8. Threshold Voltage vs Source to Bulk voltage.

Figure 33.38

Chapter 34

AE_Lecture 9_revised_Noise(Untitled)[1]

Lecture no-9 Noise sources and theoretical formulation of noise parameters.

Internal Noise Sources

- Resistors
- Vacuum Tubes
- BJT & Other Solid State Devices

External Noise Sources

- Atmospheric
- Man Made Electric DC Machines
- Extraterrestrial sources
- Multiple Transmission Paths
- Random Changes in attenuation within the transmission medium.

1.ATMOSPHERIC NOISES

Due to electric discharge in thunder clouds spurious radio waves are produced.

In time domain, electric discharge is a SPIKE (or a Dirac Delta Function). In frequency domain we have uniformly distributed RF waves in MW region 540kHz to1.6 MHz. Below 100MHz field strength of the radiations from the electric discharges are significant in Medium Wave Range of RF and not in Short Wave Range. This is why during thunder storms maximum static is produced in MW Range of radio reception.

2.MAN MADE SOURCES

- High voltage powerline corona discharge.
- Commutator-generated noise in DC electric motors..
- Switching gear noise.
- EM Interference by high intensity radio transmitters in neighbourhood.

3.EXTRATERRESTRIAL NOISE SOURCES

i. Periodic increase in Solar Activities(The period is 11 years) in the form of increased sun-spots and furious sun-flares lead to major disruptions in power transmissions and communication systems. The surface of the Sun is a roiling mass of plasma- charged high-energy particles- some of which escape from the surface and travel through the space as the solar wind. During a sun storm solar wind carries billion-tonne glob of plasma, a fireball known as coronal mass ejection(CME). If the CME hits the Earth, it changes the configuration of Earth's Magnetic field leading to severe Electro-Magnetic Induction in the long lines of Power Grids. This will cause increased dc currents leading to saturation

[1]This content is available online at <http://cnx.org/content/m35842/1.1/>.

of the magnetic core of the transformers. The saturation of magnetic cores will limit the opposing e.m.f. leading to runaway currents in the secondary coil. This leads to rapid heating, melting of the transformer. One such event in March 1989 in Quebec, Canada, left 6 million people without electricity for 9 hours.

ii. Global Radio Broadcast at short wave RF gets seriously affected due to disruptions of ionosphere surrounding the Earth.

iii. QUASERS-Quasi-Stellar Radio Sources are important Radio Noise Sources in frequency range from MHz to GHz.

iv. Pulsars RF interference- Pulsars are Neutron Stars which are rapidly spinning and which have the magnetic field axis inclined to geo-graphical polar axis of spin. Due to this inclination, there is synchrotron radiation covering the entire span of spectrum. It emits radio waves, optical waves, X-Rays and Gamma Rays. This is emitted from the polar ends of the magnetic axis. Hence a beam of EM radiation are sweeping the entire space around the spinning Neutron Star at the same rate as that at which it is spinning. If our Earth falls in its line of sight, it receives periodic burst of EM radiations hence they are called pulsars. This is generally very weak hence does not cause much disturbance on Earth.

4.MULTIPLE TRANSMISSION PATHS-This occurs due to reflection off buildings, earth, airplanes & ships or from refraction from stratification in the transmission medium.

1. Diffused Noise Source-received signals are numerous reflected components.
2. Specular Noise Source-Received signals are one or two reflected strong rays.

5.RANDOM CHANGES IN ATTENNUATION IN THE ATMOSPHERE -this leads to fading.

INTERNAL NOISE SOURCES

Thermal Noise :- Random Motion of electrons in the conductor leading to fluctuations in the conducting semi free electron density(n) in the metallic lattice. This leads to fluctuating dipole leading to thermal voltages. This directly depends on the absolute temperature of the conductor.

Shot Noise:- Statistical fluctuations in the thermionic emissions from the cathode or the fluctuations in the forward current in the forward biased pn junction diode.

Partition Noise:- Statistical fluctuations in the current division or current merger in Vacuum tubes or in solid state devices.

Flicker Noise:-The number of free electrons or holes present in the channel decide the conductivity of the channel in FET devices. But due to interface states at the Gate Oxide in MOS the channel conductivity fluctuates due to random capture of majority carriers from the channel. This noise is inversely proportional to frequency. Hence it is also known as [

$$\frac{1}{f}]$$

Figure 34.1

noise.

Thermal Noise in Resistors(R)

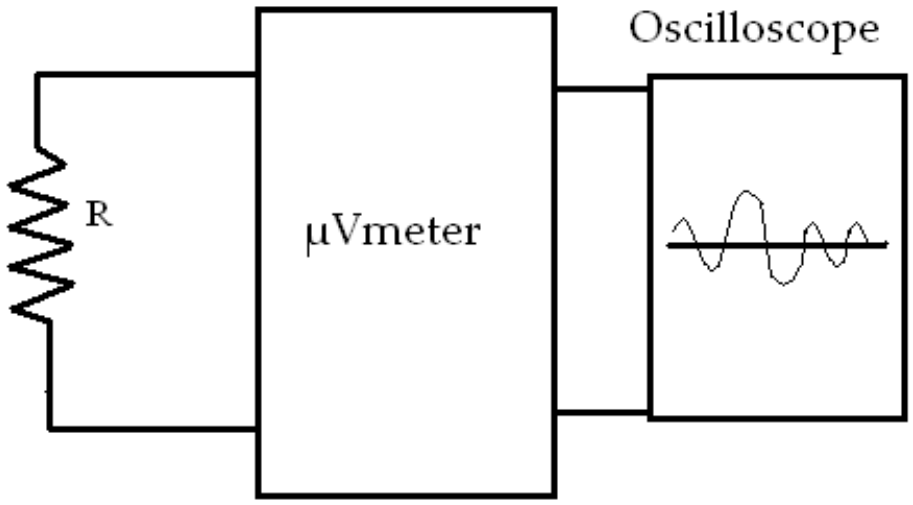


Figure 1. Thermal Noise can be detected across the terminals of resistance by a sensitive ac voltmeter or by a sensitive oscilloscope.

Figure 34.2

Random motion of electrons due to thermal energy(

$\frac{1}{2}kT$ *is the thermal energy asosciated with electron for every degree of freedom*

Figure 34.3

)leads to fluctuating dipole in the metallic lattice. This leads to random voltage fluctuation at the terminals.

This random voltage

$$\propto T(in\ kelvin)$$

Figure 34.4

Mean Square Noise Power Spectral density=

$$kT\ (Joules) = kT\left(\frac{W}{Hz}\right) = S_N$$

Figure 34.5

In double sided representation

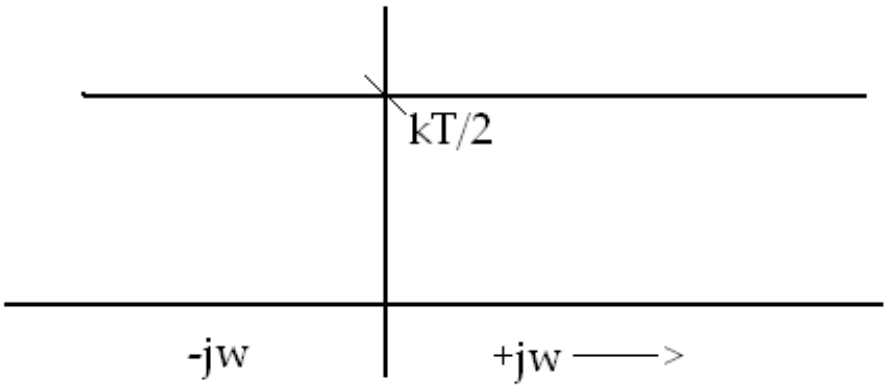


Figure 34.6

Figure 2. Noise Power Spectral Density Distribution w.r.t. frequency in a double sided spectrum.

We have almost uniform Noise Power Spectral Density over the entire frequency spectrum. Therefore Thermal noise(Johnson Noise) is also known as White Noise. Just as WHITE LIGHT has all the seven colours in equal magnitude, in the same way WHITE NOISE has equal spectral components over the entire frequency spectrum.

The actual Noise Power measured will depend on the Bandwidth B Hz.

Therefore Mean Square Noise Power in a resistance over B Hz.

$$P_{an} = S_N B$$

Figure 34.7

watts= available noise power;

$$P_{an} = kTB\ Watts$$

Figure 34.8

At 300K,

$$S_N = kT = 4.412 \times 10^{-21} J$$

Figure 34.9

=

$$4.412 \times 10^{-21} W/Hz$$

Figure 34.10

Let BW=1MHz

$$\therefore P_{an} = kTB = 4.412 \times 10^{-15} W$$
$$= Avaiable\ Power\ assosciated\ with\ Thermal\ Noise$$

Figure 34.11

This is the noise available from the resistance under consideration.

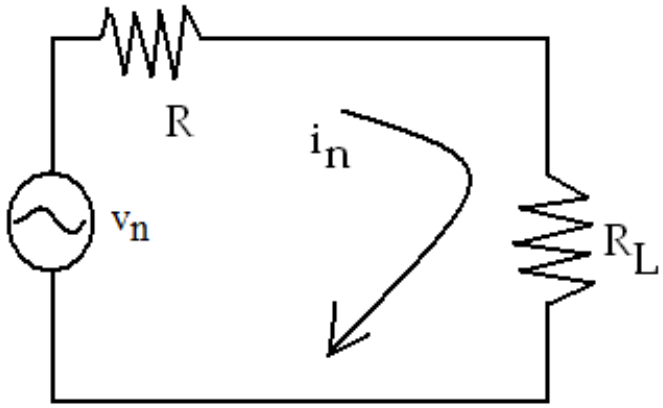


Figure 34.12

Figure 3. Equivalent circuit of a noisy resistance connected to load. The noisy Resistor has been represented as a noise voltage source of v n delivering noise voltage to the load and with an internal resistance R having no noise.

$$(i_n)_{RMS} = \frac{v_n}{R + R_L}$$

Figure 34.13

If $R=R_L$, then

$$(i_n)_{RMS} = \frac{v_n}{2R}$$

Figure 34.14

Maximum power transferred to R_L =Available noise power from the resistance to the load
=

$$i_n^2 R_L = i_n^2 R = P_{AN}$$

Figure 34.15

= kTB

$$\therefore P_{AN} = \frac{v_n^2}{4R^2} \times R = \frac{v_n^2}{4R}$$

Figure 34.16

$$\therefore v_n^2 = 4RP_{AN} = 4RkTB$$

Figure 34.17

Mean Square Noise Voltage= $<v_n^2>$ =

$$4RkTB$$

Figure 34.18

RMS Value of Noise Voltage=$\sqrt{<v_n^2>}$ =

$$\sqrt{4RkTB}$$

Figure 34.19

If R=1k, B=1MHz, T=300K

$$\sqrt{\left(\overline{v_n^2}\right)} = rms\ V_n = 4\mu V$$

Figure 34.20

$$RMS\ value\ of\ \ Noise\ Voltage = 4\mu V$$

Figure 34.21

The signals received at the antenna of a receiver is of comparable amount and hence the intelligent signal can easily be swamped by the thermal noise at the front end of a communication receiver. In deep space communication the problem is further compounded due to the fact that received signal from PIONEER or VOYAGER from the very edge of heliosphere is one or two orders of magnitude fainter than 4μV.

CALCULATION OF EFFECTIVE NOISE TEMPERATURE and DEFINITION of NOISE FIGURE.

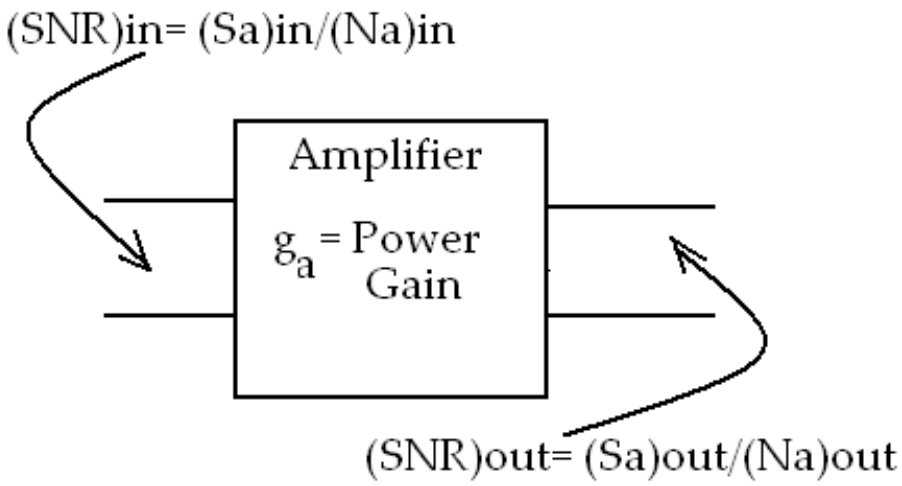


Figure 34.22

Figure 4. A two port network with SNR at the input and output.
SNR=Signal to Noise Ratio=

$$\frac{Mean\ Square\ Signal\ Voltage}{Mean\ Square\ Noise\ Voltage} = \frac{<V_s^2>}{<V_n^2>}$$

Figure 34.23

$$(S_a)_{out} = g_a(S_a)_{in}$$

Figure 34.24

$$(N_a)_{out} = g_a(N_a)_{in}$$

Figure 34.25

So, ratio

$$\left(\frac{S_a}{N_a}\right)_{out} = (SNR)_{out} = \left(\frac{S_a}{N_a}\right)_{in} = (SNR)_{in}$$

Figure 34.26

But actually it is not so because there is some internally generated noise in the amplifier.
Thus

$$(N_a)_{out} \neq g_a(N_a)_{in}$$

Figure 34.27

It is actually:

$$(N_a)_{out} = g_a(N_a)_{in} + N_{int}$$

Figure 34.28

Thus:

$$(SNR)_{out} = \frac{g_a(S_a)_{in}}{g_a(N_a)_{in} + N_{int}}$$

Figure 34.29

$$(SNR)_{out} = \frac{\frac{g_a(S_a)_{in}}{g_a(N_a)_{in}}}{1 + \frac{N_{int}}{g_a(N_a)_{in}}} = \frac{(SNR)_{in}}{1 + \frac{N_{int}}{g_a(N_a)_{in}}}$$

Figure 34.30

Therefore:
Noise Figure=

$$\frac{(SNR)_{in}}{(SNR)_{out}} = 1 + \frac{N_{int}}{g_a(N_a)_{in}}$$

Figure 34.31

An Ideal Noise Figure for an amplifier should be 0dB but it is never 0dB in actual practice. In actual practice the noise figure can be 0.1dB/ 0.2dB/0.5dB/1 dB or more.

EFFECTIVE NOISE TEMPERATURE

At the input:

$$(N_a)_{in} = kT_iB$$

Figure 34.32

There is a thermal noise generator of equivalent temperature=

$$T_i$$

Figure 34.33

This is the noise picked up by the antenna .
The noise power at the o/p:

$$(N_a)_{out} = g_akT_iB + \Delta N$$

Figure 34.34

Here

$$\Delta N = Internal\ Noise\ Power$$

Figure 34.35

Therefore:

$$(N_a)_{out} = g_akB\left(T_i + \frac{\Delta N}{g_akB}\right)$$

Figure 34.36

Thus:

$$(N_a)_{out} = g_a kB(T_i + T_e)$$

Figure 34.37

Where:

$$T_e = Effective\ Noise\ Temperature\ of\ \Delta N$$

Figure 34.38

=

$$\frac{\Delta N}{g_a kB}$$

Figure 34.39

$$(SNR)_{in} = \left(\frac{S_a}{N_a}\right)_{in} = \frac{(S_a)_{in}}{kT_i B}$$

Figure 34.40

$$(SNR)_{out} = \frac{g_a (S_a)_{in}}{g_a kB(T_i + T_e)}$$

Figure 34.41

$$Noise\ Figure = \frac{(SNR)_{in}}{(SNR)_{out}} = \left(1 + \frac{T_e}{T_i}\right)$$

Figure 34.42

While the signal is passing through an amplifier the signal to noise ratio deterioration is defined by

$$\frac{T_e}{T_i}$$

Figure 34.43

. If by cryogenic cooling effective noise temperature of the front end amplifier is minimized to zero then we achieve the ideal N.F. of 1 or 0dB.

IN COMMUNAICATION RECEIVER SYSTEMS

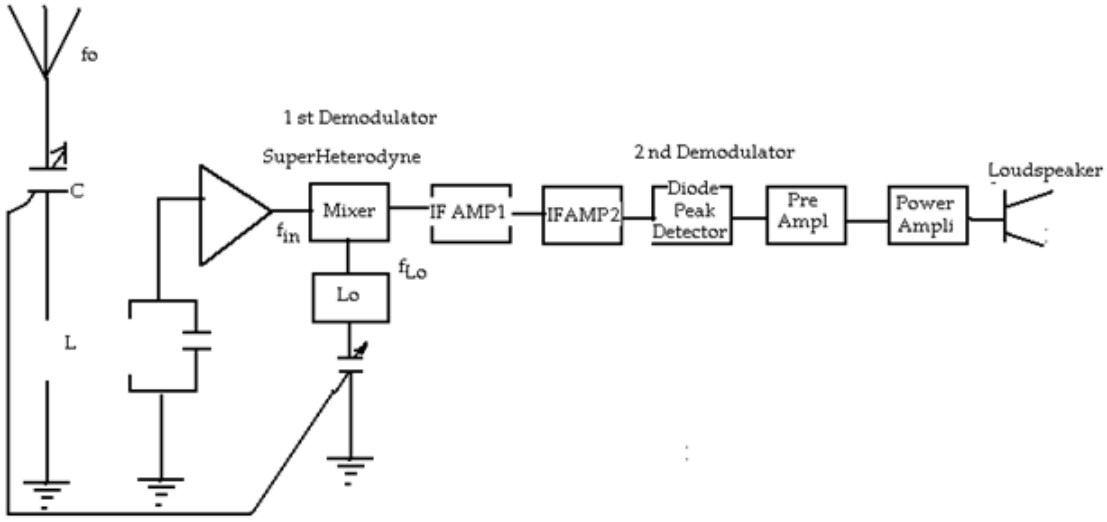


Figure 34.44

Figure 5. A Communication Receiver in RF range. Different stages of the receiver are shown. In the first stage we have series resonance circuit tuned to a given station or tuned to a given communication frequency. At resonance frequency maximum electromagnetic induction takes place and maximum current is introduced in the primary coil of RF Transformer. The

first stage is a RF tuned amplifier. After amplification, picked up radio frequency is downward frequency translated to intermediate frequency (IF). IF is 455kHz in AM Radio Receivers or 10.7MHz in TV or FM Radio.IF signal is amplified and then second detection or demodulation takes place. In the second detection it is again downward frequency translated to base band signals. This base band signal is voltage amplified by pre-amplifier and power amplified by Complementary Symmetry Amplifier. The power amplified is fed to the Speaker or Video Monitor.

The first downward frequencytranslation is known as 1st detection or 1st demodulation. This is also known as superhetrodyne mixing of tuned frequency f_0 and f_{Lo} and $f_{Lo} - f_0$ = Intermediate Frequency (I.F.).

FRISS FORMULA will have to be utilized to calculate the overall noise figure.

FRISS FORMULA

What is the overall noise figure of 2 cascaded stages ?

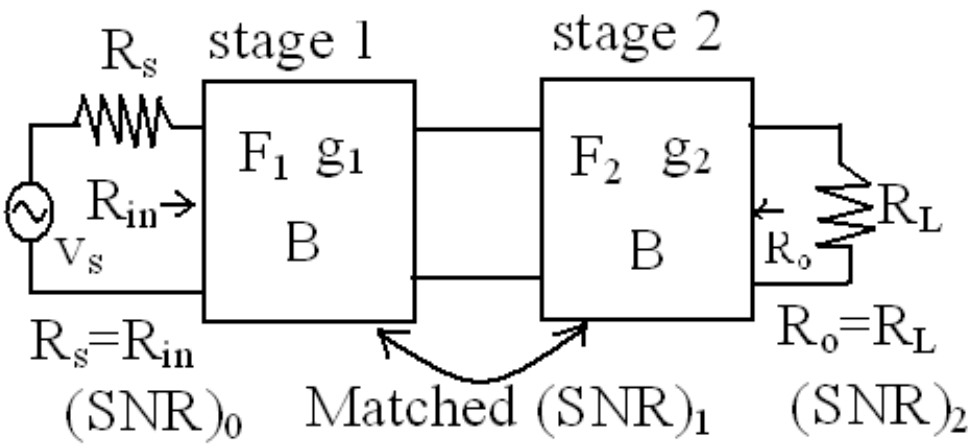


Figure 34.45

Figure 6: Two Stage Cascaded Amplifier

We have a matched network for maximum power transfer.

Overall Noise Figure

$$F = F_1 + \frac{(F_2 - 1)}{g_1}$$

Figure 34.46

For n Stage cascade system:

$$F = F_1 + \frac{(F_2 - 1)}{g_1} + \frac{(F_3 - 1)}{g_1 g_2} + - - - - - - + \frac{(F_n - 1)}{g_1 g_2 - - - g_{n-1}}$$

Figure 34.47

This formula implies that the overall Noise Figure is dominated by the noise figure of the first stage.

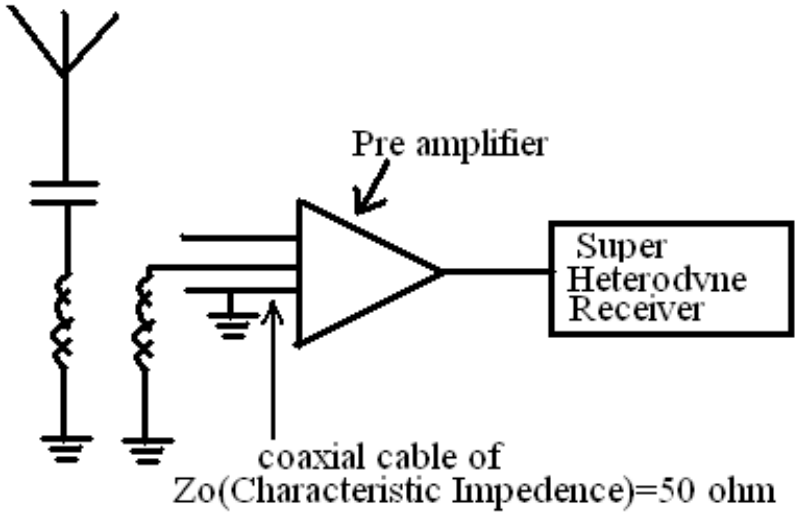


Figure 7(a) A Typical Antenna Stage With A Preamplifier

Figure 34.48

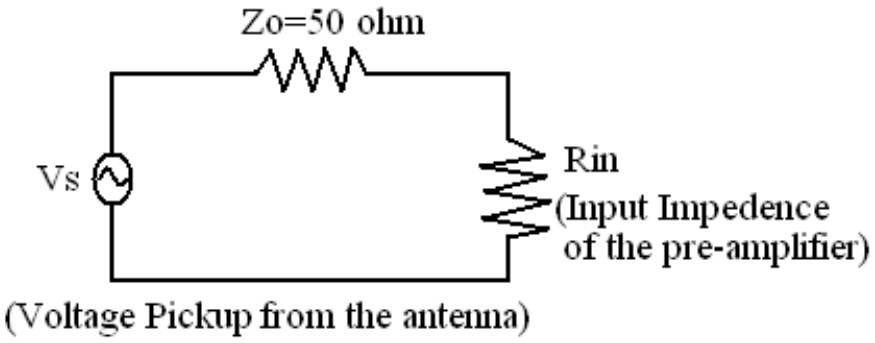


Figure 7(b) Equivalent Circuit Of the antenna Stage Of the receiver(Zo=Rin for maximum power transfer)

Figure 7 INPUT STAGE OF A RECEIVER OR THE FRONT END OF THE RECEIVER

Figure 34.49

Front end amplifier is referred to as Low Noise Amplifier.

With a good front-end having cryogenic cooling, we achieve a good amplification with no deterioration in SNR as we proceed along the cascade chain.

Table 1. Typical Noise Figure

Amplifier	NF(abs)	NF(dB)	T_e (K)	Gain(dB)	f_{op}(GHz)
Parametric Amplifier(uncooled)	1.45	1.61	130	10-20	9
Parametric Amplifier(77K)	1.17	0.69	50	10-20	3&6
Parametric Amplifier(4K)	1.03	0.13	9	10-20	4
Travelling Wave Tube(TWT)	1.59	2.00	170	20-30	2.66
	1.86	2.7	250		3
	2.69	4.3	490		9
Tunel Diode Amplifier-Ge	2.38	3.77	400	20-40	?
Tunnel Diode Amplifier-GaAs	1.69	2.28	200	20-40	?
Low Noise Heterodyne Receiver	2.38	3.77	400	20-40	500kHz-30MHz
IC BJT IF Amplifier for TV	5.01	7	1163	50	10.7MHz
GaAs MESFET Amplifier	?	?	?	?	?

Table 34.1

(1)Mumford & Scheibe,Noise Performance Factors in Communication Systems,Horizon House-Microwace,Inc,Dedham,Massachusets(1968),pp 36,39
(2)Linear Integrated Circuits Data Book,Motorola Inc.,(1974).
References:
1.Ziemer & Tranter,Principles of Communications-System,Modulation and Noise,Wiley India,5th Edition,2002.
2. Shanmugam,Digital and Analog Communication Systems, Wiley-India,Reprint 2007.

APPENDIX-1. Derivation Of The FRISS FORMULA (Refer to figure 6)

Noise at the output of the second stage is:

$$N_{a2} = g_2 N_{a1} + \Delta N_2$$

Figure 34.50

_ _ _ _ _ _(1)

Similarly the output of the first stage is:

$$N_{a1} = g_1 N_{a0} + \Delta N_1$$

Figure 34.51

_ _ _ _ _ _(2)

Available Noise power Input at the First stage is:

$$N_{a0} = kT_o B$$

Figure 34.52

_ _ _ _ _ _ _ _(3)

Substituting (3) into (2), we get,

$$N_{a1} = g_1 kT_o B + \Delta N_1$$

Figure 34.53

_ _ _ _(4)

Substituting (4)in (1),we get,

$$N_{a2} = g_2(g_1 kT_o B + \Delta N_1) + \Delta N_2$$

Figure 34.54

Further Simplifying it,

$$N_{a2} = g_2 g_1 kB(T_o + \Delta N_1 / g_1 kB) + \Delta N_2$$

Figure 34.55

_ _ _ _ _ _(5)
But

$$\Delta N_1 / g_1 kB = T_{e1} = Effective\ Temperature\ of\ the\ stage\ 1$$

Figure 34.56

_ _(6)
And

$$\Delta N_2 / g_2 kB = T_{e2} = Effective\ Temperature\ of\ the\ stage\ 2$$

Figure 34.57

_ _ _(7)
Also,

$$F_1 = 1 + T_{e1} / T_o$$

Figure 34.58

and

$$F_2 = 1 + T_{e2}/T_o$$

Figure 34.59

_ _ _ _ _ _ _ (8)
From Eq(8), we have

$$T_{e2} = (F_2 - 1)T_o$$

Figure 34.60

_ _ _ _ _ _ _ (9)
From Eq(9)and(7),

$$\Delta N_2 = T_{e2}\, g_2 kB = (F_2 - 1)T_o g_2 kB$$

Figure 34.61

_ _ _ _ _ (10)
Using relations(6) ,(8) and(10),
Eq(5) can be re-written as:

$$N_{a2} = g_2 g_1 kB(T_o + \Delta N_1/g_1 kB) + \Delta N_2$$

Figure 34.62

$$N_{a2} = g_2 g_1 kB(T_o + T_{e1}) + (F_2 - 1)T_o g_2 kB$$

Figure 34.63

Simplifying:

$$N_{a2} = g_2 g_1 kBT_o F_1 + (F_2 - 1) g_2 kBT_o$$

Figure 34.64

_ _ _ _ _ _(11)
But,

$$N_{a2} = kBT_o g_2 g_1 F$$

Figure 34.65

_ _ _ _ _(12)
[this is arrived at by induction logic recognizing the $N_{a1}=g_1 kBF_1 T_0$]
Where F is the overall noise figure.
Hence dividing(11)by (12), we get,

$$F = F_1 + \frac{F_2 - 1}{g_1}$$

Figure 34.66

_ _ _ _ _ _(13)
For 3 stages:

$$F = F_1 + \frac{F_2 - 1}{g_1} + \frac{(F_3 - 1)}{g_1 g_2}$$

Figure 34.67

_ _ _ _ _ _ _(14)
For n stages:

$$F = F_1 + \frac{(F_2 - 1)}{g_1} - - + \frac{(F_n - 1)}{g_1 g_2 - - - g_{n-1}}$$

Figure 34.68

_ _ _ _ *(15) FRISS FORMULA.*

Chapter 35

AE_Lectur10_PowerAmplifiers_Part1_Power Analysis of Emitter Follower.[1]

The Output Stage Of an Electronic system

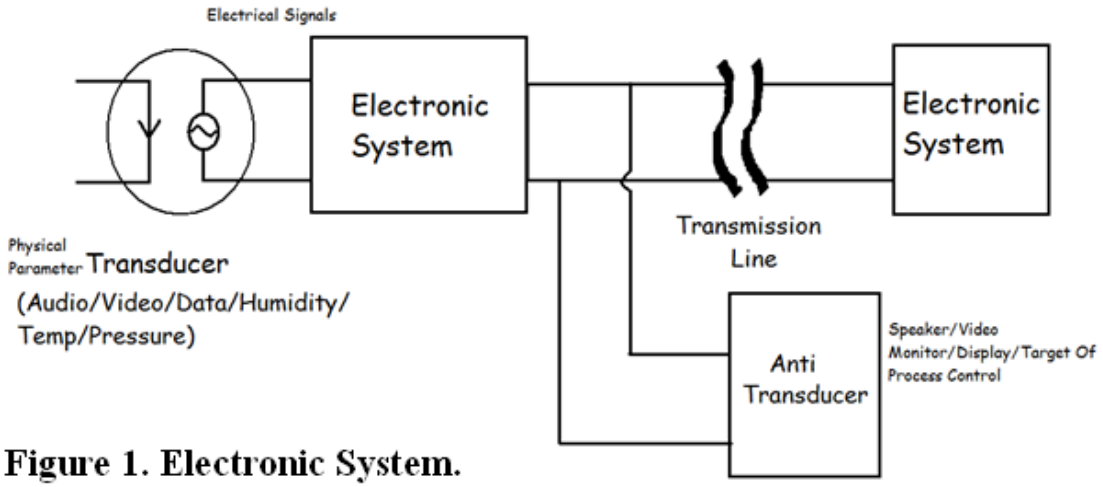


Figure 35.1

Figure 1. The Block Diagram of an Electronic System.

The output of an electronic system is invariably a Speaker/VideoMonitor/VideoDisplay/Target of a Process Control System. Driving any of these loads requires power. Power means(voltage × current). Since most of the systems are using low voltages(Logic Systems have 5V,Analog systems also operate at 5V) hence output stage has to deliver a large current in order to drive a load like speaker/video monitor/display/transmission lines.

This output stage must be a voltage controlled voltage source (VCVS).

[1] This content is available online at <http://cnx.org/content/m32256/1.1/>.

WHY Output STAGE IS VCVS??

Because O/P is preceded by the pre-amplifier which amplifies voltage only.

O/P must be a voltage source with a low output impedence. This ensures a constant voltage drive for variable load. The voltage gain has been provided by the preamplifier. Power Amplifier or the ouput amplifier is required to provide current amplification. O/P stage is a large signal amplifier hence considerable amplitude distortion occurs. This has to be minimized..

All the above requirements are fulfilled by the CC-BJT configuration.

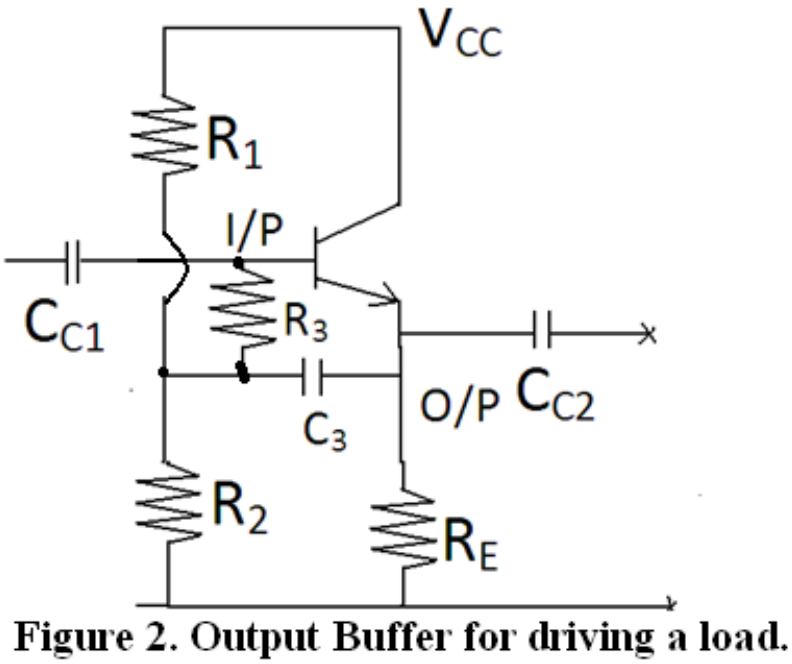


Figure 2. Output Buffer for driving a load.

Figure 35.2

Figure 2. CC or Emitter Follower stage.

If R1||R2 is neglected by BOOTSTRAPPING then:

$$R_{in} = (1 + \beta_{fo})R_E$$

Figure 35.3

$$R_{out} = R_E || \left(\frac{r_\pi + R_S}{\beta_{fo} + 1} \right)$$

Figure 35.4

$$A_i = \beta_{fo}$$

Figure 35.5

This is an ideal VCVS.

CC BJT is also known as EMITTER FOLLLOWER.

So Emitter Follower is always the O/P stage of the Electronic system. Emitter Follower also isolates the load from the system. Hence it is called a BUFFER .

If suitable power transistors with heat sink is utilized then emitter follower can deliver a large current and hence a large power to the load. But it has a problem:

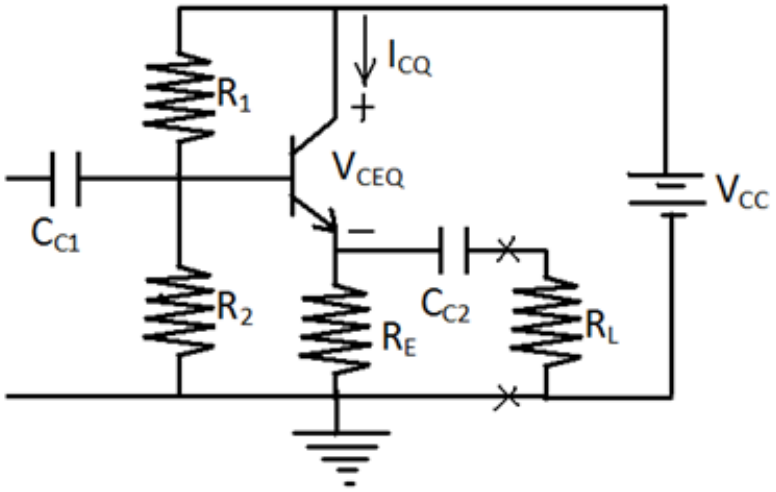


Figure 3. Circuit Diagram of CE Amplifier.

Figure 35.6

$$Generally\ V_{CEQ} = \frac{1}{2} V_{CC}\ to\ obtain\ maximum\ symmetrical\ swing$$

Figure 35.7

$$\&\ \ I_{CQ} = \frac{V_{CC} - V_{CEQ}}{R_E} = \frac{1}{2}\frac{V_{CC}}{R_E}$$

Figure 35.8

$$\therefore \textit{Device Dissipation} = I_{CQ} \times V_{CEQ}$$

Figure 35.9

$$= \left(\frac{1}{2}\frac{V_{CC}}{R_E}\right)\left(\frac{1}{2}V_{CC}\right) = \frac{1}{4}\frac{V_{CC}^2}{R_E}$$

Figure 35.10

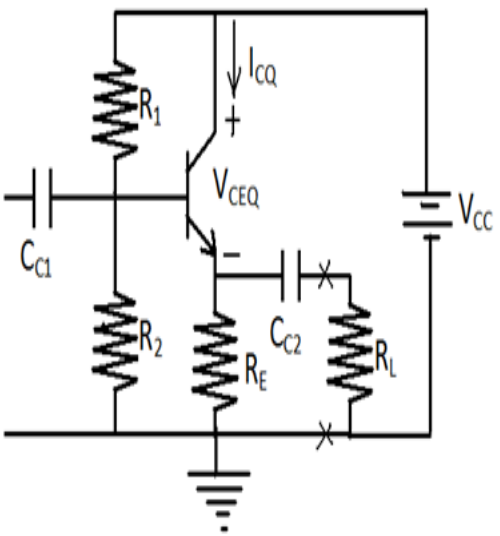


Figure 3. Circuit Diagram of CE Amplifier.

Figure 35.11

Under Maximum Symmetrical Swing

Amplitude of the O/P Voltage across R_L

$$= \left(\frac{V_{CC}}{2}\right)$$

Figure 35.12

$$\therefore \textit{Power delivered to the load} = \frac{(v_{rms})^2}{R_L} = \left(\frac{V_{CC}}{2\sqrt{2}}\right)^2 \times \frac{1}{R_L} = \left(\frac{V_{CC}^2}{4 \times 2 \times R_L}\right)$$

Figure 35.13

$$\textit{Power delivered to the load} = P_L = \left(\frac{V_{CC}^2}{8R_L}\right)$$

Figure 35.14

$$\textit{Total D.C. Power Deivered by the Battery} = (V_{CC})(I_{DC})$$

Figure 35.15

Where

$$I_{DC} = I_{CQ} = \frac{1}{2}\frac{V_{CC}}{R_E}$$

Figure 35.16

$$\therefore P_{in} = V_{CC} \times \frac{1}{2}\frac{V_{CC}}{R_E} = \frac{V_{CC}^2}{2R_E}$$

Figure 35.17

$$\therefore Efficiency\ of\ Power\ Conversion = \frac{P_L}{P_{in}} = \frac{\left(\frac{V_{CC}^2}{8R_L}\right)}{\left(\frac{V_{CC}^2}{2R_E}\right)}$$

Figure 35.18

$$\eta = \frac{P_L}{P_{in}} = \frac{1}{4}\left(\frac{R_E}{R_L}\right)$$

Figure 35.19

If

$$R_E = R_L, then\ \eta = 25\ \%$$

Figure 35.20

Under no signal conditions:

$$P_{in} = P_{device} + P_{R_E}$$

Figure 35.21

$$P_{device} = Power\ dissipated\ across\ the\ device$$

Figure 35.22

$$P_{R_E} = Power\ dissipated\ across\ R_E$$

Figure 35.23

$$P_{in} = Standby\ Power$$

Figure 35.24

Even when there is no signal, power is consumed and dissipated in the form of heat. This is wasteful and not eco-friendly. CC Amplifier or Emitter Follower will always have this problem because it is operating in Class A mode.

By definition, Class A has current conducting in the active device for 360° phase angle of input signal..

Class B has current conducting in the active device for 180° phase angle of input signal.

Class AB has current conducting in the active device for slightly more than 180° phase angle of input signal.

Class C has current conducting in the active device for less than 180° phase angle of input signal.

Hence Class B and Class C mode of operation does not have the problem of standby dissipation. Under no signal condition the active device is not conducting hence standby power dissipation is zero.

Therefore we go for Class B mode of operation. Class B mode of operation will improve the power conversion efficiency from 25% in capacitance coupled load in Class A CC-BJT Amplifier to 78.8% in Class B PushPull Amplifier and in Class B complementary symmetry Amplifier. Class B Push Pull Amplifier

was Transformer Coupled Discrete Amplifier whereas Complementary Symmetry gets rid of Transformer Coupling and is amenable to Integration and its integrated version is being fabricated. This suppresses the even harmonics also which are bound to be generated because of large signal operation.

So today in Integrated Circuit Era, power amplifier is invariably Complementary Symmetry Amplifier which we will study in Part 2.

Chapter 36

AE_Lectur10_PowerAmplifiers_Part2_Power Analysis of ClassB Amplifiers.[1]

AE_LECTURE NO- 10_ Part2

CLASS B (COMPLEMENTARY CONFIGURATION)

By making I_{CQ}=0,a fantastic improvement is achieved in power conversion efficiency[Previously Push pull configuration was used but that needed transformer coupling. Now we use Complementary Symmetry Configuration which is amenable to IC Technology]

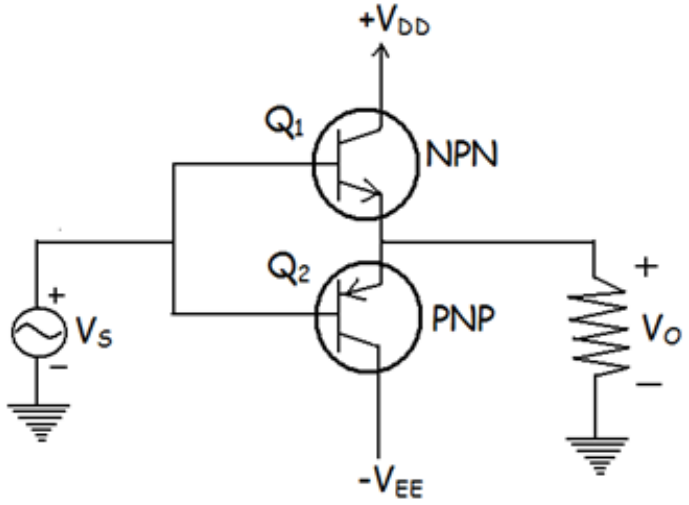


Figure 1. Complementary Symmetry Amplifier.

Figure 36.1

Figure 1. Class B Complimentary Symmetry Configuration.

[1]This content is available online at <http://cnx.org/content/m32262/1.1/>.

When v_s=0, both Q_1 and Q_2 are off.
When v_s = Positive half then
Q_1 is ON and Q_2 is OFF.
When v_s = Negative half then
Q_1 is OFF and Q_2 is ON.
In the first case Q_1 is sourcing current to the load and in the second half of the sinusoidal cycle, Q_2 is sinking the current from the load.

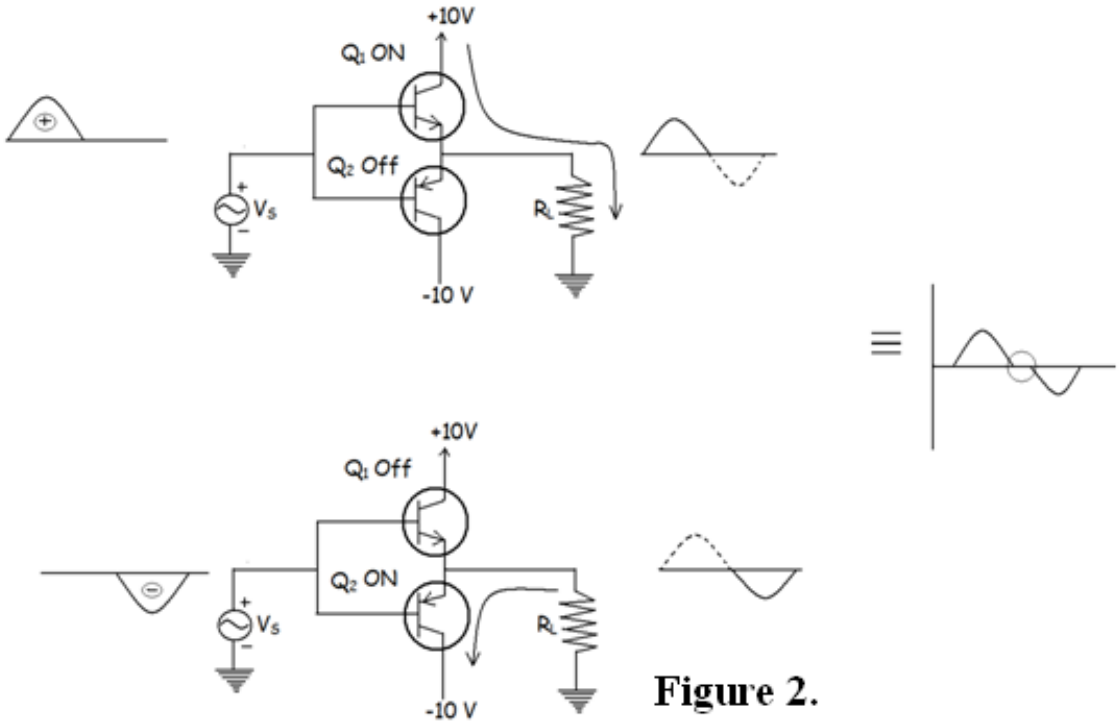


Figure 36.2

Figure 2. Complimentary Symmetry action of Q 1 and Q 2 in a Complimentary-Symmetry Amplifier.

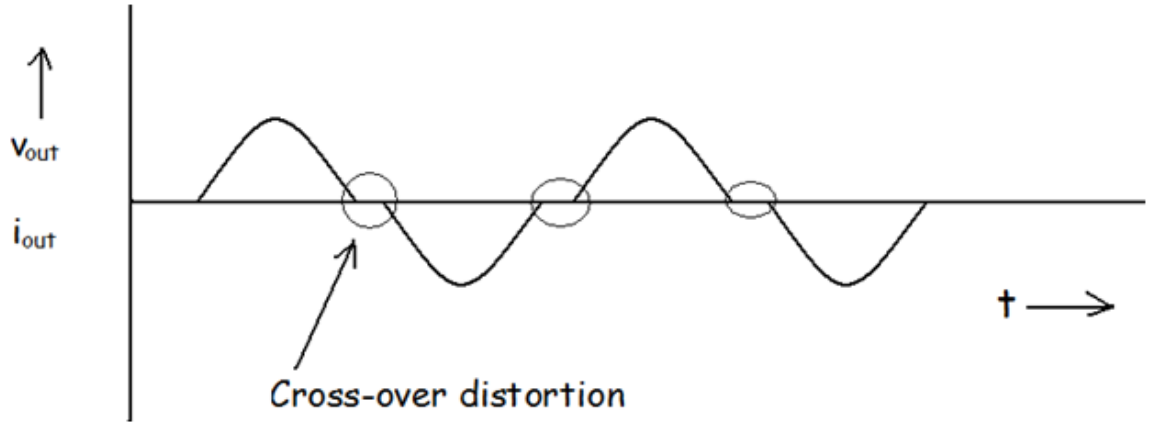


Figure 3. During transfer of conduction from Q1 to Q2 or from Q2 to Q1, momentarily both transistors are off. This is the dead zone and cause of cross-over distortion.

Figure 36.3

Figure 3. Illustration of Cross-Over Distortion in Class B mode of operation. During cross-over distortion, both Q_1 & Q_2 are off and it causes the Dead Zone.

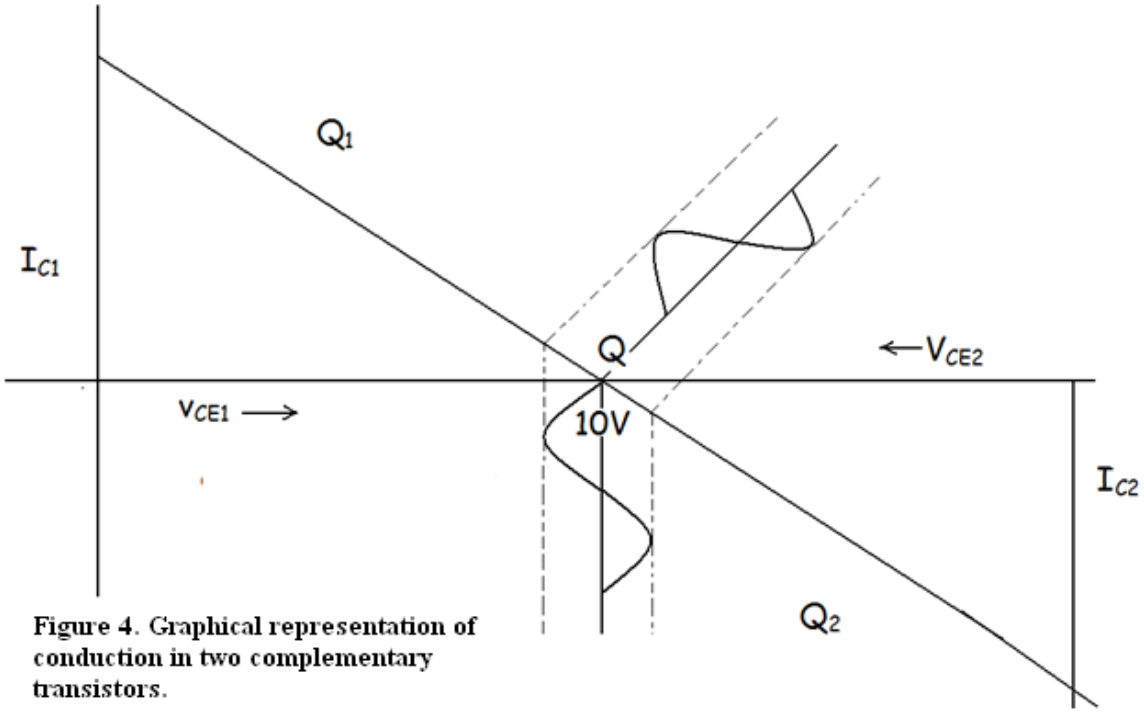


Figure 36.4

Figure 4. The load line and the dynamic swing of the Q-point under signal condition.
This is Class B operation.
Q_1 conducts for 180° of the I/P Voltage in positive half.
Q_2 conducts for 180° of the I/P Voltage in negative half.
In class A→there is one BJT Q_o. Q_o conducts for 360° of the I/P Voltage.
CLASS B Power Conversion Efficiency.
Let $|V_{CC}|=|V_{EE}|$

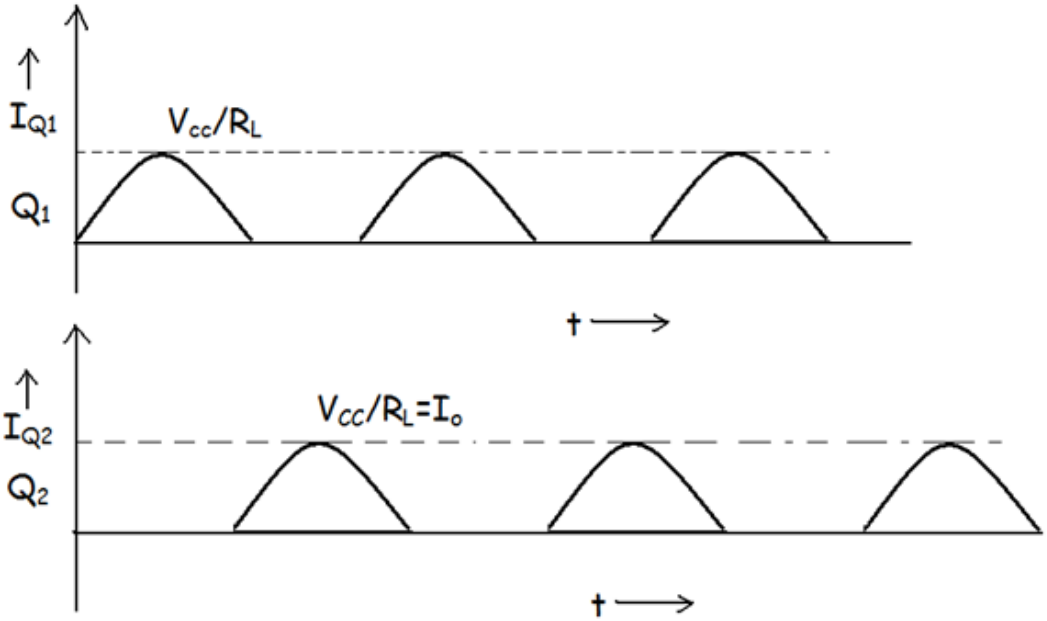


Figure 5. Conduction phase of the two complementary transistors

Figure 36.5

Figure 5. Half Wave Rectified Voltage Wave-Form passing through individual BJT but at the load there is full sinusoidal signal..

Half wave rectified current is passing through each BJT.

Average of this half wave rectified current

$$= \frac{1}{T}\int_0^{T/2} I_o \sin\omega t \; dt$$

Figure 36.6

$$= \frac{1}{T} I_o \left[\frac{-\cos \omega t}{\omega} \right]_0^{T/2}$$

Figure 36.7

$$(I_{av})_{Q_1} = \frac{1}{T} \frac{I_o}{\frac{2\pi}{T}} \left[-\cos \frac{\omega T}{2} + \cos 0 \right]$$

Figure 36.8

But

$$\frac{\omega T}{2} = \frac{2\pi}{T} \times \frac{T}{2} = \pi$$

Figure 36.9

$$\therefore (I_{av})_{Q_1} = \frac{I_o}{2\pi} [1 + 1] = \left(\frac{I_o}{\pi} \right)$$

Figure 36.10

Where

$$I_o = \left(\frac{V_{CC}}{R_L} \right)$$

Figure 36.11

Average power supplied by each battery

$$= (V_{CC})(I_{av})_{Q_1} = (V_{EE})(I_{av})_{Q_2} = \left(\frac{V_{CC} \times I_o}{\pi}\right)$$

Figure 36.12

$$\therefore \text{Average power supplied by 1 battery} = V_{CC} \times \frac{1}{\pi} \times \frac{V_{CC}}{R_L} = \frac{{V_{CC}}^2}{\pi R_L} \text{\_\_\_\_\_(1)}$$

Figure 36.13

$$\text{Total Power Supplied} = \text{Power from } V_{CC} + \text{Power from } V_{EE}$$

Figure 36.14

$$P_{Total} = \left(\frac{2{V_{CC}}^2}{\pi R_L}\right) \text{\_\_\_\_\_(2)}$$

Figure 36.15

$$\text{Power delivered to the load} = \left(\frac{I_o^2}{2} R_L\right) = \frac{1}{2}\left(\frac{V_{CC}}{R_L}\right)^2 R_L$$

Figure 36.16

$$P_{load} = \left(\frac{V_{CC}^2}{2R_L}\right)$$

Figure 36.17

$$\therefore \eta = Efficiency\ of\ power\ conversion = \frac{P_{load}}{P_{Total}} = \frac{\frac{V_{CC}^2}{2R_L}}{\frac{2V_{CC}{}^2}{\pi R_L}} = \left(\frac{\pi}{4}\right) \sim 0.785$$

Figure 36.18

Therefore 78.5% Efficiency can be achieved in full load condition.

CROSS-OVER DISTORTION is removed by Class AB operation.

Under quiescent condition , both BJT are conducting slightly so that there is no dead zone in switch over condition.

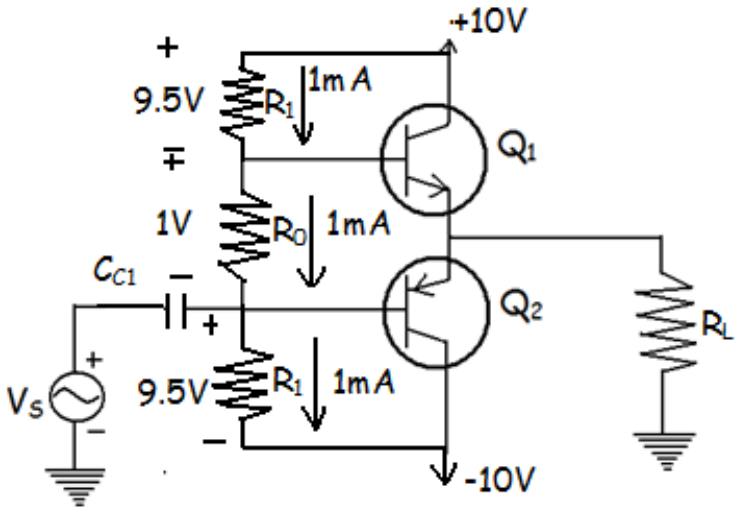


Figure 6. Biasing Network of Complementary Symmetry Amplifier for Clas AB mode of operation.

Figure 36.19

Figure 6. The Biasing Network to ensure Class AB mode of operation.

$$R_1 = R_2 = 9.K \; ; \; R_o = 1 \; K$$

Figure 36.20

1 V bias will keep Q_1 and Q_2 barely conducting because 0.5 V is the cut-in voltage and 1V across R_0 ensures that both transistors are barely conducting because they in cut-in stage.

If 1 V is not sufficient then we may take 1.1V to bias Q_1 and Q_2 so that dead zone is removed.

THE OUTPUT STAGE OF OPERATIONAL AMPLIFIER

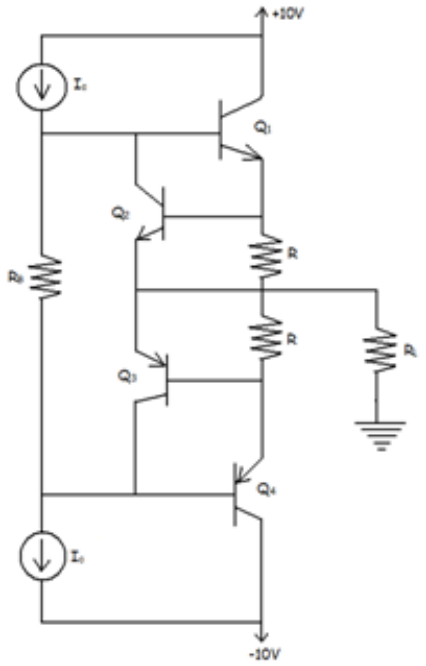


Figure 7. Output CS stage of uA741

Figure 36.21

Figure 7. The output stage of μA741 Operational Amplifier.

Q_2, Q_3 are short circuit protection BJT's.

Normally Q_2 & Q_3 are off. But as excessive current passes through Q_1 & Q_4, Q_2 or Q_3 turn ON.

In positive half,Q_2 turns ON & limits the current in Q_1 by shunting I_{B1}.

In positive half,Q_3 turn ON & limits the current in Q_4 by shunting I_{B4}.

Typically if R=25Ω then maximum output current is 28 mA because 28mA X 25 Ω=0.7 V which turns on Q_2 or Q_3 as the case may be.

TOTAL HARMONIC DISTORTION OF CLASS B AMPLIFIER

Non linear operation causes harmonic distortion or amplitude distortion.

Large signal condition leads to nonlinear operation.

SINCE power amplifier is large signal system hence harmonic distortion is inevitable.

$$v_o = V_o \cos \omega_o t + V_1 \cos 2\omega_1 t + V_2 \cos 3\omega_1 t + - - - - -$$

Figure 36.22

$$\therefore Total\ distortion\ content = \sqrt{\frac{V_1^2}{2} + \frac{V_2^2}{2} + - - - - -}$$

Figure 36.23

$$\therefore Total\ Harmonic\ Distortion = \left[\frac{\sqrt{\frac{V_1^2}{2} + \frac{V_2^2}{2} + - - - - -}}{V_o/\sqrt{2}} \right]$$

Figure 36.24

In high fidelity audio amplifiers Total Harmonic Distortion<0.1%.

Class B mode of operation ensures that even harmonic cancel.

Refer to Figure 2.

If $i_{source}\ (\omega t) = I_C + B_0 + B_1 Cos\omega t + B_2 Cos2\omega t + B_3 Cos3\omega t + B_4 Cos4\omega t$ .....

Then $i_{sink}\ (\omega t) = i_{source}(\omega t + \pi) = I_C + B_0 - B_1 Cos\omega t + B_2 Cos2\omega t - B_3 Cos3\omega t + B_4 Cos4\omega t$ -.....

Now net output current through the load = $i_{out}\ (\omega t) = i_{source}\ (\omega t) - i_{sink}\ (\omega t)$

Therefore $i_{out}\ (\omega t) = 2(B_1 Cos\omega t + B_3 Cos3\omega t + B_5 Cos5\omega t$ -.....)

Hence overall harmonic distortion is suppressed automatically in Class B complimentary symmetry amplifier. Therefore signal fidelity is maintained inspite of large signal power amplification.

TRANSFORMER COUPLED CLASS AB PUSH PULL AMPLIFIER

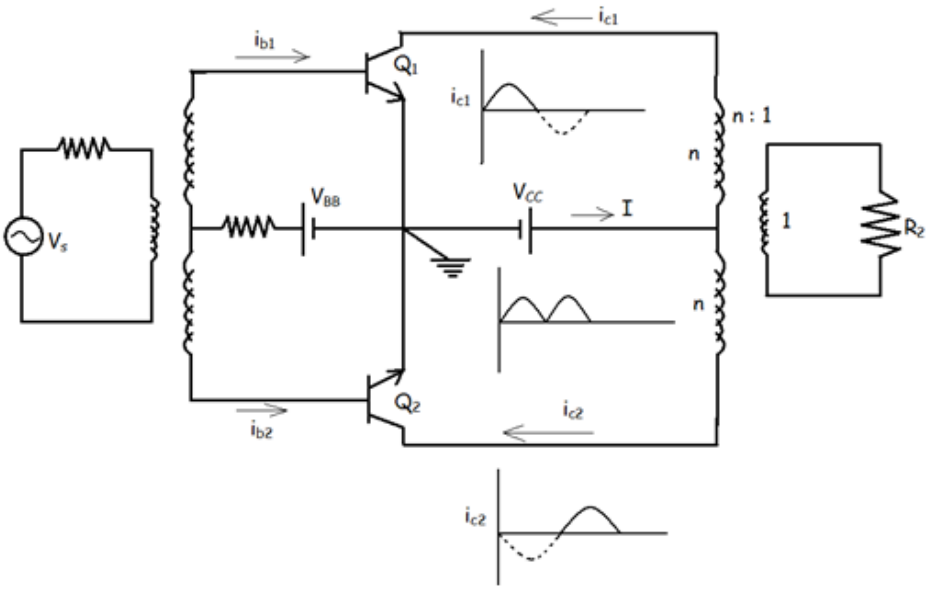


Figure 8. Physical operation of Class B push-pull amplifier.

Figure 36.25

Figure 8. Circuit Diagram of Transformer Coupled Class B Push-Pull Amplifier.

Below in Figure 9, the graphical interpretation of Class B Push-Pull Amplifier is given. The battery V_{CC} in the output loop of the Class B amplifier supplies a full wave rectified current - one half is being supplied to Q_1 and the other half is supplied to Q_2. The two half together result in a full sine wave in the secondary coil of the output transformer as shown in Figure 9B.

Figure 9A gives the load line of one half of the circuit.

Figure 9B gives the transfer characteristics.(input to output).

Figure 9C gives the resultant sine wave generated in the secondary loop of the output transformer

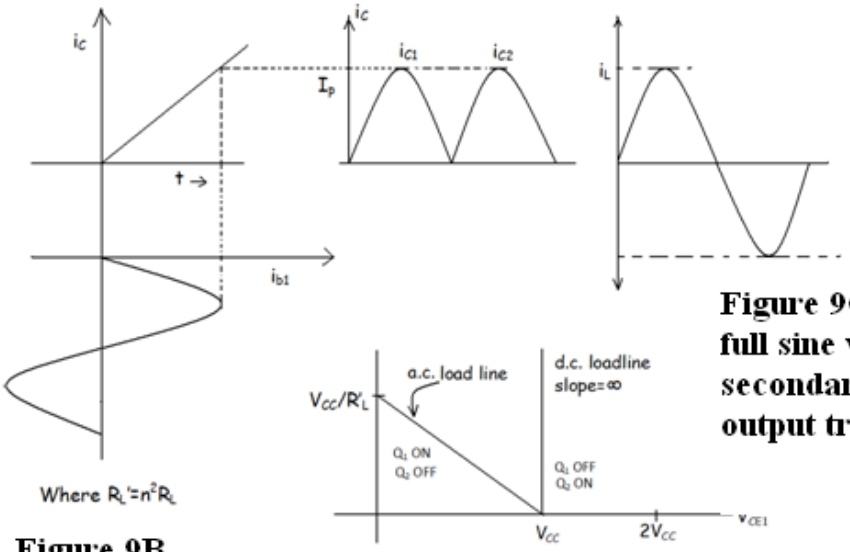


Figure 9B. Transfer Characteristics

Figure 9C. The resultant full sine wave in the secondary coil of the output transformer.

Figure 9A. The dc(static) and ac(dynamic load line) of one half of the circuit.

Figure 36.26

Figure 9. Load Line and Q-point swing under signal condition.
TRANSFOMER COUPLED CLASS A CE AMPLIFIER

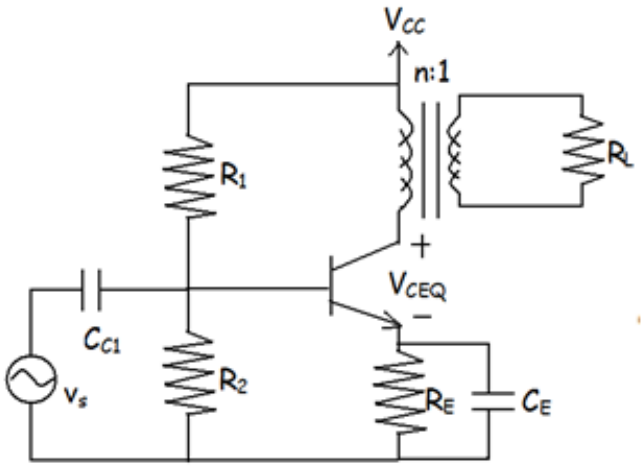
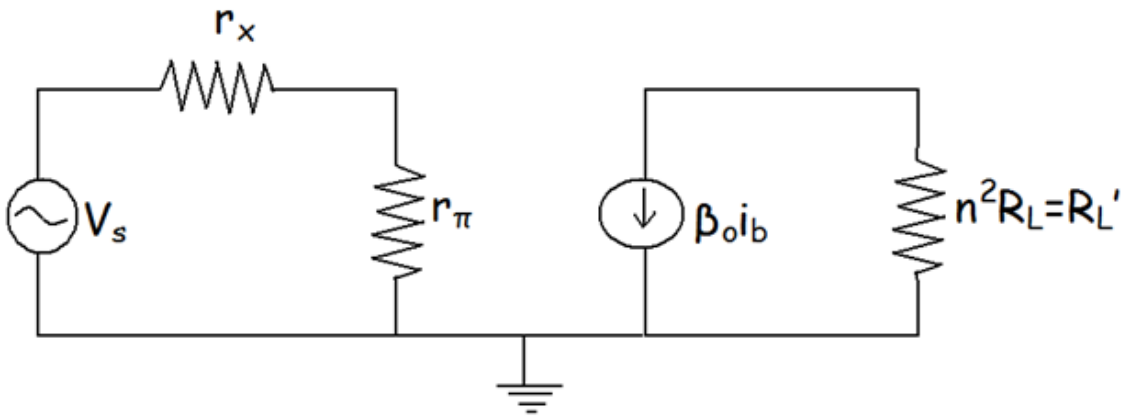


Figure 10. Transformer coupled Class A CE Amplifier.

Figure 36.27

Figure 10. Circuit Diagram of Class A transformer coupled CE Amplifier.



R_L' is the effective load as seen on the primary side of transformer.

Figure 11. Incremental circuit of Transformer coupled CE Amplifier. DC load is zero but AC load is R_L'

Figure 36.28

Figure 11. Incremental Circuit of transformer coupled CE amplifier. The load is reflected as n^2R_L. Under no load condition there is no collector dissipation.

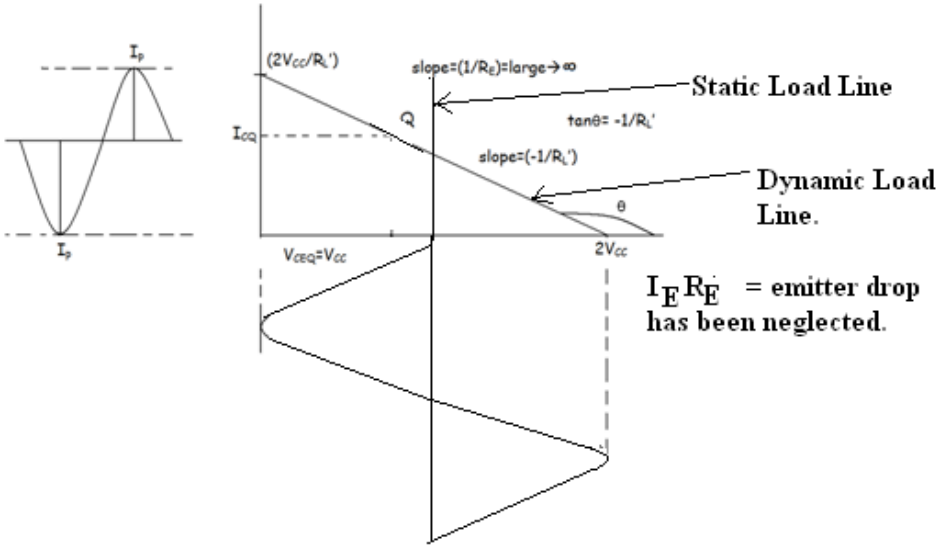


Figure 12. Graphical working of Transformer coupled CE Amplifier CE Amplifier sees zero dc load but R_L' ac load.

Figure 36.29

$$I_{av}\ from\ the\ battery = I_{CQ} = \frac{1}{2}\left(\frac{2V_{CC}}{R_L'}\right) = \left(\frac{V_{CC}}{R_L'}\right)$$

Figure 36.30

$$\therefore\ Power\ from\ the\ battery = I_{CQ} \times V_{CC} = \left(\frac{V_{CC}^2}{R_L'}\right) = P_{Total}$$

Figure 36.31

$$power\ delivere\ to\ the\ load = \left(\frac{I_{peak}}{\sqrt{2}}\right)^2 R_L^{'}$$

Figure 36.32

Where

$$I_{peak} = \left(\frac{V_{CC}}{R_L^{'}}\right)$$

Figure 36.33

$$\therefore P_{load} = \left(\frac{V_{CC}}{R_L^{'}}\right)^2 \times \frac{1}{2} R_L^{'} = \frac{V_{CC}^2}{2R^{'}_L}$$

Figure 36.34

$$\therefore \eta = \frac{P_{load}}{P_{Total}} = \frac{\frac{V_{CC}^2}{2R^{'}_L}}{\frac{V_{CC}^2}{R^{'}_L}} = \frac{1}{2} = 0.5$$

Figure 36.35

$$Standby\ Power = Power\ dissipated\ across\ BJT = I_{av}V_{CEQ} = \frac{V_{CC}^2}{R_L^{'}}$$

Figure 36.36

During signal condition half of this power is delivered to the load and half power is dissipated in BJT.

The considerable improvement in Power Conversion Efficiency is due the fact that under no signal condition dc load is zero hence there is no standby power dissipation in the load circuit though there is power dissipation in the active device. Due to this the efficiency rises from 25% to 50%.

In direct coupled CE Amplifier, the power conversion efficiency is 25%. This has not been dealt with. We analyzed the capacitive coupled Load in CC Amplifier . In this case also power conversion efficiency is 25%.

Class C tuned amplifier give more than 99% power conversion efficiency. This we will deal in RF tuned amplifier.

Chapter 37

AE_Lecture10_Supplementary[1]

AE_Lecture10_SupplementaryNotes.

Class A Direct Coupled Resistive Load Power Analysis.

Here we are analyzing Class A_ CE Amplifier with resistive load connected as R_C .

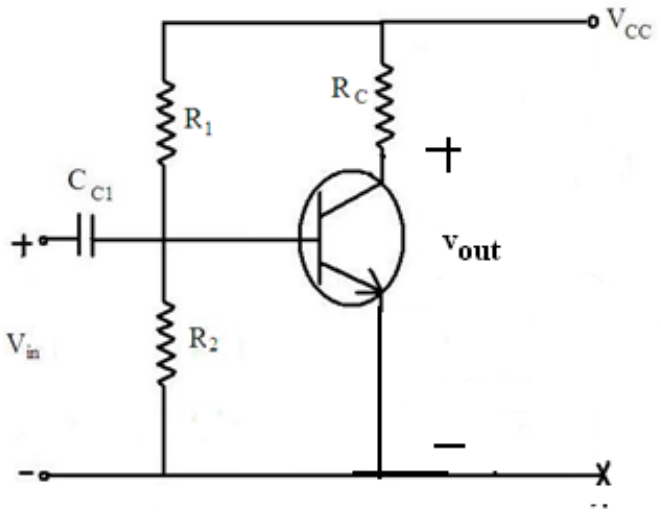


Figure 1. Class A CE Amplifier with resistive load connected as R_C

Figure 37.1

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[1] This content is available online at <http://cnx.org/content/m32376/1.1/>.

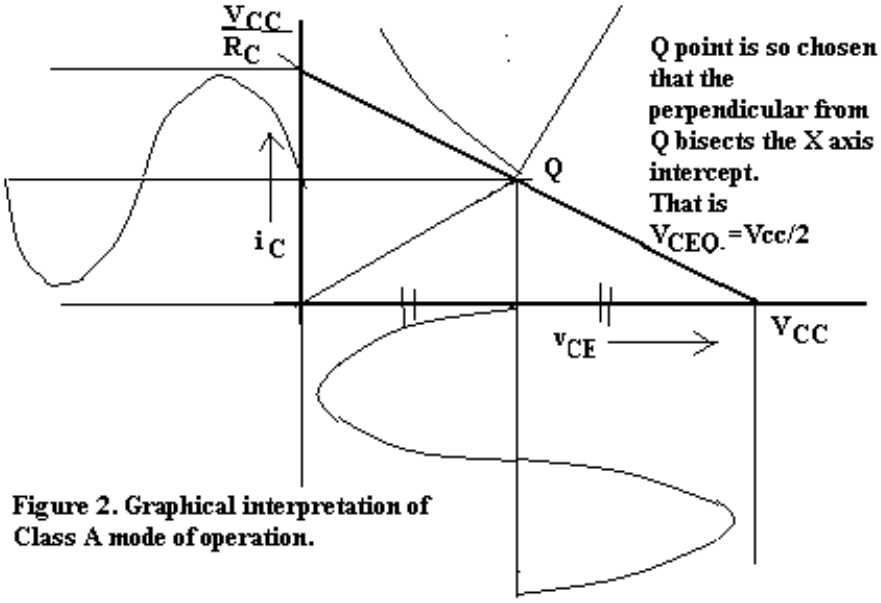

Figure 37.2

Under no signal condition:
The dc power drawn from the battery is = $P_{battery} = I_{CEQ}V_{CC}$
For maximum symmetrical swing, Q point is chosen to give :
$I_{CEQ} = V_{CC}/(2R_C)$ and $V_{CEQ} = V_{CC}/2$;
Therefore $P_{battery} = {V_{CC}}^2/(2R_C)$;
Power dissipated in the device = $P_{dissip} = I_{CEQ}V_{CEQ} = {V_{CC}}^2/(4\ R_C)$;
Power dissipated in the collector resistance = $P_{RC} = (I_{CEQ})^2.\ R_C = {V_{CC}}^2/(4\ R_C)$;
$P_{battery} = P_{dissip} + P_{RC}$;
This means power drawn from the battery is equally dissipated across the collector resistance and the device .
When maximum signal is applied at the input, we get maximum output signal.
It will be noticed in Figure 2 that when maximum current flows in BJT there is minimum voltage across BJT and when there is maximum voltage across BJT then there is minimum current through BJT. Both these situations minimize the device dissipation. The saved portion of device dissipation is converted into signal power.
The signal voltage across the load i.e. R_C is = $(V_{CC}/2)\mathrm{Sin}(\omega t)$
Therefore signal power developed across the load = ${Vrms}^2/R_C$;
Vrms = (amplitude of the sinusoidal voltage swing) = $(V_{CC}/2)/\sqrt{2}$;
Signal Power = $P_{signal} = {Vrms}^2/R_C = ((V_{CC}/2)/\sqrt{2})^2/R_C = (V_{CC})^2/(8R_C)$;
Power Conversion of efficiency = $\eta = P_{signal}/\ P_{battery} = 2/8 = 1\ /\ 4 = 25\%$;
Class A Transformer Coupled Load.

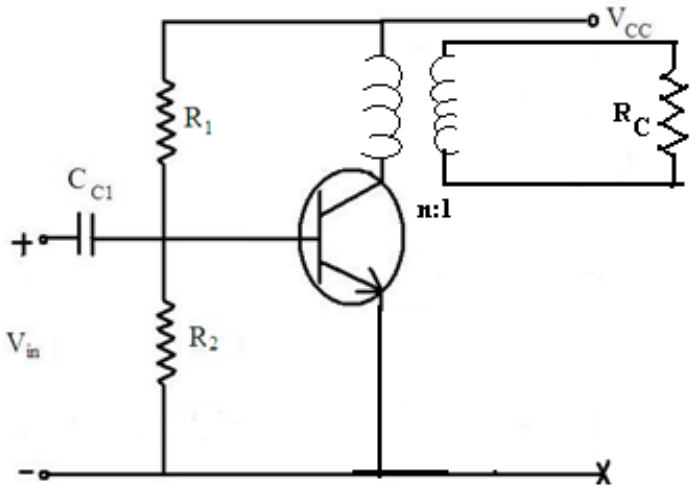

Figure 3. Class A CE Amplifier with transformer coupled resistive load R_C

Figure 37.3

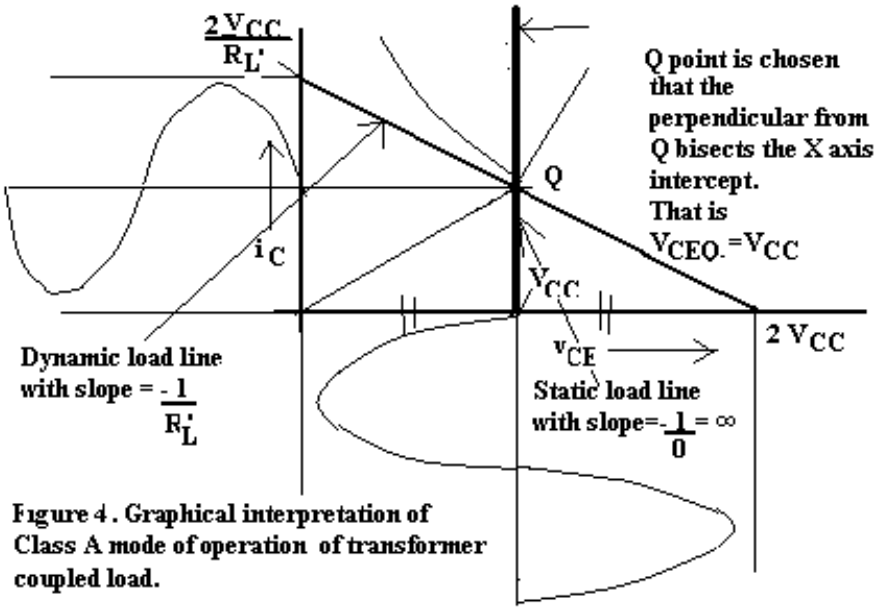

Figure 4. Graphical interpretation of Class A mode of operation of transformer coupled load.

Figure 37.4

Figure 4 gives the static and dynamic load line in case of ClassA CE transformer coupled resisitive load. Since transformer primary coil offers 0Ω under dc condition hence the static load line has a slope of = -1/0 = ∞. Therefore Static load line is a vertical line parallel to Y axis and cutting X axis at V_{CC}.

Q point is so chosen that we obtain maximum symmetrical swing. For this the vertical from Q must bisect the X axis intercept of the Dynamic Load Line.

Hence slope of OQ = negative slope of the dynamic load Line= $1/R_L$'

where R_L' = n^2 R_L and n= turns ratio of primary to secondary..

Therefore Q point is : $V_{CEQ} = V_{CC}$ and I_{CQ}= V_{CC}/ R_L' .

Under no signal condition the power drawn from the battery =

$P_{battery} = V_{CC} \times I_{CQ} = (V_{CC})^2 / R_L$'= this power is totally dissipated in the device. There is no resistive dissipation as the dc ohmic resistance is zero in collector circuit.

Signal Power delivered to the load as seen on the primary side is = $Vrms^2/R_L$' ;

But Vrms = amplitude of maximum sinusoidal swing/ $\sqrt{2}$;

As seen from the graph in Figure 4 the amplitude of maximum sinusoidal swing= V_{CC};

Hence P_{signal} = (Vrms= $V_{CC}/\sqrt{2}$)^2/R_L' = (V_{CC})^2/ (2R_L');

Therefore $\eta = 1/2 = 50\%$. Almost hundred percent improvement over the direct coupled load but still not permissible for Power Amplifiers.Here half of the device power dissipation under no signal condition is being transformed into signal power under signal condition. Thus we achieve 50% power conversion efficiency.

So we go for Class B mode of operation where we will achieve 80% power conversion efficiency.

In RF applications we will go for Class C mode of operation which will provide 99% power conversion efficiency.

Here the question arises why do we not go for Class C mode of operation in Audio Frequency Range.

This is because Class C suffers from very severe harmonic distortion which can be removed only by tuned circuits and tuned circuits are not practical at audio range.

Chapter 38

AE_Lecture11_Part1_Audio Oscillators[1]

AE_LECTURE 11_Part1.
Section 1. FEEDBACK SYSTEMS STABILITY AND OSCILLATORS

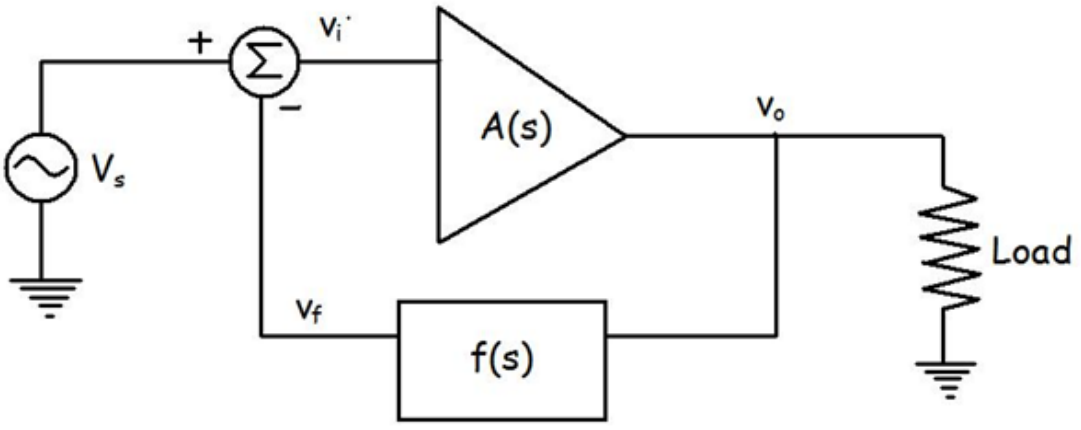

Figure 1. Block Diagram of a feed back system

Figure 38.1

Figure 1. Block Diagram of feedback system.

Here 's' implies s-domain and s=σ+jω. Just as we have time domain, we have frequency domain, s-domain and z-domain.

In Time-domain we study the response of a system with respect to time.

In Frequency-domain we study the steady state sinusoidal response of a system.

[1]This content is available online at <http://cnx.org/content/m32428/1.2/>.

In s-domain we get to see the total response of the system. Whenever a certain input is applied we have a transient response and steady state response. Total response is the sum total of transient plus steady state response.

z-domain is for discrete time systems and s-domain is for continuous time systems.

In the Block Diagram of a feedback system, we have the Basic Amplifier Block A(s) , the feedback network block f(s) and comparison node. f(s) can be frequency independent or frequency selective.

$$v_i = \left(v_s - v_f\right)$$

Figure 38.2

$$v_o(s) = A(s)v_i(s)$$

Figure 38.3

$$v_f(s) = f(s)v_o(s)$$

Figure 38.4

$$\therefore \frac{v_o(s)}{v_s(s)} = \frac{A(s)}{1 + A(s)f(s)} = \frac{A(s)}{1 - [-A(s)f(s)]}$$

Figure 38.5

$$A_{closed}(s) = \frac{A_{open}(s)}{1 - L(s)}$$

Figure 38.6

$$L(s) = Loop\ Gain = -A_{open}(s)f(s)$$

Figure 38.7

In negative feed back

$$L(s) = negative$$

Figure 38.8

In positive feed back

$$L(s) = positive$$

Figure 38.9

Negative feed back system is a degenerative system:

$$A_{closed} = \frac{A_{open}}{1 + |L(s)|}$$

Figure 38.10

And $A_{closed} < A_{open}$ Hence a degenerate system.

Positive feedback system is a regenerative system:
$A_{closed} = A_{open}/[1- |L(s)|]$
If

$$|L(s)| < 1$$

Figure 38.11

then

$$A_{closed} > A_{open}$$

Figure 38.12

Hence regenerative system

$$If\ |L(s)| \geq 1$$

Figure 38.13

then

$$A_{closed} \rightarrow \infty$$

Figure 38.14

and system becomes unstable and oscillatory.
We can take advantage of instability and realize a pure sine wave oscillator.
When

$$L(s) = -A(s)f(s) = 1\angle 0^{\circ}$$

Figure 38.15

. This is BARKHAUSEN CRITERIA.
Then we realize a pure sine wave oscillator.

For self starting condition we allow

$$L(s) = -A(s)f(s)$$

Figure 38.16

to be slightly greater than

$$1\angle 0^{\circ}$$

Figure 38.17

.This will ensure self starting condition but it will cause a slight distortion.

Section 2. Class of audio oscillators(1 Hz → 100kHz)

Wien Bridge Oscillator, Phase-Shift Oscillator and Quadrature Oscillator.

2.1. Wien Bridge Oscillator.

Here Op.Amp is connected as an Non-inverting amplifier with a gain of 3/_0º. The feedback network is a notch filter providing a dip of exactly 1/3 and phase angle 0º at an angular frequency of

$$\omega_0 =$$

Figure 38.18

$$\frac{1}{R_0 C_0}$$

Figure 38.19

. Thus an exact loop gain of unity with 0º phase shift is achieved. But for selfstarting condition the non-inverting gain is kept slightly larger than 3.

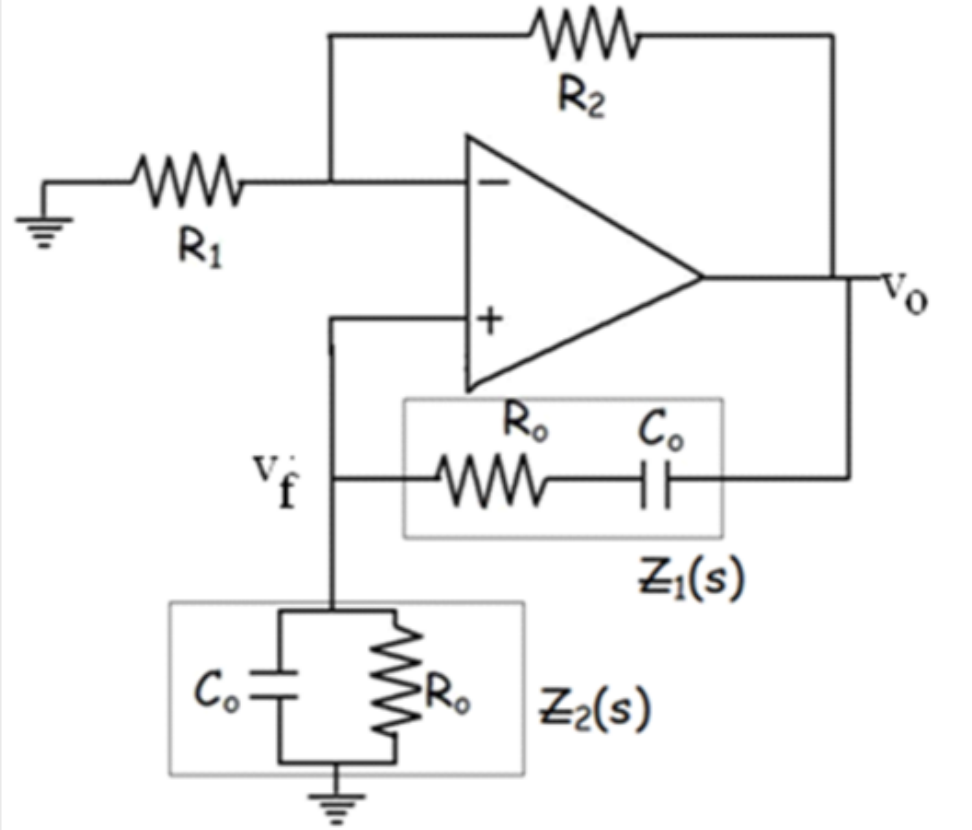

Figure 2. Wien Bridge Oscillator.

Figure 38.20

Figure 2. Circuit Diagram of Wien Bridge Oscillator.

$$\frac{v_f}{v_o} = \frac{Z_2(s)}{Z_1(s) + Z_2(s)} = \frac{\frac{\left[R_o\left(\frac{1}{sC_o}\right)\right]}{\left(R_o + \frac{1}{sC_o}\right)}}{\left(R_o + \frac{1}{sC_o}\right) + \frac{\left\{R_o\left(\frac{1}{sC_o}\right)\right\}}{\left(R_o + \frac{1}{sC_o}\right)}}$$

Figure 38.21

$$= \frac{\frac{R_o}{1 + sR_oC_o}}{\frac{(1 + sR_oC_o)}{sC_o} + \frac{R_o}{(1 + sR_oC_o)}}$$

Figure 38.22

$$= \frac{sR_oC_o}{sR_oC_o + (1 + sR_oC_o)^2}$$

Figure 38.23

$$= \frac{sR_oC_o}{sR_oC_o + 1 + s^2{R_o}^2{C_o}^2 + 2sR_oC_o}$$

Figure 38.24

$$\frac{v_f(s)}{v_o} = \frac{sR_oC_o}{s^2{R_o}^2{C_o}^2 + 3sR_oC_o + 1}$$

Figure 38.25

Replacing s by jω,

$$\frac{v_f(s)}{v_o(s)} = \frac{j\omega_oR_oC_o}{\left(1 - \omega_o{}^2{R_o}^2{C_o}^2\right) + 3j\omega_oR_oC_o}$$

Figure 38.26

At

$$\omega_o = \frac{1}{\omega_oR_o}; \left(1 - \omega_o{}^2{R_o}^2{C_o}^2\right) = 0$$

Figure 38.27

$$\frac{v_f(j\omega)}{v_o} = \frac{1}{3}\angle 0^\circ$$

Figure 38.28

$$\therefore if\ \frac{v_o}{v_f} = 3 = \left(1 + \frac{R_2}{R_1}\right)$$

Figure 38.29

Then Loop Gain=

$$1\angle 0^{\circ}$$

Figure 38.30

Oscillation Frequency=

$$\omega_o = \frac{1}{R_o C_o}$$

Figure 38.31

$$\frac{R_2}{R_1} = 2$$

Figure 38.32

; This gives a non-inverting gain of 3.
2.2. RC PHASE SHIFT OSCILLATOR

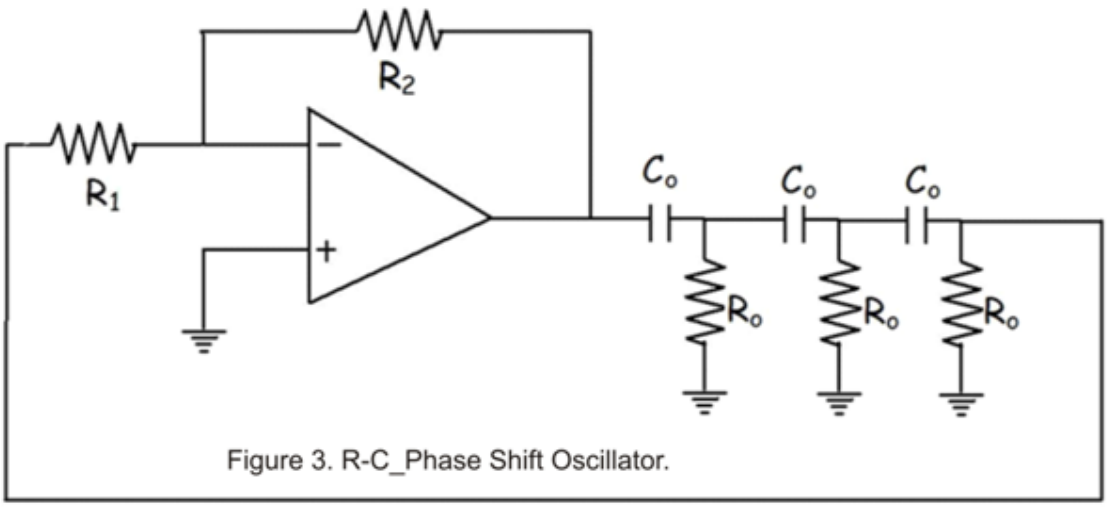

Figure 38.33

Figure 3. Circuit Diagram of RC phase shift oscillator.

Here Op Amp is connected as an inverting amplifier providing a gain of 29 and phase shift of 180^o.

The RC phase shift network gives an attenuation of 1/29 and a phase shift of another 180^o.

Thus an exact Loop Gain of $1/\_0^o$ is achieved. But for self starting condition the inverting gain is kept slightly larger than 29.

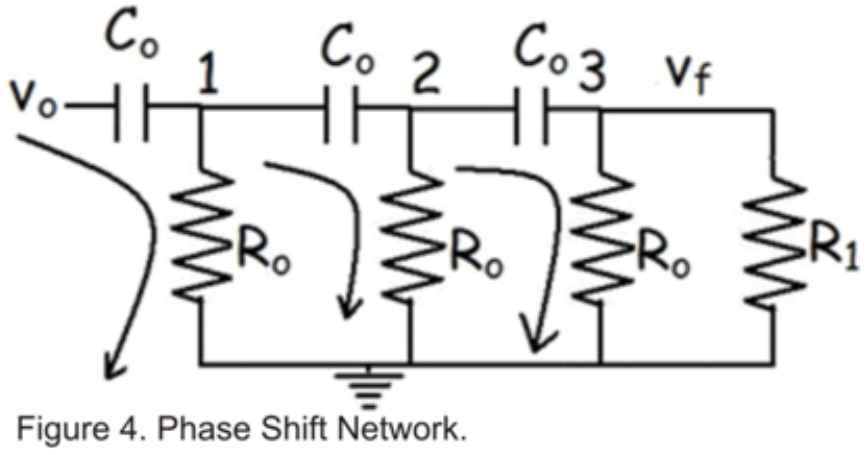

Figure 38.34

Figure 4. The feed back network.
The Loop Gain expression is:
L(jω) =

$$\frac{R_2}{R_1} \times \frac{j\omega^3}{Re\Delta + jIm\Delta}$$

Figure 38.35

where Δ =

$$\frac{(s_0+2j\omega)^2(s_0+j\omega)}{(j\omega)^2(j\omega)} - \frac{(2s_0+3j\omega)}{j\omega}$$

Figure 38.36

and

$$s_0$$

Figure 38.37

=

$$\frac{1}{R_0C_0}$$

Figure 38.38

;
Re(Δ) =

$$s_0^3 - 8\omega^2 s_0 + 2s_0\omega^2$$

Figure 38.39

Im(Δ)=

$$\omega(5s_0^2 - \omega^2)$$

Figure 38.40

To satisfy the Barkhausen Criteria, Re(Δ) = 0;
But ReΔ=

$$s_0^3 - 8\omega^2 s_0 + 2s_0\omega^2 = 0$$

Figure 38.41

Therefore by cancelling

$$s_0$$

Figure 38.42

through out, we get

$$s_0^2 = 6\omega^2$$

Figure 38.43

Therefore

$$\omega_{osc} = \frac{s_0}{\sqrt{6}}$$

Figure 38.44

=

$$\frac{1}{\sqrt{6}R_0C_0}$$

Figure 38.45

;
Second part of the Barkhausen Criteria says that at oscillatory frequency the phase angle should be zero.
L(ω=

$$\frac{s_0}{\sqrt{6}}$$

Figure 38.46

) =

$$\frac{R_2}{R_1} \times \frac{j(s_0/\sqrt{6})^3}{\omega_{osc}(5s_0^2 - \omega_{osc}{}^2)}$$

Figure 38.47

=

$$\frac{R_2}{R_1} \times \frac{j(s_0/\sqrt{6})^2}{(5s_0^2 - s_0^2/6)}$$

Figure 38.48

=

$$\frac{R_2}{R_1}\left(\frac{s_0^2/6}{29s_0^2/6}\right.$$

Figure 38.49

)

L(ω=

$$\frac{s_0}{\sqrt{6}}$$

Figure 38.50

) =

$$\frac{R_2}{R_1}\left(\frac{1}{29}\right.$$

Figure 38.51

) = 1 ;
Therefore

$$\frac{R_2}{R_1} = 29;$$

Figure 38.52

Chapter 39

AE_Lecture11_Part2_Radio-Frequency Oscillators[1]

AE_LECTURE 11_Part2.

Part 2 deals with RF Oscillators.

Section 1. Class of RF OSCILLATORS

(100kHz- 1000kHz:Medium Wave RF & 1MHz-30MHz:Short Wave RF;
30MHz-70MHz: Amateur Band for HAM Radio practitioners;
70MHz-300MHz: Very High Frequency (VHF) Band for FM and TV transmissions;
300MHz-800MHz: Ultra High Frequency(UHF) Band for Police Communication;
1GHz-100GHz: Microwaves for satellite communication;
Terra Hz(0.4μm-100μm): Optical Fiber Communication)
LC oscillators are RF oscillators.

[1] This content is available online at <http://cnx.org/content/m32429/1.1/>.

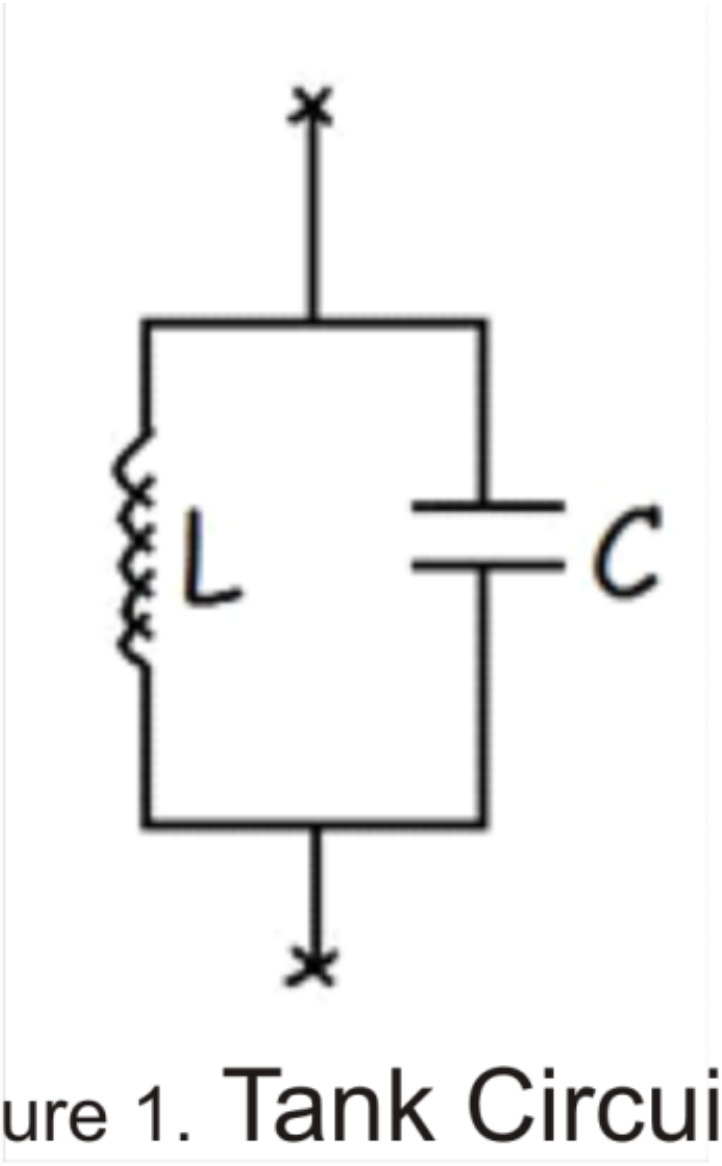

Figure 1. Tank Circuit

Figure 39.1

Figure 1. Parallel Resonance Circuit or Tank Circuit.

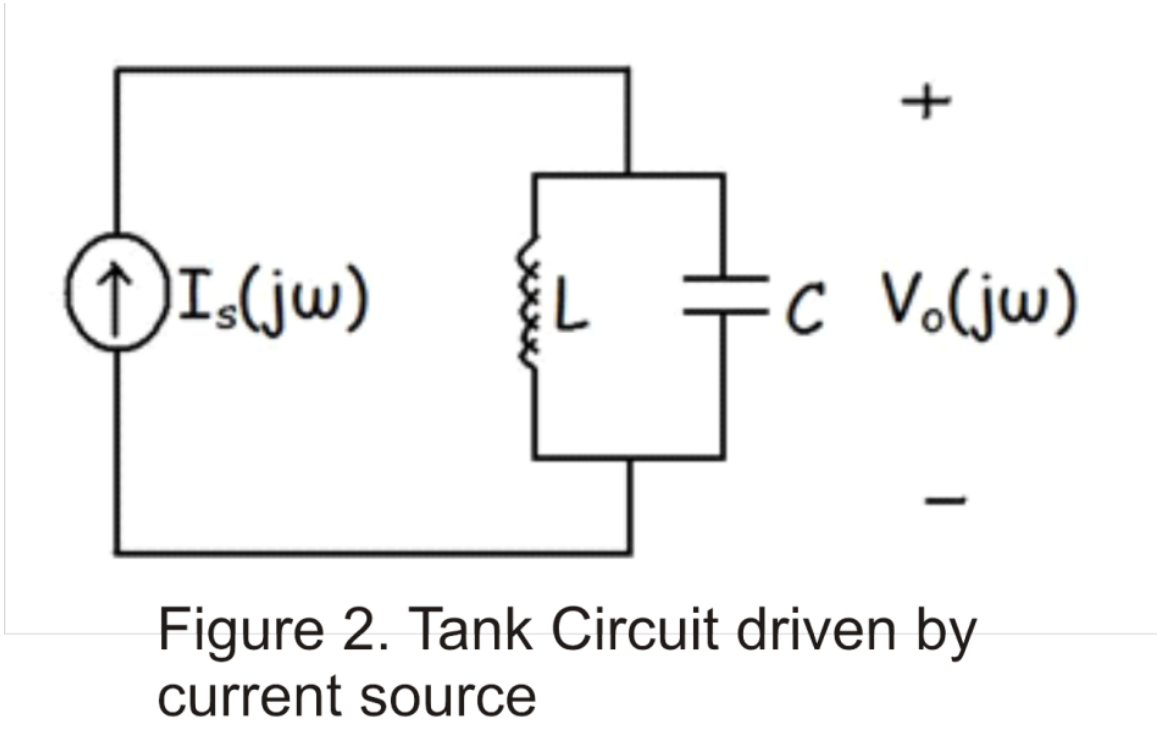

Figure 39.2

Figure 2. Circuit Diagram of a Tank Circuit driven by a constant current source.
Parallel resonance circuit is known as tank Circuit.
Resonance frequency=ω_o=

$$\frac{1}{\sqrt{LC}}$$

Figure 39.3

$$V_o(j\omega) = I_s(j\omega)Z_{tank}(j\omega)$$

Figure 39.4

$$Z_{tank}(j\omega) = \frac{1}{\left[\frac{1}{j\omega} + j\omega\right]} = \frac{j\omega}{(1-\omega^2 LC)} = \frac{j\omega L}{LC\left(\frac{1}{LC} - \omega^2\right)}$$

Figure 39.5

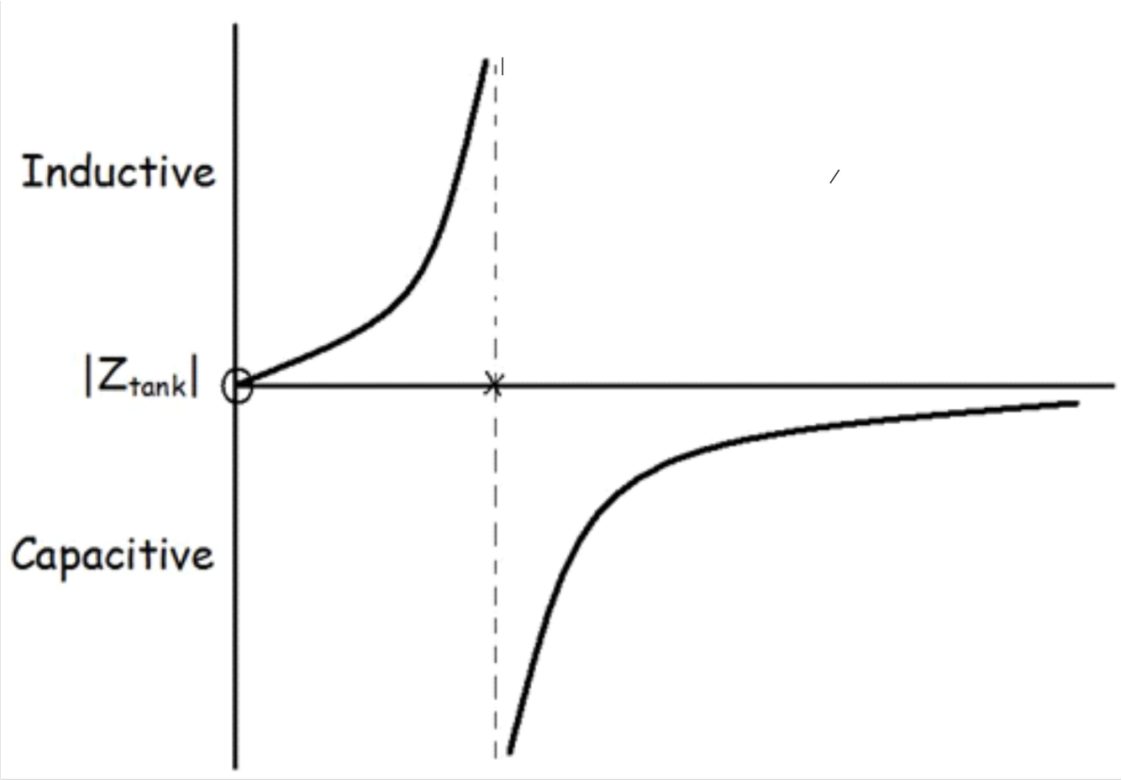

Figure 3. PoleZero Pattern of Tank Circuit

Figure 39.6

Figure 3. Magnitude of the reactance of a tank circuit vs frequency.

$$Z_{tank} = \frac{j\omega}{C(\omega_o^2 - \omega^2)}$$

Figure 39.7

At $\omega =$

$$\frac{1}{\sqrt{LC}}$$

Figure 39.8

;

$$Z_{tank}(j\omega_o) = \infty$$

Figure 39.9

$$At\ \omega < 1/\sqrt{LC}$$

Figure 39.10

$$Z_{tank} = +\ reactance. Hence\ Inductive$$

Figure 39.11

$$At\ \omega > 1/\sqrt{LC}$$

Figure 39.12

$$\angle Z_{tank} = -\ reactance\ .Hence\ Capacitive$$

Figure 39.13

When quality factor Q of the tank circuit $=\infty$, the circuit is purely reactive and there is no dissipation.

When quality factor Q is finite say 1000 then an equivalent R_P comes in parallel with the tank circuit. R_P accounts for the losses

$$Q = R_p/\omega_o L$$

Figure 39.14

For a finite quality factor tank circuit, the effective impedance is a pure resistance R_P at resonance frequency.

Hence

$$Z_{tank}(j\omega_o) = R_p$$

Figure 39.15

Frequency response of the tank circuit is :

$$V_{out}(j\omega_o) = I_s(j\omega_o)R_p$$

Figure 39.16

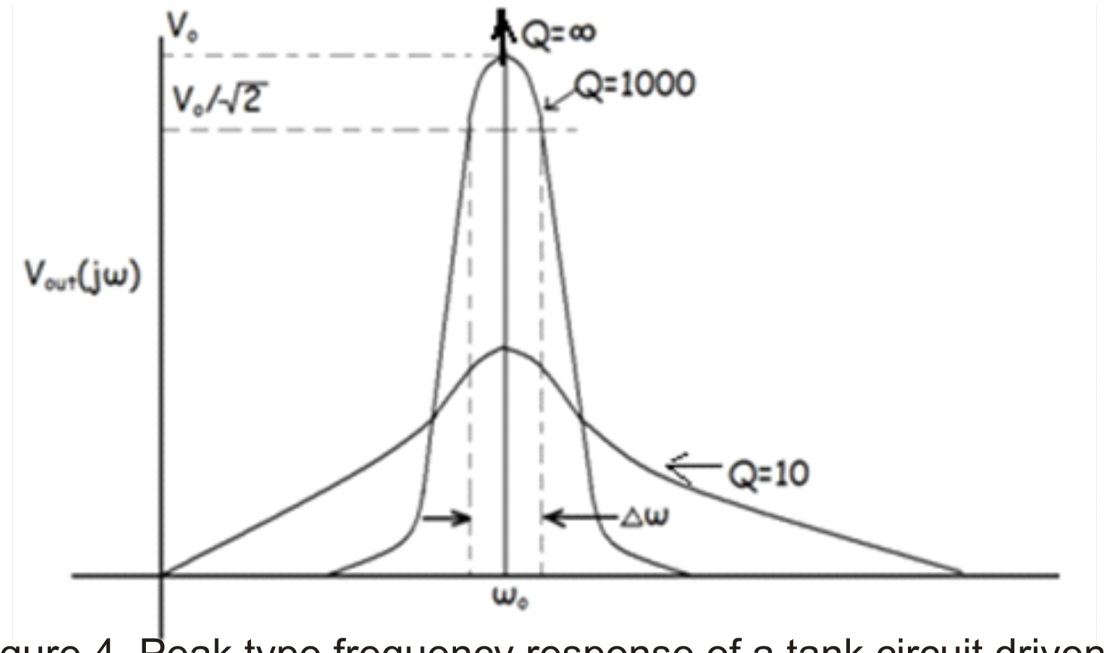

Figure 4. Peak type frequency response of a tank circuit driven by a current source.

Figure 39.17

Figure4. The peak response of a tank circuit for various quality factors.

$$\Delta\omega = Band\ Width$$

Figure 39.18

$$Q = \frac{\omega_o}{\Delta\omega}$$

Figure 39.19

At Q=∞, spike response.
At Q=finite, peak response.
As Q falls, sharpness of the peak response is lost.
Section 1.1. GENERALIZED LC OSCILLATOR.

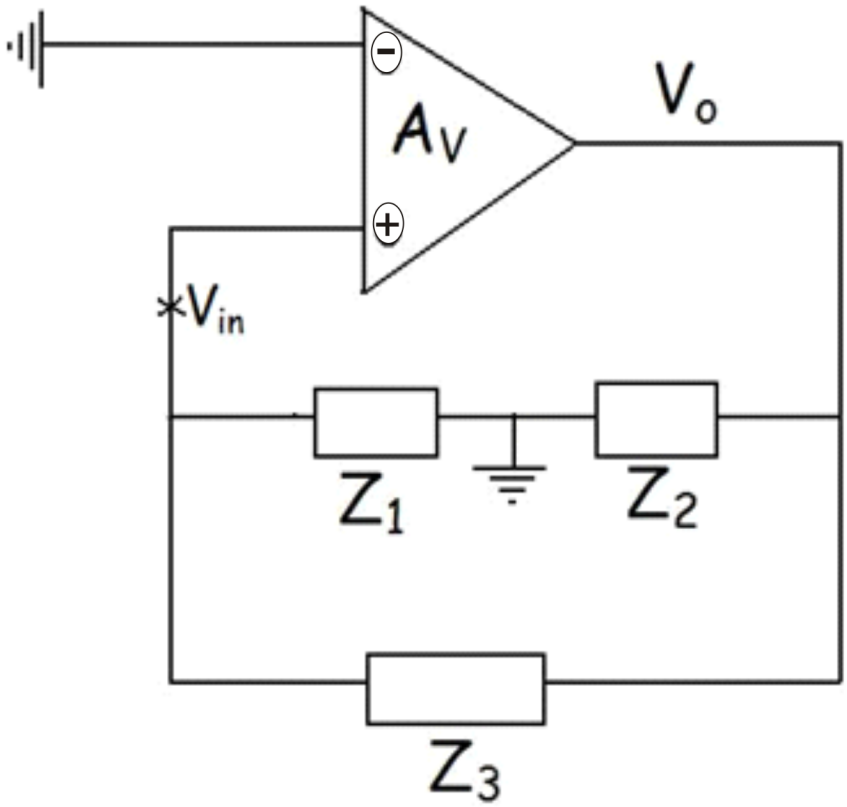

Figure 5. Generalized Configuration of RF Oscillator using an Op Amp.

Figure 39.20

Figure 5. Block Diagram of generalized LC Oscillator

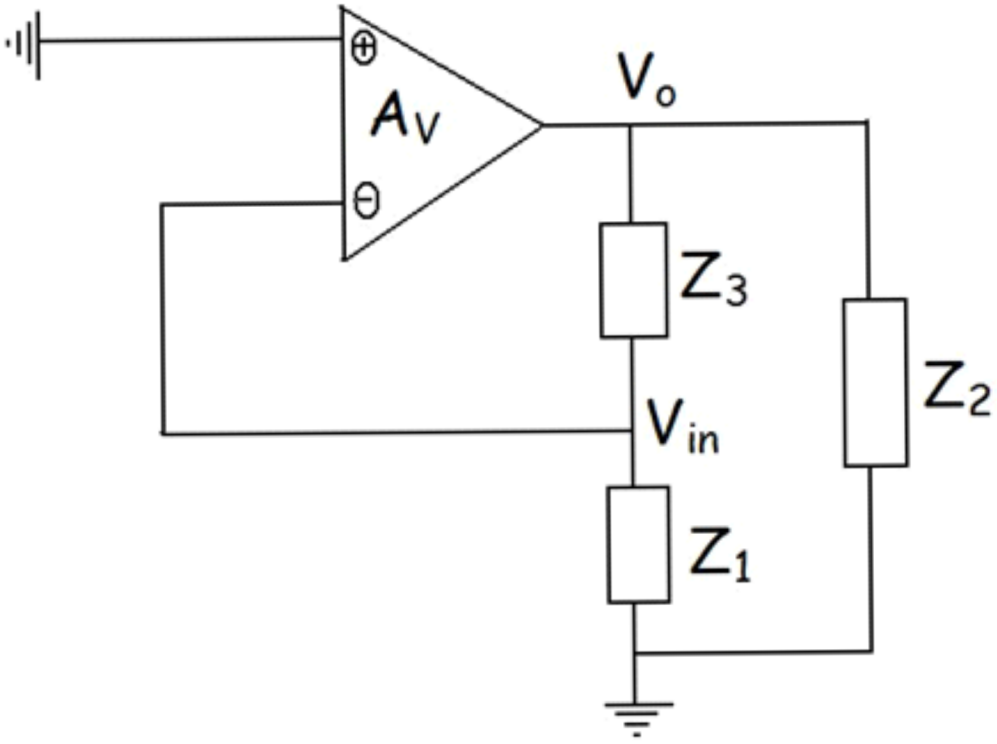

Figure 6. Reorientation of the generalized configuration to visualize the feedback

Figure 39.21

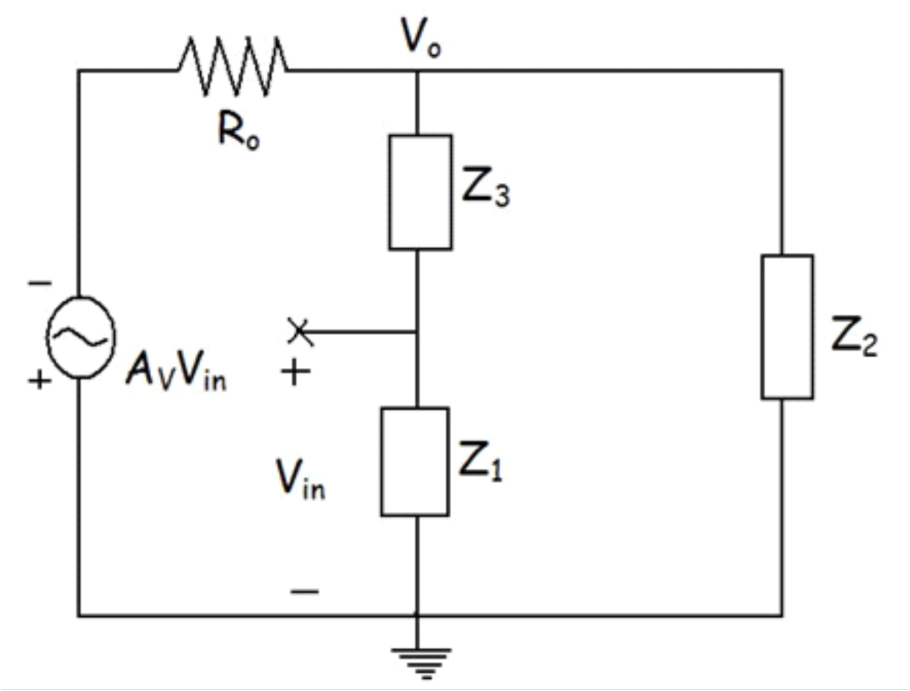

Figure 7. The incremental circuit of the generalized oscillator.

Figure 39.22

$$v_o = \frac{-A_V v_{in}(Z_L)}{(R_o + Z_L)}$$

Figure 39.23

Where

$$Z_L = Z_2 || (Z_1 + Z_3)$$

Figure 39.24

Therefore:

$$v_{in} = \frac{-v_o(R_o + Z_L)}{(A_V Z_L)} \text{ - - - - - - - - - - - - (1)}$$

Figure 39.25

Examining the feedback network in Figure 8:
Feed back voltage

$$v_f = \frac{v_o \times Z_1}{Z_1 + Z_3} \text{ _____ (2)}$$

Figure 39.26

If loop gain=1 [U+221F] 0 °

$$v_{in} = v_f$$

Figure 39.27

$$\therefore \frac{-v_o(R_o + Z_L)}{(A_V Z_L)} = \left(\frac{v_o \times Z_1}{Z_1 + Z_3}\right)$$

Figure 39.28

$$\frac{-\left[R_o + \frac{(Z_2)(Z_1+Z_3)}{(Z_1+Z_3+Z_2)}\right]}{A_V \frac{(Z_2)(Z_1+Z_3)}{(Z_1+Z_3+Z_2)}} = \frac{Z_1}{Z_1+Z_3}$$

Figure 39.29

$$or\ \frac{-[R_o(Z_1+Z_3+Z_2)+(Z_2)(Z_1+Z_3)]}{(A_V)(Z_2)\cancel{(Z_1+Z_3)}} = \frac{Z_1}{\cancel{Z_1+Z_3}}$$

Figure 39.30

$$or\ 1 = \frac{-Z_1 Z_2 A_V}{[R_o(Z_1+Z_3+Z_2)+(Z_2)(Z_1+Z_3)]} - - - - - - - - - - -(3)$$

Figure 39.31

This identity can be true only if

$$(Z_1+Z_2+Z_3) = 0 \_\_\_\_\_(4)$$

Figure 39.32

$$\&(Z_1 + Z_3) = -Z_2 \_\_\_\_\_ (5)$$

Figure 39.33

Subs(4) & (5) in (3)

$$1 = \frac{-Z_1 \cancel{Z_2} A_V}{(\cancel{Z_2})(Z_1 + Z_3)} = \frac{(-Z_1)A_V}{-Z_2}$$

Figure 39.34

$$\therefore 1 = \frac{Z_1}{Z_2} A_V$$

Figure 39.35

Starting condition is

$$\left(\frac{Z_1}{Z_2} A_V\right) > 1$$

Figure 39.36

This means

$$\boldsymbol{Z_1 \text{ and } Z_2}$$

Figure 39.37

are same kind of reactance and

Figure 39.38

is of opposite kind of reactance.
Table 1. Different possible configurations of a generalized LC Oscillator.

	Z 1	**Z 2**	**Z 3**	Type of Oscillator
1	L	L	C	Hartley Oscillator
2	C	C	L	Colpitts Oscillator

Table 39.1

Chapter 40

AE_Lecture11_Part3_Radio-Frequency Oscillators Continued[1]

Section 1.2. Colpitts Oscillator Using Op-Amp

Theoretical Analytical results have been taken from"Microelectronic Circuits_Analysis & Design" by Rashid, Publisher Thomson(Indian Edition),1999.Chapter 14_Power Amplifiers.

[1]This content is available online at <http://cnx.org/content/m32430/1.2/>.

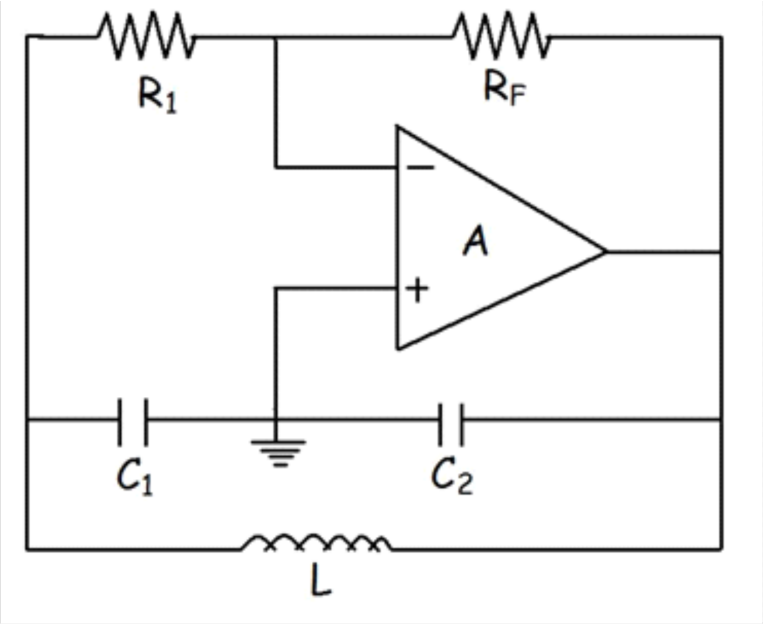

Figure 8. Colpitts Oscillator based on Op.Amp.

Figure 40.1

Figure 8. Circuit Diagram of Colpitts Oscillator.
The frequency of oscillation:

$$\omega_o = \frac{1}{\sqrt{L\left(\frac{C_1 C_2}{C_1 + C_2}\right)}}$$

Figure 40.2

The Barkhausen Criteria is satisfied by the following ratio:
gmR1=C2/C1+(C1/C2)(R1/RL)+(L/(C2RL^2))+L/(C1R1RL)
For large values of RL: gmR1=C2/C1 and gm=Aopen/RL

But magnitude of Aopen = magnitude of the voltage gain of the Basic Amplifier in Figure 8. The basic amplifier is an inverting amplifier hence /Aopen/= RF/R1

Therefore gmR1=(Aopen/RL)R1=(RF/R1)*(R1/RL)=RF/RL=C2/C1;

Therefore when RL is large then we must satisfy the condition:RF/RL = C2/C1

A typical Colpitts oscillator with fosc at 150kHz will have the component values as follows:

R1 = 100kohm, RF= 1000kohm, RL = 100kohm,C1=0.01uF,C2=0.1uF,L=124uH

Section 1.2.1.Colpitt's oscillator Using BJT

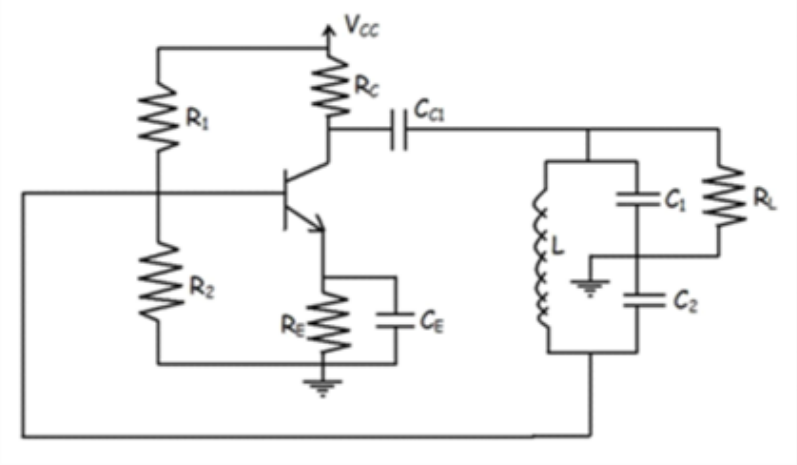

Figure 9. Colpitt's configuration using BJT.

Figure 40.3

Figure 9.Circuit Diagram of Colpitts Oscillator using BJT.

Section 1.3.1. Hartley Oscillator Using Op-Amp

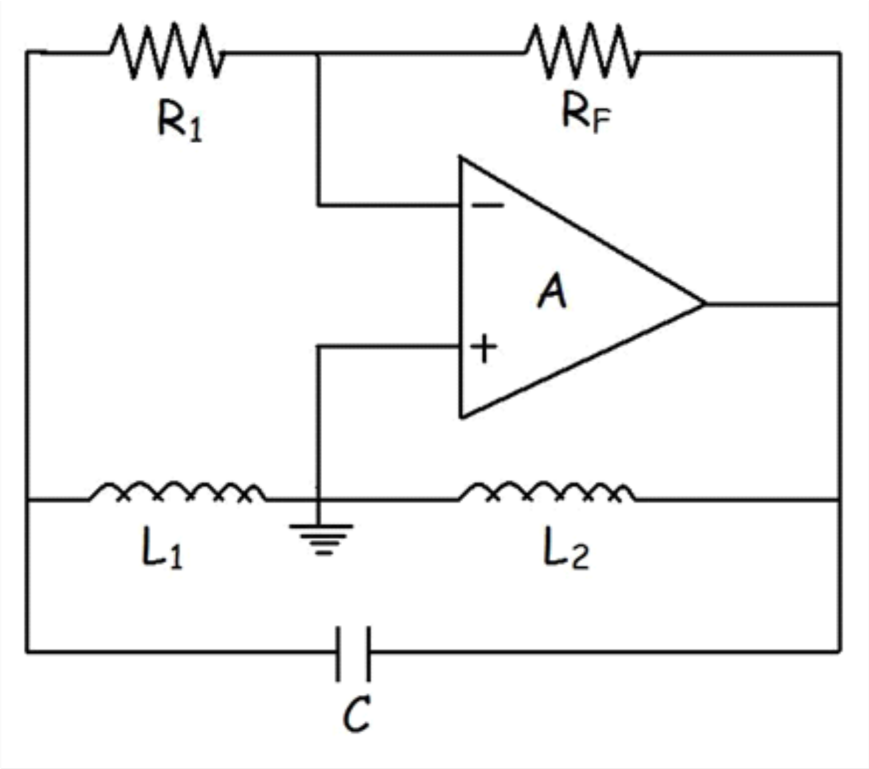

Figure 10. Hartley Oscillator based on Op Amp.

Figure 40.4

Figure 10. Circuit Diagram of Hartley Oscillator using Op.Amp.
For oscillation:
gmR1 = (L1/L2)+(R1.L2)/(RL.L1)
For large values of R_L,
gm.R1 = L1/L2
But gm = Aopen/RL and /Aopen/ = RF/R1
Therefore gmR1=RF/RL =(L1/L2)+(R1.L2)/(RL.L1)
Typical device parameters of a Hartley Oscillator with fosc = 33kHz are:
R1=100kohms, RF = 1Mohms, RL = 900kohms, L1=L2=125uH, C = 0.1uF.

$$\omega_o = \frac{1}{\sqrt{(C)(L_1 + L_2)}}$$

Figure 40.5

Section 1.3.2. HARTLEY OSCILLATOR USING JFET

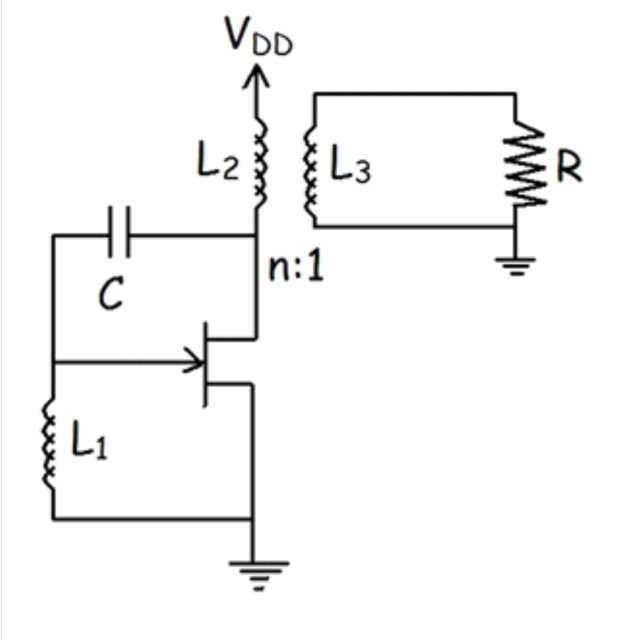

Figure 11. Hartley Oscillator using JFET.

Figure 40.6

Figure 11. Circuit Diagram of Hartley Oscillator using JFET.

$$\omega_o = \frac{1}{\sqrt{C(L_1 + L_2)}}$$

Figure 40.7

Here

$$g_m = \frac{L_2}{L_1 R_L} \because R_1 = \infty$$

Figure 40.8

$$R_L = n^2 R$$

Figure 40.9

$$L_2 = n^2 L_3$$

Figure 40.10

Section 1.4. TUNED OSCILLATOR

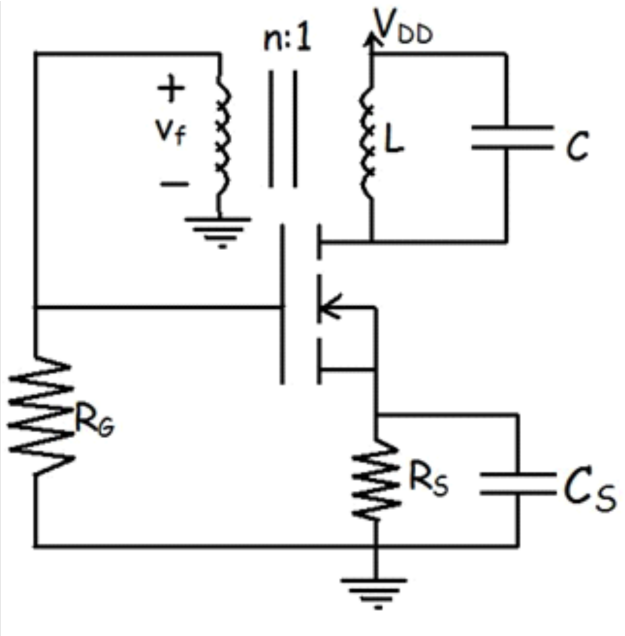

Figure 12. Tuned Oscillator

Figure 40.11

Figure 12. Circuit diagram of a tuned oscillator.

$$\omega_o = \frac{1}{\sqrt{LC}}$$

Figure 40.12

$$R_1 = r_d || \frac{R_G}{n^2}$$

Figure 40.13

$$g_m R_1 = 1$$

Figure 40.14

Section 2. CRYSTAL OSCILLATOR

In Colpitts oscillator, inductor is replaced by a crystal.

Quartz crystal is preferred due to the stability and accuracy.

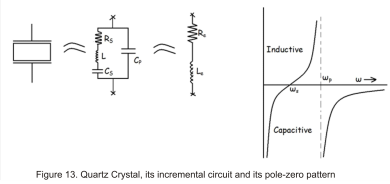

Figure 13. Quartz Crystal, its incremental circuit and its pole-zero pattern

Figure 40.15

Figure 13. The symbol of a quartz crystal, the equivalent circuit, pole-zero pattern of a crystal resonance circuit.

Q(of series resistance)=

$$\left(\frac{\omega_0 L}{R_s}\right)$$

Figure 40.16

Q(Of Tank Circuit)=

$$\left(\frac{R_p}{\omega_o L}\right)$$

Figure 40.17

Mass of the crystal gives rise to L_s
Elasticity of the crystals gives rise to C_s.
Damping force gives rise to R_s.
L_S, C_S and R_S comprises the intrinsic series resonance path through the crystal.
Table 2. COMMON CUTS OF QUARTZ CRYSTAL(RCA Corp.)

Frequency	32kHz	280kHz	525kHz	2MHz	10MHz
Cut	XY Bar	DT	DT	AT	AT
R_s	40KΩ	1820Ω	1400Ω	82Ω	5Ω
L	4800H	25.9H	12.7H	0.52H	12mH
C_s(pF)	0.0491	0.0126	0.00724	0.0122	0.0145
C_p(pF)	2.85	5.62	3.44	4.27	4.35
Q	25,000	25,000	30,000	80,000	150,000

Table 40.1

Section 2.1.CRYSTAL OSCILLATOR CIRCUIT

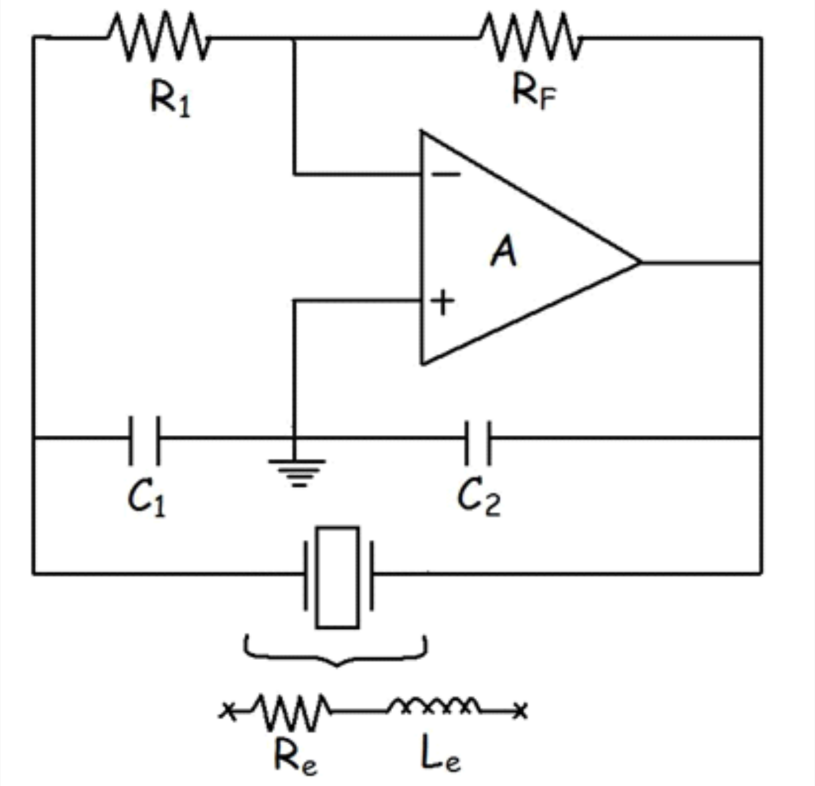

Figure 14. Crystal Oscillator using an Op.Amp.

Figure 40.18

Figure 14. Crystal Oscillator circuit using an Op.Amp.
The tank circuit of CRYSTAL OSCILLATOR

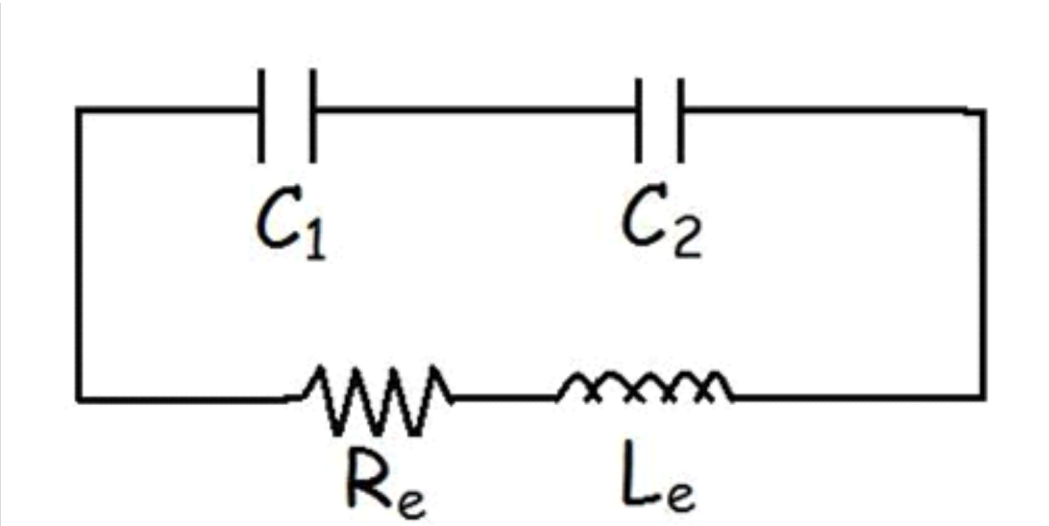

Figure 15. Parallel Resonance Circuit or the Tank Circuit in the Crystal Oscillator.

Figure 40.19

EXACT RELATION

$$\omega_o = \left[\frac{C_1R_1 + C_2R_1 + C_2R_e}{C_1C_2L_eR_1}\right]^{1/2}$$

Figure 40.20

When Q is very high which is true for crystal then $R_e \sim 0$.
And

$$g_m R_1 = \frac{C_2}{C_1}$$

Figure 40.21

In near future, we will have a Paradigm Shift. The scaling of CMOS will hit the wall. For that day we are developing ' MICROELECTROMECHANICAL SYSTEM(M E M S)',Molecular Electronics & Nanotechnology.

We have to replace low Q integrated capacitor & inductors. These will be replaced by MEMS structure. MEMS & CMOS will enable highly efficient single chip radio.

In 2002 Hewlett-Packard & HCLA announced a molecular array with 100nm center to center memory element spacing(9/10/02)

If we achieve 35nm center to center we will achieve 100 Gb memory space in $1(\text{cm})^2$.

Chapter 41

AE_Lecture 12_Tuned Amplifiers[1]

AE_LECTURE 12_Tuned Amplifier.

Section 1.TUNED AMPLIFIER

Tuned amplifiers are amplifiers as well as Band-Pass Filters.

RC-Active Filters are made of RC circuit and Op-Amp.

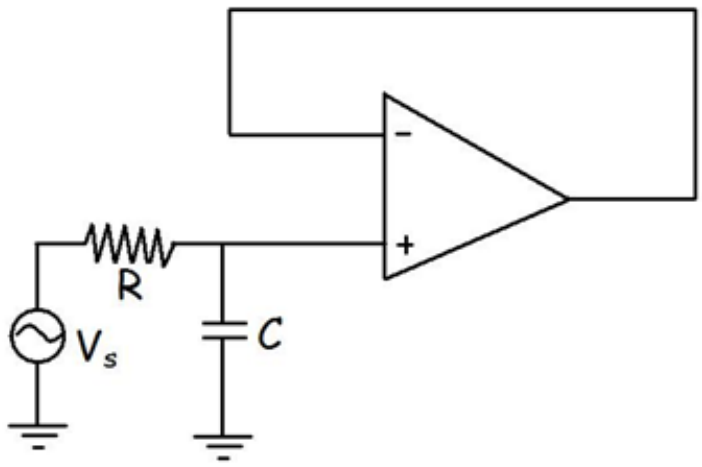

Figure 1. Low Pass Active Filter.

Figure 41.1

Figure 1. Circuit diagram of Low Pass Active Filter

This is a LOW PASS ACTIVE FILTER. But it operates at 100kHz and below because the frequency response of op-amp is very limited.

[1] This content is available online at <http://cnx.org/content/m32492/1.1/>.

To operate in RF,VHF,UHF range we have to go for circuits using parallel resonance circuits as tank circuit made of L-C-R circuits.

In communication applications we require narrow band frequency selective amplifiers so that from among closely spaced broadcasting stations, a station of choice is tuned to.

In AM radio broadcast we may need to tune to 1 MHz with a B.W. of 20kHz.

$$Q = \frac{\omega_o}{\Delta\omega} = \frac{1MHz}{20kHz} = \frac{1000}{20} = 50$$

Figure 41.2

This means a Q=50 is required.

In FM Radio Broadcast which is in VHF range, we need to tune to 100MHz with a B.W.=200kHz,here Q=500.

These narrow band pass RF-VHF amplifiers are called Tuned Amplifiers.

The tuned amplifiers are Class A amplifiers but in tuned power amplifiers the conservation of power is at premium therefore we go for class C amplifiers. Class C amplifier gives an energy conversion efficiency of 99%.Therefore dissipation and hence heating of the components is reduced.

All communication and broadcast receivers require RF amplifiers and IF Amplifiers. These are all tuned amplifiers with a peak response and a narrow band-width.

Section 1.1.SINGLE TUNED AMPLIFIER

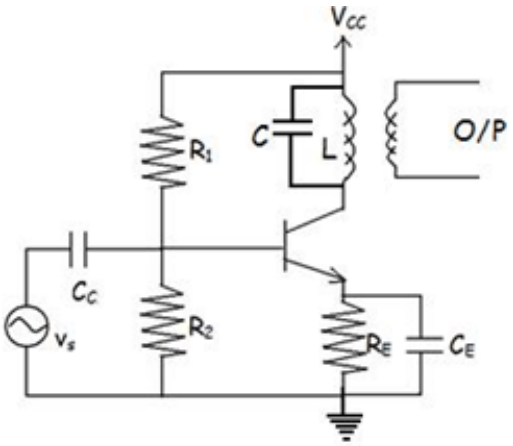

Figure 2. Single Tuned Amplifier.

Figure 41.3

Figure 2. Circuit Diagram of a Single Tuned Amplifier.

This is a CE BJT except that R_c is replaced by LC Tank Circuit. The equivalent circuit is:

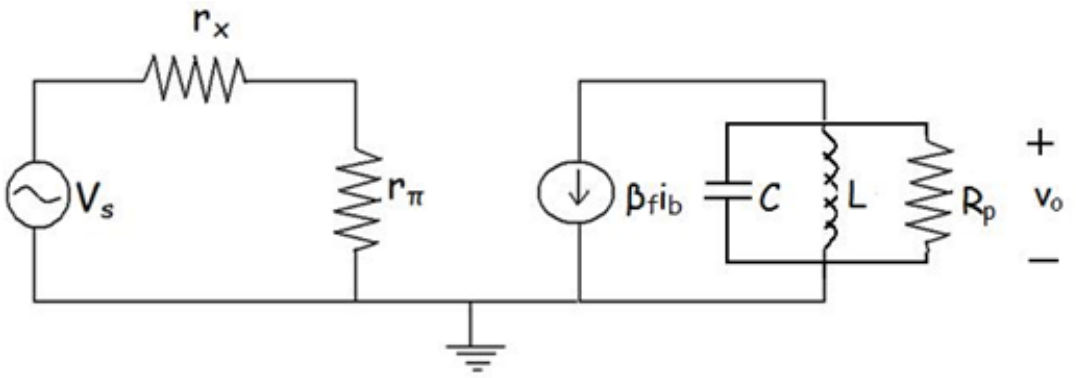

Figure 3. Incremental representation of the circuit in Figure 2.

Figure 41.4

Figure 3. The incremental circuit representation of the tank circuit.

All the losses of the tank circuit namely copper losses and dielectric losses are lumped in R_p. Since inductor is air cored hence no hysteresis and eddy current losses.

This gives a peak gain of:

$A_V(j\omega_o) = -g_m R_p$

Off resonance the gain rapidly falls. The rapid fall of the gain at off-resonance defines the selectivity or skirt selectivity of the tuned amplifier.

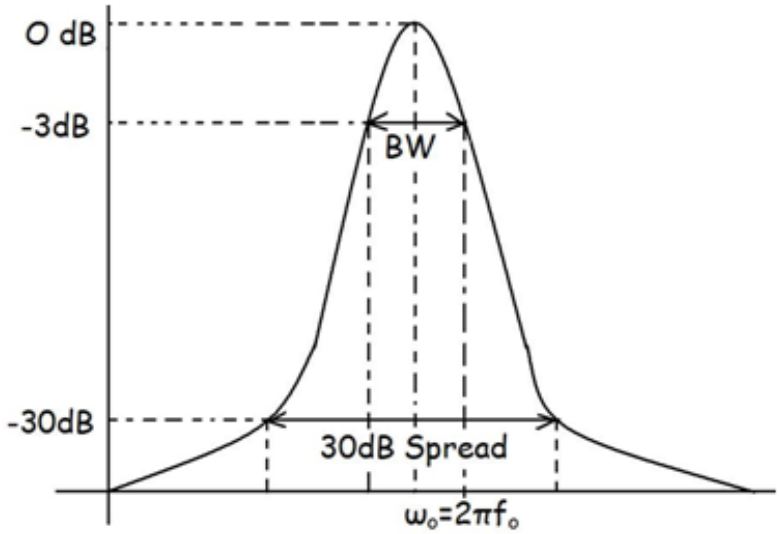

Figure 4. Gain Magnitude-Frequency Response of Tuned Am.

Figure 41.5

Figure 4. Definition of Skirt Selectivity from the frequency response curve of the tank circuit.

Skirt selectivity=

$$\left(\frac{30\ dB\ Spread}{3\ dB\ B.W.}\right)$$

Figure 41.6

Ideal tuned amplifier will have 0 dB or unity skirt selectivity but practically skirt selectivity is always greater than 1.

$$\omega_o = \frac{1}{\sqrt{LC}}$$

Figure 41.7

$$BW = \frac{1}{R_p C}$$

Figure 41.8

$$Q = \frac{R_p}{\omega_o L} = \frac{\omega_o}{\Delta\omega} = \omega_o R_p C$$

Figure 41.9

Q of Resonance circuit= Q of inductor.

$$Q = \frac{Power\ Stored}{Power\ Dissipated}$$

Figure 41.10

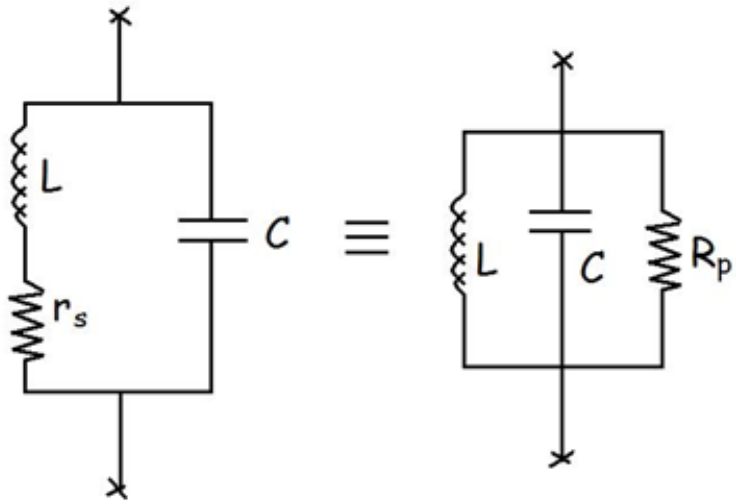

Figure 5. Two representations of a Tank Circuit.

Figure 41.11

Figure 5. The equivalent circuit representation of a tank circuit with losses represented by a series resistance in left hand diagram and by a shunt resistance in right hand diagram.

$$Q = \frac{\omega_o L}{r_s} = \frac{R_p}{\omega_o L}$$

Figure 41.12

For Q≫1, this equivalence is correct.
Section 2. USE OF AUTO TRANSFORMER TO IMPLEMENT A TUNED CIRCUIT
The problem(1) of the tutorials requires a Tank Circuit.

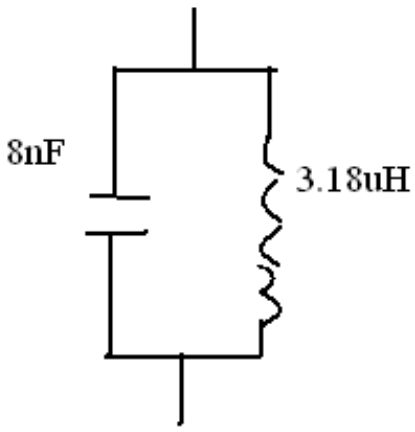

Figure 6. A tank circuit.

Figure 41.13

Figure 6. A tank circuit with 3.18μH in parallel with 8nF.

The inductance value is too small and it cannot be physically realized. So we use an Autotransformer to achieve the same.

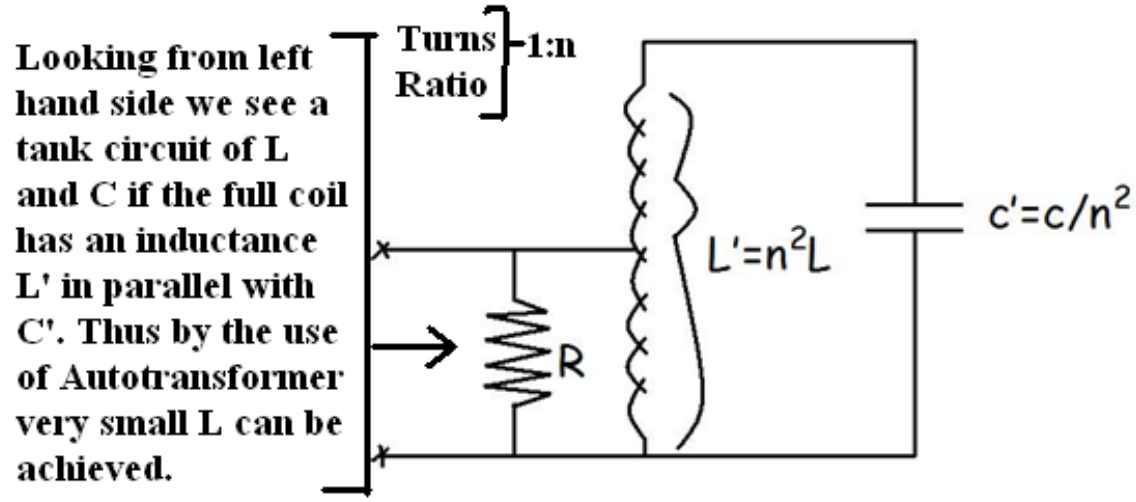

Fig.7 By use of Auto-transformer, small L can be realized where $L = L'/n^2$ and $C = C'n^2$.

Figure 41.14

Figure 7. Autotransformer Coupling for realizing small inductance of a given tuned circuit from a realistic real life inductor.

We require L=3.18μH and C=8 nF.

By use of Autotransformer if n=3

L'=$(n)^2$L=9 X 3.18 μH=28.6μH

C'=C/n^2=8 nF/9=0.9nF

L' and C' ae easily implementable.

Section 2.1.Use of autotransformer to reduce the loading of a subsequent IF Stage.

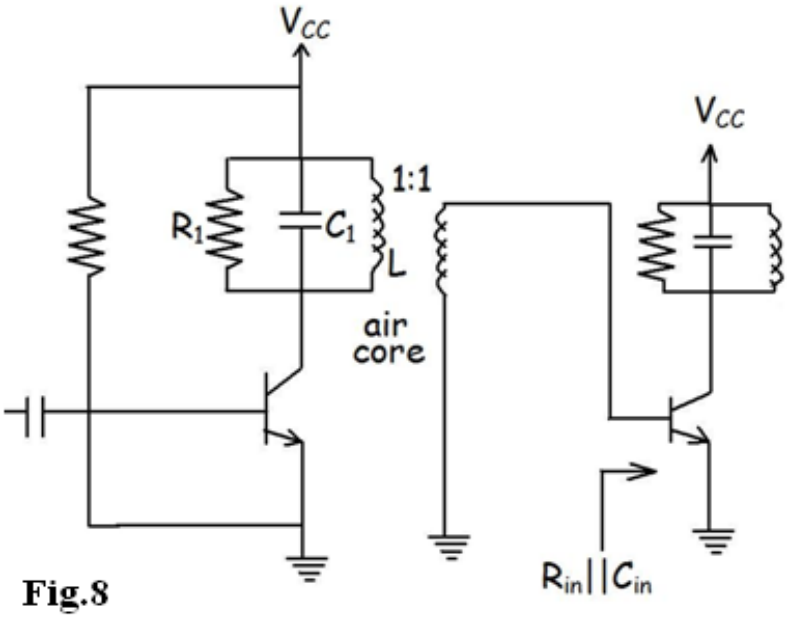

Figure 41.15

Figure 8. The deterioration of selectivity due to the loading caused by the reduced input impedance of the subsequent stage.

R_{in} will increase the B.W. and reduce the selectivity. Therefore tapped transformer is used.

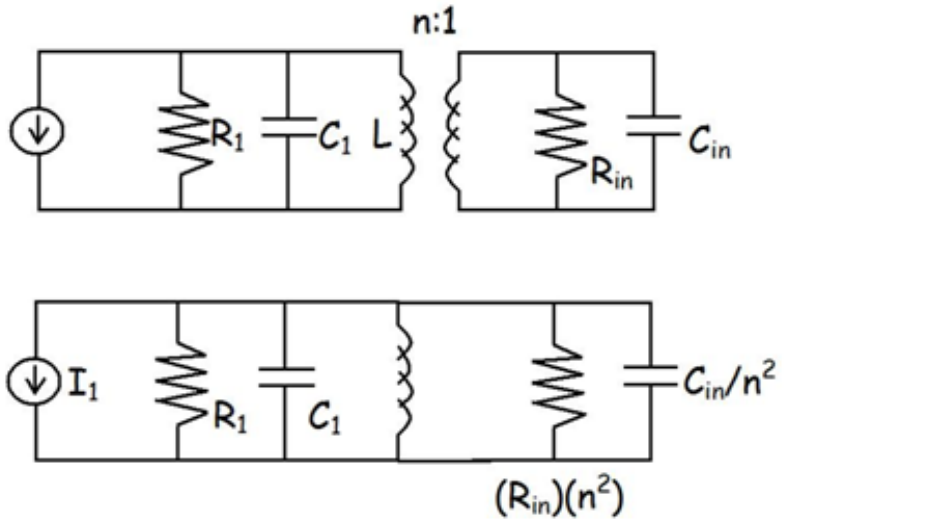

Figure 9. Use of step-down transformer to avoid loading.

Figure 41.16

Figure 9. The equivalent circuit for a tapped transformer coupled circuit.
If

$$R_{in} \times n^2$$

Figure 41.17

$\gg R_1$; $C_{in}/n^2 \ll C_1$ => Loading Avoided.
Section 3. DOUBLE TUNED CIRCUIT

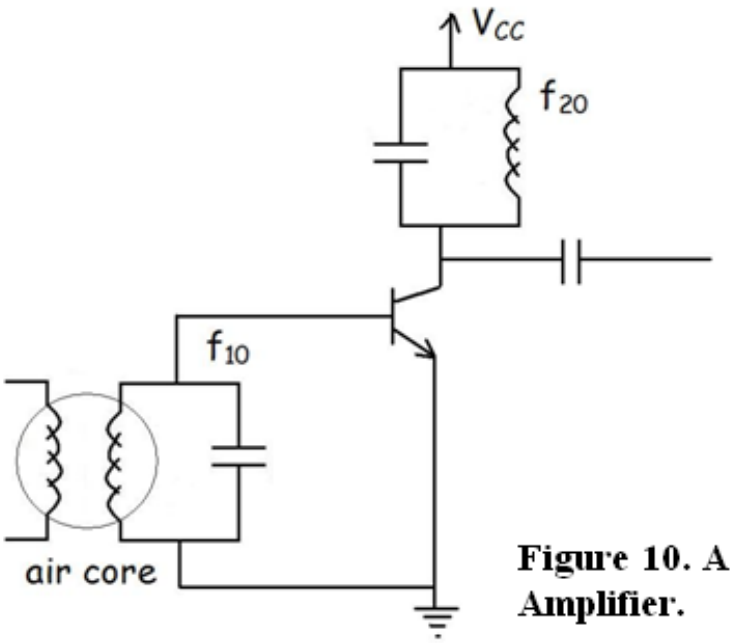

Figure 10. A double tuned Amplifier.

Figure 41.18

Figure 10. The circuit diagram of a double tuned r.f. amplifier.

In Figure 10 we see a tank circuit at the input as well as at the output. Because of the two tank circuits , these amplifiers are known as double-tuned amplifier. Double-tuned amplifiers are synchronous tuned and stagger tuned.

In synchronous tuned circuit, the two resonance frequencies are identical:

$f_{10}=f_{20}$

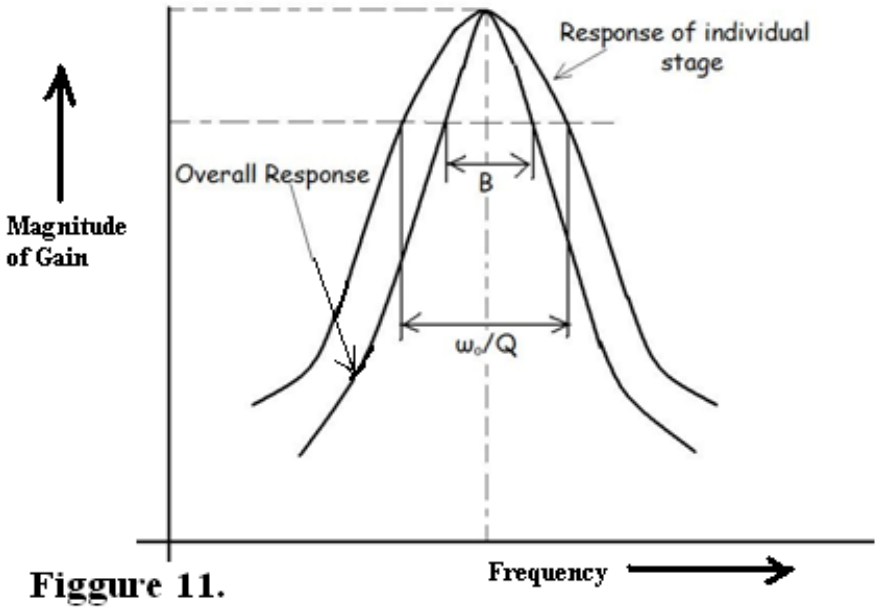

Figure 41.19

Figure 11. Frequency response of a synchronously tuned circuit.

$$B = \frac{\omega_o}{Q}\sqrt{2^{1/n} - 1}$$

Figure 41.20

In practice it is difficult to achieve synchronous tuned amplifier. Since BJT is a non-unilateral device especially in CE configuration there is considerable interaction between input and output. If we tune input tank to f_{10} and we try to tune the output tank to same frequency f_{10} immediately input will get off-tuned. If we try to tune input then output will be off tuned. Therefore it is better to keep the two tanks off tuned by Δf. This is called stagger tuned Amplifier.

$f_{20}=f_{10}+\Delta f$

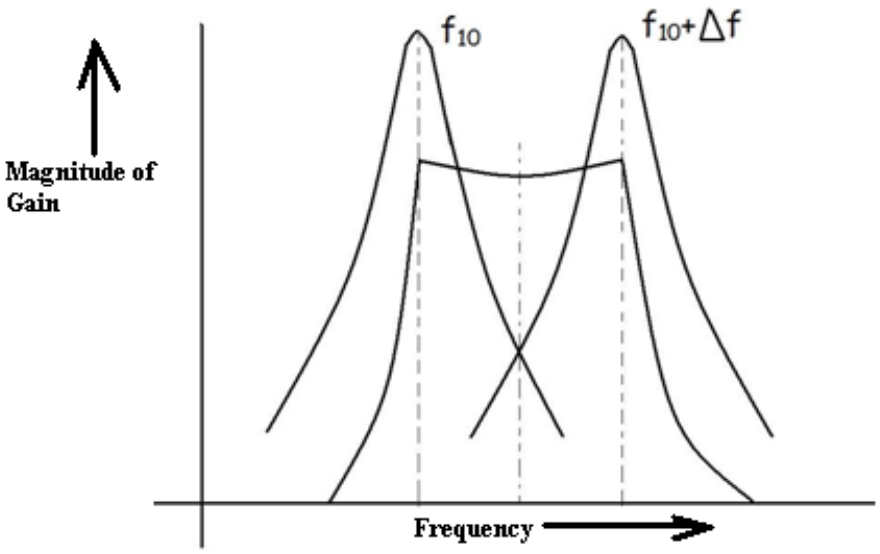

Figure 12.Staggered Tuned Amplifier.

Figure 41.21

Figure 12. Frequency response of a staggered tuned circuit.

Staggered tuned amplifier provides a better pass-band filter.. It has a wider BW maintaining a steep skirt. All IF Amplifiers in super-hetrodyne Receivers are double tuned amplifiers and are stagger tuned. There are several stages of IF Amplifiers for increased sensitivity. But to obtain the best results these multistage double tuned amplifiers need to be aligned. This is a strenuous process. By means of trimmer and padder this process is carried out.

Chapter 42

TUTORIAL NO.1 of Lecture 1 of Analog Electronics.[1]

TUTORIAL NO.1

(1) What are the Solid State Equivalents of the electronic components and systems in Vacuum Tube Era?

Vacuum Tube Era(1895- 1954)	Solid State Era(1954 onward)
Incandescent Lamp	White Light Emitting Diodes(still in experimental stage)
Cathode Ray Oscilloscope(Raster Scan System)- here we address pixel by pixel	Liquid Crystal Display (Line at a time display)- here we address row of pixels at a time.
Vacuum Diode	PN junction silicon diode(Rectifier-full wave and half wave)
Vacuum Pentode	Bipolar Junction Transistor (BJT)or Field Effect Transistor(FET)
Thyratron for industrial applications(thyratron was made of gas filled tubes)	Thyristors for industrial applications(Silicon Controlled Rectifiers_SCR made of four layer PNPN diode- these are also rectifiers but here the angle of firing or phase angle for which the SCR is on can be controlled hence it is called controlled rectifier)

continued on next page

[1] This content is available online at <http://cnx.org/content/m29639/1.1/>.

Gas filled discharge tubes produce different colours such as a. Sodium Vapour Discharge Lamps-Yellow Light; b. Neon Lamps_ Orange-Red Light; c. Mercury Vapour Lamps-UV light; d. Argon Discharge Lamps-Bluish purple light; e. Krypton Discharge Lamp-White light;	Different Coloured Light Emitting Diodes(LED) or LASER Diodes
Photo Multipliers	Photo-diodes(sensors as well as Photo Voltaic Cell or Solar Cell)
Photography Cameras	Charge Coupled Devices Camera

Table 42.1

We have studied different applications of Op.Amp. in Basic Electronics Class as well as we have studied Negative feedback Amplifiers. All the op amp amplifiers are negative feed back amplifiers. Each amplifier application approximates one of the ideal controlled sources. In the following example you have got to identify the controlled sources which the particular example of op.amp. application approximates.

(2). **Explain how a Non-inverting amplifier is a Transconductance amplifier**.

Ans:

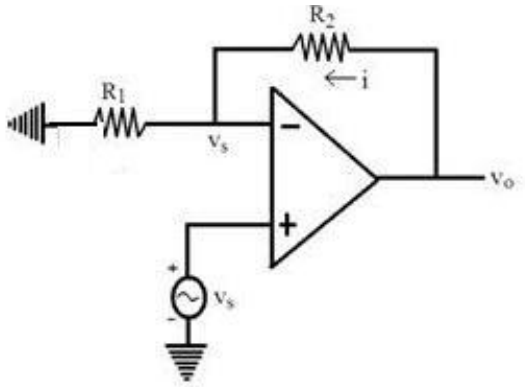

Figure 42.1

$v_O/v_S = (1+ R_2/R_1)$

From this equation we get:

$(v_O - v_S)/R_2 = i$;

Thus it is an input voltage is being converted to a current i . Hence it is voltage-to-current converter therefore it is an ideal trans-conductance amplifier or voltage controlled current source.

If we are working in terms of output voltage and input voltage then we have VCVS. It is an ideal Voltage Amplifier.

(3) **Explain how an inverting amplifier is an ideal trans-resistance amplifier.**

Ans:-

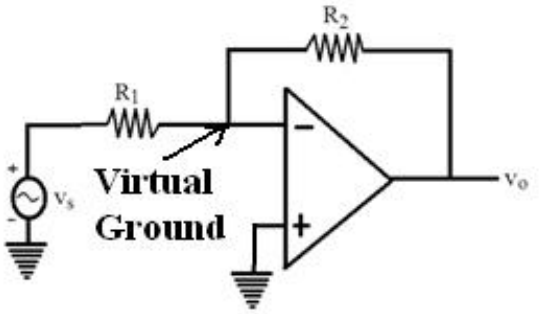

Figure 42.2

By Norton Theorem At the input terminal:-

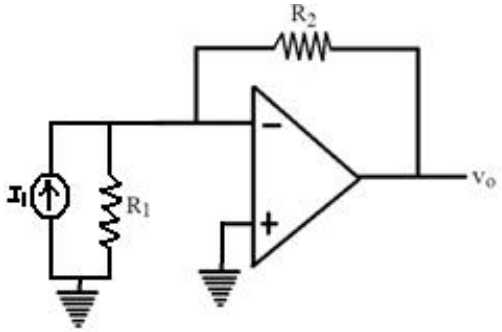

Figure 42.3

Here all input current i_1 flows into R_2 because we know that input impedance of the Op.Amp. is very large in tens of Megohms and input voltage at the double ended input of OP.Amp. is practically zero.

Therefore $v_o = - i_2 R_2$;

Here input current is being converted into output voltage;

This is known as current to voltage converter. This is used to convert photo-ionic currents generated in photocells or in photo=diodes into voltage sources with very low source impedance. Here a current source with high internal impedance is converted to a voltage source v_o with low internal impedance.

4) **Give the characteristics of the four ideal amplifiers and give an example of each.**

Ans)

Ideal Amplifier	Gain	Rin	Rout	Example
Voltage Controlled Voltage Source (Voltage Amplifier)	$A_{V_o} = \frac{open\ circuit\ voltage\ at\ o/p}{Input\ voltage}$	∞	0	Triode,Op-Amp,Emitter follower,voltage follower,source follower, Non-Inv Amplifier
Voltage Controlled Current Source (Transconductance Amplifier)	$G_{MS} = \frac{Short\ circuit\ current\ at\ o/p}{Input\ voltage}$	∞	∞	Pentode,Field Effect Transistor(FET)
Current Controlled Voltage Source (Transresistance Amplifier)	R_{MS}	0	0	Inverting Amplifier
Current Controlled Current Source (Current Amplifier)	$A_{I_s} = \frac{Short\ circuit\ current\ at\ o/p}{Input\ Current}$	0	∞	Bipolar Junction Transistor(BJT)(CE & CB)CE->i_b controls $\beta_{fo} i_b$CB->i_e controls $\alpha_{fo} i_e$

Table 42.2

Electronics In Action
MP3 Player Amplifier Characteristics (Used In APPLE IPods)

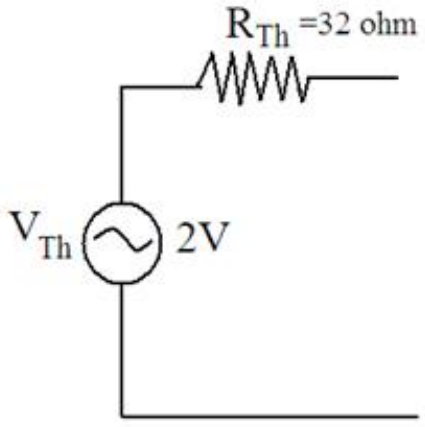

Figure 42.4

Constant voltage Source
Band Width = 20 Hz – 20 kHz

Pout =30 mW in each channel of a stereo head phone
Total Harmonic Distortion = 0.1 % at full power;
This is called a high fidelity system.

Chapter 43

Tutorial 2 on Active Devices.[1]

Tutorial 2 on Active Devices.

Summary: Here we give a short introduction to discrete and integrated circuits.

Key words: Passive Devices, Active Devices, Discrete Circuits, Integrated Circuits;

1. Active devices are the electronic components which enable amplification and oscillation. Give a Table of passive and active components.

Passive components	Active components
Resistance: Carbon track Resistance of $\frac{1}{4}$ and $\frac{1}{2}$ W, thin film NiCr resistance, CERMET resistances, wire wound resistance of 1W and above power rating. Surface Mounted Chip Resistance,	Vacuum Tube Era:Diode,Triode,Tetrode,Pentode.
Capacitance: electrolytic capacitors(10μF and above), ceramic capacitors, polystyrene capacitors, mica capacitors, gang capacitors with air-gap(variable capacitors for tuning), trimmer(variable capacitor used in series) and padder (variable capacitors in parallel).Surface Mounted Chip Capacitances.	Solid State Era:PN Jn. Diode,Bipolar Junction Transistor(BJT),Field Effect Transistor(FET),JFET , MOSFET and CMOS,Photodiode, Light Emitting Diode & LASE DIODE.
Inductors(these can be fabricated by winding enamel wire of proper guage on a thread bobbin).	Industrial Devices: Silicon Control Rectifier, DIAC, TRIAC, Uni-Junction Transistor(UJT)
Rheostat(wire wound) heavy duty variable resistance.	
Carbon Track Potentiometer(linear & logrithimic).	

Table 43.1

1. Why is the Solid State Era called the harbinger of Third Wave of Civilization?

First Wave of Civilization is Agriculture-labour intensive production.

Second Wave of Civilization is Industry- capital intensive production.

Third Wave of Civilization is Computerization, Automation and Robotization-knowledge intensive production.

[1]This content is available online at <http://cnx.org/content/m29772/1.1/>.

I.C. technology is the enabling technology of the present times and I.C.Technology is based on Solid State Physics & Devices. Hence SSPD is the harbinger of Third Wave of Civilization.

3. Who is the Father of Electronics ?

J.J. Thomson is the Father of Electronics. He discovered electron through the study of cathode ray which is a beam of electrons emitted from cathode through thermal ionic emission and collected by positively charged anode.

4. Why was the introduction of Public Service Telephone Network(PSTN) delayed by 40 years though Alexandre Grahm Bell invented telephone in 1876 ?

Triode and Pentode were invented in 1903 and 1905 respectively. Lee de Forest the inventor of Triode also invented RC-coupled Amplifier. This became the enabling technology of PSTN. Heaviside discovery of distortion-less transmission condition removed the phase distortion or propagation distortion . For this the transmission line was heavily loaded with large inductors.This enabled the first long distance call from New York to Denver, Colorado, over a distance of 2000 miles without Amplifier in 1911. Use of RC-coupled Amplifier overcame the problem of attenuation and the signal getting lost over long distances of transmission. Combining the loading for distortionless transmission and amplification, enabled first long distance call from New York to San –Francisco over a distance of 4000miles in 1913. From then onward PSTN very rapidly grew.

[Heaviside Distortionless transmission condition is :

$$\frac{L}{R} = \frac{C}{G} \qquad \textbf{Eq.1}$$

Figure 43.1

Here L= the inductance of line pair over 1 km,
R= ohmic resistance of the line over 1km,
C= inter wiring capacitance per km length of the transmission line,
G= conductance between the lines per km length .
The line can be represented as a distributed model shown in the figure:

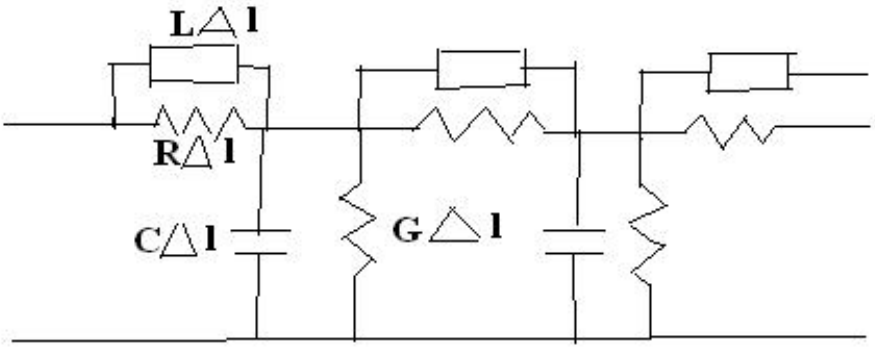

Figure 43.2

In a practical cable this balance was not achieved hence transmission line had to be loaded with a large inductors at certain intervals.]

5. When did formally Solid State Era ushered in ?

In 1948, Shockley, Bardeen & Braittain invented solid state Ge Bipolar Transistor. Subsequently Si BJT was manufactured. This ushered in Solid State era.

6. When was Integrated Circuit Technology born?

In 1959 , Jack Kilby of Texas Instrument and Robert Noyce of FairChild simultaneously announced the invention of Integrated Circuit Technolgy.

7. How was INTEL born?

Robert Noyce and Gordon Moore together launched INTEL (Integrated Electronics) in 1968. They were later joined by Andy Grove.

8. What is Moore's Law?

Gordon Moore predicted that number of transistors on integrated circuits(a rough measure of computer processing power) will double every 18 months at a minimum cost. It became a self fulfilling prophecy. Moore's Law has become a yardstick of our progress as we harness the cunning of NATURE's design strategies.

9. In this long journey of 50 years from micro to nano era where have we arrived?

In a single day the state-of-art fabs are producing 100 trillion transistors roughly 250 times the number of stars in our galaxy Milky Way. There are 43 commercial 300-mm wafer Fabs. Many more are coming on-line. Today IC Technology is the enabling Technology of the post-industrial Society.

10. What is the future direction of IC Technology?

In the future we hope to go from 45nm technology to 32nm technology to 22nm technology to 16nm technology.

Chapter 44

Tutorial 3 of AnalogElectronicsLecture3.[1]

Tutorial 3 of AnalogElectronicsLecture3.
DATA SHEET OF DIFFUSED SILICON PLANAR [BAY 73]

A) BV_A=125 V (MIN)@100μA Absolute Maximum Ratings
B) Storage temperature ratings -65^{o}C to +200^{o}C

Maximum Junction Operating temperature 175^{o}C
Lead temperature +260^{o}C

A) Power dissipation

Maximum Total Power Dissipation at 25^{o}C Ambient= 500mW
Linear power derating factor(from 25^{o}C)=3.33mW/^{o}C

A) Maximum Voltage and current

WIV working inverse voltage BAY73 = 100V
I_o Average Rectified Current= 200 mA
I_F Continuous Forward Current= 500 mA
i_f Peak Repititive forward current = 600 mA
i_f(surge) Peak Forward surge Current
Pulse width= 1 sec 1A
Pulse Width= 1μsec 4A
Electrical Characteristics(25^{o}C Ambient)

Symbol	Characteristic	Bay 73		Units	Test Condition
		MIN	MAX		
continued on next page					

[1] This content is available online at <http://cnx.org/content/m30821/1.1/>.

V_F	Forward Voltage	0.850.60	1.000.65	VV	$I_F = 200mA$ $I_F = 1\ mA$
I_R	Reverse Current		0.50	nA	$V_R = 100\ V$ $T_A = 25ºC$
B_V	Breakdown Voltage	125		V	$I_R = 100\mu A$
C	Capacitance		8	pF	V_R =0V,f=1MHz
t_{r_r}	Reverse Recovery Time		3	μsec	$I_F = 10mA$ $V_R = 35V$ $R_L = 100k\Omega$ $C_L = 10pF$

Table 44.1

Data Sheet Of Zener Diode

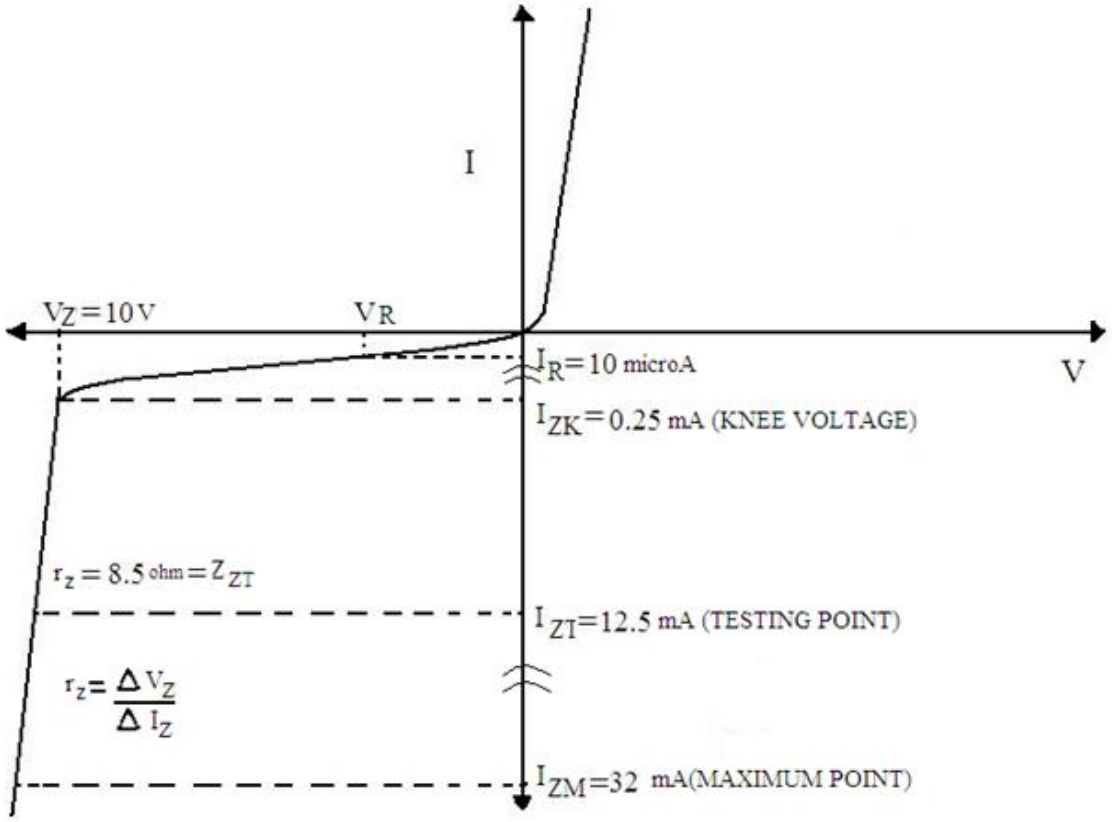

Figure 44.1

Figure 1. I-V characteristics of Zener Diode.

We have Zener break down below 4V and Avalanche Breakdown above 6V and between 4V and 6V we have mixed breakdown that is partly Zener and remaining Avalanche.

Zener Breakdown has negative temperature coefficient and Avalanche Breakdown has positive temperature coefficient. Hence at around 5V Breakdown we have almost zero temp coefficient. Hence 5V Breakdown Zener Diode can be used as an Ideal Reference Voltage Source or as a Standard Voltage Source.

Electrical Characteristics Of Zener Diode(T ambient =25ºC)

V_Z(V)	I_{ZT}(mA)	Z_{ZT} (Ω)at I_{ZT}(mA)	Z_{ZK} (Ω) atI_{ZK} (mA)	I_R (μA)at V_R(V)	V_R(V)	I_{ZM}(mA)	Temperature Coefficient %/ºC

continued on next page

-10	12.5	8.5	700 at 0.25	10	7.2	32	0.072

Table 44.2

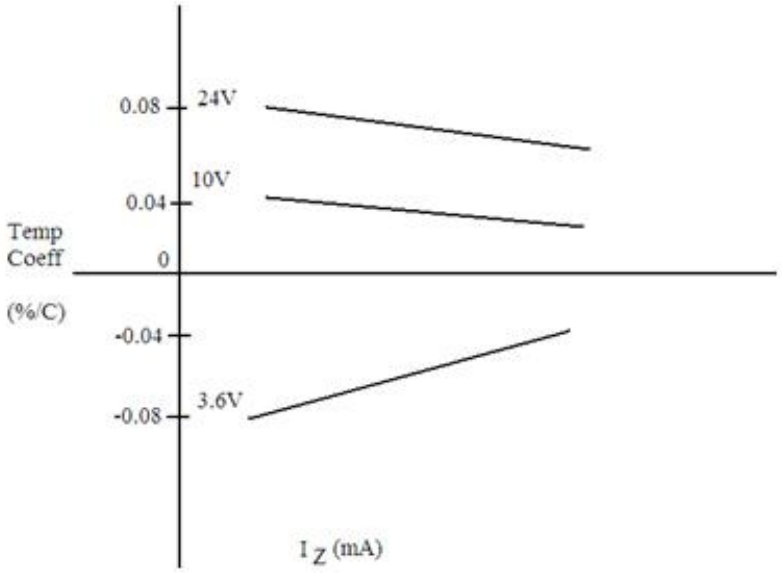

Figure 44.2

Figure 2. Temperature Coefficient of Breakdown Voltages.
Current Controlled attenuator

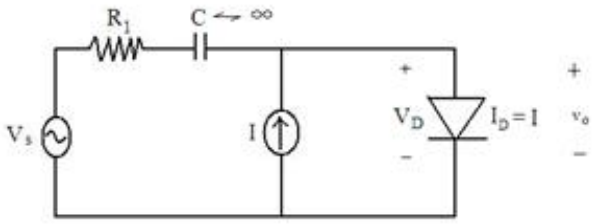

Figure 44.3

Figure 3. Current controlled attenuator.
Incremental circuit is :

$$\frac{1}{i^{\omega c}} \to 0 \, , \quad \therefore$$

Figure 44.4

C acts as a short circuit.
Diode is replaced by

$$r_d = \frac{V_T}{I_D}$$

Figure 44.5

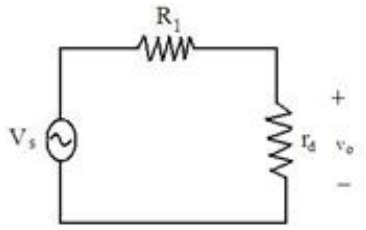

Figure 44.6

Figure 4. Incremental Model of Current Controlled Attenuator.

$$v_o = \frac{v_s}{R_1 + r_d} \times r_d$$

Figure 44.7

$$v_o = \frac{v_s}{1 + \frac{R_1}{r_d}}$$

Figure 44.8

$$v_o = \frac{v_s}{1 + \left(\frac{R_1}{V_T}\right)(I)}$$

Figure 44.9

we have:-
R_1=1kΩ
I_s=10^{-15}A

Diode Attenuator Characteristics		
I	r_d	v_o
1μA	25kΩ	0.96 v_s
10μA	2.5kΩ	0.71 v_s
100μA	250Ω	0.20 v_s
1mA	25Ω	0.024 v_s

Table 44.3

TUTORIAL (3) DIODE-Q POINT AND INCREMENTAL PARAMETERS AND SWITCHING PARAMETERS

(1)

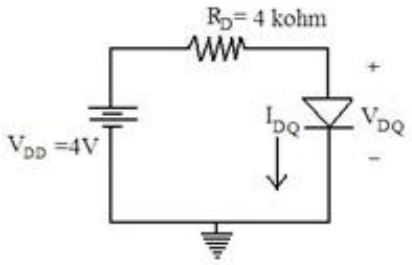

Figure 44.10

Figure 5.A diode circuit of problem 1.
Given ideality factor η=1 and $I_s=10^{-12}$A
Determine I_{DQ}, V_{DQ} by graphical method or iteration method.
[Ans: V_{DQ} =0.535V ,I_{DQ}=0864mA]
(2)

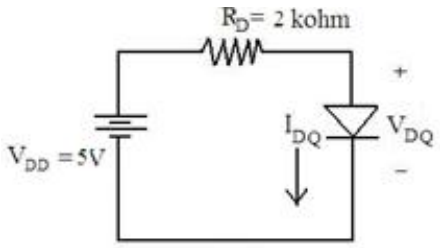

Figure 44.11

Figure 6. A diode circuit of problem 2.
Given η=1 and $I_s=10^{-13}$A
Determine I_{DQ}, V_{DQ} by graphical method or iteration method.
[Ans: V_{DQ} =0.619V , I_{DQ}=2.19mA]
(3)A diode circuit is given below:

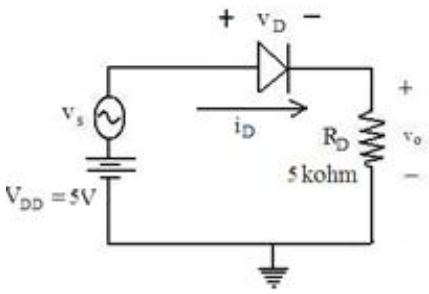

Figure 44.12

Figure 7. A diode circuit with a signal source in Problem 3.

Figure 44.13

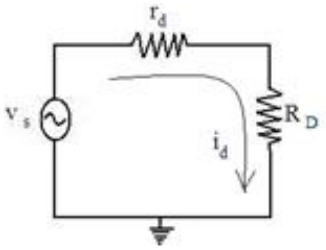

Figure 44.14

Figure 8. Incremental model of the diode circuit under signal condition.
v_s=[0.1Sin(ωt)]V
Let V_{DQ}=0.6V
Determine I_{DQ}, V_{DQ}, r_d and $v_o = i_d R_D$. [$v_o = i_d R_D$=0.0995 sin(ωt) (V)]
{Ans I_{DQ} =0.88 mA, V_{DQ} =0.6V, r_d=29.5Ω}
(4) **) Calculate the values of the incremental resistance rd for a diode with Is (reverse saturation current)= 1fA operating at ID=50 μA,2mA,3A.**

Ans: We know that

$$r_d = \frac{V_T}{I_D}$$

Figure 44.15

where

$$I_D = I_S \, exp\left(\frac{V_D}{V_T}\right)$$

Figure 44.16

Thus we get r_d = 500Ω, 12.5Ω, 8.33mΩ

(5) What is the small signal diode resistance r d at room temperature and at 100ºC for operating current I D =1.5 mA ?

Ans: We know that:

$$r_d = \left(\frac{kT}{q}\right)\Big/ I_D$$

Figure 44.17

Thus we get

$$r_d = 16.7\ \Omega \ at\ 300K \ and \ r_d = 21.4\Omega \ at \ T = 100ºC$$

Figure 44.18

Chapter 45

Tutorial 3_supplementary_AE Lecture No.3.[1]

Tutorial 3_supplementary_AE Lecture No.3.

Problems on parasitic capacitances associated with Diode at high frequencies.

Problem 1.Given a diode under reverse bias with a depletion width 4μm.

a. If cross sectional area is 1mm square, determine C_{jD} given

Absolute permittivity $\varepsilon_0 = 8.854\times10^{-12}$F/m and relative permittivity or dielectric constant (k) = ε_r= 11.6 [Answer: 26pF]

a. If C_{jD}= 15pF then determine the cross sectional area. [Ans.0.6 mm^2]

Problem 2. A diode is under forward bias condition at V_D = 0.7V. Reverse Saturation current I_S=16nA at 300K. Minority carrier life time are $\tau_n = \tau_p$ = 25μsec.

a. Find C_d = diffusion capacitance ; [1/($r_d C_d$) = 1/ τ_n +1/ τ_p ; [Answer 5.74μF]
b. Find V_D which gives C_d = 10μF; [Answer V_D = 0.729V]

Problem 3. A silicon PN junction has doping concentrations $N_A = 10^{19}$/cc & $N_D = 10^{15}$/cc. Cross sectional area A= 0.001cm^2. Since it is one sided step junction major role is played by holes injected in N-type region. Hence the life-time of holes is given τ_p(P region)= 0.3μsec.

Under forward bias condition of V_D = 0.6V , determine:

a. Diffusion Capacitance C_d ;
b. Transition or Junction Capacitance C_{jD};

Solution: Here I_D is not given nor the saturation current I_S is given. We can use the doping to find either of the two.

$I_D = Q_p/\tau_p$ and

Q_p= charge stored in N region under forward biased condition =

q{p_n(0)-p_n(thermal equilibrium)}L_pA;

and $L_p=\sqrt{(D_p\tau_p)}$ and $D_p = \mu\times V_T$ = 450 cm^2/(V-sec)×26mV= 11.7 cm^2/sec;

Therefore $L_p = 1.94\times10^{-3}$ cm.

Therefore I_D= q{p_n(0)-p_n(thermal equilibrium)}L_pA/τ_p = 2.453mA;

Therefore r_d = 26mV/2.453mA =10.59 Ω.

$r_d\times C_d = \tau_p$ therefore C_d =28,000pF.

[1] This content is available online at <http://cnx.org/content/m30892/1.1/>.

Calculation of C_{jD}:
$C_{jD} = \varepsilon A/d_n$ where d_n = the depletion width on N-side = $\sqrt{(q\varepsilon N_D/2)}\sqrt{(\phi_{B0}\text{-}V_F)}$;
In a one sided step junction $d \sim d_n$ (depletion width on the lightly doped side);
Therefore $C_{jD} = \varepsilon A/[\sqrt{(q\varepsilon N_D/2)}\sqrt{(\phi_{B0}\text{-}V_F)}] = \sqrt{(2\varepsilon/(qN_D))} \times (1/\sqrt{(\phi_{B0}\text{-}V_F)})$;
ϕ_{B0} = Built in barrier potential under zero bias condition= $V_T \ln(N_A N_D/n_i^2)$=817.056mV;
Therefore C_{jD}= 19.8 pF.

Chapter 46

AE_Tutorial 4_BJT incremental model.[1]

AE_Tutorial 4_BJT incremental model.

Small signal model of a BJT

(1) BJT Small signal parameters versus current

Given β_o=100,

V_A [Early Voltage]=75V,

V_{CE}=10V

$$g_m = \frac{I_c}{V_T}$$

Figure 46.1

$$r_o = \frac{V_A + V_{CE}}{I_C}$$

Figure 46.2

---

[1] This content is available online at <http://cnx.org/content/m31739/1.1/>.

$$\mu_f = g_m r_o = \left(\frac{V_A + V_{CE}}{V_T}\right)$$

Figure 46.3

$$r_\pi = \frac{\beta_o}{g_m}$$

Figure 46.4

$$g_m = 40 I_C$$

Figure 46.5

I_c	g_m	r_π	r_o	μ_f
1μA	4 x 10^{-5}S	2.5MΩ	85MΩ	3400
10μA	4 x 10^{-4}S	250kΩ	8.5MΩ	3400
100μA	0.004S	25kΩ	850kΩ	3400
1mA	0.04S	2.5kΩ	85kΩ	3400
10mA	0.40S	250Ω	8.5kΩ	3400

Table 46.1

(2)Calculate the values of g_m, r_π, r_o, μ_f for a BJT with β_o=75,V_A=60V and Q-point(50μA,5V).
(Answer: 2mS, 37.5kΩ, 1.3MΩ, 2600)
(3)Calculate the values of g_m, r_π, r_o, μ_f for a BJT with β_o=50,V_A=75V and Q-point(250μA,15V).
(Answer: 10mS, 5kΩ, 360MΩ, 3600)
(4)What is the small signal limit of BJT?
[Answer: |

Figure 46.6

|

Figure 46.7

5mV and |

Figure 46.8

|

Figure 46.9

20% of I_C]

We will see that small signal limit of FET is 400mV. This is because BJT is an EXPONENTIAL DEVICE whereas FET is a QUADRATIC DEVICE.

5)Find the transit time for a NPN BJT with base width 1μm and μ_n=500

Figure 46.10

& T=300K

According to Einstein Eq:

$$\frac{D_n}{\mu_n} = V_T = 26mV$$

Figure 46.11

[Answer:

$$\frac{W^2}{2D_n} = \tau_n = 0.4\ nsec$$

Figure 46.12

]
(6)In problem (5) for I_{CQ}=1mA determine C_D(diffusion capacitance)for the BJT.
[Ans: $C_D r_e = \tau_t$; Therefore C_D=16pF]
(3)Give the hybrid-π parameters of a BJT operating at I_{CQ}= 2mA,V_{CEQ}= 5V,β_F=40 and h_{re}=3.83x10^{-4} = η = Base Width Modulation Factor.
[Answer:

$$g_m = \frac{I_C}{V_T} = \frac{1}{13\Omega}; g_\pi = \frac{1}{r_\pi} = \frac{g_m}{\beta_{fo}} = \frac{1}{520\Omega}$$

Figure 46.13

$$g_o = \frac{1}{r_o} = \frac{\eta}{g_m} = \frac{1}{33.942K}; g_\mu = \frac{1}{r_\mu} = \frac{1}{\beta_{fo} r_o} = \frac{1}{1.34M\Omega}]$$

Figure 46.14

$$\beta_{fo}(Incremental\ current\ gain) = \beta_F(DC\ Current\ gain)$$

Figure 46.15

(4) Measurement of low frequency h parameters h_{ie}, h_{re}, h_{fe} and h_{oe} at I_{CQ}=0.5mA yield h_{ie}=2050 ohm, h_{re}=5x10^{-4}, h_{fe}=40, h_{oe}=2x10^{-5},CB output capacitance C_{ob}=3pF and $|h_{fe}|$ at 1MHz is $40/\sqrt{2}$; At 290K(V_T=25mV) calculate g_m, r_x, r_π, r_o, r_μ, C_π, C_μ.

Answer:

$$g_m = \frac{I_{CQ}}{V_T} = \frac{1}{50\Omega}, h_{fe} = 40 = \beta_{fo}, r_\pi = \frac{\beta_{fo}}{g_m} = 2K$$

Figure 46.16

$$g_o = h_{re}g_m = \frac{1}{100K}; r_\mu = \beta_{fo}r_o = 4\ M$$

Figure 46.17

$$\omega_\beta = \frac{1}{r_\pi(C_\pi + C_\mu)}; C_\pi + C_\mu = 79.6pF$$

Figure 46.18

$$C_\mu = \text{Cob} = 3\text{pF}; C_\mu = 76.6pF$$

Figure 46.19

$$h_{ie} = r_x + r_\pi = 2050; r_x = 50\Omega$$

Figure 46.20

(5)If

$\beta_{fo} = 100$ *and* $|\beta| = 50$ *at* 4 MHz. *Calculate* f_β & f_T, *also find* C_π *given* $g_m = 50\ mS, C_\mu = 4pF$

Figure 46.21

Answer:-

$$f_\beta = 2.31\ MHz, f_T = \beta_{fo} f_\beta = 231 MHz, C_\pi = 30.5pF$$

Figure 46.22

Chapter 47

AE_Tutorial 5_Mid&High frequency Analysis of CE & CB BJT Amplifier[1]

TUTORIAL 5_MID & HIGH frequency analysis of CE & CB amplifiers.
(1)

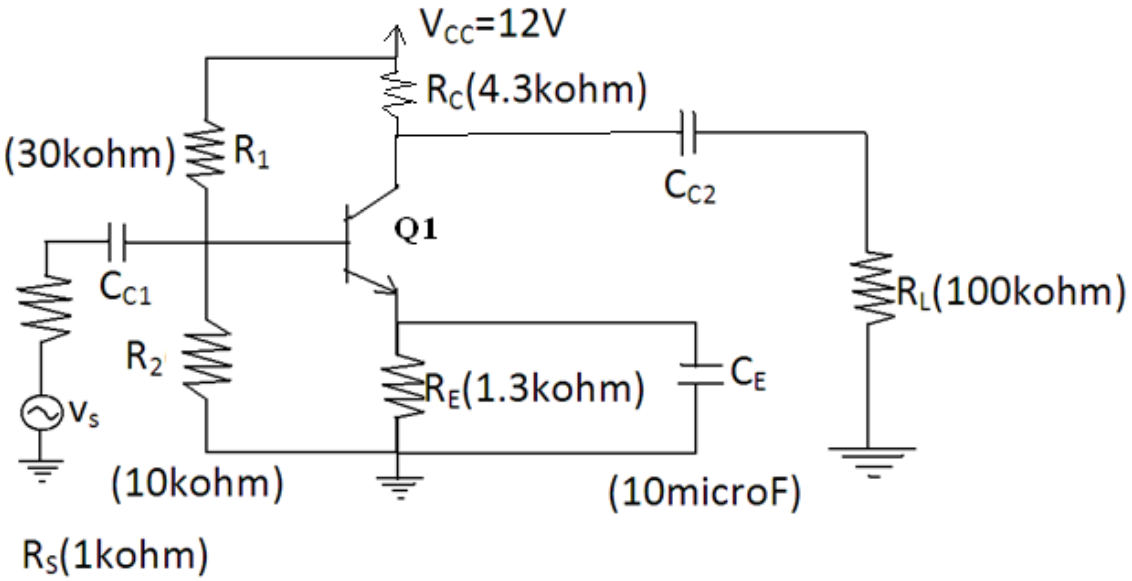

Figure 1. Circuit diagram of RC-coupled CE BJT Amplifier

Figure 47.1

[1]This content is available online at <http://cnx.org/content/m31743/1.1/>.

$$\beta_o = 100, f_T = 500MHz, C_\mu = 0.5pF, r_x = 250\Omega$$

Figure 47.2

Q point(1.6mA,3V)
Find A_{vo} And f_h.
Solution:-

$$A_{V_o} = -\frac{\beta_o R_C \,||\, R_L}{R_{Th} + r_x + r_\pi}$$

Figure 47.3

$$= -\frac{100(4.12k)}{0.882k + 0.25k + 1.56k} \sim -153$$

Figure 47.4

$$C_T = C_\pi + C_\mu(1 + g_m R_L)$$

Figure 47.5

$$C_\pi + C_\mu = \frac{g_m}{2\pi f_T}$$

Figure 47.6

$$\therefore C_\pi = 19.9pF$$

Figure 47.7

$$R_C \,||\, R_L = 4.12k\Omega, R_{Th} = R_s \,||\, R_B = 1k\Omega \,||\, \left(\frac{R_1 R_2}{R_1 + R_2}\right) = 1k\Omega \,||\, 7.5k\Omega$$

Figure 47.8

$$\therefore R_{Th} = 0.882k\Omega; r_{\pi o} = r_\pi \,||\, (R_{Th} + r_x) = 1.56k \,||\, 7.5k$$

Figure 47.9

$$\therefore r_{\pi o} = 0.656k\Omega$$

Figure 47.10

$$C_T = 19.9pF + 0.5pF(1 + 264) = 152.4pF$$

Figure 47.11

$$f_h = \frac{1}{2\pi r_{\pi o} C_T} = \frac{1}{2\pi(0.656k)(152.4pF)} \sim 1.56MHz$$

Figure 47.12

$$A_{vo} = -153, f_h = 1.56MHz, A_{Vs} = -135$$

Figure 47.13

(2)In problem (1),if C_μ =1pF,what is the new value of A_{Vo} &f_h ?
[Answer:- A_{Vo} remains -153 but f_h deteriorates to 835kHz.]
(3) Given CB BJT Amplifier in Figure 2.

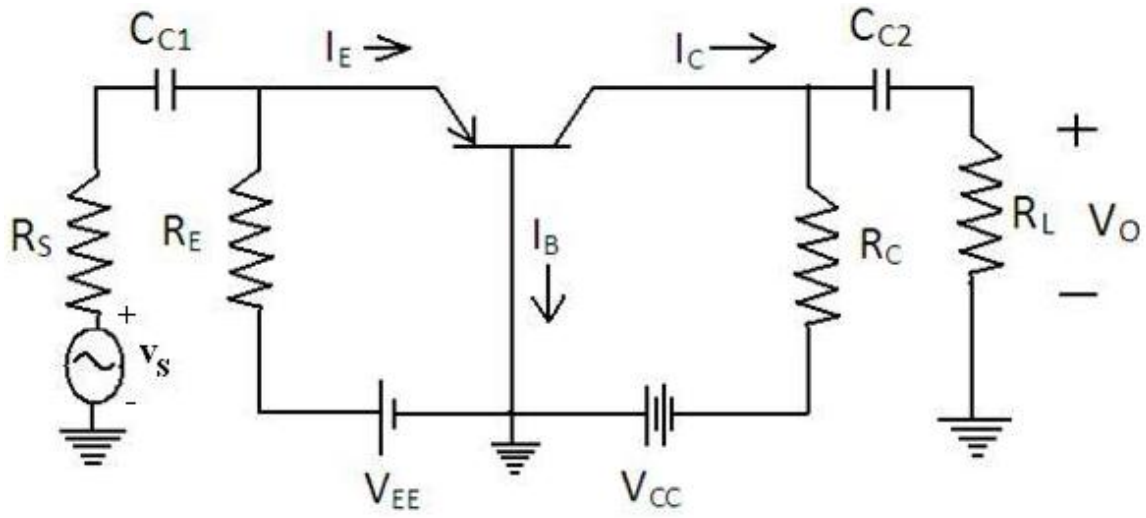

Figure 2. RC-coupled CB BJT Amplifier with two battery biasing.

Figure 47.14

All the parameters are the same & Q point is the same.
R_C = 22k, R_L = 75k, R_E = 43k, R_S = 0.1k;
[Ans: A_{VS}=48, f_h=10.7MHz]
Solution: We will have to use the T-model for analyzing CB BJT Amplifier and we will use open circuit time constant method for detrmining the upper -3dB frequency.
C_μ =0.5pF, C_π =19.9pF

$$C_\mu \sim C_C; \quad C_\pi = C_e$$

Figure 47.15

MIDBAND GAIN Analysis:

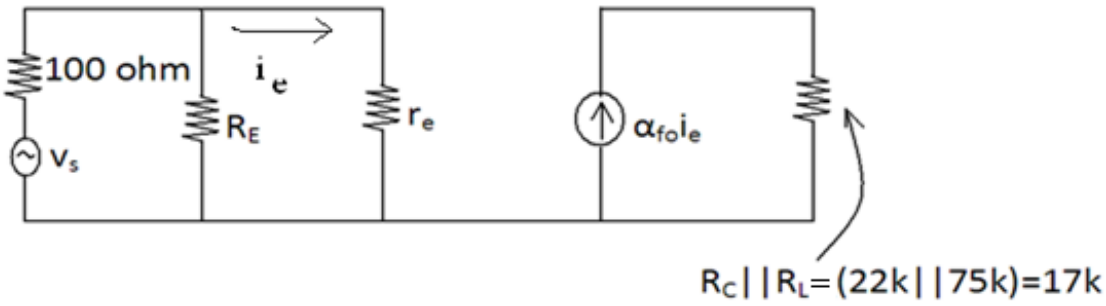

Figure 3. Mid-frequency incremental model of CB BJT Amplifier

Figure 47.16

$$r_e = \frac{V_T}{I_E} = \frac{25mA}{0.1mA} = 250\Omega$$

Figure 47.17

$$v_o = (\alpha_{fo} i_e)(17k\Omega)$$

Figure 47.18

$$v_s = i_e(0.1k\Omega + 0.25k\Omega)$$

Figure 47.19

$$\frac{v_o}{v_s} = A_{vso} = \frac{17k\Omega}{0.35\Omega} = 48.57$$

Figure 47.20

At high frequency

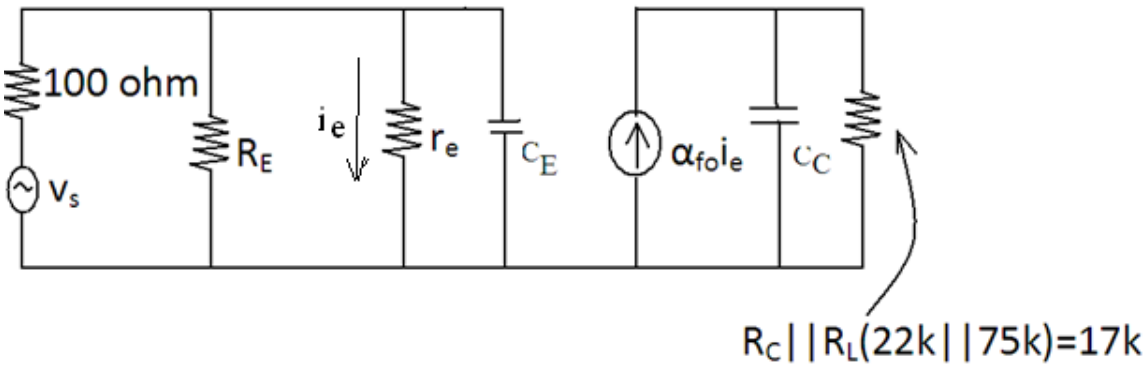

Figure 4. High frequency incremental model of CB BJT Amplifier

Figure 47.21

$$\tau_{o1} = (C_e)(r_e || R_E || R_s)$$

Figure 47.22

$$(r_e || R_E || R_s) = (0.25k) || (43k) || (0.1k) = \frac{(0.25)(0.1)}{0.35} = 71\Omega$$

Figure 47.23

$$\tau_{o2} = (C_C)(R_C \,||\, R_L)$$

Figure 47.24

$$\tau_o = \tau_{o1} + \tau_{o2}$$

Figure 47.25

$$\sim\tau_{o2}$$

Figure 47.26

$$\omega_h = \frac{1}{\tau_{o2}}$$

Figure 47.27

$$\tau_{o1} = (19.9pF)(71\ ohm) = 1.4nsec$$

Figure 47.28

$$\tau_{o2} = (0.5pF)(17kohm) = 8.5nsec$$

Figure 47.29

$$\therefore \tau_o = 9.9nsec = 10nsec$$

Figure 47.30

$$\therefore \omega_h = \frac{1}{10} \times 10^9 \, rad/_{sec} = 10^8 \, rad/_{sec}$$

Figure 47.31

$$\omega_h = 100 \, \frac{Mrad}{sec}$$

Figure 47.32

$$f_h = \frac{100}{2\pi} MHz$$

Figure 47.33

Chapter 48

AE_Tutorial6_Mid & High Frequency Analysis of CC & Cascode.[1]

AE_TUTORIAL NO.6_Analysis of CC & Cascode Amplifiers

Table of CC Amplifier performance Parameters

Internal voltage gain=

$$\frac{v_o}{v_{in}} = \frac{\beta_o R_C || R_L}{r_\pi + (1+\beta_o) R_C || R_L} = \frac{g_m R_C || R_L}{1 + g_m R_C || R_L}$$

Figure 48.1

$$R_{in} = r_\pi + (1+\beta_o) R_C || R_L$$

Figure 48.2

$$R_{out} = \frac{1}{g_m}$$

Figure 48.3

---

[1] This content is available online at <http://cnx.org/content/m31744/1.1/>.

I/P signal range 0.005(1+

$$g_m R_L$$

Figure 48.4

)
Terminal Current Gain (

$$1 + \beta_o$$

Figure 48.5

)
Problem 1.

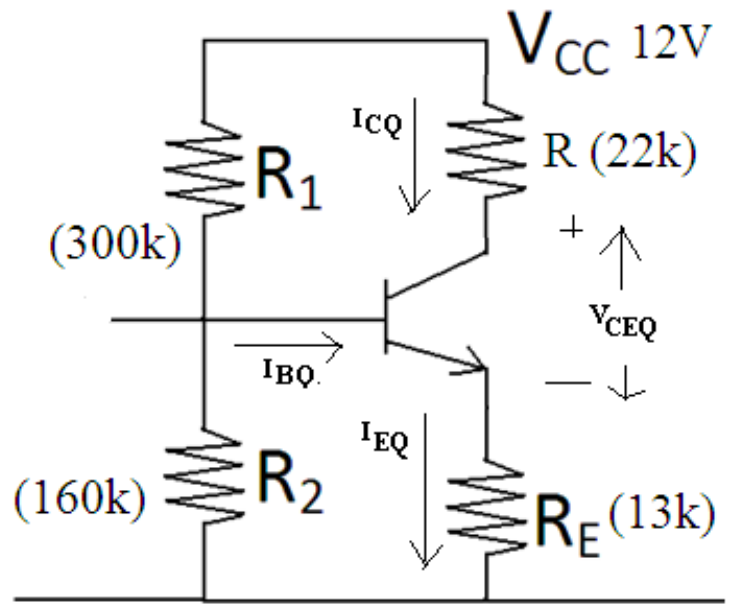

Figure 1. A BJT with self bias.

Figure 48.6

Given:

$$\beta_F = 100, V_A = 50V$$

Figure 48.7

Find the Q point and hybrid pi parameters.
[Ans:

$$I_{CQ} = 245\mu A, V_{CEQ} = 3.64V, g_m = 9.8mS, r_\pi = 10.2k\Omega, r_o = 219k\Omega, \mu_f = 2130]$$

Figure 48.8

Problem 2. Draw the small signal equivalent circuit or the incremental circuit of CC amplifier.

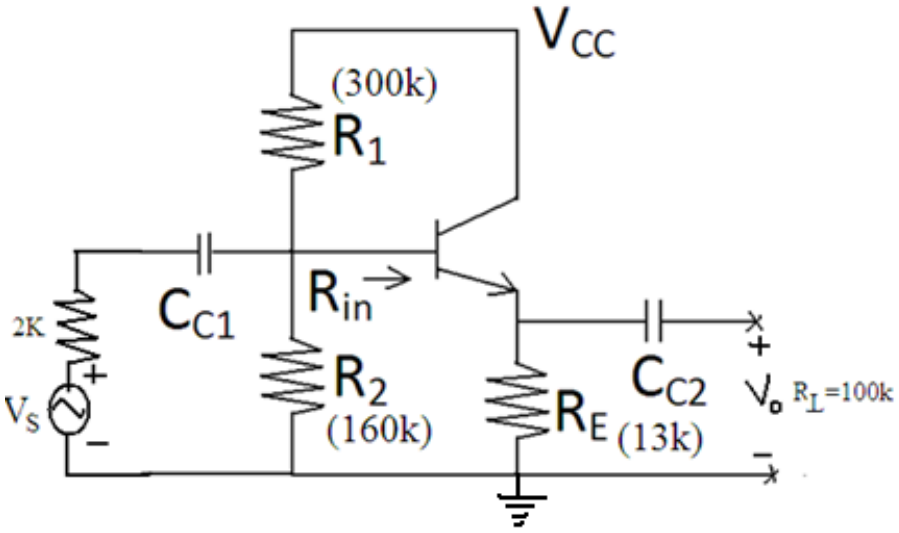

Figure 2. Circuit diagram of CC Amplifier.

Figure 48.9

Given:

$$\beta_F = 100, V_A = 50V$$

Figure 48.10

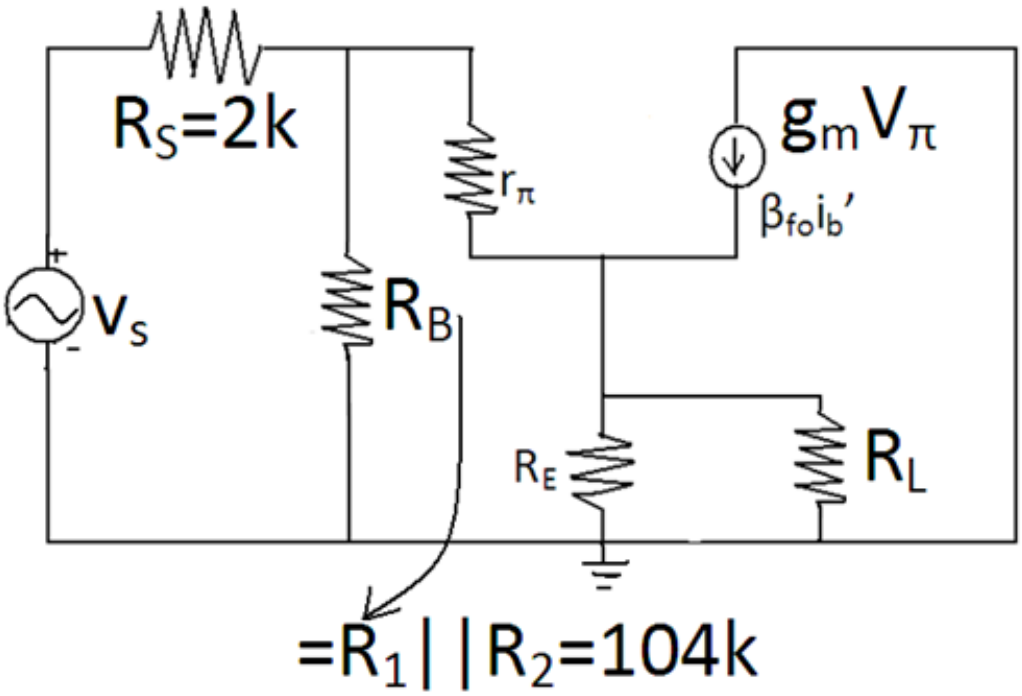

Figure 3. Mid-frequency model of CC BJT Amplifier.

Figure 48.11

Find the Q point and the hybrid-π parameters
Ans:

$$I_{CQ} = 245\mu A, V_{CEQ} = 8.8V, g_m = 9.8mS, r_\pi = 10.2k\Omega, r_o = 240k\Omega$$

Figure 48.12

Problem 3.Calculate the voltage gain and R_{in} of the CC amplifier of Problem 2.

[Ans

$$R_{in}(seen\ from\ source) = R_B||\left(r_\pi + (1+\beta_o)R_E{}'\right)$$

Figure 48.13

$$\therefore R_{in} = (104k\Omega)||(10.2k\Omega + (101)11.5k\Omega)$$

Figure 48.14

$$R_{in} = (104k\Omega)||(1.17M\Omega)$$

Figure 48.15

$$A_{Vo}(Internal) = \frac{(\beta_o+1)R_L}{r_\pi + (1+\beta_o)R_L} = \frac{(101)(11.5k)}{10.2k + (101)11.5k} = 0.991$$

Figure 48.16

$$A_{Vos}(Overall\ w.r.t.\ v_s) = A_{Vo}\left(\frac{R_{in}}{R_s+R_{in}}\right) = \frac{(0.991)(104k\,||\,117k)}{2k+(104k\,||\,117k)} = 0.956$$

Figure 48.17

]

(4)Determine the input dynamic range for CC amplifier ?

The voltage developed across r_π must be less than 5mV if BJT is to remain a linear device. Therefore

$$v_{be} = i_b r_\pi = \frac{v_{in}}{(r_\pi + (1+\beta_o)R_E')} \times r_\pi = \frac{v_{in}}{1 + g_m R_E' + \frac{R_E'}{r_\pi}} \sim \frac{v_{in}}{1 + g_m R_E'}$$

Figure 48.18

$$\therefore v_{in} \leq (5mV)\left(1 + g_m R_E'\right) \leq 5mV(1 + 112) \leq 0.565V$$

Figure 48.19

Therefore signal handling capacity has increased by

$$\left(1 + g_m R_E'\right)$$

Figure 48.20

times because of negative feedback property of CC amplifier. Similarly in an Emitter Degenerate amplifier also the signal handling capacity increases due to negative feedback.

(5)How do the I/P signal handling capacity of CC and CD compare?

Ans:- CC I/P signal handling 0.565V

CD I/P signal handling 1.23V

BJT is an exponential device whereas FET is a quadratic device therefore FET can handle larger signal with little or no harmonic distortion.

(6)What is the output resistance of CC amplifier ?

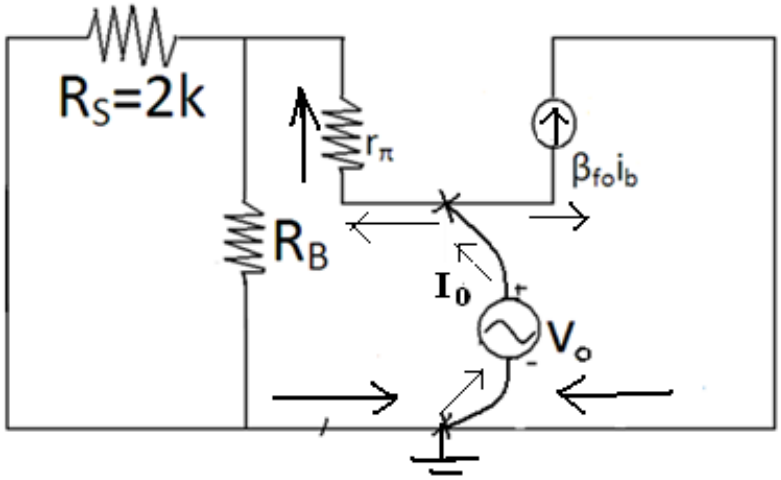

Figure 4. The incremental circuit for determining the mid-frequency output impedance of CC Amplifier.

Figure 48.21

$$i_o = i_b(1+\beta_{fo}) \& i_b = \frac{v_o}{(r_\pi + R_S||R_B)}$$

Figure 48.22

$$\therefore i_o = \frac{v_o(1+\beta_{fo})}{(r_\pi + R_S||R_B)}$$

Figure 48.23

$$\therefore \frac{v_o}{i_o} = R_o = \frac{(r_\pi + R_S||R_B)}{(1+\beta_{fo})} = \frac{(10.2k + 1.96k)}{101} = 120\Omega$$

Figure 48.24

This Ro comes in parallel with Re'. Because of very high

$$R_{in}$$

Figure 48.25

and very low

$$R_{out}$$

Figure 48.26

and Av $\sim$ 1, CC amplifier acts as an ideal voltage source for driving variable loads and transmission lines.
(6)Make a table of the performance parameters of CC amplifier.

Avo	0.956
R_{in} (without loading of biasing network)	1.17Mohm
R_{out}	121ohm
I/P *Dynamic Range*	0.565V
Current Gain	101

Table 48.1

By Bootstrap technique the loading of Biasing network can be removed.
(7)Referring to the figure in Lecture 10,Calculate the two port hybrid parameters of the CASCODE amplifier.
Make the following assumptions.
Q_1(I_{C1}=101μA,5V) and Q_2(I_{C2}=100μA,V_{CE2} 10V)Q_1 and Q_2 are identical,β_F =β_{fo}=100,V_A=75V;
What are the hybrid $-\pi$ parameters of Q_2 at I_{C2}=100μA,V_{CE2}=10V.What are the current gain and amplification factor of the cascade amplifier?
[Ans: Hybrid parameters of the Cascode

$$h_i = \beta_{fo}\frac{V_T}{I_C} = 100 \times \frac{25mA}{0.1mA} = \frac{2500}{0.1} = 25k;$$

Figure 48.27

$$h_r = h_{re}h_{rb} = \frac{r_\pi}{r_\mu} \times \frac{r_x}{r_\mu} = 0 \ \because r_x = 0$$

Figure 48.28

$$g_m(overall\ transconductance) = \frac{i_o}{v_{in}} = g_{m1} = \frac{I_C}{V_T} = \frac{0.1mA}{25mV} = \frac{1}{250\Omega} = 0.004$$

Figure 48.29

$$h_o = \frac{1}{r_{ob}} = h_{ob} = \frac{1}{r_o(of\ CE)(1+\beta_{fo})}$$

Figure 48.30

$$But\ r_o(of\ Q_2) = \frac{V_A + V_{CEQ}}{I_{C_2}} = \frac{75V + 10V}{0.1mA} = \frac{85V}{0.1mA} = 850k$$

Figure 48.31

$$\therefore h_o = \frac{1}{r_{ob}} = \frac{1}{850k(101)} = \frac{1}{85M}$$

Figure 48.32

$$h_f = h_{fe}.h_{fb} = 100 \times 0.99 = 99 = Current\ Gain;$$

Figure 48.33

$$\mu_f = g_m r_o = \frac{85000{,}000}{250} = 340{,}000$$

Figure 48.34

$$Hybrid\ \pi\ parameters\ of\ Q_2$$

Figure 48.35

$$r_\pi = \frac{\beta_o}{g_m} = 25k, g_m = \frac{1}{250}; r_o = 850k; \mu_f = \frac{850000}{250} = 3400$$

Figure 48.36

]
(8)Find the midband gain and

$$\omega_h$$

Figure 48.37

of a CASCODE amplifier.
Given β_{fo}=100, f_T=500MHz, Cμ=0.5pF,r_x=250Ω, R_S=882Ω,R_L=4.12kΩ.
Q point(1.6mA,3V)for Q2.
[Answer:–151, 10MHz].

$$\omega_h = \frac{1}{r_{\pi 01}\left[C_\pi + 2C_\mu\right] + (r_x + R_L)C_\mu}$$

Figure 48.38

In CE configuration same transistor will give 1.56 MHz upper cut off frequency.
(9)Find the midband gain and f_H for a CB amplifier .Given β_{fo}=100,f_T=500MHz,Cμ=0.5pF,r_x =250Ω.
Q point(0.1mA,3.5V).
[ANSWER: 48, 10.7MHz]

Chapter 49

AE_Tutorial8_MOSFET&JFET[1]

AE_TUTORIAL 8_MOSFET&JFET

Tutorial on NMOS (TRIODE REGION)

(1)Calculate K_n'' for a NMOSFET with μ_n= 500

$$\frac{cm^2}{V-sec}$$

Figure 49.1

and T_{ox}=25nm

Solution: $K_n''= \mu_n C_{ox}''= \mu_n$

$$\frac{\epsilon_r \epsilon_o}{T_{ox}}$$

Figure 49.2

$$\therefore Kn''$$

Figure 49.3

=

[1]This content is available online at <http://cnx.org/content/m31760/1.2/>.

$$\left(500\ \frac{cm^2}{V-sec}\right)\times$$

Figure 49.4

$$\left(3.9\times 8.854\times 10^{-14}\ \frac{F}{cm}\right)\times\frac{1}{25\times10^{-9}\times100\ cm}$$

Figure 49.5

=

$$\frac{500\times3.9\times8.854\times10^{-14}}{25\times10^{-8}}\ \frac{F}{V-sec}=(69.1\times10^{-6})\frac{Q}{V^2sec}$$

Figure 49.6

$$\mathrm{Kn''}=69.1\ \frac{\mu A}{V^2}$$

Figure 49.7

; μ_n in bulk is 1500

$$\frac{cm^2}{V-sec}$$

Figure 49.8

but in 2D sheet it is only 500

$$\frac{cm^2}{V-sec}$$

Figure 49.9

(2)A NMOSFET has K_n'=50

$$\frac{\mu A}{V^2}$$

Figure 49.10

. What is the value of K_n if

W	20μm	60μm	10μm
L	1μm	3μm	0.25μm

Table 49.1

Answer: $K_n = K_n'$

$$\left(\frac{W}{L}\right)$$

Figure 49.11

= 1000

$$\frac{\mu A}{V^2}$$

Figure 49.12

, 1000

$$\frac{\mu A}{V^2}$$

Figure 49.13

, 2000

$$\frac{\mu A}{V^2}$$

Figure 49.14

(3)Calculate the Drain current in NMOS FET if V_{GS}=0, 1, 2, 3V;When V_{DS}=0.1V and W=10μm, L=1μm, V_{Th}=1.5V and K_n'=250

$\frac{\mu A}{V^2}$. What is the value of Kn?

Figure 49.15

Answer:

$$I_D = K_n\left(V_{GS} - V_{TN} - \frac{V_{DS}}{2}\right) \text{ where Kn} = 250\frac{\mu A}{V^2}$$

Figure 49.16

Expanding K_n and rearranging the terms,

$$I_D = \left[(C''_{ox}W)\left(V_{GS} - V_{TN} - \frac{V_{DS}}{2}\right)\right]\left(\mu_n \frac{V_{DS}}{L}\right)$$

Figure 49.17

Where

- $C''_{ox}W$ *is the capacitance per unit length*

Figure 49.18

- $\mu_n \frac{V_{DS}}{L}$ *is the Drift velocity in the channel* $(\mu_n E)$

Figure 49.19

.

- $(C''_{ox} W)\left(V_{GS} - V_{TN}\frac{V_{DS}}{2}\right)$ *is the average charge per unit length*

Figure 49.20

because average channel voltage =

$$\frac{V_{DS}}{2}$$

Figure 49.21

V_{DS}=0.1V				
V_{GS}	0	1V	2V	3V
I_{DS}	0	0	11.3μA	36.3μA

Table 49.2

(4)What is the region of operation and drain current of an NMOSFET having V_{TN}=1V,K_n=1

$$\frac{\mathbf{mA}}{\mathbf{V^2}}$$

Figure 49.22

,λ=0.02 V^{-1}

For (a)Vgs =0V,Vds=1V, (b)Vgs=2V, Vds=0.5V, (c)Vgs=2V, Vds=2V; Ans: (a) device is cutoff, drain current =0; (b) device is in triode region, drain current is 325uA; (c) device is in pentode region, drain current is 520uA;

(5)

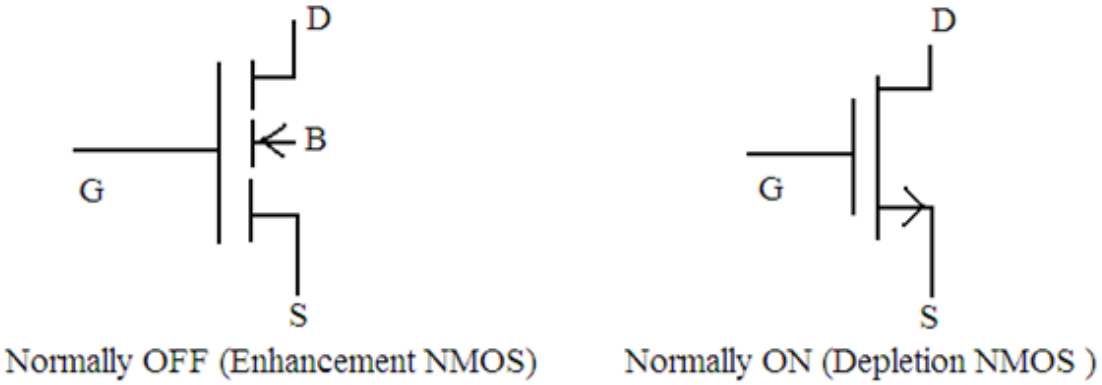

Figure 1. Symbol of (E)NMOS and (D)NMOS. Broken line means normally-off and continuous line means normally-on device.

Figure 49.23

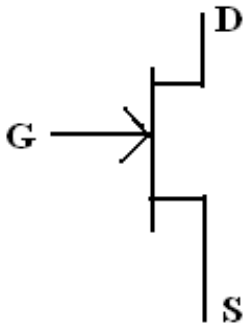

Figure 2. Symbol of nJFET

Figure 49.24

In Triode region:

$$I_{DS} = \frac{2I_{DSS}}{V_P^2}(V_{GS} - V_P - \frac{V_{DS}}{2})V_{DS}$$

Figure 49.25

for $V_{GS} \geq V_P$ and V_{GS} - $V_P \geq V_{DS} \geq 0$;
In Pentode region:

$$I_{DS} = I_{DSS}(1 - \frac{V_{GS}}{V_P})^2$$

Figure 49.26

for $V_{DS} \geq V_{GS}$ - $V_P \geq 0$;
Here I_{DSS} =

$$I_{DSS} = \frac{K_n}{2} V_P^2$$

Figure 49.27

Or

$$K_n = \frac{2I_{DSS}}{V_P^2}$$

Figure 49.28

The pinch off voltage ranges from 0 to -25V and I_{DSS} can range from 10μA to 10A.
If channel length modulation is included:

$$I_D = I_{DSS}\left(1 - \frac{|V_{GS}|}{|V_p|}\right)^2 (1 + \lambda |V_{DS}|)$$

Figure 49.29

---

(6) Calculate the drain current for NMOS FET operating at V_{GS}=5V, V_{DS}=10V and V_{TN}=1V,K_n=1

$$\frac{mA}{V^2}$$

Figure 49.30

,λ=0.02 V^{-1} and λ=0.
[Answer I_D=9.6mA with λ=0.02V^{-1} and I_D=8.0mA with λ=0]
(7)Calculate the drain current for NMOS FET operating at V_{GS}=5V, V_{DS}=10V and V_{TN}=1V, K_n=25

$$\frac{\mu A}{V^2}$$

Figure 49.31

, and λ=0.01 V^{-1}]

V_{GS}	V_{DS}	I_D
4V	5V	?
5V	10V	?

Table 49.3

[Answer: 118μA, 220μA]

Chapter 50

AE_Tutorial 9_Multistage Amplifiers[1]

AE_TUTORIAL 9_ MULTISTAGE AMPLIFIERS.

Band Width Shrinkage Factor

n	$\sqrt{2^{\frac{1}{n}}-1}$
1	1
2	0.644
3	0.510
4	0.435
5	0.368
6	0.350
7	0.323

Table 50.1

(1)

[1]This content is available online at <http://cnx.org/content/m31762/1.1/>.

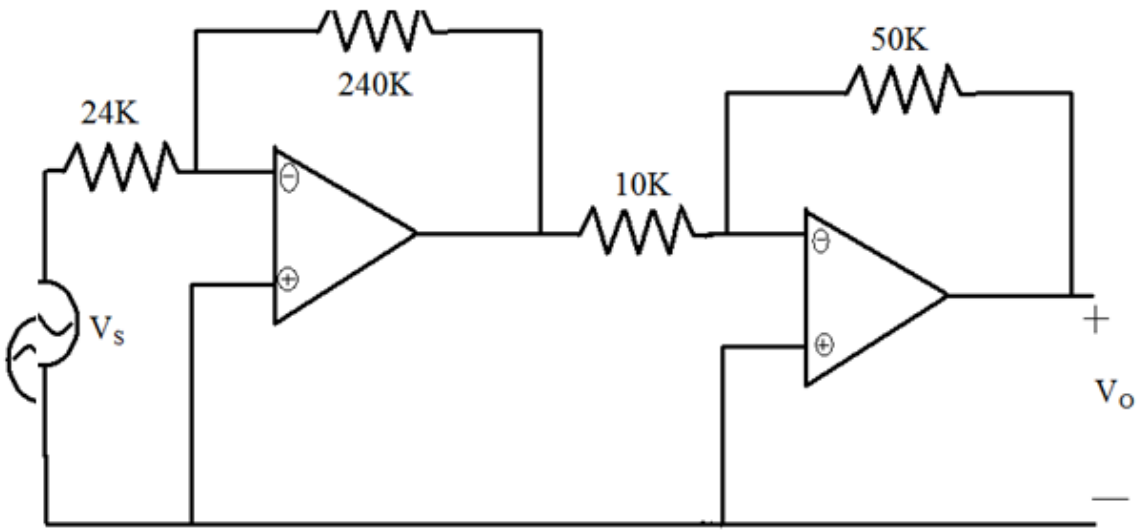

Figure 1. Two-stage Amplifier. Two inverting amplifiers have been cascaded.

Figure 50.1

Determine Avo and overall B.W. ; Assume f_u=1 MHz.
{Answer: A_{vo}=50, $(BW)_{overall} \sim (0.644)\times 10^5$ Hz}
Solution:

$$\frac{v_o}{v_1} = -\left[\frac{50}{10}\right], \frac{v_1}{v_s} = -\left[\frac{240}{24}\right]$$

Figure 50.2

$$\therefore \frac{v_o}{v_s} = \frac{v_o}{v_1}\frac{v_1}{v_s} = -(5)(-10) = 50$$

Figure 50.3

$$\therefore A_{Vo} = 50$$

Figure 50.4

$$(B.W.)_{overall} = (B.W.)_{single}(B.W.Shrinkage\ Factor)$$

Figure 50.5

For stage1, BW=

$$\frac{10^6}{10} = 10^5$$

Figure 50.6

For stage2, BW=

$$\frac{10^6}{5} = 2 \times 10^5$$

Figure 50.7

$$\therefore (B.W.)_{overall} \sim (10^5)\sqrt{2^{\frac{1}{2}} - 1} \sim (0.644 \times 10^5)$$

Figure 50.8

---

(2)

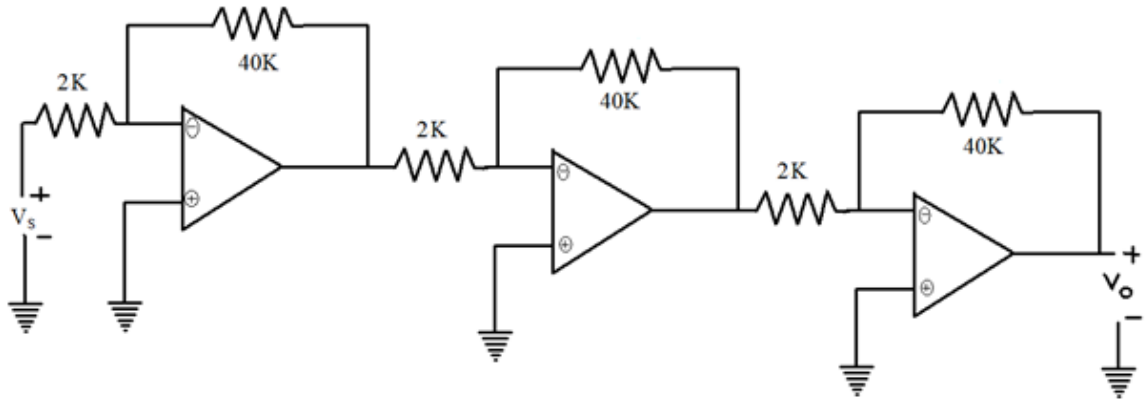

Figure 2. Three stage cascading of Inverting Amplifiers.

Figure 50.9

3 stage cascaded amplifier: Assume f_u=1 MHz. **Determine: overall B.W and overall gain.**
{ $A_{vo}=(-20)^3$; BW=$(10^6/20)(0.510)$Hz}
For one stage, voltage gain= -40/2= - 20V= V_o/V_1

$$\therefore Overall\ Voltage = \left(\frac{V_0}{V_1}\right) \times \left(\frac{V_1}{V_2}\right) \times \left(\frac{V_2}{V_5}\right) = \left(\frac{V_0}{V_5}\right) = (-20)(-20)(-20)$$

Figure 50.10

$$A_{V_O} = -8000$$

Figure 50.11

$$(B.W.)_{overall} = (B.W.)_{single}(B.W.Shrinkage\ Factor)$$

Figure 50.12

For stage1 BW=

$$\frac{10^6}{20} = 5 \times 10^4$$

Figure 50.13

For stage2 BW=

$$\frac{10^6}{20} = 5 \times 10^4$$

Figure 50.14

For stage3 BW=

$$\frac{10^6}{20} = 5 \times 10^4$$

Figure 50.15

$$(B.W.)_{overall} = 5 \times 10^4\sqrt{2^{1/3} - 1} \sim (5 \times 10^4)(0.510)$$

Figure 50.16

(3)**Design a multistage amplifier that meet the following specification**

$$(A_{V\,O})_{overall} = 86\ dB \pm 1dB;$$

Figure 50.17

$$R_{in} > 10k\Omega$$

Figure 50.18

$$R_{out} \sim 0.01\Omega$$

Figure 50.19

$$f_h \geq 75kHz$$

Figure 50.20

Given

$$A_{V\,open} = 10^5\ ; R_{id} = 10^9\Omega; R_{out} = 50\Omega; GBP = 1\ MHz$$

Figure 50.21

Solution:
86 dB = 20 log(

$$A_{V_{overall}}$$

Figure 50.22

)

$$A_{V_{overall}} = 10^{4.3} = 10^4 10^{0.3} = 40{,}000$$

Figure 50.23

Let us choose 3 stages:
Each stage with gain 40, closed loop B.W. of single stage $=10^6/40=25$ kHz

---

$$Therefore\ (B.W.)_{overall} = (B.W.)_{single}(B.W.Shrinkage\ Factor)$$

Figure 50.24

$$B.W.Shrinkage\ Factor = \sqrt{2^{1/3} - 1}$$

Figure 50.25

$$(B.W.)_{overall} = (25\ kHz) \times (0.5) = 12.5kHz$$

Figure 50.26

This design does not meet our specification:

Therefore we choose 3 stages each with gain as 30.

$$Therefore\ (B.W.)_{single} = \frac{10^6}{30} = 33.3\ kHz$$

Figure 50.27

$$Therefore\ (B.W.)_{overall} = (B.W.)_{single}(B.W.Shrinkage\ Factor) = (300\ kHz)\sqrt{2^{1/3} - 1}$$
$$= 15.0\ kHz$$

Figure 50.28

$$Since\ R_{in} = R_1 = 10\ k\Omega\ \ therefore\ R_2 = 300k\Omega$$

Figure 50.29

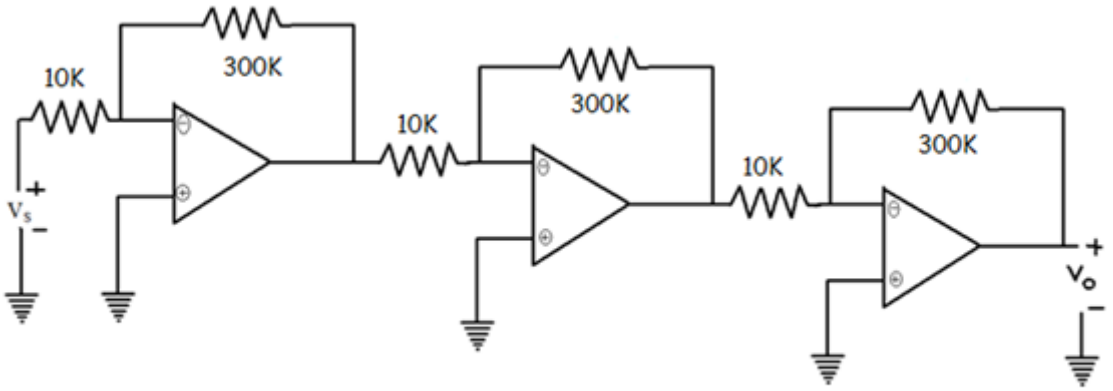

Figure 3. Three-stage cascaded Inverting Amplifier.

Figure 50.30

This multistage amplifier does not meet the given specifications.
We will have to use a higher performance Op Amp of f_u = 10MHz to meet the above specifications.
4)

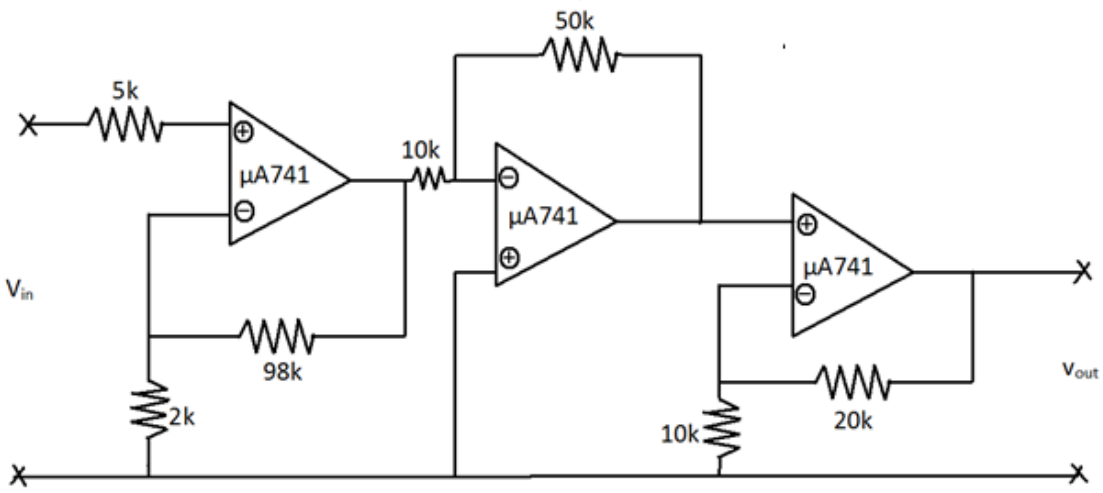

Figure 4. 3-stage cascaded amplifier. NonInv-Inv-NonInv cascading.

Figure 50.31

(a)Determine the flat band gain and BW of each stage.

(b)Write the expression for each stage including the effect of ω_h.
(c)Plot the asymptotic plot.
(d)Determine the overall gain and the overall BW.
Solution:-
(a)&(b)1 st stage is a non-inverting amplifier.

$$A_{V_1}(j\omega) = \frac{\left(1 + \frac{98}{2}\right)}{\left(1 + j\frac{\omega}{\omega_{h1}}\right)}$$

Figure 50.32

2^{nd} stage is Inverting amplifer.

$$A_{V_2}(j\omega) = \frac{-\left(50k/10k\right)}{\left(1 + j\frac{\omega}{\omega_{h_2}}\right)}$$

Figure 50.33

3^{rd} stage is a non-inverting amplifier.

$$A_{V_3}(j\omega) = \frac{\left(1 + 20k/10k\right)}{\left(1 + j\frac{\omega}{\omega_{h_3}}\right)}$$

Figure 50.34

$$f_{h_1} \times \left(1 + \frac{98}{2}\right) = 10^6$$

Figure 50.35

$$f_{h_1} = \frac{10^6}{50} = 20\ kHz(Dominant\ Pole)$$

Figure 50.36

$$f_{h_2} \times \left(\frac{50}{10}\right) = 10^6 \qquad f_{h_2} = \frac{10^6}{5} = 167\ kHz$$

Figure 50.37

$$f_{h_3} \times \left(1 + \frac{20}{10}\right) = 10^6 \qquad f_{h_3} = \frac{10^6}{3} = 333\ kHz$$

Figure 50.38

Lowest pole is the dominant pole in LPF.
(c)Flat band Gain=50 X 5 X3 =750
In db the gain is $20\log_{10}(750) = 57.5$ dB

$$A_V(j\omega)|_{overall} = \frac{50}{\left(1 + j\frac{\omega}{\omega_{h_1}}\right)} \times \frac{-5}{\left(1 + j\frac{\omega}{\omega_{h_2}}\right)} \times \frac{3}{\left(1 + j\frac{\omega}{\omega_{h_3}}\right)}$$

Figure 50.39

$$\frac{1}{\omega_h{}^2} = \frac{1}{\omega_{h_1}{}^2} + \frac{1}{\omega_{h_2}{}^2} + \frac{1}{\omega_{h_3}{}^2} \approx \frac{1}{\omega_{h_1}{}^2}$$

Figure 50.40

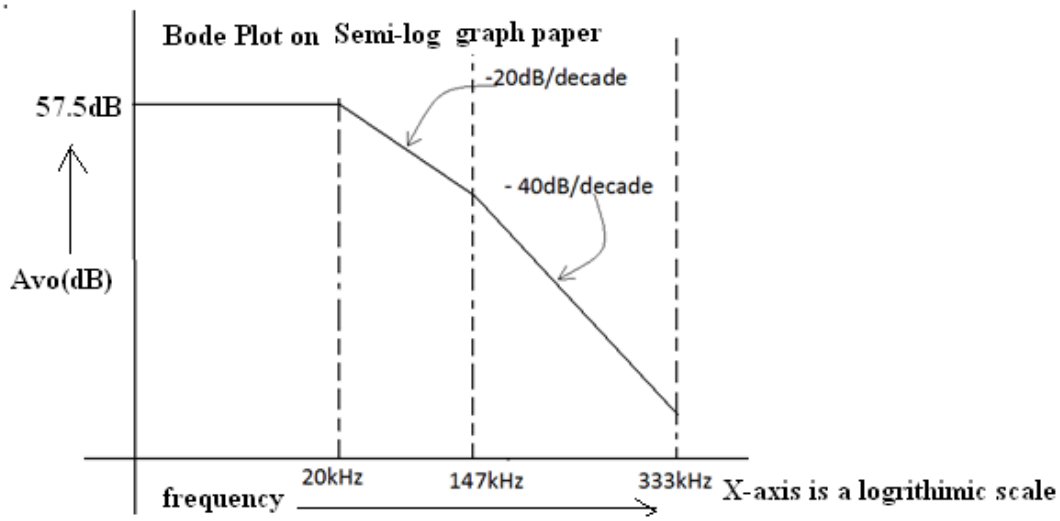

Figure 5. Bode Plot of the magnitude of the Voltage Gain in Problem 4

Figure 50.41

Chapter 51

AE_Tutorial 10_Noise[1]

AE_TUTORIAL NO 10_Problems on NOISE PARAMETRS.

Problem (1) *Calculate the available power per Hz of BW for a resistance at room temperature (T=290 K).Express in decibels with reference to 1mW(dBm) And with reference to 1 W(dBW).*

Solution: Available power per Hz =kT (W/Hz)

Power in W/Hz=kT=4 x 10^{-21} W/Hz

Power in dBm=10 log(4 x 10^{-21}/1 x 10-3)= -174dBm

Power in dBW= 10 log(4 x 10^{-21}/1)= -204dBW

PROBLEM(2) *Given one port network:*

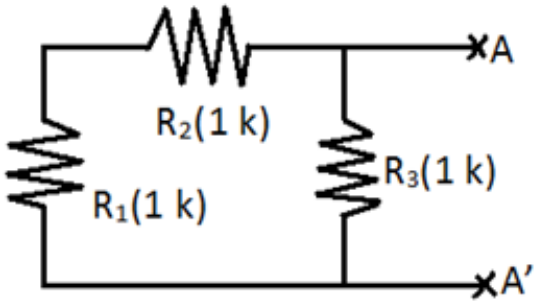

Figure 1. related to problem 2.

Figure 51.1

Determine <v n 2 > at AA' in BW=100kHz. Also determine the rms voltage at AA'.

SOLUTION: R_{eq} at AA'=R3||(R1+R2)

= 1K||(1K+1K)

= 1K||(2K)

= 1 x 2/ 1+2 =2/3 K

[1]This content is available online at <http://cnx.org/content/m32192/1.1/>.

Therefore $<v_n^2>|_{AA'} = (4kTB)R_{eq}|_{AA'} = (4 \times k \times 290 \times 100 \times 10^3) \times (2/3) \times 10^3$
$= 1 \times 10^{-12}(V)^2$
rms noise voltage=

$$\sqrt{< v_m^2 >} = 10^{-6}V = 1\mu V$$

Figure 51.2

PROBLEM(3) *In TV receiver the antenna is often mounted on a tall mast and long lossy cable is used to connect the antenna to the receiver. To overcome the effect of lossy cable, a pre amplifier is mounted on the antenna as shown in the figure.*

(a)Find the overall noise figure.

(b)Find the overall noise figure if pre-amplifier is omitted and gain of front end is increased by 20dB.Normally the NOISE FIGURE of the front end of the receiver is 16dB.

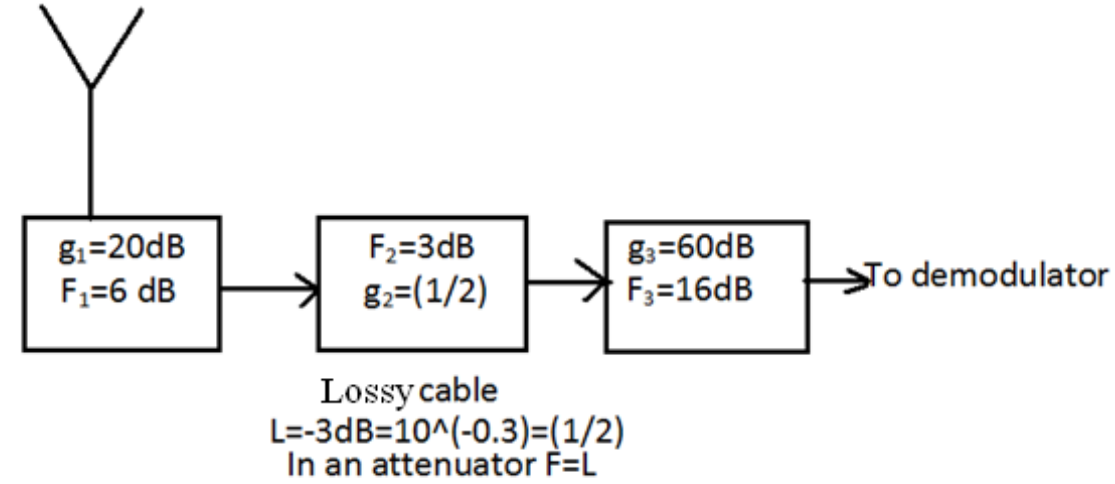

Figure 2. This figure relates to Problem 3.

Figure 51.3

Note: The first stage is the pre-amplifier kept at the top of the mast which carries the antenna. This pre-amplifier is supposed to compensate for the loss occurring while carrying the signal from the antenna to the front end of the receiver.

The second block represents the lossy cable.

The third block is the front end of the receiver which has a noise figure of 16dB.

Solution of Problem(3):

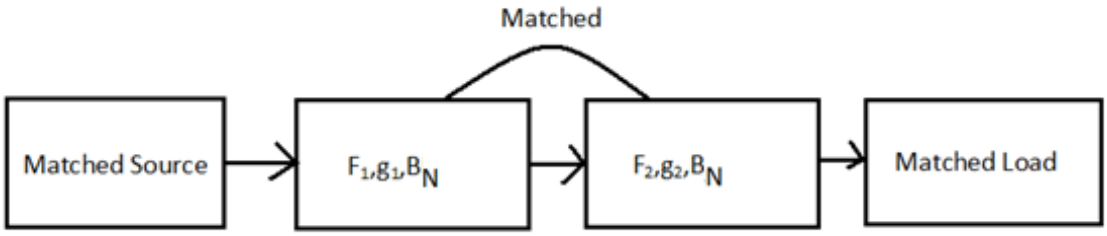

Figure 3. This is the block representation of Figure 2.

Figure 51.4

The noise figure of 2 stages is given by the formula:

$$F = F_1 + \frac{F_2 - 1}{g_1}$$

Figure 51.5

Generalizing this result we get

$$F = F_1 + \frac{F_2 - 1}{g_1} + \frac{F_3 - 1}{g_1 g_2} + \frac{F_4 - 1}{g_1 g_2 g_3} + - - - -$$

Figure 51.6

Therefore the overall Noise figure is largely determined by the Noise Figure of the FIRST stage and the gain of the 1st stage. F1 should be very low and the gain

$$g_1$$

Figure 51.7

should be very high.
Part(a)

$$F_1 = 6dB \rightarrow F_1 = 10^{0.6} = 4$$

Figure 51.8

$$g_1 = 20dB \rightarrow g_1 = 10^2 = 100$$

Figure 51.9

$$F_2 = 3dB \rightarrow F_2 = 10^{0.3} = 2 = L$$

Figure 51.10

$$g_2 = \frac{1}{L} = \frac{1}{2}$$

Figure 51.11

$$F_3 = 16dB \rightarrow F_3 = 10^{1.6} = 40$$

Figure 51.12

$$g_3 = 60dB \rightarrow g_3 = 10^6$$

Figure 51.13

When all three stages are considered:

$$F_{overall} = F_1 + \frac{F_2 - 1}{g_1} + \frac{F_3 - 1}{g_1 g_2}$$

Figure 51.14

$$= 4 + \frac{2-1}{100} + \frac{40-1}{100\left(\frac{1}{2}\right)} = 4.79$$

Figure 51.15

$$F_{overall} = 4 + 0.01 + 3.9 \times 10^{-7} = 4.79$$

Figure 51.16

$$F_{overall} in\ dB = 10 \log_{10} 4.79 = 6.8 dB$$

Figure 51.17

Part(b) Without the pre-amplifier

$$F = F_2 + \frac{F_3 - 1}{g_2} = 2 + \frac{40 - 1}{(1/2)} = 80 = 19 dB$$

Figure 51.18

In part(b), we have a very bad overall noise figure resulting into a very poor reception of the TV station tuned to.

To overcome this problem we always mount a pre-amplifier on the tall mast which carries the antenna.

Chapter 52

AE_Tutorial 11_Power Amplifiers[1]

AE_Tutorial 11_Power Amplifiers(Audio)

Problems have been taken from Microelectronic Circuits_Analysis & Design by Rashid, Publisher Thomson(Indian Edition),1999.Chapter 14_Power Amplifiers.

Problem 1. Design of a transformer coupled Class A Amplifier.

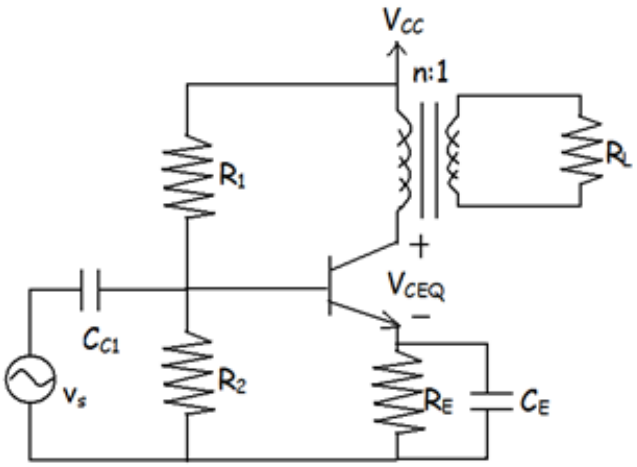

Figure 1 . Transformer coupled Class A CE Amplifier.

Figure 52.1

Refer to Figure 1.Design a Transformer-coupled Class A CE Amplifier to give an output power of P_L = 10W at a load resistance of 4Ω speaker. Assume DC bias of V_{CC} =12V. The BJT has short circuit dc as

[1]This content is available online at <http://cnx.org/content/m32317/1.1/>.

well as incremental current gain of 100.

Solution.

Step 1. Maximum Voltage Swing = $V_{CE}(max) = 2V_{CC}$ = 24 V;

Step 2. Whatever power is dissipated by BJT under no signal, half of it at most will be transferred to the load under full signal condition.

Therefore Collector Power Dissipation under no signal condition is $P_C = 2\ P_L$ = 20W= $I_{CQ} \times V_{CC} = I_{CQ} \times 12$

Therefore I_{CQ} = 20/12 = 1.67A;

In Figure 12 in AE_Lecture 10_Part2, the load line graphical interpretation of Class A amplifier is given.

The slope of the dynamic load line is = $-(1/R_L') = -(I_{CQ}/V_{CC})$;

Therefore R_L' = 12/1.67 = 7.19Ω;

Step 3. $R_L' = n^2 \times R_L = n^2 \times 4\Omega$ where n = turns ratio = primary coil no. of turns/ secondary coli number of turns;

Therefore n = $\sqrt{(7.19/4)}$ =1.34;

Step 4. Peak Collector Current = $2I_{CQ}$ = 3.34A;

Step 5. The quiescent base current = I_{CQ}/β_F = 1.67/100 A =16.7mA;

The biasing network has to be designed to achieve the above quiescent point (1.67A, 12V).

Problem2. Finding the efficiency and power dissipation of a complementary push-pull amplifier.

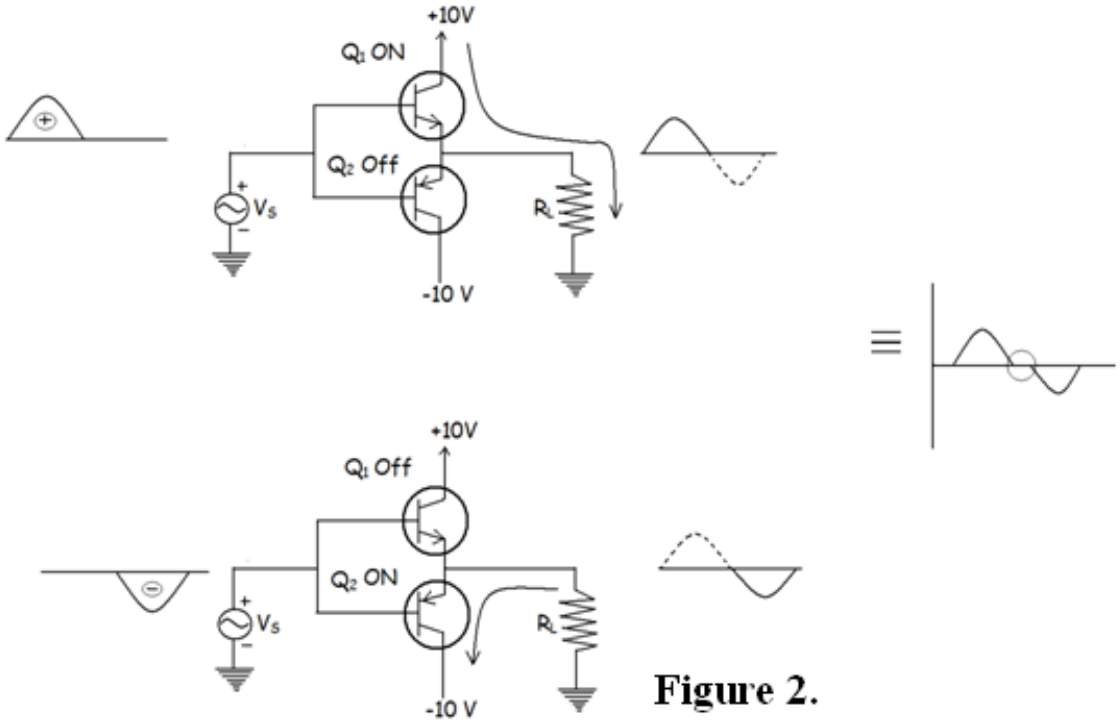

Figure 2.

Figure 52.2

Refer to Figure 2 .

(a) Calculate the efficiency and power dissipation of each transistor in the complementary push-pull output stage if V_{CC} = +12V and V_{EE} =-12V and R_L = 50Ω. The parameters of the transistors are: β_{f0} = β_F = 100, V_{CE}(sat)=0.2V and V_{BE}(on)=0.72V.

(b) Use Orcad simulation to plot the transfer characteristic.

Solution.

Peak load voltage in positive half is = V_P =V_{CC} − $V_{CE(sat)}$= (12-0.2)= 11.8V;

Similarly negative peak voltage = -11.8 V.

Positive peak current = magnitude of negative peak current = V_P /R_L = 11.8/50 = 0.236A

Under signal condition average current drawn from one battery = I_P/π since each battery supplies half wave rectified current. Hence power supplied by one battery is = $(I_P/\pi)\times V_{CC}$;

Power supplied by two batteries = P_S = $2(I_P/\pi)\times V_{CC}$ = $(2\times 0.236\times 12)/\pi$ = 1.803W;

Output power across the load = P_L = $(I_P/\sqrt{2})\times (V_P/\sqrt{2})$ = 1.392W;

Power conversion efficiency = 1.392/1.803= 77.2%;

Power dissipation in each transistor is = (P_S - P_L)/2 = 206mW.

Problem 3.Design a transformer- coupled Class B Amplifier.

Refer to Figure 3.

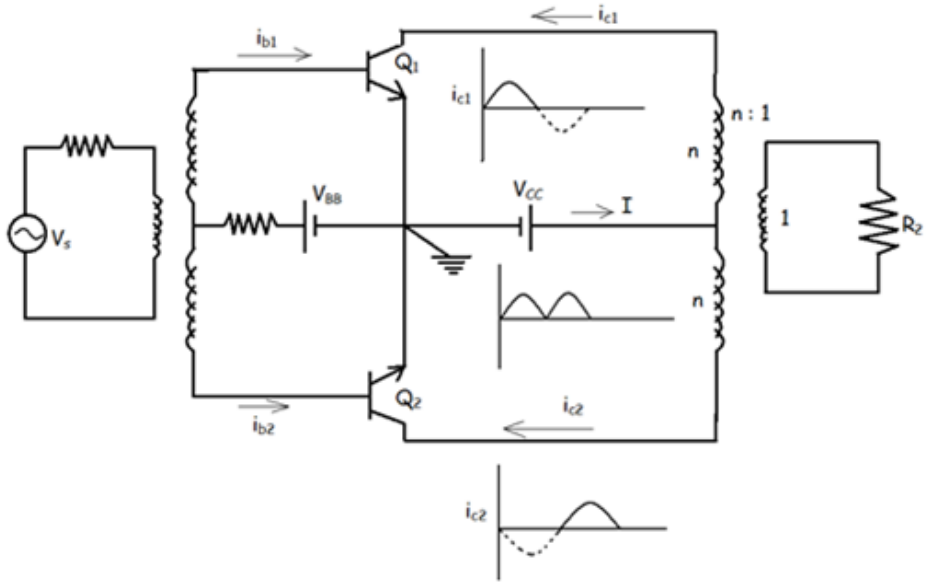

Figure 3. Physical operation of Class B push-pull amplifier.

Figure 52.3

Design a transformer-coupled Class B push-pull amplifier to supply a maximum output power of P_L(max) =10W at a load resistance of R_L = 4Ω. Assume a DC supply of 15V and current gain 100 and $V_{BE(ON)}$=0.7V.

Solution:

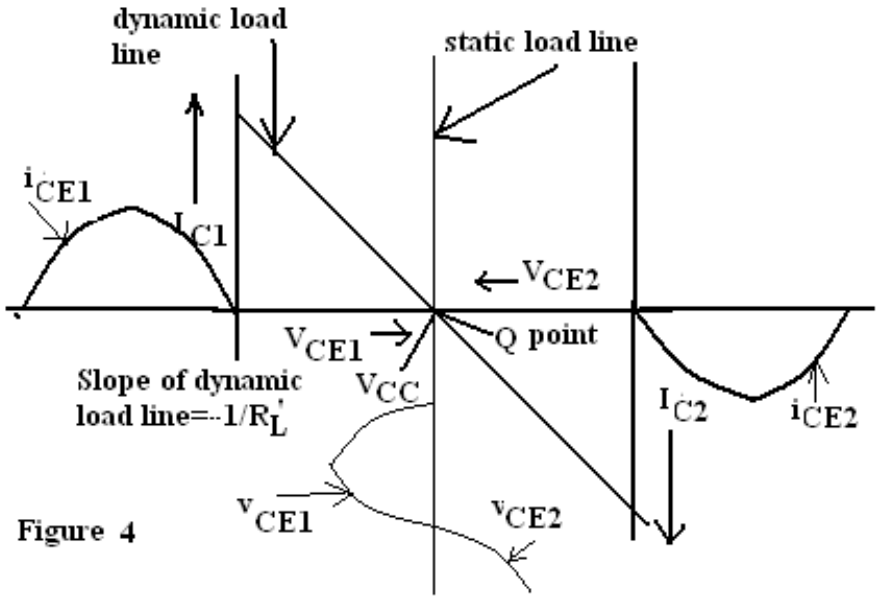

Figure 52.4

Step1

Maximum voltage swing across either of BJTs =V_{CE}(max)=2V_{CC} = 30V;

Step 2 Effective load resistance as seen by the primary side is $R_L' = n^2 R_L$.

P_L(max) = $V_{CC}^2/(2\ R_L')$ $\leftrightarrow$ this is because there is a sinusoidal voltage swing across the reflected load R_L' of amplitude V_{CC}.

Therefore $R_L' = V_{CC}^2/(2\ P_L(\text{max})) = 15^2/(2\times 10) = 11.25\Omega$;

Ste 3. Calculation of Peak collector current:

I_C(peak) = V_{CC}/R_L' = 15/11.25 =1.33A;

Step 3. Average Current supplied by each transistor.

Each transistor supplies half wave rectified current.

Hence I_C (average) = I_C(peak)/π = 1.33/3.14= 0.424A;

Total average current supplied by the battery= 2 I_C (average)=0.848A;

Step 4. DC Power from the battery = V_{CC} ×2 I_C (average) =15×0.848 = 12.72W;

Step 5. Average Collector Power Dissipation for both transistors is given by :

$2P_C = P_{DC} - P_L = [(2V_C(\text{peak})/\pi) \div R_L'] \times V_{CC} - V_C(\text{peak})^2/(2\ R_L')$;

Under Maximum Collector Power dissipation condition, V_C(peak) is not V_{CC} but $2V_{CC}/\pi$

And I_C(peak) = $2V_{CC}/(\pi\ R_L')$; Detailed analysis is given in Rashid's book.

Therefore $2P_C$ (max) = P_{DC} (max)− P_L (max)= $[(2\times(2V_{CC}/\pi))(1/\pi) \div R_L'] \times V_{CC} - (2V_{CC}/\pi)^2/(2\ R_L')$

= 4 $V_{CC}^2/(\pi^2\ R_L')$ - $2V_{CC}^2/(\pi^2\ R_L')$ = $2V_{CC}^2/(\pi^2\ R_L')$=$(2/\pi^2)\times 2(V_{CC}^2/(2\ R_L')$=$(4/\pi^2)$ P_L(max);

Therefore P_C (max) = $(2/\pi^2)$ P_L(max) = $(2/\pi^2)\times 10$ = 2W;

Step 6. Required turns ratio: $R_L' = n^2 \times R_L$;

Therefore n =$\sqrt{(R_L'/R_L)}$ = $\sqrt{(11.25/4)}$ =1.68.

Chapter 53

AE_Tutorial 12_Oscillators[1]

AE_Tutorial 12. Problems on OSCILLATORS

Problems have been taken from:

"Microelectronic Circuit Design" by R.C.Jaeger and T.N. Blalock, 2nd Edition, McGraw Hill,2006.

"Microelectronic Circuits- Analysis & Design", Muhammad H. Rashid, Thomson, Indian Edition, 1999.

Problem (1)Wien Bridge Oscillator

[1]This content is available online at <http://cnx.org/content/m32489/1.1/>.

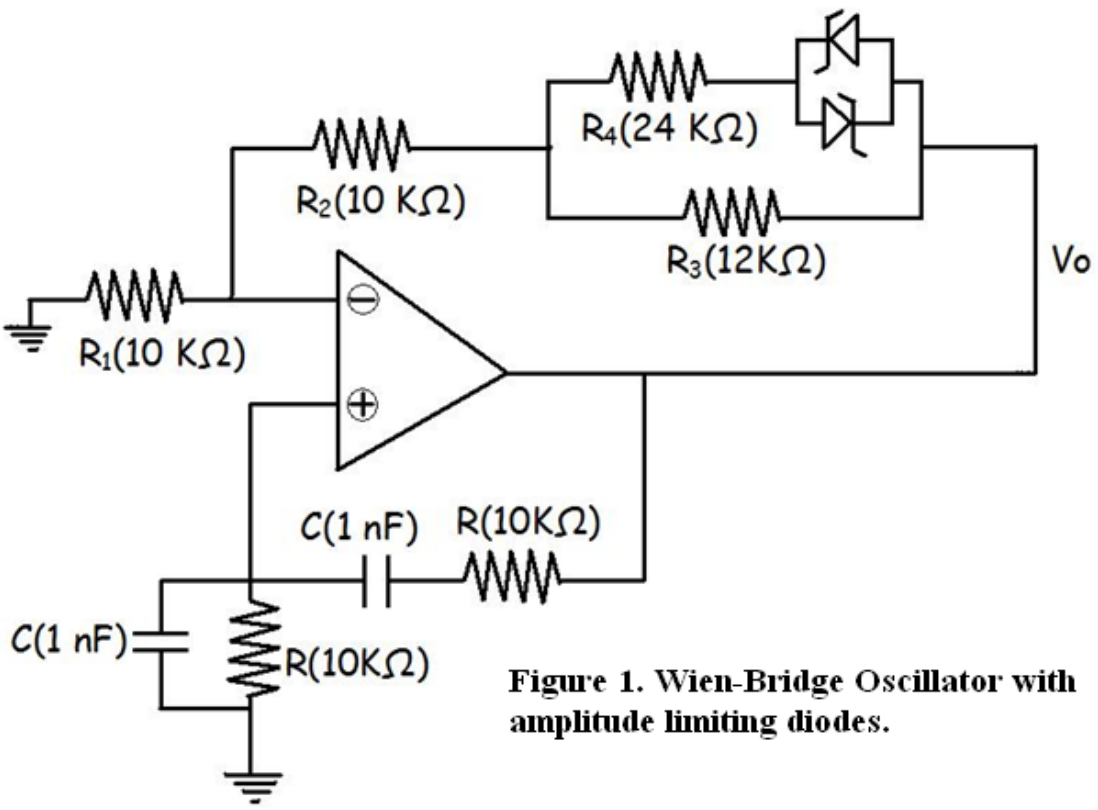

Figure 1. Wien-Bridge Oscillator with amplitude limiting diodes.

Figure 53.1

$$(v_o)_{max} = \frac{3V_D}{\left(2 - \frac{R_2}{R_1}\right)\left(1 + \frac{R_4}{R_3}\right) - \left(\frac{R_4}{R_1}\right)} \quad where \quad \frac{R_2}{R_1} < 2$$

Figure 53.2

$$\omega_o = \frac{1}{RC}$$

Figure 53.3

This is called Diode amplitude stabilization of a Wien Bridge Oscillator.
Determine frequency of oscillation & the amplitude of the oscillation.
[Ans:- 9.95 kHz,3.0V]
When the diodes are off,the gain of the amplifier is

$$\left(1 + \frac{R_2 + R_3}{R_1}\right) \; where \; \frac{R_2 + R_3}{R_1} > 2$$

Figure 53.4

So that loop gain >1 and the oscillations grow.
When diode turn ON, the gain is

$$\left[1 + \left(\frac{R_2 + R_3 || R_4}{R_1}\right)\right] \; where \; \frac{R_2 + R_3 || R_4}{R_1} < 2$$

Figure 53.5

and the oscillations decay.
PROBLEM(2)

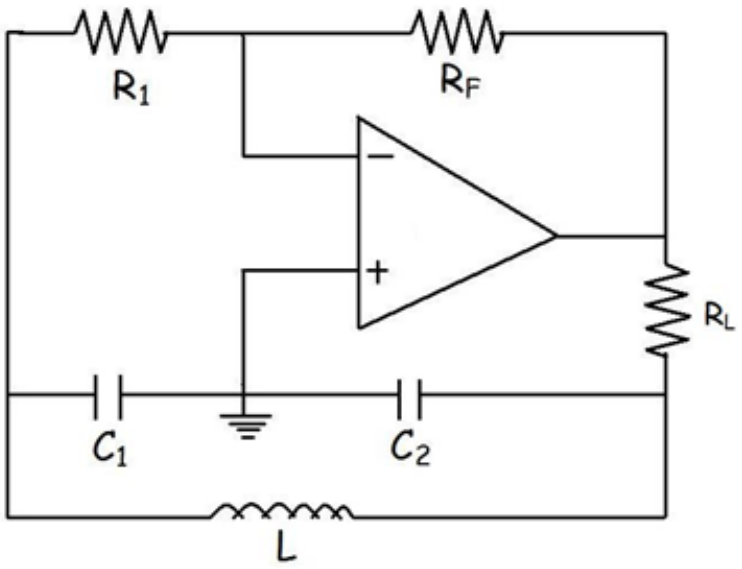

Figure 2. Circuit Diagram of Colpitts Oscillator.

Figure 53.6

$$g_m R_1 = \frac{C_2}{C_1} \quad ; \quad \frac{R_F}{R_L} = \frac{C_2}{C_1} = \frac{AR_1}{R_L} \; where \; A = 10$$

Figure 53.7

Design the Colpitt's for oscillation frequency

$$f_o = 150 \; kHz$$

Figure 53.8

Step(1) Choose

$$C_1 = 0.01\mu F \ \& \ C_2 = 0.1\mu F$$

Figure 53.9

$$\therefore \frac{C_2}{C_1} = \frac{0.1}{0.01} = 10$$

Figure 53.10

Step(2) Calculate L from

$$\omega_o = \frac{1}{\sqrt{L\left(\frac{C_1 C_2}{C_1 + C_2}\right)}}$$

Figure 53.11

$$\therefore L = \frac{C_1 + C_2}{{\omega_o}^2 C_1 C_2} = 124\mu H$$

Figure 53.12

Step(3) Calculate R_F & R_L.
Let R_L=100kΩ Therefore R_F=

$$\left(\frac{C_2}{C_1}\right) R_L = 1M\Omega$$

Figure 53.13

Step(4) Determine R_1_ _ _ _ _ _Let A=10

$$\frac{10R_1}{R_{I.}} = \frac{C_2}{C_1} = 10$$

Figure 53.14

$$\therefore R_1 = 100k\Omega$$

Figure 53.15

Step(5) Determmine g_m

$$g_m R_1 = \frac{C_2}{C_1}$$

Figure 53.16

$$g_m(100k) = 10$$

Figure 53.17

$$g_m = \left(\frac{1}{10}\right) mS = 0.1 \frac{mA}{V}$$

Figure 53.18

PROBLEM(3) Colpitts Oscillator Using BJT

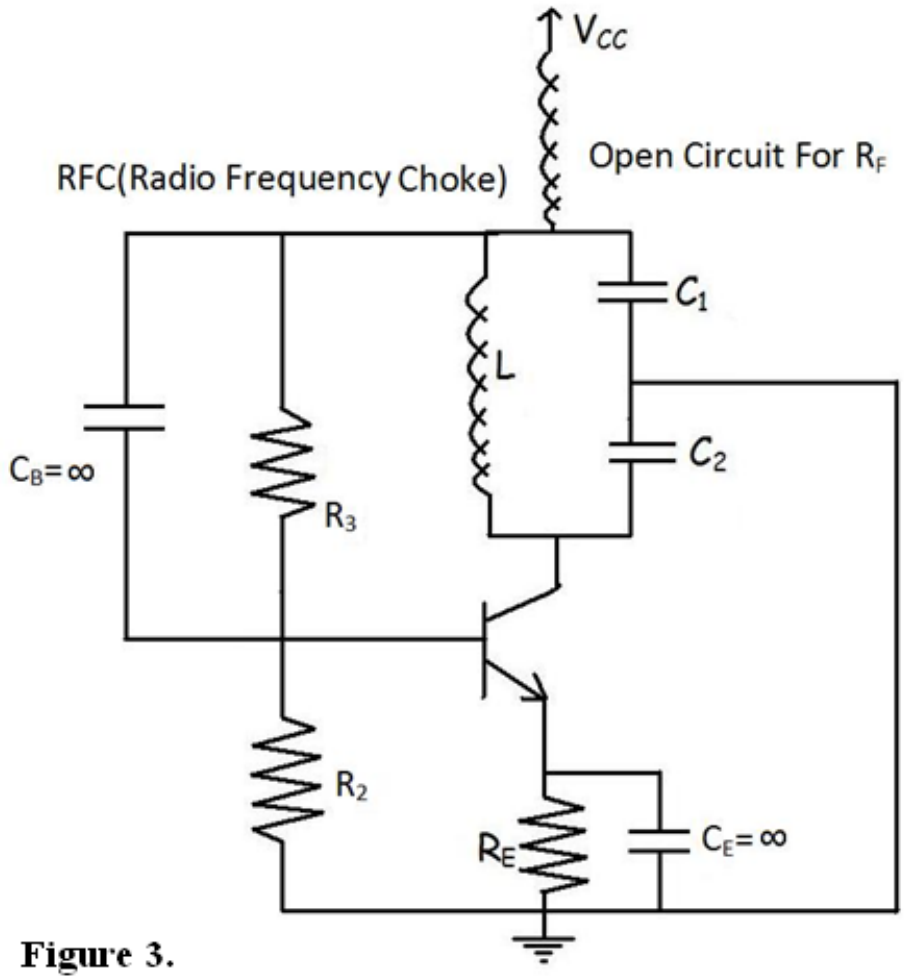

Figure 53.19

$$r_\pi = 1.1k\Omega; h_{fe} = 100; L = 1.5mH; C_1 = 1nF; C_2 = 99nF; R_L = 10k\Omega$$

Figure 53.20

Calculate (i) Frequency of oscillation.

(ii)Check the Barkhausen criteria.
(iii)Determine R_2.
Solution:-
RFC acts as a open circuit And C_B and C_E acts as a short circuit.
Therefore the Equivalent Circuit is :-

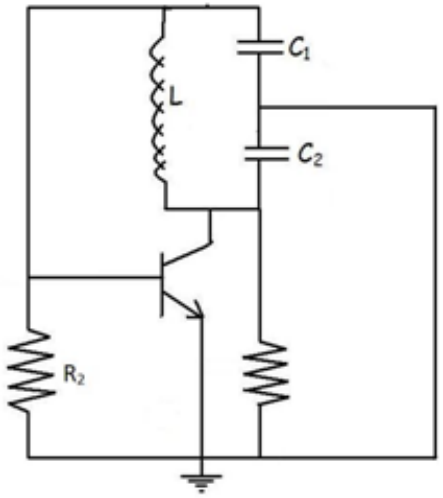

Figure 4. Colpitts Oscillator.

Figure 53.21

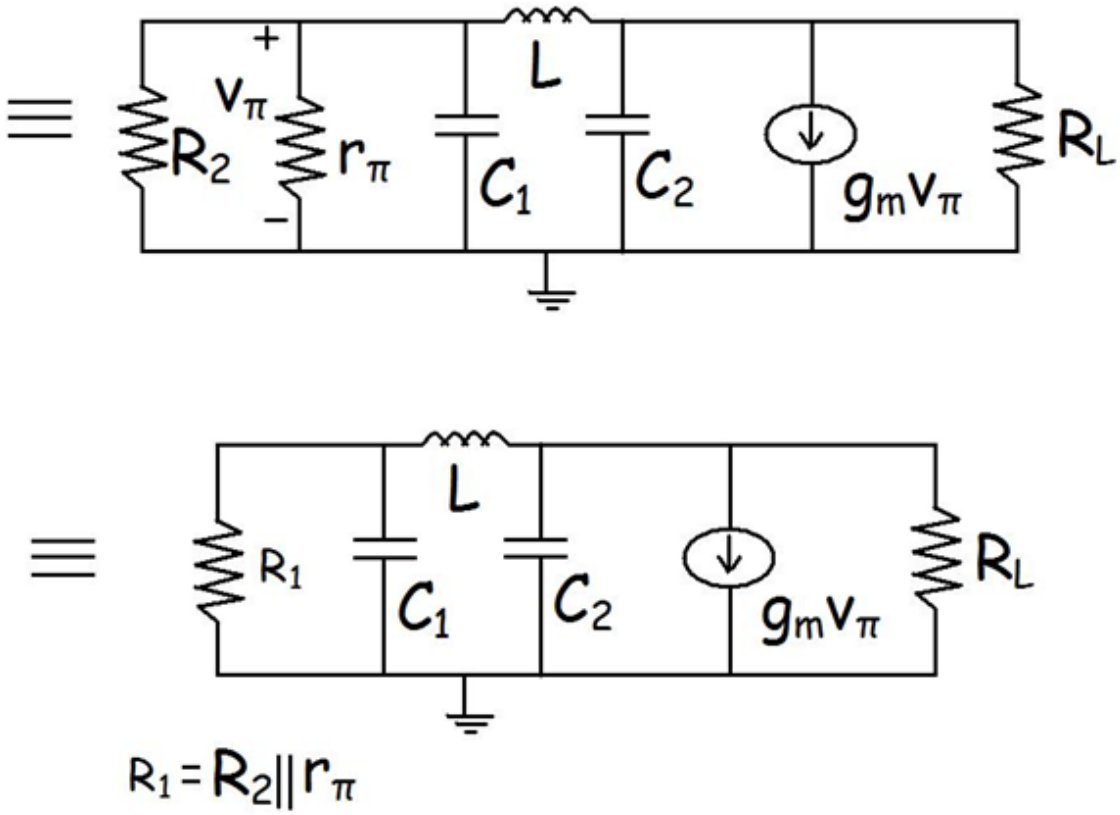

Figure 5. The incremental representation of Colpitts in Figure 4.

Figure 53.22

From the nodal equations we get equating the imaginary parts

$$\omega_o = \sqrt{\frac{C_1 + C_2}{C_1 C_2 L}} \quad \text{——(1)}$$

Figure 53.23

Equating Real parts we get

$$g_m R_1 = \frac{C_2}{C_1} + \frac{C_1}{C_2}\frac{R_1}{R_L} + \frac{L}{C_2 {R_L}^2} + \frac{L}{C_1 R_1 R_L}$$

Figure 53.24

For large values of

$$R_L$$

Figure 53.25

$$g_m R_1 = \frac{C_2}{C_1} \text{\_\_\_\_\_} (2)$$

Figure 53.26

Gain

$$|A_V| = |g_m R_L|$$

Figure 53.27

Subs

$$|A_V| = |g_m R_L|$$

Figure 53.28

in Eq(2)

$$g_m R_1 = \frac{A_V R_1}{R_L} = \frac{C_2}{C_1} - - - - - - - (3)$$

Figure 53.29

For

$$R_2 \gg r_\pi$$

Figure 53.30

$$R_1 = r_\pi || R_2 = r_\pi = \frac{h_{fe}}{g_m} - - - - - - - - - (4)$$

Figure 53.31

Sub (4) in (3)

$$g_m \frac{h_{fe}}{g_m} = \frac{A_V R_1}{R_L} = \frac{C_2}{C_1}$$

Figure 53.32

$$h_{fe} = \frac{C_2}{C_1} = \frac{99nF}{1nF} = 99$$

Figure 53.33

(i)This

$$h_{fe}$$

Figure 53.34

can be provided by BJT hence Barkhausen Criteria is satisfied
(ii)Frequency of oscillation=

$$f_o = \frac{1}{2\pi}\sqrt{\frac{C_1+C_2}{C_1C_2L}} = 130.6kHz$$

Figure 53.35

(iii)

$$R_1 = \frac{C_2}{C_1} \times \frac{1}{g_m} = \frac{99}{g_m} = 99\frac{r_\pi}{h_{fe}} = \frac{99\times 1.1k\Omega}{100}$$

Figure 53.36

$$R_1 = 1089\Omega = r_\pi || R_2$$

Figure 53.37

$$\therefore \frac{r_\pi R_2}{r_\pi + R_2} = 1089 \ \therefore R_2 = 108.9k\Omega$$

Figure 53.38

PROBLEM(4)LC-Tuned MOS Oscillator
Design an oscillator at

$$f_o = 110kHz, g_{ds} = 5\frac{mA}{V}\ ; r_d = 25k\Omega\ ; R_G = 10k\Omega$$

Figure 53.39

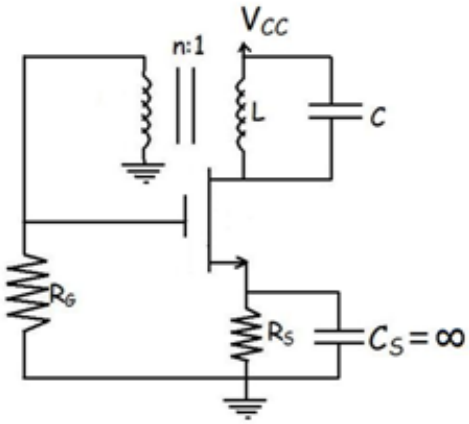

Figure 6. Tuned Oscillator

Figure 53.40

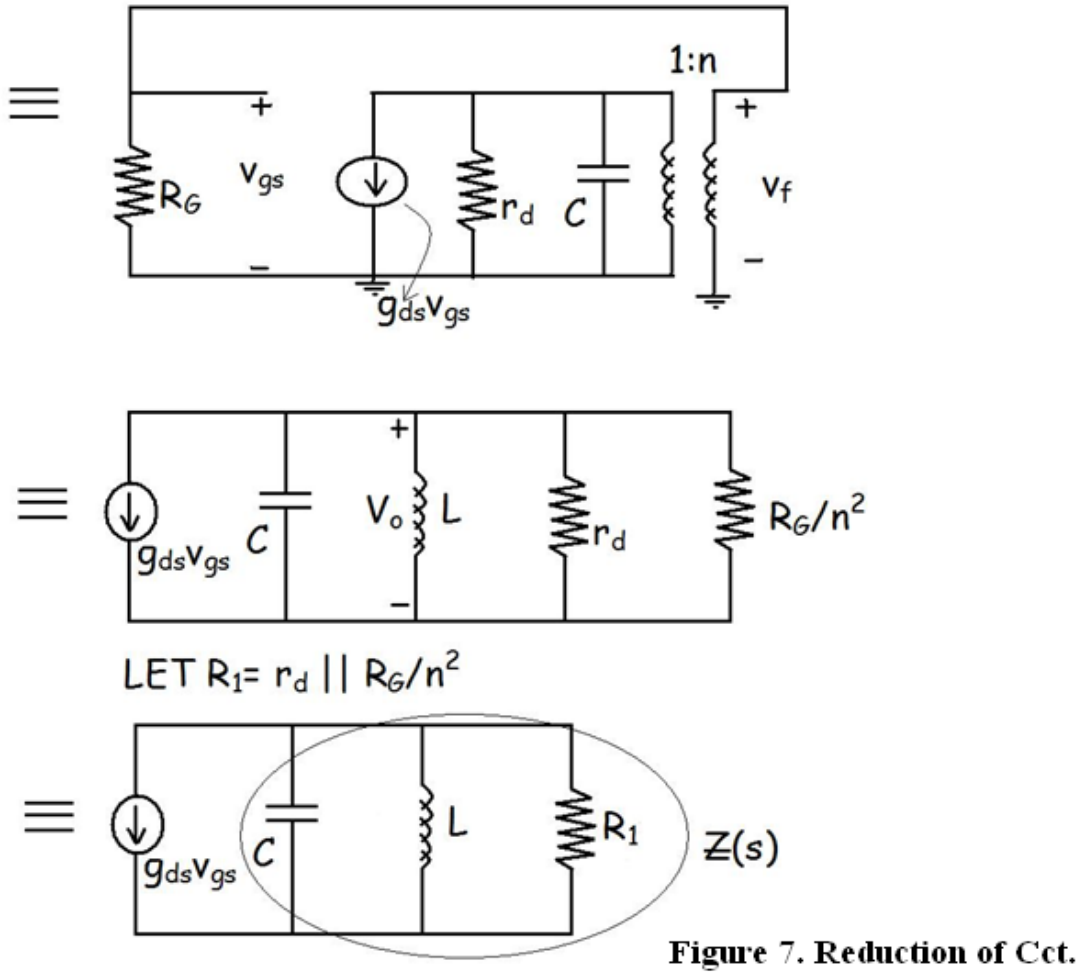

Figure 53.41

$$Z(s) = \frac{1}{\frac{1}{R_1} + SC + \frac{1}{SL}}$$

Figure 53.42

$$\therefore \frac{V_o(s)}{g_m V_{GS}(s)} = \mathcal{Z}(s)$$

Figure 53.43

$$\therefore A_V(s) = \frac{V_o(s)}{V_{GS}(s)} = g_m \mathcal{Z}(s)$$

Figure 53.44

$$A_V(j\omega) = \frac{g_m}{\left(\frac{1}{R_1}\right) + j\left(\omega C - \frac{1}{\omega L}\right)}$$

Figure 53.45

For oscillation Loop Gain= $1\angle 0^\circ$

$$\therefore V_o(j\omega) = V_{gs}(j\omega)$$

Figure 53.46

$$\therefore Imaginary\ Part = 0$$

Figure 53.47

$$\therefore \omega C = \frac{1}{L\omega} \;\&\; \omega_o = \frac{1}{\sqrt{LC}}$$

Figure 53.48

$$At\ this\ frequency\ A_V(j\omega) = g_m R_1 = 1$$

Figure 53.49

Step(1) Choose a suitable value of C:
Let C=0.01μF
Step(2) Calculate the value of L from

$$\omega_o = \frac{1}{\sqrt{LC}}$$

Figure 53.50

$$L = \frac{1}{4\pi^2 C_o{}^2 f^2} = 112.6\mu H$$

Figure 53.51

Step(3) Find the value of R_1 from Eq

$$g_m R_1 = 1$$

Figure 53.52

$$R_1 = 200\Omega$$

Figure 53.53

Step(4)

$$R_1 = r_d || \frac{R_G}{n^2}$$

Figure 53.54

$$\therefore\ n^2 = 49.6, n = 7.04$$

Figure 53.55

PROBLEM(5)
Design a Hartley Oscillator at f_o=5MHz.USE 2N3822 n-JFET whose parameters are

$$g_m = 3\frac{mA}{V}$$

Figure 53.56

Load Resistance is R_L=100Ω
The circuit is:-

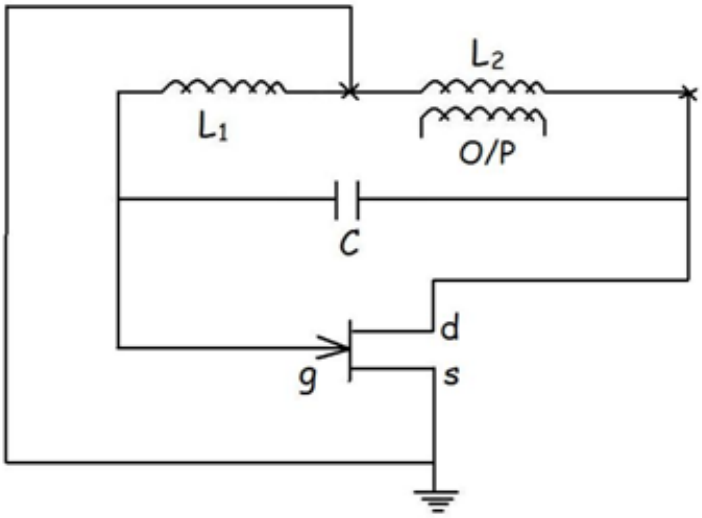

Figure 8. Circuit Diagram of Hartley Oscillator.

Figure 53.57

Practically it is implemented in the following manner:-

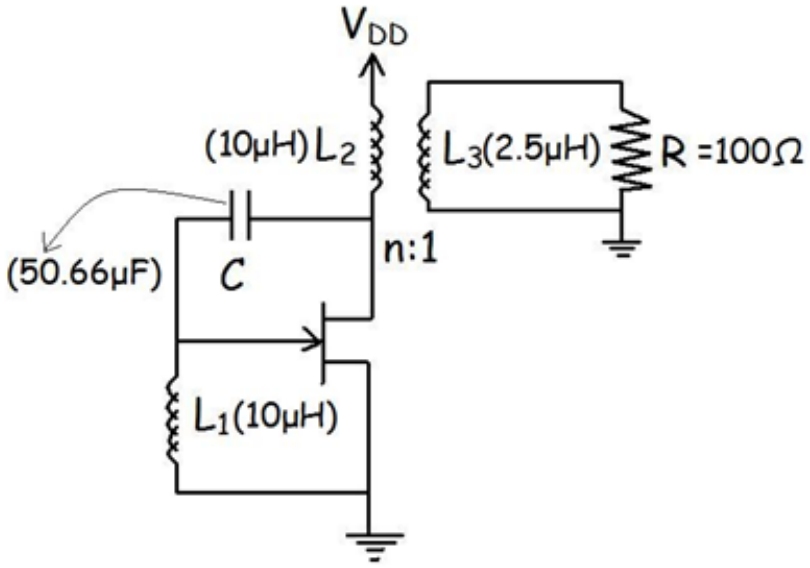

Figure 9. Practical implementation of Hartley Oscilator.

Figure 53.58

The incremental circuit is given in Figure 10.

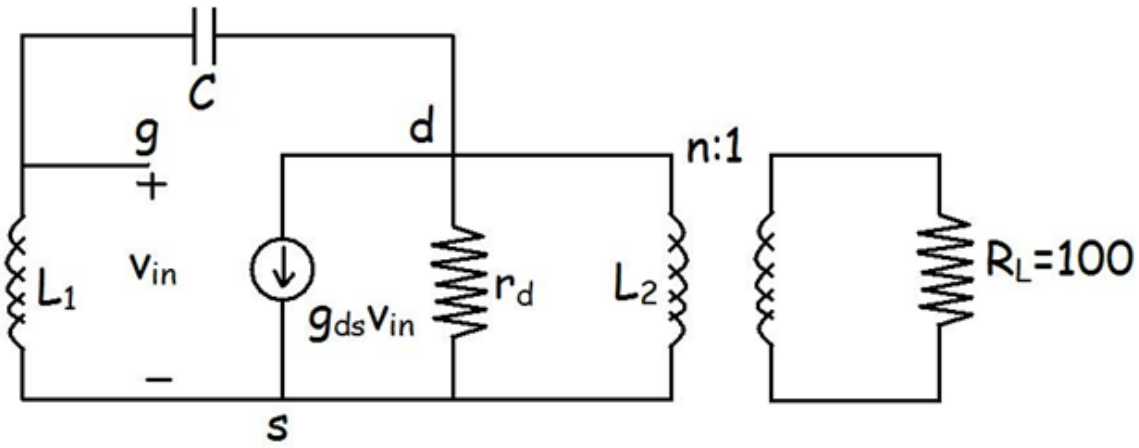

Figure10 Incremental representation of Circuit in Figure 9.

Figure 53.59

Solution:-

$$L_1 = L_2 = 10\mu H$$

Figure 53.60

$$\because \omega_o^2 = \frac{1}{(L_1 + L_2)(C)} \rightarrow C = 50.66pF$$

Figure 53.61

BY analysis:-

$$g_m = \frac{L_2}{(L_1 R_L)} \therefore R_L^* = 333.3\Omega$$

Figure 53.62

We take

$$R_L^* = 400\Omega$$

Figure 53.63

$$\frac{R_L^*}{\mathrm{R_L}} = n^2 = \frac{400}{100} = 4$$

Figure 53.64

$$\therefore n = 2$$

Figure 53.65

$$\frac{L_2}{L_3} = n^2 \rightarrow L_3 = \frac{10\mu H}{4} = 2.5\mu H$$

Figure 53.66

PROBLEM(6)CRYSTAL OSCILLATOR

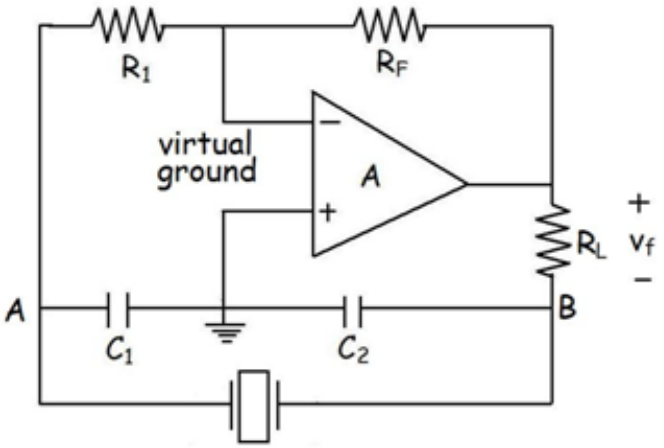

Figure 11. Crystal Oscillator.

Figure 53.67

This is a Colpitts-derived op-amp crystal oscillator which uses crystal as an inductor.
This uses a 2 MHz crystal oscillator

$$C_1 = 0.01\mu F; C_2 = 0.1\mu F; R_L = 100k\Omega; R_1 = 100k\Omega; R_F = 1\ M\Omega$$

Figure 53.68

Find the frequency of oscillator.
Given

$$C_S = 0.0122pF; C_p = 4.27pF; R_S = 82\Omega; L_S = 0.52H$$

Figure 53.69

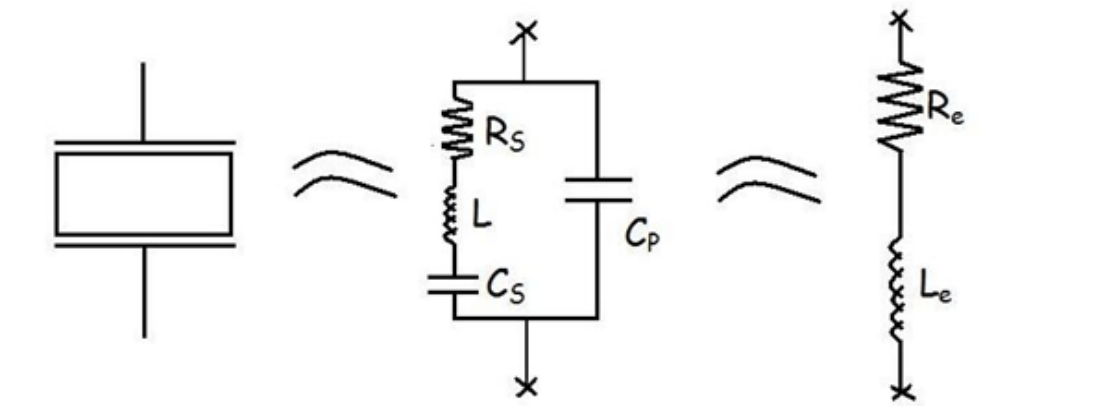

Figure 12. Electrical equivalent of a quartz crystal.

Figure 53.70

$$\omega_s = \frac{1}{\sqrt{L_S C_S}} \quad ; \quad \omega_p = \frac{1}{\sqrt{L_S\left(\frac{C_S C_p}{C_S + C_p}\right)}}$$

Figure 53.71

Equivalent Circuit of Crystal Oscillator:

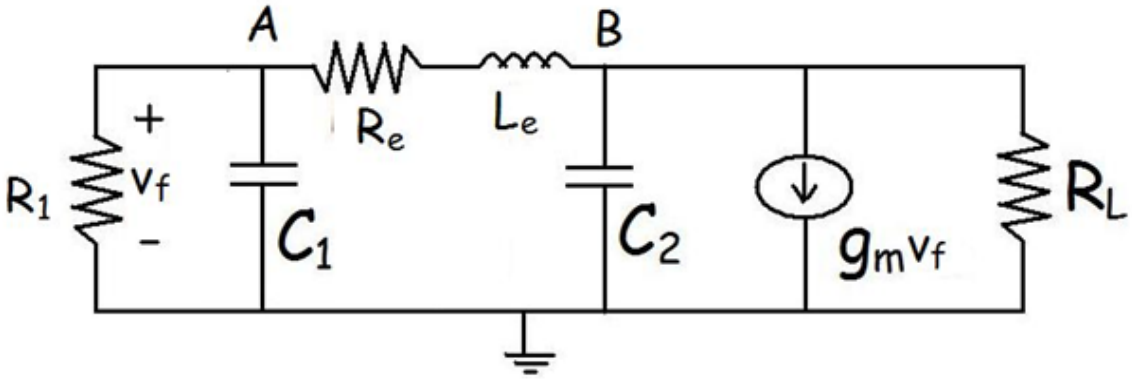

Figure 13. Incremental representation of Crystal Oscillator in Fig.11.

Figure 53.72

This can also be expressed as:

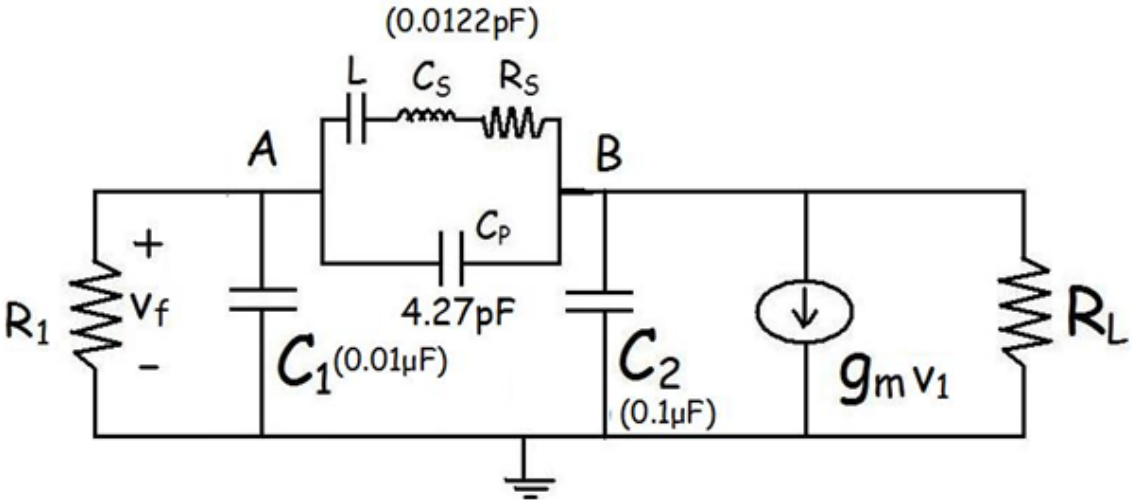

Figure 14. A second incremental representation of Crystal Oscillator.

Figure 53.73

$$C_{eqp} = \left(C_p + \frac{C_1 C_2}{C_1 + C_2}\right) = 9095pF$$

Figure 53.74

Effective Capacitance C_{eq} is parallel with

$$L_S$$

Figure 53.75

is given by

$$C_{eq} = \frac{(C_S)C_{eqp}}{C_S + C_{eqp}} = 0.0122pF$$

Figure 53.76

$$\therefore f_o(Frequency\ of\ oscillation\ of\ the\ crystal) = \frac{1}{2\pi\sqrt{L_S \mathrm{Ceq}}} = 1.998MHz$$

Figure 53.77

It is given that 2MHz crystal is used. Hence the result is self consistent.
This is the frequency of the Crystal Oscillator.

Figure 53.78

Figure 53.79

Chapter 54

AE_Tutorial 13_Tuned Amplifiers[1]

AE_Tutorial 13_Problems on TUNED AMPLIFIER

Problems have been taken from "Microelectronic Circuit Design" by R.C.Jaeger & T.N.Blalock, McGraw Hill Publibcation,2006.

Problem(1)

Design a tuned amplifier having f_o=1MHz, 3dB BW=10kHz and resonance gain= -$g_m R_C$= -10, Use a FET which at the given bias point g_m=5mA/V and r_o=10kΩ.

Solution:

$$A_V(j\omega_o) = -g_m R_C = -10$$

Figure 54.1

$$or - 5 \times 10^{-3} \times R_C = -10$$

Figure 54.2

$$\therefore R_C = \frac{10}{5} = 2K\Omega$$

Figure 54.3

[1] This content is available online at <http://cnx.org/content/m32495/1.2/>.

$$\because r_o = 10k\Omega \ \ \& \ \ R_C = 2K\Omega = \ r_o||R_L$$

Figure 54.4

$$\therefore R_L = 2.5k\Omega$$

Figure 54.5

$$BW = 2\pi \times 10 \times 10^3 = \frac{1}{CR_C}$$

Figure 54.6

$$\therefore C = 7.958nF$$

Figure 54.7

$$\omega_o = 2\pi \times 10^6 = \frac{1}{\sqrt{LC}}$$

Figure 54.8

$$\therefore L = 3.18\mu H$$

Figure 54.9

These L and C values are not realizable hence Autotransformer will have to be used along with L' and C' where turns ratio is chosen to get $L = L'/n^2$ and $C = C'n^2$.

If n = 3 and L'=28.6μH and C'=0.9nF then it is possible to realize the tank circuit as required in this problem. The actual Autotransformer Configuration is described in the Text (Lecture 12).

Problem(2):

Repeat Problem 1 but with new Q of the tank circuit as 150, find R_p. Then find the new value of R_L so that Q of the circuit remains unchanged at resonance frequency 1MHz.

$$Q = \frac{R_p}{L\omega_o}$$

Figure 54.10

$$\therefore R_p = 3k\Omega$$

Figure 54.11

Let the new value of R_L be R_L'.

If Q should remain unchanged then

$$r_o || R_L^{'} = 3\ k\Omega$$

Figure 54.12

$$\therefore R_L' = 5k\Omega$$

Figure 54.13

Problem(3)
Part(a)

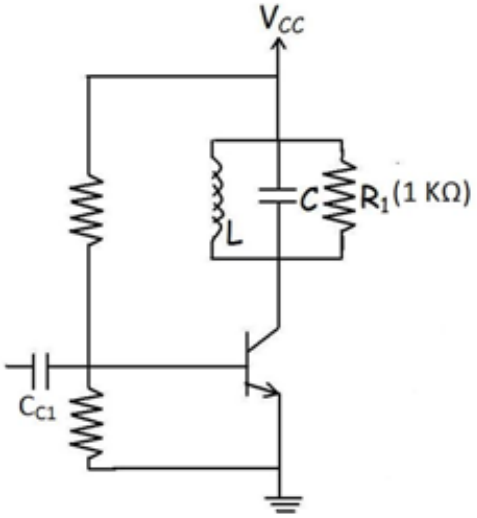

Figure 1. Single Tuned Amplifier

Figure 54.14

L=5μH . Determine C=?
Design an Intermediate Frequency Amplifier which resonates at f_o=455kHz & -3 dB BW=10kHz. Determine C* to give a resonance frequency at fo=455kHz. [Ans: C_1^*=24.45nF]

$$Q_o = \frac{455}{10} = 45.5 = \left(\frac{R_p}{L\omega_o}\right)$$

Figure 54.15

$$R_p = 650.38\Omega$$

Figure 54.16

Part(b):- The IF tuned amplifier is coupled to a second IF stage.

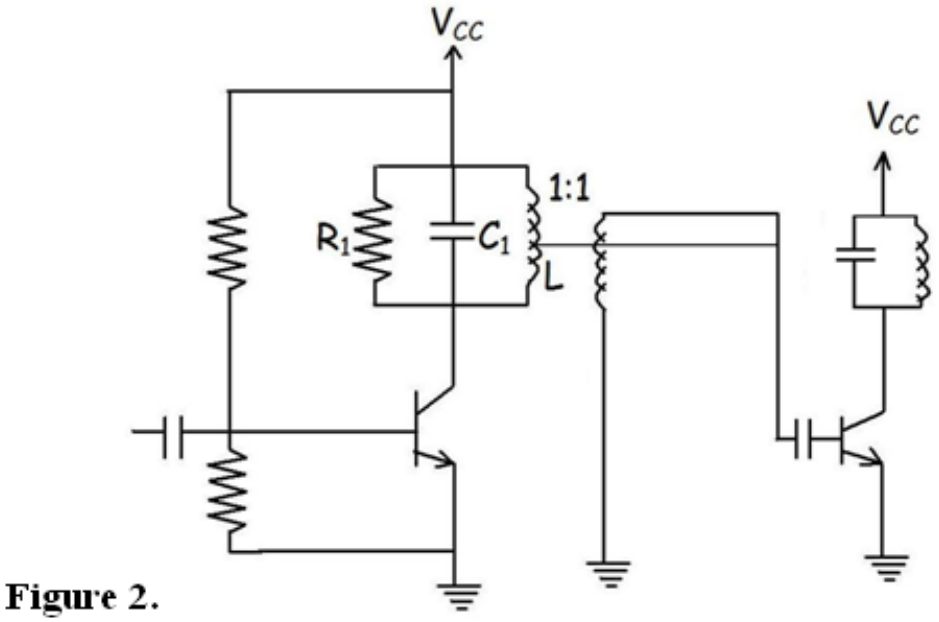

Figure 54.17

Equivalent Circuit:-

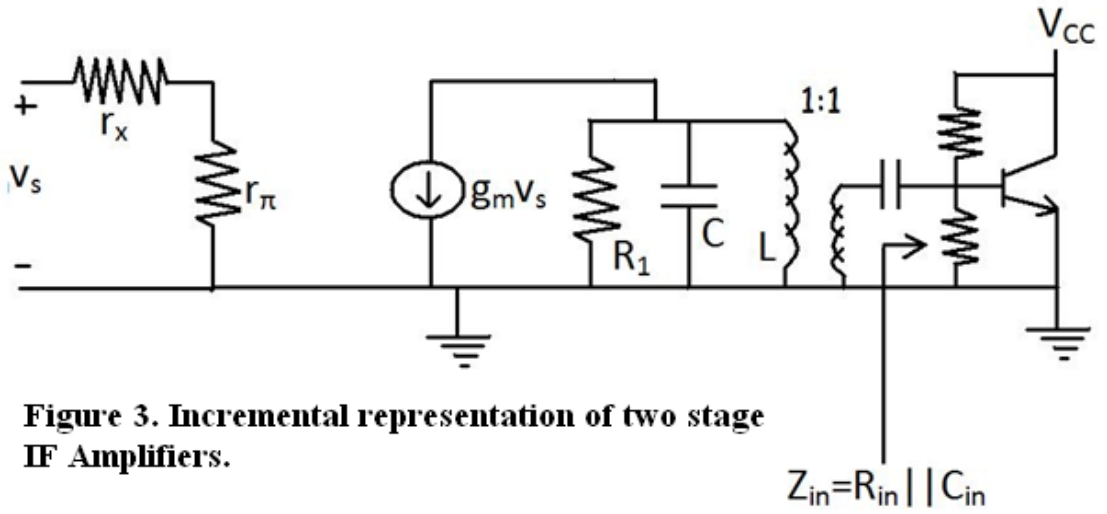

Figure 3. Incremental representation of two stage IF Amplifiers.

Figure 54.18

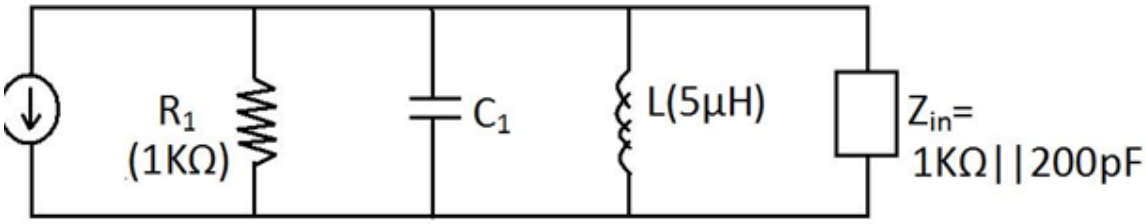

Figure 4. The resulting load as seen by the first stage of two stage IF Amplifier.

Figure 54.19

R_{in}=1kΩ, C_{in}=24.27nF
Determine C_1 required and the resulting B.W.
To give f_o=455kHz

$$C^* = (C_1 + 200pF) = 24.45nF$$

Figure 54.20

$$C_1 = 24.45nF - 0.2\ nF = 24.25nF$$

Figure 54.21

The resulting resistance= 1kΩ||R_{in}=1kΩ||1kΩ=500Ω=

$$R_p$$

Figure 54.22

$$\therefore Q_o = \left(\frac{\omega_o}{BW}\right) = \left(\frac{R_p}{L\omega_o}\right)$$

Figure 54.23

$$\therefore BW = \frac{{\omega_o}^2 L}{R_p} = \frac{(2\pi \times 455 \times 10^3)^2 \times 5 \times 10^{-6}}{2\pi \times 500}$$

Figure 54.24

$$\therefore BW = (2\pi)(13kHz)$$

Figure 54.25

This is larger than desired. This is due to loading caused by Z_{in} of the subsequent stage.
Part(C) By using tapped transformer the loading can be removed. Let g_m=40mA/V

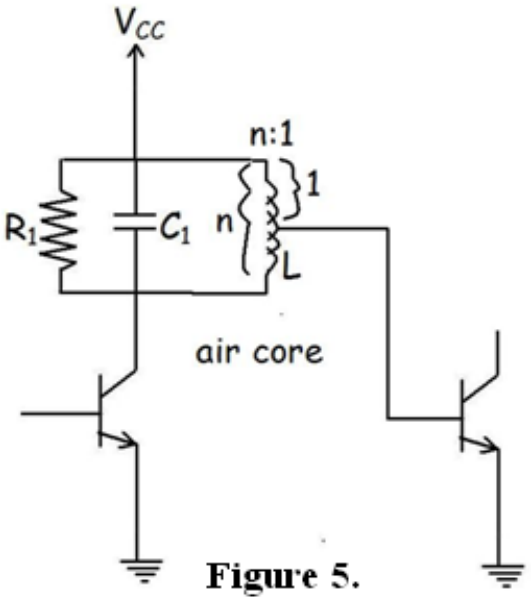

Figure 54.26

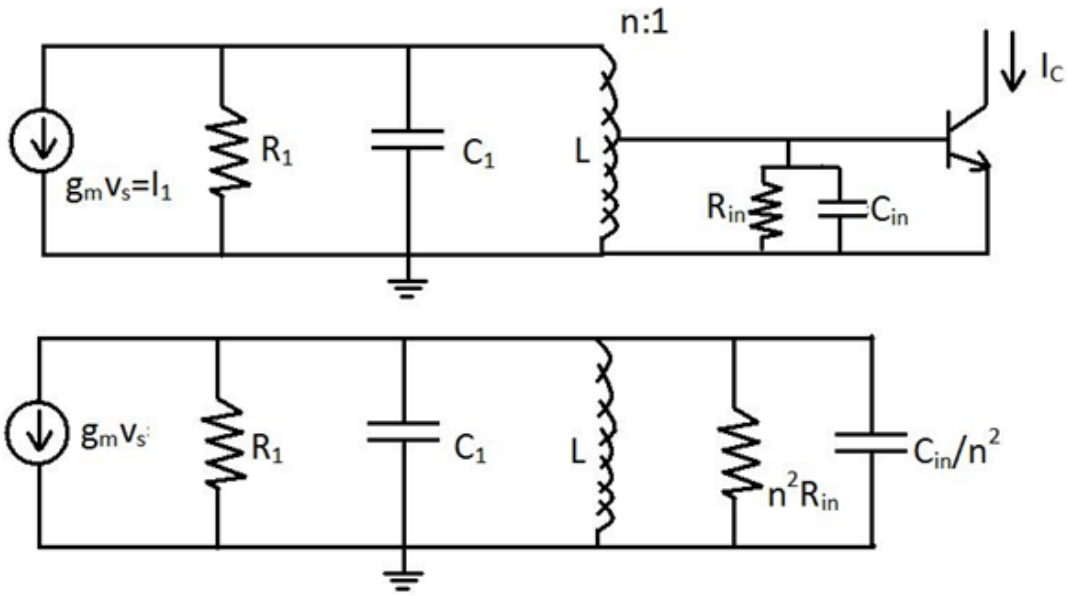

Figure 6. Incremental representation of two stage IF with tapped transformer.

Figure 54.27

To achieve a BW of 10kHz, find the value of n=?, C_1=? And current gain at resonance.
Ans:- n=1.36, C_1=24.36nF, I_C/I_1=19.1 A/A

Chapter 55

Analog Electronics_Univ Question Paper with Solution of Even09[1]

Question Paper of University Examination_EC1305_Spring09_Analog Electronics

A. What are the ideal characteristics of a voltage amplifier ? Explain it with respect to the value of source and load resistances.

B. The two npn transistors are connected as in Figure 1.b. having collector currents 1mA and 10mA with corresponding base-to-emitter voltages of 0.63V and 0.7V. What would be the total current if the base-to-emitter voltage becomes 0.65V ?

Solution of Question 1.A.

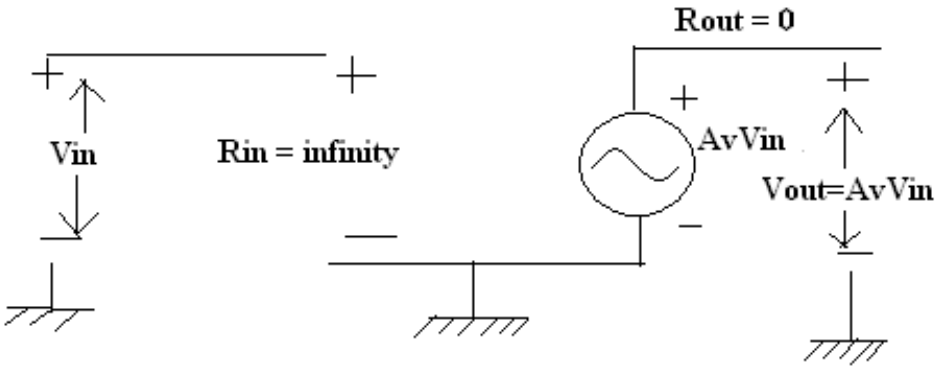

Figure of Question 1.a.

Figure 55.1

Voltage Gain = Vout/Vin = Av
irrespective of Rs (source resistance) and R_L (load resistance).

[1]This content is available online at <http://cnx.org/content/m32963/1.2/>.

The output terminal voltage is equal to open circuit voltage at the output irrespective of Load Resistance. Hence it acts as a voltage controlled voltage source where output is a constant voltage source and is suitable for driving variable loads.

All this is true only when input resistance (Rin) is large and output resistance is small (Rout).

Solution of Question 1.b.

Individually Q1 gives Ic1= 1mA at Vbe1= 0.63V;

Q2 gives Ic2 = 10mA at Veb2 = 0.7V

Ie1= Ie01Exp(Vbe1/25mV). Therefore Ie1= 1mA = Ie01Exp(630mV/25mV). 1

Ie2= Ie02Exp(Vbe2/25mV). Therefore Ie1= 10mA = Ie01Exp(700mV/25mV). 2

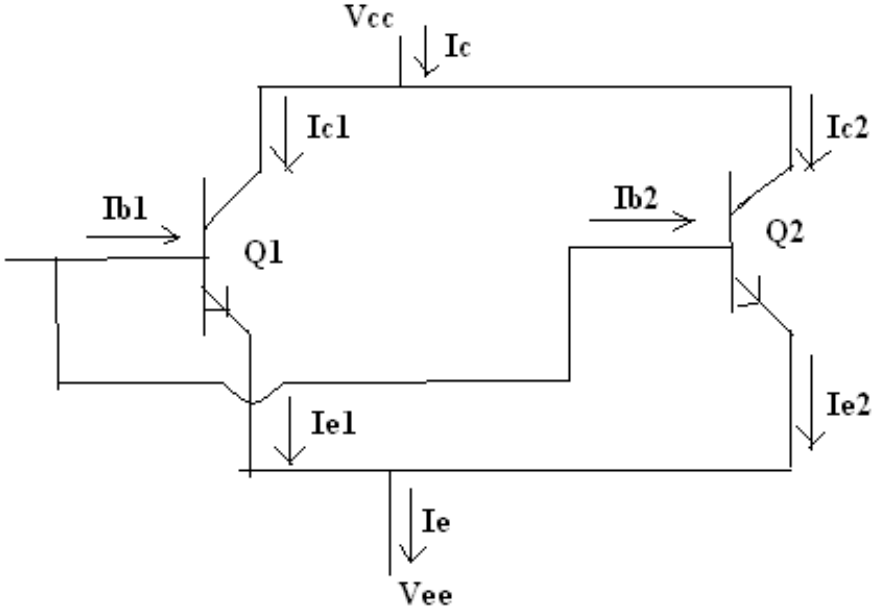

Figure 1.(b).

Figure 55.2

We have to determine the total Ie when Vbe^*= 0.65V;

Solving equations 1 and 2 we get: Ie01=11.4pA and Ie02 = 6.9pA.

When they are connected in parallel as shown both have the same Vbe^*=650mV;

Therefore the total current Ie = Ie1+Ie2

Where Ie1 =11.4pAExp(Vbe^*/25) and Ie2 = 6.9pAExp(Vbe^*/25)

Therefore Ie = 11.4pAExp(650/25) + 6.9pAExp(650/25) = 2.2+1.35 = 3.55mA

Hence **Ie = 3.55mA.**

a. BJT amplifier in Figure 2(a) is biased with a constant current source I = 1mA and BJT has a very high β f0 = very high. Obtain Voltage Gain of the amplifier. The current source may be taken as open circuit in the equivalent circuit.

b. For the circuit shown in Figure 2 (b), obtain the collector current of Transistor T4 when Vo = 0.2V. *Assume β F = 100 and β I = 0.01 and V BE = 0.7V.*

Solution of Question 2.a.

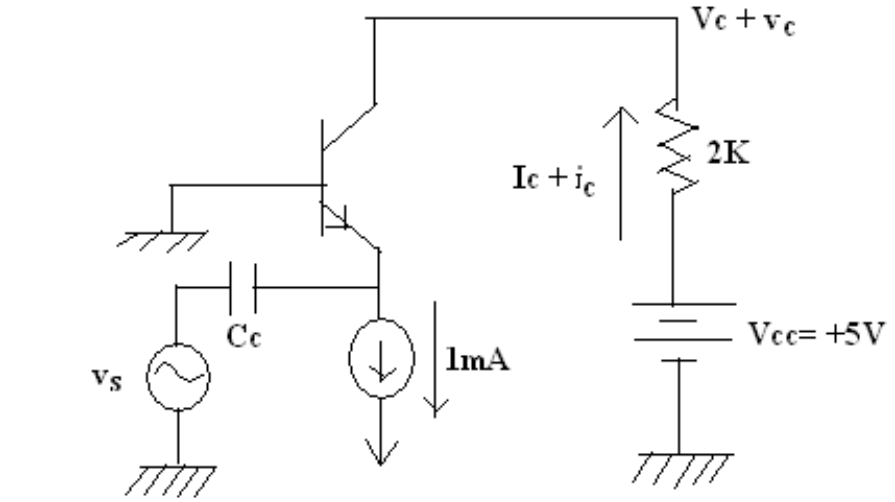

Figure 2 (a).

Figure 55.3

This is a CB amplifier. We re-orient the circuit as follows.

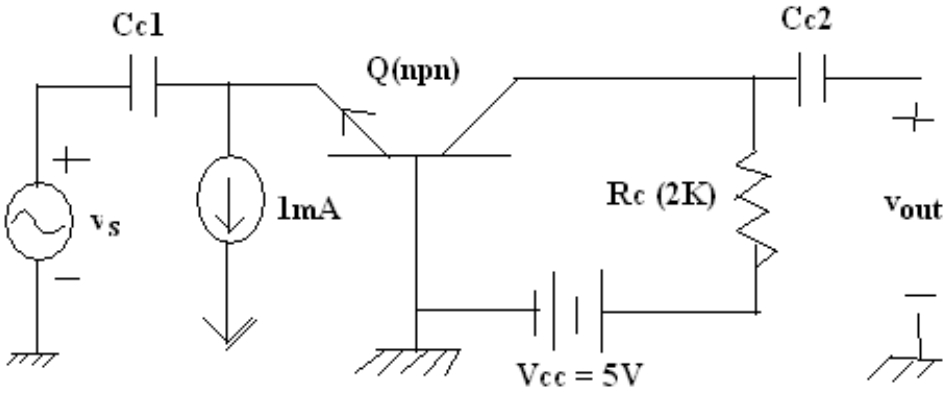

Figure 2.a reoriented.

Figure 55.4

Now we draw the incremental model of the above circuit. While drawing the incremental model, DC Voltage Source will appear as short circuit and DC Current Source will appear as open circuit.

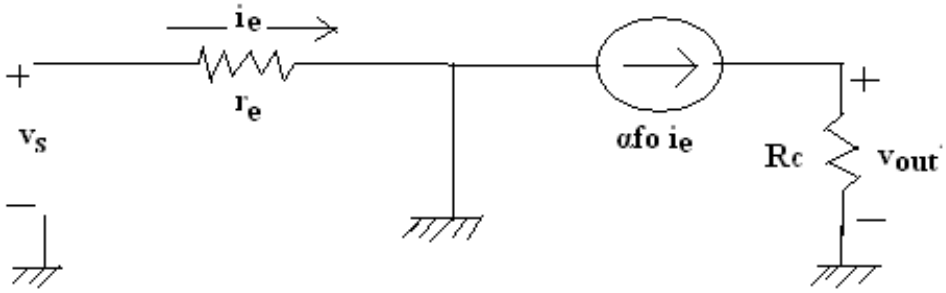

Figure 2a-3. The incremental circuit of the CB Amplifier.

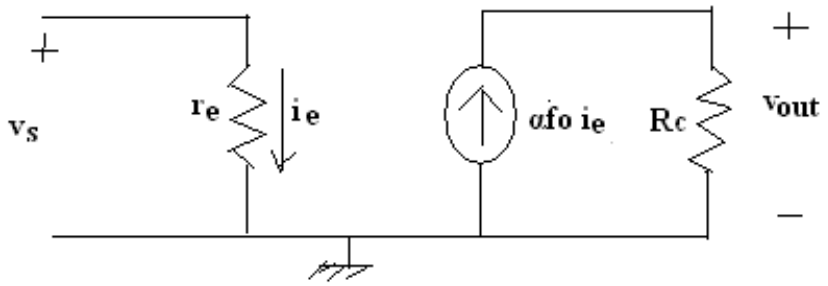

Figure 2a-4. The incremental circuit drawn as two non-interacting loops: input loop and output loop. Since we have neglected base spreading resistance rx therefore there is no reverse interaction.

Figure 55.5

Since bias current is 1 mA therefore r_e (emitter Incremental resistance) = 25 Ω
Since β is very high therefore $\alpha = 1$.
Hence

$$\frac{v_{out}}{v_s} = \frac{R_c}{r_e} = \frac{2000}{25}$$

Figure 55.6

= **80**. [Non-inverting Amplifier]
Solution of question 2.b.
The circuit is a TTL NAND gate. The question states that Vo is 0.2V. This assumes that INPUT is HIGH and OUTPUT is LOW as should be the case in a TTL NAND gate.

Vo = 0.2V implies that T3 is in saturation.

If Vin = 5V then T1 is in inverse active mode meaning by Veb1 is reverse biased and Vbc1 is forward biased. This drives T2 to be ON.

Flow of Ic2 causes T4 to be OFF and T3 to be saturated. Therefore Vo = 0.2V and Ic4 =0.

Therefore **collector current of T4 is zero.**

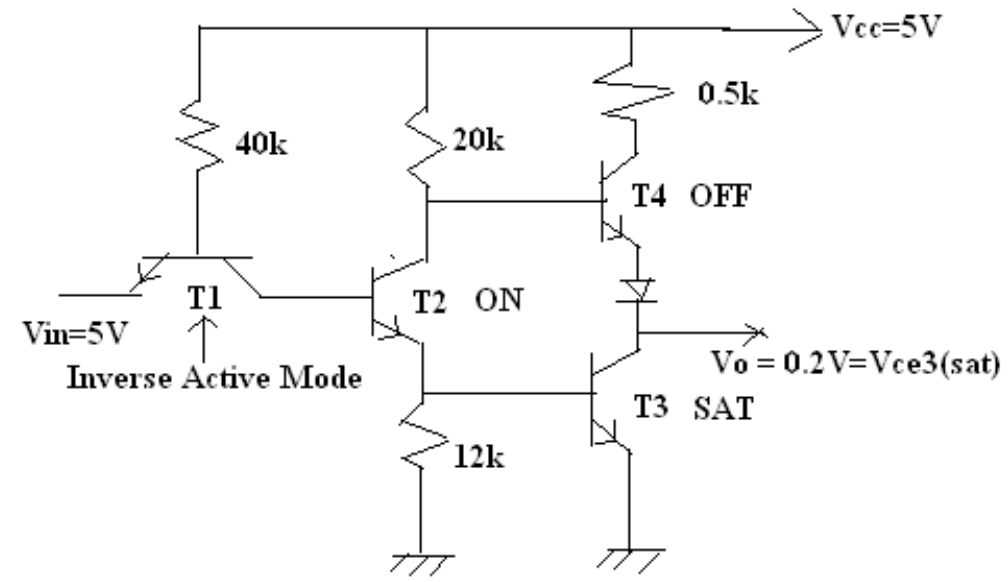

Figure 2(b). A TTL NAND gate with input HIGH.

Figure 55.7

(a) Obtain the relation between Io and Iref of Figure 3(a)

Solution of question 3(a).

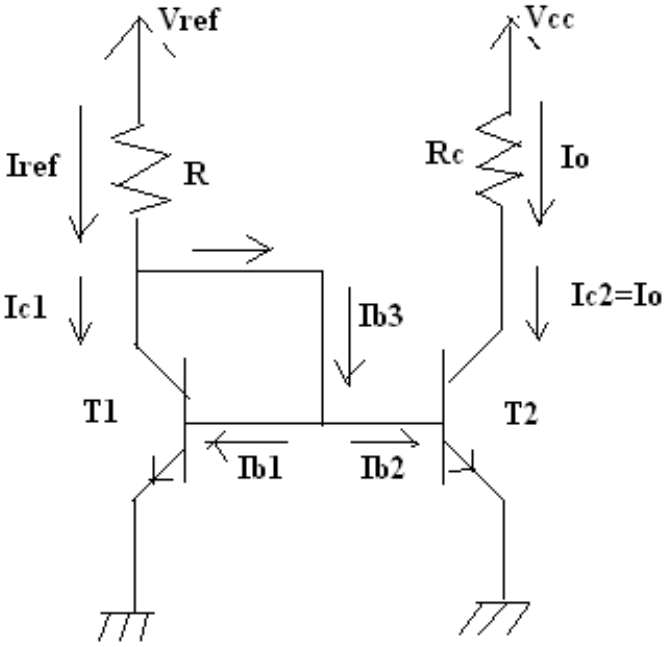

Figure 3 (a). Current Mirror

Figure 55.8

This is a current mirror circuit where Ib1 = Ib2 = Ib
Therefore Ic1 = β_{F1}Ib1 and Ic2 = β_{F2}Ib2
Since they are matched transistors therefore $\beta_{F1} = \beta_{F2}$
Hence Ic1 = Ic2 = Io;
But Iref = Ic1 + 2Ib $\approx$ Io since $\beta_{F1} = \beta_{F2}$ is very high hence 2Ib is negligible compared to Ic1.
Therefore the answer is **Iref $\approx$ Io**

(b) Calculate the value of output current Io for Vin =5V in the circuit diagram of Figure3(b).Obtain the maximum value of R L that can be used in the circuit for Vce2(sat) =0.3V.

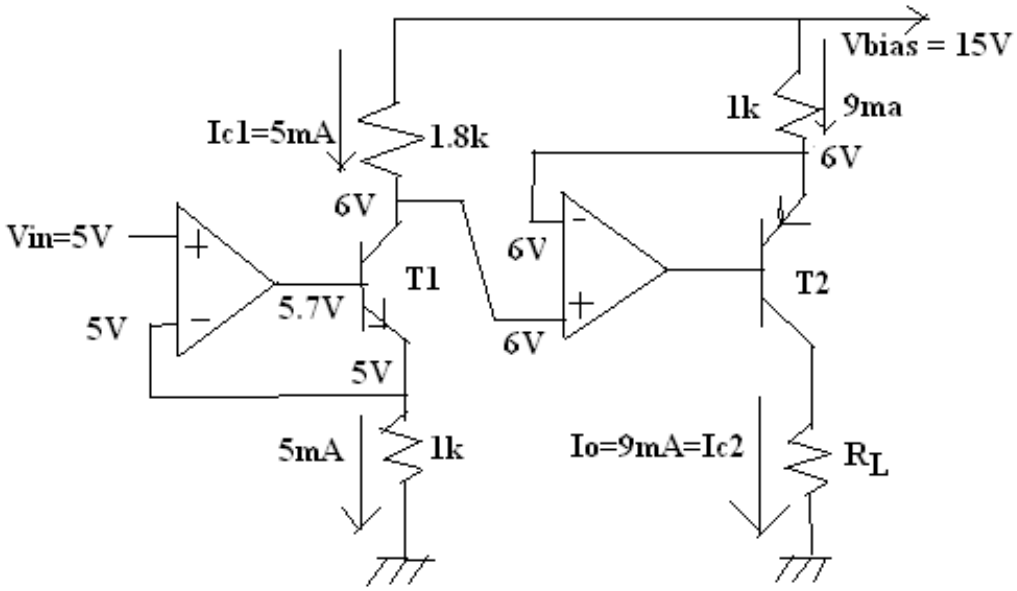

Figure 55.9

Solution of question 3(b).
Op Amps always follow two summing point restraints:
Summing point Restraint 1 : Inverting I/P Voltage = Non-inverting I/P;
Summing point Restraint 2 : Ib1 = Ib2 =0.
In Op Amp 1 since Vin = 5 V therefore inverting I/P = 5V.
Hence current through Re1=1k is 5mA.
Therefore Ic1 = 5mA . This gives Vc1= 15 – Ic1. 1.8k = 6V;
Therefore Voltage at INV I/P of Op Amp 2 is = 6V.
Therefore Ve2= 6V hence Ie1 = (15-6)V/1k = 9mA
Therefore Ic2 = 9mA = Io
Therefore **Io = 9mA**
If T2 is to go into saturation Then Vce2(sat)= 0.3V
Therefore voltage across R_L is =IoR_L = 5.7V since 15V= 9V + 0.3 + 5.7V;
R_L = 5.7/Io = 5.7/9mA = 630 Ω.
R L should be less than 630Ω to prevent T2 from being driven into saturation.
(a) Draw a Hybrid-π mpdel.
The answer is given in Lecture No.4
(b) The circuit shown in Figure 4(b) is a power amplifier which drives 8Ω speaker. Obtain the value of Ic2 and Vce2.
Solution of question 4(b):

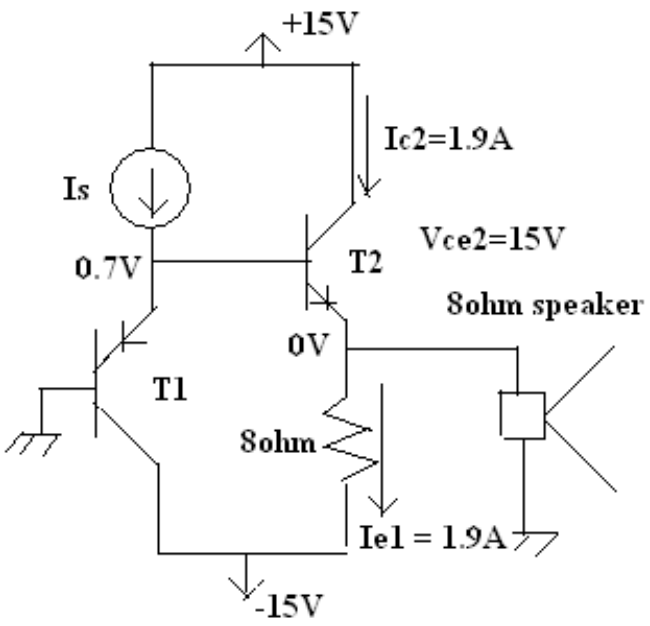

Figure 4(b)

Figure 55.10

As seen from the figure, Ve1 = 0.7V since Vb1 is ground.
But Ve1 = Vb2 = 0.7V therefore Ve2=0V.
Therefore the drop across Re1 is 15V
Therefore Ie2 = 15/8=1.9A = Ic2 and as seen from the figure Vce2= 15V
Therefore **Ic2= 1.9A & Vce2 = 15V**

(a) Derive expression for the voltage gain and 3dB frequency of the amplifier shown in Figure 5(a). Neglect the base spreading resistance r x . Obtain total input capacitance.

Solution of question 5 (a).

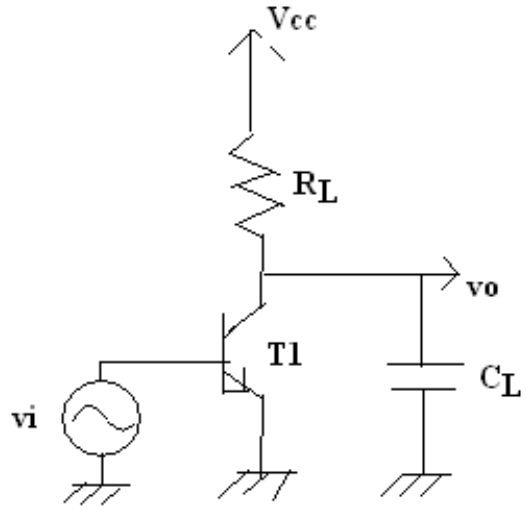

Figure 5(a).

Figure 55.11

The midband gain Avo = $-g_m R_L$
Therefore **total input capacitance is**
Miller Capacitance C M = C π + C μ (1+ g m R L).
Now we draw the incremental circuit of Figure 5(a)

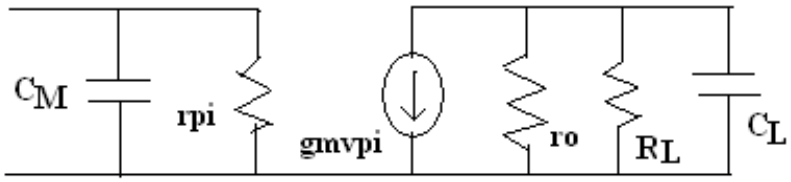

Figure 5a-1. Incremental circuit of Figure5(a).

Figure 55.12

We apply open circuit time constant method to determine upper -3dB frequency:

$$\frac{1}{\omega_h} = \tau 10 + \tau 20$$

Figure 55.13

Where $\tau 10 = C_M \times r_\pi$ and $\tau 20 = C_L \times (R_L || ro)$
Therefore

$$\boldsymbol{\omega_h = \frac{1}{\tau 10 + \tau 20}}$$

Figure 55.14

5 *(b) The lower and upper cut-off frequencies of 1st stage of a two stage amplifier are 100Hz and 140kHz and those of the second stage are 200Hz and 100kHz. If the two stages are cascaded what is the overall bandwidth?*

Solution of question 5 (b) :
We have to use the following formulae

$$\frac{1}{\omega_{hoverall}} = \sqrt{\frac{1}{\omega_{h1}^2} + \frac{1}{\omega_{h2}^2}}$$

Figure 55.15

$$\omega_{loverall} = \sqrt{\omega_{l1}^2 + \omega_{l2}^2}$$

Figure 55.16

Using these two formulae we get:
(f_l)overall = 223.6 Hz
(f_h)overall = 81.372 kHz.
6 *(a) Compare and contrast the dynamic behavior of the two circuits shown in Figure 6 (a)*

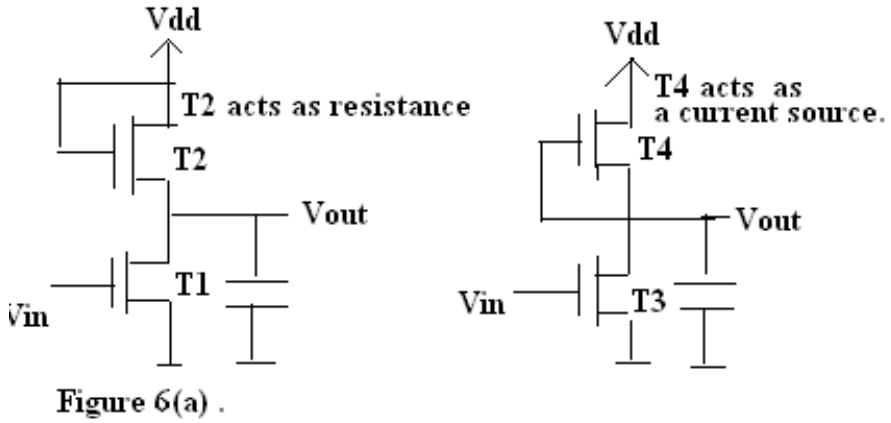

Figure 55.17

Both are NAND gates taught in VLSI.

The second gate is much faster as T4 acts as a current source which helps rapidly charge C_L when I/P is Low and O/P is High.

6 *(b) Each stage of a three stage amplifier without feedback has identical poles and its open loop transfer function is expressed as:*

$$\frac{A_0}{\left(1+\frac{j\omega}{\omega h}\right)}$$

Figure 55.18

Determine its maximum value of feedback factor f max for which the amplitude remains stable. Also determine the corresponding frequency.

The overall gain of three stage amplifier is :

$$\frac{A_0^3}{\left(1+\frac{j\omega}{\omega h}\right)^3}$$

Figure 55.19

= A open
A closeed =

$$\frac{A_{open}}{1+fA_{open}}$$

Figure 55.20

Where f = feedback factor.
For stability, loop gain = -f A open $< 1/0^\circ$
At high frequencies : Loop Gain =

$$\frac{-f\times A_0^3}{\left(\frac{j\omega}{\omega h}\right)^3}$$

Figure 55.21

=

$$\frac{-f\times A_0^3}{-j\left(\frac{\omega}{\omega h}\right)^3}$$

Figure 55.22

=

$$\frac{f\times A_0^3}{j\left(\frac{\omega}{\omega h}\right)^3}$$

Figure 55.23

$< 1/0^\circ$

Therefore f < (1/0 °)×j

$$\left(\frac{\omega}{\omega h}\right)^3$$

Figure 55.24

×

$$\frac{1}{A_0^3}$$

Figure 55.25

Therefore f <

$$\left(\frac{\omega}{\omega h}\right)^3$$

Figure 55.26

×

$$\frac{1}{A_0^3}$$

Figure 55.27

Feedback factor will depend upon the frequency ω we are using.
Suppose we are using ω* frequency then
fmax =

$$\left(\frac{\omega*}{\omega h}\right)^3$$

Figure 55.28

×

$$\frac{1}{A_0^3}$$

Figure 55.29

Hence

$$\sqrt[3]{f_{max}}$$

Figure 55.30

×

$$\omega_h \times A_0 = \omega*$$

Figure 55.31

7 (a) *In the following variant of Wien-Bridge Oscillator Fig 7(a) determine the gain and frequency for sustained oscillation?*

(b) A tank circuit is connected to non-inverting terminal of the Op Amp shown in Fig 7(b) having a non-inverting gain of 12. Determine the resonant frequency and Band width of the amplifier. If the input is a current source I S , obtain the transfer function between the output voltage and input current source.

Solution of question 7 (a). This is a variant of Wien Bridge Oscillator hence we will adopt the same procedure for determining the gain of the basic amplifier for sustained oscillation and the frequency of sustained oscillation.

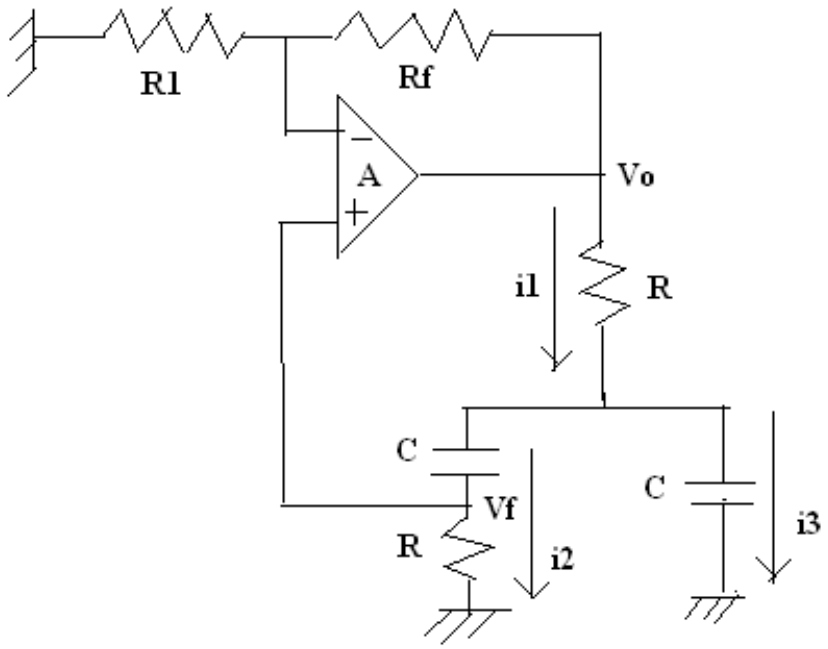

Figure 7 (a). A variant of Wien Bridge Oscillator.

Figure 55.32

The Loop Gain has to be determined and set to $1/0°$,. This is the Barkhausen Criteria. The frequency at which this criteria is satisfied is the frequency of sinusoidal oscillation. If the loop gain is less than $1/0°$ we will not get any oscillation. If loop gain is greater than $1/0°$ then we will get clipped sinusoidal. But to achieve self starting condition we have to keep loop gain slightly greater than $1/0°$ and use amplitude limiting diodes to prevent clipping.

In the Figure above:

$$i_1 = \frac{v_0(j\omega C)(2+j\omega CR)}{[j\omega CR(2+j\omega CR)+(1+j\omega CR)]}$$

Figure 55.33

$$i_2 = \frac{i_1}{(2 + j\omega CR)}$$

Figure 55.34

$$v_f = i_2 \times R$$

Figure 55.35

Therefore

$$\frac{v_f}{v_0} = \frac{j\omega CR}{[(1+j\omega CR)+j\omega CR(2+j\omega CR)]}$$

Figure 55.36

=feedback factor
Let

$$\omega_0 = \frac{1}{CR}$$

Figure 55.37

Therefore:

$$\frac{v_f}{v_0} = \frac{j\frac{\omega}{\omega_0}}{\left[\left(1 + j\frac{\omega}{\omega_0}\right) + \left(j\frac{\omega}{\omega_0}\right)\left(2 + j\frac{\omega}{\omega_0}\right)\right]}$$

Figure 55.38

In order to get a real feedback factor, the real part in the denominator should be zero. Equating Real part of Denominator = 0 we get:

$$1 - \left(\frac{\omega}{\omega_0}\right)^2 = 0$$

Figure 55.39

Therefore Oscillator Frequency =

$$\omega^* = \frac{\omega_0}{1}$$

Figure 55.40

Imaginary Part of the Denominator =

$$\frac{j3}{1}$$

Figure 55.41

Therefore feedback factor at

$$\omega^* = \omega_0 :$$

Figure 55.42

$$\frac{v_f}{v_0} = \frac{j\times 1}{j\times 3} = \frac{1}{3}$$

Figure 55.43

$= \mathbf{f}$
Therefore Gain of the Basic Amplifier =

$$\frac{3}{1} = \left(\frac{R_F}{R_1} + 1\right)$$

Figure 55.44

$$f_{osc} = \frac{1}{2\pi CR}$$

Figure 55.45

Solution of question 7(b):

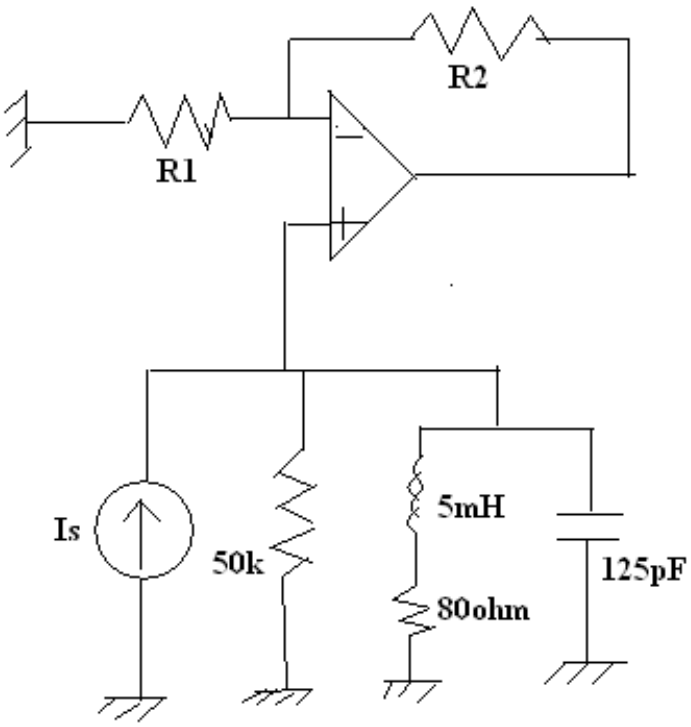

Figure 7. b. Single tuned amplifier.

Figure 55.46

Gain of the Amplifier = 12 = (1+R1/R2);
Q =

$$\frac{\omega_0 \times L}{80ohm} = \frac{R_p}{\omega_0 \times L}$$

Figure 55.47

R p = 50kΩ.
A parallel resonance circuit called a tank circuit can be expressed in two ways:

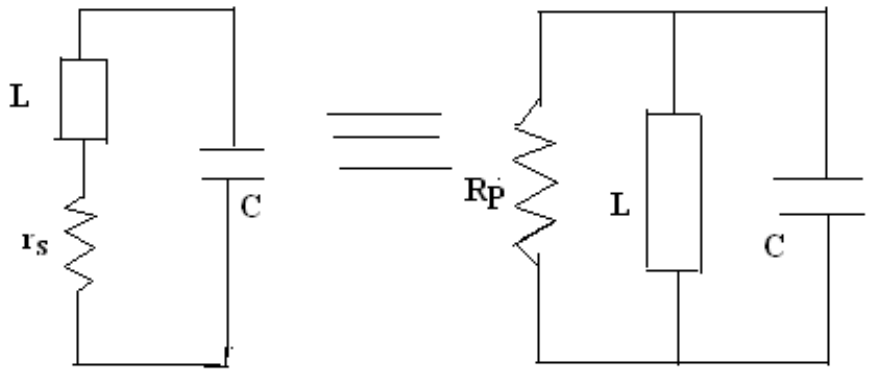

Figure 7(b)-1 Equivalence of a tank circuit with resistance r_S in series with the inductor and resistance R_P in parallel with inductor.

Figure 55.48

Both are equivalent hence:
Q =

$$\frac{\omega_0 \times L}{80ohm} = \frac{R_p}{\omega_0 \times L}$$

Figure 55.49

Resonance Frequency =

$$\omega_0 =$$

Figure 55.50

$$\frac{1}{\sqrt{LC}}$$

Figure 55.51

;

Therefore f 0 = 63.66kHz.

BW = Resonance Frequency/Q = 63.66kHz/12.5 = 5kHz

Q of the tank circuit per se is 25 but it is in parallel with the source resistance of 50k hence Q deteriorates to 12.5.

The Transfer Function =

$$\frac{v_0}{i_s}$$

Figure 55.52

;

The gain of the non-inverting amplifier =12=

$$\frac{v_{out}}{v_{in}}$$

Figure 55.53

But v in = i s Z where Z is the impedance of the tank circuit and at resonance its value is 50k||50k = 25k.

Therefore

$$\frac{v_0}{i_s} = 12 \times Z$$

Figure 55.54

8 (a) *The circuit of a power amplifier as shown in Fig 8 (a) amplifies the power of the signal vm(t) to feed to a 5Ω loud speaker. What is the maximum power delivered to the 5Ω loud speaker for the maximum output swing from the Op-Amp subject to battery supply of ±8V and ICmax = 2A and PCmax = 1W. After mounting the transistor on a heat sink it sustains PCmax = 3W. The circuit has a current booster as the Op.Amp can supply only 25mA at the most.*

Solution of question 8(a).

Op Amp acts as Non Inverting Amplifier with gain = 1+ 8/2 = 5

Output Swing of Op Amp peak to peak is = 15 V from 7.5V to -7.5V.

Complementary Symmetry Amplifier has been put as a current booster and it has a voltage gain of UNITY only.

Therefore $v_{out} = 5v_{in}$

Max Power delivered to the load = $V_{outrms}{}^2/5 = (7.5/\sqrt{2})^2/5 = 5.625$W;

P max delivered to the speaker = 5.625W

I_{cmax} = 2A therefore V_{0max} = 10V but our swing is limited to ±7.5V

Therefore it cannot deliver more than 5.625W.

At maximum power delivery the dissipation in the amplifier is = $P_{dissipation}$ = 5.625W(1-η) = 1.19W since power conversion efficiency = 0.788.

This is well within the 3W of heat dissipation which is permitted with the heat sink hence the design is OK.

Chapter 56

AE_EC1405_EVENSEM_2011_MidSemester[1]

MIDSEMESTER TEST

EC1405_Analog Electronics_IT & CSE Fourth Semester.

Time: 2 hours Total Marks:18 points

Question 1 is compulsory and any two of the remaining three questions.

Question 1.

- Give the spectrum slot allotted for AM_Medium Wave-AIR local transmission, for AM_Short Wave_Global Transmission, for Doordarshan Transmission for Channel 2 to 6 and for FM Radio transmission by AIR.
- Describe Amplitude Distortion also known as Harmonic Distortion. Give an example of Amplitude Distortion.
- Describe Frequency Distortion and an application where Frequency Distortion occurs.
- Describe the different schemes of Biasing and which schemes are preferred in actual circuits.
- Draw the Frequency Domain Response and Time Domain response of Emitter Degenerate Amplifier at 100Hz and at 10kHz.
- How does a HPF(High Pass Filter) behave at very low frequencies where time period of repetition of input square wave is much larger than the Time Constant of HPF.
- How does a LPF(Low Pass Filter) behave at very high frequencies where time period of repetition of input square wave is much smallerthan the Time Constant of LPF.
- What is the CRO display under Component Testing mode for resistance R which is high, low, open circuit and short circuit.

Question 2.

[1] This content is available online at <http://cnx.org/content/m37338/1.1/>.

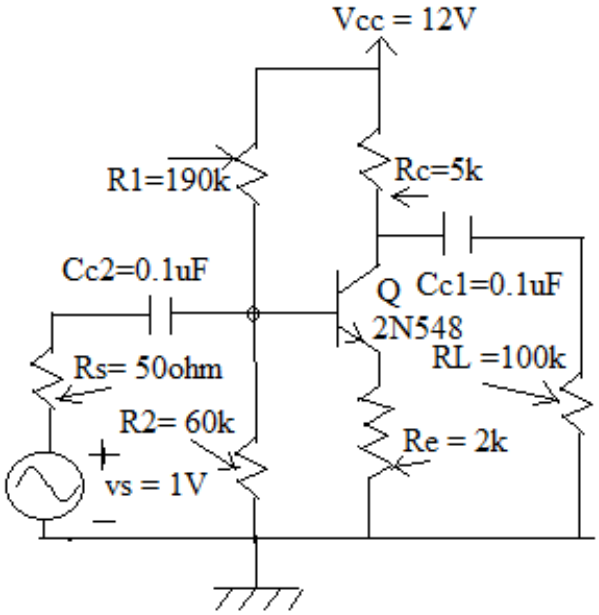

Figure 56.1

- Identify the amplifier.
- If I_{CQ}= 1mA, V_{CEQ} = 5V then write down the incremental parameters of the BJT either for its h-model or for its Hybrid-pi Model.
- Draw the DC and AC load line on the I-V family of curves of Q BC548 and mark the Q point.
- Using the load line draw the output curve if the input voltage is

v_S = 1VSin(ωt).

Question 3.

If a Low Pass Filter has R = 10k and C = 1μF then calculate its cutoff frequency.

a. What is the frequency response BODE PLOT of the magnitude of the transfer function H(jω) of LPF ?

b. What is the Time Domain Response of LPF for:

1. T of the square wave $\gg \tau$ (time constant) of LPF;
2. T of the square wave $\approx \tau$ (time constant) of LPF;
3. T of the square wave $\ll \tau$ (time constant) of LPF;

(Assume that input square wave is of 10V amplitude and it is offsetted by 5V).

Question 4.

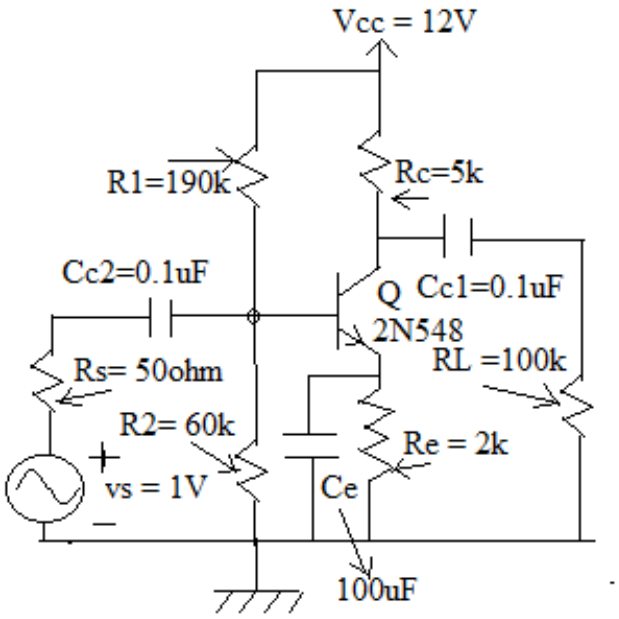

Figure 56.2

- Identify the amplifier.
- If I_{CQ}= 1mA, V_{CEQ} = 5V then write down the incremental parameters of the BJT either for its h-model or for its Hybrid-pi Model.
- Draw the DC and AC load line on the I-V family of curves of Q BC548 and mark the Q point.
- Using the load line draw the output curve if the input voltage is

$v_S = 5mVSin(\omega t)$.

Chapter 57

AE_EC1405_EVENSEM_2011_MidSemester[1]

Solutions of Midesemester Examination_AE_EC1405_EVEN_2011

1. i.Give the spectrum slot allocated for the following applications:

Application	Spectrum Slot
Medium Wave AIR local broadcast_AM	540kHz to 1.7Mhz
Short Wave Global Broadcast of different countries_AM	5.95MHz to 26.1MHz
Doordarshan TV Broadcast_ Channel 2 to 6	54MHz to 88MHz
AIR_FM broadcast	88MHz to 108MHz

Table 57.1

ii. Nonlinear characteristics of the active device causes Amplitude Distortion or Harmonic Distortion. In RC-coupled Amplifier when input voltage exceeds 10mVpeak to peak the small signal approximation is vilated and Amplitude distortion occurs.

iii. When the full spectrum of the given intelligent signal say speech signal is not transmitted then Frequency Distortion occurs as Sqaure Wave passing through RC Low Pass Filter. If the Time Period(T) of the square wave is comparable to the time constant of RC Filter(τ) then rounding off of the edges occur. When T $\ll \tau$, then the square wave is completely obliterated. Only the mean value or the DC part remains with slight ripple.

iv. Different Schemes of Biasing:

Biasing Schemes	Applications
Two Battery Biaing	Expensive, cumbersome and preferred only for device characterrization

continued on next page

[1]This content is available online at <http://cnx.org/content/m37339/1.1/>.

Fixed Biasing	No feedback hence drift prone. Q-point drifts with temperature, aging and replacement.
Potential Divider Biasing	No feedback hence drift prone. Q-point drifts with temperature, aging and replacement.
Self Biasing	Through R_E , negative current-series feedback is provided hence no drift of Q-point with temperatue, aging and replacement. Finds wide application in Discrete Amplifiers.
Collector-Base feedback bising	Through R_B, negative voltage shunt feedback is provided hence no drift of Q-point with temperature, aging and replacement. Finds wide application in Discrete Amplifiers.
Widlar Biasing	This also has negative voltage shunt feedback hence no drift of Q-point with temperature, aging and replacement. Finds wide application in Integrated Circuit Amplifiers.

Table 57.2

v. Frequency Domain Response of the magnitude of the Voltage Gain of Emitter Degenerate Amplifier:

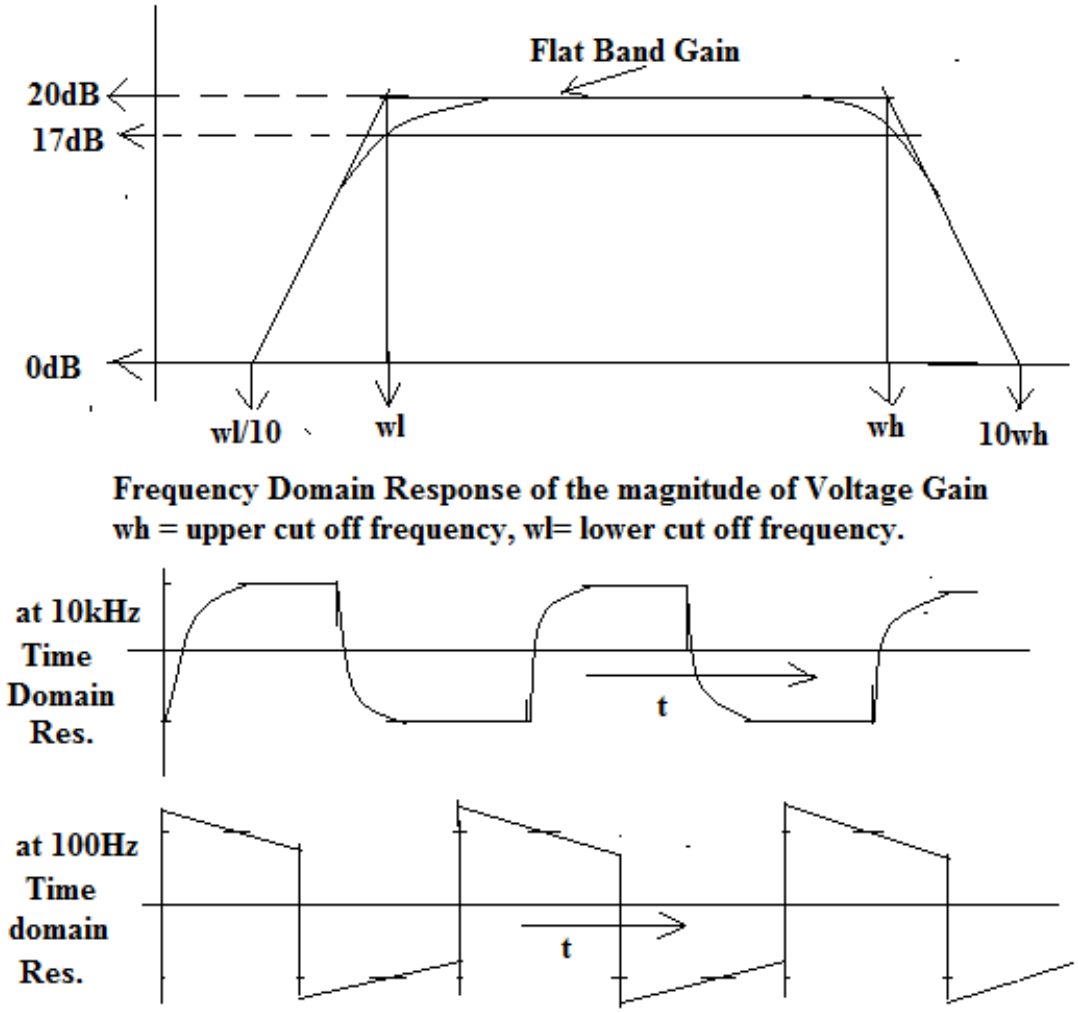

Figure 57.1

The square wave response of the Emiter Degenerate Amplifier is the Time Domain Response. At 10kHz, rounding off of the edges of the square wave is taking place. At 100Hz, the top and bottom of the square wave are sagging or tilting.

vi. High Pass Filter behaves as differentiator at very low frequencies. It just produces positive spikes at positive edges and negative spikes at negative edges.

vii. Low Pass Filter behaves as integrator at very high frequencies. It gives the mean value of the input square wave .

viii. CRO display under Component Testing Mode for resistances:

Resistance value	Display
Very high resistance	Inclined line with very low angle of inclination
Low resistance	Inclined line with high angle of inclination
Open Circuit	Horizontal line
Short Circuit	Vertical line.

Table 57.3

1. Identify the Amplifier ? Emitter degenerate Amplifier.

Q point I_{CQ} = 1mA and V_{CEQ} = 5V
Parameters of h-model:

h- parameter	value
hie	2.6k+100ohm
hre	10^{-4}
hfe	100
hoe	1/40k

Table 57.4

Hybrid-π Parameters:

Hybrid-π Parameters	value
rx	100Ω
rπ	2.6kΩ
rμ	4M
ro	40k
βfo	100
Cπ	100pF
Cμ	5pF

Table 57.5

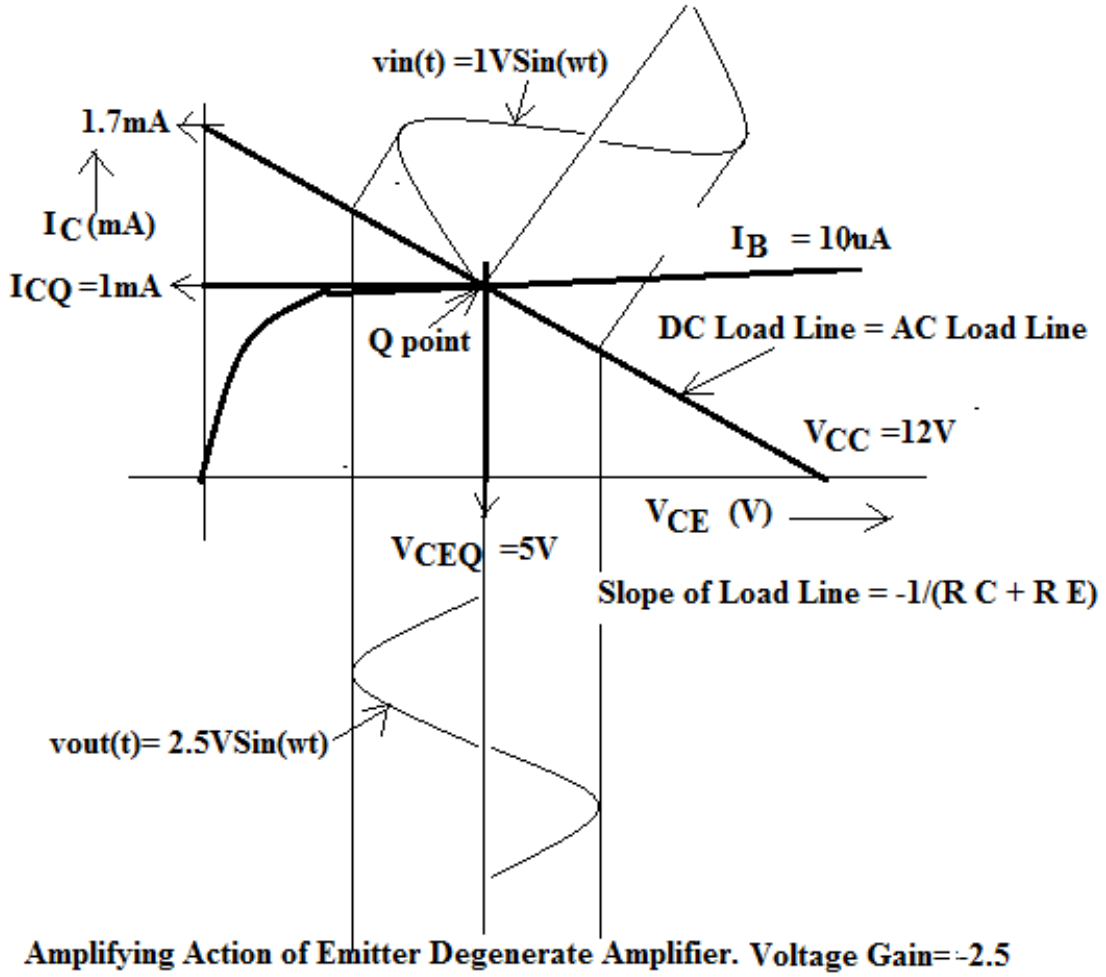

Figure 57.2

1. (a) Low Pass Filter R = 10k and C = 1μF

Therefore Time Constant = τ = RC = 10 msec ;
Upper Cut off Circular Frequency = ω_h = (1/10)kradians/sec;
Upper Cut off Frequency = f_h = 15.9Hz.
Bode Plot:

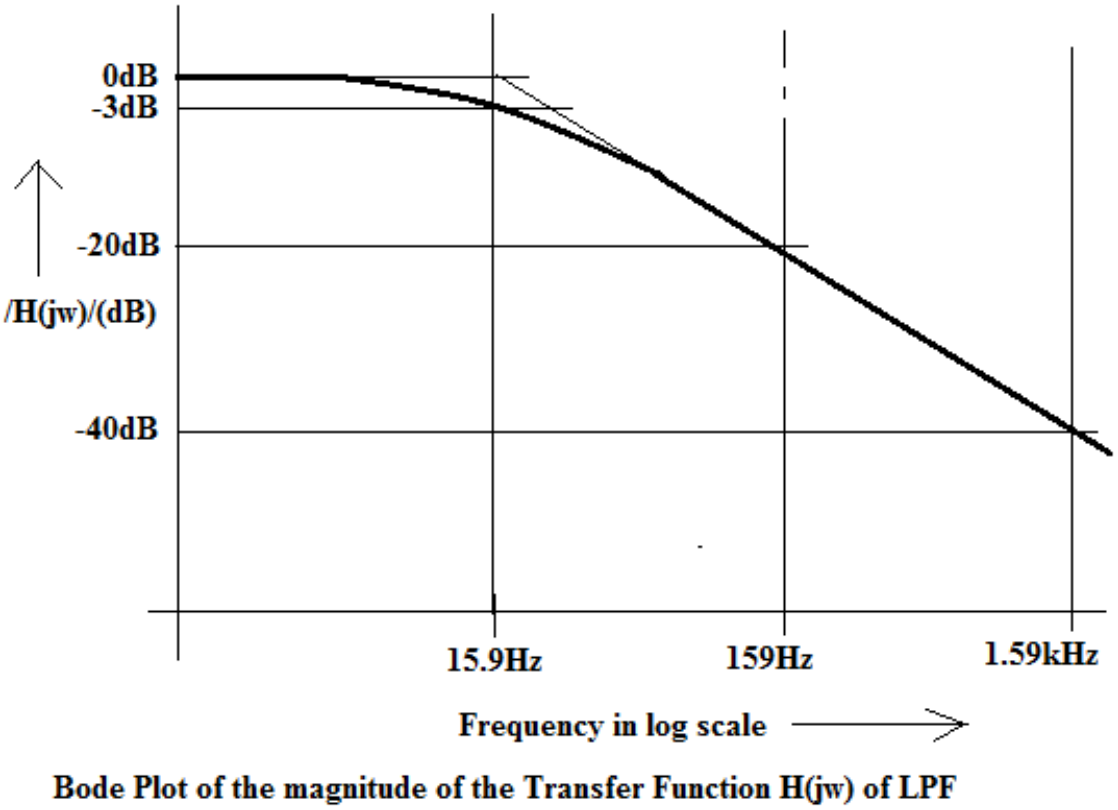

Figure 57.3

b. Time Domain Response of LPF:

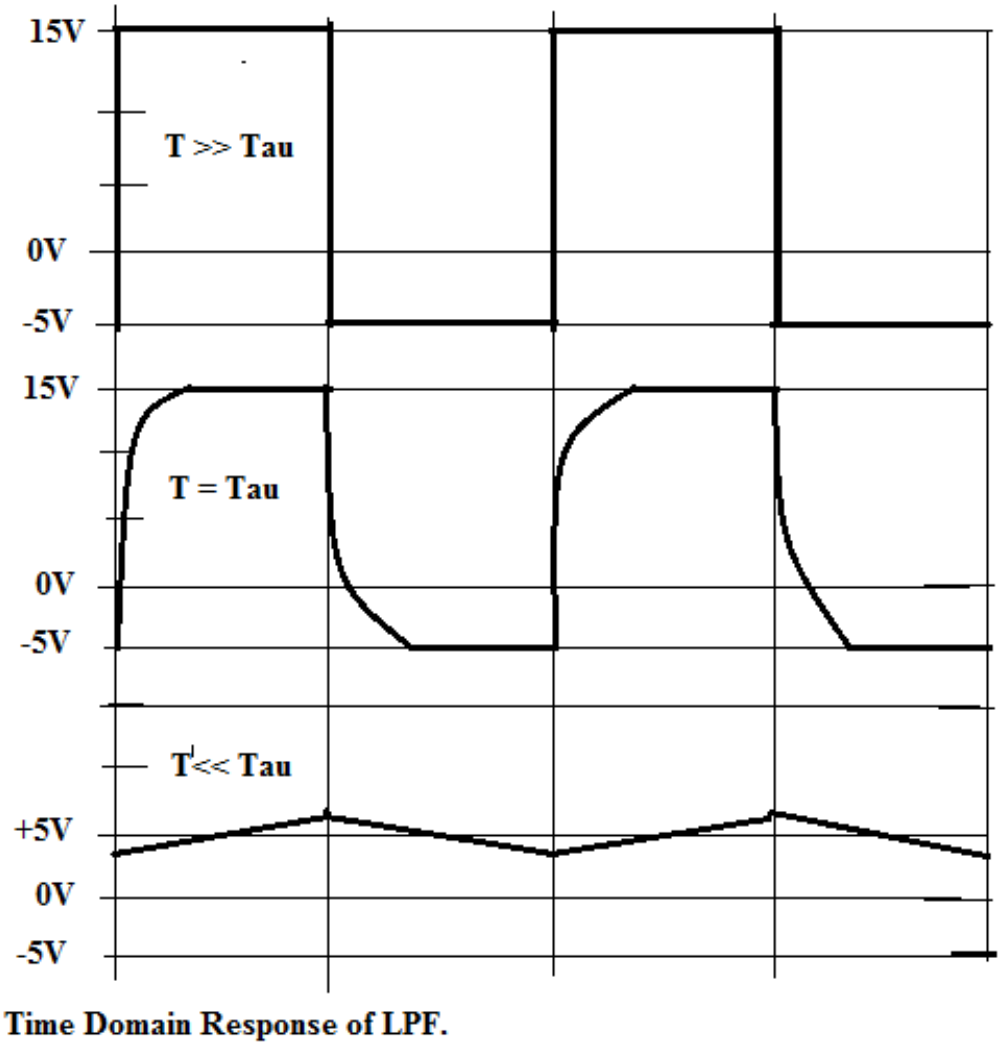

Figure 57.4

1. (a) This is a RC-coupled Amplifier.

(b) Q point I_{CQ} = 1mA and V_{CEQ} = 5V
Parameters of h-model:

h- parameter	value
hie	2.6k+100ohm
hre	10^{-4}
hfe	100
hoe	1/40k

Table 57.6

Hybrid-π Parameters:

Hybrid-π Parameters	value
rx	100Ω
rπ	2.6kΩ
rμ	4M
ro	40k
βfo	100
Cπ	100pF
Cμ	5pF

Table 57.7

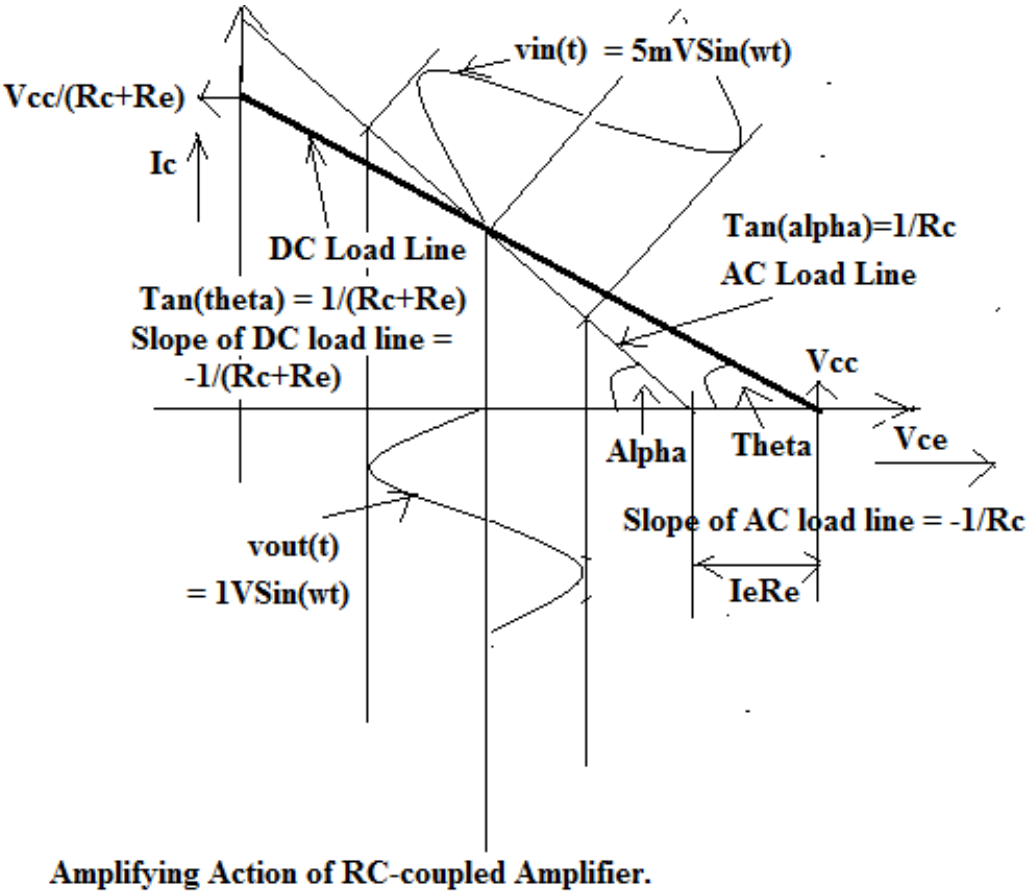
vin(t) = 5mVSin(wt)
Vcc/(Rc+Re)
Ic
DC Load Line
Tan(theta) = 1/(Rc+Re)
Slope of DC load line =
-1/(Rc+Re)
Tan(alpha)=1/Rc
AC Load Line
Vcc
Vce
Alpha
Theta
Slope of AC load line = -1/Rc
IeRe
vout(t)
= 1VSin(wt)
Amplifying Action of RC-coupled Amplifier.

Figure 57.5

Index of Keywords and Terms

Keywords are listed by the section with that keyword (page numbers are in parentheses). Keywords do not necessarily appear in the text of the page. They are merely associated with that section. *Ex.* apples, § 1.1 (1) **Terms** are referenced by the page they appear on. *Ex.* apples, 1

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