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1394 Open HCI
Isochronous Transmit DMA

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1394 HCI PEN

Agenda

- Context Programs (Descriptors)
- Command & Control
- Timing & Cycle Loss
- Using the IT DMA
- Packet Data Format

Isoch Transmit Context Program (Descriptors)

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IT Descriptors

- Five descriptors to choose from
  - OUTPUT_MORE
  - OUTPUT_MORE-Quadlet
  - OUTPUT_LAST
  - OUTPUT_LAST-Quadlet
  - STORE_VALUE
- One Z Block per packet (cycle)

Descriptors for a Typical Packet

- Use OUTPUT_MORE-Quadlet to send 4-byte Isoch packet header
  - Headers are specified by software (not synthesized), one per packet
- Use OUTPUT_MORE for payload blocks (optional, up to six)
- Use OUTPUT_LAST for final payload block

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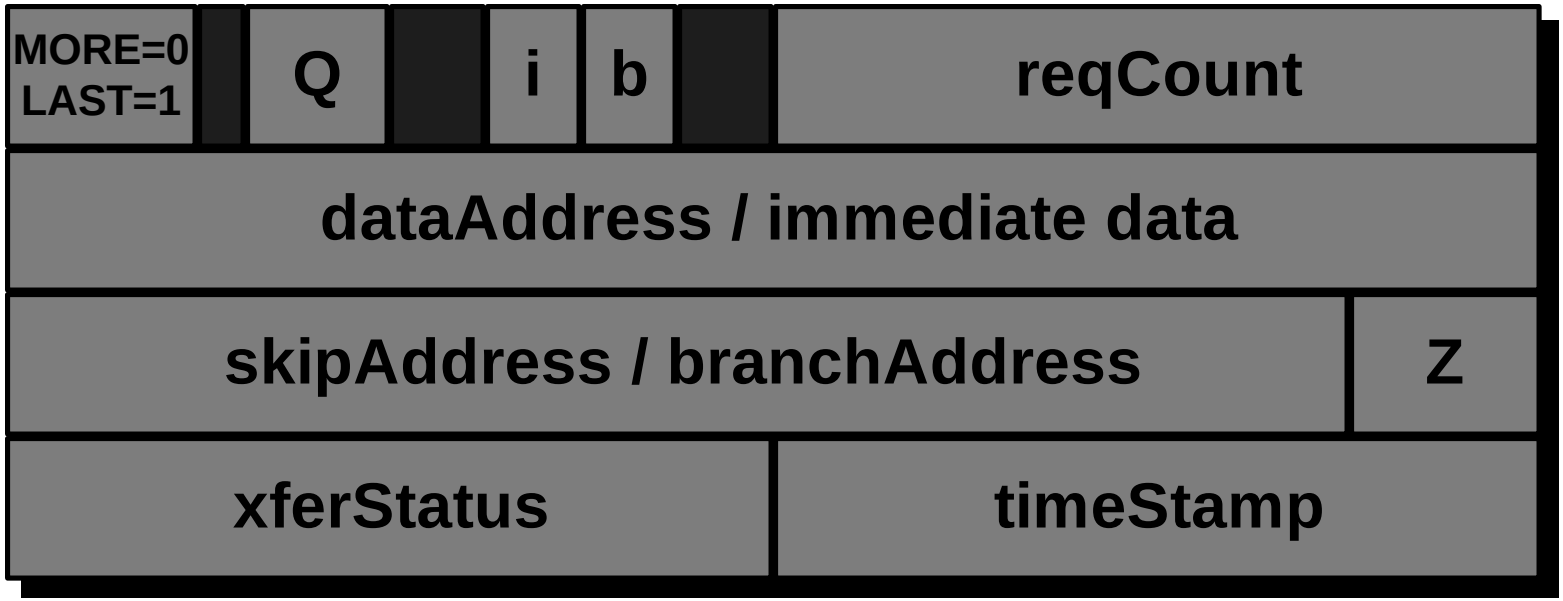
OUTPUT Descriptors



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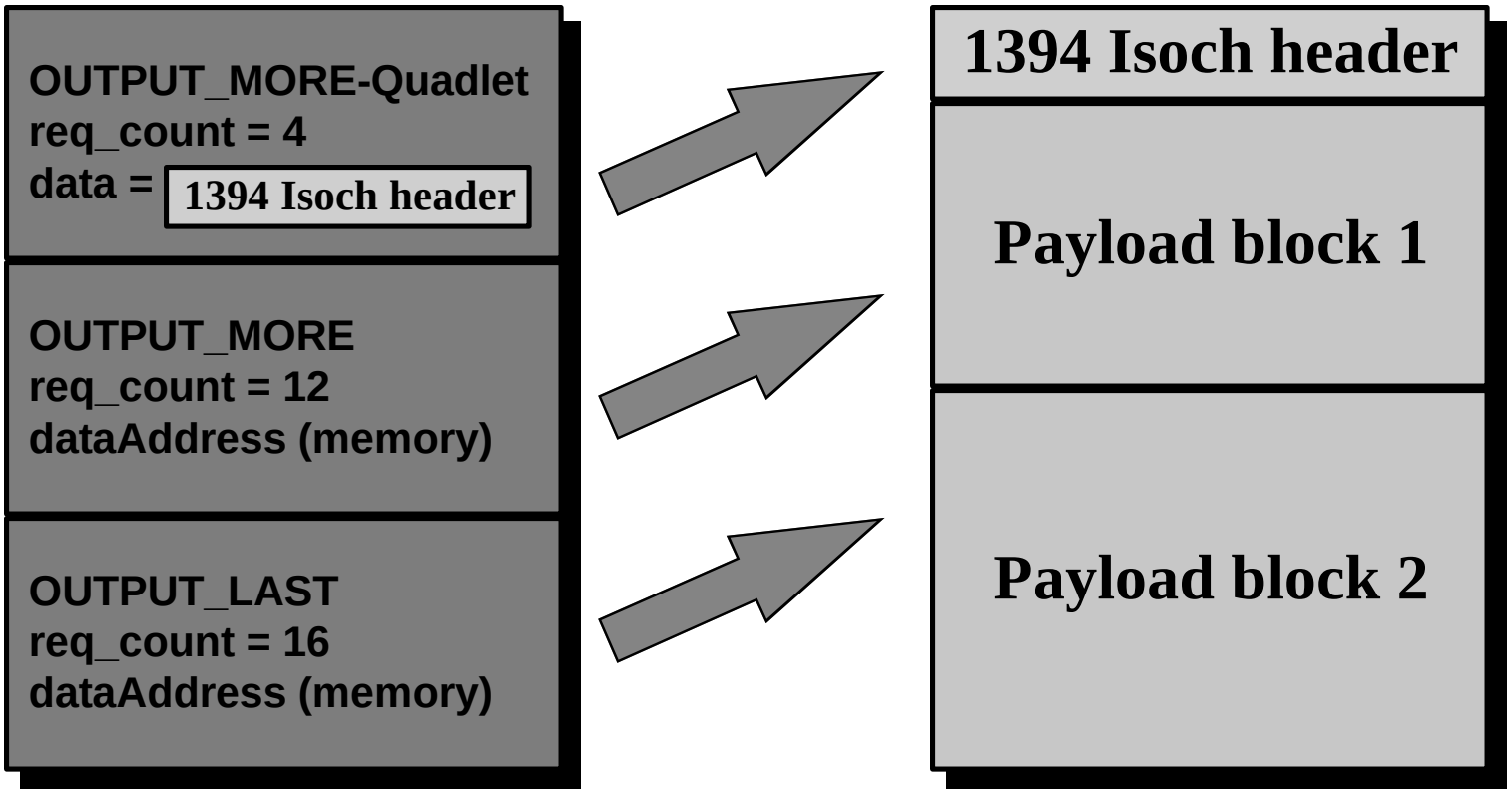
Typical Packet



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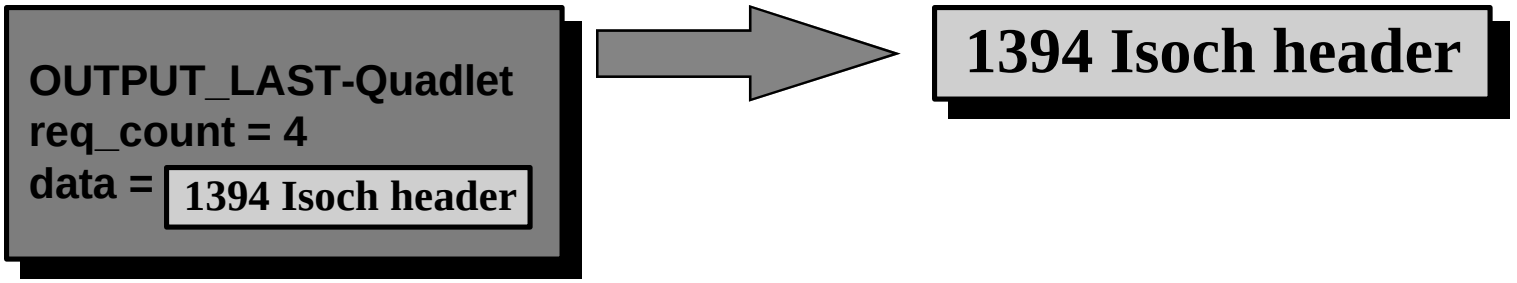
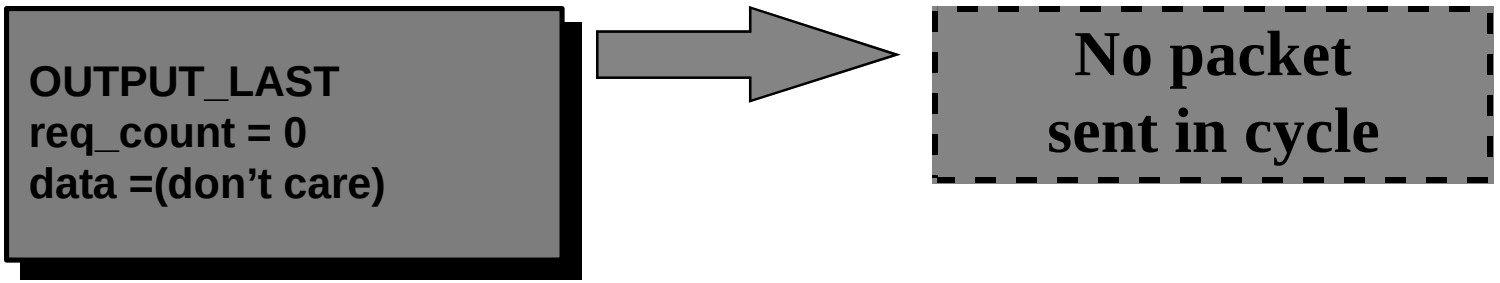
Empty Packet



No Packet



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STORE_VALUE

- Optional, once per Z Block
- First descriptor in block
- Stores immediate value to memory
  - 16-bit value (reqCount field)
  - Target is 32-bit location, 32-bit aligned
  - Writes zeroes to high 16 bits of target, immediate value to low 16 bits of target

STORE_VALUE Descriptor

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Packets & Cycles

- One Z Block per isochronous cycle
  - Descriptors contiguous in memory
  - Sends 0 or 1 packets (usually 1)
- Regular and Skip branches
  - Regular branch in final descriptor
  - Skip branch in first descriptor
  - Branch has Z value of target Z Block
  - Branch Z = 0 to end program

Isoch Transmit Command & Control

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Command Pointer

- To start an isoch transmit context:
  - Load CommandPtr register
  - Set run bit in Control register
- When a context stops (active = 0), CommandPtr indicates end location

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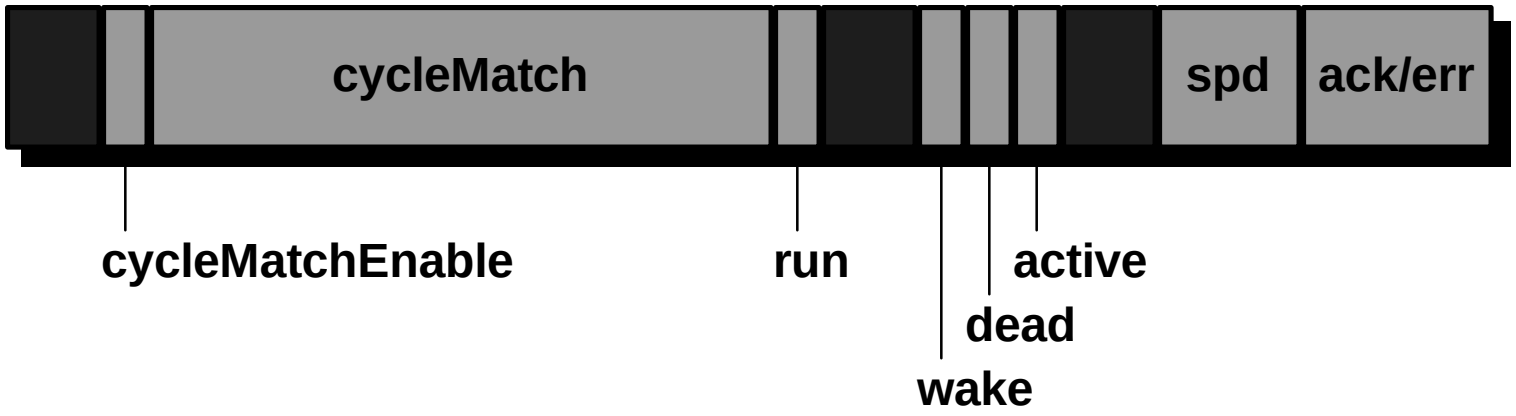
Context Control



- Set run to start immediately
- Set run and cycleMatchEnable to start on cycle # cycleMatch

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Multiple Channels

- Implement 4 to 32 Contexts
  - Determine count via isoXmitIntMask
- Each Context...
  - Has one CommandPtr
  - Has one ContextControl
  - Should transmit on one isoch channel
  - Has one interrupt bit

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Interrupts

- One (isochTx) in IntEvent register
- Per-Context interrupt bits
  - isoXmitIntEvent
  - isoXmitIntMask (also context count)
  - isochTx = ((Event & Mask) != 0)
- Interrupts triggered by OUTPUT_LAST with i = 3

Isoch Transmit Timing & Cycle Loss

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IT DMA Timing

- Goal: Process one Descriptor Block per Context after each CycleStart packet is sent or received
- Goal: Have data in FIFO before CycleStart
- Consequence: IT DMA works ahead
- Interrupts may preceed transmission

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Synchronization

- Typically, some Contexts are running, and some are not
- Contexts can start / stop at any time
- Start on specific cycle, or immediate
  - Specify start cycle # in ContextControl
- Stop on Z = 0, error, or immediate

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Cycle Loss

- Isochronous cycle on bus can be lost
  - Bus reset from 1394-1995 device
- IT DMA can compensate
  - Skip packets
  - Delay packets
  - Stop Context
  - Method is Context-specific

Cycle Loss (2)

- **Each Z Block has skipAddress**

This branch is taken (instead of transmitting) when the intended transmit cycle is lost

This branch is taken after a packet is transmitted normally

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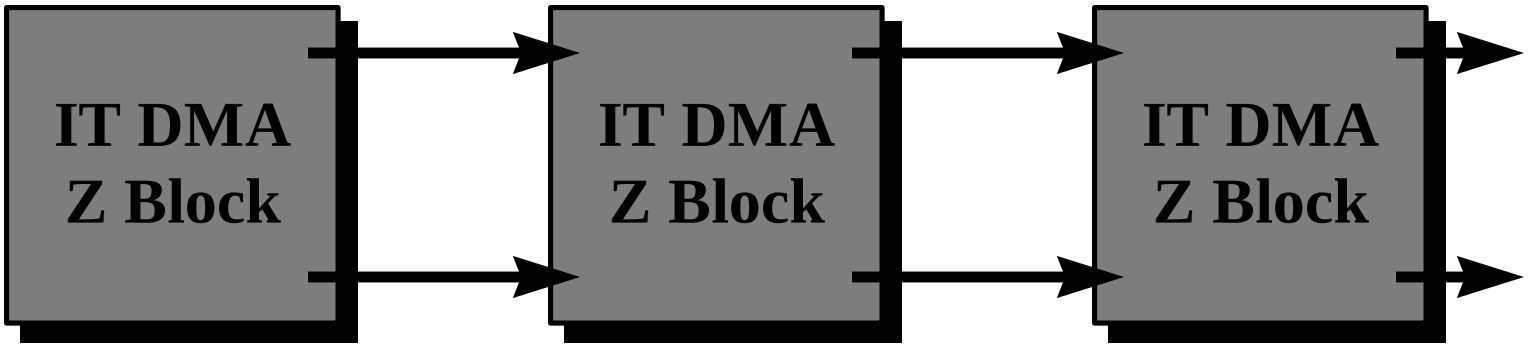
Skip on Loss

- **This program skips packets to compensate for cycle loss**



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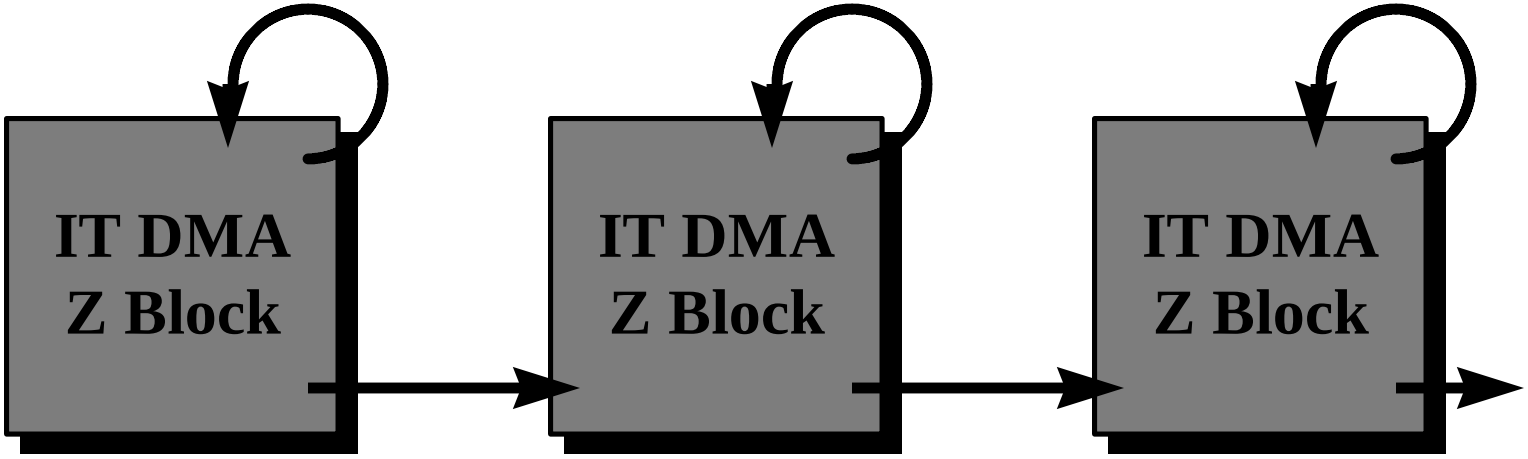
Delay on Loss

- **This program delays packets to compensate for cycle loss**



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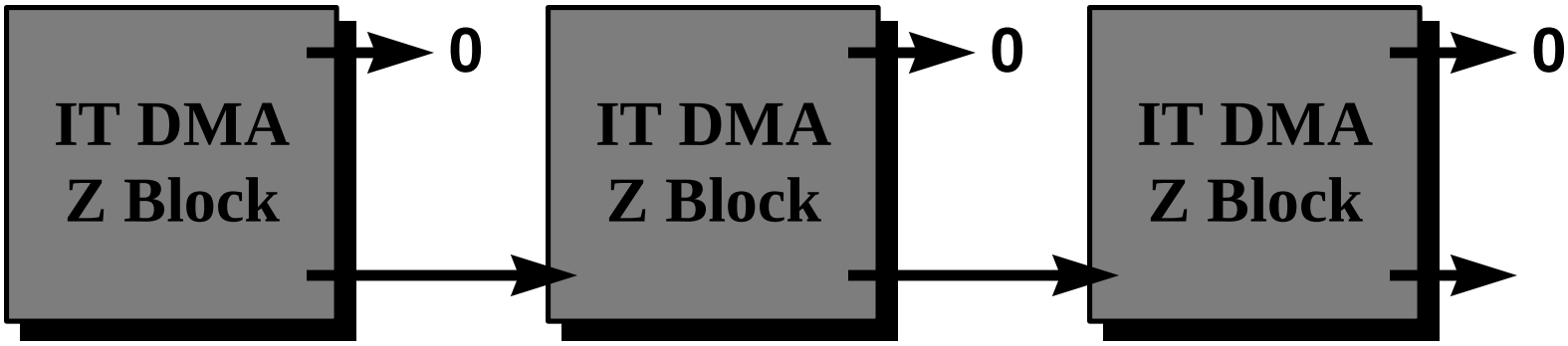
Stop on Loss

- **This program stops in the event of cycle loss (skipAddress Z = 0)**



Isoch Transmit Using the IT DMA

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9.3.3, 9.4, etc.

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Using the IT DMA

- Iso Transmit may continue for hours
- Not possible to have all data or all descriptors in host memory at start
- Common solutions:
  - Write descriptor loop, refresh data
  - Append descriptors on the fly
  - Either way, use interrupts for timing

Using the IT DMA (2)

- Choose cycle loss (skipAddress) per Context, based on application
- Set packet header (channel number, sync bits, tag, etc.) per packet
- One packet (or none) per Z Block

Isoch Transmit Packet Data Format

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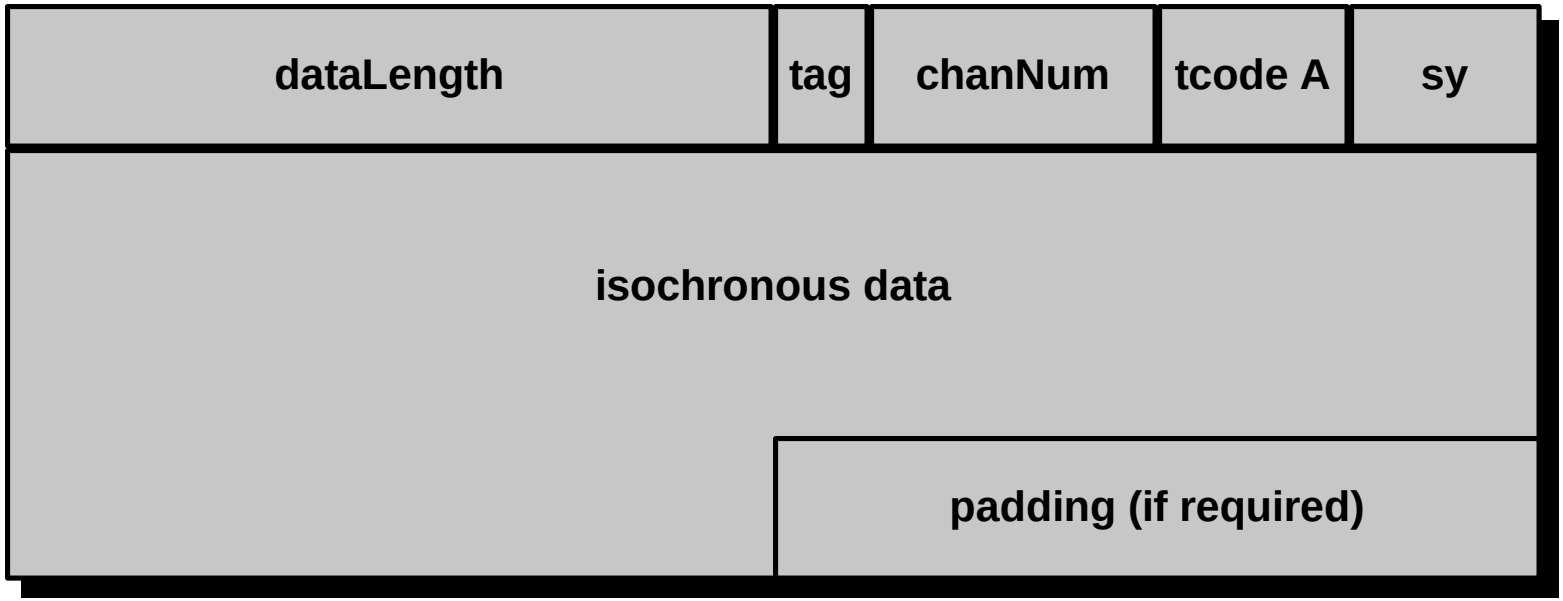
Packet Format



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Z = 0

(End)