IBM @server pSeries 620 Model 6F1

Technical Overview and Introduction

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IBM

IBM @server pSeries 620 Model 6F1

The pSeries product line is part of the IBM @server brand - a new generation of servers featuring unmatched availability and scalability, broad support of open standards for the development of portable new applications, and IBM @server Advantage for managing the unprecedented demands of e-business.

On April 17 2001, IBM introduced the IBM @server pSeries 620 Model 6F1 and IBM @server pSeries 660 Model 6H1 to enhance the mid-range server lineup with products using many of the design elements that led to the success of the high-end pSeries Model 680.

Overview

While the pSeries 620 Model 6F1 and pSeries 660 Model 6H1 are the systems that provide a growth path for existing installations of IBM RS/6000 Model F80s and H80s, the Model M80 is designed to provide leadership performance among the mid-range 8-way systems.

In addition to providing CPU and I/O expandability, the Model 6F1 combined with the latest storage technology provides the maximum internal storage capability available among the current line of IBM @server pSeries mid-range servers.

This paper discusses, in detail, the processor, memory, I/O, expandability, reliability, and other technical aspects related to Model 6F1.

An update to this paper, indicated by the change bars, was made to reflect the new processor features available after April 9 2002.

pSeries 620 Model 6F1 Description

Model 6F1 is a member of the 64-bit family of symmetric multiprocessing (SMP) servers from IBM. The Model 6F1 is a 64-bit deskside system, that can be configured as a 1-, 2-, or 4-way 450 MHz RS64 III, as a 1-, 2-, or 4-way 600 MHz RS64 IV, 6-way 668 MHz RS64 IV, or as a 1-, 2-, 4-, or 6-way 750 MHz RS64 IV SMP processor with up to 32 GB of real memory.

Several available Model 6F1 configurations offer flexibility regarding the number of CPUs, memory DIMMs, 32- and 64-bit PCI adapters, and disk drives desired for a specific application or usage. The architecture allows 32- and 64-bit applications to run simultaneously.

Physical Package

The Model 6F1 is packaged in a rugged black deskside steel chassis. The Model 6F1 server includes a modular hot-swap disk subsystem that allows fast, easy addition and replacement of drives. It has a maximum internal storage capacity of 1.1 TB (880.8 GB hot-swappable) and the possibility to double this as new storage technologies are made available. The Model 6F1 has a flexible I/O subsystem including ten 64-bit hot-plug PCI slots. It is shipped with the internal adapters and devices installed and configured; software can also be pre installed if desired.

The Model 6F1 is designed to operate in a typical office environment with standard AC power at 100-127 volts or 200-240 volts. Model 6F1 systems are built with two standard internal hot-swappable power supplies that combine to provide ample power for any configuration. An optional third internal hot-plug power supply with two hot-plug fans can be ordered to provide redundant power and cooling, allowing the system to continue running in the event of a failed fan or power supply. In the event of one of the fans failing, the other fans increase their speed to provide sufficient cooling. The hot-plug fans are performance monitored by the SPCN (see “System Power Control Network (SPCN)” on page 18). The hot-plug power supplies and fans can be replaced concurrently if the optional redundant power is installed.

The dimensions of the Model 6F1 are 483 mm W x 728 mm D x 610 mm H (19.0” W x 28.7” D x 24.0” H). The weight is from 70 kg (155 lbs) to 95 kg (209 lbs) depending on the configuration. Similar to the Model F80, the Model 6F1 does not provide rollers.

The Model 6F1 is designed for customer setup of the machine and for subsequent addition of most features.

Figure 1 shows three quarters view of a Model 6F1 showing the location of the major features. A discussion of these features follows.

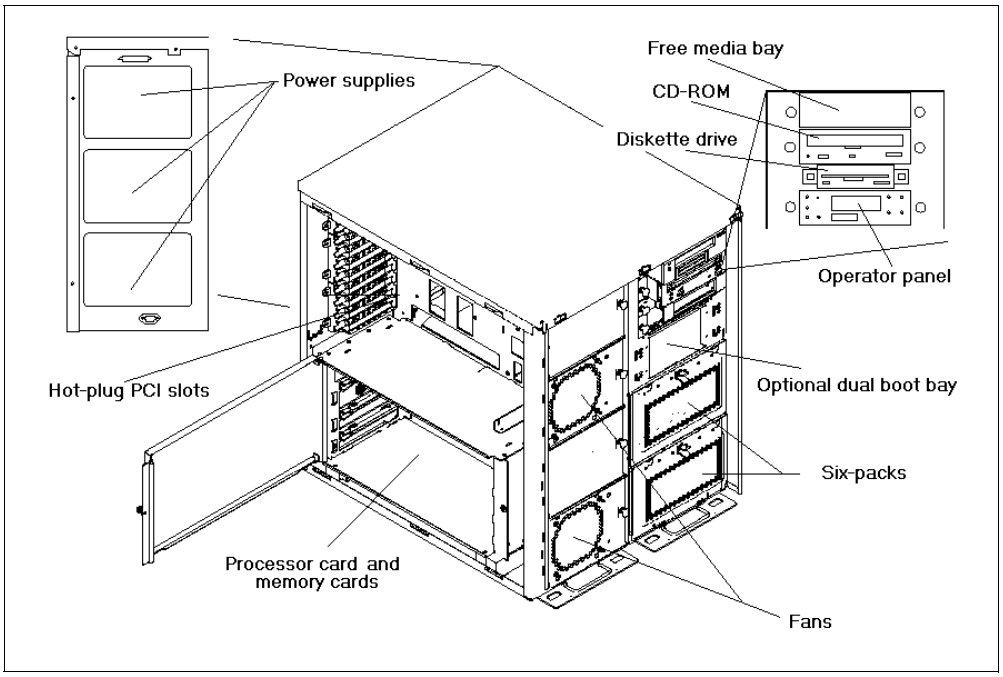


Figure 1. Model 6F1 Overview

On the lower section of the chassis are three slots on the backplane used for the processor card (top slot) and the two possible memory cards (middle and bottom slots). A *dummy* memory card is installed in all shipped units for each unused memory slot for safety and proper machine cooling.

The following ports are provided by Model 6F1 as shown in Figure 2:

- One Ultra2 SCSI port for external attachment use (mini 68-pin VHDCI[1] connector)

  The industry standard VHDCI 68-pin connector on the backside of the Model 6F1 allows attachment of various LVD and SE external subsystems. A 0.3 meter converter cable, VHDCI to P, mini-68 pin to 68-pin, (# 2118) can be used with older external SE subsystems to allow a connection to the VHDCI connector.
- 10/100 Mb/s Ethernet port (RJ-45 connector)
- Four serial ports (max. 230 KB/s, 9-pin D-shell)

  Serial ports one and two can only be used for service processor menus. No “heartbeat-type” devices can be used on these ports. “Heartbeat-type” devices or cables must be installed on serial port three or serial port four.
- One parallel port (bi-directional)
- Test port

  The test port is for diagnostics and is normally covered with a metal plate. It uses the same connector as the parallel port. To avoid confusion, this port should remain covered.
- Keyboard and mouse port
- Pass through port for cabling internal devices to external adapter ports.

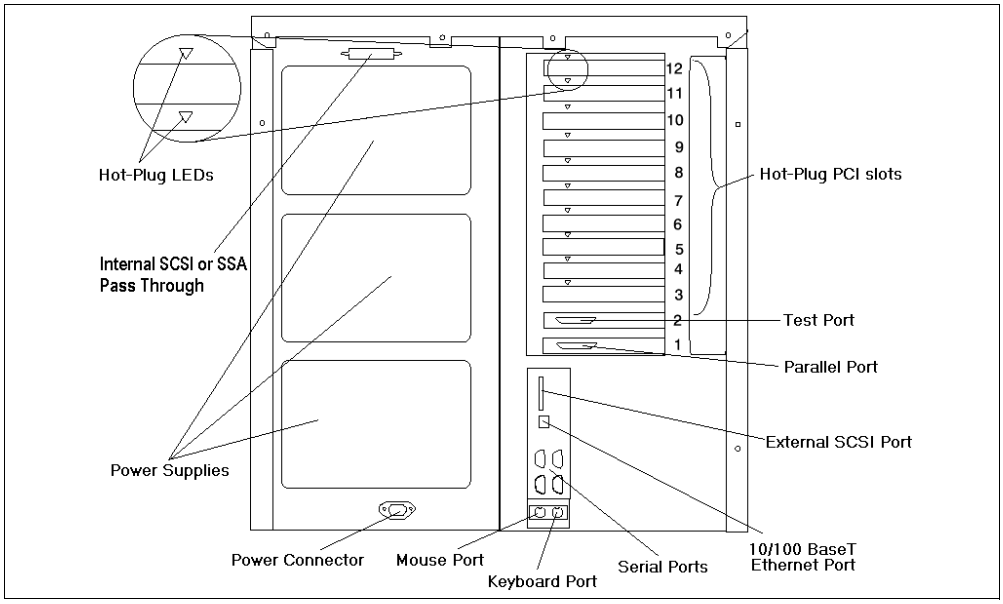


Figure 2. Model 6F1 Rear View

Internal Storage

The system comes preconfigured with a CD-ROM, diskette drive, and one free media bay for customer expansion, such as a tape device. Any devices in the media bays are connected to the internal F/W SCSI controller (no additional cable is required).

[1] Very High Density Cable Interconnect (VHDCI)

The Model 6F1 features two six-packs providing 12 hot-swap disk bays and an additional boot disk bay for two additional disks (not hot-swappable). The two six-packs can be either equipped with a SCSI backplane (# 6553) or SSA backplane (# 6554). SCSI and SSA six-packs can be mixed.

The SCSI backplane supports one inch and 1.6 inch drives. If the older 1.6 inch drives are used, these occupy two adjacent bays. The new SCSI carrier has one of two interposers between the drive and backplane, depending on whether the drive is 68-pin or 80-pin SCSI. All SCSI drives sold new with a Model 6F1 are 80-pin drives.

SCSI RAID is supported for the *under-the-cover* disks, but requires the addition of a SCSI RAID adapter. To cable a second internal SCSI RAID six-pack, a cable assembly is attached to an external SCSI port on the SCSI RAID adapter, run through a pass through opening in the rear bulkhead on the power supply side of the backpanel, and attached to the SCSI backplane.

SSA disks require the addition of an SSA adapter. To cable internal SSA, a cable assembly is attached to two external ports on the SSA adapter. This runs through a pass through opening in the rear bulkhead on the power supply side of the backpanel and is attached to both ends of the SSA backplane. When using both SSA six-packs, the cable runs to one end of each of the two backplanes with a short SSA cable in between the two backplanes. These configurations provide a loop, which is part of the SSA architecture. The SSA six-pack requires dummy jumper cards in vacant bays to maintain the SSA loop, and so can only support one inch drives. Booting from SSA disks attached to an Advanced SerialRAID adapter (# 6230) is supported from the six-pack or external SSA disks provided that the disks are arranged in a non-RAID configuration.

The optional dual boot bay holds a two-pack located between the operator panel and the top six-pack of the cabinet (D13, D14 in Figure 3). They are SCSI drives attached to the same carriers as are used for the six-packs. They plug into a backplane in the two-pack that does not support hot-swap, but may be inserted while the hardware is powered on. The backplane is designed in such a way that the two disks can either be part of the same SCSI bus or attached to different SCSI busses to support mirroring of the boot image. The disks should have 80-pin connectors so that a flex interposer between the disks and the backplane is unnecessary. These two disks do not impact the two six-packs, so the six-packs can be used, for example, in a RAID configuration. If the dual boot bay option is not installed, one of the six-packs will not be able to provide RAID, because booting from RAID disks is not supported.

Figure 3 shows the internal devices and bays of a Model 6F1.

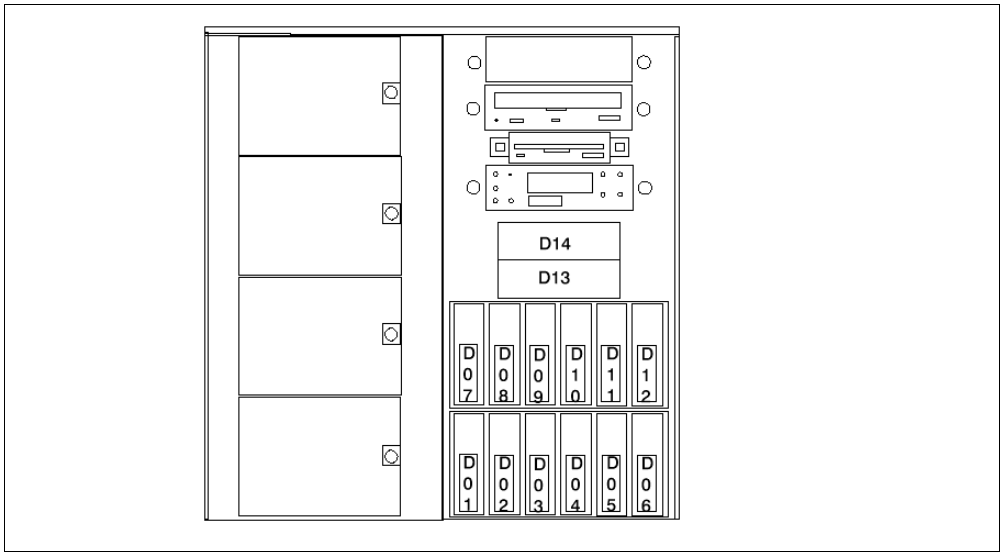


Figure 3. Internal Devices and Bays of the Model 6F1

Operator Panel

The Model 6F1 cabinet incorporates the operator panel and indicators for the system. The panel consists of the following features (see Figure 4):

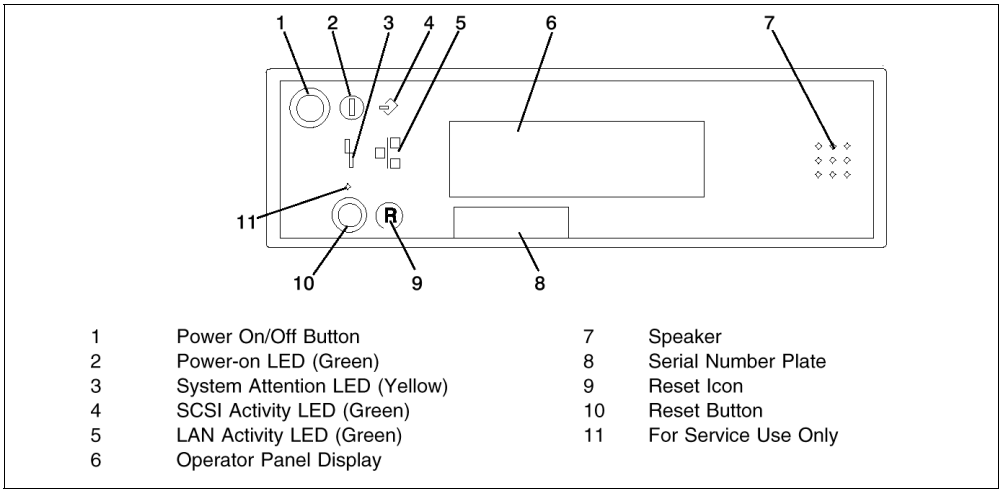
- Power On/Off Button
- Power-on LED (Green)
- System Attention LED (Yellow)

  This LED indicates to a user that there is an attention condition on the system.
- System Activity LEDs (Green)

  These LEDs report the status of the integrated SCSI and Ethernet ports.
- Operator Panel Display

  The display has two lines of sixteen characters each. The display shows reference codes from the service processor, the SPCN, and the operating system. These codes can be either informational codes or error codes. Informational codes will have the System Attention LED off; and error codes will have the System Attention LED on.
- Service Processor Reset Button

  The service processor reset button is a single execution button used to reset the service processor and bring the system back into standby mode. Access to this button is restricted by only having access to this button through a *pinhole* in the operator panel cover. This button is for service use only.
- Speaker (beeper)



1	Power On/Off Button	7	Speaker
2	Power-on LED (Green)	8	Serial Number Plate
3	System Attention LED (Yellow)	9	Reset Icon
4	SCSI Activity LED (Green)	10	Reset Button
5	LAN Activity LED (Green)	11	For Service Use Only
6	Operator Panel Display		

Figure 4. Operator Panel

System Architecture and Technical Overview

Figure 5 shows the system schematic of the Model 6F1. In this section, the different physical components in the schematic and the SMP processor configurations are discussed.

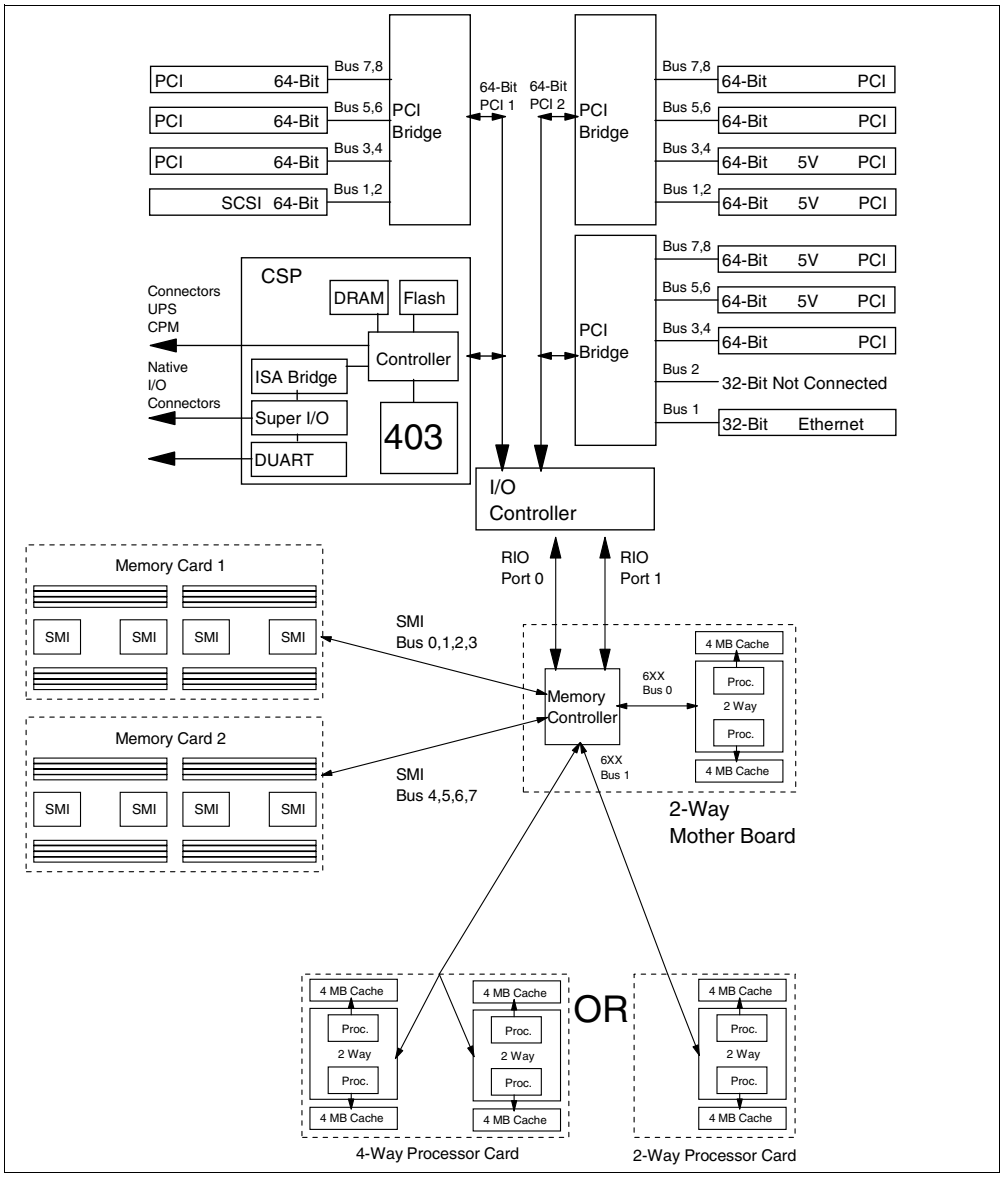


Figure 5. RS/6000 Model 6F1 System Schematic for 2-, 4-, or 6-Way 600 or 668 MHz SMP

CPU Architecture

The key components in the CPU include the processor, the processor packaging, memory controller, memory subsystem, and the I/O interface.

RS64 IV RISC Processor

The RS64 IV processor card used in the Model 6F1 has the following attributes:

- 600 MHz, 668 MHz, or 750 MHz operating frequency
- 128 KB on-chip L1 instruction cache, 2-way associative with parity and retry for data integrity
- 128 KB on-chip L1 data cache with ECC, 2-way associative
- On-chip L2 cache directory with ECC

- 8 MB of off-chip L2 cache using ECC double data rate (DDR) SRAM per processor for 6-, 4-, 2-, 1-way at 750 MHz, 8 MB of off-chip L2 cache using ECC double data rate (DDR) SRAM per processor for 6-way SMP at 668 MHz, 4 MB of off-chip L2 cache using ECC double data rate (DDR) SRAM per processor for 2- and 4-way SMP at 600, and 2 MB of off-chip L2 cache using ECC Single Data Rate (SDR) SRAM for a 1-way system at 600 MHz.
- PowerPC 6xx bus architecture, 16-byte wide bus interface

The RS64 IV processor is available in three operating frequencies: 600 MHz, 668 MHz, and 750 MHz. The frequency is accomplished by leveraging IBMs copper (CMOS 8S) and silicon-on-insulator (SOI) technology.

The copper technology and an improved manufacturing process allow the chip to operate at 1.8 V. The lower operating voltage coupled with the smaller circuit dimensions result in reduced wattage in the RS64 IV and allow additional function to be placed on the chip.

The size of the level one (L1) instruction and data caches is 128 KB each. Innovative custom circuit design techniques were used to maintain the one cycle load-to-use latency for the L1 data cache. The level two (L2) cache directory was integrated into the RS64 IV chip, reducing off-chip accesses that impact performance.

IBM uses double data rate (DDR) SRAM technology for the L2 cache in the RS64 IV processor. DDR technology provides two transfers of data on the 16-byte wide L2 data bus every SRAM clock cycle. The DDR SRAM technology also reduced L2 access latency as measured in nanoseconds. This technology allows L2 access to perform at processor clock speed.

Hardware multi-threading (HMT)

The RS64 IV supports the Hardware Multi-threading (HMT) concept wherein two logical processors share one physical hardware processor. Hardware multi-threading provides a mechanism of improving overall system throughput by overlapping memory access with other computation. AIX Version 4.3.3 and AIX Version 5.1 support HMT. It is enabled by the `bosdebug -H on` command and activated on subsequent reboot. When invoked, AIX presents the system as having twice as many processors as are physically installed. Each has typically a little more than one half the performance of a non-HMT system. HMT does not work on Single Processor systems. For further information, see /usr/lpp/bos/README.HMT as shipped with the AIX operating system.

Processor Boards

The processor boards used in the Model 6F1 for 1-, 2-, 4-, and 6-way SMP configurations come in the form of a single book, and are described as follows:

Single Processor 600 MHz

As shown in Figure 6, a single processor board consists of a single RS64 IV processor operating at 600 MHz, on-board memory slots, and a memory controller in a single book consisting of a motherboard and an empty daughter card. Upgrades to additional processors require

changing of the processor book. However, the single processor board is a cost-reduced package.

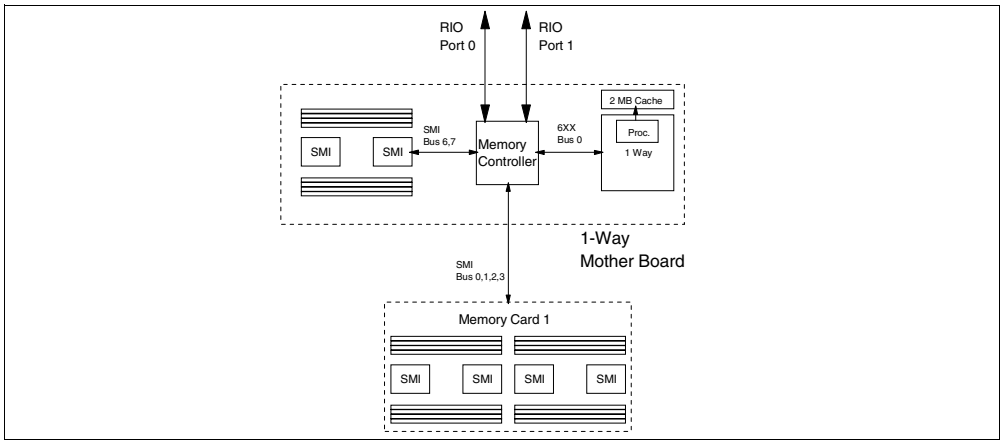


Figure 6. RS/6000 Model 6F1 System Schematic for 1-Way Processor

2- and 4- Way SMP 600 MHz

A 2-way SMP configuration is provided by a processor board consisting of a pair of RS64 IV processors operating at 600 MHz and a memory controller. Expansion to 4-way SMP is provided by interfacing an additional processor board consisting of a pair of RS64 IV processors operating at 600 MHz. However, the upgrade from 2-way to 4-way SMP is offered as a book swap, because the interface between the mother card and daughter card requires a factory tolerance that is unable to be reproduced in the field.

6-Way SMP 668 MHz

A 6-way SMP configuration uses two processor boards interfaced to each other. One processor board consists of a pair of RS64 IV processors operating at 668 MHz and a memory controller. The other processor board consists of four RS64 IV processors operating at 668 MHz. Upgrades from a 2- or 4-way SMP to a 6-way SMP are offered as a book swap because the interface between the mother card and daughter card requires a factory tolerance that is unable to be reproduced in the field.

1-, 2-, 4-, and 6-Way SMP 750 MHz

The new processors are offered on 1-, 2-, 4-, and 6-way cards running at 750 MHz. The Level 2 cache per processor is 8 MB for all 750 MHz processor cards. A mew manufacturing process enables IBM to place processor modules on to a single motherboard for the 4-way and 6-way configurations as shown in Figure 7 on page 10. 1- and 2-way cards are manufactured as before. Elimination of the mother/daughter card connector dramatically increases the reliability.

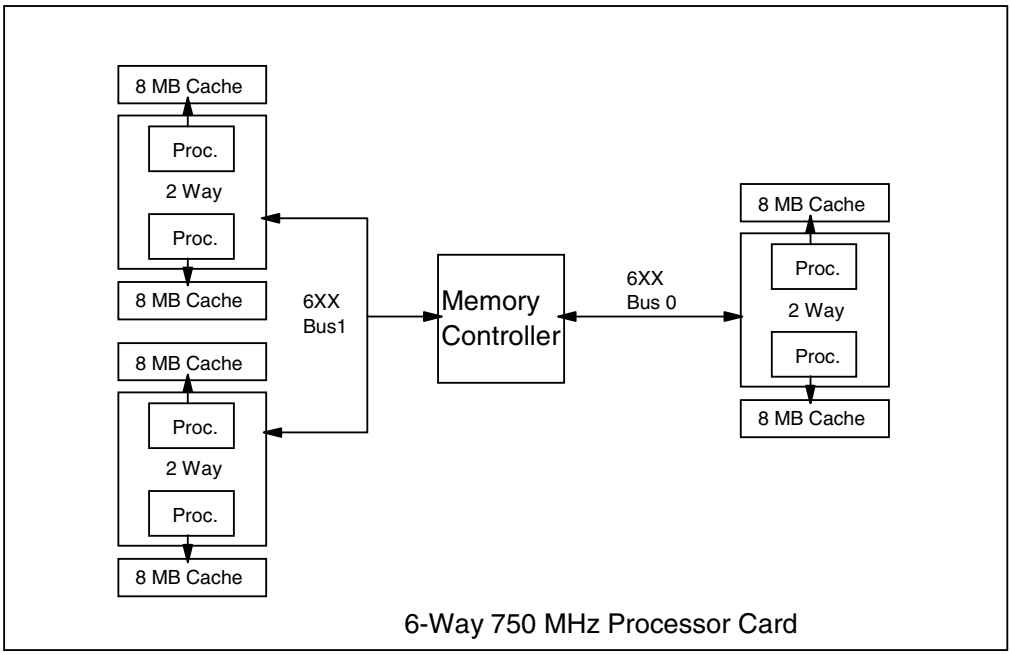


Figure 7. pSeries 620 Model 6F1 System Schematic for 6-Way Processor 750 MHz

Memory Controller

A single custom chip provides the function of the memory controller and the I/O hub in the Model 6F1. The controller chip provides interfaces to processors, memory, and the I/O subsystem.

The RS64 IV processors on the processor boards are connected to the memory controller through the PowerPC 6xx bus. The controller chip is a part of the first processor board. The memory controller provides a single 6xx bus interface in a single processor configuration. For 2-way SMP configurations, the controller provides a 6xx bus interface to the pair of RS64 IV processors present in the same board. The memory controller provides another 6xx bus interface for CPU expansion using an additional processor board. The 4- and 6-way SMP configurations consists of a total of two processor boards that use the two 6xx bus interfaces provided by the memory controller installed together in a book.

In the Model 6F1, the 6xx bus is a 16-byte wide bus, the operating clock rate of which depends on the processor clock speed. The 6xx bus operates at a clock rate of 150 MHz with a processor clock speed of 600 MHz or 750 MHz. For a processor clock speed of 668 MHz, the 6xx bus operates at a clock rate of 133.6 MHz.

Memory Subsystem

The memory controller provides two memory bus interfaces and provides the reliability functions of ECC as well as memory scrubbing. Memory scrubbing provides a built-in hardware function designed to perform continuous background reads of data from memory to check for correctable errors. The memory configuration for a single processor configuration and 2-, 4-, or 6-way configurations is:

- In a single processor configuration, the on-board memory, consisting of eight DIMM slots, is interfaced to one of the two memory interfaces in the controller.

The other interface is used by a separate riser memory card. The riser memory card provides 16 DIMM slots. While the DIMM slots in the on-board memory are populated in pairs, the slots in the riser memory card are populated in quads. The minimum configuration requires a pair of DIMMs in the on-board memory. Once the on-board memory slots are filled and more memory capacity is desired, the DIMMs are moved to the riser memory card and the next increment is made as a quad. The single processor configuration can provide a maximum memory of 16 GB by using the riser memory card and populating each of the 16 slots with 1024 MB DIMMs.

- In 2-, 4-, or 6-way SMP configurations, the memory is provided using two separate riser memory cards, each with 16 DIMM slots and populated with DIMMs in quads. The two riser cards are interfaced to the two memory interfaces on the memory controller. The minimum 2-way SMP configuration requires a single riser memory card populated with a quad of DIMMs. The second riser memory card with minimum of a quad of DIMMs can be configured only after the 16 DIMM slots in the first riser memory card are fully populated. 2-, 4-, or 6-way processor configuration can support up to 32 GB maximum memory by using the two memory riser cards fully populated with 1024 MB DIMMs.

The Model 6F1 uses 200-pin 10ns SDRAM DIMMs. DIMMs of equal sizes must be used while populating in pairs or quads. DIMM size used in one pair or quad can, however, coexist with a different DIMM size used in another pair or quad.

In the Model 6F1, the bus interface from each riser memory card to the memory controller is 8-bytes wide (two interfaces each 4-bytes wide) and operates at a clock rate of 300 MHz or 267.2 MHz. No additional memory bandwidth can be achieved by splitting memory between cards.

Bus Bandwidth

The following are the theoretical maximum bandwidths as applicable for a 6-way 668 MHz SMP configuration:

- Memory port bandwidth: 2.14 GB/s
- Processor port bandwidth: 2.14 GB/s
- Total I/O bandwidth: 1 GB/s (500 MB/s bi-directional)

The following are the theoretical maximum bandwidths applicable for 2-, or 4-way 600 MHz SMP configurations:

- Memory port bandwidth: 2.4 GB/s
- Processor port bandwidth: 2.4 GB/s
- Total I/O bandwidth: 1 GB/s (500 MB/s bi-directional)

The following are the theoretical maximum bandwidths as applicable for 1-, 2-, 4-, or 6-way, 750 MHz SMP configurations:

- Memory port bandwidth: 2.4 GB/s
- Processor port bandwidth: 2.4 GB/s
- Total I/O bandwidth: 1 GB/s (500 MB/s bi-directional)

I/O Hub Function

The memory controller also functions as the I/O hub. The controller provides two RIO (remote I/O) ports. The two RIO ports are attached to an I/O host bridge chip. Each RIO port has two uni-directional 1-byte wide links. All the I/O transfers take place using one primary RIO port, which operates at 500 MHz (500 MB/s bi-directional or an aggregate of 1 GB/s). The controller uses the other RIO port, which operates at 500 MHz (500 MB/s bi-directional or aggregate of 1 GB/s), as a fail-over to the primary RIO port. In contrast to Model 6H1 or Model M80, these RIO connections in the Model 6F1 are not visible outside the cabinet, but the function is the same.

Internal I/O Architecture

As already discussed, the system includes one I/O host bridge chip managing all the I/O between the I/O adapters and the memory controller using RIO connections. On the other side, the I/O host bridge provides two primary PCI busses operating at 66 MHz with a width of 64 bits.

The service processor and a PCI-to-PCI bridge chip are connected to the first primary PCI bus. The PCI-to-PCI bridge provides three 64-bit hot-plug PCI slots and the onboard dual SCSI adapter (F/W SCSI-2 internal, Ultra2 SCSI external). A PCI-to-ISA bridge chip is connected to the service processor, providing an ISA bus. The ISA bus is used by the National Super I/O chip providing the floppy drive controller, two of the four serial ports, keyboard and mouse ports, and the parallel printer interface. A 16552 DUART[2] chip is also connected to the service processor, providing the other two serial ports.

The second bus is connected to another two PCI bridges, which provide another seven 64-bit hot-plug PCI slots. The onboard 10/100 Mb/s Ethernet adapter is connected to this chip.

Each slot represents a separate PCI bus, which simplifies the hot-plug function. Figure 8 shows the design of the I/O architecture.

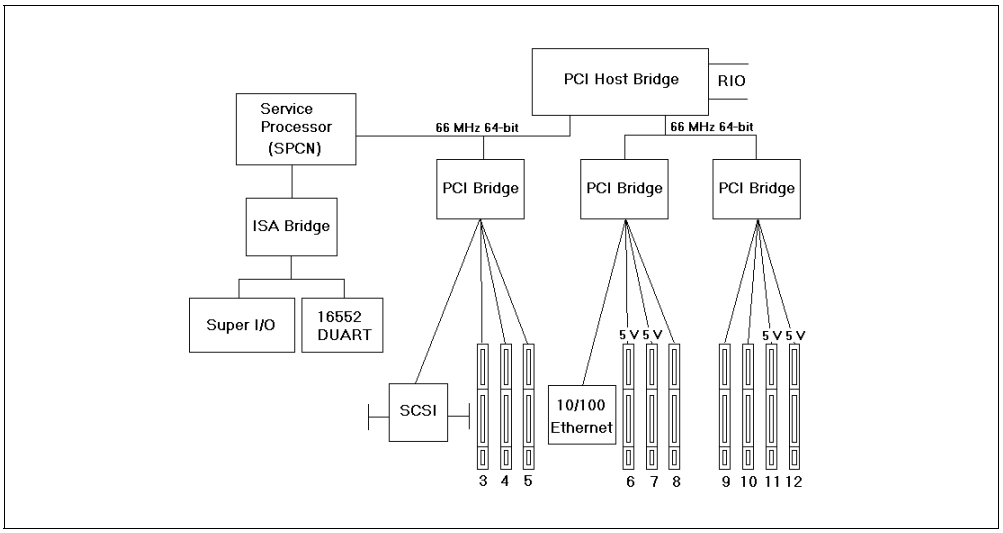


Figure 8. Internal Architecture of Model 6F1

[2] Dual Universal Asynchronous Receiver-Transmitter (DUART)

PCI Slots

All PCI slots are PCI 2.2 compliant and are hot-plug enabled, which allows most PCI adapters to be removed, added, or replaced without powering down the system. This function enhances system availability and serviceability.

Six 64-bit slots operate at 3.3 V signaling at 66 MHz, in contrast to the four 64-bit slots that operate at 5 V signaling at 50 MHz (see Figure 8). When adding adapters to the system, it is important which signaling the adapter works: 3.3 V, 5 V, or universal, which means the adapter works at both voltages. That is, for example, the reason why a PCI 3-Channel Ultra2 SCSI RAID Adapter (# 2494) can be placed only in slots 6, 7, 11, or 12. Refer to the *PCI Adapter Placement Reference Guide*, SA38-0538 for further information.

32-bit versus 64-bit PCI Slots

Choosing between 32-bit and 64-bit slots influences slot placements and affects performance. Higher-speed adapters use 64-bit slots because they can transfer 64 bits of data in each data transfer phase.

32-bit adapters can typically function in 64-bit slots; however, 32-bit adapters still operate in 32-bit mode and offers no performance advantages in a 64-bit slot. Likewise most 64-bit adapters can operate in 32-bit PCI slots but the 64-bit adapters operate in 32-bit mode and reduce performance potential.

Hot-Plug PCI Adapters

The function of hot-pluggable PCI adapters is to provide concurrent additions or removals of PCI adapters when the system is running.

In the chassis, the installed adapters inside the slots are protected by plastic separators, designed to prevent grounding and damage when adding or removing adapters. The hot-plug LEDs outside the chassis indicate if a adapter can be plugged in or removed from the system. These LEDs are also visible inside the chassis. Inside, the light from the LED is routed to the top of the plastic separators, using light pipes, which makes it very easy to locate the right slot. The hot-plug PCI adapters are secured with retainer clips on top of the slots; therefore, you do not need a screwdriver to add or remove a card and there is no screw that can be dropped inside the chassis.

The function of hot-plug is not only provided by the PCI slot, but also by the function of the adapter. Most adapters are hot-pluggable, but some are not. Be aware that some adapters must not be removed when the system is running, such as the adapter with the operating system disks connected to it, or the adapter that provides the system console. Refer to the *PCI Adapter Placement Reference Guide*, SA38-0538 for further information.

To manage hot-plug PCI adapters, it is important to turn off slot power before adding, removing, or replacing the adapter, which is done by the operating system. There are three possibilities for managing hot-plug PCI slots in AIX:

- Command line:
  - `lsslot` - List slots and their characteristics
  - `drslot` - Dynamically reconfigures slots
- SMIT
- Web-based System Manager

When working with the commands and tools mentioned above, the hot-plug LEDs (see Figure 2) change their state. Table 1 provides the possible states of the hot-plug LEDs.

Table 1. Hot-Plug LED Indications

LED Indication	PCI Slot Status	Definition
Off	Off	Slot power is off. It is safe to remove or replace adapters.
On (not flashing)	On	Slot power is on. Do not remove or replace adapters.
Flashing slowly (one flash per second)	Identify	Indicates the slot has been identified by the software; do not remove or replace adapters at this time.
Flashing fast (six to eight flashes per second)	Action	Indicates the slot is ready for adding, removing, or replacing of adapters.

To add a hot-plug PCI adapter use the `drslot` command to set the slot first into the Identify state (LED flashes slowly) to verify the right slot was selected. After pressing **Enter,** the LED changes its state to the Action state (LED flashes fast). Then add the adapter to the system. When finished, press **Enter** again to turn on slot power. The hot-plug LED will change its state to On. Now the adapter is integrated into the system and can be configured using AIX `cfgmgr` (configuration manager).

Removal of adapters requires deconfiguration in AIX first. The adapter must be in a defined state or removed from the ODM.

Figure 9 shows an example of adding a hot-plug PCI adapter to a running system.

```
# lsslot -c pci
# Slot Description                       Device(s)
P1-I3  PCI 64 bit, 66 MHz, 3.3 volt slot  Empty
P1-I4  PCI 64 bit, 66 MHz, 3.3 volt slot  Empty
P1-I5  PCI 64 bit, 66 MHz, 3.3 volt slot  ent1
P1-I6  PCI 64 bit, 50 MHz, 5 volt slot    Empty
P1-I7  PCI 64 bit, 50 MHz, 5 volt slot    Empty
P1-I8  PCI 64 bit, 66 MHz, 3.3 volt slot  scsi2, scsi3
P1-I9  PCI 64 bit, 66 MHz, 3.3 volt slot  Empty
P1-I10 PCI 64 bit, 66 MHz, 3.3 volt slot  Empty
P1-I11 PCI 64 bit, 50 MHz, 5 volt slot    ssa0
P1-I12 PCI 64 bit, 50 MHz, 5 volt slot    Empty

# drslot -c pci -Ia -s P1-I6

The visual indicator for the specified PCI slot has
been set to the identify state. Press Enter to continue
or enter x to exit.

[Enter]

The visual indicator for the specified PCI slot has
been set to the action state. Insert the PCI card
into the identified slot, connect any devices to be
configured and press Enter to continue. Enter x to exit.

[Enter]
```

Figure 9. Adding a Hot-Plug PCI Adapter

Software Requirements

The Model 6F1 requires AIX Version 4.3.3 with the AIX 4330-10 recommended maintenance package (APAR IY17356), which is included on all pre-installed systems and on the 04/2002 Update CD that ships with AIX Version 4.3.3 as of April 2002 or AIX 5L Version 5.1 with 5100-02 maintenance package or later.

You can also download the actual maintenance level from the Internet to install the machine using NIM[3]. The URL to obtain the maintenance level is:

`http://techsupport.services.ibm.com/rs6k/fixes.html`

If you have problems downloading the latest maintenance level, ask your IBM Business Partner or IBM representative.

Investment Protection and Expansion

The following sections discuss how configurations, upgrades, and design features help you lower your cost of ownership.

High Availability

Reliability of the system is further hardened by using the HACMP clustering solution available across the entire range of RS/6000 and pSeries servers. The

[3] Network Installation Manager (NIM)

HACMP solution exploits redundancy between server resources and provides application uptime. The Model 6F1 is available in a high-availability cluster solution package named the HA-6F1. This solution consists of the following components:

- Two pSeries 620 Model 6F1 Enterprise Servers
- AIX Version 4.3.3 operating system (unlimited user license), or AIX 5L Version 5.1 (unlimited user license)
- HACMP 4.4.0 cluster software (APAR IY17684)
- One 7133-T40 SSA disk subsystem with at least four disk drives
- All necessary redundant hardware and cables

This solution is sold at a price lower than the sum of its parts. Ask your IBM Business Partner or IBM representative for further information.

Reliability, Availability, and Serviceability (RAS) Features

Some RAS features such as redundant power supplies or N+1 hot-plug fans have already been discussed. Additional topics are covered in the following sections.

Error Recovery for Caches and Memory

The RS64 IV processor L1 cache, the L2 cache, system busses, and the memory are protected by error correction code (ECC) logic. The ECC codes provide single bit error correction and double bit error detection for the L2 cache and the memory. All recovered error events are reported by an attention interrupt to the service processor, where they are monitored for threshold conditions.

The standard memory card has single error-correct and double-error detect ECC circuitry to correct single-bit memory failures. The double-bit detection helps maintain data integrity by detecting and reporting multiple errors beyond what the ECC circuitry can correct. In many cases (using DIMMs with 9 or 18 DRAM chips and when memory is configured in quads, for example), memory chips are organized such that the failure of any specific memory module only affects a single bit within an ECC word (bit scattering), thus allowing error correction and continued operation in the presence of a complete chip failure (Chipkill recovery).

Another function, named *memory scrubbing*, provides a built-in hardware function, that performs continuous background reads of data from memory, to check for correctable errors. Correctable errors are corrected and rewritten to memory, and a threshold counter is maintained that will signal the service processor with a special attention when the threshold is exceeded.

Chipkill

The Model 6F1 provides Chipkill Memory with selected memory options. Chipkill Memory protects the server from any single memory chip failure and multibit errors from any portion of a single memory chip. Memory chip failures can cause server system crashes that can result in the permanent loss of business data. Chipkill DIMMs for the Model 6F1 provide the self-contained capability to correct real-time, multibit DRAM errors, including complete DRAM failures. This technology provides enhanced multibit error detection and correction that is transparent to the system.

Note

The Chipkill Memory technology is not supported on the 256 MB (2 X 128 MB) Memory (#4110)

Dynamic Processor Deallocation

The processors are continuously monitored for errors such as L2 cache ECC errors. When a predefined error threshold is met, an error log with warning severity and threshold exceeded status is returned to AIX. At the same time, the service processor marks the processor for deconfiguration at the next boot. In the meantime, AIX will attempt to migrate all resources associated with that processor (tasks, interrupts, etc.) to another processor, and then stop the failing processor.

The capability of Dynamic Processor Deallocation is only active in systems with more than two processors, because device drivers and kernel extensions, which are common to multi-processor and uni-processor systems, would change their mode to uni-processor mode with unpredictable results. Dynamic processor deallocation is not supported when HMT is enabled.

Persistent Processor and Memory Deconfiguration

Processor and memory modules with a failure history are marked *bad* to prevent them from being configured on subsequent boots. This history is kept in the VPD[4] records on the FRU[5], so the information moves physically with the FRU and is cleared when the FRU is replaced, and stays with the failed FRU when it is returned to IBM. A CPU or memory module is marked bad when:

- It fails BIST[6]/POST[7] testing during boot (as determined by the service processor).
- It causes a machine check or check stop during runtime and the failure can be isolated specifically to that processor or memory module (as determined by the service processor).
- It reaches a threshold of recovered failures (for example, ECC correctable L2 cache errors, see the preceding) that result in a predictive call-out (as determined by service processor).

During CEC[8] initialization, the service processor checks the VPD values and does not configure CPUs or memory that are marked bad, much in the same way that it would deconfigure them for BIST/POST failures.

I/O Expansion (RIO) Recovery

The RIO interface supports packet retry on its interface, which means that it will automatically try to resend a packet if it gets no acknowledgment or a bad response until a time-out threshold is reached.

RIO also supports a closed loop topology configuration, which is required for pSeries products. RIO hubs will automatically attempt to reroute packets through the alternate RIO port if a successful transmission cannot be completed (for

[4] Vital Product Data (VPD)
[5] Field Replaceable Unit (FRU)
[6] Built-in self-test (BIST)
[7] Power-on self-test (POST)
[8] Central Electronic Complex (CEC)

example, the retry threshold is exceeded) through the primary port. Therefore, no single link failure in the RIO loop will cause the system to go down, although the failure will be reported for deferred maintenance.

PCI Bus Error Recovery

As described in the PCI slot section, every slot is connected through a PCI-to-PCI bridge chip to a primary PCI bus, therefore, each slot is logically and physically isolated onto its own individual PCI bus. This fact provides a special error handling mode that allows the bridge chip to *freeze* access to an adapter when a PCI bus error occurs on the interface between that adapter and bridge chip. In this frozen mode, DMAs[9] are blocked, stores to that device address space are discarded, and loads result in a return value of all 1s. Device drivers can be programmed to look for these dummy responses on loads and can attempt recovery. The AIX support for this function is not available yet.

System Power Control Network (SPCN)

SPCN consists of a set of power/environmental controllers, interconnected by a set of serial communication links. In Model 6F1 systems, the SPCN function is integrated into the service processor and provides the following functions:

- Powering all the system parts up or down, when requested.

  The SPCN hardware has connections to the VPD that are resident on each of the pluggable cards and the backplane. The VPD is located on each of the cards in the form of an I^2C[10] chip. This chip is accessed during initial power on sequence and the data contents are read by the service processor. Using this function, the service processor decides not to use components that are marked *bad.*

- Powering down all the system parts on critical power faults.
- Monitors power, fans, and thermal conditions in the system for problem conditions, which result in an EPOW. EPOW stands for environmental and power off warnings and is a function to inform the service processor or the operating system early, about a hardware event. There are different warnings; such as cooling warnings or power fail warnings that result in entries in the error log. If there is a serious error, such as the temperature reaches a specific limit, the system will be shut down.
- Reporting power and environmental faults, as well as faults in the SPCN network itself, on operator panels and through the service processor
- Assigning and writing location information into various VPD elements in the system.

Disk Redundancy (Mirroring, RAID, Dual Controllers)

pSeries and AIX provide a number of options for increasing the robustness of storage subsystems, all of which involve some level of redundancy of disks and/or adapters.

AIX disk mirroring provides the ability to define transparent double or triple redundancy of disk data by mapping disk write data to two or three physical disks. On disk reads, the request is issued to all disks in the mirror group, and the first error-free response is returned, which also has some performance benefits. If one of the disks fails, the data is still readable from the other disk(s).

[9] Direct memory access (DMA)
[10] Inter-IC (I^2C)

There are also customer options for SCSI and SSA RAID controller adapters, that can provide the same protection with better performance and less redundancy overhead. Also available are storage subsystems that provide under-the-covers redundancy for high availability.

To provide protection against adapter failures, AIX also supports dual-controller options where the same disk subsystem can be accessed through both a primary adapter path and through a backup adapter path if the primary fails.

Hot Swap Disk and Service Aid

The hardware within the system is designed with the capability to remove and install disks without powering down the system.

An AIX Diagnostics Service Aids provides positive identification (a blinking LED) at the disk device as a visual aid for removal.

Service Processor

The Model 6F1 has an integrated service processor. When the system is powered down, but still plugged into an active power source, the service processor and SPCN functions are still active under standby power. This function provides enhanced RAS by not requiring AIX to be operational for interfacing with a system administrator or service director for RS/6000 and pSeries 6xx. This means that all service processor menu functions (using the local, remote, or terminal concentrator console), as well as dial out capability, are available even if the system is powered down or unable to power up. The next sections talk about selected features of the service processor.

Automatic Reboot

The system will automatically reboot (if the appropriate policy flags are set) in the following conditions:

- Power is restored after a power loss during normal system operation.
- Hardware checkstop failures.
- Machine check interrupt.
- Operating system hang (Surveillance failure).
- Operating system failure.

Surveillance

The service processor, if enabled through service processor setup parameters, performs a surveillance of AIX through a heartbeat mechanism. If there is no heartbeat within the time-out period, the service processor does the following:

- Creates a system reset to allow an AIX dump to occur.
- Upon receiving a reboot request (either after the dump, or immediately if dump is not enabled), the service processor captures scan debug data for the system.
- Reboots the system.

Dial-Out (Call Home), Dial-In

If enabled, the service processor can dial a preprogrammed telephone number to report errors. When enabled, it is also possible to access the service processor remotely through a modem connection. When the service processor is in standby

mode (if, for example, the system is powered off, or an error occurred), the service processor monitors an incoming phone line to answer calls, prompts for a password, verifies the password, and remotely displays the standby menu. The remote session can be mirrored on the local ASCII console if the server is so equipped and the user enables this function.

Processor and Memory Boot Time Deconfiguration

As described previously, processors can be dynamically deconfigured by the system. It is also possible to deconfigure processors and also memory with menus of the service processor for benchmarking reasons. For further information, refer to the *IBM @server pSeries 620 Model 6F1 Service Guide*, SA38-5068.

Note

If the memory is to be temporary deconfigured (for benchmarking or sizing, for example), it is also possible to use the AIX `rmss` command to simulate a specific amount of memory (only below the real memory limit).

Fast Boot

This feature, set as the default, allows you to select the IPL type, mode, and speed for your boot capabilities using service processor menus. Selecting fast boot results in several diagnostic tests being skipped and a shorter memory test being run; therefore, the startup process is faster, but possible problems might not be discovered at startup.

Service Processor Restart

The service processor design for the Model 6F1 includes the ability to reset the service processor. This enables the system firmware to force a hard reset of the service processor if it detects a loss of communication. Because this would typically occur while the system is already up and running, the service processor reset will be accomplished without impacting system operation.

Boot to SMS Menu

The Boot Mode menu allows you to select, among other things, to boot to SMS menu. This function provides booting into SMS menu without pressing a key. This function is useful because it is not necessary to wait in front of the system and press the **F1** (graphic display) or **1** (ASCII terminal) at the right moment.

System Upgrades

Upgrades from an existing Model F50 to a Model 6F1 are not currently offered, however it is possible to order new features to make a Model F80 function similar to a Model 6F1, while maintaining the original model type and serial number.

You can replace the existing system processor book with a processor book containing faster processors or a greater number of processors. Table 2 provides the different feature conversions.

Table 2. Conversion matrix

Existing configuration	Required configuration
RS64 III, 1-way, 450 MHz	RS64 III, 2-way, 450 MHz

Existing configuration	Required configuration
RS64 III, 1-way, 450 MHz	RS64 III, 4-way, 450 MHz
RS64 III, 1-way, 450 MHz	RS64 IV, 2-way, 600 MHz
RS64 III, 1-way, 450 MHz	RS64 IV, 4-way, 600 MHz
RS64 III, 1-way, 450 MHz	RS64 IV, 6-way, 668 MHz
RS64 III, 1-way, 450 MHz	RS64 IV, 2-way, 750 MHz
RS64 III, 1-way, 450 MHz	RS64 IV, 4-way, 750 MHz
RS64 III, 1-way, 450 MHz	RS64 IV, 6-way, 750 MHz
RS64 III, 2-way, 450 MHz	RS64 III, 4-way, 450 MHz
RS64 III, 2-way, 450 MHz	RS64 IV, 2-way, 600 MHz
RS64 III, 2-way, 450 MHz	RS64 IV, 4-way, 600 MHz
RS64 III, 2-way, 450 MHz	RS64 IV, 6-way, 668 MHz
RS64 III, 2-way, 450 MHz	RS64 IV, 2-way, 750 MHz
RS64 III, 2-way, 450 MHz	RS64 IV, 4-way, 750 MHz
RS64 III, 2-way, 450 MHz	RS64 IV, 6-way, 750 MHz
RS64 III, 4-way, 450 MHz	RS64 IV, 4-way, 600 MHz
RS64 III, 4-way, 450 MHz	RS64 IV, 6-way, 668 MHz
RS64 III, 4-way, 450 MHz	RS64 IV, 4-way, 750 MHz
RS64 III, 4-way, 450 MHz	RS64 IV, 6-way, 750 MHz
RS64 III, 6-way, 500 MHz	RS64 IV, 6-way, 668 MHz
RS64 III, 6-way, 500 MHz	RS64 IV, 4-way, 750 MHz
RS64 III, 6-way, 500 MHz	RS64 IV, 6-way, 750 MHz
RS64 IV, 1-way, 600 MHz	RS64 IV, 2-way, 600 MHz
RS64 IV, 1-way, 600 MHz	RS64 IV, 4-way, 600 MHz
RS64 IV, 1-way, 600 MHz	RS64 IV, 6-way, 688 MHz
RS64 IV, 1-way, 600 MHz	RS64 IV, 2-way, 750 MHz
RS64 IV, 1-way, 600 MHz	RS64 IV, 4-way, 750 MHz
RS64 IV, 1-way, 600 MHz	RS64 IV, 6-way, 750 MHz
RS64 IV, 2-way, 600 MHz	RS64 IV, 4-way, 600 MHz
RS64 IV, 2-way, 600 MHz	RS64 IV, 6-way, 688 MHz
RS64 IV, 2-way, 600 MHz	RS64 IV, 2-way, 750 MHz
RS64 IV, 2-way, 600 MHz	RS64 IV, 4-way, 750 MHz
RS64 IV, 2-way, 600 MHz	RS64 IV, 6-way, 750 MHz
RS64 IV, 4-way, 600 MHz	RS64 IV, 6-way, 688 MHz
RS64 IV, 4-way, 600 MHz	RS64 IV, 4-way, 750 MHz

Existing configuration	Required configuration
RS64 IV, 4-way, 600 MHz	RS64 IV, 6-way, 750 MHz
RS64 IV, 6-way, 688 MHz	RS64 IV, 6-way, 750 MHz
RS64 IV, 1-way, 750 MHz	RS64 IV, 2-way, 750 MHz
RS64 IV, 1-way, 750 MHz	RS64 IV, 4-way, 750 MHz
RS64 IV, 1-way, 750 MHz	RS64 IV, 6-way, 750 MHz
RS64 IV, 2-way, 750 MHz	RS64 IV, 4-way, 750 MHz
RS64 IV, 2-way, 750 MHz	RS64 IV, 6-way, 750 MHz
RS64 IV, 4-way, 750 MHz	RS64 IV, 6-way, 750 MHz

The existing Model F80 processor being replaced should be returned to IBM.

Memory DIMMs from the F80 can remain. Migrating to a 2-, 4-, or 6 - way processor the DIMMs will be installed on the memory cards in quads. Therefore it might be necessary to order two additional DIMMs to complete the quad.

Most of the adapters can remain in the Model F80. Concerning the graphics accelerators, only a GXT130P is supported in Model 6F1. For further information about adapters, especially if the adapter is supported in Model 6F1, refer to the *PCI Adapter Placement Reference Guide*, SA38-0538.

Most disk drives can move into a new Model 6F1 or remain if only newer processors are ordered. Migration of 68-pin drives will limit the performance of the bus to which they are attached to SE 40 MB/s, rather than the LVD 80 MB/s, which is possible for an entire complement of 80-pin Ultra2 drives.

When upgrading from an Model F80 that does not run AIX 4.3.3 ML10, it is required to upgrade to AIX 4.3.3 ML10 or higher before you can upgrade the F80 system.

External Storage Expandability

Storage expansion for the Model 6F1 can be provided through several IBM storage options. The storage subsystems can be connected externally as stand-alone towers or be placed within a rack.

External disk storage capacity can also be provided by attaching the Model 6F1 to storage servers. Using differential Ultra SCSI, the Model 6F1can be attached to the IBM Enterprise Storage Server. And by using the Fibre Channel Adapter, the Model 6F1 can be attached to the IBM Fibre Channel RAID Storage server or the IBM Enterprise Storage Server.

SP Attachment

The Model 6F1 cannot be attached as a logical node, nor is it supported to be used as a Control Workstation (CWS) in an SP system.

Reference

The following sections list additional materials available for further research.

System Documentation

For more detailed information, refer to the following documents:

- *IBM @server pSeries 620 Model 6F1 Installation Guide*, SA38-0569
- *IBM @server pSeries 620 Model 6F1 User's Guide*, SA38-0567
- *IBM @server pSeries 620 Model 6F1 Service Guide*, SA38-0568
- *PCI Adapter Placement Reference Guide*, SA38-0538

Select IBM Redbooks

The following IBM Redbooks are related to the material discussed in this paper:

- *IBM @server pSeries 680 Handbook Including RS/6000 Model S80,* SG24-6023
- *IBM Enterprise Storage Server*, SG24-5465
- *Monitoring and Managing IBM SSA Disk Subsystems*, SG24-5251
- *AIX 5L Differences Guide Version 5.1 Edition,* SG24-5765
- *NIM: From A to Z in AIX 4.3*, SG24-5524
- *AIX Logical Volume Manager, from A to Z: Introduction and Concepts*, SG24-5433
- *Understanding IBM @server pSeries Performance and Sizing*, SG24-4810

Select Internet Links

For more detailed information, see the following Web sites:

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www.ibm.com/servers/aix/
www.chips.ibm.com/
www.research.ibm.com/topics/serious/chip/
www.storage.ibm.com/
www.hursley.ibm.com/~ssa/rs6k/
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