IBM System z10 Enterprise Class

Parwez Hamid
Senior Certified IT Specialist
parwez_hamid@uk.ibm.com

The Future Runs on System z

IBM Systems

Introducing
The IBM System z10 Enterprise Class

The worlds' most powerful enterprise computing platform

Introducing the IBM System z10™ Enterprise Class… a marriage of evolution and revolution

Evolution

– Scalability and virtualization to reduce cost and complexity

– Improved efficiency to further reduce energy consumption

– Improved security and resiliency to reduce risk

– New heights in storage scalability and data protection

Revolution

– 4.4 GHz chip to deliver improved performance for CPU intensive workloads

– 'Just in time' deployment of capacity resources

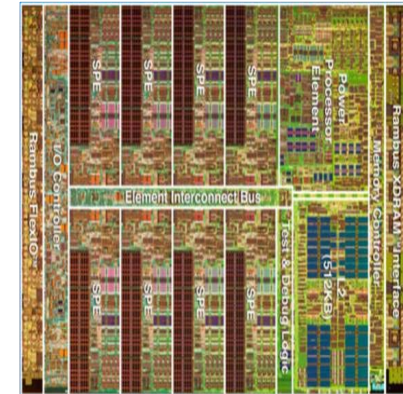– Vision to expand System z capabilities with Cell Broadband Engine™ technology

Collaborate to Innovate

- **OpenSolaris™ for System z under z/VM**

SINE NOMINE
ASSOCIATES

opensolaris

- **SAP Business Intelligence Accelerator**

- **"GameFrame" with Cell Broadband Engine**

Cell Broadband Engine

IBM z10 EC Continues the CMOS Mainframe Heritage

Chart: MHz (y-axis, 0 to 4000) vs. year/model (x-axis)

- 1997 G4 — 300 MHz
- 1998 G5 — 420 MHz
- 1999 G6 — 550 MHz
- 2000 z900 — 770 MHz
- 2003 z990 — 1.2 GHz
- 2005 z9 EC — 1.7 GHz
- 2008 z10 EC — 4.4 GHz
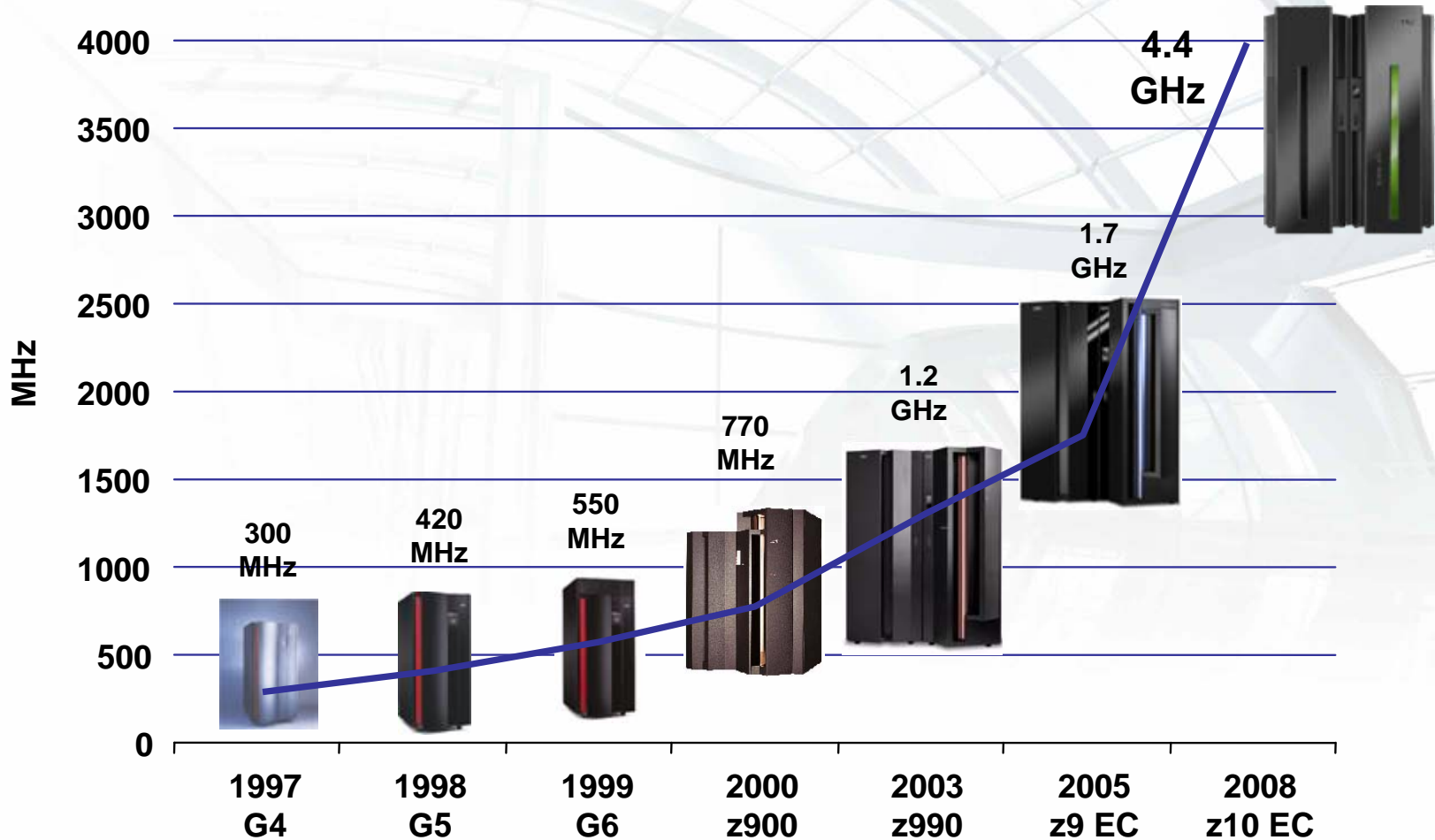
- G4 - 1st full-custom CMOS S/390
- G5 - IEEE-standard BFP; branch target prediction
- G6 – Copper Technology (Cu BEOL)
- z900 - Full 64-bit z/Architecture
- z990 - Superscalar CISC pipeline
- z9 EC - System level scaling
- z10 EC – Architectural extensions

Making high performance a reality

- **New Enterprise Quad Core z10 processor chip**
  - 4.4 GHz - additional throughput means improved price/performance
  - Cache rich environment optimized for data serving
  - 50+ instructions added to improve compiled code efficiency
  - Support for 1MB page frames

- **Hardware accelerators on the chip**
  - Hardware data compression
  - Cryptographic functions
  - Hardware Decimal Floating point

- **CPU intensive workloads get performance improvements from new core pipeline design**
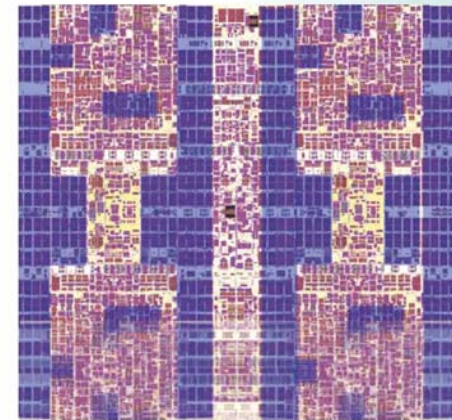
**Enterprise Quad Core z10 processor chip**

Microprocessors: z10 EC and Power6™

- **These are siblings – but not identical twins**

- **They share lots of DNA**
  - IBM 65nm SOI technology
  - Design building blocks: latches, SRAMs, regfiles, dataflow elements
  - Large portions of Fixed, Binary and Decimal floating point arithmetical instructions
  - Core pipeline design style - High-frequency, low-latency, mostly-in-order
  - Many designers worked on both chips

- **They have different personalities**
  - In support of different z and p markets
  - Very different cores
  - Different cache hierarchy and coherency model
  - Different SMP topology and protocol
  - Different chip organization
  - IBM System z is optimized for Enterprise Data Serving Hub
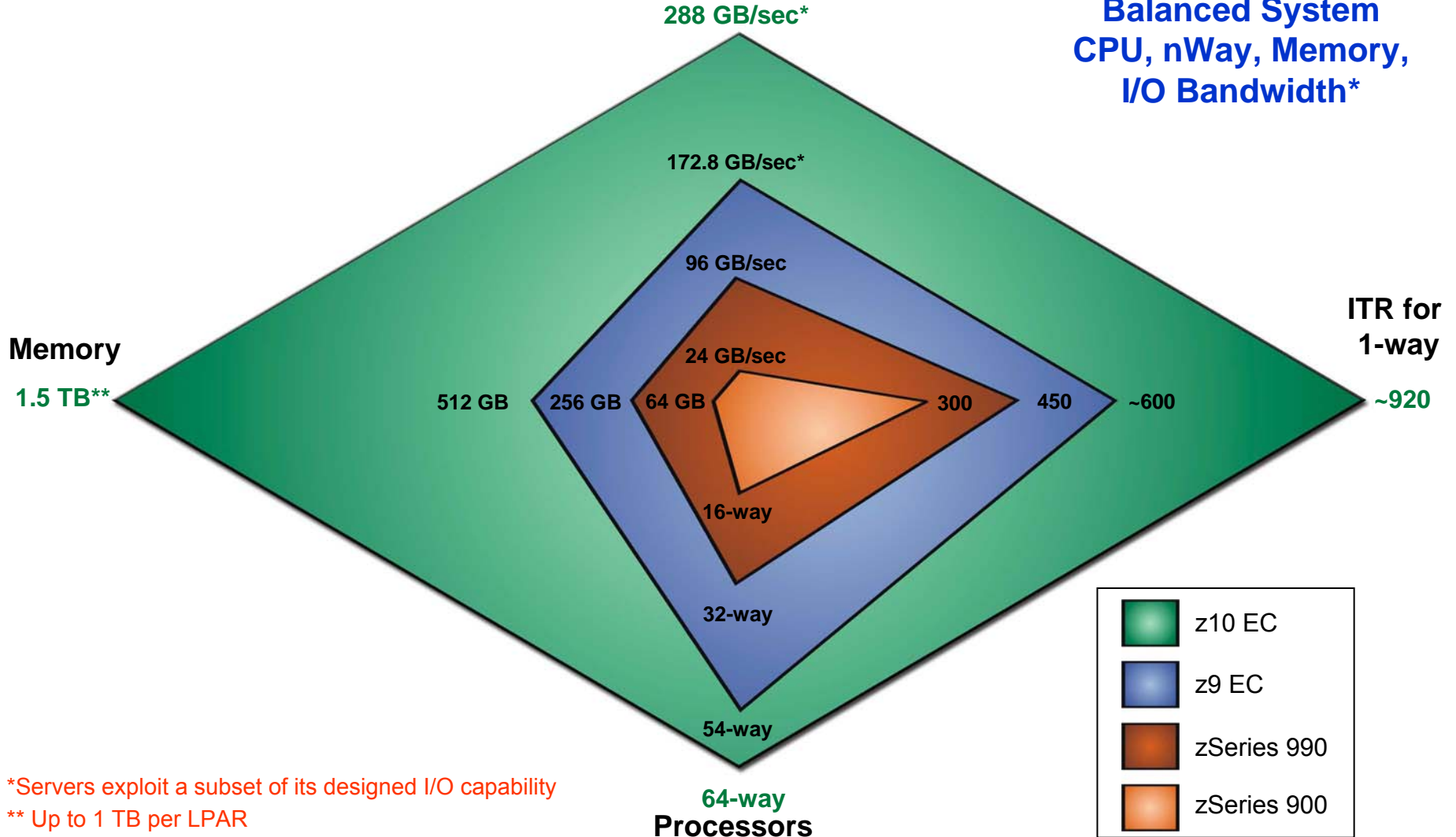
Enterprise Quad Core z10 processor chip
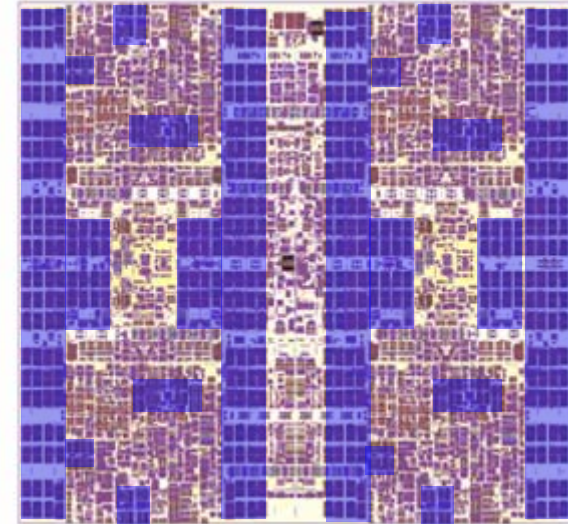
Dual Core POWER6 processor chip
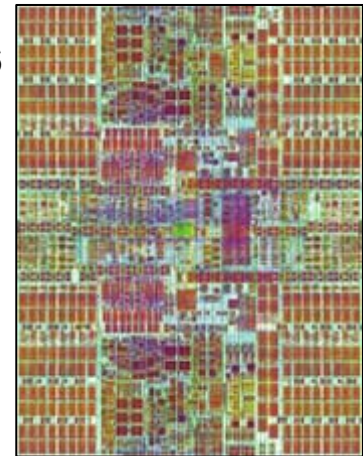
IBM System z: System Design Comparison

System I/O Bandwidth

288 GB/sec*

Balanced System CPU, nWay, Memory, I/O Bandwidth*

172.8 GB/sec*

96 GB/sec

24 GB/sec

Memory

1.5 TB**

ITR for 1-way

512 GB   256 GB   64 GB   300   450   ~600   ~920

16-way

32-way

54-way

64-way Processors

*Servers exploit a subset of its designed I/O capability
** Up to 1 TB per LPAR

	z10 EC
	z9 EC
	zSeries 990
	zSeries 900

8

Improved server performance and scalability with faster and more processors and improved dispatching synergy

- The z10 EC delivers on average 50% more performance in a n-way configuration than a z9 ™ EC n-way
  - The uniprocessor is expected to deliver 62% more performance than z9 EC uniprocessor *
- The z10 EC 64-way offers 70% more server capacity than the largest z9 EC**
- Introducing HiperDispatch for improved synergy with z/OS® operating system to deliver scalability and performance
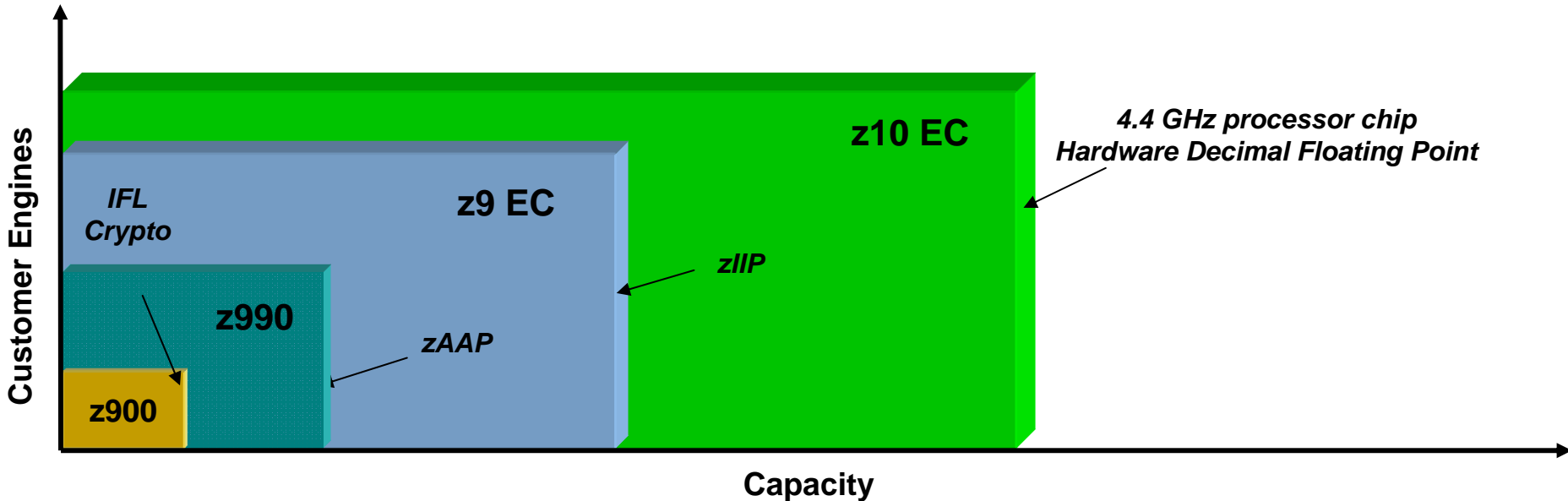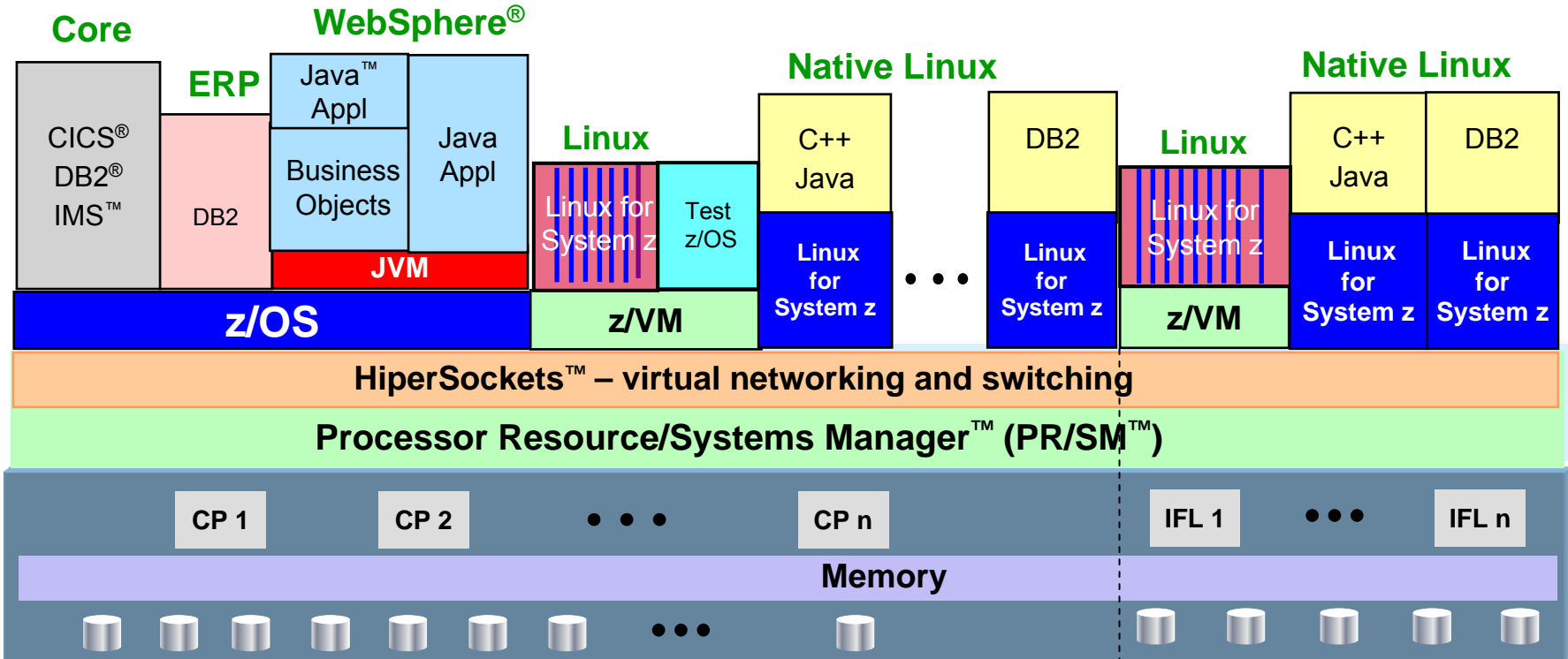

Significant capacity for traditional growth and consolidation

* LSPR mixed workload average running z/OS 1.8 - z10 EC 701 versus z9 EC 701
** This is a comparison of the z10 EC 64-way and the z9 EC S54 and is based on LSPR mixed workload average running z/OS 1.8

System z – The Ultimate Virtualization Resource

Core

ERP

WebSphere®

Linux

Native Linux

Native Linux

CICS® DB2® IMS™	DB2	Java™ Appl / Business Objects	Java Appl	Linux for System z	Test z/OS	C++ Java		DB2	Linux for System z	C++ Java	DB2

JVM

z/OS	z/VM	Linux for System z	• • •	Linux for System z	z/VM	Linux for System z	Linux for System z

HiperSockets™ – virtual networking and switching

Processor Resource/Systems Manager™ (PR/SM™)

CP 1	CP 2	• • •	CP n	IFL 1	• • •	IFL n

Memory

- **Massive, robust consolidation platform; virtualization is built in, not added on**
- **Up to 60 logical partitions on PR/SM; 100's to 1000's of virtual servers on z/VM**
- **Virtual networking for memory-speed communication, as well as virtual layer 2 and layer 3 networks supported by z/VM**
- **Most sophisticated and complete hypervisor function available**
- **Intelligent and autonomic management of diverse workloads and system resources based on business policies and workload performance objectives**

IBM System z family

IBM System z9 EC (2094)

- Announced 7/05 - Superscalar Server with up to 64 PU cores
- 5 models – Up to 54-way
- Granular Offerings for up to 8 CPs
- PU (Engine) Characterization
  - **CP, SAP, IFL, ICF, zAAP, zIIP**
- On Demand Capabilities
  - **CUoD, CIU, CBU, On/Off CoD**
- Memory – up to 512 GB
- Channels
  - **Four LCSSs**
  - **Multiple Subchannel Sets**
  - **MIDAW facility**
  - **63.75 subchannels**
  - **Up to 1024 ESCON® channels**
  - **Up to 336 FICON® channels**
  - **FICON Express2 and 4**
  - **10 GbE, GbE, 1000BASE-T**
  - **Coupling Links**
- Configurable Crypto Express2
- Parallel Sysplex clustering
- HiperSockets – up to 16
- Up to 60 logical partitions
- Enhanced Availability
- Operating Systems
  - **z/OS, z/VM, z/VSE™, TPF, z/TPF, Linux on System z**

IBM System z9 BC (2096)

- Announced 4/06 - Superscalar Server with 8 PU cores
- 2 models – Up to 4-way
- High levels of Granularity available
  - **73 Capacity Indicators**
- PU (Engine) Characterization
  - **CP, SAP, IFL, ICF, zAAP, zIIP**
- On Demand Capabilities
  - **CUoD, CIU, CBU, On/Off CoD**
- Memory – up to 64 GB
- Channels
  - **Two LCSSs**
  - **Multiple Subchannel Sets**
  - **MIDAW facility**
  - **63.75 subchannels**
  - **Up to 420 ESCON channels**
  - **Up to 112 FICON channels**
  - **FICON Express2 4 Gbps**
  - **10 GbE, GbE, 1000BASE-T**
  - **Coupling Links**
- Configurable Crypto Express2
- Parallel Sysplex clustering
- HiperSockets – up to 16
- Up to 30 logical partitions
- Enhanced Availability
- Operating Systems
  - **z/OS, z/OS.e, z/VM, z/VSE, TPF, z/TPF, Linux on System z**

IBM System z10 EC (2097)

- Announce 2/08 - Server with up to 77 PU cores
- 5 models – Up to 64-way
- Granular Offerings for up to 12 CPs
- PU (Engine) Characterization
  - **CP, SAP, IFL, ICF, zAAP, zIIP**
- On Demand Capabilities
  - **CUoD, CIU, CBU, On/Off CoD, CPE**
- Memory – up to 1.5 TB for Server and up to 1 TB per LPAR
- Channels
  - **Four LCSSs**
  - **Multiple Subchannel Sets**
  - **MIDAW facility**
  - **63.75 subchannels**
  - **Up to 1024 ESCON channels**
  - **Up to 336 FICON channels**
  - **FICON Express2 and 4**
  - **10 GbE, GbE, 1000BASE-T**
  - **InfiniBand Coupling Links***
- Configurable Crypto Express2
- Parallel Sysplex clustering
- HiperSockets – up to 16
- Up to 60 logical partitions
- Enhanced Availability
- Operating Systems
  - **z/OS, z/VM, z/VSE, TPF, z/TPF, Linux on System z**

* All statements regarding IBM's future direction and intent are subject to change or withdrawal without notice, and represent goals and objectives only.

Continuing the modular design for flexibility
Facilitates upgradeability and availability

IBM System z10 Enterprise Class (z10 EC)

Machine Type: 2097

5 Models: **E64**

E56

E40

E26

E12

Processor Units (PUs):

- **New Enterprise Quad Core technology**
  - 4.4 GHz
- **One to four book modular design**
- **Sub-capacity available up to 12 CPs**
- **Enhanced capacity 64-way model**
- **17 PUs per book**
  - 17 and 20 for Model E64

Memory:

- **Up to 1.5 TB memory**
  - 384 GB per book
- **16 GB HSA separately managed**
  - not included in customer purchased memory
- **Star L2 cache book interconnect**

I/O:

- **6 GBps InfiniBand host buses for I/O**
- **New OSA-Express3 10 GbE**
- **InfiniBand Coupling Links**

Increasing capacity, reducing outages and enhancing capabilities

- **Five hardware models**
- **Faster Uni Processor [1]**
- **Up to 64 customer PUs**
- **36 CP Subcapacity Settings**
- **Star Book Interconnect**
- **Up to 1.5 TB memory**
- **Fixed 16 GB HSA as standard**
- **Large Page Support (1 MB)**
- **HiperDispatch**
- **Enhanced CPACF SHA 512, AES 192 and 256-bit keys**
- **Hardware Decimal Floating Point**
- **Just in Time Deployment for capacity offerings – permanent and temporary**

- **6.0 GBps InfiniBand HCA to I/O interconnect**
- **SCSI IPL included in Base LIC**
- **OSA-Express3 10 GbE [2]**
- **HiperSockets Multi Write Facility enhancements**
- **HiperSockets Layer 2 Support**
- **InfiniBand Coupling Links [2]**
- **STP using InfiniBand [2]**
- **Capacity Provisioning Support**
- **Scheduled Outage Reduction**
- **Improved RAS**
- **FICON LX Fiber Quick Connect**
- **Power Monitoring support**

[1] Compared to z9 EC
[2] Planned availability 2Q08

SOD: PSIFB for z9 EC & z9 BC for non-dedicated CF Models*

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z10 EC Multi-Chip Module (MCM)

- **96mm x 96mm MCM**
  - 103 Glass Ceramic layers
  - 7 chip sites

- **CMOS 11s chip Technology (65 nm)**

  5 Enterprise Quad Core Processor (PU) chips
  - 21.97 mm x 21.17 mm
  - 1.0 billion transistors/chip
  - L1 cache/PU core
    - 64 KB I-cache + 128 KB D-cache
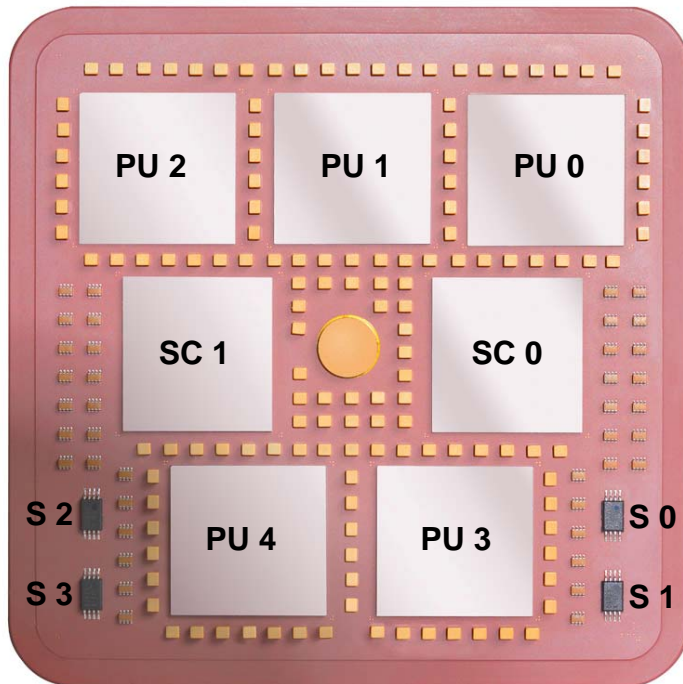 - L1.5 cache/PU core
    - 3 MB
  - 4.4 GHz / 0.23 ns Cycle Time

  2 Storage Control (SC) chips
  - 21.11 mm x 21.71 mm
  - 1.6 billion transistors/chip
  - L2 cache 24 MB/SC chip (48 MB/MCM)
  - L2 access to/from other MCM/Books

  4 SEEPROM (S) chips
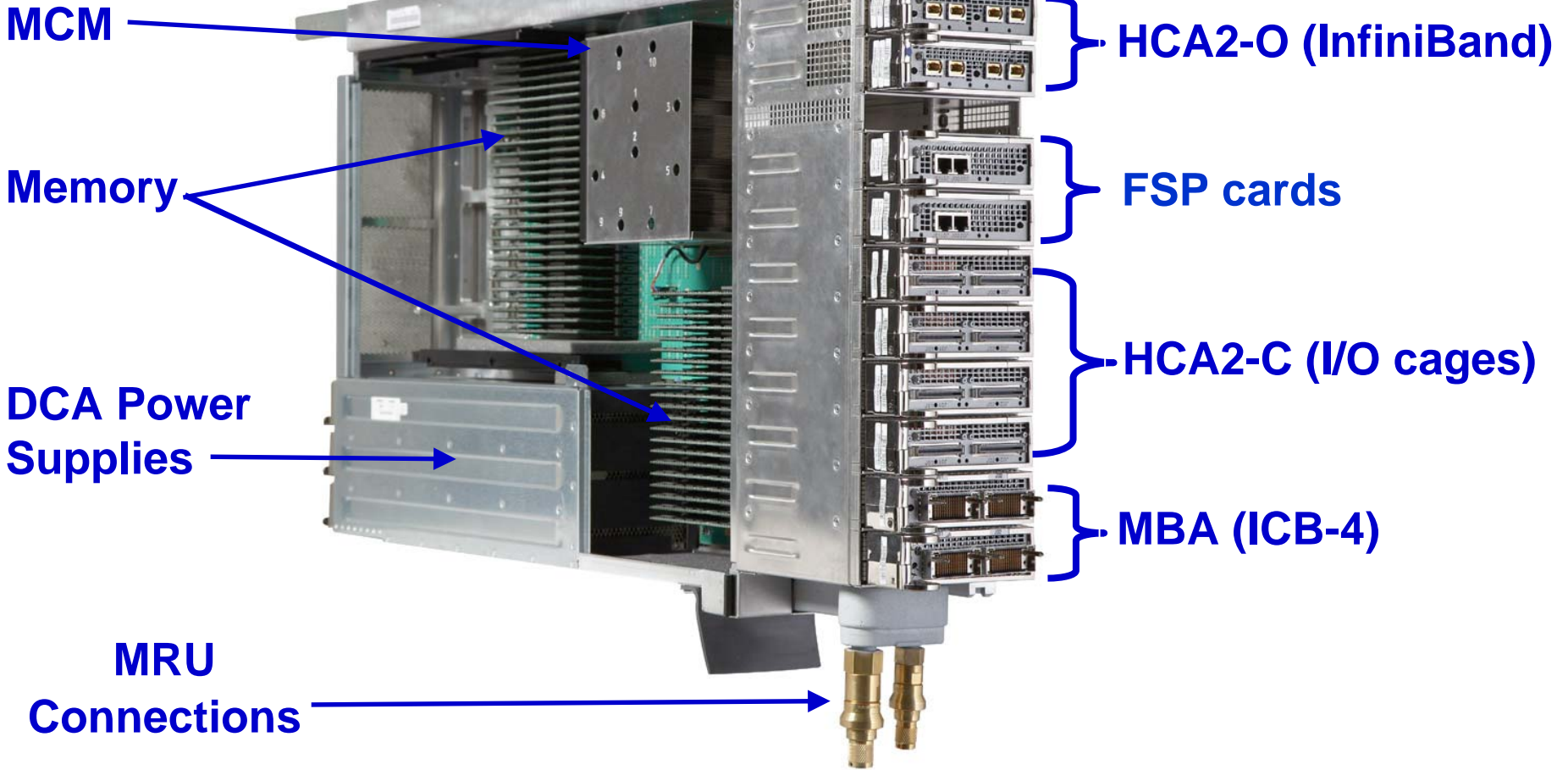 - Product data for MCM, chips and other engineering information

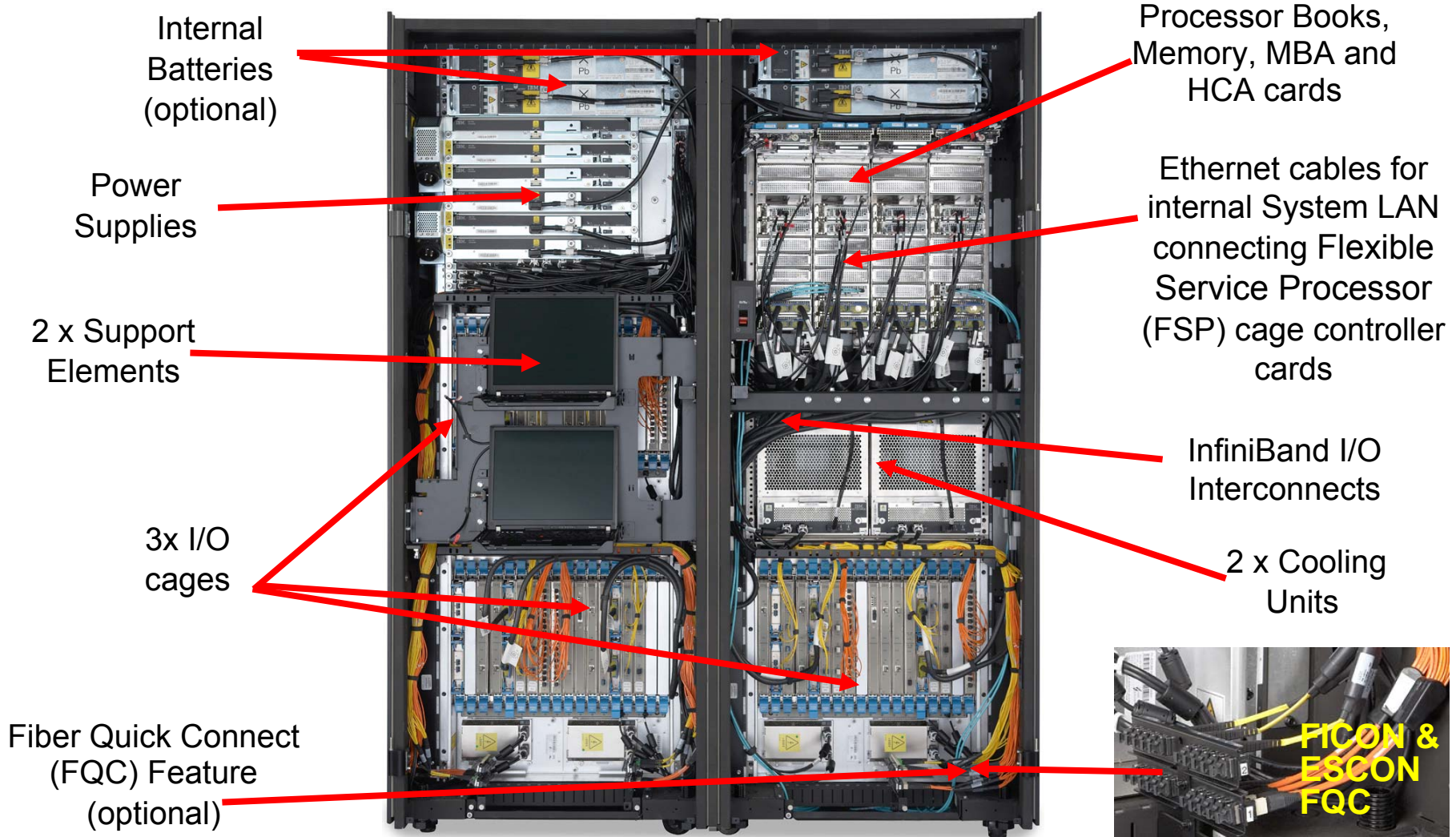 **Clock Functions distributed across PU and SC chips**

z10 EC Book Layout – Under the covers

Fanouts

MCM

Memory

DCA Power Supplies

MRU Connections

HCA2-O (InfiniBand)

FSP cards

HCA2-C (I/O cages)

MBA (ICB-4)

z10 EC – Under the covers (Model E56 or E64)

Internal Batteries (optional)

Power Supplies

2 x Support Elements

3x I/O cages

Fiber Quick Connect (FQC) Feature (optional)

Processor Books, Memory, MBA and HCA cards

Ethernet cables for internal System LAN connecting Flexible Service Processor (FSP) cage controller cards

InfiniBand I/O Interconnects

2 x Cooling Units

FICON & ESCON FQC

z10 EC Base and Sub-Capacity Offerings

**CP Capacity
Relative to Full Speed
7xx = 100%
6xx ≈ 69.35%
5xx ≈ 51.20%
4xx ≈ 23.69%
xx = 01 Through 12**

7xx

6xx

5xx

4xx
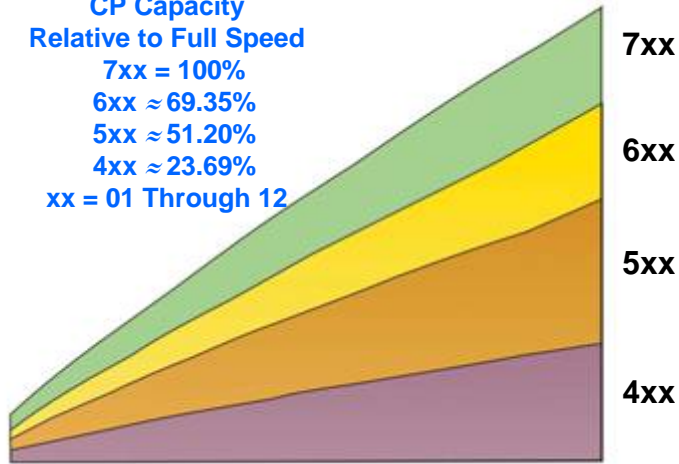
- The z10 EC has 36 additional capacity settings at the low end
- **Available on ANY H/W Model for 1 to 12 CPs. Models with 13 CPs have to be full capacity**
- All CPs must be the same capacity within the z10 EC
- All specialty engines run at full capacity. The one for one entitlement to purchase one zAAP or one zIIP for each CP purchased is the same for CPs of any capacity.
- Only 12 CPs can have granular capacity, other PU cores must be CBU or characterized as specialty engines

Sub Capacity Models

E12   E26   E40   E56   E64
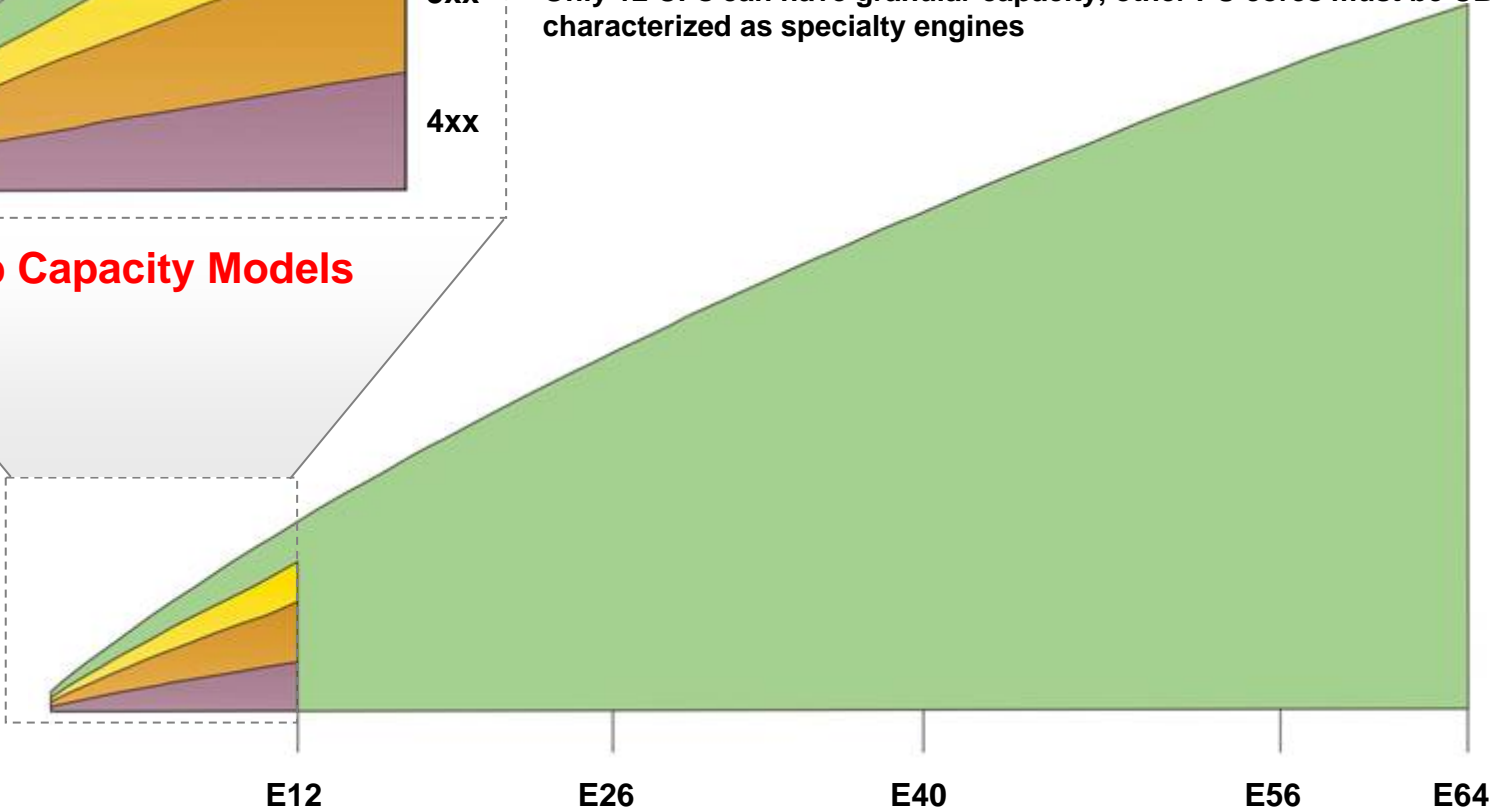
Focused performance boost
Hardware Decimal Floating Point

- **Decimal arithmetic widely used in commercial and financial applications**

- **Computations often handled in software**

- **First delivered with the System z9 - brought improved precision and function**
  - Avoids rounding and other problems with binary/decimal conversions

- **On z10 EC integrated on every core giving a performance boost to execution of decimal arithmetic**

- **Growing industry support for DFP standardization**
  - Java BigDecimal, C#, XML, C/C++, GCC, DB2® V9, Enterprise PL/1, Assembler
  - Endorsed by key software vendors including Microsoft® and SAP
  - Open standard definition led by IBM

Bringing high performance computing benefits to commercial workloads

Compiler Optimization & Performance

Maximize Exploitation of z10 Hardware Architecture[1]

- ✓ Exploit latest hardware without need of expert knowledge of architecture
  - • Enables exploitation of z10 hardware without source code changes
- ✓ Exploit new z10 instructions from the General-Instructions-Extension facility
- ✓ Exploit IEEE Decimal Floating-Point (DFP)
- ✓ Exploit Additional Floating-Point Registers (AFP)
- ✓ Exploit 64-bit instruction set and registers even in 32-bit code
- ✓ Support IEEE Binary Floating-Point which eases platform portability
- ✓ Maximize application performance using new & innovative optimization technologies
  - • Reduces total cost of ownership
  - • Up to 10-25% Performance Improvements[2]

[1] Individual features in the content list may not be applicable to all IBM compiler languages.

Check specific language documentation for details.

[2] Performance improvement results based on select benchmarks. Results will vary depending on application.
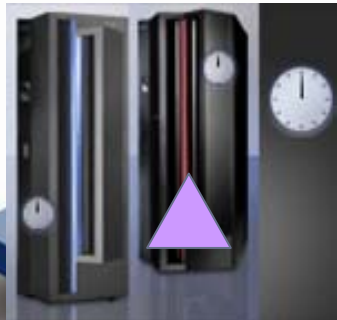
z10 EC HiperDispatch

- **HiperDispatch – z10 EC unique function**
  - Dispatcher Affinity (DA) - New z/OS Dispatcher
  - Vertical CPU Management (VCM) - New PR/SM Support

- **Mitigate impact of scaling differences between processor and memory**
  - Access to memory and remote caches not scaling with processor speed
  - Increased performance sensitivity to cache misses in multi-processor system

- **Optimize performance by redispatching units of work to same processor group**
  - Keep processes running near their cached instructions and data
  - Minimize transfers of data ownership among processors / books

- **Tight collaboration across entire z10 EC hardware/firmware/OS stack**
  - Concentrate logical processors around shared L2 caches
  - Communicate effective cache topology for partition to OS
  - **Dynamically optimize allocation of logical processors and units of work**

Evolution of System z Specialty Engines

Building on a strong track record of technology innovation with specialty engines – DB Compression, SORT, Encryption, Vector Facility

IBM System z9 Integrated Information Processor (zIIP) 2006

Eligible for zIIP:

- **DB2 remote access and BI/DW**
- **ISVs**
- **New! IPSec encryption**
- **z/OS XML**
- **z/OS Global Mirror***

System z Application Assist Processor (zAAP) 2004

Eligible for zAAP:

- **Java execution environment**
- **z/OS XML**

Integrated Facility for Linux (IFL) 2000

Internal Coupling Facility (ICF) 1997

*SOD: IBM plans to enhance z/VM in a future release to support the new System z10 EC capability to allow any combination of CP, zIIP, zAAP, IFL, and ICF processor-types to reside in the same z/VM LPAR
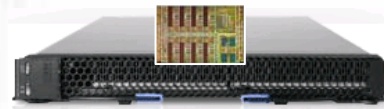
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System z and Cell Broadband Engine – The Vision
A 'Marriage' of Two Technologies that Perfectly Complement Each Other

Cell Blade

QS20, QS21, QS22, QS2x

Integrated and / or Networked Cell (NG)

z today

z tomorrow

Preserves the same programming model between Network and Integrated

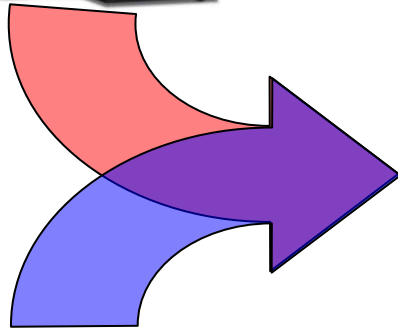| Aerospace and Defense	Financial Services Sector	Chemicals and Petroleum	Digital Video Surveillance	Digital Media	Information Based Medicine	Electronic Design Automation

z10 EC System Upgrades

z9 EC

z990

E64

E56

E40

E26

E12

Concurrent Upgrade

- **z10 EC to higher hardware z10 EC model**
  - **Upgrade of z10 EC Models E12, E26, E40 and E56 to E64 is disruptive**
  - **When upgrading to z10 EC E64, unlike the z9 EC, the first Book is retained**
- **Any z9 EC to any z10 EC**
- **Any z990 to any z10 EC**

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Helping to get you connected to your world

- **Improved performance and flexibility for connectivity**
- **Broad set of options to meet your needs**
- **Excellent investment protection when you upgrade to the z10 EC**

Within the server

- HiperSockets™
  - **Multi Write Facility** *new!*
  - **Layer2 support** *new!*
- Integrated console controller
- Integrated communications controller support

To the Data

- FICON/FCP
  - FICON® Express4
  - FICON Express2
  - FICON Express (Required for FCV)
- ESCON®

* Note: Red items carry forward on a Machine MES only, not available for new system orders

To the Network

- OSA-Express3 [1]
  - **10 Gigabit Ethernet** *new!*
- OSA-Express2
  - 1000BASE-T Ethernet
  - Gigabit Ethernet LX and SX
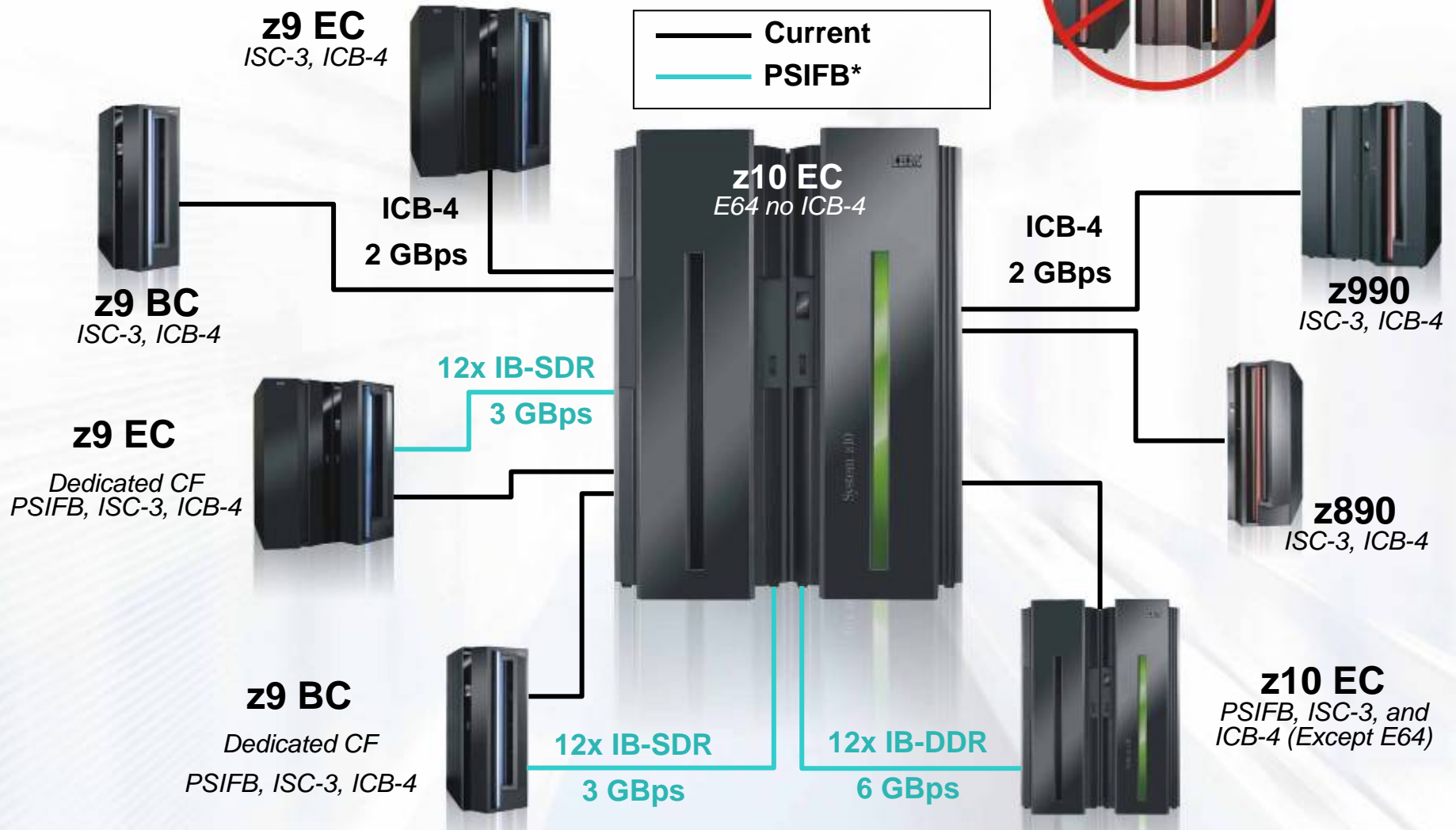 - 10 Gigabit Ethernet LR

For Clustering

new!

- **InfiniBand Coupling Links [1]**
- **ICB-4**
- **ISC-3 (peer mode only)**
- **IC (define only)**
- **STP - NTP Client Support**
- **Support for n-2 and above servers**

[1] Planned availability 2Q08

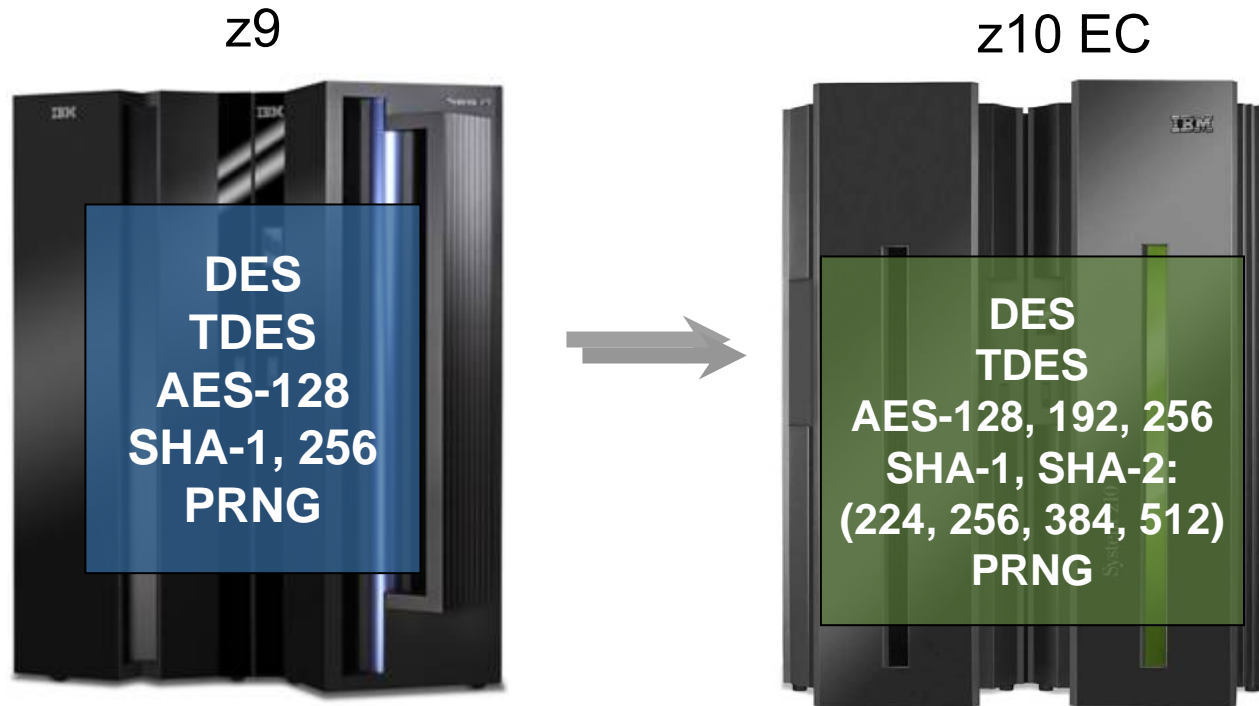# z10 EC Parallel Sysplex coexistence and coupling connectivity

z800, z900
Not supported!

Legend	
——	**Current**
——	**PSIFB***

z9 EC
ISC-3, ICB-4

z9 BC
ISC-3, ICB-4

z9 EC
Dedicated CF
PSIFB, ISC-3, ICB-4

z9 BC
Dedicated CF
PSIFB, ISC-3, ICB-4

z10 EC
E64 no ICB-4

ICB-4
2 GBps

ICB-4
2 GBps

z990
ISC-3, ICB-4

z890
ISC-3, ICB-4

z10 EC
PSIFB, ISC-3, and
ICB-4 (Except E64)

12x IB-SDR
3 GBps

12x IB-SDR
3 GBps

12x IB-DDR
6 GBps

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z10 EC CP Assist for Cryptographic Functions (CPACF)

Integrated Cryptographic Service Facility (ICSF)

Crypto Express2

PU PU PU PU PU

CP Assist for Cryptographic Function

z9

DES
TDES
AES-128
SHA-1, 256
PRNG

z10 EC

DES
TDES
AES-128, 192, 256
SHA-1, SHA-2:
(224, 256, 384, 512)
PRNG

High performance clear key symmetric encryption/decryption

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z10 EC – Hardware RAS Improvements for Outage Avoidance

Sources of Outages - Pre z9 -Hrs/Year/Syst-
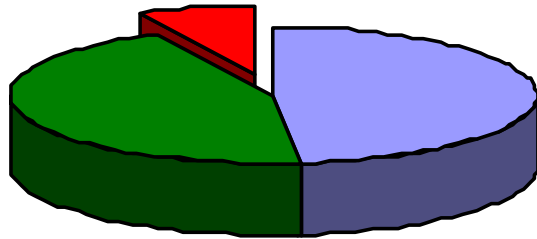
- ■ Scheduled (CIE+Disruptive Patches + ECs)
- ■ Planned - (MES + Driver Upgrades)
- ■ Unscheduled (UIRA)

Impact of Outage

	Prior Servers	z9 EC	z10 EC
Unscheduled Outages	✓	✓	✓
Scheduled Outages	✓	✓	✓
Planned Outages		✓	✓
Preplanning requirements			✓

Increased Focus over time

z10 EC Enhancements designed to avoid Outages

- **Continued Focus on Firmware Quality**
- **Reduced Chip Count on MCM**
- **Memory Subsystem Improvements**

- **DIMM FRU indicators**
- **Single Processor Core Checkstop**
- **Single Processor Core Sparing**
- **Point to Point SMP Fabric (not a ring)**
- **Rebalance PSIFB and I/O Fanouts**
- **Redundant 100Mb Ethernet service network w/ VLAN**

- **Elimination of unnecessary CBU passwords**
- **Enhanced Driver Maintenance (EDM) Upgrades**
  - **Multiple "from" sync point support**
  - **Improved control of channel LIC levels**
- **Reduce Pre-planning to Avoid POR**
  - **16 GB for HSA**
  - **Dynamic I/O Enabled by Default**
  - **Add Logical Channel Subsystem (LCSS)**
  - **Change LCSS Subchannel Sets**
  - **Add/Delete Logical Partitions**
- **Reduce Pre-Planning to Avoid LPAR Deactivate**
  - **Change Partition Logical Processor Config**
  - **Change Partition Crypto Coprocessor Config**
- **CoD – Flexible Activation/Deactivation**

Just in time capacity gives you control

- **Permanent and temporary offerings – with you in charge**
  - Permanent offerings – Capacity Upgrade on Demand (CUoD), Customer Initiated Upgrade (CIU)
  - Temporary offerings include On/Off Capacity on Demand (On/Off CoD) , Capacity Backup Upgrade (CBU) and a new one – Capacity for Planned Event (CPE)

- **No customer interaction with IBM at time of activation**
  - Broader customer ability to order temporary capacity

- **Multiple offerings can be in use simultaneously**
  - All offerings on Resource Link
  - Each offering independently managed and priced

- **Flexible offerings may be used to solve multiple situations**
  - Configurations based on real time circumstances
  - Ability to dynamically move to any other entitled configuration

- **Offerings can be reconfigured or replenished dynamically**
  - Modification possible even if offering is currently active
  - Some permanent upgrades permitted while temporary offerings are active

- **Policy based automation capabilities**
  - Using Capacity Provisioning Manager with z/OS 1.9
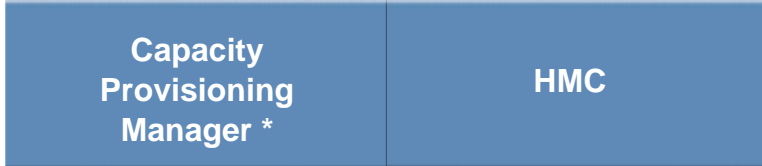 - Using scheduled operations via HMC

On demand simplified
New architectural approach for capacity

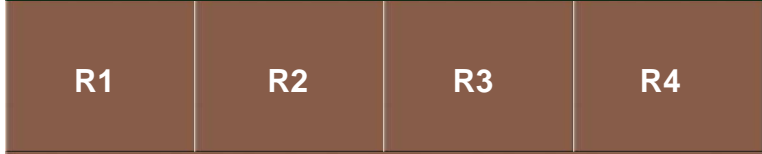**Orders downloaded from System Support electronically or by IBM Service**

SE Hard Drive

| Customer defined policy or manual operations	Capacity Provisioning Manager *	HMC

API
query, activate, deactivate

Authorization Layer

- Enforce terms and conditions
- Enforce physical model limitations

R1	R2	R3	R4

- Up to 4 temporary capacity offerings
- Each record represents an individual offering
- Customer assigns in any combination

Dormant Capacity

CIU - CBU – On/Off CoD – CPE

Permanent Capacity
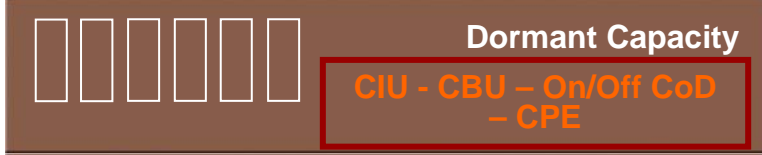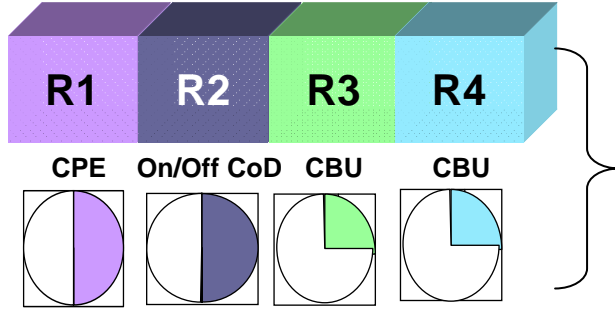
- Base model
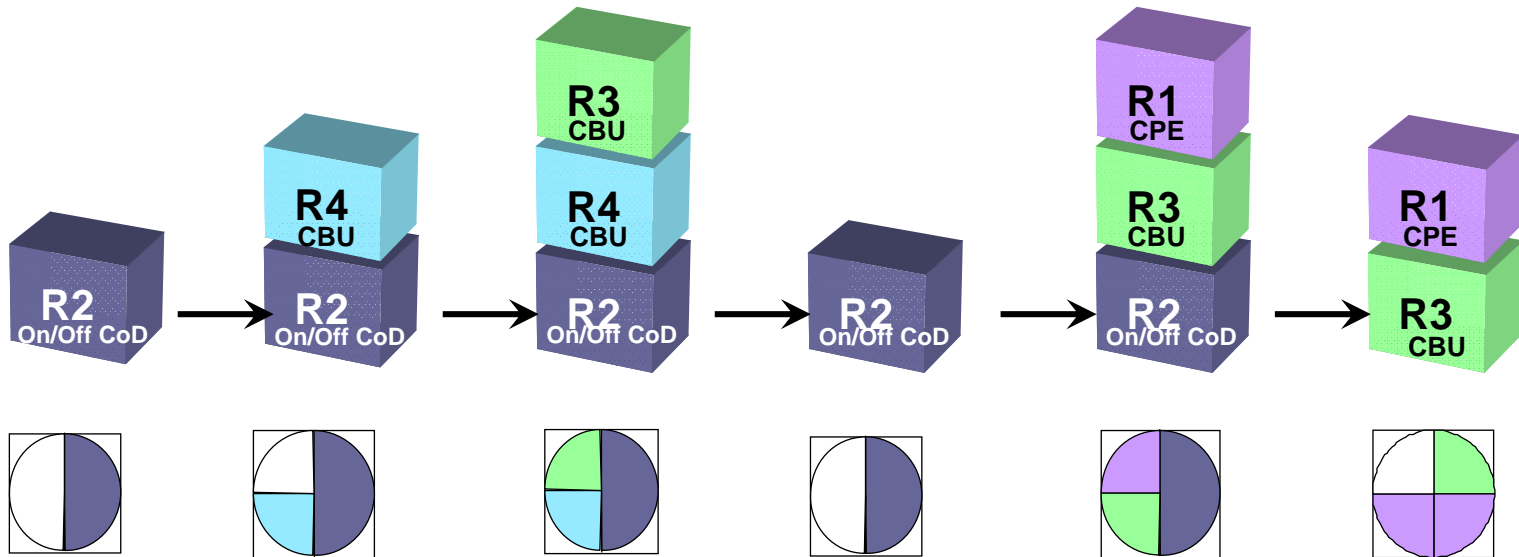- Change permanent capacity via MES order
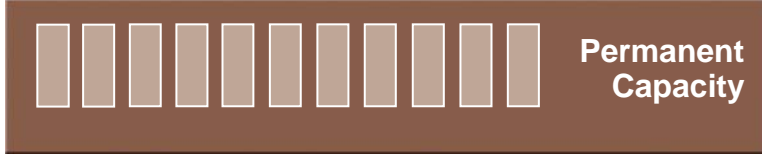
* Capacity Provisioning available with z/OS v1.9

z10 EC CoD – Activation Sequence Examples

Record and associated authorization

Activation and usage of dormant resources over time

Time

Tracking energy consumption within the infrastructure

- **ResourceLink™ provides tools to estimates server energy requirements <u>before</u> you purchase a new system or an upgrade**

- **Offers a 15% improvement in performance per KWh over z9 EC**

- **Has energy efficiency monitoring tool**
  - Introduced on IBM System z9 platform in April 2007
  - Power and thermal information displayed via the System Activity Display (SAD)

- **New IBM Systems Director Active Energy Manager (AEM) for Linux on System z V3.1**
  - Offers a single view of actual energy usage across multiple heterogeneous IBM platforms within the infrastructure
  - AEM V3.1 energy management data can be exploited by Tivoli® enterprise solutions such as IBM Tivoli Monitoring, IBM Tivoli Usage and Accounting Manager, and IBM Tivoli OMEGAMON® XE on z/OS
  - AEM V3.1 is a key component of IBM's Cool Blue™ portfolio within Project Big Green

System z10 EC Operating System Support

Operating System	ESA/390 (31-bit)	z/Architecture (64-bit)
z/OS Version 1 Releases 7[1], 8 and 9	No	Yes
Linux on System z[2], Red Hat RHEL 4, & Novell SUSE SLES 9	Yes	Yes
Linux on System z[2], Red Hat RHEL 5, & Novell SUSE SLES 10	No	Yes
z/VM Version 5 Release 2[3] and 3[3]	No	Yes
z/VSE Version 3 Release 1[2][4]	Yes	No
z/VSE Version 4 Release 1[2][5]	No	Yes
z/TPF Version 1 Release 1	No	Yes
TPF Version 4 Release 1 (ESA mode only)	Yes	No

1. **z/OS R1.7 + zIIP Web Deliverable required for z10 EC to enable HiperDispatch**
2. **Compatibility Support for listed releases. Compatibility support allows OS to IPL and operate on z10 EC**
3. **Requires Compatibility Support which allows z/VM to IPL and operate on the z10 EC providing System z9 functionality for the base OS and Guests.**
4. z/VSE v3. 31-bit mode only. It does not implement z/Architecture, and specifically does not implement 64-bit mode capabilities. z/VSE is designed to exploit select features of IBM System z10, System z9, and zSeries hardware.
5. z/VSE V4 is designed to exploit 64-bit real memory addressing, but will not support 64-bit virtual memory addressing

Note: Refer to the z/OS, z/VM, z/VSE subsets of the 2097DEVICE Preventive Planning (PSP) bucket prior to installing a z10 EC

Operating systems

z/OS

- Providing intelligent dispatching on z10 EC for performance
- Up to 64-way support
- Simplified capacity provisioning on z10 EC
- New high availability disk solution with simplified management
- Enabling extreme storage volume scaling
- Facilitating new zIIP exploitation

z/TPF

- Support for 64+ processors
- Workload charge pricing
- Exploit encryption technology

z/VSE™

- Interoperability with Linux on System z
- Exploit encryption technology
- MWLC pricing with sub-capacity option

z/VM

- Consolidation of many virtual images in a single LPAR
- Enhanced management functions for virtual images
- Larger workloads with more scaleability

Linux on System z

- Large Page Support improves performance
- Linux CPU Node Affinity is designed to avoid cache pollution
- Software support for extended CP Assist instructions AES & SHA

IBM System z10 EC - Key Dates

- **z10 EC Announce – February 26, 2008**
  - Capacity Planning Tools (zPCR, zTPM, zCP3000)
  - SAPR Guide and SA Confirmation Checklist available
    - SAPR Guide, SA06-016-00
- **Availability dates**
  - z10 EC all Models, February 26, 2008
    - Driver Level 73G
  - Model upgrades within z10 EC – May 26, 2008
  - Feature Upgrades within the z10 EC – May 26, 2008
  - Upgrades from z990, z9 EC to z10 EC – February 26, 2008
  - OSA Express3 10 GbE LR – Planned Availability*, 2Q08
  - PSIFB – InfiniBand Coupling Links for z10 EC, z9 EC and z9 BC ICF models – Planned Availability*, 2Q08
  - STP Enhancements
    - NTP Client Support – October 15, 2007
- **New ITSO Redbooks (Draft versions)**
  - z10 EC Technical Introduction, SG24-7515 - February 26, 2008
  - z10 EC Technical Guide, SG24-7516 - February 26, 2008
  - z10 EC Capacity on Demand, SG24-7504 - March, 2008
  - Getting Started with InfiniBand on z10 EC and System z9, SG24-7539 – May, 2008

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IBM System z10 Enterprise Class
Innovative Enterprise Systems Solutions, Now and in the Future

IBM System z10™ Enterprise Class enables clients to **consolidate and virtualize** their server environment…

to **reduce costs and simplify** their IT infrastructure…

with high performance, **energy efficient green technologies**,…

providing the most **resilient and secure** system to support business innovation and growth.

The Future Runs on System z

Any Qs?
Call me if and when you have one?

Parwez hamid
Senior Certified IT Specialist
parwez_hamid@uk.ibm.com
+44 20 8818 4711

z10 EC functional comparison to z9 EC

Processor / Memory		
	▪ Uniprocessor Performance	▪ 62% performance improvement over z9 EC uniprocessor *
	▪ n-way Performance	▪ On average 50% more performance than z9 EC in a n-way configuration
	▪ System Capacity	▪ 70% system capacity performance improvement over z9 EC 54-way **
	▪ Processor Design	▪ New 4.4GHz processor chip
	▪ Models	▪ z10 EC has 5 and z9 EC has 5 models, both with up to 4 books
	▪ Processing Units (PUs)	▪ z10 EC has up to 64 PUs to configure, up to 54 on z9 EC
	▪ Granular Capacity	▪ z10 EC has up to 100 Capacity settings versus 78 on the z9 EC
	▪ Memory	▪ z10 EC has up to 1.5 TB vs. up to 512 GB on z9 EC
	▪ Fixed HSA	▪ z10 EC has fixed 16 GB HSA, z9 EC had HSA carved from purchased memory

Virtualization		
	▪ LPARs	▪ z10 EC has up to 64 logical processors in an LPAR versus 54 on z9 EC
	▪ HiperDispatch	▪ z10 EC has HiperDispatch for improved synergy with z/OS Operating System to deliver scalability and performance

Connectivity		
	▪ HiperSockets	▪ z10 EC New HiperSockets Layer 2 and Multiple Write Facility
	▪ FICON for SANs	▪ Up to 336 FICON channels on z10 EC and z9 EC
	▪ Total channels	▪ Same - Up to 1024 channels
	▪ Internal I/O Bandwidth	▪ z10 EC has industry standard 6 GBps InfiniBand supports high speed connectivity and high bandwidth versus z9 EC using 2.7 GBps Self Time Interconnects (STIs)
	▪ Enhanced I/O structure	▪ Star L2 Cache Book Interconnect versus Ring Topology interconnect on z9 EC
	▪ Coupling	▪ Coupling with InfiniBand [1] – improved distance and potential cost savings
	▪ Cryptography	▪ Improved AES 192 and 256 and stronger hash algorithm with Secure Hash Algorithm (SHA-512)
	▪ LAN Connectivity	▪ New OSA-Express3[1] for 10 Gigabit Ethernet connectivity

On Demand / RAS		
	▪ Capacity Provisioning Mgr	▪ z10 EC & z/OS (1.9) for policy based advice and automation
	▪ RAS Focus	▪ z10 EC can help eliminate preplanning required to avoid scheduled outages
	▪ Just in Time deployment of Capacity	▪ Capacity on Demand offerings CBU and On/Off CoD plus new Capacity for Planned Events are resident on z10 EC

Environmentals		
	▪ Monitoring	▪ z10 EC displays energy efficiency on SAD screens
		▪ Utilizes IBM Systems Director Active Energy Manager for Linux on System z for trend calculations and management of other servers that participate

* LSPR mixed workload average running z/OS 1.8 - z10 EC 701 versus z9 EC 701

** This is a comparison of the z10 EC 64-way and the z9 EC S54 and is based on LSPR mixed workload average running z/OS 1.8

[1] Planned availability 2Q08

System z10 EC : Another innovation milestone from IBM

Comparisons of z10 EC to the acclaimed z9 EC

Capability	Percentage improvement over z9 EC (%)
New Chip Technology –higher frequency	260
Single processor	60
Maximum Server Configuration	70
Maximum Available Memory	300
Maximum Available Capacity Settings	30
Maximum Number of Usable Processor Units	20
Maximum Available sub-capacity settings	50
Maximum Number of Total Processor Units	20

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System z10 EC Compared to System z9 EC

Hardware Highlights	z10 EC	z9 EC
New Chip Technology – 2.6X	4.4 GHz	1.7 GHz
Singe processor – 1.62X (62% faster)	920 MIPS *	580 MIPS
Maximum Server Configuration – 1.7X (70% larger)	30,657 MIPS *	17,801 MIPS
Maximum Available Memory – 3X	1.5 TB	512 GB
Maximum Available Capacity Settings – 1.28X (nearly 30% more)	100	78
Maximum Number of Usable Processor Units – 1.185X (nearly 20% more)	64	54
Maximum Available sub-capacity settings – 1.5X (50% more)	36	24
Maximum Number of Total Processor Units – 1.2X (20% more)	77	64
Energy Efficiency		
z10 EC offers a 14.0% improvement in MIPS capacity per kWh *		
Pricing Highlights		
Hardware price performance improvement on z10 EC is anticipated to be 17-20% annually		
Price performance improvements in zIIPs, zAAPs and IFLS – 35% improvement		
IT savings versus x86 solutions may be up to 80%		

•*Based on LSPR final Ratings as of 1/28/08;.*

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